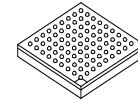


MCIMX6XxAxxxxxB
MCIMX6XxAxxxxxC

i.MX 6SoloX Automotive and Infotainment Applications Processors



Package Information
Plastic Package
BGA 19 x 19 mm, 0.8 mm pitch
BGA 17 x 17 mm, 0.8 mm pitch
BGA 14 x 14 mm, 0.65 mm pitch

| |
|-----------------------------|
| Ordering Information |
| See Table 1 on page 3 |

1 Introduction

The i.MX 6SoloX automotive and infotainment processors represent NXP Semiconductor’s latest achievement in integrated multimedia-focused products offering high-performance processing with a high degree of functional integration. These processors are designed considering the needs of the growing automotive infotainment, telematics, HMI, and display-based cluster markets.

The i.MX 6SoloX processor features NXP’s advanced implementation of the single Arm® Cortex®-A9 core, which operates at speeds of up to 800 MHz, in addition to the Arm Cortex-M4 core, which operates at speeds of up to 227 MHz. This type of heterogeneous multicore architecture provides greater levels of system integration, smart low-power system awareness, and fast real-time responsiveness. The i.MX 6SoloX includes a GPU processor capable of supporting 2D and 3D operations, a wide range of display and connectivity options, and integrated power management. Each processor provides a 32-bit DDR3/DDR3L/LPDDR2-800 memory interface and a number of other interfaces for connecting peripherals,

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such as WLAN, Bluetooth™, GPS, displays, and camera sensors.

The i.MX 6SoloX processors are specifically useful for applications such as:

- Entry-level infotainment
- Telematics

The features of the i.MX 6SoloX processors include:

- Dual-core architecture with one Arm Cortex-A9 processor plus one Arm Cortex-M4 processor—Dual-core architecture enables the device to run an open operating system like Linux on the Cortex-A9 core and an RTOS like MQX™ or FreeRTOS™ on the Cortex-M4 core. The Cortex-M4 core is standard on all i.MX 6SoloX processors.
- Multilevel memory system—The multilevel memory system of each processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processors support many types of external memory devices, including DDR3, low voltage DDR3, LPDDR2, NOR Flash, NAND Flash (MLC and SLC), OneNAND, Quad SPI, and managed NAND, including eMMC up to rev 4.4/4.41/4.5.
- Smart speed technology—Power management implemented throughout the IC that enables multimedia features and peripherals to consume minimum power in both active and various low power modes.
- Dynamic voltage and frequency scaling—The processors improve the power efficiency of devices by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—The multimedia performance of each processor is enhanced by a multilevel cache system, NEON™ MPE (Media Processor Engine) co-processor, a programmable smart DMA (SDMA) controller, and an asynchronous sample rate converter.
- 2x Gigabit Ethernet with AVB—2x 10/100/1000 Mbps Gigabit Ethernet controllers with support for Audio Video Bridging (AVB) for reliable, high-quality, low-latency multimedia streaming.
- Human-machine interface—Each processor provides a single integrated graphics processing unit that supports an OpenGL ES 2.0 and OpenVG 1.1 3D and 2D graphics accelerator. In addition, each processor provides up to two separate display interfaces (parallel display and LVDS display) and a CMOS sensor interface (parallel).
- Interface flexibility—Each processor supports connections to a variety of interfaces: High-speed USB on-the-go with PHY, high-speed USB host with PHY, High-Speed Inter-Chip USB, multiple expansion card ports (high-speed MMC/SDIO host and other), 2 Gigabit Ethernet controllers with support for Ethernet AVB, PCIe-II, two 12-bit ADC modules with 4 dedicated single-ended inputs, two CAN ports, ESAI audio interface, and a variety of other popular interfaces (such as UART, I²C, and I²S serial audio).
- Automotive environment support—Each processor includes interfaces, such as two CAN ports, an MLB25/50 port, an ESAI audio interface, and an asynchronous sample rate converter for multichannel/multisource audio.
- Advanced security—The processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. The security features are discussed in detail in the *i.MX 6SoloX Security Reference Manual* (IMX6XSRM).

- Integrated power management—The processors integrate linear regulators and internally generate voltage levels for different domains. This significantly simplifies system power management structure.

For a comprehensive list of the i.MX 6SoloX features, see [Section 1.2, “Features”](#).

1.1 Ordering Information

[Table 1](#) provides examples of orderable sample part numbers covered by this data sheet.

Table 1. Ordering Information

| Part Number | Options | Mask Set | Cortex-A9 Speed ¹ | Cortex-M4 Speed | Qualification Tier | Junction Temperature Range | Package |
|-----------------|--|----------------------|------------------------------|-----------------|--------------------|----------------------------|--|
| MCIMX6X1AVO08AB | Features not supported: - 2D&3D GPU - PCIe - LVDS | 2N19K or 3N19K | 800 MHz | 227 MHz | Automotive | -40 to +125°C | 17x17NP (NP=No PCIe) Package code “VO” 17mm x 17mm 0.8pitch Map BGA |
| MCIMX6X1AVO08AC | Features not supported: - 2D&3D GPU - PCIe - LVDS | 4N19K | 800 MHz | 227 MHz | Automotive | -40 to +125°C | 17x17NP (NP=No PCIe) Package code “VO” 17mm x 17mm 0.8pitch Map BGA |
| MCIMX6X1AVK08AB | Features not supported: - 2D&3D GPU - PCIe - LVDS | 2N19K or 3N19K | 800 MHz | 227 MHz | Automotive | -40 to +125°C | 14x14NP (NP=No PCIe) Package code “VK” 14mm x 14mm 0.65pitch Map BGA |
| MCIMX6X1AVK08AC | Features not supported: - 2D&3D GPU - PCIe - LVDS | 4N19K | 800 MHz | 227 MHz | Automotive | -40 to +125°C | 14x14NP (NP=No PCIe) Package code “VK” 14mm x 14mm 0.65pitch Map BGA |
| MCIMX6X2AVN08AB | Features not supported: - 2D&3D GPU - LVDS | 2N19K or 3N19K | 800 MHz | 227 MHz | Automotive | -40 to +125°C | 17x17WP (WP=With PCIe) Package code “VN” 17mm x 17mm 0.8pitch Map BGA |
| MCIMX6X2AVN08AC | Features not supported: - 2D&3D GPU - LVDS | 4N19K | 800 MHz | 227 MHz | Automotive | -40 to +125°C | 17x17WP (WP=With PCIe) Package code “VN” 17mm x 17mm 0.8pitch Map BGA |
| MCIMX6X4AVM08AB | Full-featured device | 2N19K or 3N19K | 800 MHz | 227 MHz | Automotive | -40 to +125°C | 19x19 Package code “VM” 19mm x 19mm 0.8pitch Map BGA |
| MCIMX6X4AVM08AC | Full-featured device | 4N19K | 800 MHz | 227 MHz | Automotive | -40 to +125°C | 19x19 Package code “VM” 19mm x 19mm 0.8pitch Map BGA |

Introduction

¹ If a 24 MHz input clock is used (required for USB), the maximum Cortex-A9 speed for 1 GHz speed grade is limited to 996 MHz and the maximum Cortex-A9 speed for 800 MHz speed grade is limited to 792 MHz.

Figure 1 describes the part number nomenclature so that the users can identify the characteristics of the specific part number they have (for example, cores, frequency, temperature grade, fuse options, and silicon revision). The primary characteristic which describes which data sheet applies to a specific part is the temperature grade (junction) field.

- The i.MX 6SoloX Automotive and Infotainment Applications Processors data sheet (IMX6SXAEC) covers parts listed with an “A (Automotive temp)”
- The i.MX 6SoloX Applications Processors for Consumer Products data sheet (IMX6SXCEC) covers parts listed with a “D (Commercial temp)” or “E (Extended Commercial temp)”
- The i.MX 6SoloX Applications Processors for Industrial Products data sheet (IMX6SXIEC) covers parts listed with “C (Industrial temp)”

Ensure to have the proper data sheet for specific part by verifying the temperature grade (junction) field and matching it to the proper data sheet. If there will be any questions, visit see the web page nxp.com/imx6series or contact a NXP representative for details.

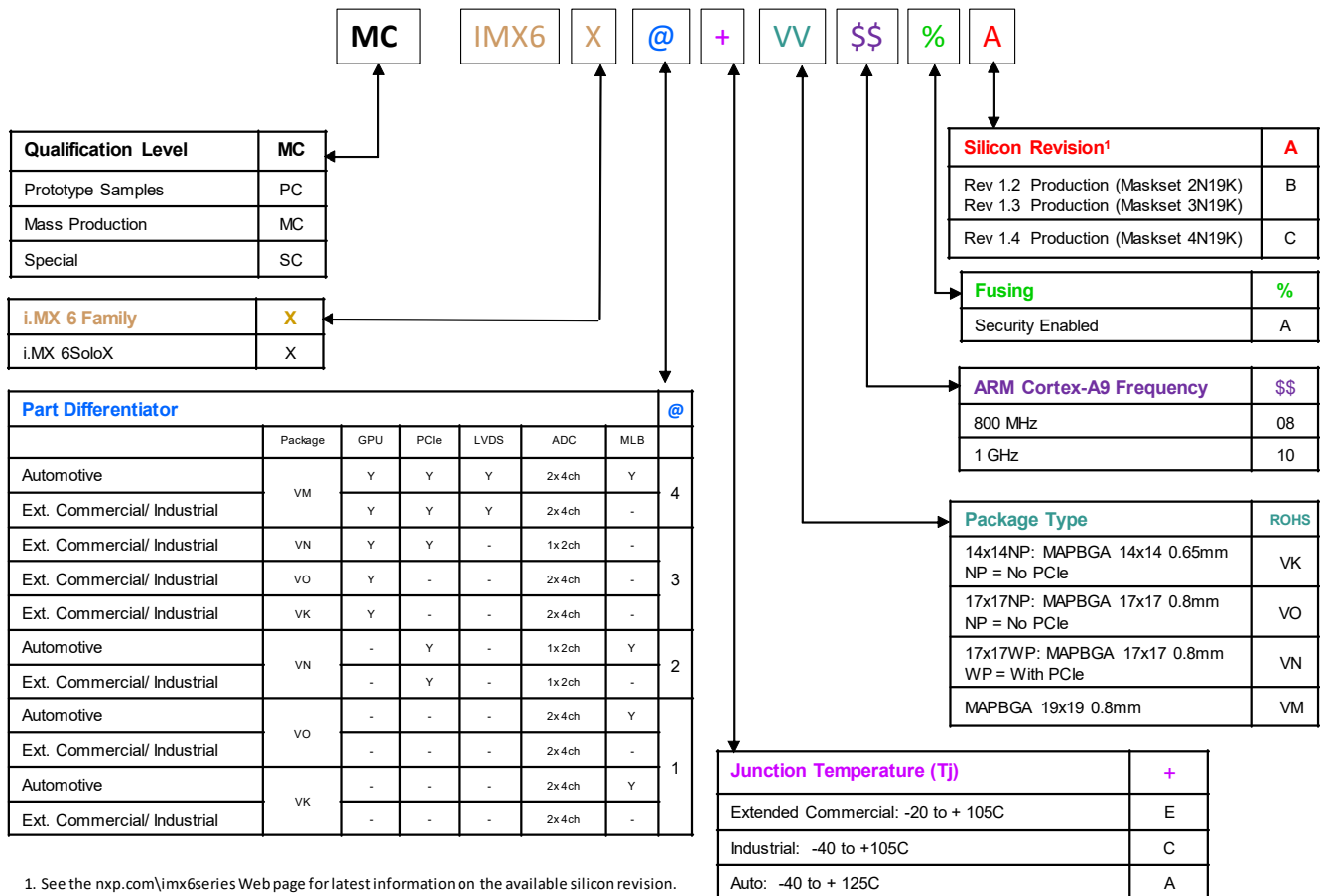


Figure 1. Part Number Nomenclature—i.MX 6SoloX

1.2 Features

The i.MX 6SoloX processors are based on the Arm Cortex-A9 MPCore™ platform, which has the following features:

- Supports single Arm Cortex-A9 MPCore processor (with TrustZone)
- The core configuration is symmetric, where each core includes:
 - 32 KByte L1 Instruction Cache
 - 32 KByte L1 Data Cache
 - Private Timer and Watchdog
 - Cortex-A9 NEON MPE (Media Processing Engine) coprocessor

The Arm Cortex-A9 MPCore complex includes:

- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- 256 KB unified I/D L2 cache:
 - Two Master AXI bus interfaces output of L2 cache
- Frequency of the core (including NEON coprocessor and L1 cache), as per [Table 10, “Operating Ranges,” on page 26](#).
- NEON MPE coprocessor
 - SIMD Media Processing Architecture
 - NEON register file with 32x64-bit general-purpose registers
 - NEON Integer execute pipeline (ALU, Shift, MAC)
 - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
 - NEON load/store and permute pipeline
 - 32 double-precision VFPv3 floating point registers

The Arm Cortex-M4 platform:

- Cortex-M4 CPU core
- MPU (Memory Protection Unit)
- FPU (Floating Point Unit)
- 16 KByte Instruction Cache
- 16 KByte Data Cache
- 64 KByte TCM (Tightly-Coupled Memory)

The SoC-level memory system consists of the following additional components:

- Boot ROM, including HAB (96 KB)
- Internal multimedia / shared, fast access RAM (OCRAM, 128 KB)
- Internal RAM for state retention or general use (OCRAM_S, 16KB)
- Secure/non-secure RAM (32 KB)

Introduction

- External memory interfaces: The i.MX 6SoloX processors support latest, high volume, cost effective handheld DRAM, NOR, and NAND Flash memory standards.
 - 16/32-bit LPDDR2-800, 16/32-bit DDR3-800 and DDR3L-800
 - 16-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size, BA-NAND, PBA-NAND, LBA-NAND, OneNAND and others. BCH ECC up to 62 bits. 16-bit boot is supported from OneNAND. 8-bit boot is supported from other NAND types.
 - 16/32-bit NOR Flash. All EIMv2 pins are muxed on other interfaces.

Each i.MX 6SoloX processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Displays—Total three interfaces available.
 - Two parallel 24-bit display ports, each up to 1080P at 60 Hz
 - LVDS serial port—One port up to 85 MP/sec (for example, WXGA at 60 Hz)
- Camera sensors:
 - Two parallel camera ports (up to 24 bit and up to 133 MHz peak)
- Expansion cards:
 - Four MMC/SD/SDIO card ports all supporting:
 - 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR-104 mode (104 MB/s max)
 - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 200 MHz in HS200 mode (200 MB/s max)
- USB:
 - Two high speed (HS) USB 2.0 OTG (Up to 480 Mbps), with integrated HS USB Phy
 - One HS-IC USB (High-Speed Inter-Chip USB) host
- Expansion PCI Express port (PCIe) v2.0 one lane
 - PCI Express (Gen 2.0) dual mode complex, supporting Root complex operations and Endpoint operations. Uses x1 PHY configuration.
- Miscellaneous IPs and interfaces:
 - Three SSIs and two SAIs supporting up to five I2S or AC97 ports
 - Enhanced Serial Audio Interface (ESAI)
 - Sony Philips Digital Interconnect Format (SPDIF), Rx and Tx
 - Audio MUX (AUDMUX)
 - Medium Quality Sound (MQS) module provides an opportunity for BOM cost reduction if high-quality sound is not required
 - Six UARTs, up to 5.0 Mbps each:
 - Providing RS232 interface
 - Supporting 9-bit RS485 multidrop mode
 - One of the six UARTs (UART1) supports 8-wire while others support 4-wire. This is due to the SoC IOMUX limitation, since all UART IPs are identical.
 - Five eCSPI (Enhanced CSPI)

- Four I²C
- Two Gigabit Ethernet Controllers (designed to be compatible with IEEE AVB standards and IEEE Std 1588®), 10/100/1000 Mbps
- Eight Pulse Width Modulators (PWM)
- System JTAG Controller (SJC)
- GPIO with interrupt capabilities
- 8x8 Key Pad Port (KPP)
- Two Quad SPIs
- Two Flexible Controller Area Network (FlexCAN), 1 Mbps each
- Three Watchdog timers (WDOG)
- Up to two 4-channel, 12-bit Analog to Digital Converters (ADC), VM, VO, VK packages
- One 2-channel, 12-bit Analog to Digital Converter (ADC), VN package
- MLB (MediaLB) provides interface to MOST Networks (MOST25, MOST50)

The i.MX 6SoloX processors integrate advanced power management unit and controllers:

- Provide PMU, including LDO supplies, for on-chip resources
- Use Temperature Sensor for monitoring the die temperature
- Support DVFS techniques for low power modes
- Use software state retention and power gating for Arm Cortex-A9 CPU core, the Arm Cortex-M4 CPU core, and the Arm NEON MPE coprocessor.
- Support various levels of system power modes
- Use flexible clock gating control scheme

The i.MX 6SoloX processors use dedicated hardware accelerators to meet the targeted multimedia performance. The use of hardware accelerators is a key factor in obtaining high performance at low power consumption, while having the CPU core relatively free for performing other tasks.

The i.MX 6SoloX processors incorporate the following hardware accelerators:

- GPU—2D (BitBlit) and 3D (OpenGL ES) Graphics Processing Unit
- PXP—PiXel Processing Pipeline for image resize, rotation, overlay and CSC. Off loading key pixel processing operations are required to support the LCD display applications.
- ASRC—Asynchronous Sample Rate Converter

Security functions are enabled and accelerated by the following hardware:

- Arm TrustZone including the TZ architecture (separation of interrupts, memory mapping, etc.)
- SJC—System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- CAAM—Cryptographic Acceleration and Assurance Module, containing cryptographic and hash engines, 32 KB secure RAM, and True and Pseudo Random Number Generator (NIST certified).
- SNVS—Secure Non-Volatile Storage, including Secure Real Time Clock
- CSU—Central Security Unit. Enhancement for the IC Identification Module (IIM). Will be configured during boot and by eFUSES and will determine the security level operation mode as well as the TZ policy.

Introduction

- A-HAB—Advanced High Assurance Boot—HABv4 with the new embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization.

NOTE

The actual feature set depends on the part numbers as described in [Table 1](#). Functions, such as display and camera interfaces, connectivity interfaces, video hardware acceleration, and 2D and 3D hardware graphics acceleration may not be enabled for specific part numbers.

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6SoloX processor system.

2.1 Block Diagram

Figure 2 shows the functional modules in the i.MX 6SoloX processor system.

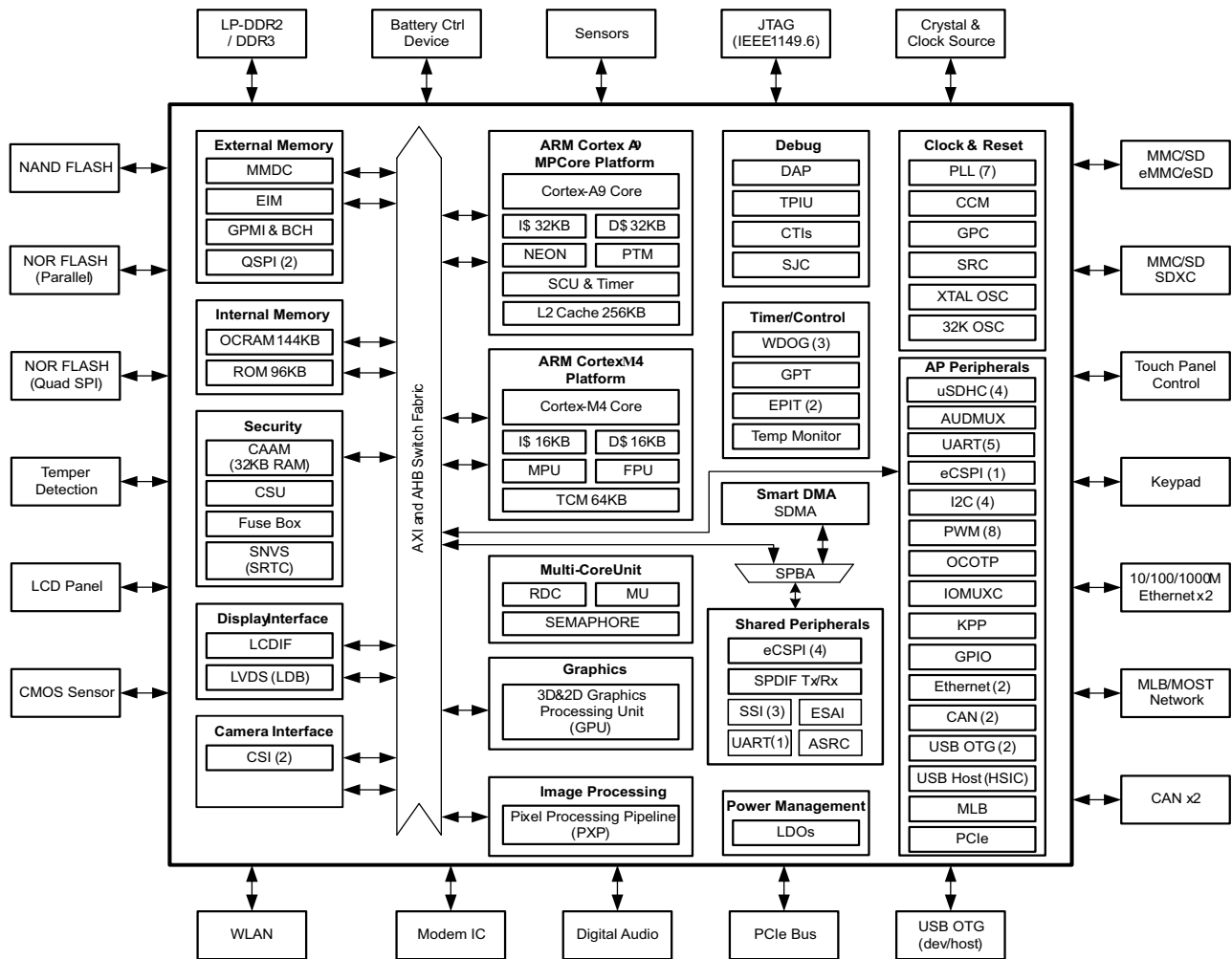


Figure 2. i.MX 6SoloX System Block Diagram

NOTE

The numbers in brackets indicate number of module instances. For example, PWM (8) indicates eight separate PWM peripherals.

3 Modules List

The i.MX 6SoloX processors contain a variety of digital and analog modules. [Table 2](#) describes these modules in alphabetical order.

Table 2. i.MX 6SoloX Modules List

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|-------------------|---|-----------------------------------|---|
| ADC1 ADC2 | Analog to Digital Converter | — | The ADC is a 12-bit general purpose analog to digital converter. |
| ARM | ARM Platform | Arm | The ARM Core Platform includes 1x Cortex-A9 and 1x Cortex-M4 cores. It also includes associated sub-blocks, such as the Level 2 Cache Controller, SCU (Snoop Control Unit), GIC (General Interrupt Controller), private timers, watchdog, and CoreSight debug modules. |
| ASRC | Asynchronous Sample Rate Converter | Multimedia Peripherals | The Asynchronous Sample Rate Converter (ASRC) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversion of up to 10 channels of about -120dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs. |
| AUDMUX | Digital Audio Mux | Multimedia Peripherals | The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports. |
| BCH | Binary-BCH ECC Processor | System Control Peripherals | The BCH module provides up to 62-bit ECC for NAND Flash controller (GPMI). |
| CAAM | Cryptographic accelerator and assurance module | Security | CAAM is a cryptographic accelerator and assurance module. CAAM implements several encryption and hashing functions, a run-time integrity checker, and a Pseudo Random Number Generator (PRNG). The pseudo random number generator is certified by Cryptographic Algorithm Validation Program (CAVP) of National Institute of Standards and Technology (NIST). Its DRBG validation number is 94 and its SHS validation number is 1455. CAAM also implements a Secure Memory mechanism. In i.MX 6SoloX processors, the security memory provided is 32 KB. |
| CCM GPC SRC | Clock Control Module, GeneralPowerController, System Reset Controller | Clocks, Resets, and Power Control | These modules are responsible for clock and reset distribution in the system, and also for the system power management. |
| CSI | Parallel CSI | Multimedia Peripherals | The CSI IP provides parallel CSI standard camera interface port. The CSI parallel data ports are up to 24 bits. It is designed to support 24-bit RGB888/YUV444, CCIR656 video interface, 8-bit YCbCr, YUV or RGB, and 8-bit/10-bit/26-bit Bayer data input. |

Table 2. i.MX 6SoloX Modules List (continued)

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|--|-----------------------------------|----------------------------|--|
| CSU | Central Security Unit | Security | The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 6SoloX platform. |
| CTI | Cross Trigger Interfaces | Debug/Trace | Cross Trigger Interfaces allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A9 Core Platform. |
| DAP | Debug Access Port | System Control Peripherals | The DAP provides real-time access for the debugger without halting the core to: System memory and peripheral registers All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A9 Core Platform. |
| DBGMON | Debug Monitor | Debug | DBGMON is a real-time debug monitor to record last AXI transaction before system reset. |
| eCSPI1 eCSPI2 eCSPI3 eCSPI4 eCSPI5 | Configurable SPI | Connectivity Peripherals | Full-duplex enhanced Synchronous Serial Interface. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals. |
| EIM | NOR-Flash /PSRAM interface | Connectivity Peripherals | The EIM NOR-FLASH / PSRAM provides: Support 16-bit (in muxed IO mode only) PSRAM memories (sync and async operating modes), at slow frequency Support 16-bit (in muxed IO mode only) NOR-Flash memories, at slow frequency Multiple chip selects |
| ENET1 ENET2 | Ethernet Controller | Connectivity Peripherals | The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the i.MX 6SoloX Applications Processor Reference Manual (IMX6SXR) for details. |
| EPIT1 EPIT2 | Enhanced Periodic Interrupt Timer | Timer Peripherals | Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly. |

Table 2. i.MX 6SoloX Modules List (continued)

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|---|----------------------------------|-------------------------------|---|
| ESAI | Enhanced Serial Audio Interface | Connectivity Peripherals | The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. All serial transfers are synchronized to a clock. Additional synchronization signals are used to delineate the word frames. The normal mode of operation is used to transfer data at a periodic rate, one word per period. The network mode is also intended for periodic transfers; however, it supports up to 32 words (time slots) per period. This mode can be used to build time division multiplexed (TDM) networks. In contrast, the on-demand mode is intended for non-periodic transfers of data and to transfer data serially at high speed when the data becomes available. The ESAI has 12 pins for data and clocking connection to external devices. |
| FLEXCAN1 FLEXCAN2 | Flexible Controller Area Network | Connectivity Peripherals | The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames. |
| Fuse Box | Electrical Fuse Array | Security | Electrical Fuse Array. Enables setup of boot modes, security levels, security keys, and many other system parameters. The fuses are accessible through OCOTP_CTRL interface. |
| GC400T | Graphics Engine | Multimedia Peripherals | The GC400T is a graphics engine with separate 2D and 3D pipelines to provide both 2D and 3D acceleration. It supports DirectFB and GAL APIs. It supports OpenGL ES1.1/2.0 and OpenVG 1.1 APIs. |
| GIC | Global Interrupt Controller | Arm/Control | The Global Interrupt Controller (GIC) collects interrupt requests from all i.MX 6SoloX sources and routes them to the Arm MPCore(s). Each interrupt can be configured as a normal or a secure interrupt. Software Force Registers and software Priority Masking are also supported. This IP is part of the Arm Core complex. |
| GIS | General Interrupt Service module | Camera, Display, & Graphics | GIS can be used to automate the flow of data from the camera to the display. |
| GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6 GPIO7 | General Purpose I/O Modules | System Control Peripherals | Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O. |

Table 2. i.MX 6SoloX Modules List (continued)

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|----------------------------------|----------------------------------|-------------------------------------|--|
| GPMI | General Purpose Memory Interface | Connectivity Peripherals | The GPMI module supports up to 8x NAND devices and 60-bit ECC encryption/decryption for NAND Flash Controller (GPMI2). GPMI supports separate DMA channels for each NAND device. |
| GPT | General Purpose Timer | Timer Peripherals | Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either with an external clock or an internal clock. |
| I2C-1 I2C-2 I2C-3 I2C-4 | I2C Interface | Connectivity Peripherals | I2C provide serial interface for external devices. Data rates of up to 400 kbps are supported. |
| IOMUXC | IOMUX Control | System Control Peripherals | This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable. |
| KPP | Key Pad Port | Connectivity Peripherals | KPP Supports 8x8 external key pad matrix. KPP features are: <ul style="list-style-type: none"> • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection |
| LCDIF | LCD Interface | Multimedia Peripherals | The LCDIF provides display data for external LCD panels from simple text-only displays to WVGA, 16/18/24 bpp color TFT panels. The LCDIF supports all of these different interfaces by providing fully programmable functionality and sharing register space, FIFOs, and ALU resources at the same time. The LCDIF supports RGB (DOTCLK) modes as well as system mode including both VSYNC and WSYNC modes. |
| LVDS (LDB) | LVDS Display Bridge | Connectivity Peripherals | LVDS Display Bridge is used to connect an external LVDS display interface. LDB supports the following signals: <ul style="list-style-type: none"> • One clock pair • Four data pairs |
| MLB | MediaLB | Connectivity/Multimedia Peripherals | The MLB interface module provides a link to a MOST® data network, using the standardized MediaLB protocol (MOST25, MOST 50). |
| MMDc | Multi-Mode DDR Controller | Connectivity Peripherals | DDR Controller supports 16/32-bit LPDDR2-800, DDR3-800 and DDR3L-800. |

Table 2. i.MX 6SoloX Modules List (continued)

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|--|----------------------------------|--|--|
| MU | Messaging Unit | Interprocessor Communication & Synchronization | The MU module supports interprocessor communication between the Cortex-A9 and Cortex-M4 cores. |
| OCOTP_CTRL | OTP Controller | Security | The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically-programmable (eFUSE) polyfuses. The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non-volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals, requiring permanent non-volatility. |
| OCRAM | On-Chip Memory Controller | Data Path | The On-Chip Memory controller (OCRAM) module is designed as an interface between system's AXI bus and internal (on-chip) SRAM memory module. |
| OCRAM 128 KB | Internal RAM | Internal Memory | Internal RAM, which is accessed through OCRAM memory controller. |
| OCRAM_S 16KB | Secure/nonsecure RAM | Secured Internal Memory | Secure/nonsecure internal RAM, interfaced through the CAAM. OCRAM_S can be used by software for state retention of the CPU and other hardware blocks. |
| OSC32KHz | OSC32KHz | Clocking | Generates 32.768 KHz clock from external crystal. |
| PCIe | PCI Express 2.0 | Connectivity Peripherals | The PCIe IP provides PCI Express Gen 2.0 functionality. |
| PMU | Power-Management functions | Data Path | Integrated power management unit. Used to provide power to various SoC domains. |
| PWM-1 PWM-2 PWM-3 PWM-4 PWM-5 PWM-6 PWM-7 PWM-8 | Pulse Width Modulation | Connectivity Peripherals | The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound. |
| PXP | PiXel Processing Pipeline | Display Peripherals | A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma-mapping, and rotation. The PXP is enhanced with features specifically for gray scale applications. |
| QSPI | Quad Serial Peripheral Interface | Connectivity Peripherals | The Quad Serial Peripheral Interface (QuadSPI) block acts as an interface to one or two external serial flash devices, each with up to four bidirectional data lines. |
| ROM 96KB | Boot ROM | Internal Memory | Supports secure and regular boot modes |

Table 2. i.MX 6SoloX Modules List (continued)

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|----------------|----------------------------|------------------------------|--|
| RDC | Resource Domain Controller | Multicore Isolation/Sharing | RDC module supports domain-based access control to shared resources. |
| SEMA4 | Semaphore | Multicore/Isolation /Sharing | Supports hardware-enforced semaphores. |
| SEMA42 | Semaphore | Multicore/Isolation /Sharing | SEMA42 is similar to SEMA4 with the following key differences: SEMA42 increases the number of access domains from 2 to 15 SEMA42 does not have interrupt to indicate semaphore release RDC programming model supports the option to require hardware semaphore for peripherals shared between domains. Signaling between the SEMA42 and RDC binds peripherals to semaphore gates within SEMA42. |
| SAI1 SAI2 | — | — | The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces. |
| SDMA | Smart Direct Memory Access | System Control Peripherals | The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features: Powered by a 16-bit Instruction-Set micro-RISC engine Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels 48 events with total flexibility to trigger any combination of channels Memory accesses including linear, FIFO, and 2D addressing Shared peripherals between ARM and SDMA Very fast Context-Switching with 2-level priority based preemptive multi-tasking DMA units with auto-flush and prefetch capability Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) DMA ports can handle unit-directional and bi-directional flows (copy mode) Up to 8-word buffer for configurable burst transfers for EMIv2.5 Support of byte-swapping and CRC calculations Library of Scripts and API is available |

Table 2. i.MX 6SoloX Modules List (continued)

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|--|--|-------------------------------|--|
| SJC | System JTAG Controller | System Control Peripherals | The SJC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX 6SoloX processors use JTAG port for production, testing, and system debugging. In addition, the SJC provides BSR (Boundary Scan Register) standard support, which complies with IEEE1149.1 and IEEE1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX 6SoloX SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration. |
| SNVS | Secure Non-Volatile Storage | Security | Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting. |
| SPDIF | Sony Philips Digital Interconnect Format | Multimedia Peripherals | A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. Has Transmitter and Receiver functionality. |
| SSI1 SSI2 SSI3 | I2S/SSI/AC97 Interface | Connectivity Peripherals | The SSI is a full-duplex synchronous interface, which is used on the AP to provide connectivity with off-chip audio peripherals. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock / frame sync options. The SSI has two pairs of 8x24 FIFOs and hardware support for an external DMA controller in order to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream that reduces CPU overhead in use cases where two time slots are being used simultaneously. |
| TEMPMON | Temperature Monitor | System Control Peripherals | The Temperature sensor IP is used for detecting die temperature. The temperature read out does not reflect case or ambient temperature. It reflects the temperature in proximity of the sensor location on the die. Temperature distribution may not be uniformly distributed, therefore the read out value may not be the reflection of the temperature value of the entire die. |
| TZASC | Trust-Zone Address Space Controller | Security | The TZASC (TZC-380 by Arm) provides security address region control functions required for intended application. It is used on the path to the DRAM controller. |
| UART1 UART2 UART3 UART4 UART5 UART6 | UART Interface | Connectivity Peripherals | Each of the UARTv2 modules support the following serial data transmit/receive protocols and configurations: <ul style="list-style-type: none"> • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 5 Mbps. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • Option to operate as 8-pins full UART, DCE, or DTE • UART1/6 support 8-pin, UART2/3/4/5 support 4-pin |

Table 2. i.MX 6SoloX Modules List (continued)

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|--------------------------------------|---|--------------------------------------|--|
| uSDHC1 uSDHC2 uSDHC3 uSDHC4 | SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller | Connectivity Peripherals | <p>i.MX 6SoloX specific SoC characteristics: All four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are:</p> <ul style="list-style-type: none"> Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.5/4.2/4.3/4.4/4.41/ including high-capacity (size > 2 GB) cards HC MMC. Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDHC cards up to 32 GB. Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v3.0. Conforms to the SD Host Controller Standard Specification version 3.0. <p>All four ports support:</p> <ul style="list-style-type: none"> 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) All ports can work with 1.8 V and 3.3 V cards. Each port is placed on a separate power domain. |
| USB | Universal Serial Bus 2.0 | Connectivity Peripherals | <p>USBOH3 contains:</p> <ul style="list-style-type: none"> Two high-speed OTG 2.0 modules with integrated HS USB PHYs One high-speed Host module connected to HSIC USB port |
| WDOG1 WDOG3 | Watch Dog | Timer Peripherals | The Watch Dog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the Arm core, and a second point evokes an external event on the WDOG line. |
| WDOG2 (TZ) | Watch Dog (TrustZone) | Timer Peripherals | The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode software. |
| XTALOSC | Crystal Oscillator Interface | Clocks, Resets, and Power Control | The XTALOSC module connects to an external crystal to provide system clocks. |

3.1 Special Signal Considerations

Table 3 lists special signal considerations for the i.MX 6SoloX processors. The signal names are listed in alphabetical order.

The package contact assignments can be found in Section 6, “Package Information and Contact Assignments.” Signal descriptions are provided in the *i.MX 6SoloX Applications Processor Reference Manual (IMX6SXRM)*.

Table 3. Special Signal Considerations

| Signal Name | Remarks |
|---------------------------------------|---|
| CCM_CLK1_P/ CCM_CLK1_N CCM_CLK2 | <p>Two general purpose differential high speed clock Input/outputs are provided. Any or both of them could be used:</p> <ul style="list-style-type: none"> To feed external reference clock to the PLLs and further to the modules inside SoC, for example as alternate reference clock for PCIe, Video/Audio interfaces, etc. To output internal SoC clock to be used outside the SoC as either reference clock or as a functional clock for peripherals <p>See the <i>i.MX 6SoloX Applications Processor Reference Manual (IMX6SXRM)</i> for details on the respective clock trees.</p> <p>The clock inputs/outputs are LVDS differential pairs compatible with TIA/EIA-644 standard, the frequency range supported is 0...600 MHz.</p> <p>Alternatively one may use single ended signal to drive CLKx_P input. In this case corresponding CLKx_N input should be tied to the constant voltage level equal 1/2 of the input signal swing. Termination should be provided in case of high frequency signals.</p> <p>See LVDS pad electrical specification for further details.</p> <p>After initialization, the CLKx inputs/outputs could be disabled (if not used). If unused any or both of the CLKx_N/P pairs may be left unconnected.</p> |
| RTC_XTALI/RTC_XTALO | <p>If the user needs to configure RTC_XTALI and RTC_XTALO as an RTC oscillator, a 32.768 kHz crystal (≤ 100 kΩ ESR, 10 pF load), should be connected between RTC_XTALI and RTC_XTALO. Keep in mind the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from RTC_XTALI and RTC_XTALO to either power or ground (> 100 MΩ). This will debias the amplifier and cause a reduction of startup margin. Typically RTC_XTALI and RTC_XTALO should bias to approximately 0.5 V.</p> <p>If it is desired to feed an external low frequency clock into RTC_XTALI the RTC_XTALO pin should be left unconnected or driven with a complimentary signal. The logic level of this forcing clock should not exceed VDD_SNVS_CAP level and the frequency should be < 100 kHz under typical conditions.</p> <p>When a high accuracy real time clock is not required, the system can use an internal low frequency ring oscillator. It is recommended to connect RTC_XTALI to GND and leave RTC_XTALO unconnected.</p> |
| XTALI/XTALO | <p>A 24.0 MHz crystal should be connected between XTALI and XTALO. NXP BSP (board support package) software requires 24 MHz on XTALI/XTALO. For details on crystal selection, see the “i.MX 6SoloX Design Checklist” chapter of the <i>Hardware Development Guide for i.MX 6SoloX Applications Processors (IMX6SXHDG)</i>, as well as the engineering bulletin <i>i.MX 6 Series Crystal Drive (24 MHz)</i> (EB830).</p> <p>The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTALI must be directly driven by the external oscillator and XTALO is left unconnected.</p> <p>If this clock is used as a reference for USB and PCIe, then there are strict frequency tolerance and jitter requirements. See OSC24M chapter and relevant interface specifications chapters for details.</p> |

Table 3. Special Signal Considerations (continued)

| Signal Name | Remarks |
|-------------|--|
| DRAM_VREF | When using DDR_VREF with DDR I/O, the nominal reference voltage must be half of the NVCC_DRAM supply. The user must tie DDR_VREF to a precision external resistor divider. Use a 1 k Ω 0.5% resistor to GND and a 1 k Ω 0.5% resistor to NVCC_DRAM. Shunt the resistor from DRAM_VREF to ground with a closely mounted 0.1 μ F capacitor. To reduce supply current, a pair of 1.5 k Ω 0.1% resistors can be used. Using resistors with recommended tolerances ensures the \pm 2% DDR_VREF tolerance (per the DDR3 specification) is maintained when four DDR3 ICs plus the i.MX 6SoloX are drawing current on the resistor divider. |
| ZQPAD | DRAM calibration resistor 240 Ω 1% used as reference during DRAM output buffer driver calibration should be connected between this pad and GND. |
| NVCC_LVDS | On the 19 x 19 package, this ball can be shorted to VDD_HIGH_CAP on the circuit board. On the 17 x 17 and 14 x 14 packages, NVCC_LVDS is internally connected to VDD_HIGH_CAP. |
| GPANAIO | Analog output for NXP use only. This output must always be left unconnected. |
| JTAG_nnnn | The JTAG interface is summarized in Table 4 . Use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is followed. For example, do not use an external pull down on an input that has on-chip pull-up. JTAG_TDO is configured with a keeper circuit such that the floating condition is eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental and should be avoided. JTAG_MOD is referenced as SJC_MOD in the i.MX 6SoloX Applications Processor Reference Manual (IMX6SRM) . Both names refer to the same signal. JTAG_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 k Ω) is allowed. JTAG_MOD set to high configures the JTAG interface to mode compliant with IEEE1149.1 standard. JTAG_MOD set to low configures the JTAG interface for common software debug adding all the system TAPs to the chain. |
| NC | These signals are No Connect (NC) and should be left unconnected by the user. |
| POR_B | This cold reset negative logic input resets all modules and logic in the IC. |
| ONOFF | ONOFF can be configured in debounce, off to on time, and max timeout configurations. The debounce and off to on time configurations supports 0, 50, 100 and 500 msecs. Debounce is used to generate the power off interrupt. While in the ON state, if ONOFF button is pressed longer than the debounce time, the power off interrupt is generated. Off to on time supports the time it takes to request power on after a configured button press time has been reached. While in the OFF state, if ONOFF button is pressed longer than the off to on time, the state will transition from OFF to ON. Max timeout configuration supports 5, 10, 15 secs and disable. Max timeout configuration supports the time it takes to request power down after ONOFF button has been pressed for the defined time. |
| TEST_MODE | TEST_MODE is for NXP factory use. The user must tie this pin directly to GND. |
| PCIE_REXT | The impedance calibration process requires connection of reference resistor 200 Ω 1% precision resistor on PCIE_REXT pad to ground. |

Table 4. JTAG Controller Interface Summary

| JTAG | I/O Type | On-chip Termination |
|----------|----------|-----------------------|
| JTAG_TCK | Input | 47 k Ω pull-up |
| JTAG_TMS | Input | 47 k Ω pull-up |
| JTAG_TDI | Input | 47 k Ω pull-up |

Table 4. JTAG Controller Interface Summary (continued)

| JTAG | I/O Type | On-chip Termination |
|------------|----------------|---------------------|
| JTAG_TDO | 3-state output | Keeper |
| JTAG_TRSTB | Input | 47 kΩ pull-up |
| JTAG_MOD | Input | 100 kΩ pull-up |

3.2 Recommended Connections for Unused Analog Interfaces

The recommended connections for unused analog interfaces can be found in the section, “Unused analog interfaces,” of the Hardware Development Guide for i.MX 6SoloX Applications Processors (IMX6SXHDG).

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX 6SoloX processors.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See [Table 5](#) for a quick reference to the individual tables and sections.

Table 5. i.MX 6SoloX Chip-Level Conditions

| For these characteristics, ... | Topic appears ... |
|--|----------------------------|
| Absolute Maximum Ratings | on page 21 |
| Thermal Resistance | on page 23 |
| Operating Ranges | on page 26 |
| External Clock Sources | on page 29 |
| Maximum Supply Currents | on page 30 |
| Low Power Mode Supply Currents | on page 31 |
| USB PHY Current Consumption | on page 32 |
| PCIe 2.0 Power Consumption | on page 33 |

4.1.1 Absolute Maximum Ratings

CAUTION

Stresses beyond those listed under [Table 6](#) may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[Table 6](#) shows the absolute maximum operating ratings.

Table 6. Absolute Maximum Ratings

| Parameter Description | Symbol ¹ | Min | Max | Unit |
|---|---|------|--------------------|------|
| Core Supplies Input Voltage (LDO Enabled) | VDDSOC_IN VDDARM_IN | -0.3 | 1.6 | V |
| Core Supplies Input Voltage (LDO Bypass) | VDDSOC_IN VDDARM_IN | -0.3 | 1.4 | V |
| VDD_HIGH_IN Supply voltage (LDO Enabled) | VDD_HIGH_IN | -0.3 | 3.7 | V |
| VDD_HIGH_IN Supply voltage (LDO Bypass) | VDD_HIGH_IN | -0.3 | 2.85 | V |
| MLB I/O Supply Voltage | Supplies denoted as I/O Supply | -0.3 | 2.8 | V |
| Core Supplies Output Voltage (LDO Enabled) | VDD_ARM_CAP VDD_SOC_CAP | -0.3 | 1.4 | V |
| VDD_HIGH_CAP LDO Output Supply voltage | VDD_HIGH_CAP | -0.3 | 2.6 | V |
| Supply Input Voltage to Secure Non-Volatile Storage and Real Time Clock | VDD_SNVS_IN | -0.3 | 3.6 | V |
| USB VBUS Supply | USB_OTG_VBUS | — | 5.6 | V |
| Input voltage on USB signals (non-VBUS) | USB_OTG_DP, USB_OTG_DN, USB_H1_DP, USB_H1_DN, USB_OTG_CHD_B | -0.3 | 3.63 | V |
| Supply for the USB HSIC interface | NVCC_USB_H | — | 2.85 | V |
| IO Supply for DDR Interface | NVCC_DRAM | -0.4 | 1.975 ² | V |
| Supply for DDR pre-drivers | NVCC_DRAM_2P5 | -0.3 | 2.85 | V |
| IO Supply for RGMII Interface | NVCC_RGMII | -0.5 | 3.7 | V |

Table 6. Absolute Maximum Ratings (continued)

| Parameter Description | Symbol ¹ | Min | Max | Unit |
|--|---|------|----------------|------|
| IO Supply for GPIO Type Pins | NVCC_CSI NVCC_ENET NVCC_HIGH NVCC_KEY NVCC_GPIO NVCC_LCD NVCC_LOW NVCC_NAND NVCC_QSPI NVCC_SD NVCC_JTAG | -0.5 | 3.7 | V |
| IO Supply for LVDS | NVCC_LVDS | -0.3 | 2.85 | V |
| IO Supply for MLB | Supplies denoted as GPIO supplies | -0.3 | 2.9 | V |
| VP Supplies for PCIe | PCIE_VP | -0.3 | 1.4 | V |
| VPH Supplies for PCIe | PCIE_VPH | -0.3 | 2.85 | V |
| Supply for PCIe PHY | PCIE_VPTX | -0.3 | 1.4 | V |
| Supply for ADC 3P3V | VDDA_ADC_3P3 | — | 3.7 | V |
| 3.3V Supply for analog circuitry | VDD_AFE_3P3 | — | 3.7 | V |
| Input/Output Voltage Range (non-DDR pins) | V_{in}/V_{out} | -0.5 | $OVDD+0.3^3$ | V |
| Input/Output Voltage Range (DDR pins) | V_{in}/V_{out} | -0.5 | $OVDD^3+0.4^2$ | V |
| ESD damage Immunity: Human Body Model (HBM) | V_{esd_HBM} | — | 2000 | V |
| ESD damage Immunity: Charge Device Model (CDM) | V_{esd_CDM} | — | 500 | V |
| Storage Temperature Range | TSTORAGE | -40 | 150 | °C |

¹ Not all of the supplies shown exist on all packages. See the package ball maps for details on which supplies are used on each package.

² The absolute maximum voltage includes an allowance for 400 mV of overshoot on the IO pins. Per JEDEC standards, the allowed signal overshoot must be de-rated if NVCC_DRAM exceeds 1.575V.

³ OVDD is the I/O supply voltage.

4.1.2 Thermal Resistance

NOTE

Per JEDEC JESD51-2, the intent of thermal resistance measurements is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.

4.1.2.1 19x19 mm (VM) Package Thermal Resistance

Table 7 displays the 19x19 mm (VM) package thermal resistance data.

Table 7. 19x19 mm (VM) Package Thermal Resistance Data

| Rating | Test Conditions | Symbol | Value | Unit | Notes |
|--|-------------------------|------------------|-------|------|-------|
| Junction to Ambient Natural Convection | Single-layer board (1s) | $R_{\theta JA}$ | 40.6 | °C/W | 1,2 |
| Junction to Ambient Natural Convection | Four-layer board (2s2p) | $R_{\theta JA}$ | 28.0 | °C/W | 1,2,3 |
| Junction to Ambient (@ 200 ft/min) | Single layer board (1s) | $R_{\theta JMA}$ | 32.1 | °C/W | 1,3 |
| Junction to Ambient (@ 200 ft/min) | Four layer board (2s2p) | $R_{\theta JMA}$ | 23.0 | °C/W | 1,3 |
| Junction to Board | — | $R_{\theta JB}$ | 17.9 | °C/W | 4 |
| Junction to Case | — | $R_{\theta JC}$ | 7.8 | °C/W | 5 |
| Junction to Package Top | Natural Convection | Ψ_{JT} | 2 | °C/W | 6 |
| Junction to Package Bottom | Natural Convection | Ψ_{JB} | 7.5 | °C/W | 7 |

¹ Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

² Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

³ Per JEDEC JESD51-6 with the board horizontal.

⁴ Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

⁵ Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

⁶ Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

⁷ Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

4.1.2.2 17x17 mm NP (VO) and 17x17 mm WP (VN) Package Thermal Resistance

Table 8 displays the 17x17 mm NP (VO) and 17x17 mm WP (VN) package thermal resistance data.

Table 8. 17x17 mm NP (VO) and 17x17 mm WP (VN) Thermal Resistance Data

| Rating | Test Conditions | Symbol | Value | Unit | Notes |
|--|-------------------------|------------------|-------|------|-------|
| Junction to Ambient Natural Convection | Single-layer board (1s) | $R_{\theta JA}$ | 44.4 | °C/W | 1,2 |
| Junction to Ambient Natural Convection | Four-layer board (2s2p) | $R_{\theta JA}$ | 27.4 | °C/W | 1,2,3 |
| Junction to Ambient (@ 200 ft/min) | Single layer board (1s) | $R_{\theta JMA}$ | 35.2 | °C/W | 1,3 |
| Junction to Ambient (@ 200 ft/min) | Four layer board (2s2p) | $R_{\theta JMA}$ | 22.5 | °C/W | 1,3 |
| Junction to Board | — | $R_{\theta JB}$ | 13.2 | °C/W | 4 |
| Junction to Case | — | $R_{\theta JC}$ | 8.4 | °C/W | 5 |
| Junction to Package Top | Natural Convection | Ψ_{JT} | 2 | °C/W | 6 |
| Junction to Package Bottom | Natural Convection | Ψ_{JB} | 8.6 | °C/W | 7 |

¹ Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

² Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

³ Per JEDEC JESD51-6 with the board horizontal.

⁴ Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

⁵ Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

⁶ Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

⁷ Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

4.1.2.3 14x14 mm (VK) Package Thermal Resistance

Table 9 displays the 14x14 mm (VK) package thermal resistance data.

Table 9. 14x14 mm (VK) Package Thermal Resistance Data

| Rating | Test Conditions | Symbol | Value | Unit | Notes |
|--|-------------------------|------------------|-------|------|-------|
| Junction to Ambient Natural Convection | Single-layer board (1s) | $R_{\theta JA}$ | 41.2 | °C/W | 1,2 |
| Junction to Ambient Natural Convection | Four-layer board (2s2p) | $R_{\theta JA}$ | 29.6 | °C/W | 1,2,3 |
| Junction to Ambient (@ 200 ft/min) | Single layer board (1s) | $R_{\theta JMA}$ | 40.9 | °C/W | 1,3 |
| Junction to Ambient (@ 200 ft/min) | Four layer board (2s2p) | $R_{\theta JMA}$ | 24.7 | °C/W | 1,3 |
| Junction to Board | — | $R_{\theta JB}$ | 13.3 | °C/W | 4 |
| Junction to Case | — | $R_{\theta JC}$ | 9.0 | °C/W | 5 |
| Junction to Package Top | Natural Convection | Ψ_{JT} | 2 | °C/W | 6 |
| Junction to Package Bottom | Natural Convection | Ψ_{JB} | 9.9 | °C/W | 7 |

¹ Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

² Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

³ Per JEDEC JESD51-6 with the board horizontal.

⁴ Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

⁵ Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

⁶ Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

⁷ Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

4.1.3 Operating Ranges

Table 10 provides the operating ranges of the i.MX 6SoloX processors. For details on the chip's power structure, see the “Power Management Unit (PMU)” chapter of the *i.MX 6SoloX Applications Processor Reference Manual (IMX6SXRM)*.

NOTE

Applying the maximum power supply voltage results in maximum power consumption and heat generation. NXP recommends a voltage set point = (V_{min} + the supply tolerance). This results in an optimized power/speed ratio.

Table 10. Operating Ranges

| Parameter Description | Symbol | Operating Conditions | Min | Typ | Max ¹ | Unit | Notes |
|--------------------------------------|------------------------------|----------------------|--------------------|------|------------------|------|--|
| Power Supply Operating Ranges | | | | | | | |
| Run Mode: LDO enabled | VDD_ARM_IN | A9 core at 792 MHz | 1.275 | — | 1.5 | V | VDDARM_IN must be 125 mV higher than the LDO Output Set Point (VDD_ARM_CAP) for correct supply voltage regulation. |
| | | A9 core at 396 MHz | 1.175 | — | 1.5 | V | |
| | | A9 core at 198 MHz | 1.075 | — | 1.5 | V | |
| | VDD_ARM_CAP | A9 core at 792 MHz | 1.15 | — | 1.3 | V | Output voltage must be set to the following rule: $VDD_ARM_CAP - VDD_SOC_CAP < +50\text{ mV}$ |
| | | A9 core at 396 MHz | 1.05 | — | 1.3 | V | |
| | | A9 core at 198 MHz | 0.95 | — | 1.3 | V | |
| | VDD_SOC_IN | — | 1.275 | — | 1.5 | V | VDDSOC_IN must be 125mV higher than the LDO Output Set Point (VDD_SOC_CAP) for correct supply voltage regulation. |
| | VDD_SOC_CAP | — | 1.15 | — | 1.3 | V | Output voltage must be set to the following rule: $VDD_ARM_CAP - VDD_SOC_CAP < +50\text{ mV}$ |
| | Run Mode: LDO bypassed | VDD_ARM_IN | A9 core at 792 MHz | 1.15 | — | 1.3 | V |
| A9 core at 396 MHz | | | 1.05 | — | 1.3 | V | |
| A9 core at 198 MHz | | | 0.95 | — | 1.3 | V | |
| VDD_SOC_IN | | — | 1.15 | — | 1.3 | V | |

Table 10. Operating Ranges (continued)

| Parameter Description | Symbol | Operating Conditions | Min | Typ | Max ¹ | Unit | Notes |
|-----------------------------|---------------------------------|----------------------|-------|----------|------------------|------|---|
| Standby/DSM Mode | VDD_ARM_IN | — | 0.9 | — | 1.3 | V | See Table 14 and Table 15 . |
| | VDD_SOC_IN | — | 1.05 | — | 1.3 | V | |
| VDD_HIGH internal regulator | VDD_HIGH_IN | — | 2.8 | — | 3.6 | V | Must match the range of voltages that the rechargeable backup battery supports. |
| Backup battery supply range | VDD_SNVIS_IN | — | 2.4 | — | 3.6 | V | Could be combined with VDD_HIGH_IN if the system does not require real time and other data on off state. |
| USB supply voltages | USB_OTG1_VBUS/ USB_OTG2_VBUS | — | 4.4 | — | 5.5 | V | — |
| DDR I/O supply | NVCC_DRAM | LPDDR2 | 1.14 | 1.2 | 1.3 | V | — |
| | | DDR3L | 1.283 | 1.35 | 1.45 | V | |
| | | DDR3 | 1.425 | 1.5 | 1.575 | V | |
| HSIC I/O supply | NVCC_USB_H | 1.2 V operation | 1.15 | 1.2 | 1.3 | V | IOMUXC_SW_PAD_CTL_PAD_USB_H_DATA[DDR_SEL] = '10' IOMUXC_SW_PAD_CTL_PAD_USB_H_STROBE[DDR_SEL] = '10' NVCC_USB_H should be grounded through a 10k resistor if the HSIC pins are not used. |
| | | 1.5 V operation | 1.425 | 1.5 | 1.575 | V | IOMUXC_SW_PAD_CTL_PAD_USB_H_DATA[DDR_SEL] = '11' IOMUXC_SW_PAD_CTL_PAD_USB_H_STROBE[DDR_SEL] = '11' |
| | | 1.8 V operation | 1.62 | 1.8 | 1.98 | V | |
| | | 2.5 V operation | 2.25 | 2.5 | 2.75 | V | NVCC_USB_H should be grounded through a 10k resistor if the HSIC pins are not used. |
| RGMII I/O supply | NVCC_RGMII1 NVCC_RGMII2 | 1.5 V mode | 1.43 | 1.5 | 1.58 | V | — |
| | | 1.8 V mode | 1.7 | 1.8 | 1.9 | V | |
| | | 2.5 V mode | 2.25 | 2.5 | 2.625 | V | |
| | | 3.3 V mode | 3.0 | 3.15/3.3 | 3.6 | V | |

Table 10. Operating Ranges (continued)

| Parameter Description | Symbol | Operating Conditions | Min | Typ | Max ¹ | Unit | Notes |
|-------------------------------------|---|----------------------|-------|--------------------|------------------|------|--|
| GPIO supplies | NVCC_CSI NVCC_ENET NVCC_GPIO NVCC_HIGH NVCC_KEY NVCC_LCD1 NVCC_LOW NVCC_NAND NVCC_QSPI NVCC_SD1 NVCC_SD2 NVCC_SD4 NVCC_JTAG | — | 1.65 | 1.8 2.8 3.15 | 3.6 | V | All digital I/O supplies (NVCC_xxxx) must be powered (unless otherwise specified in this data sheet) under normal conditions whether the associated I/O pins are in use or not and the associated IO pins need to have a pull-up or pull-down resistor applied to limit any floating gate current. |
| | NVCC_LVDS NVCC_DRAM_2P5 | — | 2.25 | 2.5 | 2.75 | V | |
| PCIe supplies | PCIE_VP | — | 1.023 | 1.1 | 1.21 | V | — |
| | PCIE_VPH | — | 2.325 | 2.5 | 2.75 | V | |
| | PCIE_VPTX | — | 1.023 | 1.1 | 1.21 | V | |
| A/D converter supply | VDDA_ADC_3P3 | — | 3 | 3.15 | 3.6 | V | VDDA_ADC_3P3 must be powered even if the ADC is not used. VDDA_ADC_3P3 should not be powered when the other SoC supplies (except VDD_SNVS_IN) are off. |
| Temperature Operating Ranges | | | | | | | |
| Junction temperature | T _J | Automotive | −40 | — | 125 | °C | See the application note, <i>i.MX 6SoloX Product Lifetime Usage Estimates</i> (AN5062) for information on product lifetime (power-on years) for this processor. |

¹ Applying the maximum voltage results in maximum power consumption and heat generation. NXP recommends a voltage set point = (V_{min} + the supply tolerance). This results in an optimized power/speed ratio.

Table 11 shows on-chip LDO regulators that can supply on-chip loads.

Table 11. On-Chip LDOs¹ and their On-Chip Loads

| Voltage Source | Load | Comment |
|----------------|---------------|--|
| VDD_HIGH_CAP | NVCC_LVDS | Board-level connection to VDD_HIGH_CAP |
| | NVCC_DRAM_2P5 | |
| | PCIE_VPH | |

¹ On-chip LDOs are designed to supply i.MX6 loads and must not be used to supply external loads.

4.1.4 External Clock Sources

Each i.MX 6SoloX processor has two external input system clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI).

The RTC_XTALI is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watch-dog counters. The clock input can be connected to either external oscillator or a crystal using an internal oscillator amplifier. Additionally, there is an internal ring oscillator, which can be used instead of the RTC_XTALI if accuracy is not important.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either external oscillator or a crystal using an internal oscillator amplifier.

CAUTION

The internal RTC oscillator does not provide an accurate frequency and is affected by process, voltage, and temperature variations. NXP strongly recommends using an external crystal as the RTC_XTALI reference. If the internal oscillator is used, careful consideration must be given to the timing implications on all of the SoC modules dependent on this clock.

Table 12 shows the interface frequency requirements.

Table 12. External Input Clock Frequency

| Parameter Description | Symbol | Min | Typ | Max | Unit |
|-------------------------------------|------------|-----|---------------------------|-----|------|
| RTC_XTALI Oscillator ^{1,2} | f_{ckil} | — | 32.768 ³ /32.0 | — | kHz |
| XTALI Oscillator ^{2,4} | f_{xtal} | — | 24 | — | MHz |

¹ External oscillator or a crystal with internal oscillator amplifier.

² The required frequency stability of this clock source is application dependent. For recommendations, see the Hardware Development Guide for i.MX 6SoloX Applications Processors (IMX6XHDG).

³ Recommended nominal frequency 32.768 kHz.

⁴ External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 12 are required for use with NXP BSPs to ensure precise time keeping and USB operation. For RTC_XTALI operation, two clock sources are available.

- On-chip 40 kHz ring oscillator—this clock source has the following characteristics:
 - Approximately 25 μ A more I_{dd} than crystal oscillator
 - Approximately $\pm 50\%$ tolerance
 - No external component required
 - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit:
 - At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
 - Higher accuracy than ring oscillator

Electrical Characteristics

— If no external crystal is present, then the ring oscillator is utilized

The decision of choosing a clock source should be taken based on real-time clock use and precision timeout.

4.1.5 Maximum Supply Currents

The data shown in [Table 13](#) represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

Table 13. Maximum Supply Currents

| Power Line | Conditions | Max Current | Unit |
|--|--|--------------------------------------|------|
| VDD_ARM_IN | 996 MHz Arm clock based on Power Virus operation | 1100 | mA |
| VDD_SOC_IN | 996 MHz Arm clock | 1260 | mA |
| VDD_HIGH_IN | — | 125 ¹ | mA |
| VDD_SNVS_IN | — | 400 ² | μA |
| USB_OTG1_VBUS/USB_OTG2_VBUS (LDO_USB) | — | 50 ³ | mA |
| VDDA_ADC_3P3 | — | 1.5 | mA |
| Primary Interface (IO) Supplies | | | |
| NVCC_DRAM | — | (See Note ⁴) | — |
| NVCC_DRAM_2P5 | — | Use Maximum IO equation ⁵ | — |
| NVCC_ENET | N=10 | Use Maximum IO equation ⁵ | — |
| NVCC_LCD1 | N=29 | Use Maximum IO equation ⁵ | — |
| NVCC_GPIO | N=14 | Use Maximum IO equation ⁵ | — |
| NVCC_CSI | N=12 | Use Maximum IO equation ⁵ | — |
| NVCC_QSPI | N=16 | Use Maximum IO equation ⁵ | — |
| NVCC_JTAG | N=6 | Use Maximum IO equation ⁵ | — |
| NVCC_RGMII1 | N=12 | Use Maximum IO equation ⁵ | — |
| NVCC_RGMII2 | N=12 | Use Maximum IO equation ⁵ | — |
| NVCC_SD1 | N=6 | Use Maximum IO equation ⁵ | — |
| NVCC_SD2 | N=6 | Use Maximum IO equation ⁵ | — |
| NVCC_SD4 | N=11 | Use Maximum IO equation ⁵ | — |
| NVCC_NAND | N=16 | Use Maximum IO equation ⁵ | — |
| NVCC_KEY | N=10 | Use Maximum IO equation ⁵ | — |
| NVCC_LOW | N=10 | Use Maximum IO equation ⁵ | — |

Table 13. Maximum Supply Currents (continued)

| Power Line | Conditions | Max Current | Unit |
|------------|------------|--------------------------------------|------|
| NVCC_HIGH | N=10 | Use Maximum IO equation ⁵ | — |
| NVCC_USB_H | N=2 | Use Maximum IO equation ⁵ | — |

¹ The actual maximum current drawn from VDD_HIGH_IN will be as shown plus any additional current drawn from the VDD_HIGH_CAP outputs, depending upon actual application configuration (for example, NVCC_LVDS).

² Under normal operating conditions, the maximum current on VDD_SNVS_IN is shown [Table 13](#). The maximum VDD_SNVS_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVS_IN can draw up to 1 mA if the supply is capable of sourcing that current. If less than 1 mA is available, the VDD_SNVS_CAP charge time will increase.

³ This is the maximum current per active USB physical interface.

⁴ The DRAM power consumption is dependent on several factors such as external signal termination. DRAM power calculators are typically available from memory vendors which take into account factors such as signal termination. See the *i.MX 6SoloX Power Consumption Measurement Application Note (AN5050)* for examples of DRAM power consumption during specific use case scenarios.

⁵ General equation for estimated, maximum power consumption of an IO power supply:

$$I_{max} = N \times C \times V \times (0.5 \times F)$$

Where:

N—Number of IO pins supplied by the power line

C—Equivalent external capacitive load

V—IO voltage

(0.5 xF)—Data change rate. Up to 0.5 of the clock rate (F)

In this equation, I_{max} is in Amps, C in Farads, V in Volts, and F in Hertz.

4.1.6 Low Power Mode Supply Currents

[Table 14](#) and [Table 15](#) show the current core consumption (not including I/O) of i.MX 6SoloX processors in selected low power modes.

Table 14. Low Power Mode Current and Power Consumption (LDO Bypass Mode)

| Mode | Test Conditions | Supply | Typical ¹ | Units |
|----------------|---|--------------------|----------------------|-------|
| System Idle | See the Power Modes table in the Clock and Power Management chapter of the <i>i.MX 6SoloX Applications Processor Reference Manual (IMX6SXR)</i> for the definition of this mode. | VDDARM_IN (1.15 V) | 7.469 | mA |
| | | VDDSOC_IN (1.15 V) | 8.436 | |
| | | VDDHIGH_IN (3.3 V) | 3.376 | |
| | | Total | 29.430 | mW |
| Low Power Idle | See the Power Modes table in the Clock and Power Management chapter of the <i>i.MX 6SoloX Applications Processor Reference Manual (IMX6SXR)</i> for the definition of this mode. SOC LDO must be bypassed. Bandgap is disabled. | VDDARM_IN (1.15 V) | 0.001 | mA |
| | | VDDSOC_IN (1.15 V) | 2.337 | |
| | | VDDHIGH_IN (3.3 V) | 0.404 | |
| | | Total | 4.022 | mW |

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Table 14. Low Power Mode Current and Power Consumption (LDO Bypass Mode) (continued)

| Mode | Test Conditions | Supply | Typical ¹ | Units |
|---|--|---------------------|----------------------|-------|
| Suspend/ Deep Sleep mode (DSM) | See the Power Modes table in the Clock and Power Management chapter of the <i>i.MX 6SoloX Applications Processor Reference Manual (IMX6SXR)</i> for the definition of this mode. | VDD_ARM_IN (0.9 V) | 0.001 | mA |
| | | VDD_SOC_IN (1.05 V) | 1.005 | |
| | | VDDHIGH_IN (3.3 V) | 0.034 | |
| | | Total | 2.067 | mW |
| SNVS | SNVS power domain powered. All other power domains are off. | VDD_SNVS_IN (2.8 V) | 41 | μA |
| | | Total | 0.115 | mW |

¹ Typical process material in fab.

Table 15. Low Power Mode Current and Power Consumption (LDO Enabled Mode)

| Mode | Test Conditions | Supply | Typical ¹ | Units |
|---|--|-------------------|----------------------|-------|
| Low Power Idle | See the Power Modes table in the Clock and Power Management chapter of the <i>i.MX 6SoloX Applications Processor Reference Manual (IMX6SXR)</i> for the definition of this mode. SOC LDO is enabled. Bandgap is enabled. | VDDARM_IN (1.3V) | 0.008 | mA |
| | | VDDSOC_IN (1.3V) | 2.343 | |
| | | VDDHIGH_IN (3.3V) | 3.376 | |
| | | Total | 14.196 | mW |
| Suspend/ Deep Sleep mode (DSM) | See the Power Modes table in the Clock and Power Management chapter of the <i>i.MX 6SoloX Applications Processor Reference Manual (IMX6SXR)</i> for the definition of this mode. | VDDARM_IN (1.3V) | 0.033 | mA |
| | | VDDSOC_IN (1.3V) | 1.3 | |
| | | VDDHIGH_IN (3.3V) | 0.034 | |
| | | Total | 2.231 | mW |

¹ Typical process material in fab.

4.1.7 USB PHY Current Consumption

4.1.7.1 Power Down Mode

In power down mode, everything is powered down, including the USB_VBUS valid detectors in typical condition. [Table 16](#) shows the USB interface current consumption in power down mode.

Table 16. USB PHY Current Consumption in Power Down Mode

| | VDD_USB_CAP (3.0 V) | VDD_HIGH_CAP (2.5 V) | NVCC_PLL (1.1 V) |
|---------|---------------------|----------------------|------------------|
| Current | 5.1 μA | 1.7 μA | <0.5 μA |

NOTE

The currents on the VDD_HIGH_CAP and VDD_USB_CAP were identified to be the voltage divider circuits in the USB-specific level shifters.

4.1.8 PCIe 2.0 Power Consumption

Table 17 provides PCIe PHY currents under certain transmit operating modes.

Table 17. PCIe PHY Current Drain

| Mode | Test Conditions | Supply | Max Current | Unit |
|---|-----------------|------------------|-------------|------|
| P0: Normal Operation | 5G Operations | PCIE_VPH (2.5 V) | 21 | mA |
| | 2.5G Operations | PCIE_VPH (2.5 V) | 20 | |
| P0s: Low Recovery Time Latency, Power Saving State | 5G Operations | PCIE_VPH (2.5 V) | 18 | mA |
| | 2.5G Operations | PCIE_VPH (2.5 V) | 18 | |
| P1: Longer Recovery Time Latency, Lower Power State | — | PCIE_VPH (2.5 V) | 12 | mA |
| Power Down | — | PCIE_VPH (2.5 V) | 0.36 | mA |

4.2 Power Supplies Requirements and Restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

4.2.1 Power-Up Sequence

The restrictions that follow must be observed:

- VDD_SNVS_IN supply must be turned on before any other power supply or be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- When the SRC_POR_B signal is used to control the processor POR, then SRC_POR_B must be immediately asserted at power-up and remain asserted until the VDD_ARM_CAP and VDD_SOC_CAP supplies are stable. VDD_ARM_IN and VDD_SOC_IN may be applied in either order with no restrictions.

NOTE

Ensure there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

NOTE

USB_OTG1_VBUS and USB_OTG2_VBUS are not part of the power supply sequence and may be powered at any time.

4.2.2 Power-Down Sequence

There are no special restrictions for the i.MX 6SoloX IC.

4.2.3 Power Supplies Usage

All I/O pins must not be externally driven while the I/O power supply for the pin (NVCC_XXX) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Rail” columns in pin list tables of [Section 6, “Package Information and Contact Assignments.”](#)

4.3 Integrated LDO Voltage Regulator Parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and must not be used to power any external circuitry. See the *i.MX 6SoloX Applications Processor Reference Manual (IMX6SXR)* for details on the power tree scheme.

NOTE

The *_CAP signals must not be powered externally. These signals are intended for internal LDO operation only.

4.3.1 Digital Regulators (LDO_ARM, LDO_SOC, LDO_PCIE)

There are three digital LDO regulators (“Digital”, because of the logic loads that they drive, not because of their construction). The advantages of the regulators are to reduce the input supply variation because of their input supply ripple rejection and their on-die trimming. This translates into more stable voltage for the on-chip logic.

These regulators have two basic modes:

- Power Gate. The regulation FET is switched fully off limiting the current draw from the supply. The analog part of the regulator is powered down here limiting the power consumption.
- Analog regulation mode. The regulation FET is controlled such that the output voltage of the regulator equals the programmed target voltage. The target voltage is fully programmable in 25 mV steps.

For additional information, see the *i.MX 6SoloX Applications Processor Reference Manual (IMX6SXR)*.

4.3.2 Regulators for Analog Modules

4.3.2.1 LDO_1P1

The LDO_1P1 regulator implements a programmable linear-regulator function from VDD_HIGH_IN (see [Table 10](#) for minimum and maximum input requirements). Typical Programming Operating Range is 1.0 V to 1.2 V with the nominal default setting as 1.1 V. The LDO_1P1 supplies the USB Phy, LVDS Phy, and

PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded to take the necessary steps. Active-pull-down can also be enabled for systems requiring this feature.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for i.MX 6SoloX Applications Processors (IMX6XHDG).

For additional information, see the *i.MX 6SoloX Applications Processor Reference Manual (IMX6SXR)*.

4.3.2.2 LDO_2P5

The LDO_2P5 module implements a programmable linear-regulator function from VDD_HIGH_IN (see [Table 10](#) for minimum and maximum input requirements). Typical Programming Operating Range is 2.25 V to 2.75 V with the nominal default setting as 2.5 V. LDO_2P5 supplies the DDR IOs, USB Phy, LVDS Phy, E-fuse module, and PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. Active-pull-down can also be enabled for systems requiring this feature. An alternate self-biased low-precision weak-regulator is included that can be enabled for applications needing to keep the output voltage alive during low-power modes where the main regulator driver and its associated global bandgap reference module are disabled. The output of the weak-regulator is not programmable and is a function of the input supply as well as the load current. Typically, with a 3 V input supply the weak-regulator output is 2.525 V and its output impedance is approximately 40 Ω .

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for i.MX 6SoloX Applications Processors (IMX6XHDG).

For additional information, see the *i.MX 6SoloX Applications Processor Reference Manual (IMX6SXR)*.

4.3.2.3 LDO_USB

The LDO_USB module implements a programmable linear-regulator function from the USB_OTG1_VBUS and USB_OTG2_VBUS voltages (4.4 V–5.5 V) to produce a nominal 3.0 V output voltage. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. This regulator has a built in power-mux that allows the user to select to run the regulator from either USB_VBUS supply, when both are present. If only one of the USB_VBUS voltages is present, then, the regulator automatically selects this supply. Current limit is also included to help the system meet in-rush current targets.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for i.MX 6SoloX Applications Processors (IMX6XHDG).

For additional information, see the *i.MX 6SoloX Applications Processor Reference Manual (IMX6SXR)*.

4.4 PLL Electrical Characteristics

4.4.1 Audio/Video PLL Electrical Parameters

Table 18. Audio/Video PLL Electrical Parameters

| Parameter | Value |
|--------------------|-------------------------|
| Clock output range | 650 MHz ~1.3 GHz |
| Reference clock | 24 MHz |
| Lock time | <11250 reference cycles |

4.4.2 528 MHz PLL

Table 19. 528 MHz PLL Electrical Parameters

| Parameter | Value |
|--------------------|-------------------------|
| Clock output range | 528 MHz PLL output |
| Reference clock | 24 MHz |
| Lock time | <11250 reference cycles |

4.4.3 Ethernet PLL

Table 20. Ethernet PLL Electrical Parameters

| Parameter | Value |
|--------------------|-------------------------|
| Clock output range | 500 MHz |
| Reference clock | 24 MHz |
| Lock time | <11250 reference cycles |

4.4.4 480 MHz PLL

Table 21. 480 MHz PLL Electrical Parameters

| Parameter | Value |
|--------------------|-----------------------|
| Clock output range | 480 MHz PLL output |
| Reference clock | 24 MHz |
| Lock time | <383 reference cycles |

4.4.5 Arm PLL

Table 22. Arm PLL Electrical Parameters

| Parameter | Value |
|--------------------|------------------------|
| Clock output range | 650 MHz ~ 1.3 GHz |
| Reference clock | 24 MHz |
| Lock time | <2250 reference cycles |

4.5 On-Chip Oscillators

4.5.1 OSC24M

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements an oscillator. The oscillator is powered from NVCC_PLL.

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used.

4.5.2 OSC32K

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements a low power oscillator. It also implements a power mux such that it can be powered from either a ~3 V backup battery (VDD_SNVS_IN) or VDD_HIGH_IN such as the oscillator consumes power from VDD_HIGH_IN when that supply is available and transitions to the back up battery when VDD_HIGH_IN is lost.

Additionally, if the clock monitor determines that the OSC32K is not present, then the source of the 32 kHz clock will automatically switch to the internal ring oscillator.

CAUTION

The internal RTC oscillator does not provide an accurate frequency and is affected by process, voltage, and temperature variations. NXP strongly recommends using an external crystal as the RTC_XTALI reference. If the internal oscillator is used, careful consideration must be given to the timing implications on all of the SoC modules dependent on this clock.

The OSC32K runs from VDD_SNVS_CAP supply, which comes from the VDD_HIGH_IN/VDD_SNVS_IN.

Table 23. OSC32K Main Characteristics

| Characteristics | Min | Typ | Max | Comments |
|---------------------------|-----|---------------|----------------|---|
| Fosc | — | 32.768 KHz | — | This frequency is nominal and determined mainly by the crystal selected. 32.0 K would work as well. |
| Current consumption | — | 4 μ A | — | The 4 μ A is the consumption of the oscillator alone (OSC32K). Total supply consumption will depend on what the digital portion of the RTC consumes. The ring oscillator consumes 1 μ A when ring oscillator is inactive, 20 μ A when the ring oscillator is running. Another 1.5 μ A is drawn from VDD_SNVS_IN in the power_detect block. So, the total current is 6.5 μ A on VDD_SNVS_IN when the ring oscillator is not running. |
| Bias resistor | — | 14 M Ω | — | This the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amp. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations. |
| Crystal Properties | | | | |
| Cload | — | 10 pF | — | Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal. |
| ESR | — | 50 k Ω | 100 k Ω | Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin. |

4.6 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3 modes
- LVDS I/O

NOTE

The term ‘OVDD’ in this section refers to the associated supply rail of an input or output.

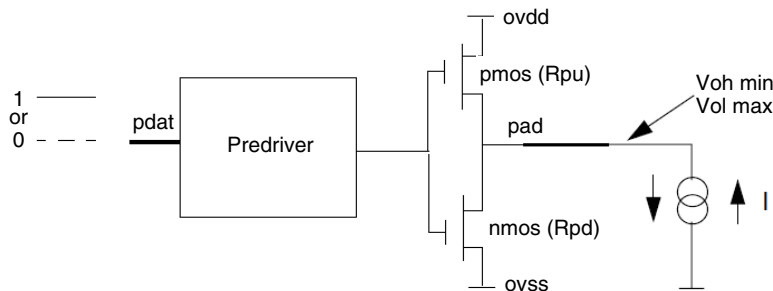


Figure 3. Circuit for Parameters Voh and Vol for I/O Cells

4.6.1 XTALI and RTC_XTALI (Clock Inputs) DC Parameters

Table 24 shows the DC parameters for the clock inputs.

Table 24. XTALI and RTC_XTALI DC Parameters

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---------------------------------------|----------------------------|---|----------------|-----|------------------|------|
| XTALI high-level DC input voltage | V _{ih} | — | 0.8 x NVCC_PLL | — | NVCC_PLL | V |
| XTALI low-level DC input voltage | V _{il} | — | 0 | — | 0.2V | V |
| RTC_XTALI high-level DC input voltage | V _{ih} | — | 0.8 | — | 1.1 ¹ | V |
| RTC_XTALI low-level DC input voltage | V _{il} | — | 0 | — | 0.2 | V |
| Input Capacitance | C _{IN} | Simulated data | — | 5 | — | pF |
| Startup current | I _{XTALI_STARTUP} | Power-on startup for 0.15msec with a driven 24 MHz clock at 1.1V. This current draw is present even if an external clock source directly drives XTALI | — | — | 600 | uA |
| DC input current | I _{XTALI_DC} | — | — | — | 2.5 | uA |

¹ This voltage specification must not be exceeded and, as such, is an absolute maximum specification.

NOTE

The V_{il} and V_{ih} specifications only apply when an external clock source is used. If a crystal is used, V_{il} and V_{ih} do not apply.

4.6.2 Single Voltage General Purpose I/O (GPIO) DC Parameters

Table 25 shows DC parameters for GPIO pads. The parameters in Table 25 are guaranteed per the operating ranges in Table 10, unless otherwise noted.

Table 25. Single Voltage GPIO DC Parameters

| Parameter | Symbol | Test Conditions | Min | Max | Units |
|--|------------------|---|-----------|----------|-------|
| High-level output voltage ¹ | V _{OH} | I _{oh} = -0.1mA (DSE=001,010) I _{oh} = -1mA (DSE=011,100,101,110,111) | OVDD-0.15 | — | V |
| Low-level output voltage ¹ | V _{OL} | I _{ol} = 0.1mA (DSE=001,010) I _{ol} = 1mA (DSE=011,100,101,110,111) | — | 0.15 | V |
| High-Level input voltage ^{1,2} | V _{IH} | — | 0.7*OVDD | OVDD | V |
| Low-Level input voltage ^{1,2} | V _{IL} | — | 0 | 0.3*OVDD | V |
| Input Hysteresis (OVDD= 1.8V) | VHYS_Low VDD | OVDD=1.8 V | 250 | — | mV |
| Input Hysteresis (OVDD=3.3V) | VHYS_High VDD | OVDD=3.3 V | 250 | — | mV |
| Schmitt trigger VT ₊ ^{2,3} | V _{TH+} | — | 0.5*OVDD | — | mV |

Table 25. Single Voltage GPIO DC Parameters (continued)

| Parameter | Symbol | Test Conditions | Min | Max | Units |
|------------------------------------|----------|-------------------------------|-----|----------|-------|
| Schmitt trigger VT- ^{2,3} | VTH- | — | — | 0.5*OVDD | mV |
| Pull-up resistor (22_kΩ PU) | RPU_22K | Vin=0V | — | 212 | μA |
| Pull-up resistor (22_kΩ PU) | RPU_22K | Vin=OVDD | — | 1 | μA |
| Pull-up resistor (47_kΩ PU) | RPU_47K | Vin=0V | — | 100 | μA |
| Pull-up resistor (47_kΩ PU) | RPU_47K | Vin=OVDD | — | 1 | μA |
| Pull-up resistor (100_kΩ PU) | RPU_100K | Vin=0V | — | 48 | μA |
| Pull-up resistor (100_kΩ PU) | RPU_100K | Vin=OVDD | — | 1 | μA |
| Pull-down resistor (100_kΩ PD) | RPD_100K | Vin=OVDD | — | 48 | μA |
| Pull-down resistor (100_kΩ PD) | RPD_100K | Vin=0V | — | 1 | μA |
| Input current (no PU/PD) | IIN | VI = 0, VI = OVDD | -1 | 1 | μA |
| Keeper Circuit Resistance | R_Keeper | VI = 0.3*OVDD, VI = 0.7* OVDD | 105 | 175 | kΩ |

¹ Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

² To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, Vil or Vih. Monotonic input transition time is from 0.1 ns to 1 s.

³ Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4.6.3 Dual Voltage GPIO I/O DC Parameters

Table 26 shows DC parameters for GPIO pads. The parameters in Table 26 are guaranteed per the operating ranges in Table 10, unless otherwise noted.

Table 26. Dual Voltage GPIO I/O DC Parameters

| Parameter | Symbol | Test Conditions | Min | Max | Unit |
|--|--------|---|-------------|------------|------|
| High-level output voltage ¹ | Voh | Ioh = -0.1 mA (DSE ² = 001, 010) Ioh = -1 mA (DSE = 011, 100, 101, 110, 111) | OVDD - 0.15 | — | V |
| Low-level output voltage ¹ | Vol | Iol = 0.1 mA (DSE = 001, 010) Iol = 1mA (DSE = 011, 100, 101, 110, 111) | — | 0.15 | V |
| High-Level DC input voltage ^{1,3} | Vih | — | 0.7 × OVDD | OVDD | V |
| Low-Level DC input voltage ^{1,3} | Vil | — | 0 | 0.3 × OVDD | V |
| Input Hysteresis | Vhys | OVDD = 1.8 V OVDD = 3.3 V | 0.25 | — | V |
| Schmitt trigger VT+ ^{3,4} | VT+ | — | 0.5 × OVDD | — | V |
| Schmitt trigger VT- ^{3,4} | VT- | — | — | 0.5 × OVDD | V |

Table 26. Dual Voltage GPIO I/O DC Parameters (continued)

| Parameter | Symbol | Test Conditions | Min | Max | Unit |
|----------------------------------|-------------------|--|-------|----------|------|
| Input current (no pull-up/down) | I _{in} | V _{in} = OVDD or 0 | -1.25 | 1.25 | μA |
| Input current (22 kΩ pull-up) | I _{in} | V _{in} = 0 V V _{in} = OVDD | — | 212 1 | μA |
| Input current (47 kΩ pull-up) | I _{in} | V _{in} = 0 V V _{in} = OVDD | — | 100 1 | μA |
| Input current (100 kΩ pull-up) | I _{in} | V _{in} = 0 V V _{in} = OVDD | — | 48 1 | μA |
| Input current (100 kΩ pull-down) | I _{in} | V _{in} = 0 V V _{in} = OVDD | — | 1 48 | μA |
| Keeper circuit resistance | R _{keep} | V _{in} = 0.3 x OVDD V _{in} = 0.7 x OVDD | 105 | 205 | kΩ |

¹ Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

² DSE is the Drive Strength Field setting in the associated IOMUX control register.

³ To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, V_{il} or V_{ih}. Monotonic input transition time is from 0.1 ns to 1 s.

⁴ Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4.6.4 DDR I/O DC Parameters

The DDR I/O pads support LPDDR2 and DDR3/DDR3L operational modes.

4.6.4.1 LPDDR2 Mode I/O DC Parameters

For details on supported DDR memory configurations, see [Section 4.10, “Multi-mode DDR Controller \(MMDC\)”](#).

Table 27. LPDDR2 I/O DC Electrical Parameters¹

| Parameters | Symbol | Test Conditions | Min | Max | Unit |
|--------------------------------------|----------------------|--------------------------|------------------------|------------------------|------|
| High-level output voltage | V _{OH} | I _{oh} = -0.1mA | 0.9*OVDD | — | V |
| Low-level output voltage | V _{OL} | I _{ol} = 0.1mA | — | 0.1*OVDD | V |
| Input Reference Voltage | V _{ref} | — | 0.49*OVDD | 0.51*OVDD | V |
| DC High-Level input voltage | V _{ih_DC} | — | V _{ref} +0.13 | OVDD | V |
| DC Low-Level input voltage | V _{il_DC} | — | OVSS | V _{ref} -0.13 | V |
| Differential Input Logic High | V _{ih_diff} | — | 0.26 | Note ² | — |
| Differential Input Logic Low | V _{il_diff} | — | Note ³ | -0.26 | — |
| Pull-up/Pull-down Impedance Mismatch | M _{mpupd} | — | -15 | 15 | % |
| 240 Ω unit calibration resolution | R _{res} | — | — | 10 | Ω |

Electrical Characteristics

Table 27. LPDDR2 I/O DC Electrical Parameters¹ (continued)

| Parameters | Symbol | Test Conditions | Min | Max | Unit |
|---------------------------------|--------|-------------------|------|-----|------|
| Keeper Circuit Resistance | Rkeep | — | 110 | 175 | kΩ |
| Input current (no pull-up/down) | Iin | VI = 0, VI = OVDD | -2.5 | 2.5 | μA |

¹ Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

² The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

³ The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

4.6.4.2 DDR3/DDR3L Mode I/O DC Parameters

For details on supported DDR memory configurations, see [Section 4.10, “Multi-mode DDR Controller \(MMDC\)](#). The parameters in [Table 28](#) are guaranteed per the operating ranges in [Table 10](#), unless otherwise noted.

Table 28. DDR3/DDR3L I/O DC Electrical Characteristics

| Parameters | Symbol | Test Conditions | Min | Max | Unit |
|--------------------------------------|----------|---|------------------------|-----------------------|------|
| High-level output voltage | VOH | Ioh= -0.1mA Voh (for DSE=001) | 0.8*OVDD ¹ | — | V |
| Low-level output voltage | VOL | Iol= 0.1mA Vol (for DSE=001) | 0.2*OVDD | V | — |
| High-level output voltage | VOH | Ioh= -1mA Voh (for all except DSE=001) | 0.8*OVDD | — | V |
| Low-level output voltage | VOL | Iol= 1mA Vol (for all except DSE=001) | 0.2*OVDD | V | — |
| Input Reference Voltage | Vref | — | 0.49*ovdd | 0.51*ovdd | V |
| DC High-Level input voltage | Vih_DC | — | Vref ² +0.1 | OVDD | V |
| DC Low-Level input voltage | Vil_DC | — | OVSS | Vref-0.1 | V |
| Differential Input Logic High | Vih_diff | — | 0.2 | See Note ³ | V |
| Differential Input Logic Low | Vil_diff | — | See Note | -0.2 | V |
| Termination Voltage | Vtt | Vtt tracking OVDD/2 | 0.49*OVDD | 0.51*OVDD | V |
| Pull-up/Pull-down Impedance Mismatch | Mmpupd | — | -10 | 10 | % |
| 240 Ω unit calibration resolution | Rres | — | — | 10 | Ω |
| Keeper Circuit Resistance | Rkeep | — | 105 | 165 | kΩ |
| Input current (no pull-up/down) | Iin | VI = 0, VI = OVDD | -2.9 | 2.9 | μA |

¹ OVDD – I/O power supply (1.425 V–1.575 V for DDR3 and 1.283 V–1.45 V for DDR3L)

² Vref – DDR3/DDR3L external reference voltage

³ The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

4.6.5 LVDS I/O DC Parameters

The LVDS interface complies with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

Table 29 shows the Low Voltage Differential Signaling (LVDS) I/O DC parameters.

Table 29. LVDS I/O DC Characteristics

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|-----------------------------|--------|-------------------------|-------|-------|-------|------|
| Output Differential Voltage | VOD | Rload-100 Ω Diff | 250 | 350 | 450 | mV |
| Output High Voltage | VOH | IOH = 0 mA | 1.25 | 1.375 | 1.6 | V |
| Output Low Voltage | VOL | IOL = 0 mA | 0.9 | 1.025 | 1.25 | V |
| Offset Voltage | VOS | — | 1.125 | 1.2 | 1.375 | V |

4.7 I/O AC Parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3/DDR3L modes
- LVDS I/O

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 4 and Figure 5.

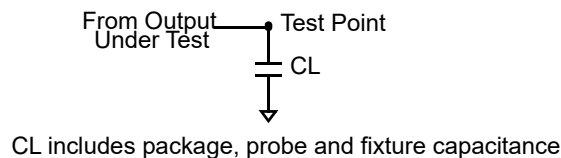


Figure 4. Load Circuit for Output

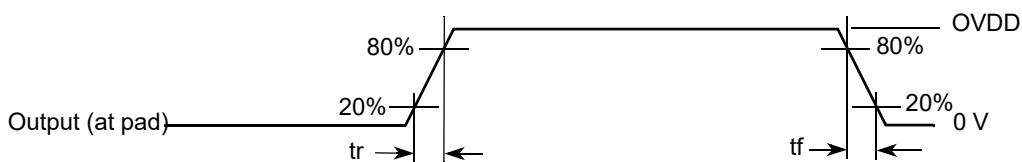


Figure 5. Output Transition Time Waveform

4.7.1 General Purpose I/O AC Parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the Table 30 and Table 31, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Electrical Characteristics

Table 30. General Purpose I/O AC Parameters 1.8 V Mode

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------|--|-----|-----|------------------------|------|
| Output Pad Transition Times, rise/fall (Max Drive, DSE=111) | tr, tf | 15 pF Cload, slow slew rate 15 pF Cload, fast slew rate | — | — | 2.72/2.79 1.51/1.54 | ns |
| Output Pad Transition Times, rise/fall (High Drive, DSE=101) | tr, tf | 15 pF Cload, slow slew rate 15 pF Cload, fast slew rate | — | — | 3.20/3.36 1.96/2.07 | |
| Output Pad Transition Times, rise/fall (Medium Drive, DSE=100) | tr, tf | 15 pF Cload, slow slew rate 15 pF Cload, fast slew rate | — | — | 3.64/3.88 2.27/2.53 | |
| Output Pad Transition Times, rise/fall (Low Drive, DSE=011) | tr, tf | 15 pF Cload, slow slew rate 15 pF Cload, fast slew rate | — | — | 4.32/4.50 3.16/3.17 | |
| Input Transition Times ¹ | trm | — | — | — | 25 | ns |

¹ Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 31. General Purpose I/O AC Parameters 3.3 V Mode

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------|--|-----|-----|------------------------|------|
| Output Pad Transition Times, rise/fall (Max Drive, DSE=101) | tr, tf | 15 pF Cload, slow slew rate 15 pF Cload, fast slew rate | — | — | 1.70/1.79 1.06/1.15 | ns |
| Output Pad Transition Times, rise/fall (High Drive, DSE=011) | tr, tf | 15 pF Cload, slow slew rate 15 pF Cload, fast slew rate | — | — | 2.35/2.43 1.74/1.77 | |
| Output Pad Transition Times, rise/fall (Medium Drive, DSE=010) | tr, tf | 15 pF Cload, slow slew rate 15 pF Cload, fast slew rate | — | — | 3.13/3.29 2.46/2.60 | |
| Output Pad Transition Times, rise/fall (Low Drive, DSE=001) | tr, tf | 15 pF Cload, slow slew rate 15 pF Cload, fast slew rate | — | — | 5.14/5.57 4.77/5.15 | |
| Input Transition Times ¹ | trm | — | — | — | 25 | ns |

¹ Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.7.2 DDR I/O AC Parameters

For details on supported DDR memory configurations, see [Section 4.10, “Multi-mode DDR Controller \(MMDC\)”](#).

[Table 32](#) shows the AC parameters for DDR I/O operating in LPDDR2 mode.

Table 32. DDR I/O LPDDR2 Mode AC Parameters¹

| Parameter | Symbol | Test Condition | Min | Max | Unit |
|--|----------|------------------|-------------|-------------|------|
| AC input logic high | Vih(ac) | — | Vref + 0.22 | OVDD | V |
| AC input logic low | Vil(ac) | — | 0 | Vref - 0.22 | V |
| AC differential input high voltage ² | Vidh(ac) | — | 0.44 | — | V |
| AC differential input low voltage | Vidl(ac) | — | — | 0.44 | V |
| Input AC differential cross point voltage ³ | Vix(ac) | Relative to Vref | -0.12 | 0.12 | V |
| Over/undershoot peak | Vpeak | — | — | 0.35 | V |

Table 32. DDR I/O LPDDR2 Mode AC Parameters¹ (continued)

| Parameter | Symbol | Test Condition | Min | Max | Unit |
|---|------------------|--|-----|-----|------|
| Over/undershoot area (above OVDD or below OVSS) | Varea | 400 MHz | — | 0.3 | V-ns |
| Single output slew rate, measured between Vol(ac) and Voh(ac) | tsr | 50 Ω to Vref. 5 pF load. Drive impedance = 40 $\Omega \pm 30\%$ | 1.5 | 3.5 | V/ns |
| | | 50 Ω to Vref. 5pF load. Drive impedance = 60 $\Omega \pm 30\%$ | 1 | 2.5 | |
| Skew between pad rise/fall asymmetry + skew caused by SSN | t _{SKD} | clk = 400 MHz | — | 0.1 | ns |

¹ Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

² Vid(ac) specifies the input differential voltage $|V_{tr} - V_{cp}|$ required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).

³ The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 33 shows the AC parameters for DDR I/O operating in DDR3/DDR3L mode.

Table 33. DDR I/O DDR3/DDR3L Mode AC Parameters¹

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|------------------|--------------------------------|--------------|-----|--------------|------|
| AC input logic high | Vih(ac) | — | Vref + 0.175 | — | OVDD | V |
| AC input logic low | Vil(ac) | — | 0 | — | Vref - 0.175 | V |
| AC differential input voltage ² | Vid(ac) | — | 0.35 | — | — | V |
| Input AC differential cross point voltage ^{3,4} | Vix(ac) | Relative to Vref | Vref - 0.15 | — | Vref + 0.15 | V |
| Over/undershoot peak | Vpeak | — | — | — | 0.4 | V |
| Over/undershoot area (above OVDD or below OVSS) | Varea | 400 MHz | — | — | 0.5 | V-ns |
| Single output slew rate, measured between Vol(ac) and Voh(ac) | tsr | Driver impedance = 34 Ω | 2.5 | — | 5 | V/ns |
| Skew between pad rise/fall asymmetry + skew caused by SSN | t _{SKD} | clk = 400 MHz | — | — | 0.1 | ns |

¹ Note that the JEDEC JESD79_3C specification supersedes any specification in this document.

² Vid(ac) specifies the input differential voltage $|V_{tr} - V_{cp}|$ required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).

³ The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

⁴ Extended range for Vix is only allowed for the clock and when the single-ended clock input signals CK and CK# are:
Monotonic with a single-ended swing VSEL/VSEH of at least $VDD/2 \pm 250$ mV, and
The differential slew rate of CK - CK# is larger than 3 V/ns

4.7.3 LVDS I/O AC Parameters

The differential output transition time waveform is shown in Figure 6.

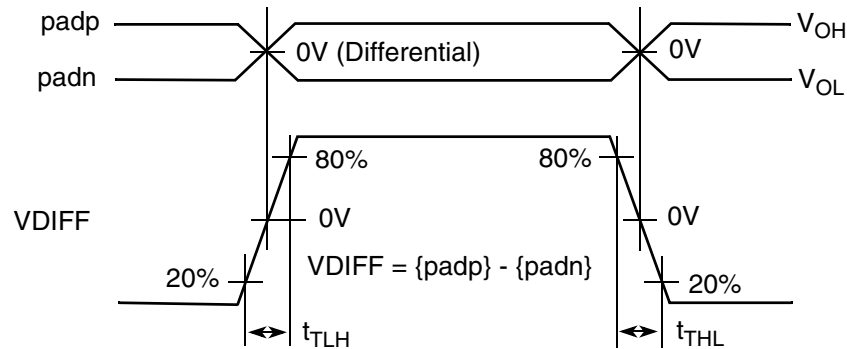


Figure 6. Differential LVDS Driver Transition Time Waveform

Table 34 shows the AC parameters for LVDS I/O.

Table 34. I/O AC Parameters of LVDS Pad

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-----------|--|-----|-----|------|------|
| Differential pulse skew ¹ | t_{SKD} | Rload = 100 Ω , Cload = 2 pF | — | — | 0.25 | ns |
| Transition Low to High Time ² | t_{TLH} | | — | — | 0.5 | |
| Transition High to Low Time ² | t_{THL} | | — | — | 0.5 | |
| Operating Frequency | f | — | — | 600 | 800 | MHz |
| Offset voltage imbalance | Vos | — | — | — | 150 | mV |

¹ $t_{SKD} = |t_{PHLD} - t_{PLHD}|$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

² Measurement levels are 20-80% from output voltage.

4.8 Output Buffer Impedance Parameters

This section defines the I/O impedance parameters of the i.MX 6SoloX processors for the following I/O types:

- Dual Voltage General Purpose I/O (DVGPIO)
- Single Voltage General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2, and DDR3/DDR3L modes
- LVDS I/O

NOTE

GPIO and DDR I/O output driver impedance is measured with “long” transmission line of impedance Z_{tl} attached to I/O pad and incident wave launched into transmission line. R_{pu}/R_{pd} and Z_{tl} form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 7).

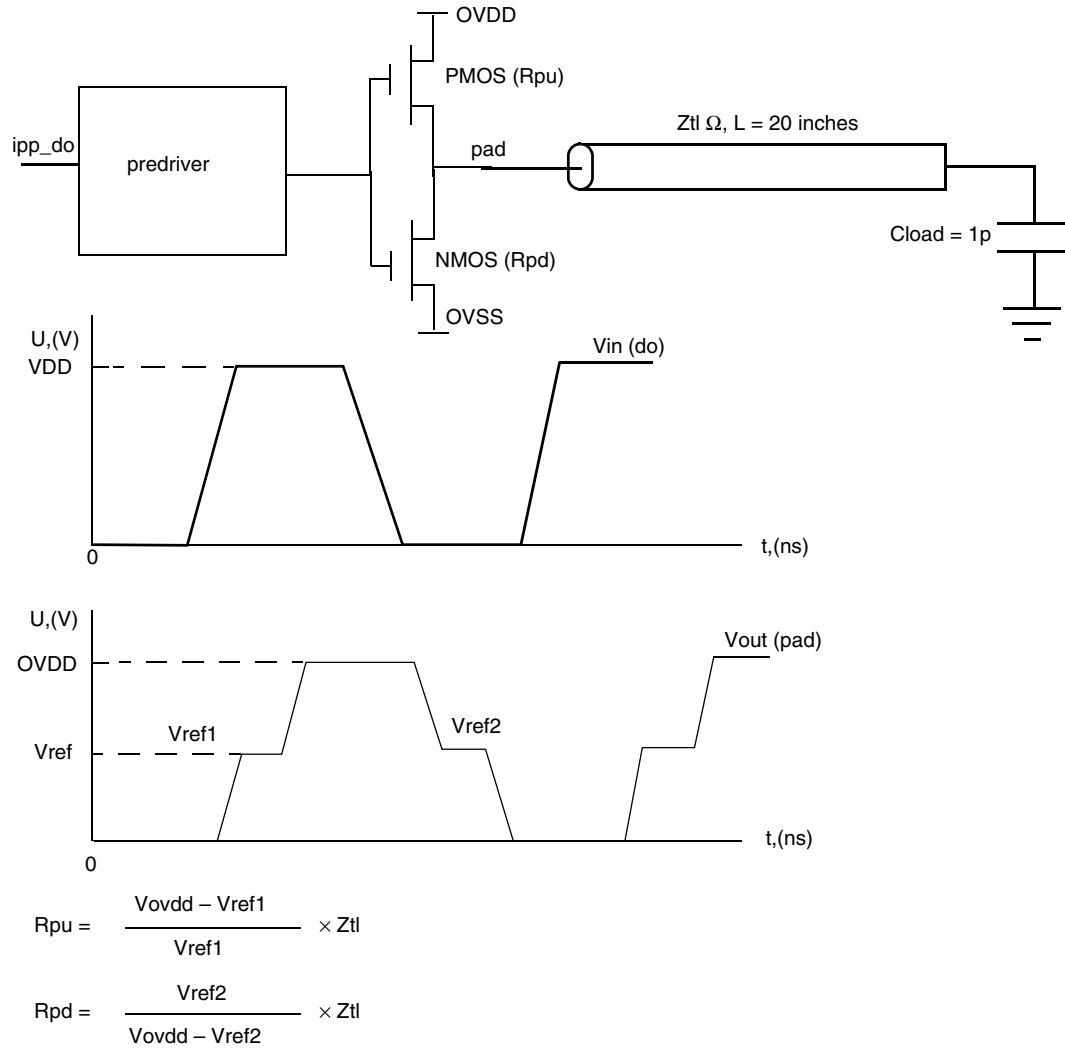


Figure 7. Impedance Matching Load for Measurement

4.8.1 Dual Voltage GPIO Output Buffer Impedance

Table 35 shows the GPIO output buffer impedance (OVDD 1.8 V).

Table 35. DVGPIO Output Buffer Average Impedance (OVDD 1.8 V)

| Parameter | Symbol | Drive Strength (DSE) | Typical | Typical | Unit |
|-------------------------|--------|----------------------|----------|----------|------|
| | | | ADD_DS=1 | ADD_DS=0 | |
| Output Driver Impedance | Rdrv | 000 | Hi-Z | Hi-Z | Ω |
| | | 001 | 262 | 235 | |
| | | 010 | 134 | 117 | |
| | | 011 | 88 | 78 | |
| | | 100 | 62 | 52 | |
| | | 101 | 51 | 43 | |
| | | 110 | 43 | 36 | |
| | | 111 | 37 | 31 | |

Table 36 shows the GPIO output buffer impedance (OVDD 3.3 V).

Table 36. DVGPIO Output Buffer Average Impedance (OVDD 3.3 V)

| Parameter | Symbol | Drive Strength (DSE) | Typical | Unit |
|-------------------------|--------|----------------------|---------|------|
| Output Driver Impedance | Rdrv | 000 | Hi-Z | Ω |
| | | 001 | 247 | |
| | | 010 | 126 | |
| | | 011 | 84 | |
| | | 100 | 57 | |
| | | 101 | 47 | |
| | | 110 | 40 | |
| 111 | 34 | | | |

4.8.2 Single Voltage GPIO Output Buffer Impedance

Table 37 shows the GPIO output buffer impedance (OVDD 1.8 V).

Table 37. GPIO Output Buffer Average Impedance (OVDD 1.8 V)

| Parameter | Symbol | Drive Strength (DSE) | Typ Value | Unit |
|-------------------------|--------|----------------------|-----------|------|
| Output Driver Impedance | Rdrv | 001 | 260 | Ω |
| | | 010 | 130 | |
| | | 011 | 88 | |
| | | 100 | 65 | |
| | | 101 | 52 | |
| | | 110 | 43 | |
| | | 111 | 37 | |

Table 38 shows the GPIO output buffer impedance (OVDD 3.3 V).

Table 38. GPIO Output Buffer Average Impedance (OVDD 3.3 V)

| Parameter | Symbol | Drive Strength (DSE) | Typ Value | Unit |
|-------------------------|--------|----------------------|-----------|------|
| Output Driver Impedance | Rdrv | 001 | 157 | Ω |
| | | 010 | 78 | |
| | | 011 | 53 | |
| | | 100 | 39 | |
| | | 101 | 32 | |
| | | 110 | 26 | |
| | | 111 | 23 | |

4.8.3 DDR I/O Output Buffer Impedance

For details on supported DDR memory configurations, see [Section 4.10, “Multi-mode DDR Controller \(MMDC\)”](#).

Table 39 shows DDR I/O output buffer impedance of i.MX 6SoloX processors.

Table 39. DDR I/O Output Buffer Impedance

| Parameter | Symbol | Test Conditions DSE (Drive Strength) | Typical | | Unit |
|----------------------------|--------|---|---|---|------|
| | | | NVCC_DRAM=1.5 V (DDR3) DDR_SEL=11 | NVCC_DRAM=1.2 V (LPDDR2) DDR_SEL=10 | |
| Output Driver Impedance | Rdrv | 000 | Hi-Z | Hi-Z | Ω |
| | | 001 | 240 | 240 | |
| | | 010 | 120 | 120 | |
| | | 011 | 80 | 80 | |
| | | 100 | 60 | 60 | |
| | | 101 | 48 | 48 | |
| | | 110 | 40 | 40 | |
| | | 111 | 34 | 34 | |

Note:

1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.
2. Calibration is done against 240 Ω external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

4.8.4 USB HSIC I/O Output Buffer Impedance

Table 40 shows the USB HSIC I/O (USB_H_DATA and USB_H_STROBE) output buffer impedance.

Table 40. USB HSIC I/O Output Buffer Impedance

| Parameter | Symbol | Drive Strength (DSE) | Typical | | | | Unit |
|-------------------------------|--------|----------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|------|
| | | | NVCC_USB_H=1.2V DDR_SEL=10 | NVCC_USB_H=1.5V DDR_SEL=11 | NVCC_USB_H=1.8V DDR_SEL=11 | NVCC_USB_H=2.5V DDR_SEL=11 | |
| Output Driver Impedance | Rdrv | 000 | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Ω |
| | | 001 | 240 | 240 | 247 | 287 | |
| | | 010 | 120 | 120 | 113 | 121 | |
| | | 011 | 80 | 80 | 73 | 76 | |
| | | 100 | 60 | 60 | 55 | 57 | |
| | | 101 | 48 | 48 | 43 | 45 | |
| | | 110 | 40 | 40 | 36 | 37 | |
| | | 111 | 34 | 34 | 30 | 31 | |

4.8.5 LVDS I/O Output Buffer Impedance

The LVDS interface complies with TIA/EIA 644-A standard. See, TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

4.9 System Modules Timing

This section contains the timing and electrical parameters for the modules in each i.MX 6SoloX processor.

4.9.1 Reset Timing Parameters

Figure 8 shows the reset timing and Table 41 lists the timing parameters.

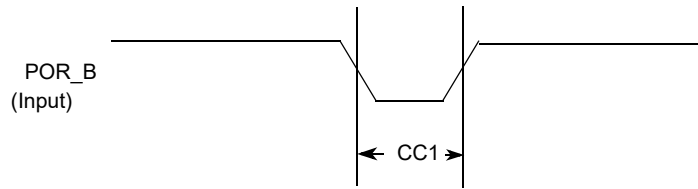


Figure 8. Reset Timing Diagram

Table 41. Reset Timing Parameters

| ID | Parameter | Min | Max | Unit |
|-----|---|-----|-----|-----------------|
| CC1 | Duration of POR_B to be qualified as valid. | 1 | — | RTC_XTALI cycle |

4.9.2 WDOG Reset Timing Parameters

Figure 9 shows the WDOG reset timing and Table 42 lists the timing parameters.

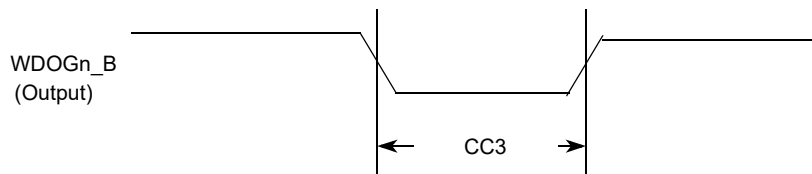


Figure 9. WDOGn_B Timing Diagram

Table 42. WDOGn_B Timing Parameters

| ID | Parameter | Min | Max | Unit |
|-----|-------------------------------|-----|-----|-----------------|
| CC3 | Duration of WDOGn_B Assertion | 1 | — | RTC_XTALI cycle |

NOTE

RTC_XTALI is approximately 32 kHz. RTC_XTALI cycle is one period or approximately 30 μs.

NOTE

WDOG1_B output signals (for each one of the Watchdog modules) do not have dedicated pins, but are muxed out through the IOMUX. See the IOMUX manual for detailed information.

4.9.3 External Interface Module (EIM)

The following subsections provide information on the EIM. Maximum operating frequency for EIM data transfer is 104 MHz. Two system clocks are used with the EIM:

- ACLK_EIM_SLOW_CLK_ROOT is used to clock the EIM module.
The maximum frequency for CLK_EIM_SLOW_CLK_ROOT is 132 MHz.

- ACLK_EXSC is also used when the EIM is in synchronous mode.
The maximum frequency for ACLK_EXSC is 132 MHz.

Timing parameters in this section that are given as a function of register settings.

4.9.3.1 EIM Interface Pads Allocation

EIM supports 32-bit, 16-bit and 8-bit devices operating in address/data separate or multiplexed modes. Table 43 provides EIM interface pads allocation in different modes.

Table 43. EIM Internal Module Multiplexing¹

| Setup | Non Multiplexed Address/Data Mode | | | | | | | Multiplexed Address/Data mode | |
|--------------------------------|-----------------------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-------------------------------|-----------------------|
| | 8 Bit | | | | 16 Bit | | 32 Bit | 16 Bit | 32 Bit |
| | MUM = 0, DSZ = 100 | MUM = 0, DSZ = 101 | MUM = 0, DSZ = 110 | MUM = 0, DSZ = 111 | MUM = 0, DSZ = 001 | MUM = 0, DSZ = 010 | MUM = 0, DSZ = 011 | MUM = 1, DSZ = 001 | MUM = 1, DSZ = 011 |
| EIM_ADDR [15:00] | EIM_AD [15:00] | EIM_AD [15:00] | EIM_AD [15:00] | EIM_AD [15:00] | EIM_AD [15:00] | EIM_AD [15:00] | EIM_AD [15:00] | EIM_AD [15:00] | EIM_AD [15:00] |
| EIM_ADDR [25:16] | EIM_ADDR [25:16] | EIM_ADDR [25:16] | EIM_ADDR [25:16] | EIM_ADDR [25:16] | EIM_ADDR [25:16] | EIM_ADDR [25:16] | EIM_ADDR [25:16] | EIM_ADDR [25:16] | EIM_DATA [09:00] |
| EIM_DATA [07:00], EIM_EB0_B | EIM_DATA [07:00] | — | — | — | EIM_DATA [07:00] | — | EIM_DATA [07:00] | EIM_AD [07:00] | EIM_AD [07:00] |
| EIM_DATA [15:08], EIM_EB1_B | — | EIM_DATA [15:08] | — | — | EIM_DATA [15:08] | — | EIM_DATA [15:08] | EIM_AD [15:08] | EIM_AD [15:08] |
| EIM_DATA [23:16], EIM_EB2_B | — | — | EIM_DATA [23:16] | — | — | EIM_DATA [23:16] | EIM_DATA [23:16] | — | EIM_DATA [07:00] |
| EIM_DATA [31:24], EIM_EB3_B | — | — | — | EIM_DATA [31:24] | — | EIM_DATA [31:24] | EIM_DATA [31:24] | — | EIM_DATA [15:08] |

¹ For more information on configuration ports mentioned in this table, see the [i.MX 6SoloX Applications Processor Reference Manual \(IMX6SXR\)](#).

4.9.3.2 General EIM Timing-Synchronous Mode

Figure 10, Figure 11, and Table 44 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the EIM_BCLK rising edge according to corresponding assertion/negation control fields.

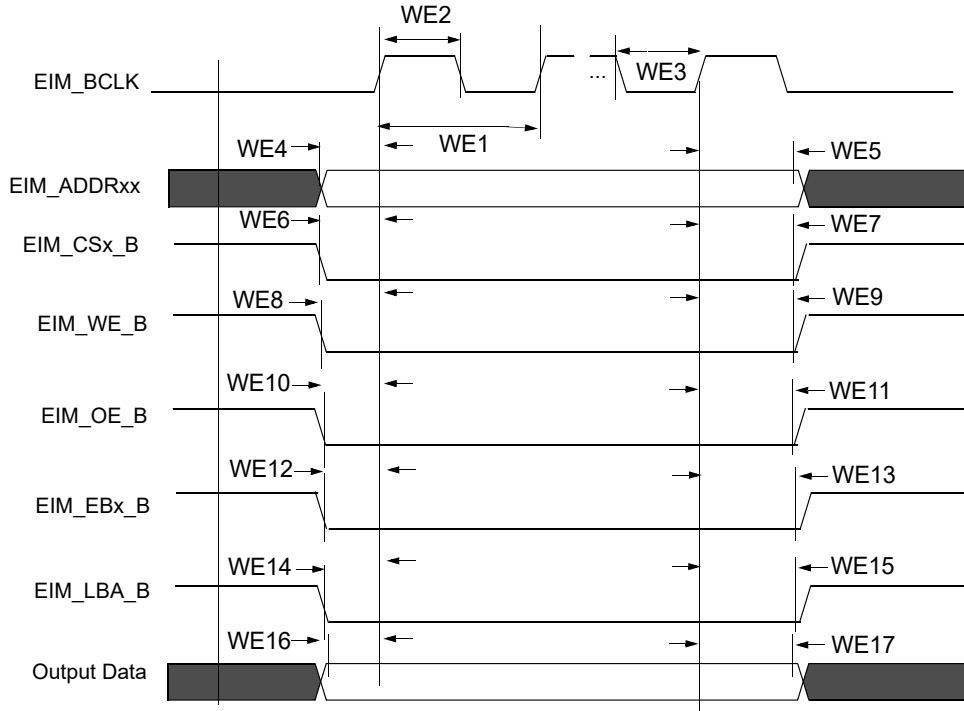


Figure 10. EIM Outputs Timing Diagram

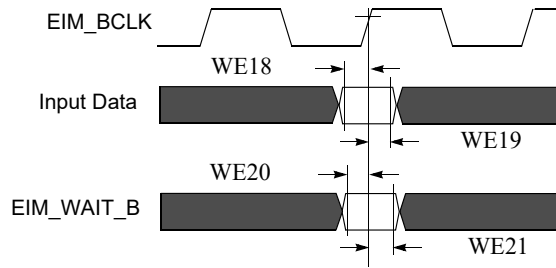


Figure 11. EIM Inputs Timing Diagram

4.9.3.3 Examples of EIM Synchronous Accesses

Table 44. EIM Bus Timing Parameters ¹

| ID | Parameter | BCD = 0 | | BCD = 1 | | BCD = 2 | | BCD = 3 | |
|------|--|-----------------|-----------------|----------|----------|-----------------|-----------------|---------------|---------------|
| | | Min | Max | Min | Max | Min | Max | Min | Max |
| WE1 | EIM_BCLK Cycle time ² | t | — | 2 x t | — | 3 x t | — | 4 x t | — |
| WE2 | EIM_BCLK Low Level Width | 0.4 x t | — | 0.8 x t | — | 1.2 x t | — | 1.6 x t | — |
| WE3 | EIM_BCLK High Level Width | 0.4 x t | — | 0.8 x t | — | 1.2 x t | — | 1.6 x t | — |
| WE4 | Clock rise to address valid ³ | -0.5 x t - 1.25 | -0.5 x t + 1.75 | t - 1.25 | t + 1.75 | -1.5 x t - 1.25 | -1.5 x t + 1.75 | -2 x t - 1.25 | -2 x t + 1.75 |
| WE5 | Clock rise to address invalid | 0.5 x t - 1.25 | 0.5 x t + 1.75 | t - 1.25 | t + 1.75 | 1.5 x t - 1.25 | 1.5 x t + 1.75 | 2 x t - 1.25 | 2 x t + 1.75 |
| WE6 | Clock rise to EIM_CSx_B valid | -0.5 x t - 1.25 | -0.5 x t + 1.75 | t - 1.25 | t + 1.75 | -1.5 x t - 1.25 | -1.5 x t + 1.75 | -2 x t - 1.25 | -2 x t + 1.75 |
| WE7 | Clock rise to EIM_CSx_B invalid | 0.5 x t - 1.25 | 0.5 x t + 1.75 | t - 1.25 | t + 1.75 | 1.5 x t - 1.25 | 1.5 x t + 1.75 | 2 x t - 1.25 | 2 x t + 1.75 |
| WE8 | Clock rise to EIM_WE_B Valid | -0.5 x t - 1.25 | -0.5 x t + 1.75 | t - 1.25 | t + 1.75 | -1.5 x t - 1.25 | -1.5 x t + 1.75 | -2 x t - 1.25 | -2 x t + 1.75 |
| WE9 | Clock rise to EIM_WE_B Invalid | 0.5 x t - 1.25 | 0.5 x t + 1.75 | t - 1.25 | t + 1.75 | 1.5 x t - 1.25 | 1.5 x t + 1.75 | 2 x t - 1.25 | 2 x t + 1.75 |
| WE10 | Clock rise to EIM_OE_B Valid | -0.5 x t - 1.25 | -0.5 x t + 1.75 | t - 1.25 | t + 1.75 | -1.5 x t - 1.25 | -1.5 x t + 1.75 | -2 x t - 1.25 | -2 x t + 1.75 |
| WE11 | Clock rise to EIM_OE_B Invalid | 0.5 x t - 1.25 | 0.5 x t + 1.75 | t - 1.25 | t + 1.75 | 1.5 x t - 1.25 | 1.5 x t + 1.75 | 2 x t - 1.25 | 2 x t + 1.75 |
| WE12 | Clock rise to EIM_EBx_B Valid | -0.5 x t - 1.25 | -0.5 x t + 1.75 | t - 1.25 | t + 1.75 | -1.5 x t - 1.25 | -1.5 x t + 1.75 | -2 x t - 1.25 | -2 x t + 1.75 |
| WE13 | Clock rise to EIM_EBx_B Invalid | 0.5 x t - 1.25 | 0.5 x t + 1.75 | t - 1.25 | t + 1.75 | 1.5 x t - 1.25 | 1.5 x t + 1.75 | 2 x t - 1.25 | 2 x t + 1.75 |
| WE14 | Clock rise to EIM_LBA_B Valid | -0.5 x t - 1.25 | -0.5 x t + 1.75 | t - 1.25 | t + 1.75 | -1.5 x t - 1.25 | -1.5 x t + 1.75 | -2 x t - 1.25 | -2 x t + 1.75 |
| WE15 | Clock rise to EIM_LBA_B Invalid | 0.5 x t - 1.25 | 0.5 x t + 1.75 | t - 1.25 | t + 1.75 | 1.5 x t - 1.25 | 1.5 x t + 1.75 | 2 x t - 1.25 | 2 x t + 1.75 |
| WE16 | Clock rise to Output Data Valid | -0.5 x t - 1.25 | -0.5 x t + 1.75 | t - 1.25 | t + 1.75 | -1.5 x t - 1.25 | -1.5 x t + 1.75 | -2 x t - 1.25 | -2 x t + 1.75 |
| WE17 | Clock rise to Output Data Invalid | 0.5 x t - 1.25 | 0.5 x t + 1.75 | t - 1.25 | t + 1.75 | 1.5 x t - 1.25 | 1.5 x t + 1.75 | 2 x t - 1.25 | 2 x t + 1.75 |
| WE18 | Input Data setup time to Clock rise | 2 | — | 4 | — | — | — | — | — |
| WE19 | Input Data hold time from Clock rise | 2 | — | 2 | — | — | — | — | — |
| WE20 | EIM_WAIT_B setup time to Clock rise | 2 | — | 4 | — | — | — | — | — |
| WE21 | EIM_WAIT_B hold time from Clock rise | 2 | — | 2 | — | — | — | — | — |

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¹ t is the maximum EIM logic (ACLK_EXSC) cycle time. The maximum allowed axi_clk frequency depends on the fixed/non-fixed latency configuration, whereas the maximum allowed EIM_BCLK frequency is:

- Fixed latency for both read and write is 104 MHz.
- Variable latency for read only is 104 MHz.
- Variable latency for write only is 52 MHz.

In variable latency configuration for write, if BCD = 0 & WBCDD = 1 or BCD = 1, axi_clk must be 104 MHz. Write BCD = 1 and 104 MHz ACLK_EXSC, will result in a EIM_BCLK of 52 MHz. When the clock branch to EIM is decreased to 104 MHz, other buses are impacted which are clocked from this source. See the CCM chapter of the *ii.MX 6SoloX Applications Processor Reference Manual (IMX6SXRM)* for a detailed clock tree description.

² EIM_BCLK parameters are being measured from the 50% point, that is, high is defined as 50% of signal value and low is defined as 50% as signal value.

³ For signal measurements, “High” is defined as 80% of signal value and “Low” is defined as 20% of signal value.

Figure 12 to Figure 15 provide few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

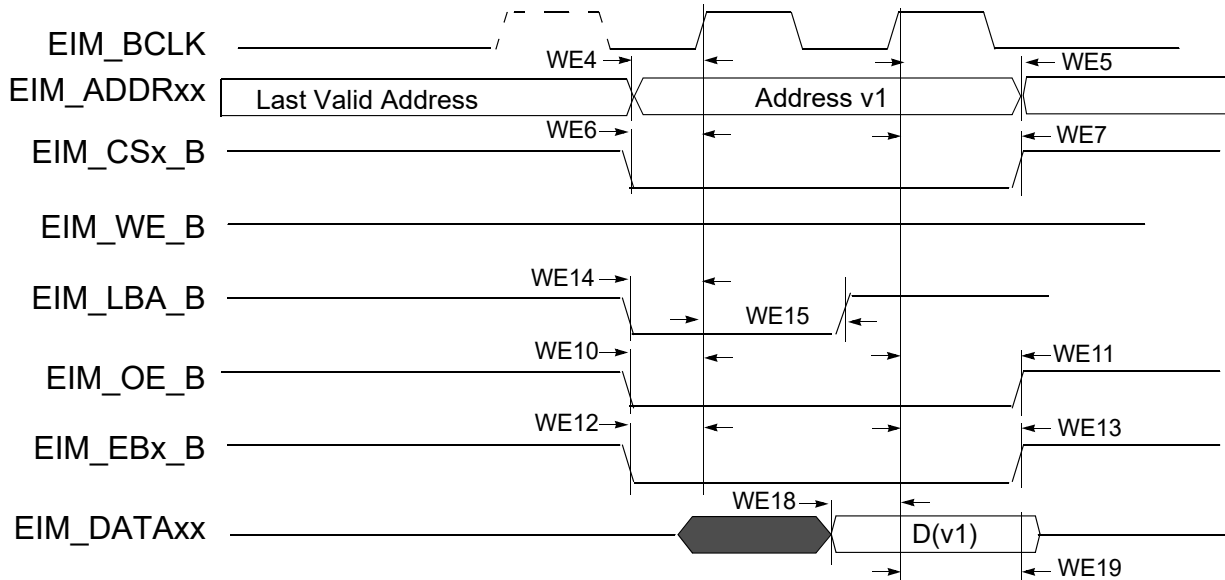


Figure 12. Synchronous Memory Read Access, WSC=1

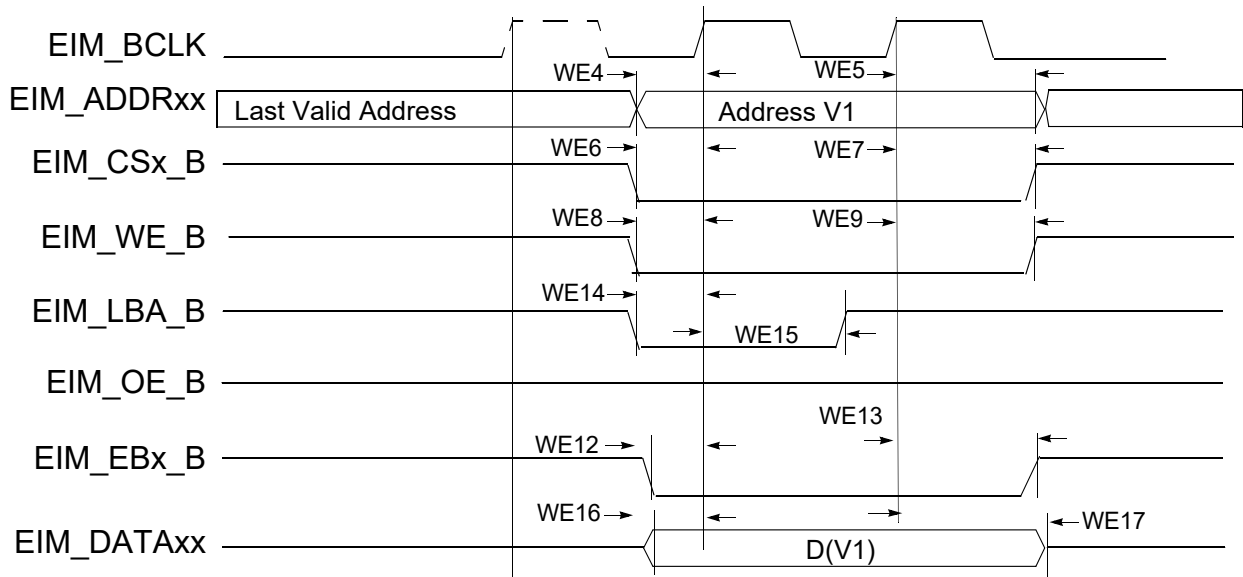


Figure 13. Synchronous Memory, Write Access, WSC=1, WBEA=0 and WADV=0

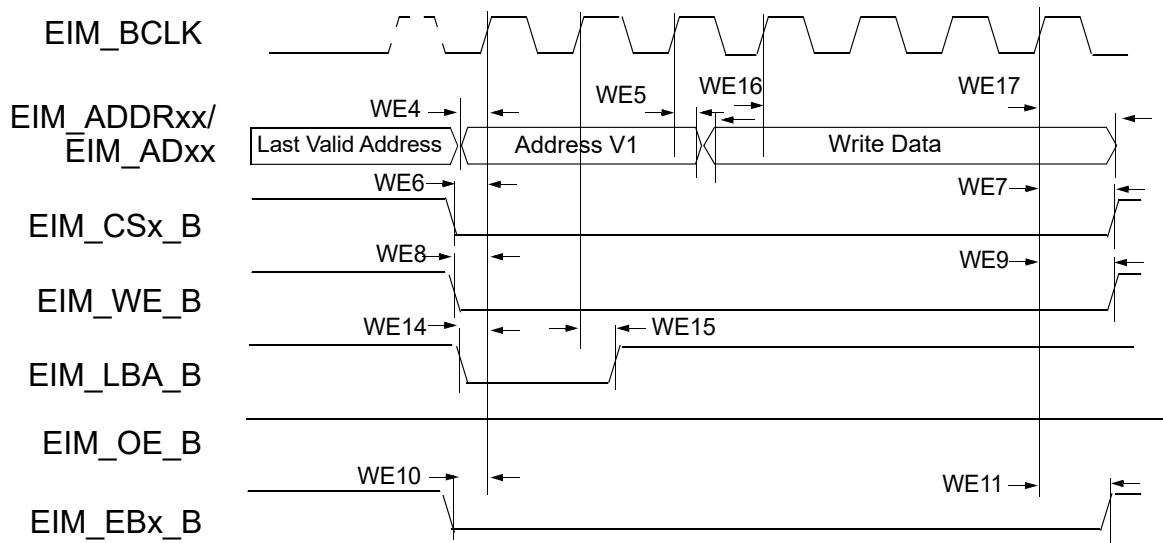


Figure 14. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6, ADVA=0, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode the 16 MSBs are driven on the data bus.

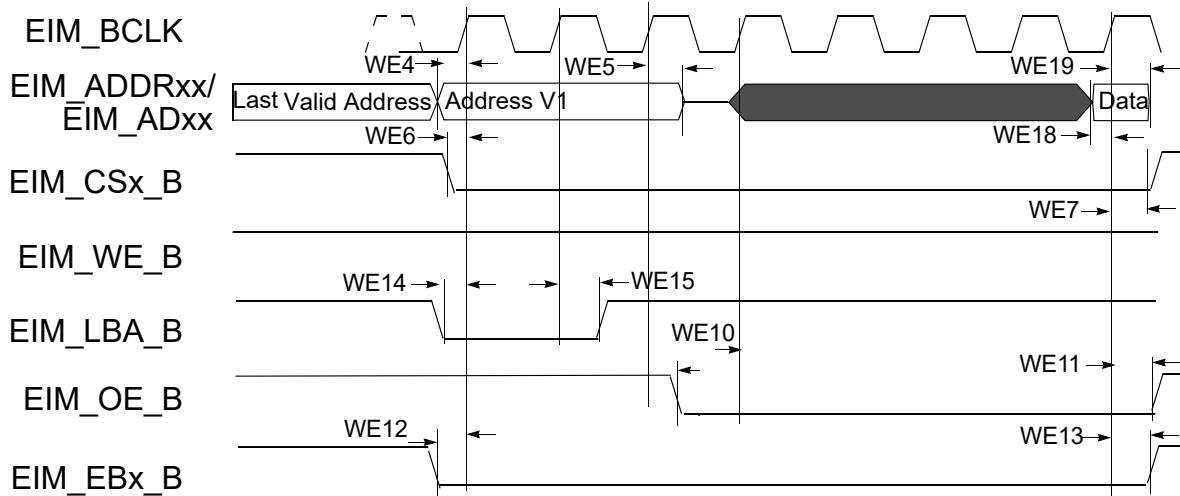


Figure 15. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=0

4.9.3.4 General EIM Timing-Asynchronous Mode

Figure 16 through Figure 21, and Table 45 help you determine timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read and write access length in cycles may vary from what is shown in Figure 16 through Figure 19 as RWSC, OEN and CSN is configured differently. See the *ii.MX 6SoloX Applications Processor Reference Manual (IMX6SXR)* for the EIM programming model.

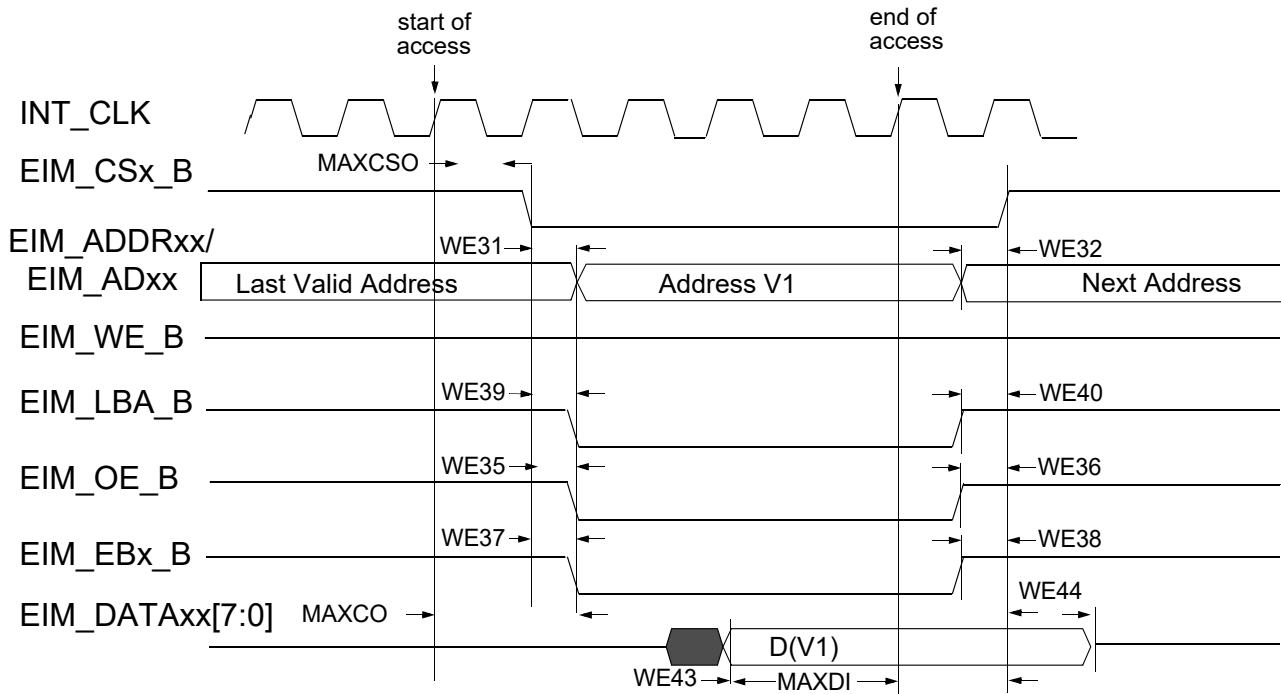


Figure 16. Asynchronous Memory Read Access (RWSC = 5)

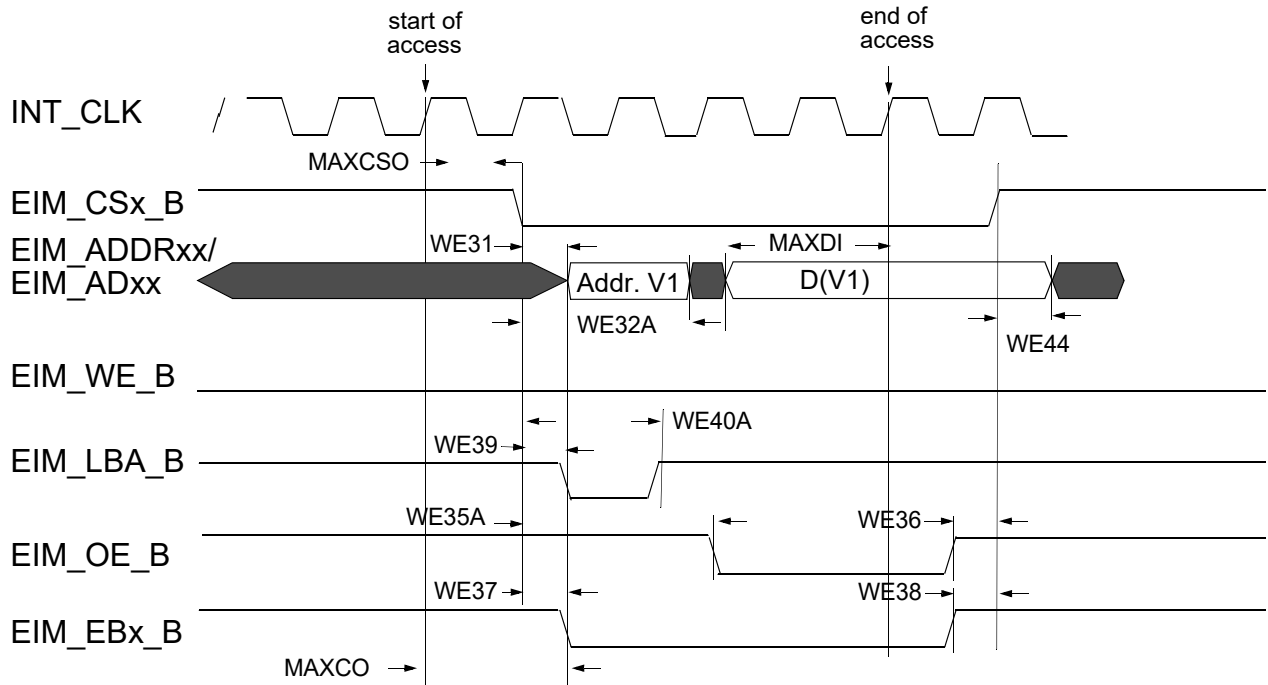


Figure 17. Asynchronous A/D Muxed Read Access (RWSC = 5)

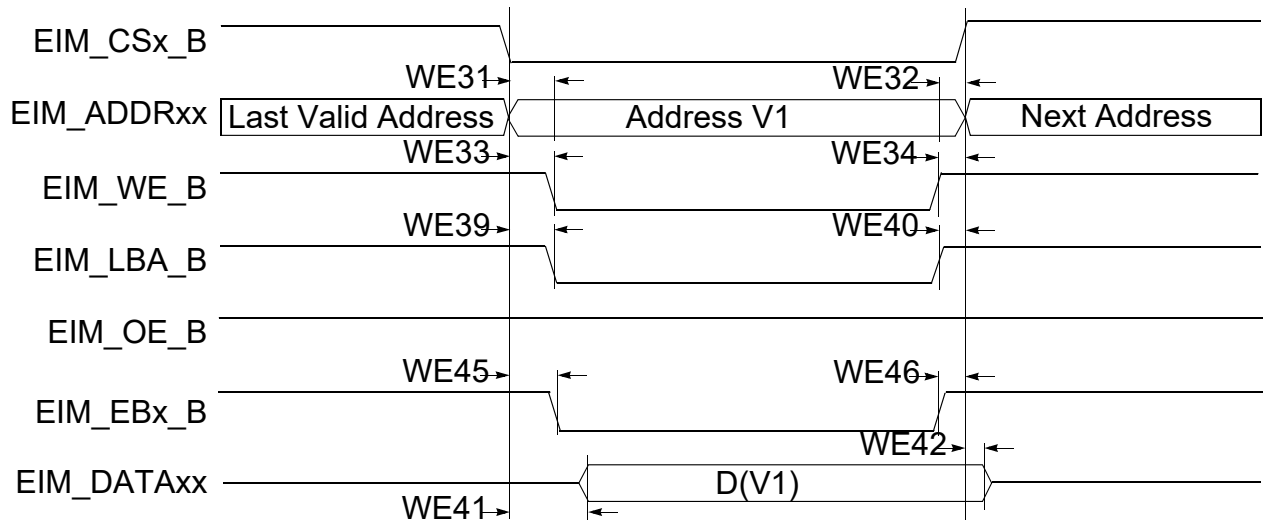


Figure 18. Asynchronous Memory Write Access

Electrical Characteristics

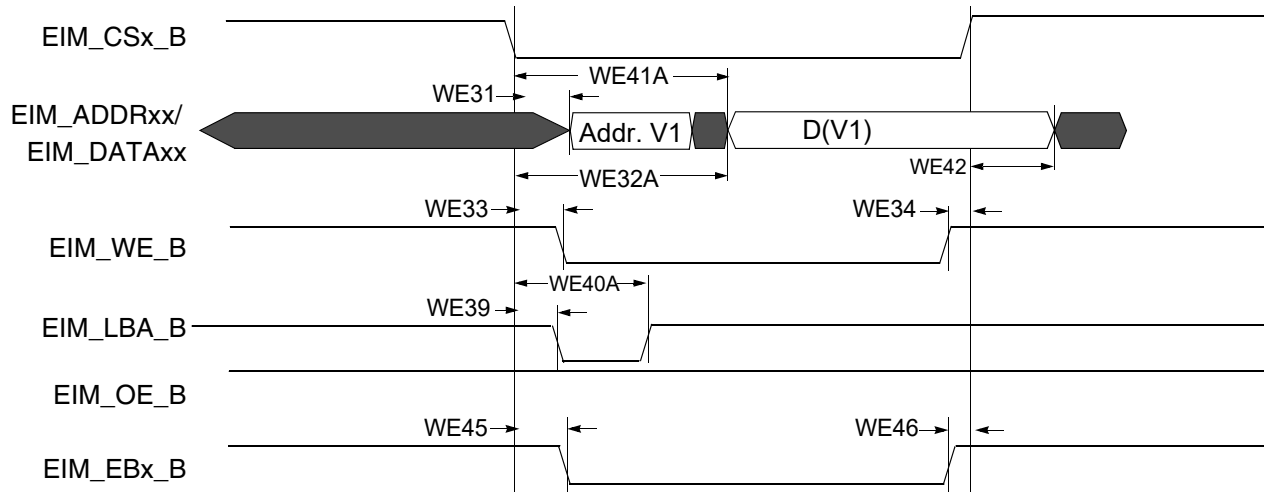


Figure 19. Asynchronous A/D Muxed Write Access

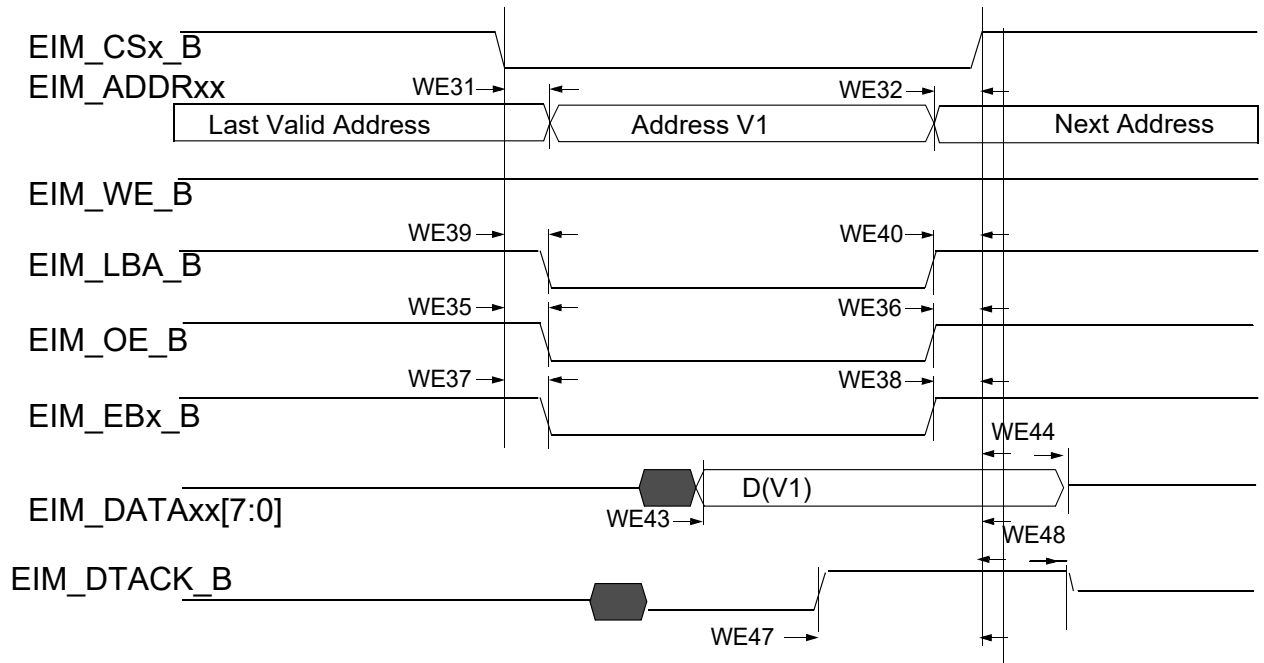


Figure 20. DTACK Mode Read Access (DAP=0)

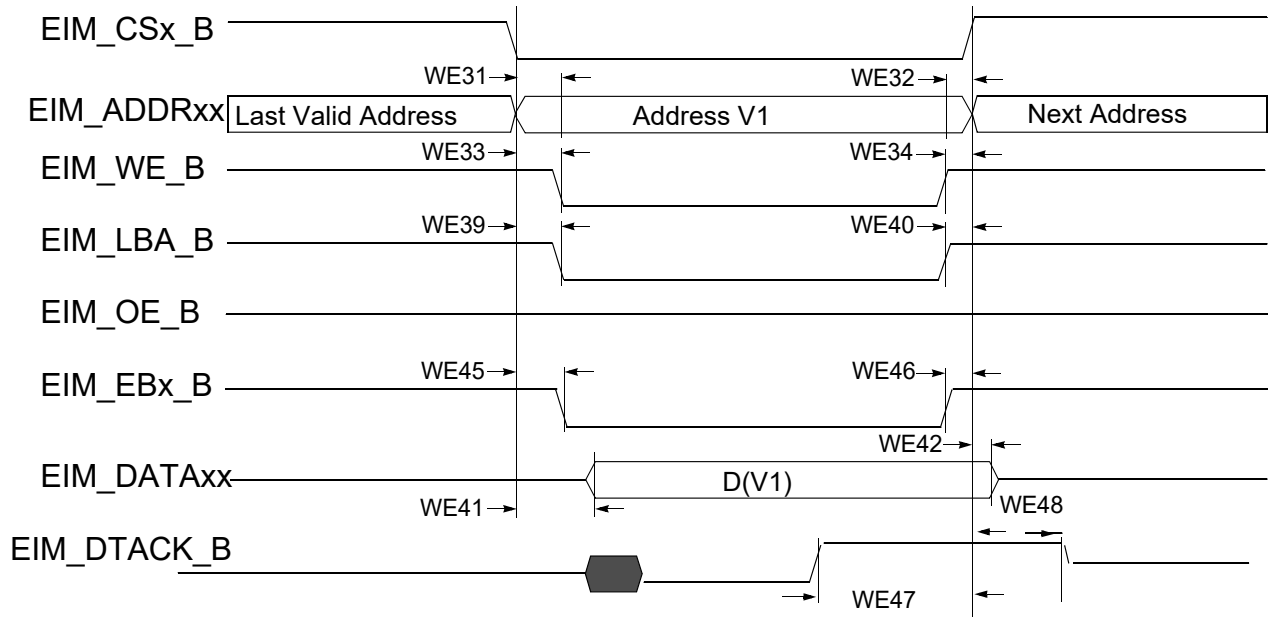


Figure 21. DTACK Mode Write Access (DAP=0)

Table 45. EIM Asynchronous Timing Parameters Relative to Chip Select^{1,2}

| Ref No. | Parameter | Determination by Synchronous measured parameters | Min | Max | Unit |
|-------------------|--|--|-------------------------------------|------------------------------------|------|
| WE31 | EIM_CSx_B valid to Address Valid | WE4-WE6-CSA×t | -3.5-CSA×t | 3.5-CSA×t | ns |
| WE32 | Address Invalid to EIM_CSx_B Invalid | WE7-WE5-CSN×t | -3.5-CSN×t | 3.5-CSN×t | ns |
| WE32A (muxed A/D) | EIM_CSx_B valid to Address Invalid | t+WE4-WE7+(ADVn+ADVA+1-CSA)×t | t - 3.5+(ADVn+A DVA+1-CSA)×t | t + 3.5+(ADVn+ADVA+1-CSA)×t | ns |
| WE33 | EIM_CSx_B Valid to EIM_WE_B Valid | WE8-WE6+(WEA-WCSA)×t | -3.5+(WEA-WCSA)×t | 3.5+(WEA-WCSA)×t | ns |
| WE34 | EIM_WE_B Invalid to EIM_CSx_B Invalid | WE7-WE9+(WEN-WCSN)×t | -3.5+(WEN-WCSN)×t | 3.5+(WEN-WCSN)×t | ns |
| WE35 | EIM_CSx_B Valid to EIM_OE_B Valid | WE10-WE6+(OEA-RCSA)×t | -3.5+(OEA-RCSA)×t | 3.5+(OEA-RCSA)×t | ns |
| WE35A (muxed A/D) | EIM_CSx_B Valid to EIM_OE_B Valid | WE10-WE6+(OEA+RADVN+RADVA+ADH+1-RCSA)×t | -3.5+(OEA+RADVN+RADVA+ADH+1-RCSA)×t | 3.5+(OEA+RADVN+RADVA+ADH+1-RCSA)×t | ns |
| WE36 | EIM_OE_B Invalid to EIM_CSx_B Invalid | WE7-WE11+(OEN-RCSN)×t | -3.5+(OEN-RCSN)×t | 3.5+(OEN-RCSN)×t | ns |
| WE37 | EIM_CSx_B Valid to EIM_EBx_B Valid (Read access) | WE12-WE6+(RBEA-RCSA)×t | -3.5+(RBEA-RCSA)×t | 3.5+(RBEA-RCSA)×t | ns |
| WE38 | EIM_EBx_B Invalid to EIM_CSx_B Invalid (Read access) | WE7-WE13+(RBEN-RCSN)×t | -3.5+(RBEN-RCSN)×t | 3.5+(RBEN-RCSN)×t | ns |

Electrical Characteristics

Table 45. EIM Asynchronous Timing Parameters Relative to Chip Select^{1,2} (continued)

| Ref No. | Parameter | Determination by Synchronous measured parameters | Min | Max | Unit |
|-------------------|---|--|--------------------------------|-------------------------------|------|
| WE39 | EIM_CSx_B Valid to EIM_LBA_B Valid | WE14-WE6+(ADVA-CSA)×t | -3.5+(ADVA-CSA)×t | 3.5+(ADVA-CSA)×t | ns |
| WE40 | EIM_LBA_B Invalid to EIM_CSx_B Invalid (ADVL is asserted) | WE7-WE15-CSN×t | -3.5-CSN×t | 3.5-CSN×t | ns |
| WE40A (muxed A/D) | EIM_CSx_B Valid to EIM_LBA_B Invalid | WE14-WE6+(ADVN+ADVA+1-CSA)×t | -3.5+(ADVN+ADVA+1-CSA)×t | 3.5+(ADVN+ADVA+1-CSA)×t | ns |
| WE41 | EIM_CSx_B Valid to Output Data Valid | WE16-WE6-WCSA×t | -3.5-WCSA×t | 3.5-WCSA×t | ns |
| WE41A (muxed A/D) | EIM_CSx_B Valid to Output Data Valid | WE16-WE6+(WADV+WADVA+ADH+1-WCSA)×t | -3.5+(WADV+WADVA+ADH+1-WCSA)×t | 3.5+(WADV+WADVA+ADH+1-WCSA)×t | ns |
| WE42 | Output Data Invalid to EIM_CSx_B Invalid | WE17-WE7-CSN×t | -3.5-CSN×t | 3.5-CSN×t | ns |
| MAXCO | Output maximum delay from internal driving EIM_ADDRxx/control flip-flops to chip outputs. | 10 | — | 10 | ns |
| MAXCSO | Output maximum delay from internal chip selects driving flip-flops to EIM_CSx_B out. | 10 | — | 10 | ns |
| MAXDI | EIM_DATAxx MAXIMUM delay from chip input data to its internal flip-flop | 5 | — | 5 | ns |
| WE43 | Input Data Valid to EIM_CSx_B Invalid | MAXCO-MAXCSO+MAXDI | MAXCO-MAXCSO+MAXDI | — | ns |
| WE44 | EIM_CSx_B Invalid to Input Data Invalid | 0 | 0 | — | ns |
| WE45 | EIM_CSx_B Valid to EIM_EBx_B Valid (Write access) | WE12-WE6+(WBEA-WCSA)×t | -3.5+(WBEA-WCSA)×t | 3.5+(WBEA-WCSA)×t | ns |
| WE46 | EIM_EBx_B Invalid to EIM_CSx_B Invalid (Write access) | WE7-WE13+(WBEN-WCSN)×t | -3.5+(WBEN-WCSN)×t | 3.5+(WBEN-WCSN)×t | ns |
| MAXDTI | Maximum delay from EIM_DTACK_B input to its internal flip-flop + 2 cycles for synchronization | 10 | — | 10 | ns |
| WE47 | EIM_DTACK_B Active to EIM_CSx_B Invalid | MAXCO-MAXCSO+MAXDTI | MAXCO-MAXCSO+MAXDTI | — | ns |
| WE48 | EIM_CSx_B Invalid to EIM_DTACK_B invalid | 0 | 0 | — | ns |

¹ For more information on configuration parameters mentioned in this table, see the *i.MX 6SoloX Applications Processor Reference Manual (IMX6SXRM)*.

² In this table:

t means clock period from axi_clk frequency.

CSA means register setting for WCSA when in write operations or RCSA when in read operations.

CSN means register setting for WCSN when in write operations or RCSN when in read operations.

ADVN means register setting for WADVN when in write operations or RADVN when in read operations.

ADVA means register setting for WADVA when in write operations or RADVA when in read operations.

4.10 Multi-mode DDR Controller (MMDC)

The Multi-mode DDR Controller is a dedicated interface to DDR3/DDR3L/LPDDR2 SDRAM.

4.10.1 MMDC Compatibility with JEDEC-Compliant SDRAMs

The i.MX 6SoloX MMDC supports the following memory types:

- LPDDR2 SDRAM compliant to JESD209-2B LPDDR2 JEDEC standard release June, 2009
- DDR3 SDRAM compliant to JESD79-3D DDR3 JEDEC standard release April, 2008

MMDC operation with the standards stated above is contingent upon the board DDR design adherence to the DDR design and layout requirements stated in the Hardware Development Guide for i.MX 6SoloX Application Processors (IMX6SXHDG).

4.10.2 MMDC Supported DDR3/LPDDR2 Configurations

The table below shows the supported DDR3/LPDDR2 configurations:

Table 46. i.MX 6SoloX Supported DDR3/LPDDR2 Configurations

| Parameter | Min | Max | Unit |
|--|------------|-----|---------|
| LPDDR2 | | | |
| JEDEC LPDDR2 Device Speed Grade ¹ | LPDDR2-800 | — | — |
| JEDEC LPDDR2 Device Bus Width | x16 | x32 | Bits |
| JEDEC LPDDR2 Device Count ² | 1 | 2 | Devices |
| DDR3/DDR3L | | | |
| JEDEC DDR3/DDR3L Device Speed Grade ³ | DDR3-800 | — | — |
| JEDEC DDR3/DDR3L Device Bus Width | x16 | x32 | Bits |
| JEDEC DDR3/DDR3L Device Count ⁴ | 1 | 2 | Devices |

¹ Higher speed grade memories are supported as long as they are backward compatible with the speed grade shown.

² Supported configurations are one 32-bit DDR memory or two 16-bit DDR memories.

³ Higher speed grade memories are supported as long as they are backward compatible with the speed grade shown.

⁴ Supported configurations are one 32-bit DDR memory or two 16-bit DDR memories.

4.11 General-Purpose Media Interface (GPMI) Timing

The i.MX 6SoloX GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select.

It supports Asynchronous timing mode, Source Synchronous timing mode and Samsung Toggle timing mode separately described in the following subsections.

4.11.1 Asynchronous Mode AC Timing (ONFI 1.0 Compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The maximum I/O speed of GPMI in asynchronous mode is about 50 MB/s. Figure 22 through Figure 25 depicts the relative timing between GPMI signals at the module level for different operations under asynchronous mode. Table 47 describes the timing parameters (NF1–NF17) that are shown in the figures.

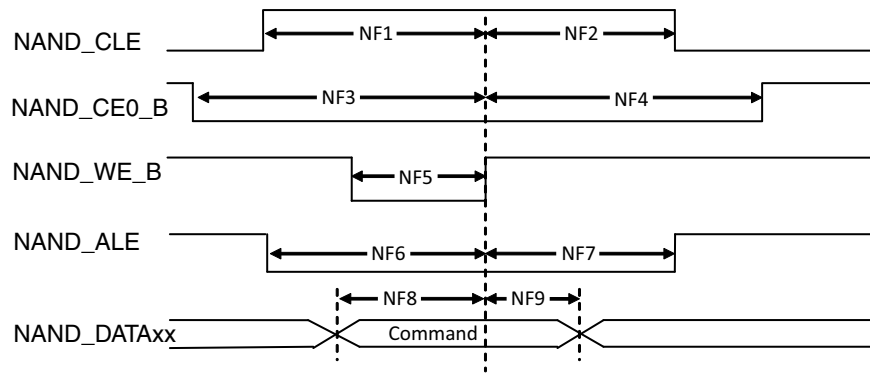


Figure 22. Command Latch Cycle Timing Diagram

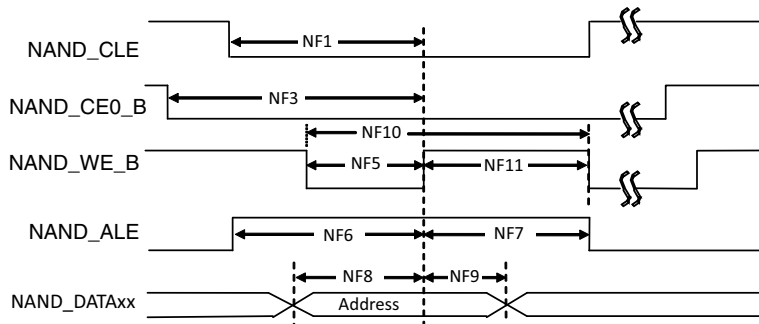


Figure 23. Address Latch Cycle Timing Diagram

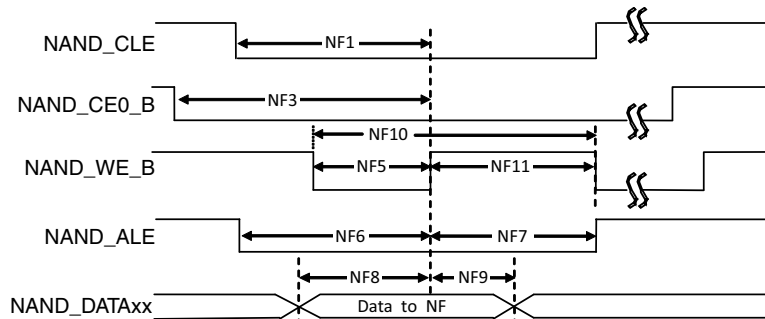


Figure 24. Write Data Latch Cycle Timing Diagram

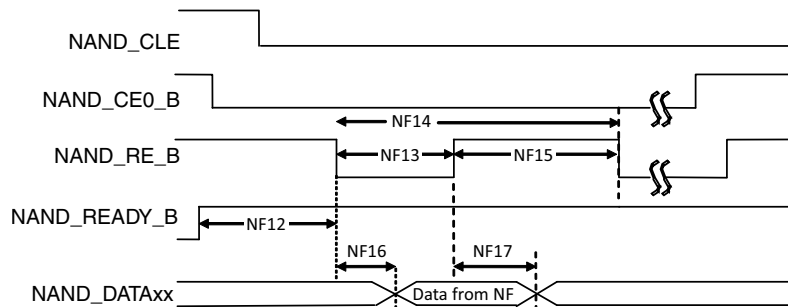


Figure 25. Read Data Latch Cycle Timing Diagram (Non-EDO Mode)

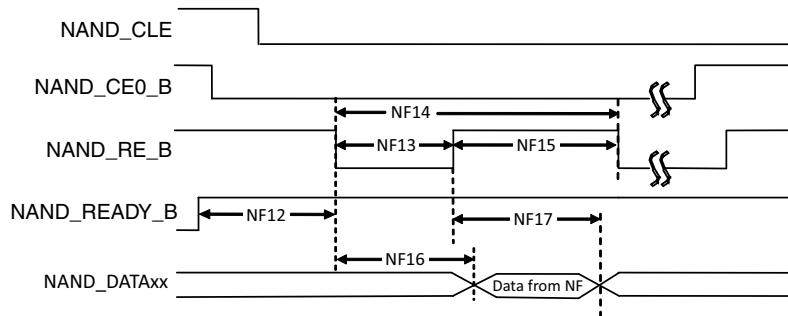


Figure 26. Read Data Latch Cycle Timing Diagram (EDO Mode)

Table 47. Asynchronous Mode Timing Parameters¹

| ID | Parameter | Symbol | Timing T = GPMI Clock Cycle | | Unit |
|-----|-----------------------|--------|---|-----|------|
| | | | Min | Max | |
| NF1 | NAND_CLE setup time | tCLS | $(AS + DS) \times T - 0.12$ [see ^{2,3}] | | ns |
| NF2 | NAND_CLE hold time | tCLH | $DH \times T - 0.72$ [see ²] | | ns |
| NF3 | NAND_CE0_B setup time | tCS | $(AS + DS + 1) \times T$ [see ^{3,2}] | | ns |
| NF4 | NAND_CE0_B hold time | tCH | $(DH+1) \times T - 1$ [see ²] | | ns |
| NF5 | NAND_WE_B pulse width | tWP | $DS \times T$ [see ²] | | ns |
| NF6 | NAND_ALE setup time | tALS | $(AS + DS) \times T - 0.49$ [see ^{3,2}] | | ns |
| NF7 | NAND_ALE hold time | tALH | $(DH \times T - 0.42$ [see ²] | | ns |

Table 47. Asynchronous Mode Timing Parameters¹ (continued)

| ID | Parameter | Symbol | Timing T = GPMI Clock Cycle | | Unit |
|------|--------------------------|------------------|------------------------------------|---|------|
| | | | Min | Max | |
| NF8 | Data setup time | tDS | DS × T - 0.26 [see ²] | | ns |
| NF9 | Data hold time | tDH | DH × T - 1.37 [see ²] | | ns |
| NF10 | Write cycle time | tWC | (DS + DH) × T [see ²] | | ns |
| NF11 | NAND_WE_B hold time | tWH | DH × T [see ²] | | ns |
| NF12 | Ready to NAND_RE_B low | tRR ⁴ | (AS + 2) × T [see ^{3,2}] | — | ns |
| NF13 | NAND_RE_B pulse width | tRP | DS × T [see ²] | | ns |
| NF14 | READ cycle time | tRC | (DS + DH) × T [see ²] | | ns |
| NF15 | NAND_RE_B high hold time | tREH | DH × T [see ²] | | ns |
| NF16 | Data setup on read | tDSR | — | (DS × T - 0.67)/18.38 [see ^{5,6}] | ns |
| NF17 | Data hold on read | tDHR | 0.82/11.83 [see ^{5,6}] | — | ns |

¹ GPMI's Async Mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

² AS minimum value can be 0, while DS/DH minimum value is 1.

³ T = GPMI clock period - 0.075ns (half of maximum p-p jitter).

⁴ NF12 is guaranteed by the design.

⁵ Non-EDO mode.

⁶ EDO mode, GPMI clock ≈ 100 MHz
(AS=DS=DH=1, GPMI_CTRL1 [RDN_DELAY] = 8, GPMI_CTRL1 [HALF_PERIOD] = 0).

In EDO mode (Figure 25), NF16/NF17 are different from the definition in non-EDO mode (Figure 24). They are called tREA/tRHOH (RE# access time/RE# HIGH to output hold). The typical value for them are 16 ns (max for tREA)/15 ns (min for tRHOH) at 50 MB/s EDO mode. In EDO mode, GPMI will sample NAND_DATAxx at rising edge of delayed NAND_RE_B provided by an internal DPLL. The delay value can be controlled by GPMI_CTRL1.RDN_DELAY (see the GPMI chapter of the *i.MX 6SoloX Applications Processor Reference Manual (IMX6SXR)*). The typical value of this control register is 0x8 at 50 MT/s EDO mode. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.11.2 Source Synchronous Mode AC Timing (ONFI 2.x Compatible)

Figure 27 to Figure 29 show the write and read timing of Source Synchronous Mode.

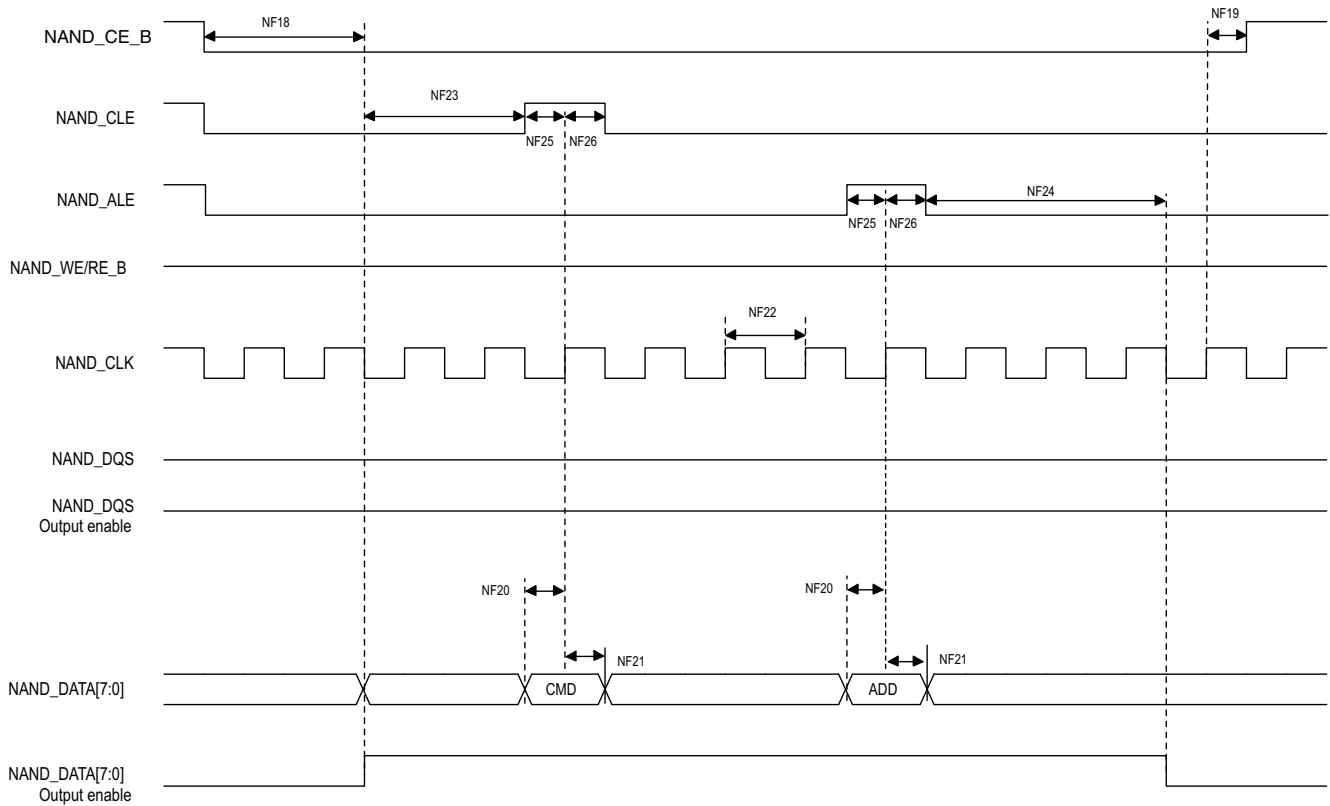


Figure 27. Source Synchronous Mode Command and Address Timing Diagram

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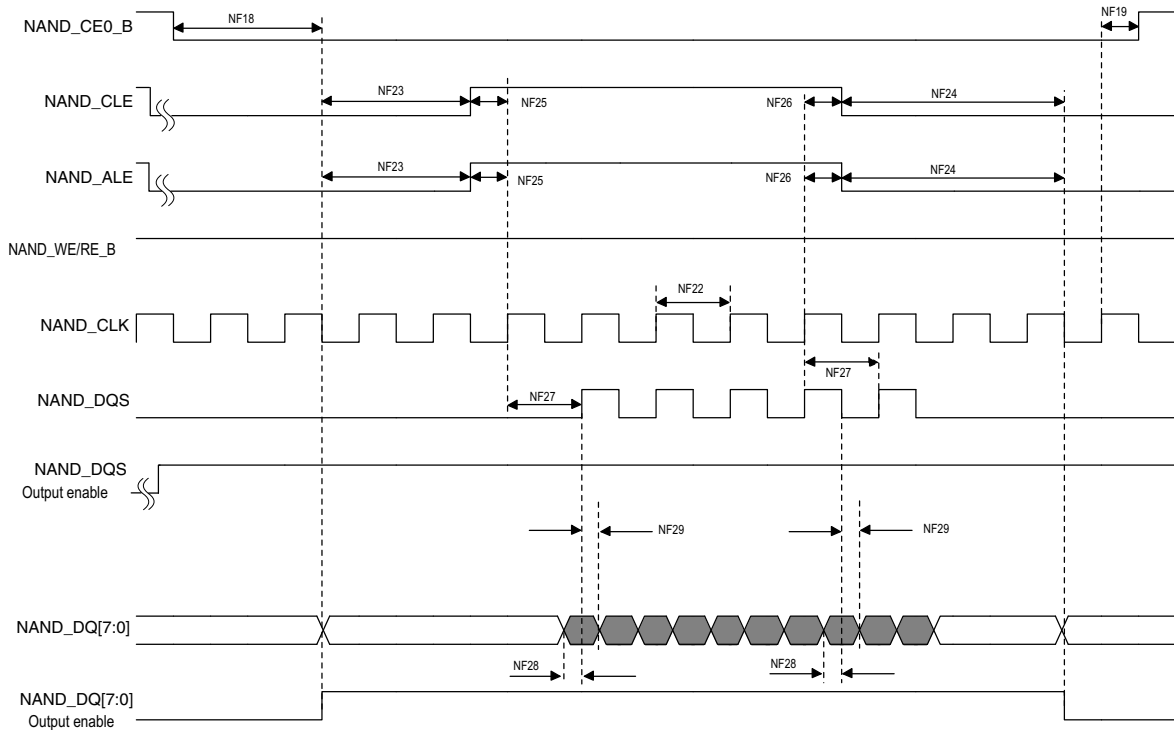


Figure 28. Source Synchronous Mode Data Write Timing Diagram

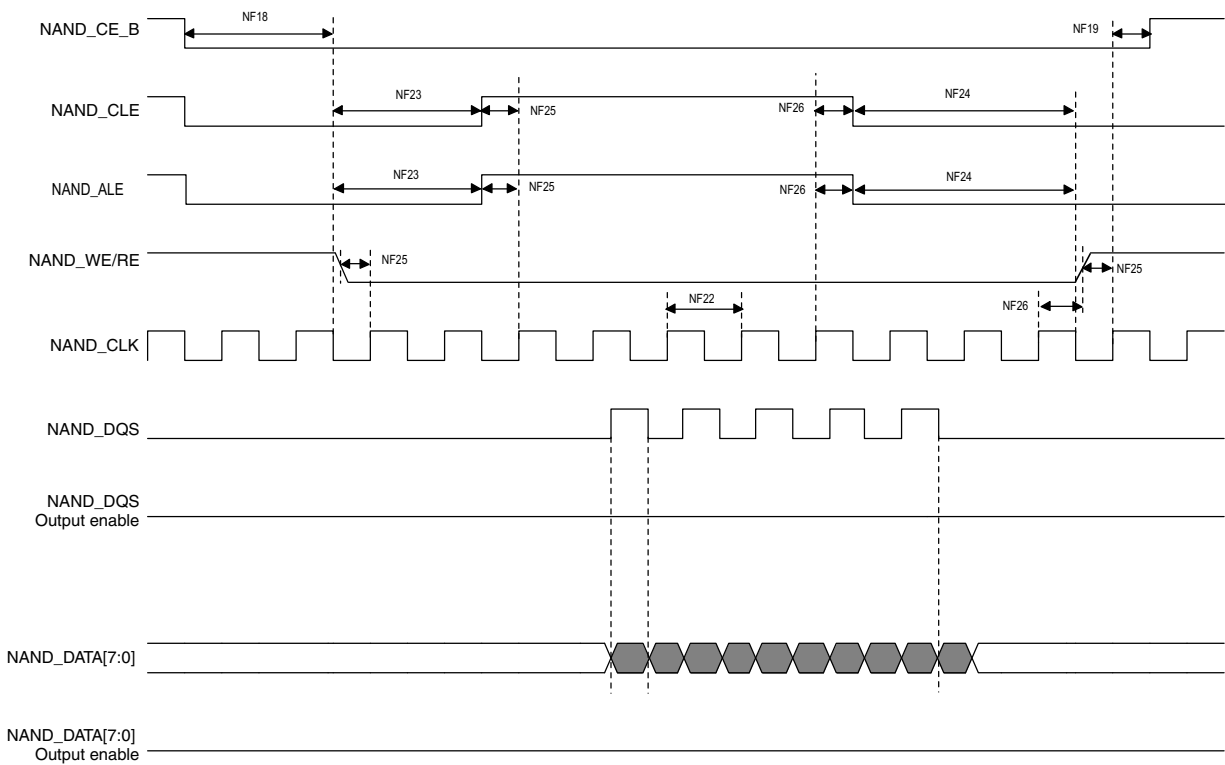


Figure 29. Source Synchronous Mode Data Read Timing Diagram

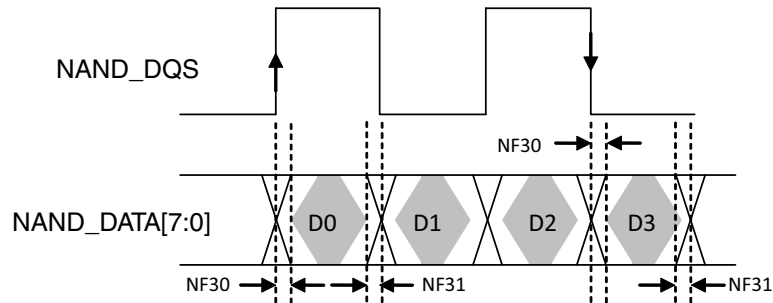


Figure 30. NAND_DQS/NAND_DQ Read Valid Window

Table 48. Source Synchronous Mode Timing Parameters¹

| ID | Parameter | Symbol | Timing T = GPMI Clock Cycle | | Unit |
|------|---|--------|---|------|------|
| | | | Min | Max | |
| NF18 | NAND_CEO_B access time | tCE | $CE_DELAY \times T - 0.79$ [see ²] | | ns |
| NF19 | NAND_CEO_B hold time | tCH | $0.5 \times tCK - 0.63$ [see ²] | | ns |
| NF20 | Command/address NAND_DATA _{Axx} setup time | tCAS | $0.5 \times tCK - 0.05$ | | ns |
| NF21 | Command/address NAND_DATA _{Axx} hold time | tCAH | $0.5 \times tCK - 1.23$ | | ns |
| NF22 | clock period | tCK | — | | ns |
| NF23 | preamble delay | tPRE | $PRE_DELAY \times T - 0.29$ [see ²] | | ns |
| NF24 | postamble delay | tPOST | $POST_DELAY \times T - 0.78$ [see ²] | | ns |
| NF25 | NAND_CLE and NAND_ALE setup time | tCALS | $0.5 \times tCK - 0.86$ | | ns |
| NF26 | NAND_CLE and NAND_ALE hold time | tCALH | $0.5 \times tCK - 0.37$ | | ns |
| NF27 | NAND_CLK to first NAND_DQS latching transition | tDQSS | $T - 0.41$ [see ²] | | ns |
| NF28 | Data write setup | — | $0.25 \times tCK - 0.35$ | | — |
| NF29 | Data write hold | — | $0.25 \times tCK - 0.85$ | | — |
| NF30 | NAND_DQS/NAND_DQ read setup skew | — | — | 2.06 | — |
| NF31 | NAND_DQS/NAND_DQ read hold skew | — | — | 1.95 | — |

¹ GPMI's source synchronous mode output timing can be controlled by the module's internal registers GPMI_TIMING2_CE_DELAY, GPMI_TIMING2_PREAMBLE_DELAY, GPMI_TIMING2_POST_DELAY. This timing depends on these registers settings. In the table, CE_DELAY/PREAMBLE_DELAY/POST_DELAY represents each of these settings.

² T = tCK (GPMI clock period) - 0.075 ns (half of maximum p-p jitter).

For DDR Source sync mode, Figure 30 shows the timing diagram of NAND_DQS/NAND_DATA_{Axx} read valid window. The typical value of tDQSQ is 0.85 ns (max) and 1 ns (max) for tQHS at 200 MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of a delayed NAND_DQS signal, which can be provided by an internal DPLL. The delay value can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the *i.MX 6SoloX Applications Processor Reference Manual (IMX6SXR)*). Generally, the typical delay value of this register is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.11.3 Samsung Toggle Mode AC Timing

4.11.3.1 Command and Address Timing

NOTE

Samsung Toggle Mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. See [Section 4.11.1, “Asynchronous Mode AC Timing \(ONFI 1.0 Compatible\),”](#) for details.

4.11.3.2 Read and Write Timing

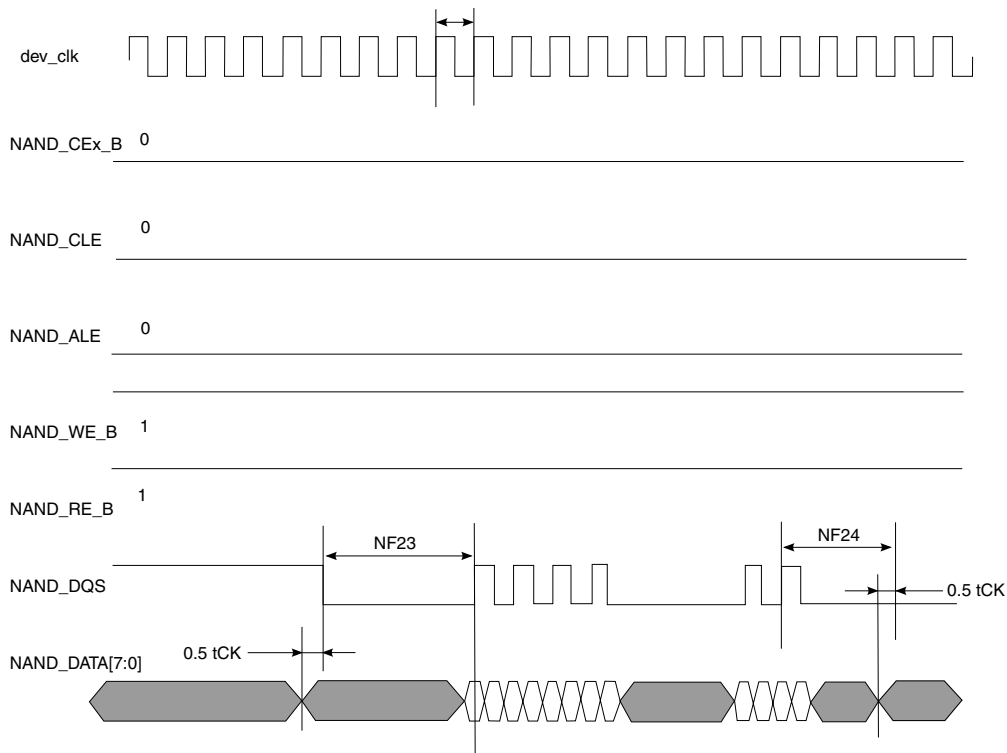


Figure 31. Samsung Toggle Mode Data Write Timing

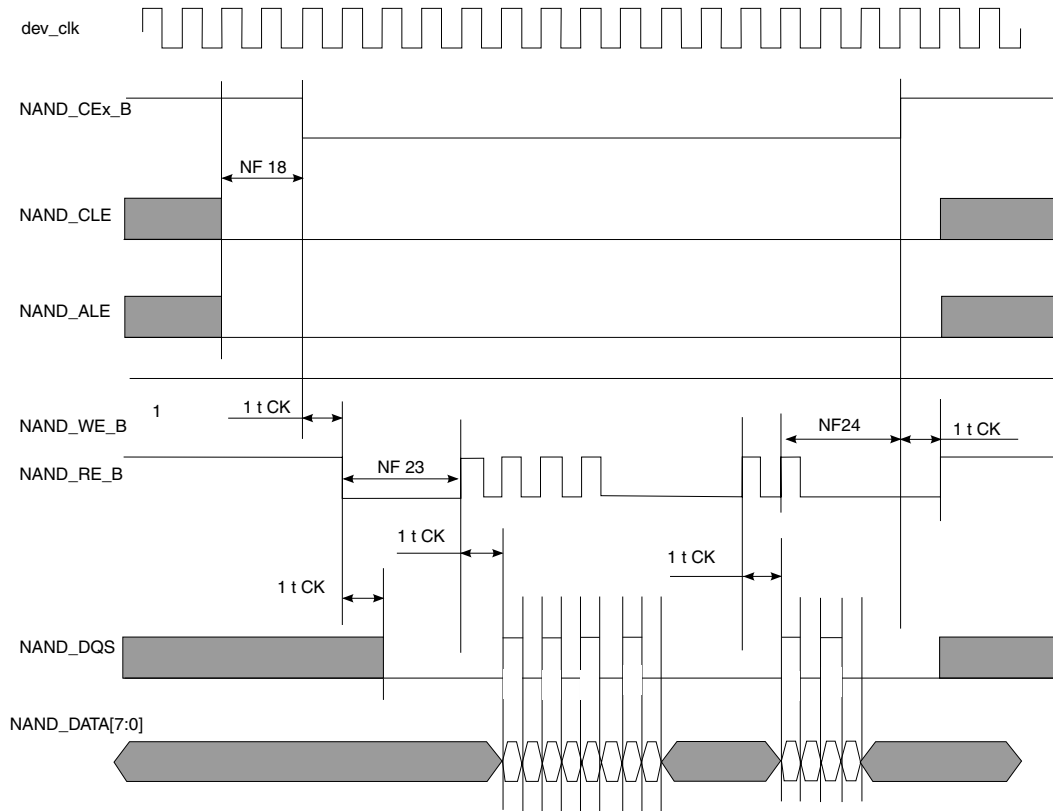


Figure 32. Samsung Toggle Mode Data Read Timing

Table 49. Samsung Toggle Mode Timing Parameters¹

| ID | Parameter | Symbol | Timing T = GPMI Clock Cycle | | Unit |
|------|--|--------|---|-----|------|
| | | | Min | Max | |
| NF1 | NAND_CLE setup time | tCLS | $(AS + DS) \times T - 0.12$ [see ^{2,3}] | | — |
| NF2 | NAND_CLE hold time | tCLH | $DH \times T - 0.72$ [see ²] | | — |
| NF3 | NAND_CE0_B setup time | tCS | $(AS + DS) \times T - 0.58$ [see ^{3,2}] | | — |
| NF4 | NAND_CE0_B hold time | tCH | $DH \times T - 1$ [see ²] | | — |
| NF5 | NAND_WE_B pulse width | tWP | $DS \times T$ [see ²] | | — |
| NF6 | NAND_ALE setup time | tALS | $(AS + DS) \times T - 0.49$ [see ^{3,2}] | | — |
| NF7 | NAND_ALE hold time | tALH | $DH \times T - 0.42$ [see ²] | | — |
| NF8 | Command/address NAND_DATAxx setup time | tCAS | $DS \times T - 0.26$ [see ²] | | — |
| NF9 | Command/address NAND_DATAxx hold time | tCAH | $DH \times T - 1.37$ [see ²] | | — |
| NF18 | NAND_CEx_B access time | tCE | $CE_DELAY \times T$ [see ^{4,2}] | — | ns |
| NF22 | clock period | tCK | — | — | ns |
| NF23 | preamble delay | tPRE | $PRE_DELAY \times T$ [see ^{5,2}] | — | ns |
| NF24 | postamble delay | tPOST | $POST_DELAY \times T + 0.43$ [see ²] | — | ns |

Table 49. Samsung Toggle Mode Timing Parameters¹ (continued)

| ID | Parameter | Symbol | Timing T = GPMI Clock Cycle | | Unit |
|------|----------------------------------|--------------------|--------------------------------|------|------|
| | | | Min | Max | |
| NF28 | Data write setup | tDS ⁶ | 0.25 × tCK - 0.32 | — | ns |
| NF29 | Data write hold | tDH ⁶ | 0.25 × tCK - 0.79 | — | ns |
| NF30 | NAND_DQS/NAND_DQ read setup skew | tDQSQ ⁷ | — | 3.18 | — |
| NF31 | NAND_DQS/NAND_DQ read hold skew | tQHS ⁷ | — | 3.27 | — |

- ¹ The GPMI toggle mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.
- ² AS minimum value can be 0, while DS/DH minimum value is 1.
- ³ T = tCK (GPMI clock period) - 0.075ns (half of maximum p-p jitter).
- ⁴ CE_DELAY represents HW_GPMI_TIMING2[CE_DELAY]. NF18 is guaranteed by the design. Read/Write operation is started with enough time of ALE/CLE assertion to low level.
- ⁵ PRE_DELAY+1) ≥ (AS+DS)
- ⁶ Shown in Figure 31.
- ⁷ Shown in Figure 32.

For DDR Toggle mode, Figure 30 shows the timing diagram of NAND_DQS/NAND_DATA_{xx} read valid window. The typical value of tDQSQ is 1.4 ns (max) and 1.4 ns (max) for tQHS at 133 MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of a delayed NAND_DQS signal, which is provided by an internal DPLL. The delay value of this register can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the *i.MX 6SoloX Applications Processor Reference Manual (IMX6SXR)*). Generally, the typical delay value is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.12 External Peripheral Interface Parameters

The following subsections provide information on external peripheral interfaces.

4.12.1 AUDMUX Timing Parameters

The AUDMUX provides a programmable interconnect logic for voice, audio, and data routing between internal serial interfaces (SSIs) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is governed by the SSI module. For more information, see the respective SSI electrical specifications found within this document.

4.12.2 CMOS Sensor Interface (CSI) Timing Parameters

The CSI enables the chip to connect directly to external CMOS image sensors, which are classified as dumb or smart as follows:

- Dumb sensors only support traditional sensor timing (vertical sync (VSYNC) and horizontal sync (HSYNC)) and output-only Bayer and statistics data.

- Smart sensors support CCIR656 video decoder formats and perform additional processing of the image (for example, image compression, image pre-filtering, and various data output formats).

The following subsections describe the CSI timing in gated and ungated clock modes.

4.12.2.1 Gated Clock Mode Timing

Figure 33 and Figure 34 shows the gated clock mode timings for CSI, and Table 50 describes the timing parameters (P1–P7) shown in the figures. A frame starts with a rising/falling edge on CSI_VSYNC (VSYNC), then CSI_HSYNC (HSYNC) is asserted and holds for the entire line. The pixel clock, CSI_PIXCLK (PIXCLK), is valid as long as HSYNC is asserted.

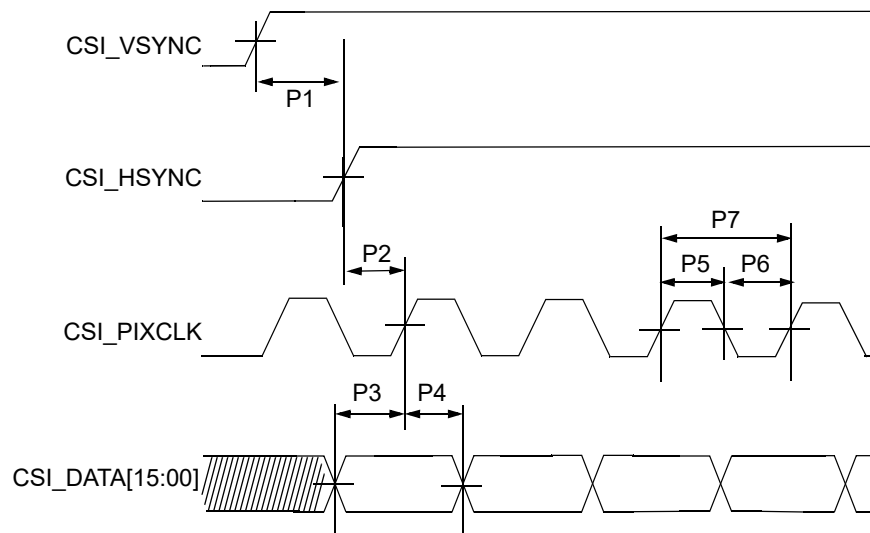


Figure 33. CSI Gated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

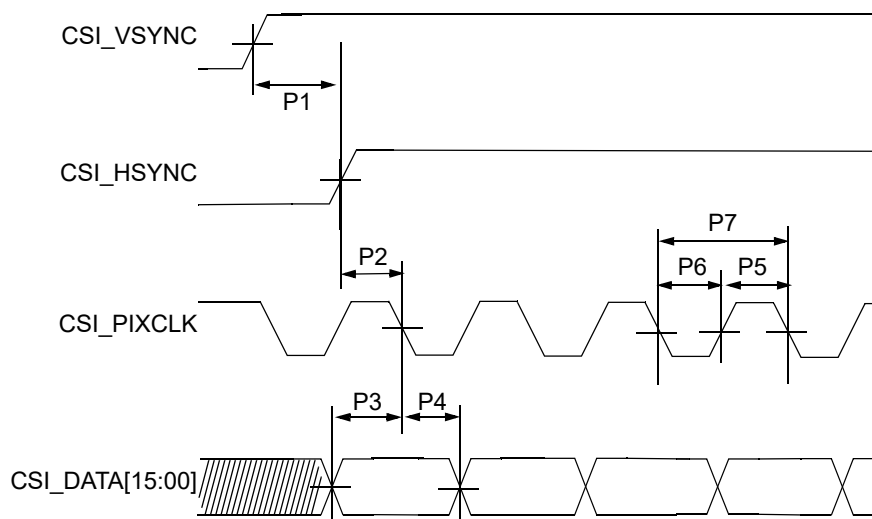


Figure 34. CSI Gated Clock Mode—Sensor Data at Rising Edge, Latch Data at Falling Edge

Table 50. CSI Gated Clock Mode Timing Parameters

| ID | Parameter | Symbol | Min | Max | Units |
|----|-----------------------------|--------|------|-----|-------|
| P1 | CSI_VSYNC to CSI_HSYNC time | tV2H | 33.5 | — | ns |
| P2 | CSI_HSYNC setup time | tHsu | 1 | — | ns |
| P3 | CSI DATA setup time | tDsu | 1 | — | ns |
| P4 | CSI DATA hold time | tDh | 1 | — | ns |
| P5 | CSI pixel clock high time | tCLKh | 3.75 | — | ns |
| P6 | CSI pixel clock low time | tCLKl | 3.75 | — | ns |
| P7 | CSI pixel clock frequency | fCLK | — | 133 | MHz |

4.12.2.2 Ungated Clock Mode Timing

Figure 35 shows the ungated clock mode timings of CSI, and Table 51 describes the timing parameters (P1–P6) that are shown in the figure. In ungated mode the CSI_VSYNC and CSI_PIXCLK signals are used, and the CSI_HSYNC signal is ignored.

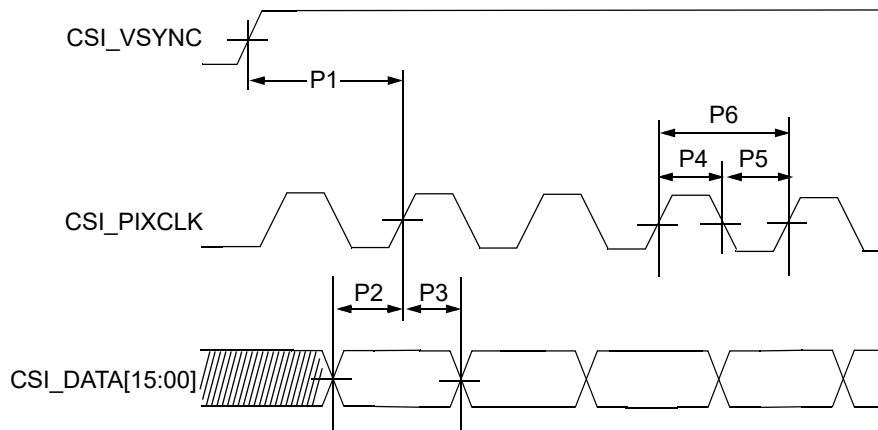


Figure 35. CSI Ungated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

Table 51. CSI Ungated Clock Mode Timing Parameters

| ID | Parameter | Symbol | Min | Max | Units |
|----|-------------------------------|--------|------|-----|-------|
| P1 | CSI_VSYNC to pixel clock time | tVSYNC | 33.5 | — | ns |
| P2 | CSI DATA setup time | tDsu | 1 | — | ns |
| P3 | CSI DATA hold time | tDh | 1 | — | ns |
| P4 | CSI pixel clock high time | tCLKh | 3.75 | — | ns |
| P5 | CSI pixel clock low time | tCLKl | 3.75 | — | ns |
| P6 | CSI pixel clock frequency | fCLK | — | 133 | MHz |

4.12.3 ECSPi Timing Parameters

This section describes the timing parameters of the ECSPi blocks. The ECSPi have separate timing parameters for master and slave modes.

4.12.3.1 ECSPi Master Mode Timing

Figure 36 depicts the timing of ECSPi in master mode. Table 52 lists the ECSPi master mode timing characteristics.

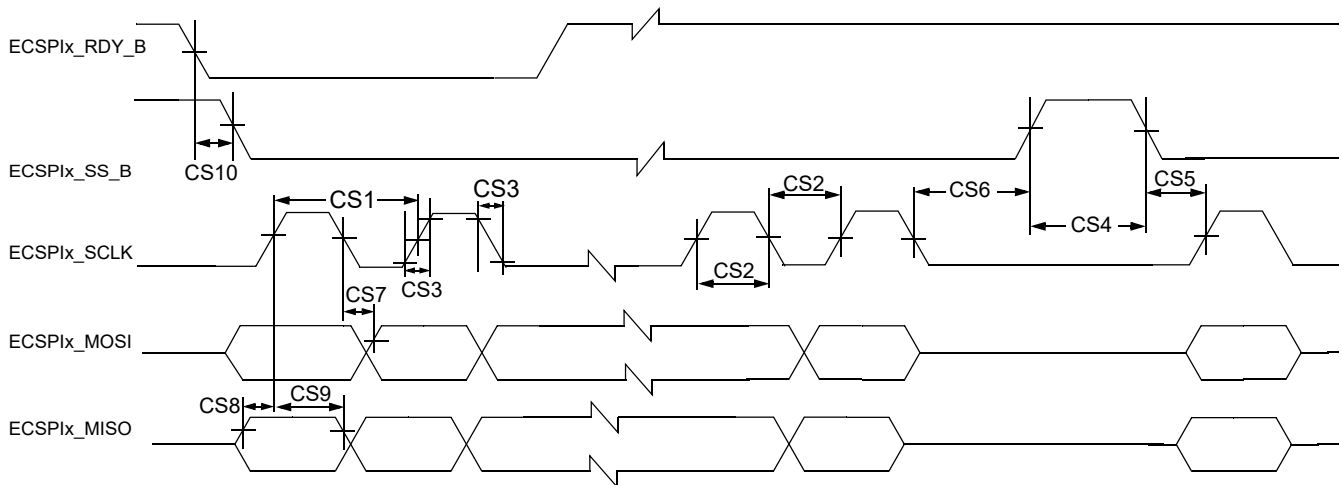


Figure 36. ECSPi Master Mode Timing Diagram

NOTE

ECSPi_x_MOSI is always driven (not tri-stated) between actual data transmissions. This limits the ECSPi to be connected between a single master and a single slave.

Table 52. ECSPi Master Mode Timing Parameters

| ID | Parameter | Symbol | Min | Max | Unit |
|-----|---|-----------------|--|-----|------|
| CS1 | ECSPi _x _SCLK Cycle Time–Read ECSPi _x _SCLK Cycle Time–Write | t_{clk} | 43 15 | — | ns |
| CS2 | ECSPi _x _SCLK High or Low Time–Read ECSPi _x _SCLK High or Low Time–Write | t_{sw} | 21.5 7 | — | ns |
| CS3 | ECSPi _x _SCLK Rise or Fall ¹ | $t_{RISE/FALL}$ | — | — | ns |
| CS4 | ECSPi _x _SS_B pulse width | t_{CSLH} | Half ECSPi _x _SCLK period | — | ns |
| CS5 | ECSPi _x _SS_B Lead Time (CS setup time) | t_{SCS} | Half ECSPi _x _SCLK period - 4 | — | ns |
| CS6 | ECSPi _x _SS_B Lag Time (CS hold time) | t_{HCS} | Half ECSPi _x _SCLK period - 2 | — | ns |
| CS7 | ECSPi _x _MOSI Propagation Delay ($C_{LOAD} = 20$ pF) | t_{PDmosi} | -1 | 1 | ns |
| CS8 | ECSPi _x _MISO Setup Time | t_{Smiso} | 14 | — | ns |

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Table 52. ECSPi Master Mode Timing Parameters (continued)

| ID | Parameter | Symbol | Min | Max | Unit |
|------|---|-------------|-----|-----|------|
| CS9 | ECSPi _x _MISO Hold Time | t_{Hmiso} | 0 | — | ns |
| CS10 | RDY to ECSPi _x _SS_B Time ² | t_{SDRY} | 5 | — | ns |

¹ See specific I/O AC parameters [Section 4.7, “I/O AC Parameters.”](#)

² SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.12.3.2 ECSPi Slave Mode Timing

[Figure 37](#) depicts the timing of ECSPi in slave mode. [Table 53](#) lists the ECSPi slave mode timing characteristics.

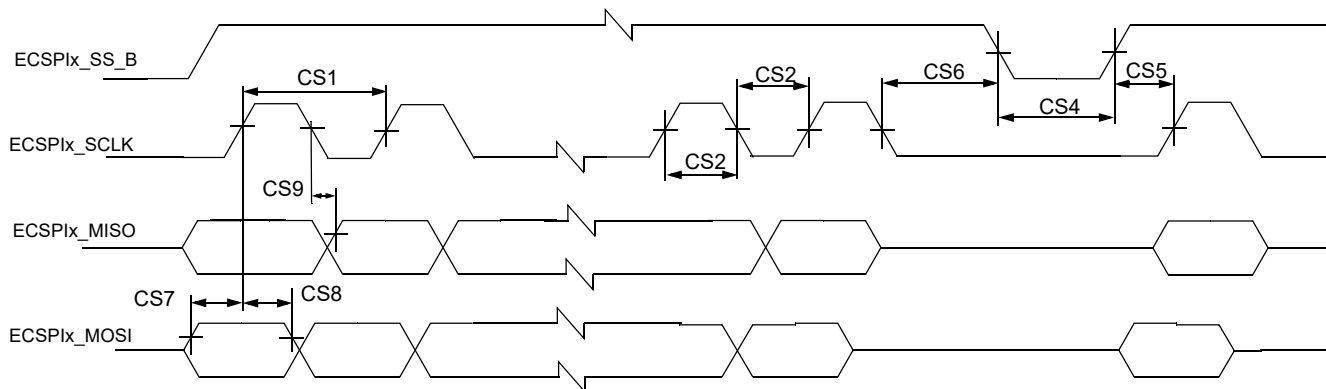


Figure 37. ECSPi Slave Mode Timing Diagram

NOTE

ECSPi_x_MISO is always driven (not tri-stated) between actual data transmissions. This limits the ECSPi to be connected between a single master and a single slave.

Table 53. ECSPi Slave Mode Timing Parameters

| ID | Parameter | Symbol | Min | Max | Unit |
|-----|---|--------------|--------------------------------------|-----|------|
| CS1 | ECSPi _x _SCLK Cycle Time–Read ECSPi _x _SCLK Cycle Time–Write | t_{clk} | 15 43 | — | ns |
| CS2 | ECSPi _x _SCLK High or Low Time–Read ECSPi _x _SCLK High or Low Time–Write | t_{sw} | 7 21.5 | — | ns |
| CS4 | ECSPi _x _SS_B pulse width | t_{CSLH} | Half ECSPi _x _SCLK period | — | ns |
| CS5 | ECSPi _x _SS_B Lead Time (CS setup time) | t_{SCS} | 5 | — | ns |
| CS6 | ECSPi _x _SS_B Lag Time (CS hold time) | t_{HCS} | 5 | — | ns |
| CS7 | ECSPi _x _MOSI Setup Time | t_{Smosi} | 4 | — | ns |
| CS8 | ECSPi _x _MOSI Hold Time | t_{Hmosi} | 4 | — | ns |
| CS9 | ECSPi _x _MISO Propagation Delay ($C_{LOAD} = 20$ pF) | t_{PDmiso} | 4 | 19 | ns |

4.12.4 Enhanced Serial Audio Interface (ESAI) Timing Parameters

The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. Table 54 shows the interface timing values. The number field in the table refers to timing signals found in Figure 38 and Figure 39.

Table 54. Enhanced Serial Audio Interface (ESAI) Timing

| No. | Characteristics ^{1,2} | Symbol | Expression ² | Min | Max | Condition ³ | Unit |
|-----|--|-------------|--|--------------|--------------|------------------------|------|
| 62 | Clock cycle ⁴ | t_{SSICC} | $4 \times T_C$ $4 \times T_C$ | 30.0 30.0 | — — | i ck i ck | ns |
| 63 | Clock high period: • For internal clock • For external clock | — — | $2 \times T_C - 9.0$ $2 \times T_C$ | 6 15 | — — | — — | ns |
| 64 | Clock low period: • For internal clock • For external clock | — — | $2 \times T_C - 9.0$ $2 \times T_C$ | 6 15 | — — | — — | ns |
| 65 | ESAI_RX_CLK rising edge to ESAI_RX_FS out (bl) high | — — | — — | — — | 17.0 7.0 | x ck i ck a | ns |
| 66 | ESAI_RX_CLK rising edge to ESAI_RX_FS out (bl) low | — — | — — | — — | 17.0 7.0 | x ck i ck a | ns |
| 67 | ESAI_RX_CLK rising edge to ESAI_RX_FS out (wr) high ⁵ | — — | — — | — — | 19.0 9.0 | x ck i ck a | ns |
| 68 | ESAI_RX_CLK rising edge to ESAI_RX_FS out (wr) low ⁵ | — — | — — | — — | 19.0 9.0 | x ck i ck a | ns |
| 69 | ESAI_RX_CLK rising edge to ESAI_RX_FS out (wl) high | — — | — — | — — | 16.0 6.0 | x ck i ck a | ns |
| 70 | ESAI_RX_CLK rising edge to ESAI_RX_FS out (wl) low | — — | — — | — — | 17.0 7.0 | x ck i ck a | ns |
| 71 | Data in setup time before ESAI_RX_CLK (SCK in synchronous mode) falling edge | — — | — — | 12.0 19.0 | — — | x ck i ck | ns |
| 72 | Data in hold time after ESAI_RX_CLK falling edge | — — | — — | 3.5 9.0 | — — | x ck i ck | ns |
| 73 | ESAI_RX_FS input (bl, wr) high before ESAI_RX_CLK falling edge ⁵ | — — | — — | 2.0 12.0 | — — | x ck i ck a | ns |
| 74 | ESAI_RX_FS input (wl) high before ESAI_RX_CLK falling edge | — — | — — | 2.0 12.0 | — — | x ck i ck a | ns |
| 75 | ESAI_RX_FS input hold time after ESAI_RX_CLK falling edge | — — | — — | 2.5 8.5 | — — | x ck i ck a | ns |
| 78 | ESAI_TX_CLK rising edge to ESAI_TX_FS out (bl) high | — — | — — | — — | 18.0 8.0 | x ck i ck | ns |
| 79 | ESAI_TX_CLK rising edge to ESAI_TX_FS out (bl) low | — — | — — | — — | 20.0 10.0 | x ck i ck | ns |
| 80 | ESAI_TX_CLK rising edge to ESAI_TX_FS out (wr) high ⁵ | — — | — — | — — | 20.0 10.0 | x ck i ck | ns |

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Table 54. Enhanced Serial Audio Interface (ESAI) Timing (continued)

| No. | Characteristics ^{1,2} | Symbol | Expression ² | Min | Max | Condition ³ | Unit |
|-----|---|--------|-------------------------|-------------|--------------|------------------------|------|
| 81 | ESAI_TX_CLK rising edge to ESAI_TX_FS out (wr) low ⁵ | — — | — — | — — | 22.0 12.0 | x ck i ck | ns |
| 82 | ESAI_TX_CLK rising edge to ESAI_TX_FS out (wl) high | — — | — — | — — | 19.0 9.0 | x ck i ck | ns |
| 83 | ESAI_TX_CLK rising edge to ESAI_TX_FS out (wl) low | — — | — — | — — | 20.0 10.0 | x ck i ck | ns |
| 84 | ESAI_TX_CLK rising edge to data out enable from high impedance | — — | — — | — — | 22.0 17.0 | x ck i ck | ns |
| 86 | ESAI_TX_CLK rising edge to data out valid | — — | — — | — — | 18.0 13.0 | x ck i ck | ns |
| 87 | ESAI_TX_CLK rising edge to data out high impedance ⁶⁷ | — — | — — | — — | 21.0 16.0 | x ck i ck | ns |
| 89 | ESAI_TX_FS input (bl, wr) setup time before ESAI_TX_CLK falling edge ⁵ | — — | — — | 2.0 18.0 | — — | x ck i ck | ns |
| 90 | ESAI_TX_FS input (wl) setup time before ESAI_TX_CLK falling edge | — — | — — | 2.0 18.0 | — — | x ck i ck | ns |
| 91 | ESAI_TX_FS input hold time after ESAI_TX_CLK falling edge | — — | — — | 4.0 5.0 | — — | x ck i ck | ns |
| 95 | ESAI_RX_HF_CLK/ESAI_TX_HF_CLK clock cycle | — | $2 \times T_C$ | 15 | — | — | ns |
| 96 | ESAI_TX_HF_CLK input rising edge to ESAI_TX_CLK output | — | — | — | 18.0 | — | ns |
| 97 | ESAI_RX_HF_CLK input rising edge to ESAI_RX_CLK output | — | — | — | 18.0 | — | ns |

- ¹ i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode
(asynchronous implies that ESAI_TX_CLK and ESAI_RX_CLK are two different clocks)
i ck s = internal clock, synchronous mode
(synchronous implies that ESAI_TX_CLK and ESAI_RX_CLK are the same clock)

- ² bl = bit length
wl = word length
wr = word length relative

- ³ ESAI_TX_CLK(SCKT pin) = transmit clock
ESAI_RX_CLK(SCKR pin) = receive clock
ESAI_TX_FS(FST pin) = transmit frame sync
ESAI_RX_FS(FSR pin) = receive frame sync
ESAI_TX_HF_CLK(HCKT pin) = transmit high frequency clock
ESAI_RX_HF_CLK(HCKR pin) = receive high frequency clock

- ⁴ For the internal clock, the external clock cycle is defined by l_{cy}c and the ESAI control register.

- ⁵ The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but it spreads from one serial clock before the first bit clock (like the bit length frame sync signal), until the second-to-last bit clock of the first word in the frame.

- ⁶ Periodically sampled and not 100% tested.

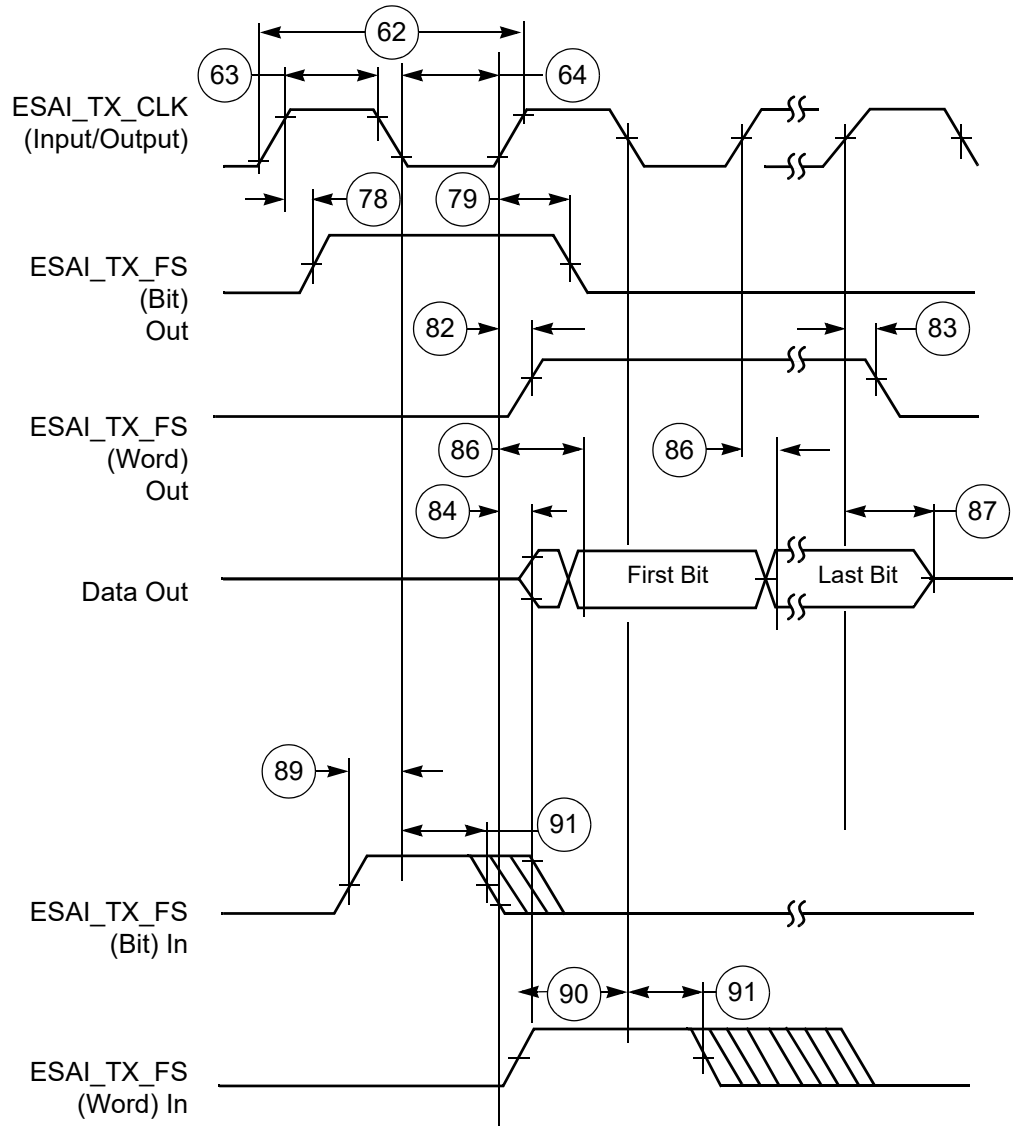


Figure 38. ESAI Transmitter Timing

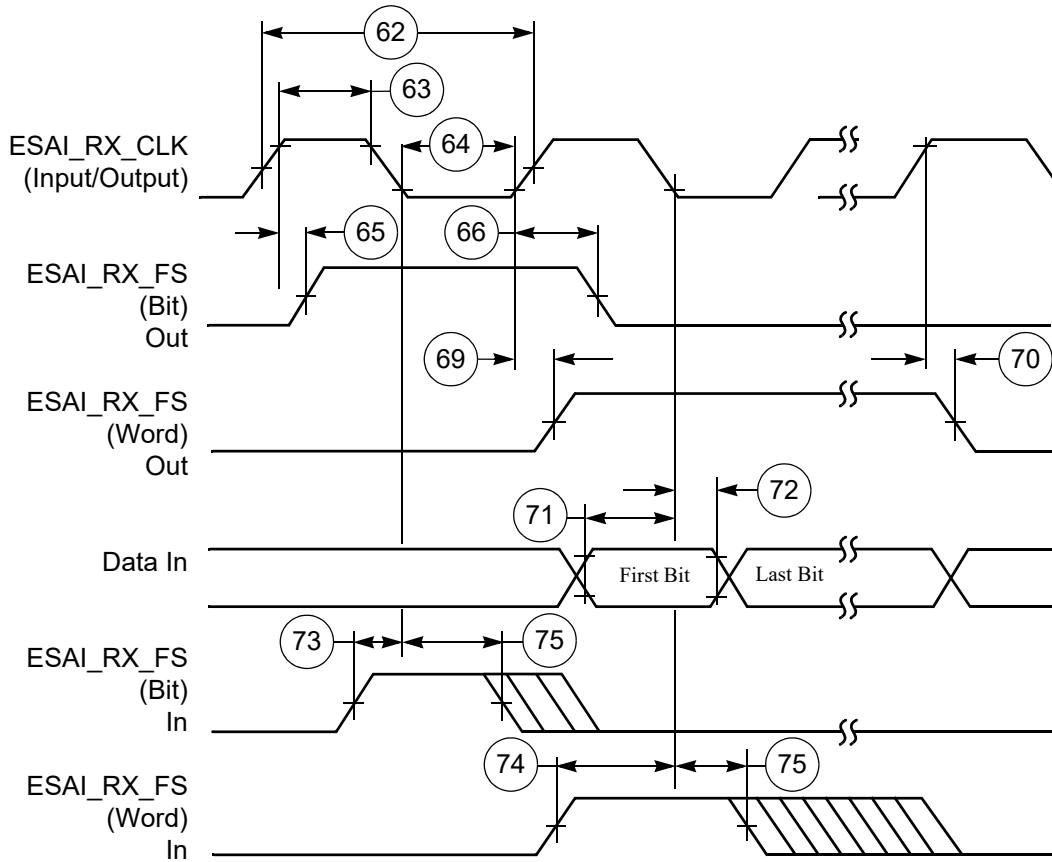


Figure 39. ESAI Receiver Timing

4.12.5 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC Timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing, eMMC4.4/4.41 (Dual Data Rate) timing and SDR104/50(SD3.0) timing.

4.12.5.1 SD/eMMC4.3 (Single Data Rate) AC Timing

Figure 40 depicts the timing of SD/eMMC4.3, and Table 55 lists the SD/eMMC4.3 timing characteristics.

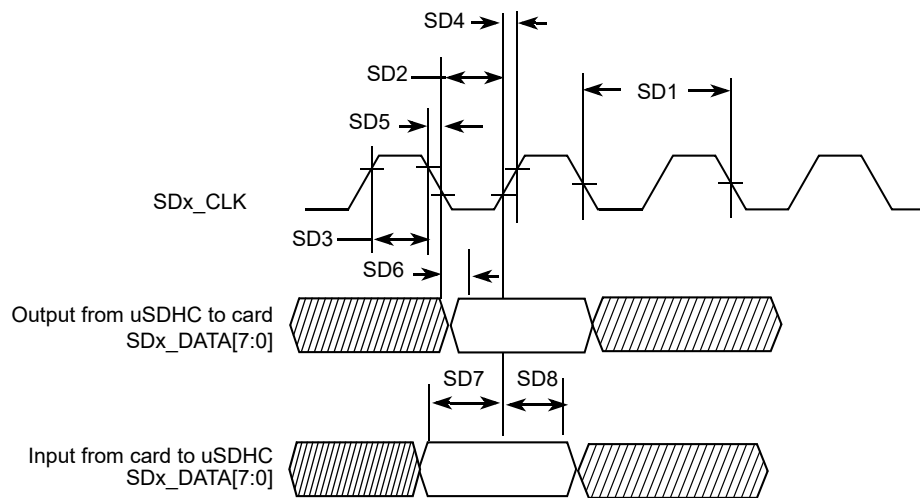


Figure 40. SD/eMMC4.3 Timing

Table 55. SD/eMMC4.3 Interface Timing Specification

| ID | Parameter | Symbols | Min | Max | Unit |
|--|---|------------|------|-------|------|
| Card Input Clock | | | | | |
| SD1 | Clock Frequency (Low Speed) | f_{PP}^1 | 0 | 400 | kHz |
| | Clock Frequency (SD/SDIO Full Speed/High Speed) | f_{PP}^2 | 0 | 25/50 | MHz |
| | Clock Frequency (MMC Full Speed/High Speed) | f_{PP}^3 | 0 | 20/52 | MHz |
| | Clock Frequency (Identification Mode) | f_{OD} | 100 | 400 | kHz |
| SD2 | Clock Low Time | t_{WL} | 7 | — | ns |
| SD3 | Clock High Time | t_{WH} | 7 | — | ns |
| SD4 | Clock Rise Time | t_{TLH} | — | 3 | ns |
| SD5 | Clock Fall Time | t_{THL} | — | 3 | ns |
| uSDHC Output/Card Inputs SD_CMD, SDx_DATAx (Reference to CLK) | | | | | |
| SD6 | uSDHC Output Delay | t_{OD} | -6.6 | 3.6 | ns |

Table 55. SD/eMMC4.3 Interface Timing Specification (continued)

| ID | Parameter | Symbols | Min | Max | Unit |
|--|------------------------------------|-----------|-----|-----|------|
| uSDHC Input/Card Outputs SD_CMD, SDx_DATAx (Reference to CLK) | | | | | |
| SD7 | uSDHC Input Setup Time | t_{ISU} | 2.5 | — | ns |
| SD8 | uSDHC Input Hold Time ⁴ | t_{IH} | 1.5 | — | ns |

- ¹ In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.
- ² In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.
- ³ In normal (full) speed mode for MMC card, clock frequency can be any value between 0–20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.
- ⁴ To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.12.5.2 eMMC4.4/4.41 (Dual Data Rate) AC Timing

Figure 41 depicts the timing of eMMC4.4/4.41. Table 56 lists the eMMC4.4/4.41 timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

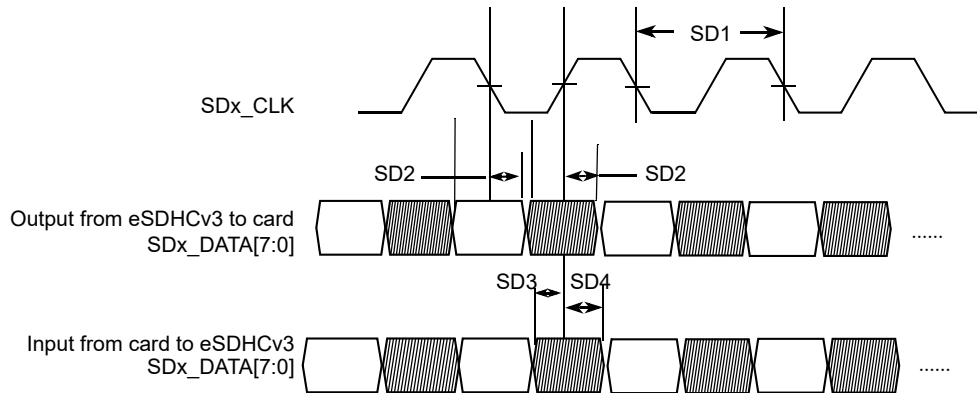


Figure 41. eMMC4.4/4.41 Timing

Table 56. eMMC4.4/4.41 Interface Timing Specification

| ID | Parameter | Symbols | Min | Max | Unit |
|--|------------------------------------|-----------|-----|-----|------|
| Card Input Clock | | | | | |
| SD1 | Clock Frequency (eMMC4.4/4.41 DDR) | f_{PP} | 0 | 52 | MHz |
| SD1 | Clock Frequency (SD3.0 DDR) | f_{PP} | 0 | 50 | MHz |
| uSDHC Output / Card Inputs SD_CMD, SDx_DATAx (Reference to CLK) | | | | | |
| SD2 | uSDHC Output Delay | t_{OD} | 2.8 | 6.8 | ns |
| uSDHC Input / Card Outputs SD_CMD, SDx_DATAx (Reference to CLK) | | | | | |
| SD3 | uSDHC Input Setup Time | t_{ISU} | 1.7 | — | ns |
| SD4 | uSDHC Input Hold Time | t_{IH} | 1.5 | — | ns |

4.12.5.3 SDR50/SDR104 AC Timing

Figure 42 depicts the timing of SDR50/SDR104, and Table 57 lists the SDR50/SDR104 timing characteristics.

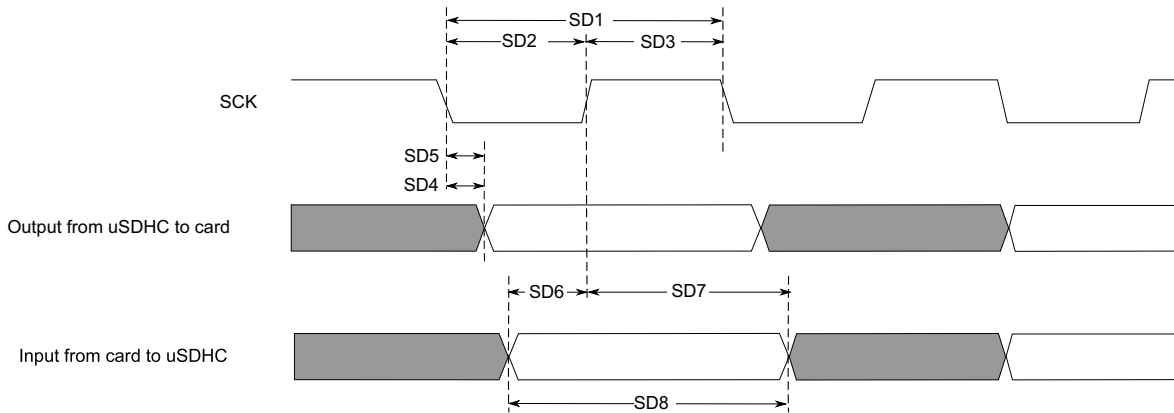


Figure 42. SDR50/SDR104 Timing

Table 57. SDR50/SDR104 Interface Timing Specification

| ID | Parameter | Symbols | Min | Max | Unit |
|--|-------------------------|-----------|-----------------------|-----------------------|------|
| Card Input Clock | | | | | |
| SD1 | Clock Frequency Period | t_{CLK} | 4.8 | — | ns |
| SD2 | Clock Low Time | t_{CL} | $0.46 \times t_{CLK}$ | $0.54 \times t_{CLK}$ | ns |
| SD3 | Clock High Time | t_{CH} | $0.46 \times t_{CLK}$ | $0.54 \times t_{CLK}$ | ns |
| uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK) | | | | | |
| SD4 | uSDHC Output Delay | t_{OD} | -3 | 1 | ns |
| uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK) | | | | | |
| SD5 | uSDHC Output Delay | t_{OD} | -1.6 | 0.74 | ns |
| uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK) | | | | | |
| SD6 | uSDHC Input Setup Time | t_{ISU} | 2.5 | — | ns |
| SD7 | uSDHC Input Hold Time | t_{IH} | 1.5 | — | ns |
| uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)¹ | | | | | |
| SD8 | Card Output Data Window | t_{ODW} | $0.5 \times t_{CLK}$ | — | ns |

¹ Data window in SDR100 mode is variable.

4.12.5.4 HS200 Mode Timing

Figure 43 depicts the timing of HS200 mode, and Table 58 lists the HS200 timing characteristics.

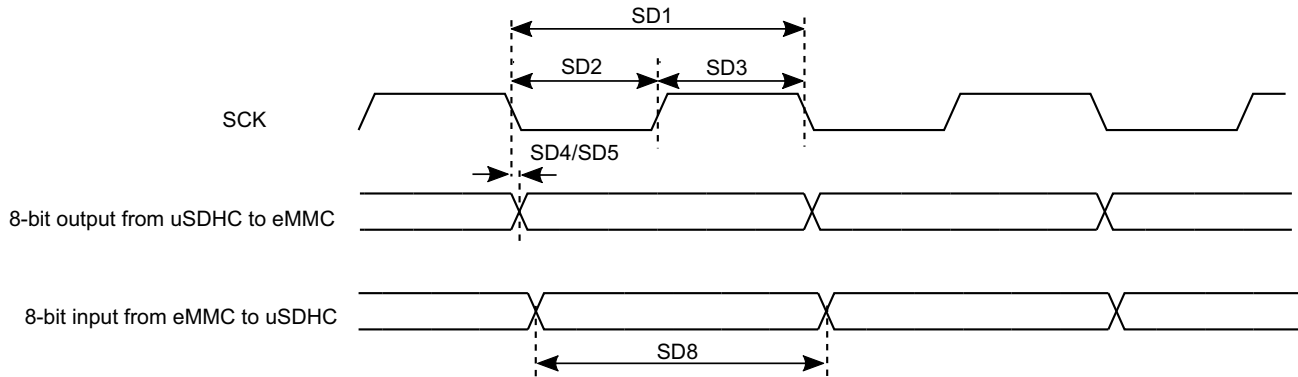


Figure 43. HS200 Mode Timing

Table 58. HS200 Interface Timing Specification

| ID | Parameter | Symbols | Min | Max | Unit |
|---|-------------------------|-----------|-----------------------|-----------------------|------|
| Card Input Clock | | | | | |
| SD1 | Clock Frequency Period | t_{CLK} | 5.0 | — | ns |
| SD2 | Clock Low Time | t_{CL} | $0.46 \times t_{CLK}$ | $0.54 \times t_{CLK}$ | ns |
| SD3 | Clock High Time | t_{CH} | $0.46 \times t_{CLK}$ | $0.54 \times t_{CLK}$ | ns |
| uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK) | | | | | |
| SD5 | uSDHC Output Delay | t_{OD} | -1.6 | 0.74 | ns |
| uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)¹ | | | | | |
| SD8 | Card Output Data Window | t_{ODW} | $0.5 \times t_{CLK}$ | — | ns |

¹HS200 is for 8 bits while SDR104 is for 4 bits.

4.12.5.5 Bus Operation Condition for 3.3 V and 1.8 V Signaling

Signaling level of SD/eMMC4.3 and eMMC4.4/4.41 modes is 3.3 V. Signaling level of SDR104/SDR50 mode is 1.8 V. The DC parameters for the NVCC_SD1, NVCC_SD2, and NVCC_SD4 supplies are identical to those shown in Table 25, “Single Voltage GPIO DC Parameters”. The DC parameters for the NVCC_LOW/NVCC_HIGH are identical to those shown in Table 26, “Dual Voltage GPIO I/O DC Parameters”.

4.12.6 Ethernet Controller (ENET) AC Electrical Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

4.12.6.1 ENET MII Mode Timing

This subsection describes MII receive, transmit, asynchronous inputs, and serial management signal timings.

4.12.6.1.1 MII Receive Signal Timing (ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER, and ENET_RX_CLK)

The receiver functions correctly up to an ENET_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement.

Figure 44 shows MII receive signal timings. Table 59 describes the timing parameters (M1–M4) shown in the figure.

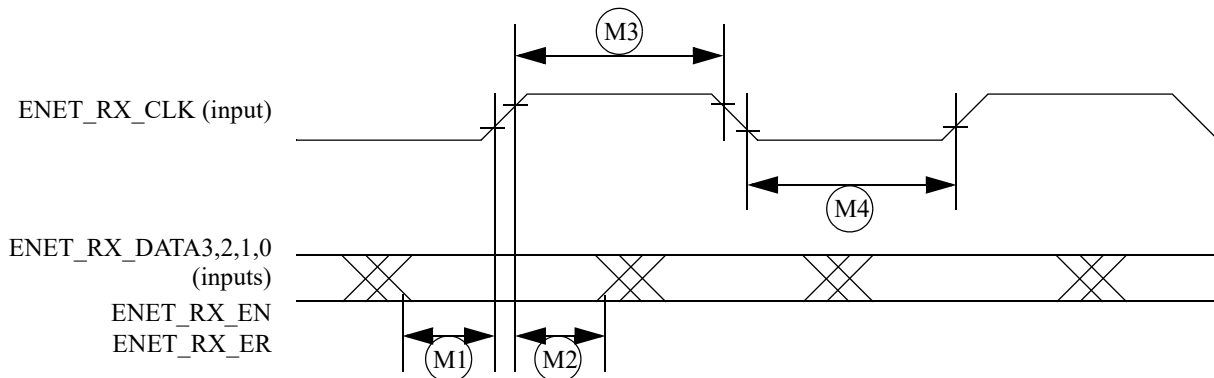


Figure 44. MII Receive Signal Timing Diagram

Table 59. MII Receive Signal Timing

| ID | Characteristic ¹ | Min | Max | Unit |
|----|--|-----|-----|--------------------|
| M1 | ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER to ENET_RX_CLK setup | 5 | — | ns |
| M2 | ENET_RX_CLK to ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER hold | 5 | — | ns |
| M3 | ENET_RX_CLK pulse width high | 35% | 65% | ENET_RX_CLK period |
| M4 | ENET_RX_CLK pulse width low | 35% | 65% | ENET_RX_CLK period |

¹ ENET_RX_EN, ENET_RX_CLK, and ENET0_RXD0 have the same timing in 10 Mbps 7-wire interface mode.

4.12.6.1.2 MII Transmit Signal Timing (ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER, and ENET_TX_CLK)

The transmitter functions correctly up to an ENET_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement.

Electrical Characteristics

Figure 45 shows MII transmit signal timings. Table 60 describes the timing parameters (M5–M8) shown in the figure.

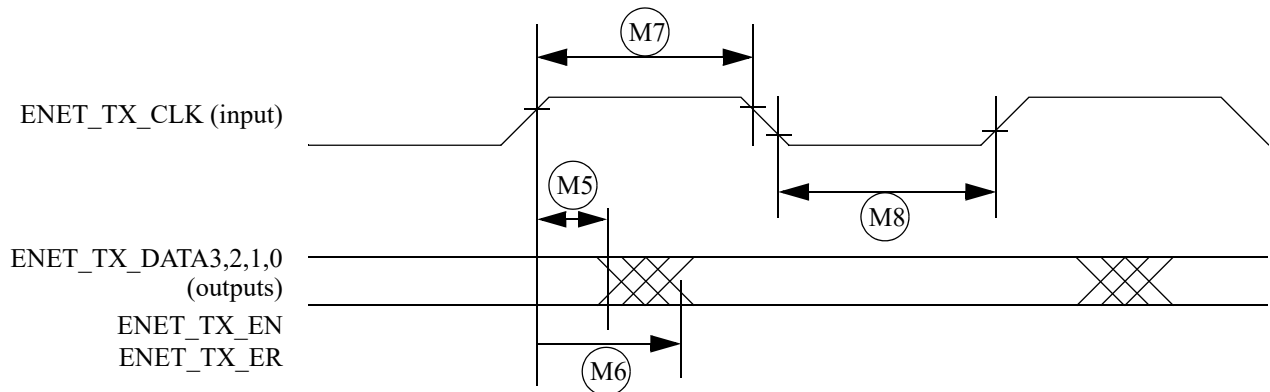


Figure 45. MII Transmit Signal Timing Diagram

Table 60. MII Transmit Signal Timing

| ID | Characteristic ¹ | Min | Max | Unit |
|----|--|-----|-----|--------------------|
| M5 | ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER invalid | 5 | — | ns |
| M6 | ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER valid | — | 20 | ns |
| M7 | ENET_TX_CLK pulse width high | 35% | 65% | ENET_TX_CLK period |
| M8 | ENET_TX_CLK pulse width low | 35% | 65% | ENET_TX_CLK period |

¹ ENET_TX_EN, ENET_TX_CLK, and ENET0_TXD0 have the same timing in 10-Mbps 7-wire interface mode.

4.12.6.1.3 MII Asynchronous Inputs Signal Timing (ENET_CRIS and ENET_COL)

Figure 46 shows MII asynchronous input timings. Table 61 describes the timing parameter (M9) shown in the figure.

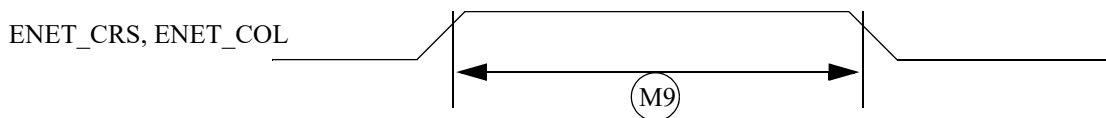


Figure 46. MII Async Inputs Timing Diagram

Table 61. MII Asynchronous Inputs Signal Timing

| ID | Characteristic | Min | Max | Unit |
|-----------------|---|-----|-----|--------------------|
| M9 ¹ | ENET_CRIS to ENET_COL minimum pulse width | 1.5 | — | ENET_TX_CLK period |

¹ ENET_COL has the same timing in 10-Mbit 7-wire interface mode.

4.12.6.1.4 MII Serial Management Channel Timing (ENET_MDIO and ENET_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification. However the ENET can function correctly with a maximum MDC frequency of 15 MHz.

Figure 47 shows MII asynchronous input timings. Table 62 describes the timing parameters (M10–M15) shown in the figure.

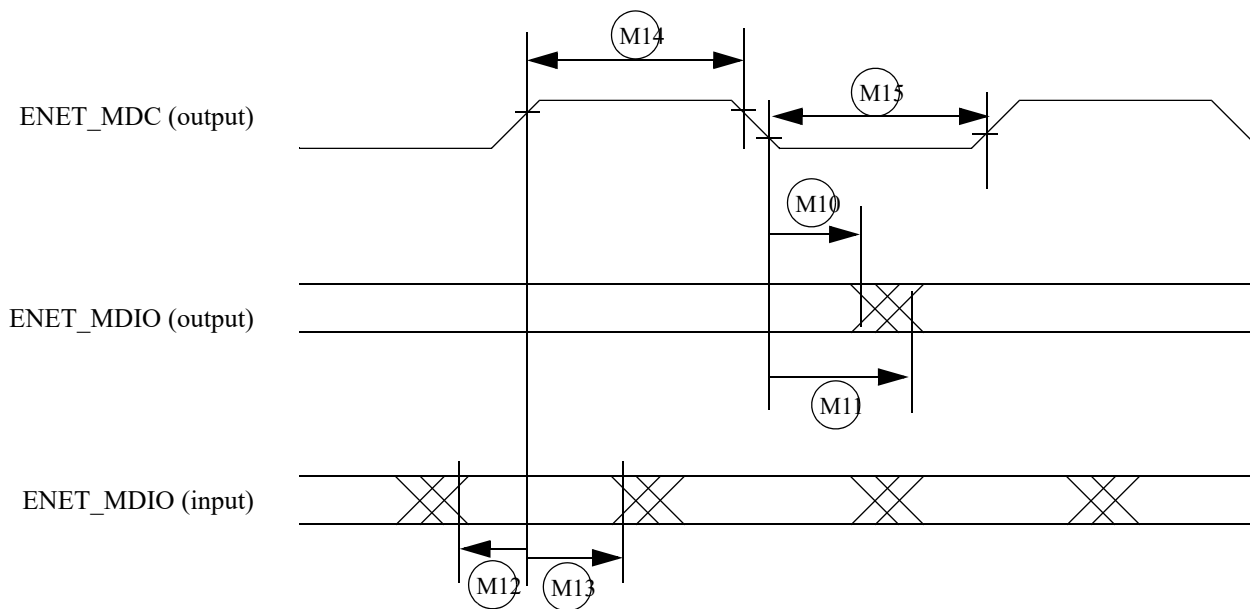


Figure 47. MII Serial Management Channel Timing Diagram

Table 62. MII Serial Management Channel Timing

| ID | Characteristic | Min | Max | Unit |
|-----|---|-----|-----|-----------------|
| M10 | ENET_MDC falling edge to ENET_MDIO output invalid (minimum propagation delay) | 0 | — | ns |
| M11 | ENET_MDC falling edge to ENET_MDIO output valid (maximum propagation delay) | — | 5 | ns |
| M12 | ENET_MDIO (input) to ENET_MDC rising edge setup | 18 | — | ns |
| M13 | ENET_MDIO (input) to ENET_MDC rising edge hold | 0 | — | ns |
| M14 | ENET_MDC pulse width high | 40% | 60% | ENET_MDC period |
| M15 | ENET_MDC pulse width low | 40% | 60% | ENET_MDC period |

4.12.6.2 RMII Mode Timing

In RMII mode, ENET_CLK is used as the REF_CLK, which is a 50 MHz \pm 50 ppm continuous reference clock. ENET_RX_EN is used as the ENET_RX_EN in RMII. Other signals under RMII mode include ENET_TX_EN, ENET_TX_DATA[1:0], ENET_RX_DATA[1:0] and ENET_RX_ER.

Figure 48 shows RMI mode timings. Table 63 describes the timing parameters (M16–M21) shown in the figure.

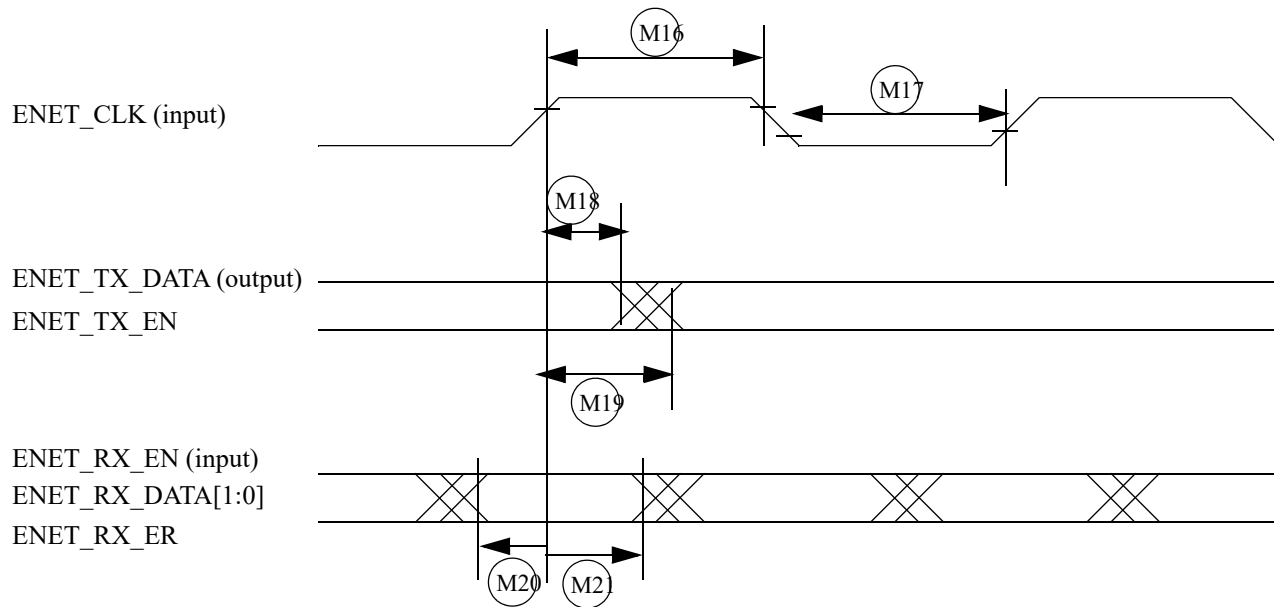


Figure 48. RMI Mode Signal Timing Diagram

Table 63. RMI Signal Timing

| ID | Characteristic | Min | Max | Unit |
|-----|--|-----|-----|-----------------|
| M16 | ENET_CLK pulse width high | 35% | 65% | ENET_CLK period |
| M17 | ENET_CLK pulse width low | 35% | 65% | ENET_CLK period |
| M18 | ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA invalid | 4 | — | ns |
| M19 | ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA valid | — | 13 | ns |
| M20 | ENET_RX_DATAD[1:0], ENET_RX_EN(ENET_RX_EN), ENET_RX_ER to ENET_CLK setup | 2 | — | ns |
| M21 | ENET_CLK to ENET_RX_DATAD[1:0], ENET_RX_EN, ENET_RX_ER hold | 2 | — | ns |

4.12.6.3 Signal Switching Specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

Table 64. RGMII Signal Switching Specifications ¹

| Symbol | Description | Min | Max | Unit |
|---------------|--|------|-----|------|
| T_{cyc}^2 | Clock cycle duration | 7.2 | 8.8 | ns |
| T_{skewT}^3 | Data to clock output skew at transmitter | -500 | 500 | ps |

Table 64. RGMII Signal Switching Specifications ¹ (continued)

| Symbol | Description | Min | Max | Unit |
|--------------------------|--------------------------------------|-----|------|------|
| T_{skewR} ⁴ | Data to clock input skew at receiver | 1 | 2.6 | ns |
| Duty_G ⁵ | Duty cycle for Gigabit | 45 | 55 | % |
| Duty_T ⁶ | Duty cycle for 10/100T | 40 | 60 | % |
| Tr/Tf | Rise/fall time (20–80%) | — | 0.75 | ns |

¹ For all signals, the maximum load is as follows:

CL = 5 pF at 1.8 V

CL = 10 pF at 2.5 V

See Figure 4 for the test circuit.

² For 10 Mbps and 100 Mbps, T_{cyc} will scale to 400 ns \pm 40 ns and 40 ns \pm 4 ns respectively.

³ For all versions of RGMII prior to 2.0; This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. For 10/100, the Max value is unspecified.

⁴ For all versions of RGMII prior to 2.0; This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. For 10/100, the Max value is unspecified.

⁵ Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three T_{cyc} of the lowest speed transitioned between.

⁶ Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three T_{cyc} of the lowest speed transitioned between.

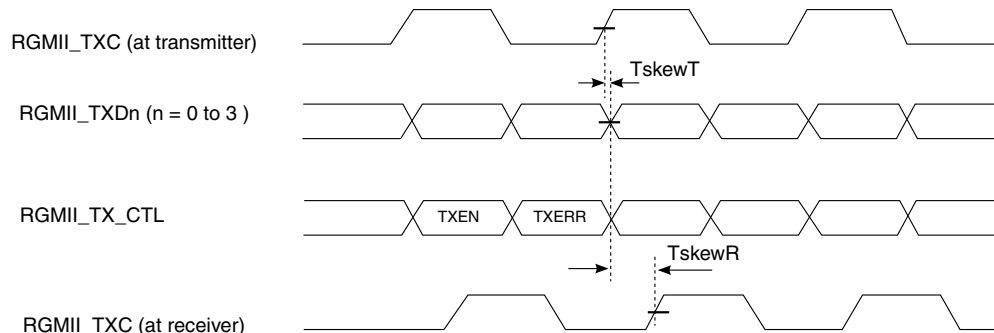


Figure 49. RGMII Transmit Signal Timing Diagram Original

Electrical Characteristics

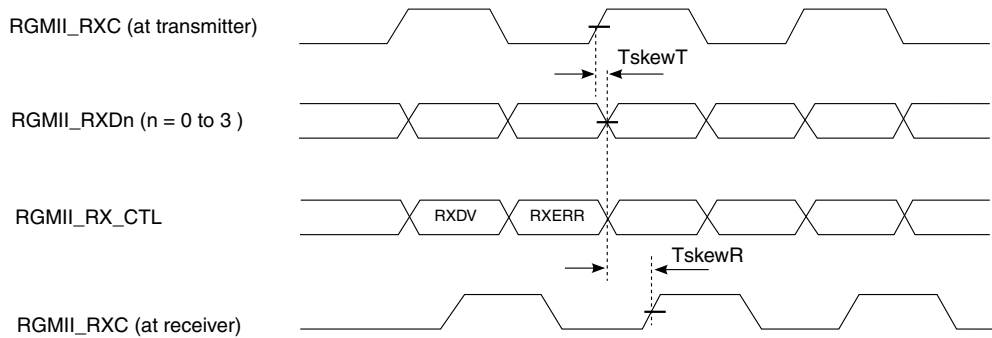


Figure 50. RGMII Receive Signal Timing Diagram Original

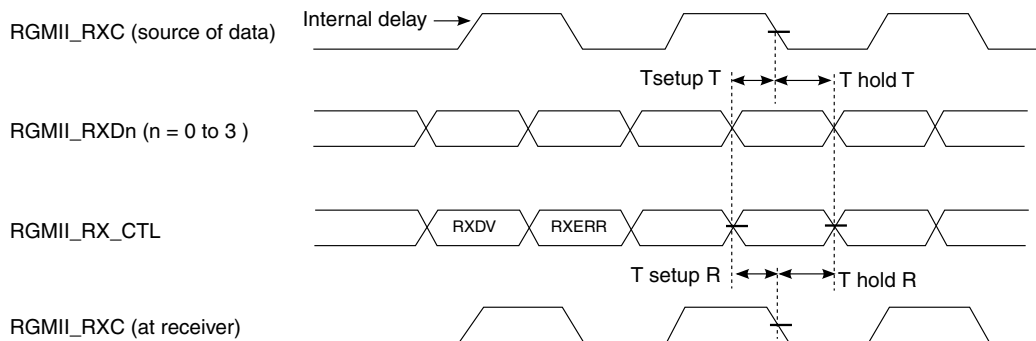


Figure 51. RGMII Receive Signal Timing Diagram with Internal Delay

4.12.7 Flexible Controller Area Network (FLEXCAN) AC Electrical Specifications

The Flexible Controller Area Network (FlexCAN) module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification. The processor has two CAN modules available for systems design. Tx and Rx ports for both modules are multiplexed with other I/O pins. See the IOMUXC chapter of the *i.MX 6SoloX Applications Processor Reference Manual (IMX6SXR)* to see which pins expose Tx and Rx pins; these ports are named CAN_TX and CAN_RX, respectively.

4.12.8 I²C Module Timing Parameters

This section describes the timing parameters of the I²C module. Figure 52 depicts the timing of I²C module, and Table 65 lists the I²C module timing characteristics.

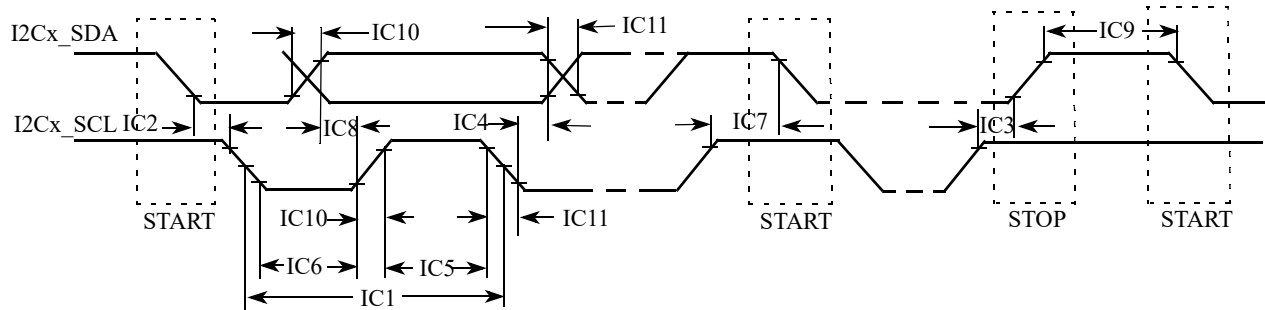


Figure 52. I²C Bus Timing

Table 65. I²C Module Timing Parameters

| ID | Parameter | Standard Mode | | Fast Mode | | Unit |
|------|---|----------------|-------------------|-------------------------------------|------------------|------|
| | | Min | Max | Min | Max | |
| IC1 | I2Cx_SCL cycle time | 10 | — | 2.5 | — | μs |
| IC2 | Hold time (repeated) START condition | 4.0 | — | 0.6 | — | μs |
| IC3 | Set-up time for STOP condition | 4.0 | — | 0.6 | — | μs |
| IC4 | Data hold time | 0 ¹ | 3.45 ² | 0 ¹ | 0.9 ² | μs |
| IC5 | HIGH Period of I2Cx_SCL Clock | 4.0 | — | 0.6 | — | μs |
| IC6 | LOW Period of the I2Cx_SCL Clock | 4.7 | — | 1.3 | — | μs |
| IC7 | Set-up time for a repeated START condition | 4.7 | — | 0.6 | — | μs |
| IC8 | Data set-up time | 250 | — | 100 ³ | — | ns |
| IC9 | Bus free time between a STOP and START condition | 4.7 | — | 1.3 | — | μs |
| IC10 | Rise time of both I2Cx_SDA and I2Cx_SCL signals | — | 1000 | 20 + 0.1C _b ⁴ | 300 | ns |
| IC11 | Fall time of both I2Cx_SDA and I2Cx_SCL signals | — | 300 | 20 + 0.1C _b ⁴ | 300 | ns |
| IC12 | Capacitive load for each bus line (C _b) | — | 400 | — | 400 | pF |

¹ A device must internally provide a hold time of at least 300 ns for I2Cx_SDA signal to bridge the undefined region of the falling edge of I2Cx_SCL.

² The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2Cx_SCL signal.

³ A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2Cx_SCL signal. If such a device does stretch the LOW period of the I2Cx_SCL signal, it must output the next data bit to the I2Cx_SDA line $\text{max_rise_time (IC9)} + \text{data_setup_time (IC7)} = 1000 + 250 = 1250$ ns (according to the Standard-mode I²C-bus specification) before the I2Cx_SCL line is released.

⁴ C_b = total capacitance of one bus line in pF.

4.12.9 LCD Controller (LCDIF) Timing Parameters

Figure 53 shows the LCDIF timing and Table 66 lists the timing parameters.

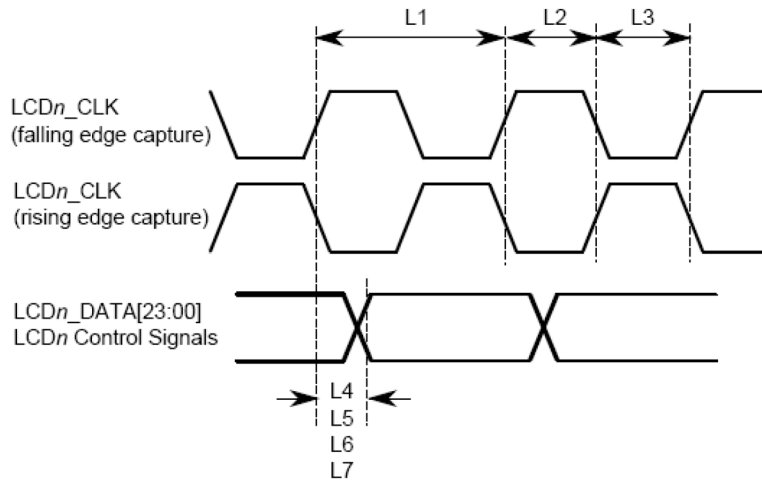


Figure 53. LCD Timing

Table 66. LCD Timing Parameters

| ID | Parameter | Symbol | Min | Max | Unit |
|----|--|----------------|-----|-----|------|
| L1 | LCD pixel clock frequency | tCLK(LCD) | - | 150 | MHz |
| L2 | LCD pixel clock high (falling edge capture) | tCLKH(LCD) | 3 | - | ns |
| L3 | LCD pixel clock low (rising edge capture) | tCLKL(LCD) | 3 | - | ns |
| L4 | LCD pixel clock high to data valid (falling edge capture) | td(CLKH-DV) | -1 | 1 | ns |
| L5 | LCD pixel clock low to data valid (rising edge capture) | td(CLKL-DV) | -1 | 1 | ns |
| L6 | LCD pixel clock high to control signals valid (falling edge capture) | td(CLKH-CTRLV) | -1 | 1 | ns |
| L7 | LCD pixel clock low to control signals valid (rising edge capture) | td(CLKL-CTRLV) | -1 | 1 | ns |

4.12.9.1 LCDIF Display Interface Signal Mapping

Table 67. LCDIF Display Interface Signal Mapping

| Pin Name | 8-bit DOTCLK LCD IF | 16-bit DOTCLK LCD IF | 18-bit DOTCLK LCD IF | 24-bit DOTCLK LCD IF | 8-bit DVI LCD IF |
|--------------------------|---------------------|----------------------|----------------------|----------------------|------------------|
| LCD_RS | — | — | — | — | CCIR_CLK |
| LCD_CS | — | — | — | — | — |
| LCD_WR_RWn | — | — | — | — | — |
| LCD_RD_E | — | — | — | — | — |
| LCD_VSYNC* (two options) | LCD_VSYNC | LCD_VSYNC | LCD_VSYNC | LCD_VSYNC | — |
| LCD_HSYNC | LCD_HSYNC | LCD_HSYNC | LCD_HSYNC | LCD_HSYNC | — |

Table 67. LCDIF Display Interface Signal Mapping (continued)

| Pin Name | 8-bit DOTCLK LCD IF | 16-bit DOTCLK LCD IF | 18-bit DOTCLK LCD IF | 24-bit DOTCLK LCD IF | 8-bit DVI LCD IF |
|---------------------------|--|--|--|--|---------------------|
| LCD_DOTCLK | LCD_DOTCLK | LCD_DOTCLK | LCD_DOTCLK | LCD_DOTCLK | — |
| LCD_ENABLE | LCD_ENABLE | LCD_ENABLE | LCD_ENABLE | LCD_ENABLE | — |
| LCD_D23 | — | — | — | R[7] | — |
| LCD_D22 | — | — | — | R[6] | — |
| LCD_D21 | — | — | — | R[5] | — |
| LCD_D20 | — | — | — | R[4] | — |
| LCD_D19 | — | — | — | R[3] | — |
| LCD_D18 | — | — | — | R[2] | — |
| LCD_D17 | — | — | R[5] | R[1] | — |
| LCD_D16 | — | — | R[4] | R[0] | — |
| LCD_D15 / VSYNC* | — | R[4] | R[3] | G[7] | — |
| LCD_D14 / HSYNC** | — | R[3] | R[2] | G[6] | — |
| LCD_D13 / LCD_DOTCLK** | — | R[2] | R[1] | G[5] | — |
| LCD_D12 / ENABLE** | — | R[1] | R[0] | G[4] | — |
| LCD_D11 | — | R[0] | G[5] | G[3] | — |
| LCD_D10 | — | G[5] | G[4] | G[2] | — |
| LCD_D9 | — | G[4] | G[3] | G[1] | — |
| LCD_D8 | — | G[3] | G[2] | G[0] | — |
| LCD_D7 | R[2] | G[2] | G[1] | B[7] | Y/C[7] |
| LCD_D6 | R[1] | G[1] | G[0] | B[6] | Y/C[6] |
| LCD_D5 | R[0] | G[0] | B[5] | B[5] | Y/C[5] |
| LCD_D4 | G[2] | B[4] | B[4] | B[4] | Y/C[4] |
| LCD_D3 | G[1] | B[3] | B[3] | B[3] | Y/C[3] |
| LCD_D2 | G[0] | B[2] | B[2] | B[2] | Y/C[2] |
| LCD_D1 | B[1] | B[1] | B[1] | B[1] | Y/C[1] |
| LCD_D0 | B[0] | B[0] | B[0] | B[0] | Y/C[0] |
| LCD_RESET | LCD_RESET | LCD_RESET | LCD_RESET | LCD_RESET | — |
| LCD_BUSY / LCD_VSYNC | LCD_BUSY (OR optional LCD_VSYNC) | LCD_BUSY (OR optional LCD_VSYNC) | LCD_BUSY (OR optional LCD_VSYNC) | LCD_BUSY (OR optional LCD_VSYNC) | — |

4.12.10 LVDS Display Bridge (LDB) Module Parameters

The LVDS interface complies with TIA/EIA 644-A standard. For more details, see TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits”.

Table 68. LVDS Display Bridge (LDB) Electrical Specification

| Parameter | Symbol | Test Condition | Min | Max | Units |
|-------------------------------------|--------------|--|------|-------|-------|
| Differential Voltage Output Voltage | V_{OD} | 100 Ω Differential load | 250 | 450 | mV |
| Output Voltage High | V_{OH} | 100 Ω differential load (0 V Diff—Output High Voltage static) | 1.25 | 1.6 | V |
| Output Voltage Low | V_{OL} | 100 Ω differential load (0 V Diff—Output Low Voltage static) | 0.9 | 1.25 | V |
| Offset Static Voltage | V_{OS} | Two 49.9 Ω resistors in series between N-P terminal, with output in either Zero or One state, the voltage measured between the 2 resistors. | 1.15 | 1.375 | V |
| VOS Differential | V_{OSDIFF} | Difference in V_{OS} between a One and a Zero state | -50 | 50 | mV |
| Output short circuited to GND | ISA ISB | With the output common shorted to GND | -24 | 24 | mA |
| VT Full Load Test | VTLoad | 100 Ω Differential load with a 3.74 k Ω load between GND and IO Supply Voltage | 247 | 454 | mV |

4.12.11 MediaLB (MLB) Characteristics

4.12.11.1 MediaLB (MLB) DC Characteristics

Table 69 lists the MediaLB 3-pin interface electrical characteristics.

Table 69. MediaLB 3-Pin Interface Electrical DC Specifications

| Parameter | Symbol | Test Conditions | Min | Max | Unit |
|-----------------------------|----------|-----------------------|-----|----------|---------|
| Maximum input voltage | — | — | — | 3.6 | V |
| Low level input threshold | V_{IL} | — | — | 0.7 | V |
| High level input threshold | V_{IH} | See Note ¹ | 1.8 | — | V |
| Low level output threshold | V_{OL} | $I_{OL} = 6$ mA | — | 0.4 | V |
| High level output threshold | V_{OH} | $I_{OH} = -6$ mA | 2.0 | — | V |
| Input leakage current | I_L | $0 < V_{in} < V_{DD}$ | — | ± 10 | μ A |

¹ Higher V_{IH} thresholds can be used; however, the risks associated with less noise margin in the system must be evaluated and assumed by the customer.

4.12.11.2 MediaLB (MLB) Controller AC Timing Electrical Specifications

This section describes the timing electrical information of the MediaLB module. Figure 54 show the timing of MediaLB 3-pin interface, and Table 70 and Table 71 lists the MediaLB 3-pin interface timing characteristics.

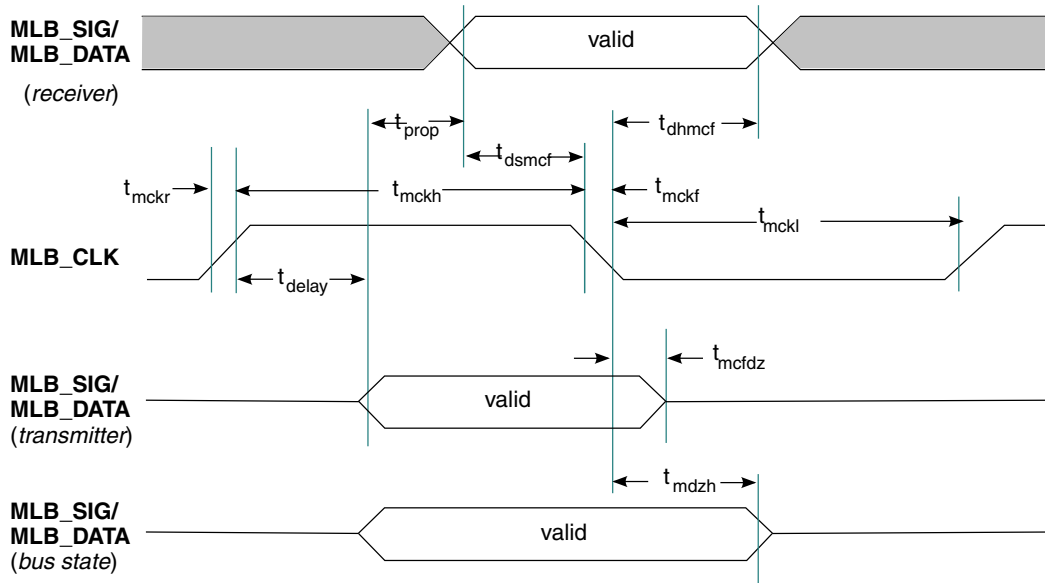


Figure 54. MediaLB 3-Pin Timing

Ground = 0.0 V; Load Capacitance = 60 pF; MediaLB speed = 256/512 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

Table 70. MLB 256/512 Fs Timing Parameters

| Parameter | Symbol | Min | Max | Unit | Comment |
|--|-------------|------------|------------|------|--|
| MLB_CLK operating frequency ¹ | f_{mck} | 11.264 | 25.6 | MHz | 256xFs at 44.0 kHz 512xFs at 50.0 kHz |
| MLB_CLK rise time | t_{mckr} | — | 3 | ns | V_{IL} TO V_{IH} |
| MLB_CLK fall time | t_{mckf} | — | 3 | ns | V_{IH} TO V_{IL} |
| MLB_CLK low time ² | t_{mckl} | 30 14 | — | ns | 256xFs 512xFs |
| MLB_CLK high time | t_{mckh} | 30 14 | — | ns | 256xFs 512xFs |
| MLB_SIG/MLB_DATA receiver input valid to MLB_CLK falling | t_{dsmcf} | 1 | — | ns | — |
| MLB_SIG/MLB_DATA receiver input hold from MLB_CLK low | t_{dhmcf} | t_{mdzh} | — | ns | — |
| MLB_SIG/MLB_DATA output high impedance from MLB_CLK low | t_{mcfdz} | 0 | t_{mckl} | ns | — ³ |

Electrical Characteristics

Table 70. MLB 256/512 Fs Timing Parameters (continued)

| Parameter | Symbol | Min | Max | Unit | Comment |
|--|-------------|-----|-----|------|---------|
| Bus Hold from MLB_CLK low | t_{mdzh} | 4 | — | ns | — |
| MLB_SIG/MLB_DATA output valid from transition of MLB_CLK (low to high) | t_{delay} | | 10 | ns | — |

¹ The controller can shut off MLB_CLK to place MediaLB in a low-power state. Depending on the time the clock is shut off, a runt pulse can occur on MLB_CLK.

² MLB_CLK low/high time includes the pulse width variation.

³ The MediaLB driver can release the MLB_DATA/MLB_SIG line as soon as MLB_CLK is low; however, the logic state of the final driven bit on the line must remain on the bus for t_{mdzh} . Therefore, coupling must be minimized while meeting the maximum load capacitance listed.

Ground = 0.0 V; load capacitance = 40 pF; MediaLB speed = 1024 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed in [Table 71](#); unless otherwise noted.

Table 71. MLB 1024 Fs Timing Parameters

| Parameter | Symbol | Min | Max | Unit | Comment |
|--|-------------|------------|------------|------|--|
| MLB_CLK Operating Frequency ¹ | f_{mck} | 45.056 | 51.2 | MHz | 1024xfs at 44.0 kHz 1024xfs at 50.0 kHz |
| MLB_CLK rise time | t_{mckr} | — | 1 | ns | V_{IL} TO V_{IH} |
| MLB_CLK fall time | t_{mckf} | — | 1 | ns | V_{IH} TO V_{IL} |
| MLB_CLK low time | t_{mckl} | 6.1 | — | ns | ² |
| MLB_CLK high time | t_{mckh} | 9.3 | — | ns | — |
| MLB_SIG/MLB_DATA receiver input valid to MLB_CLK falling | t_{dsmcf} | 1 | — | ns | — |
| MLB_SIG/MLB_DATA receiver input hold from MLB_CLK low | t_{dhmcf} | t_{mdzh} | — | ns | — |
| MLB_SIG/MLB_DATA output high impedance from MLB_CLK low | t_{mcfdz} | 0 | t_{mckl} | ns | ³ |
| Bus Hold from MLB_CLK low | t_{mdzh} | 2 | — | ns | — |
| MLB_SIG/MLB_DATA output valid from transition of MLB_CLK (low to high) | t_{delay} | — | 7 | ns | — |

¹ The controller can shut off MLB_CLK to place MediaLB in a low-power state. Depending on the time the clock is shut off, a runt pulse can occur on MLB_CLK.

² MLB_CLK low/high time includes the pulse width variation.

³ The MediaLB driver can release the MLB_DATA/MLB_SIG line as soon as MLB_CLK is low; however, the logic state of the final driven bit on the line must remain on the bus for t_{mdzh} . Therefore, coupling must be minimized while meeting the maximum load capacitance listed.

4.12.12 PCIe PHY Parameters

The PCIe interface complies with PCIe specification Gen2 x1 lane and supports the PCI Express 1.1/2.0 standard.

4.12.12.1 PCIE_REXT Reference Resistor Connection

The impedance calibration process requires connection of reference resistor 200 Ω . 1% precision resistor on PCIE_REXT pads to ground. It is used for termination impedance calibration.

4.12.13 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMx_OUT) external pin.

Figure 55 depicts the timing of the PWM, and Table 72 lists the PWM timing parameters.

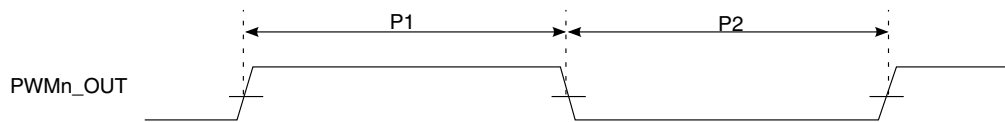


Figure 55. PWM Timing

Table 72. PWM Output Timing Parameters

| ID | Parameter | Min | Max | Unit |
|----|-----------------------------|-----|---------|------|
| — | PWM Module Clock Frequency | 0 | ipg_clk | MHz |
| P1 | PWM output pulse width high | 15 | — | ns |
| P2 | PWM output pulse width low | 15 | — | ns |

4.12.14 QUAD SPI (QSPI) Timing Parameters

Measurement conditions are with 35 pF load on SCK and SIO pins and input slew rate of 1 V/ns.

4.12.14.1 SDR Mode

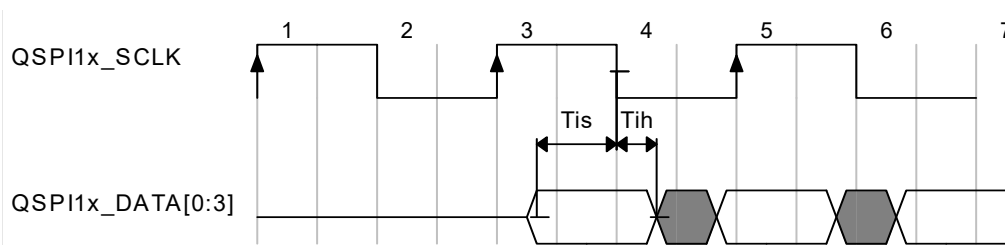


Figure 56. QuadSPI Input/Read Timing (SDR mode with internal sampling)

Table 73. QuadSPI Input/Read Timing (SDR mode with internal sampling)

| Symbol | Parameter | Value | | Unit |
|----------|---|-------|-----|------|
| | | Min | Max | |
| T_{is} | Setup time for incoming data | 8.67 | — | ns |
| T_{ih} | Hold time requirement for incoming data | 0 | — | ns |

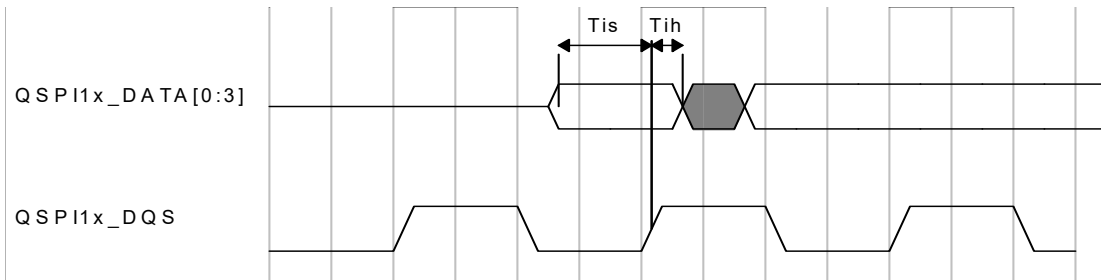


Figure 57. QuadSPI Input/Read Timing (SDR mode with loopback DQS sampling)

Table 74. QuadSPI Input/Read Timing (SDR mode with loopback DQS sampling)

| Symbol | Parameter | Value | | Unit |
|----------|---|-------|-----|------|
| | | Min | Max | |
| T_{is} | Setup time for incoming data | 1 | — | ns |
| T_{ih} | Hold time requirement for incoming data | 1 | — | ns |

NOTE

- For internal sampling, the timing values assumes using sample point 0, that is QuadSPIx_SMPR[SDRSMP] = 0.
- For loopback DQS sampling, the data strobe is output to the DQS pad together with the serial clock. The data strobe is looped back from DQS pad and used to sample input data.

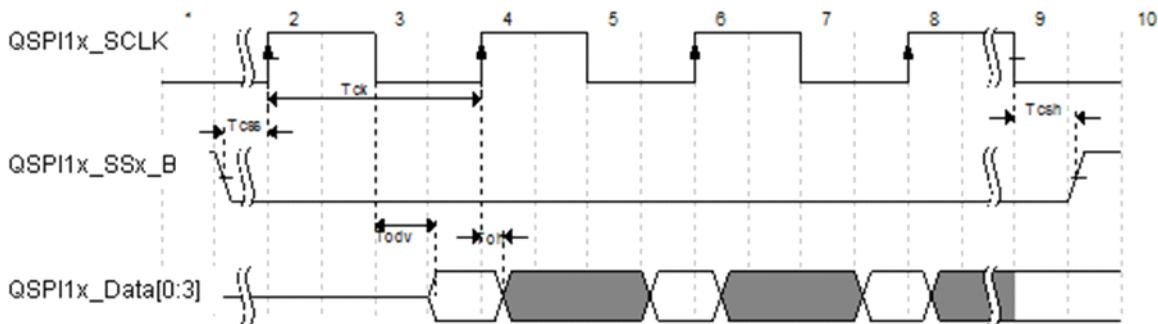


Figure 58. QuadSPI Output/Write Timing (SDR mode)

Table 75. QuadSPI Output/Write Timing (SDR mode)

| Symbol | Parameter | Value | | Unit |
|-----------|-------------------------------|-------|-----|--------------|
| | | Min | Max | |
| T_{ov} | Output Data Valid | — | 3.2 | ns |
| T_{oh} | Output Data Hold | 0 | — | ns |
| T_{ck} | SCK clock period | 12.5 | — | ns |
| T_{css} | Chip select output setup time | 3 | — | SCK cycle(s) |
| T_{csh} | Chip select output hold time | 3 | — | SCK cycle(s) |

NOTE

T_{css} and T_{csh} are configured by the QuadSPIx_FLSHCR register, the default values of 3 are shown on the timing. Please refer to Reference Manual for further details.

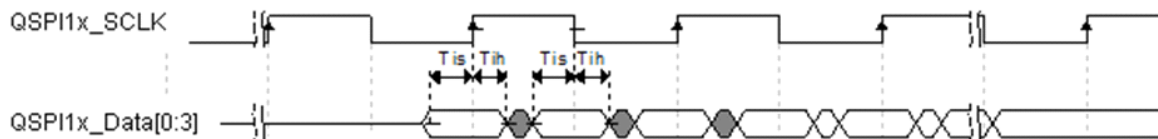
4.12.14.2 DDR Mode

Figure 59. QuadSPI Input/Read Timing (DDR mode with internal sampling)

Table 76. QuadSPI Input/Read Timing (DDR mode with internal sampling)

| Symbol | Parameter | Value | | Unit |
|----------|---|-------|-----|------|
| | | Min | Max | |
| T_{is} | Setup time for incoming data | 8.67 | — | ns |
| T_{ih} | Hold time requirement for incoming data | 0 | — | ns |

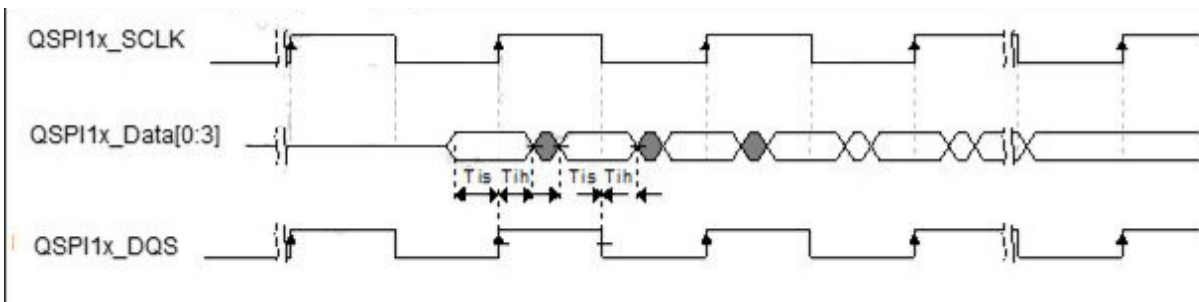


Figure 60. QuadSPI Input/Read Timing (DDR mode with loopback DQS sampling)

Table 77. QuadSPI Input/Read Timing (DDR mode with loopback DQS sampling)

| Symbol | Parameter | Value | | Unit |
|----------|---|-------|-----|------|
| | | Min | Max | |
| T_{is} | Setup time for incoming data | 1 | — | ns |
| T_{ih} | Hold time requirement for incoming data | 1 | — | ns |

NOTE

- For internal sampling, the timing values assumes sample point 0, that is QuadSPIx_SMPR[DDRSMP] = 0.
- For loopback DQS sampling, the data strobe is output to the DQS pad together with the serial clock. The data strobe is looped back from the DQS pad and used to sample input data.

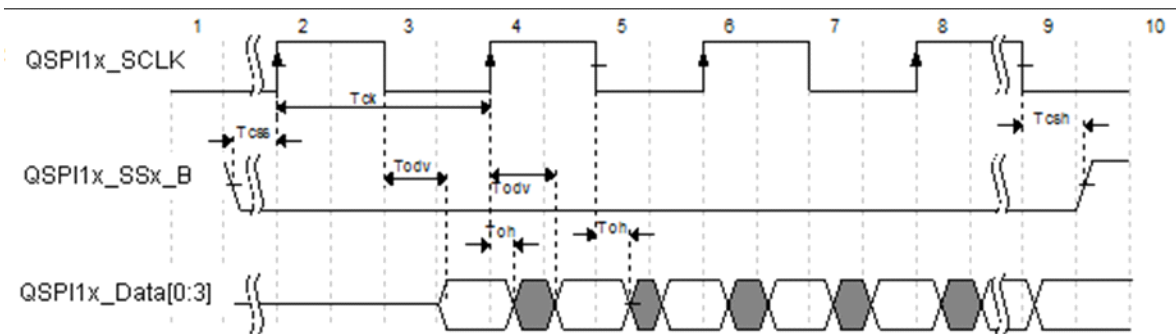


Figure 61. QuadSPI Output/Write Timing (DDR mode)

Table 78. QuadSPI Output/Write Timing (DDR mode)

| Symbol | Parameter | Value | | Unit |
|-----------|-------------------------------|-------|-----|--------------|
| | | Min | Max | |
| T_{ov} | Output Data Valid | — | 2 | ns |
| T_{oh} | Output Data Hold | 1 | — | ns |
| T_{ck} | SCK clock period | 22 | — | ns |
| T_{css} | Chip select output setup time | 3 | — | SCK cycle(s) |
| T_{csh} | Chip select output hold time | 3 | — | SCK cycle(s) |

NOTE

T_{css} and T_{csh} are configured by the QuadSPIx_FLSHCR register, the default register values of 3 are shown on the timing. Please refer to Reference Manual for further details.

4.12.15 SAI/I2S Switching Specifications

This sections provides the AC timings for the SAI in master (clocks driven) and slave (clocks input) modes. All timings are given for non-inverted serial clock polarity (SAI_TCR[TSCKP] = 0, SAI_RCR[RSCKP] = 0) and non-inverted frame sync (SAI_TCR[TFSI] = 0, SAI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SAI_BCLK) and/or the frame sync (SAI_FS) shown in the figures below.

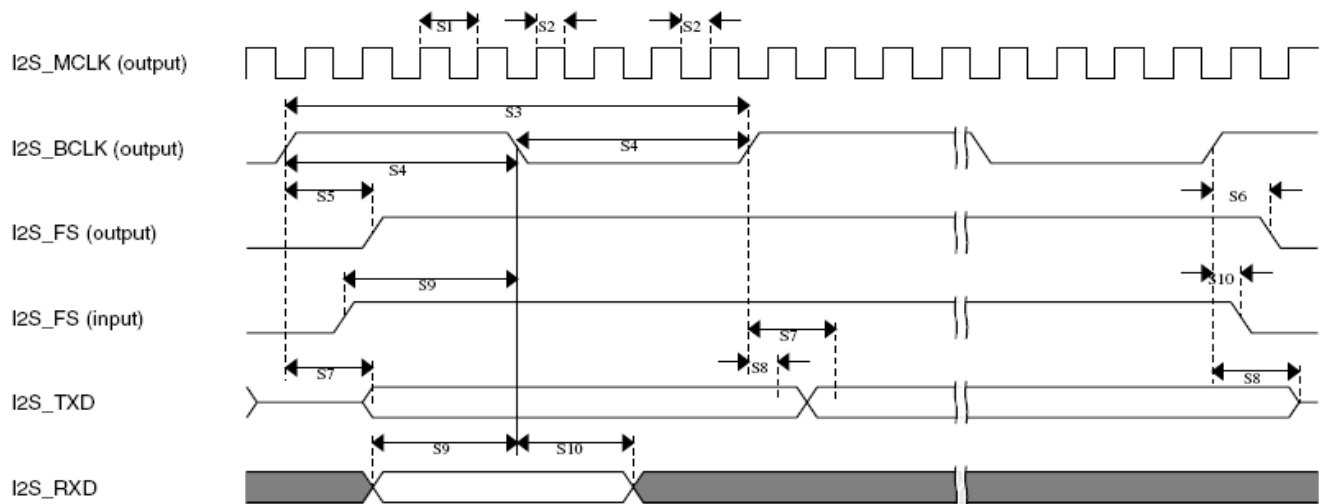


Figure 62. SAI Timing—Master Modes

Table 79. Master Mode SAI Timing

| Num | Characteristic | Min | Max | Unit |
|-----|--|--------|-----|-------------|
| S1 | SAI_MCLK cycle time | 20 | — | ns |
| S2 | SAI_MCLK pulse width high/low | 40% | 60% | MCLK period |
| S3 | SAI_BCLK cycle time | 2 x S1 | — | ns |
| S4 | SAI_BCLK pulse width high/low | 40% | 60% | BCLK period |
| S5 | SAI_BCLK to SAI_FS output valid | — | 15 | ns |
| S6 | SAI_BCLK to SAI_FS output invalid | 0 | — | ns |
| S7 | SAI_BCLK to SAI_TXD valid | — | 15 | ns |
| S8 | SAI_BCLK to SAI_TXD invalid | 0 | — | ns |
| S9 | SAI_RXD/SAI_FS input setup before SAI_BCLK | 15 | — | ns |
| S10 | SAI_RXD/SAI_FS input hold after SAI_BCLK | 0 | — | ns |

Electrical Characteristics

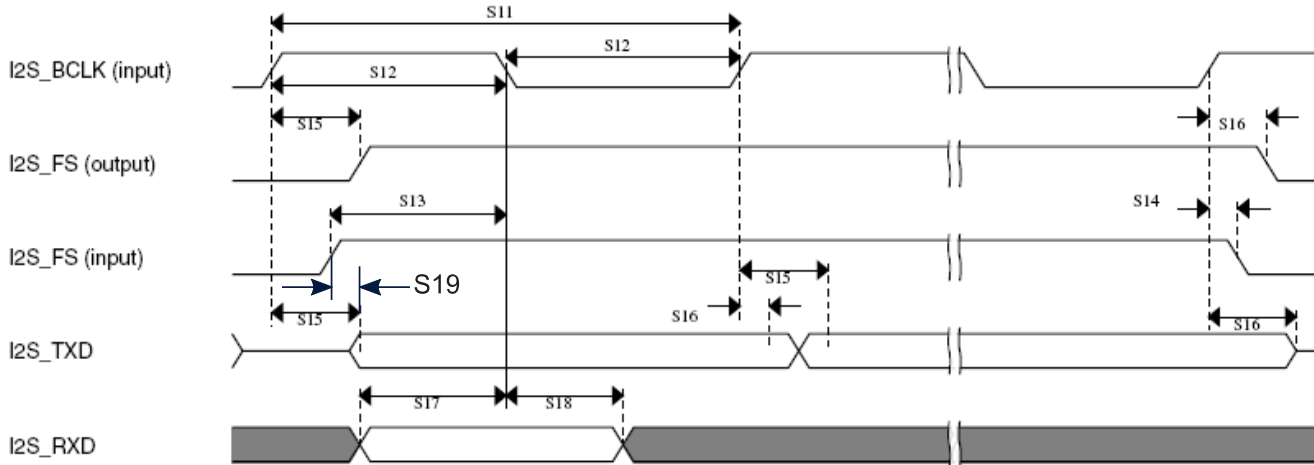


Figure 63. SAI Timing—Slave Modes

Table 80. Slave Mode SAI Timing

| Num | Characteristic | Min | Max | Unit |
|-----|--|-----|-----|-------------|
| S11 | SAI_BCLK cycle time (input) | 20 | — | ns |
| S12 | SAI_BCLK pulse width high/low (input) | 40% | 60% | BCLK period |
| S13 | SAI_FS input setup before SAI_BCLK | 10 | — | ns |
| S14 | SAI_FA input hold after SAI_BCLK | 2 | — | ns |
| S15 | SAI_BCLK to SAI_TXD/SAI_FS output valid | — | 20 | ns |
| S16 | SAI_BCLK to SAI_TXD/SAI_FS output invalid | 0 | — | ns |
| S17 | SAI_RXD setup before SAI_BCLK | 10 | — | ns |
| S18 | SAI_RXD hold after SAI_BCLK | 2 | — | ns |
| S19 | I2S_TX_FX input assertion to I2S_TXD output valid ¹ | — | 25 | ns |

¹ Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

4.12.16 SCAN JTAG Controller (SJC) Timing Parameters

Figure 64 depicts the SJC test clock input timing. Figure 65 depicts the SJC boundary scan timing. Figure 66 depicts the SJC test access port. Signal parameters are listed in Table 81.

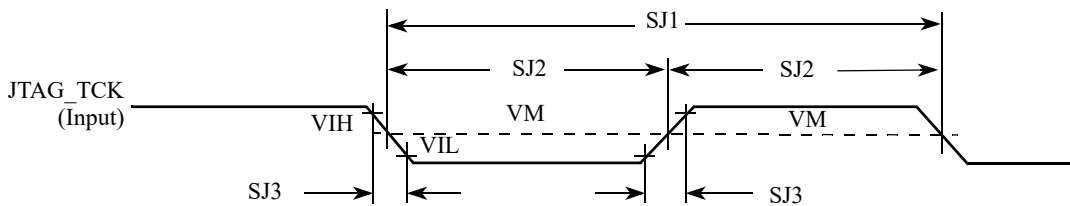


Figure 64. Test Clock Input Timing Diagram

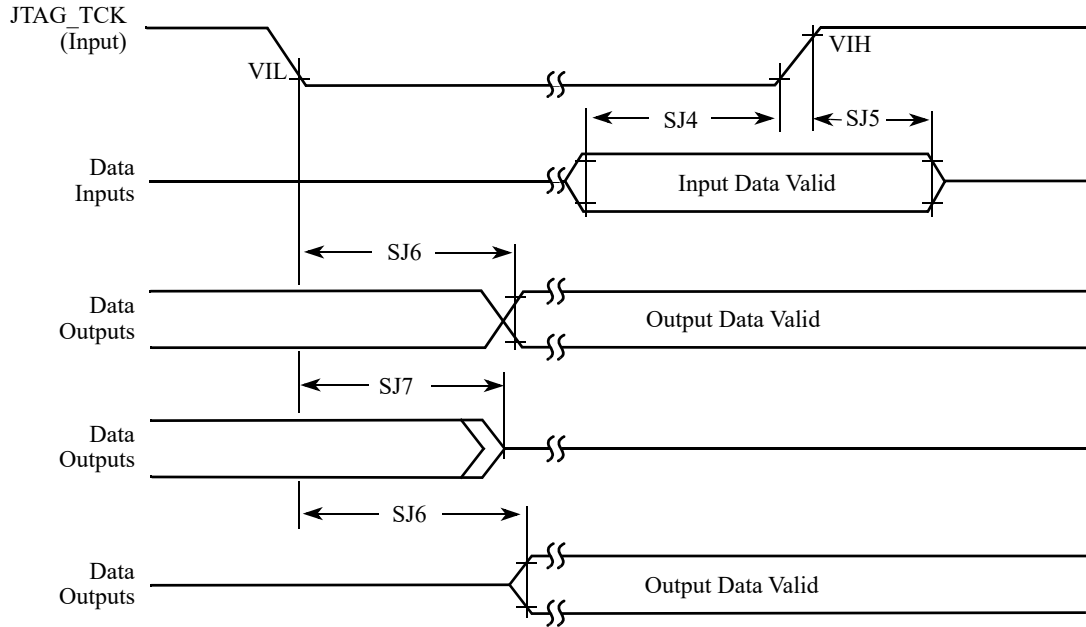


Figure 65. Boundary Scan (JTAG) Timing Diagram

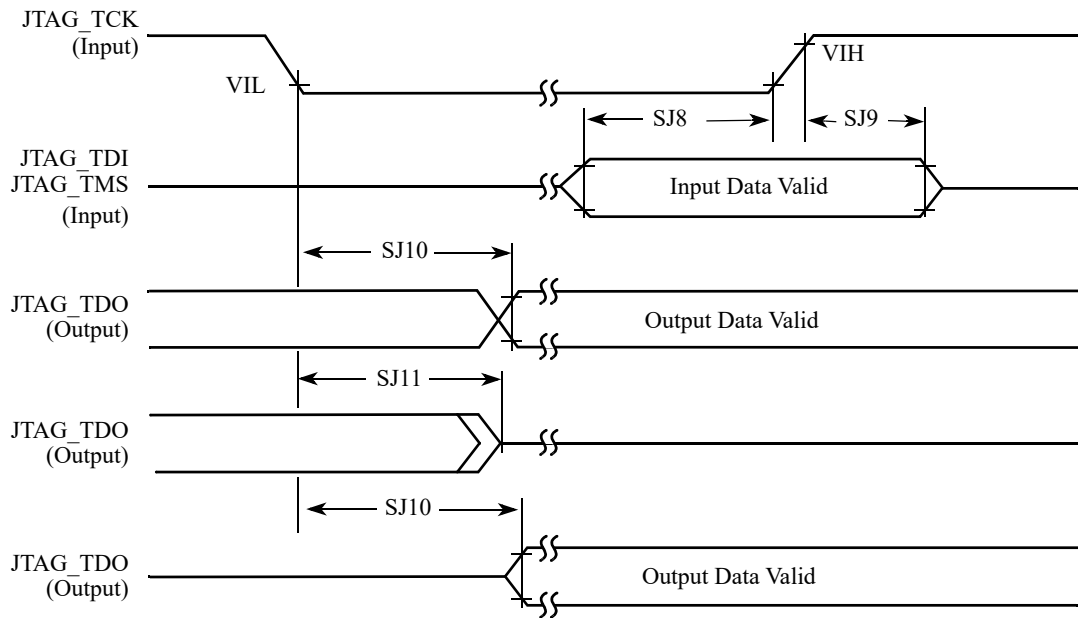


Figure 66. Test Access Port Timing Diagram

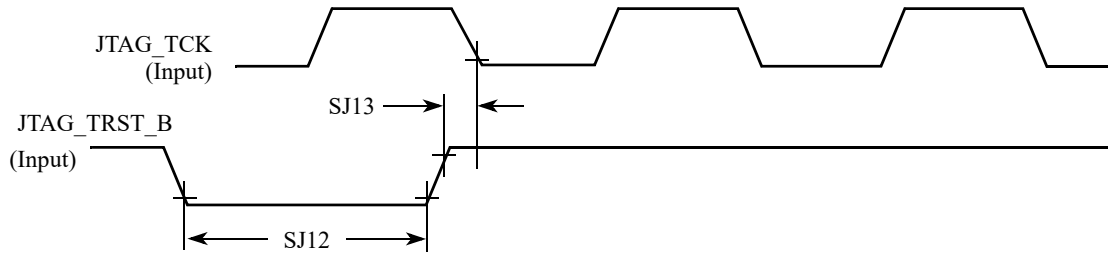


Figure 67. JTAG_TRST_B Timing Diagram

Table 81. JTAG Timing

| ID | Parameter ^{1,2} | All Frequencies | | Unit |
|------|--|-----------------|-----|------|
| | | Min | Max | |
| SJ0 | JTAG_TCK frequency of operation $1/(3 \cdot T_{DC})^1$ | 0.001 | 22 | MHz |
| SJ1 | JTAG_TCK cycle time in crystal mode | 45 | — | ns |
| SJ2 | JTAG_TCK clock pulse width measured at V_M^2 | 22.5 | — | ns |
| SJ3 | JTAG_TCK rise and fall times | — | 3 | ns |
| SJ4 | Boundary scan input data set-up time | 5 | — | ns |
| SJ5 | Boundary scan input data hold time | 24 | — | ns |
| SJ6 | JTAG_TCK low to output data valid | — | 40 | ns |
| SJ7 | JTAG_TCK low to output high impedance | — | 40 | ns |
| SJ8 | JTAG_TMS, JTAG_TDI data set-up time | 5 | — | ns |
| SJ9 | JTAG_TMS, JTAG_TDI data hold time | 25 | — | ns |
| SJ10 | JTAG_TCK low to JTAG_TDO data valid | — | 44 | ns |
| SJ11 | JTAG_TCK low to JTAG_TDO high impedance | — | 44 | ns |
| SJ12 | JTAG_TRST_B assert time | 100 | — | ns |
| SJ13 | JTAG_TRST_B set-up time to JTAG_TCK low | 40 | — | ns |

¹ T_{DC} = target frequency of SJC

² V_M = mid-point voltage

4.12.17 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 82 and Figure 68 and Figure 69 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

Table 82. SPDIF Timing Parameters

| Characteristics | Symbol | Timing Parameter Range | | Unit |
|--|--------|------------------------|------|------|
| | | Min | Max | |
| SPDIF_IN Skew: asynchronous inputs, no specs apply | — | — | 0.7 | ns |
| SPDIF_OUT output (Load = 50pf) | — | — | 1.5 | ns |
| • Skew | — | — | 24.2 | |
| • Transition rising | — | — | 31.3 | |
| SPDIF_OUT1 output (Load = 30pf) | — | — | 1.5 | ns |
| • Skew | — | — | 13.6 | |
| • Transition rising | — | — | 18.0 | |
| Modulating Rx clock (SPDIF_SR_CLK) period | srckp | 40.0 | — | ns |
| SPDIF_SR_CLK high period | srckph | 16.0 | — | ns |
| SPDIF_SR_CLK low period | srckpl | 16.0 | — | ns |
| Modulating Tx clock (SPDIF_ST_CLK) period | stckp | 40.0 | — | ns |
| SPDIF_ST_CLK high period | stckph | 16.0 | — | ns |
| SPDIF_ST_CLK low period | stckpl | 16.0 | — | ns |

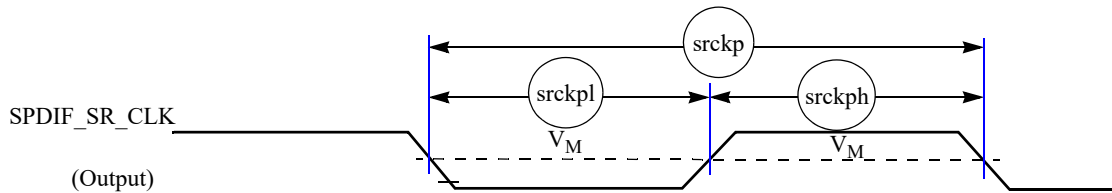


Figure 68. SPDIF_SR_CLK Timing Diagram

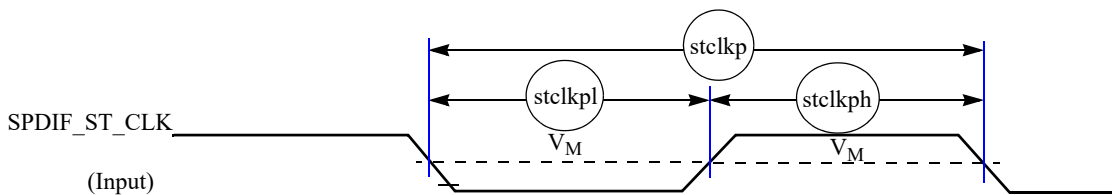


Figure 69. SPDIF_ST_CLK Timing Diagram

4.12.18 SSI Timing Parameters

This section describes the timing parameters of the SSI module. The connectivity of the serial synchronous interfaces are summarized in [Table 83](#).

Table 83. AUDMUX Port Allocation

| Port | Signal Nomenclature | Type and Access |
|---------------|---------------------|---------------------------------------|
| AUDMUX port 1 | SSI 1 | Internal |
| AUDMUX port 2 | SSI 2 | Internal |
| AUDMUX port 3 | AUD3 | External— LCD or SD4 through IOMUXC |
| AUDMUX port 4 | AUD4 | External— ENET or NAND through IOMUXC |
| AUDMUX port 5 | AUD5 | External— KPP or SD1 through IOMUXC |
| AUDMUX port 6 | AUD6 | External— SD2 or CSI through IOMUXC |
| AUDMUX port 7 | SSI 3 | Internal |

NOTE

The terms WL and BL used in the timing diagrams and tables refer to Word Length (WL) and Bit Length (BL).

4.12.18.1 SSI Transmitter Timing with Internal Clock

[Figure 70](#) depicts the SSI transmitter internal clock timing and [Table 84](#) lists the timing parameters for the SSI transmitter internal clock.

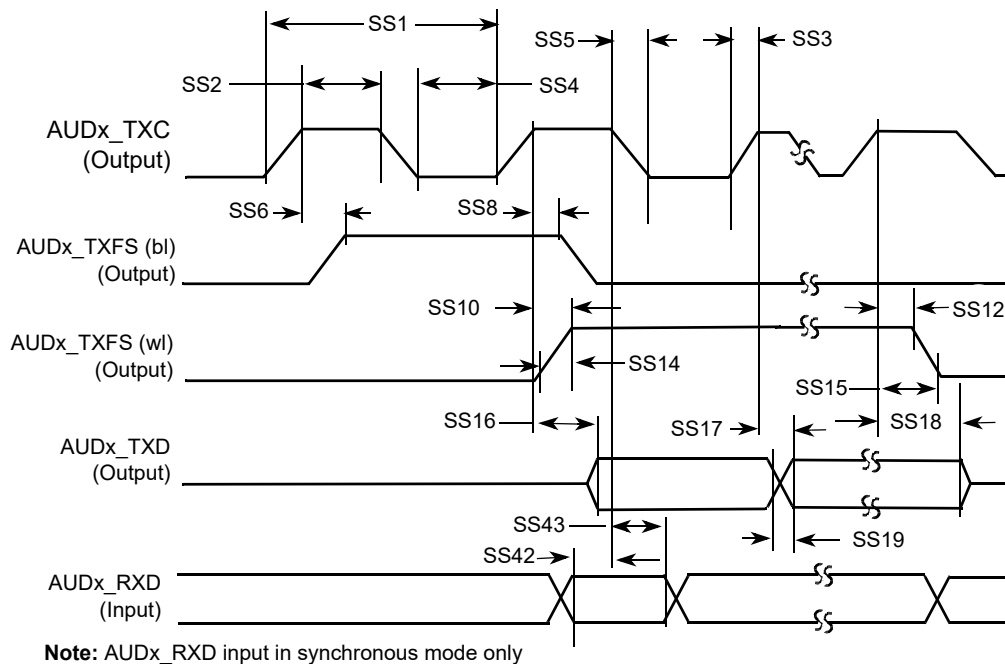


Figure 70. SSI Transmitter Internal Clock Timing Diagram

Table 84. SSI Transmitter Timing with Internal Clock

| ID | Parameter | Min | Max | Unit |
|---|---|------|------|------|
| Internal Clock Operation | | | | |
| SS1 | AUDx_TXC/AUDxRXC clock period | 81.4 | — | ns |
| SS2 | AUDx_TXC/AUDxRXC clock high period | 36.0 | — | ns |
| SS4 | AUDx_TXC/AUDxRXC clock low period | 36.0 | — | ns |
| SS6 | AUDx_TXC high to AUDx_TXFS (bl) high | — | 15.0 | ns |
| SS8 | AUDx_TXC high to AUDx_TXFS (bl) low | — | 15.0 | ns |
| SS10 | AUDx_TXC high to AUDx_TXFS (wl) high | — | 15.0 | ns |
| SS12 | AUDx_TXC high to AUDx_TXFS (wl) low | — | 15.0 | ns |
| SS14 | AUDx_TXC/AUDxRXC Internal AUDx_TXFS rise time | — | 6.0 | ns |
| SS15 | AUDx_TXC/AUDxRXC Internal AUDx_TXFS fall time | — | 6.0 | ns |
| SS16 | AUDx_TXC high to AUDx_TXD valid from high impedance | — | 15.0 | ns |
| SS17 | AUDx_TXC high to AUDx_TXD high/low | — | 15.0 | ns |
| SS18 | AUDx_TXC high to AUDx_TXD high impedance | — | 15.0 | ns |
| Synchronous Internal Clock Operation | | | | |
| SS42 | AUDx_RXD setup before AUDx_TXC falling | 10.0 | — | ns |
| SS43 | AUDx_RXD hold after AUDx_TXC falling | 0.0 | — | ns |

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

4.12.18.2 SSI Receiver Timing with Internal Clock

Figure 71 depicts the SSI receiver internal clock timing and Table 85 lists the timing parameters for the receiver timing with the internal clock.

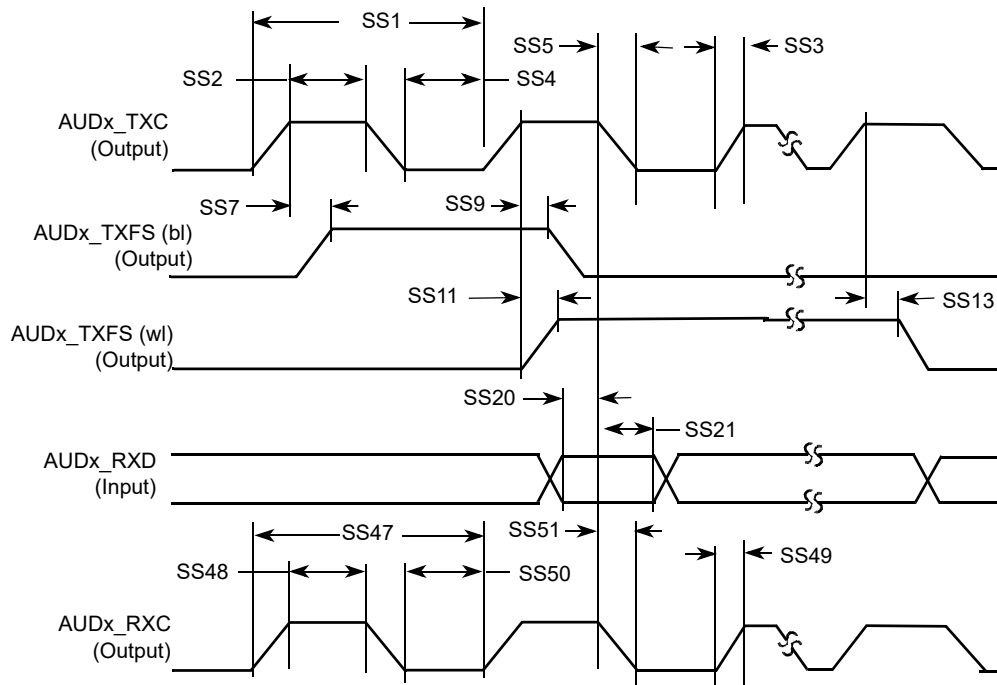


Figure 71. SSI Receiver Internal Clock Timing Diagram

Table 85. SSI Receiver Timing with Internal Clock

| ID | Parameter | Min | Max | Unit |
|---------------------------------|---|------|------|------|
| Internal Clock Operation | | | | |
| SS1 | AUDx_TXC/AUDx_RXC clock period | 81.4 | — | ns |
| SS2 | AUDx_TXC/AUDx_RXC clock high period | 36.0 | — | ns |
| SS3 | AUDx_TXC/AUDx_RXC clock rise time | — | 6.0 | ns |
| SS4 | AUDx_TXC/AUDx_RXC clock low period | 36.0 | — | ns |
| SS5 | AUDx_TXC/AUDx_RXC clock fall time | — | 6.0 | ns |
| SS7 | AUDx_RXC high to AUDx_TXFS (bl) high | — | 15.0 | ns |
| SS9 | AUDx_RXC high to AUDx_TXFS (bl) low | — | 15.0 | ns |
| SS11 | AUDx_RXC high to AUDx_TXFS (wl) high | — | 15.0 | ns |
| SS13 | AUDx_RXC high to AUDx_TXFS (wl) low | — | 15.0 | ns |
| SS20 | AUDx_RXD setup time before AUDx_RXC low | 10.0 | — | ns |
| SS21 | AUDx_RXD hold time after AUDx_RXC low | 0.0 | — | ns |

Table 85. SSI Receiver Timing with Internal Clock (continued)

| ID | Parameter | Min | Max | Unit |
|-------------------------------------|--------------------------------|-------|-----|------|
| Oversampling Clock Operation | | | | |
| SS47 | Oversampling clock period | 15.04 | — | ns |
| SS48 | Oversampling clock high period | 6.0 | — | ns |
| SS49 | Oversampling clock rise time | — | 3.0 | ns |
| SS50 | Oversampling clock low period | 6.0 | — | ns |
| SS51 | Oversampling clock fall time | — | 3.0 | ns |

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

4.12.18.3 SSI Transmitter Timing with External Clock

Figure 72 depicts the SSI transmitter external clock timing and Table 86 lists the timing parameters for the transmitter timing with the external clock.

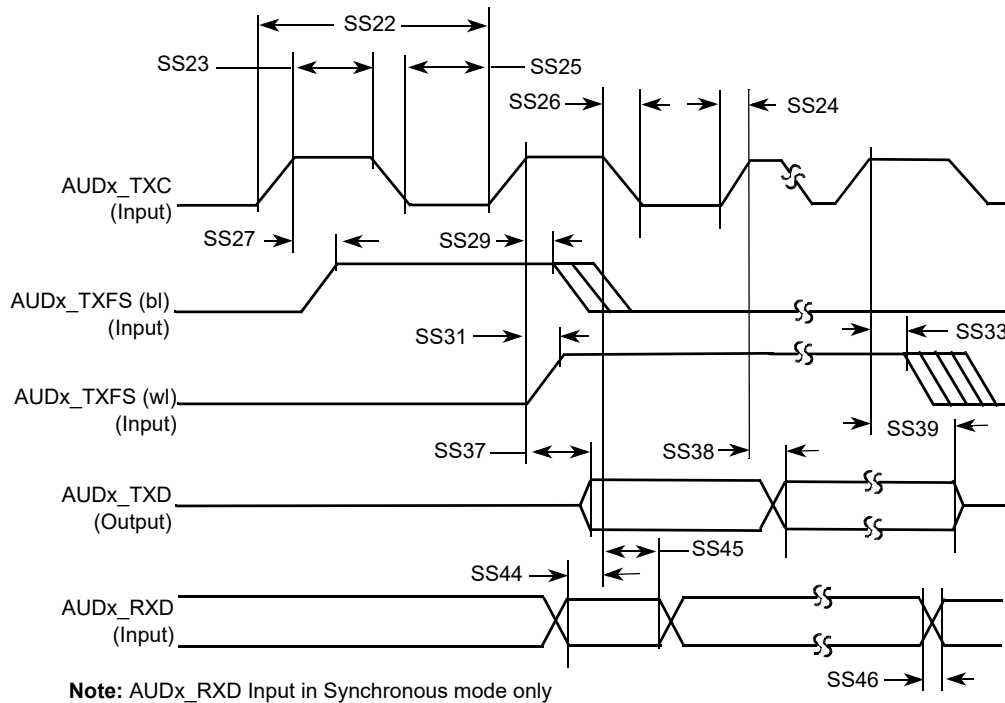


Figure 72. SSI Transmitter External Clock Timing Diagram

Table 86. SSI Transmitter Timing with External Clock

| ID | Parameter | Min | Max | Unit |
|---------------------------------|---|-------|------|------|
| External Clock Operation | | | | |
| SS22 | AUDx_TXC/AUDx_RXC clock period | 81.4 | — | ns |
| SS23 | AUDx_TXC/AUDx_RXC clock high period | 36.0 | — | ns |
| SS24 | AUDx_TXC/AUDx_RXC clock rise time | — | 6.0 | ns |
| SS25 | AUDx_TXC/AUDx_RXC clock low period | 36.0 | — | ns |
| SS26 | AUDx_TXC/AUDx_RXC clock fall time | — | 6.0 | ns |
| SS27 | AUDx_TXC high to AUDx_TXFS (bl) high | -10.0 | 15.0 | ns |
| SS29 | AUDx_TXC high to AUDx_TXFS (bl) low | 10.0 | — | ns |
| SS31 | AUDx_TXC high to AUDx_TXFS (wl) high | -10.0 | 15.0 | ns |
| SS33 | AUDx_TXC high to AUDx_TXFS (wl) low | 10.0 | — | ns |
| SS37 | AUDx_TXC high to AUDx_TXD valid from high impedance | — | 15.0 | ns |
| SS38 | AUDx_TXC high to AUDx_TXD high/low | — | 15.0 | ns |
| SS39 | AUDx_TXC high to AUDx_TXD high impedance | — | 15.0 | ns |

Table 86. SSI Transmitter Timing with External Clock (continued)

| ID | Parameter | Min | Max | Unit |
|---|--|------|-----|------|
| Synchronous External Clock Operation | | | | |
| SS44 | AUDx_RXD setup before AUDx_TXC falling | 10.0 | — | ns |
| SS45 | AUDx_RXD hold after AUDx_TXC falling | 2.0 | — | ns |
| SS46 | AUDx_RXD rise/fall time | — | 6.0 | ns |

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

4.12.18.4 SSI Receiver Timing with External Clock

Figure 73 depicts the SSI receiver external clock timing and Table 87 lists the timing parameters for the receiver timing with the external clock.

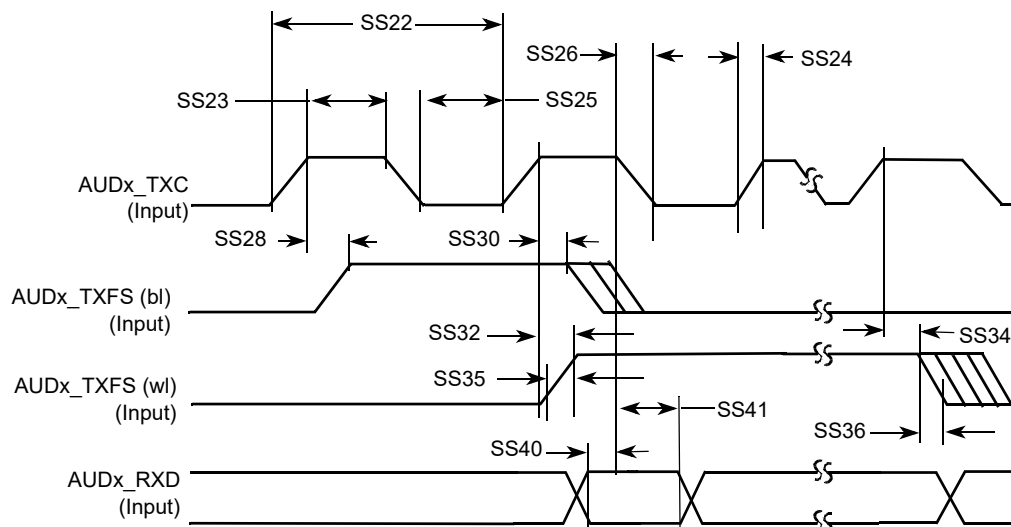


Figure 73. SSI Receiver External Clock Timing Diagram

Table 87. SSI Receiver Timing with External Clock

| ID | Parameter | Min | Max | Unit |
|---------------------------------|--|------|------|------|
| External Clock Operation | | | | |
| SS22 | AUDx_TXC/AUDx_RXC clock period | 81.4 | — | ns |
| SS23 | AUDx_TXC/AUDx_RXC clock high period | 36 | — | ns |
| SS24 | AUDx_TXC/AUDx_RXC clock rise time | — | 6.0 | ns |
| SS25 | AUDx_TXC/AUDx_RXC clock low period | 36 | — | ns |
| SS26 | AUDx_TXC/AUDx_RXC clock fall time | — | 6.0 | ns |
| SS28 | AUDx_RXC high to AUDx_TXFS (bl) high | -10 | 15.0 | ns |
| SS30 | AUDx_RXC high to AUDx_TXFS (bl) low | 10 | — | ns |
| SS32 | AUDx_RXC high to AUDx_TXFS (wl) high | -10 | 15.0 | ns |
| SS34 | AUDx_RXC high to AUDx_TXFS (wl) low | 10 | — | ns |
| SS35 | AUDx_TXC/AUDx_RXC External AUDx_TXFS rise time | — | 6.0 | ns |
| SS36 | AUDx_TXC/AUDx_RXC External AUDx_TXFS fall time | — | 6.0 | ns |
| SS40 | AUDx_RXD setup time before AUDx_RXC low | 10 | — | ns |
| SS41 | AUDx_RXD hold time after AUDx_RXC low | 2 | — | ns |

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

4.12.19 UART I/O Configuration and Timing Parameters**4.12.19.1 UART RS-232 Serial Mode Timing**

The following sections describe the electrical information of the UART module in the RS-232 mode.

4.12.19.1.1 UART Transmitter

Figure 74 depicts the transmit timing of UART in the RS-232 serial mode, with 8 data bit/1 stop bit format. Table 88 lists the UART RS-232 serial mode transmit timing characteristics.

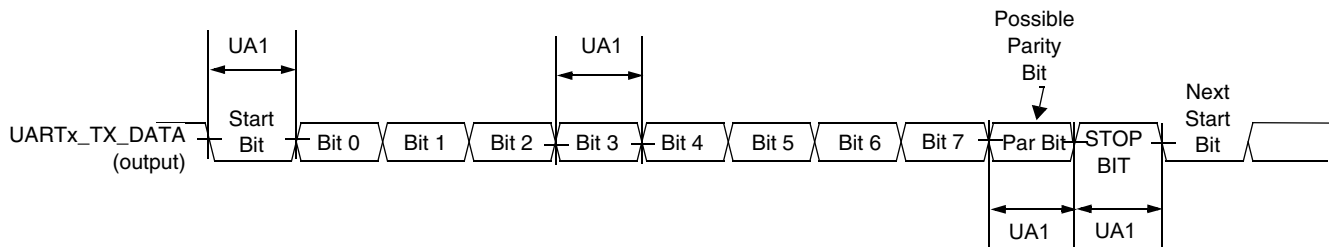


Figure 74. UART RS-232 Serial Mode Transmit Timing Diagram

Table 88. RS-232 Serial Mode Transmit Timing Parameters

| ID | Parameter | Symbol | Min | Max | Unit |
|-----|-------------------|------------|---------------------------------------|-----------------------------------|------|
| UA1 | Transmit Bit Time | t_{Tbit} | $1/F_{baud_rate}^1 - T_{ref_clk}^2$ | $1/F_{baud_rate} + T_{ref_clk}$ | — |

¹ F_{baud_rate} : Baud rate frequency. The maximum baud rate the UART can support is $(ipg_perclk \text{ frequency})/16$.

² T_{ref_clk} : The period of UART reference clock ref_clk (ipg_perclk after RFDIV divider).

4.12.19.1.2 UART Receiver

Figure 75 depicts the RS-232 serial mode receive timing with 8 data bit/1 stop bit format. Table 89 lists serial mode receive timing characteristics.

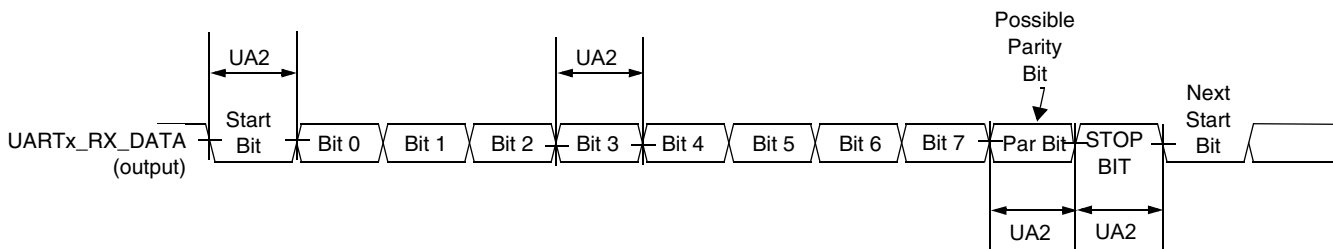


Figure 75. UART RS-232 Serial Mode Receive Timing Diagram

Table 89. RS-232 Serial Mode Receive Timing Parameters

| ID | Parameter | Symbol | Min | Max | Unit |
|-----|-------------------------------|------------|---|---|------|
| UA2 | Receive Bit Time ¹ | t_{Rbit} | $1/F_{baud_rate}^2 - 1/(16 \times F_{baud_rate})$ | $1/F_{baud_rate} + 1/(16 \times F_{baud_rate})$ | — |

¹ The UART receiver can tolerate $1/(16 \times F_{baud_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud_rate})$.

² F_{baud_rate} : Baud rate frequency. The maximum baud rate the UART can support is $(ipg_perclk \text{ frequency})/16$.

4.12.19.1.3 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

UART IrDA Mode Transmitter

Figure 76 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 90 lists the transmit timing characteristics.

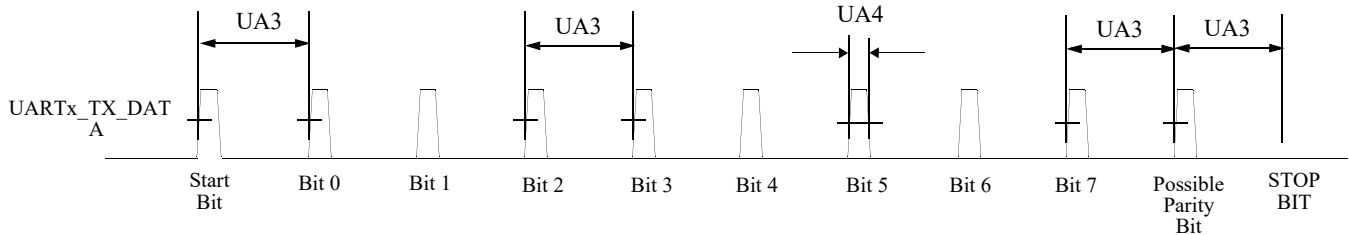


Figure 76. UART IrDA Mode Transmit Timing Diagram

Table 90. IrDA Mode Transmit Timing Parameters

| ID | Parameter | Symbol | Min | Max | Unit |
|-----|--------------------------------|----------------|---|---|------|
| UA3 | Transmit Bit Time in IrDA mode | t_{TIRbit} | $1/F_{baud_rate}^1 - T_{ref_clk}^2$ | $1/F_{baud_rate} + T_{ref_clk}$ | — |
| UA4 | Transmit IR Pulse Duration | $t_{TIRpulse}$ | $(3/16) \times (1/F_{baud_rate}) - T_{ref_clk}$ | $(3/16) \times (1/F_{baud_rate}) + T_{ref_clk}$ | — |

¹ F_{baud_rate} : Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

² T_{ref_clk} : The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

UART IrDA Mode Receiver

Figure 77 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 91 lists the receive timing characteristics.

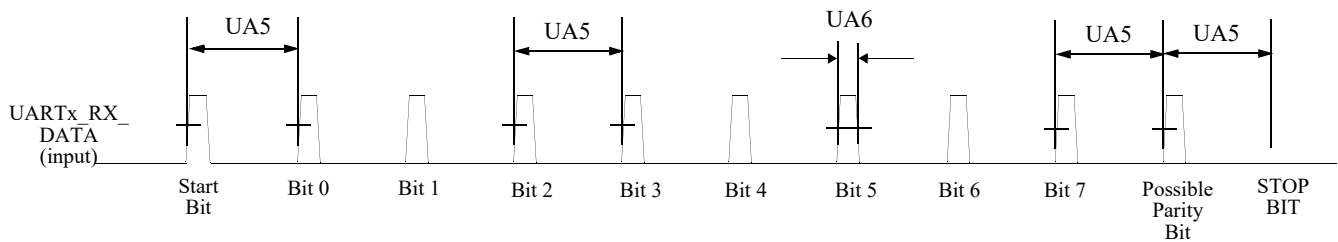


Figure 77. UART IrDA Mode Receive Timing Diagram

Table 91. IrDA Mode Receive Timing Parameters

| ID | Parameter | Symbol | Min | Max | Unit |
|-----|--|----------------|---|---|------|
| UA5 | Receive Bit Time ¹ in IrDA mode | t_{RIRbit} | $1/F_{baud_rate}^2 - 1/(16 \times F_{baud_rate})$ | $1/F_{baud_rate} + 1/(16 \times F_{baud_rate})$ | — |
| UA6 | Receive IR Pulse Duration | $t_{RIRpulse}$ | 1.41 μ s | $(5/16) \times (1/F_{baud_rate})$ | — |

- ¹ The UART receiver can tolerate $1/(16 \times F_{\text{baud_rate}})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{\text{baud_rate}})$.
- ² $F_{\text{baud_rate}}$: Baud rate frequency. The maximum baud rate the UART can support is $(\text{ipg_perclk frequency})/16$.

4.12.20 USB HSIC Timings

This section describes the electrical information of the USB HSIC port.

NOTE

In [Figure 78](#), HSIC is a DDR interface and the timing parameters shown refer to both rising and falling edges.

4.12.20.1 Transmit Timing

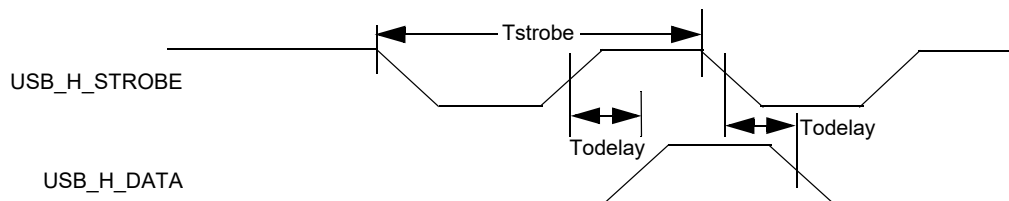


Figure 78. USB HSIC Transmit Waveform

Table 92. USB HSIC Transmit Parameters

| Name | Parameter | Min | Max | Unit | Comment |
|---------|---------------------------------|-------|-------|------|--------------------------------|
| Tstrobe | strobe period | 4.166 | 4.167 | ns | — |
| Todelay | data output delay time | 550 | 1350 | ps | Measured at 50% point |
| Tslew | strobe/data rising/falling time | 0.7 | 2 | V/ns | Averaged from 30% – 70% points |

4.12.20.2 Receive Timing

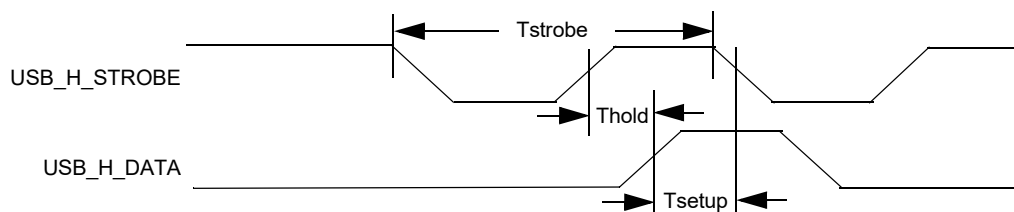


Figure 79. USB HSIC Receive Waveform

Table 93. USB HSIC Receive Parameters¹

| Name | Parameter | Min | Max | Unit | Comment |
|---------|----------------|-------|-------|------|-----------------------|
| Tstrobe | strobe period | 4.166 | 4.167 | ns | — |
| Thold | data hold time | 300 | — | ps | Measured at 50% point |

Table 93. USB HSIC Receive Parameters¹ (continued)

| Name | Parameter | Min | Max | Unit | Comment |
|--------|---------------------------------|-----|-----|------|--------------------------------|
| Tsetup | data setup time | 365 | — | ps | Measured at 50% point |
| Tslew | strobe/data rising/falling time | 0.7 | 2 | V/ns | Averaged from 30% – 70% points |

¹ The timings in the table are guaranteed when:
—AC I/O voltage is between 0.9x to 1x of the I/O supply
—DDR_SEL configuration bits of the I/O are set to (10)b

4.12.21 USB PHY Parameters

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

The USB PHY meets the electrical compliance requirements defined in revision 2.0 of the *USB On-The-Go and Embedded Host Supplement to the USB 2.0 Specification* with the amendments below (*On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification* is not applicable to Host port).

- USB ENGINEERING CHANGE NOTICE
 - Title: 5V Short Circuit Withstand Requirement Change
 - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
 - Title: Pull-up/Pull-down resistors
 - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
 - Title: Suspend Current Limit Changes
 - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
 - Title: USB 2.0 Phase Locked SOFs
 - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
 - Revision 2.0 plus errata and ECN June 4, 2010
- Battery Charging Specification (available from USB-IF)
 - Revision 1.2, December 7, 2010
 - Portable device only

4.13 A/D Converter

4.13.1 12-bit ADC Electrical Characteristics

4.13.1.1 12-bit ADC Operating Conditions

Table 94. 12-bit ADC Operating Conditions

| Characteristic | Conditions | Symbol | Min | Typ ¹ | Max | Unit | Comment |
|---|---|-------------------|-------------------|-------------------|-------------------|-------|--------------------------|
| Supply voltage | Absolute | VDDA_ADC_3P3 | 3.0 | - | 3.6 | V | — |
| | Delta to VDD (VDD-VDDA_ADC_3P3) ² | VDDA_ADC_3P3 | -100 | 0 | 100 | mV | — |
| Ground voltage | Delta to VSS (VSS-VSSAD) | Δ VSSAD | -100 | 0 | 100 | mV | — |
| Ref Voltage High | — | V _{REFH} | 1.13 | VDDA_ADC_3P3 | VDDA_ADC_3P3 | V | — |
| Ref Voltage Low | — | V _{REFL} | V _{SSAD} | V _{SSAD} | V _{SSAD} | V | — |
| Input Voltage | — | V _{ADIN} | V _{REFL} | — | V _{REFH} | V | — |
| Input Capacitance | 8/10/12 bit modes | C _{ADIN} | — | 1.5 | 2 | pF | — |
| Input Resistance | ADLPC=0, ADHSC=1 | R _{ADIN} | — | 5 | 7 | kohms | — |
| | ADLPC=0, ADHSC=0 | | — | 12.5 | 15 | kohms | — |
| | ADLPC=1, ADHSC=0 | | — | 25 | 30 | kohms | — |
| Analog Source Resistance | 12 bit mode f _{ADCK} = 40MHz ADLSMP=0, ADSTS=10, ADHSC=1 | R _{AS} | — | — | 1 | kohms | T _{samp} =150ns |
| R _{AS} depends on Sample Time Setting (ADLSMP, ADSTS) and ADC Power Mode (ADHSC, ADLPC). See charts for Minimum Sample Time versus R _{AS} | | | | | | | |
| ADC Conversion Clock Frequency | ADLPC=0, ADHSC=1 12 bit mode | f _{ADCK} | 4 | — | 40 | MHz | — |
| | ADLPC=0, ADHSC=0 12 bit mode | | 4 | — | 30 | MHz | — |
| | ADLPC=1, ADHSC=0 12 bit mode | | 4 | — | 20 | MHz | — |

¹ Typical values assume VDDA_ADC_3P3= 3.0 V, Temp = 25°C, f_{ADCK}=20 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

² DC potential difference

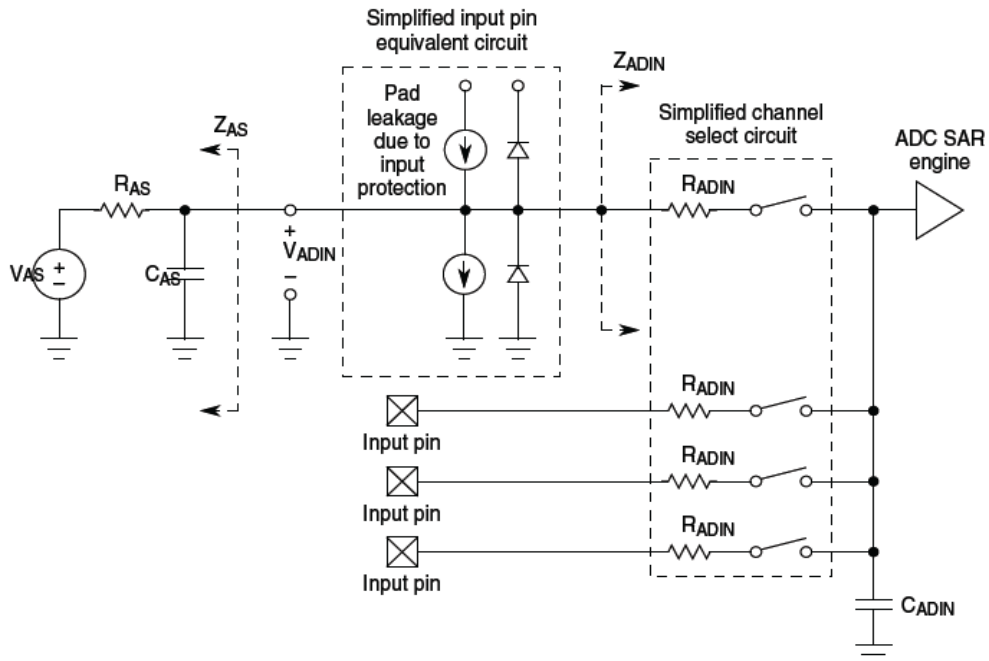


Figure 80. 12-bit ADC Input Impedance Equivalency Diagram

4.13.1.2 12-bit ADC Characteristics

Table 95. 12-bit ADC Characteristics ($V_{REFH} = VDDA_ADC_3P3$, $V_{REFL} = V_{SSAD}$)

| Characteristic | Conditions ¹ | Symbol | Min | Typ ² | Max | Unit | Comment |
|-------------------------------|-------------------------|-------------|-----|------------------|-----|---------|--------------------------------|
| [L:] Supply Current | ADLPC=1, ADHSC=0 | I_{DDAD} | — | 250 | — | μA | ADLSMP=0 ADSTS=10 ADCO=1 |
| | ADLPC=0, ADHSC=0 | | | 350 | | | |
| | ADLPC=0, ADHSC=1 | | | 400 | | | |
| [L:] Supply Current | Stop, Reset, Module Off | I_{DDAD} | — | 0.01 | 0.8 | μA | — |
| ADC Asynchronous Clock Source | ADHSC=0 | f_{ADACK} | — | 10 | — | MHz | $t_{ADACK} = 1/f_{ADACK}$ |
| | ADHSC=1 | | | 20 | | | |
| Sample Cycles | ADLSMP=0, ADSTS=00 | C_{samp} | — | 2 | — | cycles | — |
| | ADLSMP=0, ADSTS=01 | | | 4 | | | |
| | ADLSMP=0, ADSTS=10 | | | 6 | | | |
| | ADLSMP=0, ADSTS=11 | | | 8 | | | |
| | ADLSMP=1, ADSTS=00 | | | 12 | | | |
| | ADLSMP=1, ADSTS=01 | | | 16 | | | |
| | ADLSMP=1, ADSTS=10 | | | 20 | | | |
| | ADLSMP=1, ADSTS=11 | | | 24 | | | |

Table 95. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA_ADC_3P3}$, $V_{REFL} = V_{SSAD}$) (continued)

| Characteristic | Conditions ¹ | Symbol | Min | Typ ² | Max | Unit | Comment | | | |
|-------------------------------------|-------------------------|-----------------|-----|------------------|-------|--|--|-------|---|------|
| Conversion Cycles | ADLSMP=0 ADSTS=00 | Cconv | — | 28 | — | cycles | — | | | |
| | ADLSMP=0 ADSTS=01 | | | 30 | | | | | | |
| | ADLSMP=0 ADSTS=10 | | | 32 | | | | | | |
| | ADLSMP=0 ADSTS=11 | | | 34 | | | | | | |
| | ADLSMP=1 ADSTS=00 | | | 38 | | | | | | |
| | ADLSMP=1 ADSTS=01 | | | 42 | | | | | | |
| | ADLSMP=1 ADSTS=10 | | | 46 | | | | | | |
| | ADLSMP=1, ADSTS=11 | | | 50 | | | | | | |
| Conversion Time | ADLSMP=0 ADSTS=00 | Tconv | — | 0.7 | — | μs | Fadc=40 MHz | | | |
| | ADLSMP=0 ADSTS=01 | | | 0.75 | | | | | | |
| | ADLSMP=0 ADSTS=10 | | | 0.8 | | | | | | |
| | ADLSMP=0 ADSTS=11 | | | 0.85 | | | | | | |
| | ADLSMP=1 ADSTS=00 | | | 0.95 | | | | | | |
| | ADLSMP=1 ADSTS=01 | | | 1.05 | | | | | | |
| | ADLSMP=1 ADSTS=10 | | | 1.15 | | | | | | |
| | ADLSMP=1, ADSTS=11 | | | 1.25 | | | | | | |
| [P:][C:] Total Unadjusted Error | 12 bit mode | TUE | -2 | — | +5 | LSB 1 LSB = ($V_{REFH} - V_{REFL}$)/2N | With Max Averaging | | | |
| | 10 bit mode | | | | | | | -0.5 | — | +2 |
| | 8 bit mode | | | | | | | -0.25 | — | +1.5 |
| [P:][C:] Differential Non-Linearity | 12 bit mode | DNL | — | ±0.6 | ±2.5 | LSB | Waiting for histogram method confirmation | | | |
| | 10bit mode | | | ±0.5 | ±1 | | | | | |
| | 8 bit mode | | | ±0.25 | ±0.5 | | | | | |
| [P:][C:] Integral Non-Linearity | 12 bit mode | INL | — | ±2 | ±5 | LSB | Waiting for histogram method confirmation | | | |
| | 10bit mode | | | ±1 | ±2 | | | | | |
| | 8 bit mode | | | ±0.5 | ±1 | | | | | |
| Zero-Scale Error | 12 bit mode | E _{ZS} | — | 1 | 2 | LSB | VADIN = V _{REFL} With Max Averaging | | | |
| | 10bit mode | | | 0.5 | 1 | | | | | |
| | 8 bit mode | | | 0.2 | 0.5 | | | | | |
| Full-Scale Error | 12 bit mode | E _{FS} | — | ±2 | +1/-6 | LSB | VADIN = V _{REFH} With Max Averaging | | | |
| | 10bit mode | | | ±0.5 | ±1/-2 | | | | | |
| | 8 bit mode | | | ±0.25 | ±0.75 | | | | | |

Electrical Characteristics

Table 95. 12-bit ADC Characteristics ($V_{REFH} = VDDA_ADC_3P3$, $V_{REFL} = V_{SSAD}$) (continued)

| Characteristic | Conditions ¹ | Symbol | Min | Typ ² | Max | Unit | Comment |
|--------------------------------------|-------------------------|--------|----------------------------|------------------|-----|------|-------------|
| [L:] Effective Number of Bits | 12 bit mode | ENOB | 10.1 | 10.7 | — | Bits | Fin = 100Hz |
| [L:] Signal to Noise plus Distortion | See ENOB | SINAD | SINAD = 6.02 x ENOB + 1.76 | | | dB | — |

¹ All accuracy numbers assume the ADC is calibrated with $V_{REFH}=VDDA_ADC_3P3$

² Typical values assume $VDDA_ADC_3P3 = 3.0$ V, Temp = 25°C, $F_{adck}=20$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

NOTE

The ADC electrical spec is met with the calibration enabled configuration.

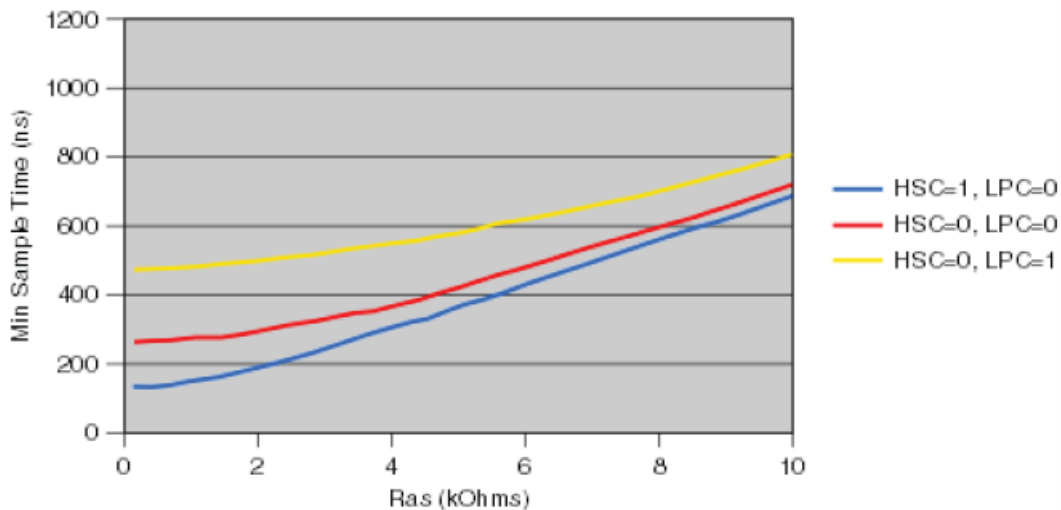


Figure 81. Minimum Sample Time versus Ras (Cas = 2pF)

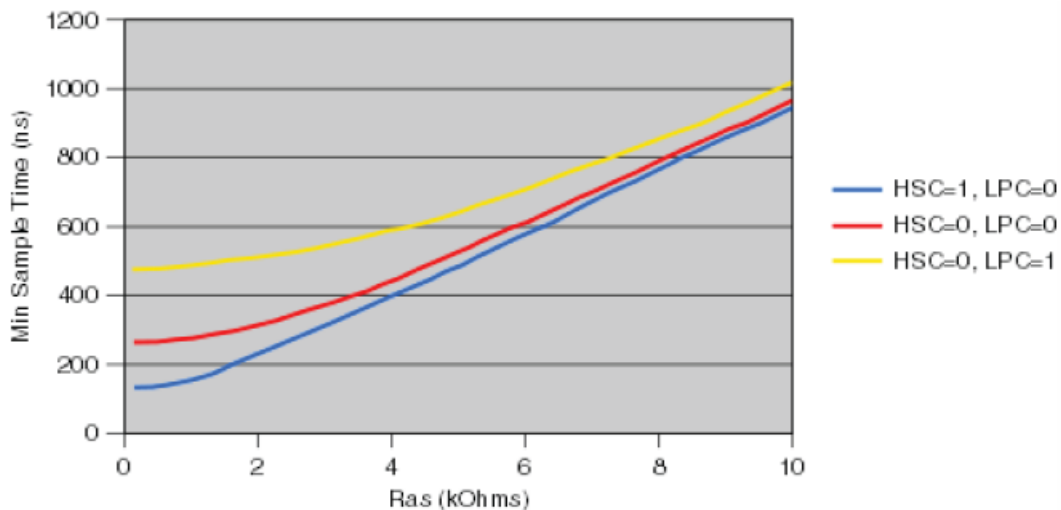


Figure 82. Minimum Sample Time versus Ras (Cas = 5pF)

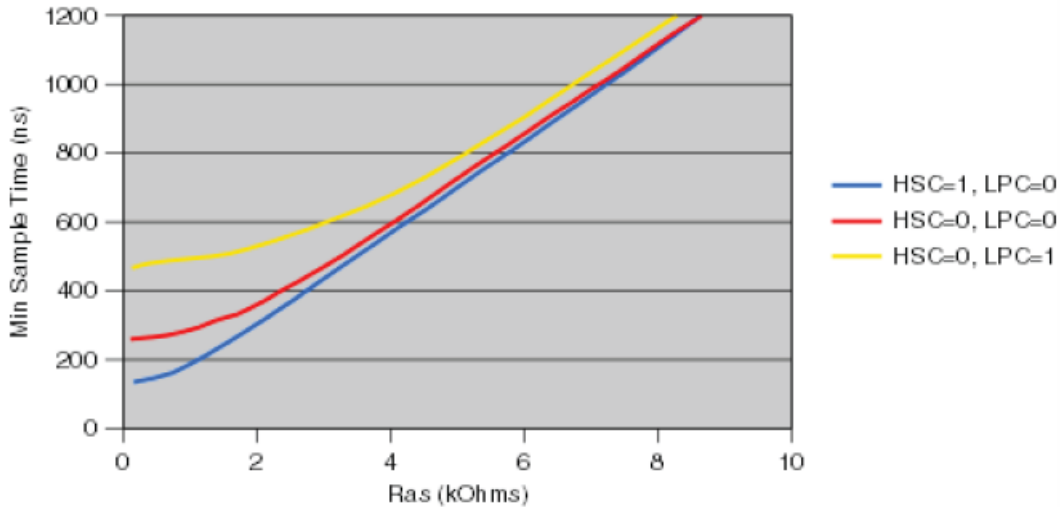


Figure 83. Minimum Sample Time versus Ras (Cas = 10pF)

5 Boot Mode Configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot Mode Configuration Pins

Table 96 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX 6SoloX Fuse Map chapter and the System Boot chapter in *i.MX 6SoloX Applications Processor Reference Manual (IMX6SXRM)*.

Table 96. Fuses and Associated Pins Used for Boot

| Pin | Direction at reset | eFuse name | State during reset (POR_B asserted) | State after reset (POR_B deasserted) | Details |
|------------|--------------------|------------|-------------------------------------|--------------------------------------|---------------------|
| BOOT_MODE0 | Input | N/A | Hi-Z | Hi-Z | Boot mode selection |
| BOOT_MODE1 | Input | N/A | Hi-Z | Hi-Z | Bootmode selection |

Table 96. Fuses and Associated Pins Used for Boot (continued)

| Pin | Direction at reset | eFuse name | State during reset (POR_B asserted) | State after reset (POR_B deasserted) | Details |
|-------------|--------------------|------------|-------------------------------------|--------------------------------------|--|
| LCD1_DATA00 | Input | BT_CFG1[0] | 100K Pull Down | Keeper | Boot Options, Pin value overrides fuse settings for BT_FUSE_SEL='0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses. |
| LCD1_DATA01 | Input | BT_CFG1[1] | 100K Pull Down | Keeper | |
| LCD1_DATA02 | Input | BT_CFG1[2] | 100K Pull Down | Keeper | |
| LCD1_DATA03 | Input | BT_CFG1[3] | 100K Pull Down | Keeper | |
| LCD1_DATA04 | Input | BT_CFG1[4] | 100K Pull Down | Keeper | |
| LCD1_DATA05 | Input | BT_CFG1[5] | 100K Pull Down | Keeper | |
| LCD1_DATA06 | Input | BT_CFG1[6] | 100K Pull Down | Keeper | |
| LCD1_DATA07 | Input | BT_CFG1[7] | 100K Pull Down | Keeper | |
| LCD1_DATA08 | Input | BT_CFG2[0] | 100K Pull Down | Keeper | |
| LCD1_DATA09 | Input | BT_CFG2[1] | 100K Pull Down | Keeper | |
| LCD1_DATA10 | Input | BT_CFG2[2] | 100K Pull Down | Keeper | |
| LCD1_DATA11 | Input | BT_CFG2[3] | 100K Pull Down | Keeper | |
| LCD1_DATA12 | Input | BT_CFG2[4] | 100K Pull Down | Keeper | |
| LCD1_DATA13 | Input | BT_CFG2[5] | 100K Pull Down | Keeper | |
| LCD1_DATA14 | Input | BT_CFG2[6] | 100K Pull Down | Keeper | |
| LCD1_DATA15 | Input | BT_CFG2[7] | 100K Pull Down | Keeper | |
| LCD1_DATA16 | Input | BT_CFG4[0] | 100K Pull Down | Keeper | |
| LCD1_DATA17 | Input | BT_CFG4[1] | 100K Pull Down | Keeper | |
| LCD1_DATA18 | Input | BT_CFG4[2] | 100K Pull Down | Keeper | |
| LCD1_DATA19 | Input | BT_CFG4[3] | 100K Pull Down | Keeper | |
| LCD1_DATA20 | Input | BT_CFG4[4] | 100K Pull Down | Keeper | |
| LCD1_DATA21 | Input | BT_CFG4[5] | 100K Pull Down | Keeper | |
| LCD1_DATA22 | Input | BT_CFG4[6] | 100K Pull Down | Keeper | |
| LCD1_DATA23 | Input | BT_CFG4[7] | 100K Pull Down | Keeper | |

5.2 Boot Device Interface Allocation

The tables below list the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The tables also describe the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 97. QSPI Boot through QSPI1

| Ball Name | Signal Name | Mux Mode | Common | Quad Mode | + Port A DQS | + Port A CS1 | + Port B | + Port B DQS | + Port B CS1 |
|--------------|-----------------|----------|--------|-----------|--------------|--------------|----------|--------------|--------------|
| QSPI1A_SCLK | qspi1.A_SCLK | Alt0 | Yes | Yes | — | — | — | — | — |
| QSPI1A_SS0_B | qspi1.A_SS0_B | Alt0 | Yes | Yes | — | — | — | — | — |
| QSPI1A_DATA0 | qspi1.A_DATA[0] | Alt0 | Yes | Yes | — | — | — | — | — |
| QSPI1A_DATA1 | qspi1.A_DATA[1] | Alt0 | Yes | Yes | — | — | — | — | — |
| QSPI1A_DATA2 | qspi1.A_DATA[2] | Alt0 | Yes | Yes | — | — | — | — | — |
| QSPI1A_DATA3 | qspi1.A_DATA[3] | Alt0 | Yes | Yes | — | — | — | — | — |
| QSPI1B_DATA3 | qspi1.B_DATA[3] | Alt0 | — | — | — | — | Yes | — | — |
| QSPI1B_DATA2 | qspi1.B_DATA[2] | Alt0 | — | — | — | — | Yes | — | — |
| QSPI1B_DATA1 | qspi1.B_DATA[1] | Alt0 | — | — | — | — | Yes | — | — |
| QSPI1B_DATA0 | qspi1.B_DATA[0] | Alt0 | — | — | — | — | Yes | — | — |
| QSPI1B_SS0_B | qspi1.B_SS0_B | Alt0 | — | — | — | — | Yes | — | — |
| QSPI1B_SCLK | qspi1.B_SCLK | Alt0 | — | — | — | — | Yes | — | — |
| QSPI1A_SS1_B | qspi1.A_SS1_B | Alt0 | — | — | — | Yes | — | — | — |
| QSPI1A_DQS | qspi1.A_DQS | Alt0 | — | — | Yes | — | — | — | — |
| QSPI1B_SS1_B | qspi1.B_SS1_B | Alt0 | — | — | — | — | — | — | Yes |
| QSPI1B_DQS | qspi1.B_DQS | Alt0 | — | — | — | — | — | Yes | — |

Table 98. QPSI Boot through QPSI2

| Ball Name | Signal Name | Mux Mode | Common | Quad Mode | + Port A DQS | + Port A CS1 | + Port B | + Port B DQS | + Port B CS1 |
|--------------|-----------------|----------|--------|-----------|--------------|--------------|----------|--------------|--------------|
| NAND_CLE | qspi2.A_SCLK | Alt2 | Yes | Yes | — | — | — | — | — |
| NAND_ALE | qspi2.A_SS0_B | Alt2 | Yes | Yes | — | — | — | — | — |
| NAND_WP_B | qspi2.A_DATA[0] | Alt2 | Yes | Yes | — | — | — | — | — |
| NAND_READY_B | qspi2.A_DATA[1] | Alt2 | Yes | Yes | — | — | — | — | — |
| NAND_CE0_B | qspi2.A_DATA[2] | Alt2 | Yes | Yes | — | — | — | — | — |
| NAND_CE1_B | qspi2.A_DATA[3] | Alt2 | Yes | Yes | — | — | — | — | — |
| NAND_RE_B | qspi2.B_DATA[3] | Alt2 | — | — | — | — | Yes | — | — |
| NAND_WE_B | qspi2.B_DATA[2] | Alt2 | — | — | — | — | Yes | — | — |
| NAND_DATA00 | qspi2.B_DATA[1] | Alt2 | — | — | — | — | Yes | — | — |

Table 98. QPSI Boot through QPSI2 (continued)

| Ball Name | Signal Name | Mux Mode | Common | Quad Mode | + Port A DQS | + Port A CS1 | + Port B | + Port B DQS | + Port B CS1 |
|-------------|-----------------|----------|--------|-----------|--------------|--------------|----------|--------------|--------------|
| NAND_DATA01 | qspi2.B_DATA[0] | Alt2 | — | — | — | — | Yes | — | — |
| NAND_DATA03 | qspi2.B_SS0_B | Alt2 | — | — | — | — | Yes | — | — |
| NAND_DATA02 | qspi2.B_SCLK | Alt2 | — | — | — | — | Yes | — | — |
| NAND_DATA06 | qspi2.A_SS1_B | Alt2 | — | — | — | Yes | — | — | — |
| NAND_DATA07 | qspi2.A_DQS | Alt2 | — | — | Yes | — | — | — | — |
| NAND_DATA04 | qspi2.B_SS1_B | Alt2 | — | — | — | — | — | — | Yes |
| NAND_DATA05 | qspi2.B_DQS | Alt2 | — | — | — | — | — | Yes | — |

Table 99. SPI Boot through ECSP1

| Ball Name | Signal Name | Mux Mode | Common | BOOT_CFG 4[5:4]=00b | BOOT_CFG 4[5:4]=01b | BOOT_CFG 4[5:4]=10b | BOOT_CFG 4[5:4]=11b |
|-----------------|-------------|----------|--------|---------------------|---------------------|---------------------|---------------------|
| KEY_COL1 | ecspi1.MISO | Alt 3 | Yes | — | — | — | — |
| KEY_ROW0 | ecspi1.MOSI | Alt 3 | Yes | — | — | — | — |
| KEY_COL0 (SCLK) | ecspi1.SCLK | Alt 3 | Yes | — | — | — | — |
| KEY_ROW1 | ecspi1.SS0 | Alt 3 | — | Yes | — | — | — |
| KEY_ROW3 | ecspi1.SS1 | Alt 7 | — | — | Yes | — | — |
| KEY_COL3 | ecspi1.SS2 | Alt 7 | — | — | — | Yes | — |
| KEY_ROW2 | ecspi1.SS3 | Alt 7 | — | — | — | — | Yes |

Table 100. SPI Boot through ECSP12

| Ball Name | Signal Name | Mux Mode | Common | BOOT_CFG 4[5:4]=00b | BOOT_CFG 4[5:4]=01b | BOOT_CFG 4[5:4]=10b | BOOT_CFG 4[5:4]=11b |
|-----------|-------------|----------|--------|---------------------|---------------------|---------------------|---------------------|
| SD4_CLK | ecspi2.MISO | Alt 2 | Yes | — | — | — | — |
| SD4_CMD | ecspi2.MOSI | Alt 2 | Yes | — | — | — | — |
| SD4_DATA1 | ecspi2.SCLK | Alt 2 | Yes | — | — | — | — |
| SD4_DATA0 | ecspi2.SS0 | Alt 2 | — | Yes | — | — | — |
| SD3_DATA0 | ecspi2.SS1 | Alt 2 | — | — | Yes | — | — |
| SD3_DATA1 | ecspi2.SS2 | Alt 2 | — | — | — | Yes | — |
| SD4_DATA2 | ecspi2.SS3 | Alt 6 | — | — | — | — | Yes |

Table 101. SPI Boot through ECSPi3

| Ball Name | Signal Name | Mux Mode | Common | BOOT_CFG4 [5:4]=00b | BOOT_CFG4 [5:4]=01b | BOOT_CFG4 [5:4]=10b | BOOT_CFG4 [5:4]=11b |
|-----------|-------------|----------|--------|------------------------|------------------------|------------------------|------------------------|
| SD4_DATA6 | ecspi3.MISO | Alt 3 | Yes | — | — | — | — |
| SD4_DATA5 | ecspi3.MOSI | Alt 3 | Yes | — | — | — | — |
| SD4_DATA4 | ecspi3.SCLK | Alt 3 | Yes | — | — | — | — |
| SD4_DATA7 | ecspi3.SS0 | Alt 3 | — | Yes | — | — | — |
| SD4_CMD | ecspi3.SS1 | Alt 6 | — | — | Yes | — | — |
| SD4_CLK | ecspi3.SS2 | Alt 6 | — | — | — | Yes | — |
| SD4_DATA0 | ecspi3.SS3 | Alt 6 | — | — | — | — | Yes |

Table 102. SPI Boot through ECSPi4

| Ball Name | Signal Name | Mux Mode | Common | BOOT_CFG4 [5:4]=00b | BOOT_CFG4 [5:4]=01b | BOOT_CFG4 [5:4]=10b | BOOT_CFG4 [5:4]=11b |
|-----------|-------------|----------|--------|------------------------|------------------------|------------------------|------------------------|
| SD2_DATA3 | ecspi4.MISO | Alt 3 | Yes | — | — | — | — |
| SD2_CMD | ecspi4.MOSI | Alt 3 | Yes | — | — | — | — |
| SD2_CLK | ecspi4.SCLK | Alt 3 | Yes | — | — | — | — |
| SD2_DATA2 | ecspi4.SS0 | Alt 3 | — | Yes | — | — | — |
| SD1_DATA3 | ecspi4.SS1 | Alt 6 | — | — | Yes | — | — |
| SD2_DATA1 | ecspi4.SS2 | Alt 6 | — | — | — | Yes | — |
| SD2_DATA0 | ecspi4.SS3 | Alt 6 | — | — | — | — | Yes |

Table 103. SPI Boot through ECSPi5

| Ball Name | Signal Name | Mux Mode | Common | BOOT_CFG4 [5:4]=00b | BOOT_CFG4 [5:4]=01b | BOOT_CFG4[5:4]=10b | BOOT_CFG4 [5:4]=11b |
|--------------|-------------|----------|--------|------------------------|------------------------|------------------------|------------------------|
| QSPI1A_SS1_B | ecspi5.MISO | Alt 3 | Yes | — | — | — | — |
| QSPI1A_DQS | ecspi5.MOSI | Alt 3 | Yes | — | — | — | — |
| QSPI1B_SS1_B | ecspi5.SCLK | Alt 3 | Yes | — | — | — | — |
| QSPI1B_DQS | ecspi5.SS0 | Alt 3 | — | Yes | — | — | — |
| QSPI1A_DATA2 | ecspi5.SS1 | Alt 2 | — | — | Yes | — | — |
| QSPI1A_DATA3 | ecspi5.SS2 | Alt 2 | — | — | — | Yes | — |
| QSPI1B_DATA3 | ecspi5.SS3 | Alt 2 | — | — | — | — | Yes |

Table 104. NAND Boot through GPMI

| Ball Name | Signal Name | Mux Mode | Common | BOOT_CFG1[3:2]=01b | BOOT_CFG1[3:2]=10b |
|--------------|-----------------|----------|--------|--------------------|--------------------|
| NAND_CLE | rawnand.CLE | Alt 0 | Yes | — | — |
| NAND_ALE | rawnand.ALE | Alt 0 | Yes | — | — |
| NAND_WP_B | rawnand.WP_B | Alt 0 | Yes | — | — |
| NAND_READY_B | rawnand.READY_B | Alt 0 | Yes | — | — |
| NAND_CE0_B | rawnand.CE0_B | Alt 0 | Yes | — | — |
| NAND_CE1_B | rawnand.CE1_B | Alt 0 | — | Yes | — |
| NAND_RE_B | rawnand.RE_B | Alt 0 | Yes | — | — |
| NAND_WE_B | rawnand.WE_B | Alt 0 | Yes | — | — |
| NAND_DATA00 | rawnand.DATA00 | Alt 0 | Yes | — | — |
| NAND_DATA01 | rawnand.DATA01 | Alt 0 | Yes | — | — |
| NAND_DATA02 | rawnand.DATA02 | Alt 0 | Yes | — | — |
| NAND_DATA03 | rawnand.DATA03 | Alt 0 | Yes | — | — |
| NAND_DATA04 | rawnand.DATA04 | Alt 0 | Yes | — | — |
| NAND_DATA05 | rawnand.DATA05 | Alt 0 | Yes | — | — |
| NAND_DATA06 | rawnand.DATA06 | Alt 0 | Yes | — | — |
| NAND_DATA07 | rawnand.DATA07 | Alt 0 | Yes | — | — |
| SD4_RESET_B | rawnand.DQS | Alt 1 | Yes | — | — |
| SD4_DATA5 | rawnand.CE2_B | Alt 1 | — | — | Yes |
| SD4_DATA6 | rawnand.CE3_B | Alt 1 | — | — | Yes |

Table 105. SD/MMC Boot through USDHC1

| Ball Name | Signal Name | Mux Mode | Common | 4-bit | 8-bit | BOOT_CFG1[1]=1 (SD Power Cycle or SD boot with SDR50/SDR104) | SDMMC MFG Mode |
|-------------|--------------|----------|--------|-------|-------|---|----------------------|
| GPIO1_IO02 | usdhc1.CD_B | Alt 1 | — | — | — | — | Yes |
| SD1_CLK | usdhc1.CLK | Alt 0 | Yes | — | — | — | — |
| SD1_CMD | usdhc1.CMD | Alt 0 | Yes | — | — | — | — |
| SD1_DATA0 | usdhc1.DATA0 | Alt 0 | Yes | — | — | — | — |
| SD1_DATA1 | usdhc1.DATA1 | Alt 0 | — | Yes | Yes | — | — |
| SD1_DATA2 | usdhc1.DATA2 | Alt 0 | — | Yes | Yes | — | — |
| SD1_DATA3 | usdhc1.DATA3 | Alt 0 | Yes | — | — | — | — |
| NAND_DATA00 | usdhc1.DATA4 | Alt 1 | — | — | Yes | — | — |
| NAND_DATA01 | usdhc1.DATA5 | Alt 1 | — | — | Yes | — | — |

Table 105. SD/MMC Boot through USDHC1 (continued)

| Ball Name | Signal Name | Mux Mode | Common | 4-bit | 8-bit | BOOT_CFG1[1]=1 (SD Power Cycle or SD boot with SDR50/SDR104) | SDMMC MFG Mode |
|--------------|----------------|----------|--------|-------|-------|---|----------------------|
| NAND_DATA02 | usdhc1.DATA6 | Alt 1 | — | — | Yes | — | — |
| NAND_DATA03 | usdhc1.DATA7 | Alt 1 | — | — | Yes | — | — |
| NAND_WP_B | GPIO4_15 | Alt 5 | — | — | — | Yes | — |
| NAND_READY_B | usdhc1.VSELECT | Alt 1 | — | — | — | Yes | — |

Table 106. SD/MMC Boot through USDHC2

| Ball Name | Signal Name | Mux Mode | Common | 4-bit | 8-bit | BOOT_CFG1[1]=1 (SD Power Cycle or SD boot with SDR50/SDR104) |
|-------------|----------------|----------|--------|-------|-------|---|
| SD2_CLK | usdhc2.CLK | Alt 0 | Yes | — | — | — |
| SD2_CMD | usdhc2.CMD | Alt 0 | Yes | — | — | — |
| SD2_DATA0 | usdhc2.DATA0 | Alt 0 | Yes | — | — | — |
| SD2_DATA1 | usdhc2.DATA1 | Alt 0 | — | Yes | Yes | — |
| SD2_DATA2 | usdhc2.DATA2 | Alt 0 | — | Yes | Yes | — |
| SD2_DATA3 | usdhc2.DATA3 | Alt 0 | Yes | — | — | — |
| NAND_DATA04 | usdhc2.DATA4 | Alt 1 | — | — | Yes | — |
| NAND_DATA05 | usdhc2.DATA5 | Alt 1 | — | — | Yes | — |
| NAND_DATA06 | usdhc2.DATA6 | Alt 1 | — | — | Yes | — |
| NAND_DATA07 | usdhc2.DATA7 | Alt 1 | — | — | Yes | — |
| NAND_RE_B | GPIO4_IO12 | Alt 5 | — | — | — | Yes |
| NAND_CE0_B | usdhc2.VSELECT | Alt 1 | — | — | — | Yes |

Table 107. SD/MMC Boot through USDHC3

| Ball Name | Signal Name | Mux Mode | Common | 4-bit | 8-bit | BOOT_CFG1[1]=1 (SD Power Cycle or SD boot with SDR50/SDR104) |
|-----------|--------------|----------|--------|-------|-------|---|
| SD3_CLK | usdhc3.CLK | Alt 0 | Yes | — | — | — |
| SD3_CMD | usdhc3.CMD | Alt 0 | Yes | — | — | — |
| SD3_DATA0 | usdhc3.DATA0 | Alt 0 | Yes | — | — | — |
| SD3_DATA1 | usdhc3.DATA1 | Alt 0 | — | Yes | Yes | — |
| SD3_DATA2 | usdhc3.DATA2 | Alt 0 | — | Yes | Yes | — |

Table 107. SD/MMC Boot through USDHC3 (continued)

| Ball Name | Signal Name | Mux Mode | Common | 4-bit | 8-bit | BOOT_CFG1[1]=1 (SD Power Cycle or SD boot with SDR50/SDR104) |
|-----------|--------------|----------|--------|-------|-------|---|
| SD3_DATA3 | usdhc3.DATA3 | Alt 0 | Yes | — | — | — |
| SD3_DATA4 | usdhc3.DATA4 | Alt 0 | — | — | Yes | — |
| SD3_DATA5 | usdhc3.DATA5 | Alt 0 | — | — | Yes | — |
| SD3_DATA6 | usdhc3.DATA6 | Alt 0 | — | — | Yes | — |
| SD3_DATA7 | usdhc3.DATA7 | Alt 0 | — | — | Yes | — |
| KEY_COL1 | GPIO2_IO11 | Alt 5 | — | — | — | Yes |

Table 108. SD/MMC Boot through USDHC4

| Ball Name | Signal Name | Mux Mode | Common | 4-bit | 8-bit | BOOT_CFG1[1]=1 (SD Power Cycle or SD boot with SDR50/SDR104) |
|-------------|----------------|----------|--------|-------|-------|---|
| SD4_CLK | usdhc4.CLK | Alt 0 | Yes | — | — | — |
| SD4_CMD | usdhc4.CMD | Alt 0 | Yes | — | — | — |
| SD4_DATA0 | usdhc4.DATA0 | Alt 0 | Yes | — | — | — |
| SD4_DATA1 | usdhc4.DATA1 | Alt 0 | — | Yes | Yes | — |
| SD4_DATA2 | usdhc4.DATA2 | Alt 0 | — | Yes | Yes | — |
| SD4_DATA3 | usdhc4.DATA3 | Alt 0 | Yes | — | — | — |
| SD4_DATA4 | usdhc4.DATA4 | Alt 0 | — | — | Yes | — |
| SD4_DATA5 | usdhc4.DATA5 | Alt 0 | — | — | Yes | — |
| SD4_DATA6 | usdhc4.DATA6 | Alt 0 | — | — | Yes | — |
| SD4_DATA7 | usdhc4.DATA7 | Alt 0 | — | — | Yes | — |
| SD4_RESET_B | GPIO6_IO22 | Alt 5 | — | — | — | Yes |
| KEY_ROW1 | usdhc4.VSELECT | Alt 1 | — | — | — | Yes |

Table 109. NOR/OneNAND Boot through EIM

| Ball Name | Signal Name | Mux Mode | Common | ADH16 Non-Mux | ADL16 Non-Mux | AD16 Mux |
|-------------|-------------|----------|--------|------------------|------------------|----------|
| NAND_DATA00 | weim.AD[0] | Alt 6 | Yes | — | — | — |
| NAND_DATA01 | weim.AD[1] | Alt 6 | Yes | — | — | — |
| NAND_DATA02 | weim.AD[2] | Alt 6 | Yes | — | — | — |
| NAND_DATA03 | weim.AD[3] | Alt 6 | Yes | — | — | — |
| NAND_DATA04 | weim.AD[4] | Alt 6 | Yes | — | — | — |

Table 109. NOR/OneNAND Boot through EIM (continued)

| Ball Name | Signal Name | Mux Mode | Common | ADH16 Non-Mux | ADL16 Non-Mux | AD16 Mux |
|--------------|---------------|----------|--------|---------------|---------------|----------|
| NAND_DATA05 | weim.AD[5] | Alt 6 | Yes | — | — | — |
| NAND_DATA06 | weim.AD[6] | Alt 6 | Yes | — | — | — |
| NAND_DATA07 | weim.AD[7] | Alt 6 | Yes | — | — | — |
| LCD1_DATA08 | weim.AD[8] | Alt 1 | Yes | — | — | — |
| LCD1_DATA09 | weim.AD[9] | Alt 1 | Yes | — | — | — |
| LCD1_DATA10 | weim.AD[10] | Alt 1 | Yes | — | — | — |
| LCD1_DATA11 | weim.AD[11] | Alt 1 | Yes | — | — | — |
| LCD1_DATA12 | weim.AD[12] | Alt 1 | Yes | — | — | — |
| LCD1_DATA13 | weim.AD[13] | Alt 1 | Yes | — | — | — |
| LCD1_DATA14 | weim.AD[14] | Alt 1 | Yes | — | — | — |
| LCD1_DATA15 | weim.AD[15] | Alt 1 | Yes | — | — | — |
| LCD1_DATA16 | weim.ADDR[16] | Alt 1 | — | Yes | Yes | Yes |
| LCD1_DATA17 | weim.ADDR[17] | Alt 1 | — | Yes | Yes | Yes |
| LCD1_DATA18 | weim.ADDR[18] | Alt 1 | — | Yes | Yes | Yes |
| LCD1_DATA19 | weim.ADDR[19] | Alt 1 | — | Yes | Yes | Yes |
| LCD1_DATA20 | weim.ADDR[20] | Alt 1 | — | Yes | Yes | Yes |
| LCD1_DATA21 | weim.ADDR[21] | Alt 1 | — | Yes | Yes | Yes |
| LCD1_DATA22 | weim.ADDR[22] | Alt 1 | — | Yes | Yes | Yes |
| LCD1_DATA23 | weim.ADDR[23] | Alt 1 | — | Yes | Yes | Yes |
| LCD1_DATA03 | weim.ADDR[24] | Alt 1 | — | Yes | Yes | Yes |
| LCD1_DATA04 | weim.ADDR[25] | Alt 1 | — | Yes | Yes | Yes |
| LCD1_DATA05 | weim.ADDR[26] | Alt 1 | — | Yes | Yes | Yes |
| NAND_ALE | weim.CS0_B | Alt 6 | Yes | — | — | — |
| QSPI1A_SCLK | weim.DATA[0] | Alt 6 | — | — | Yes | — |
| QSPI1A_SS0_B | weim.DATA[1] | Alt 6 | — | — | Yes | — |
| QSPI1A_SS1_B | weim.DATA[2] | Alt 6 | — | — | Yes | — |
| QSPI1A_DATA3 | weim.DATA[3] | Alt 6 | — | — | Yes | — |
| QSPI1A_DATA2 | weim.DATA[4] | Alt 6 | — | — | Yes | — |
| QSPI1A_DATA1 | weim.DATA[5] | Alt 6 | — | — | Yes | — |
| QSPI1A_DATA0 | weim.DATA[6] | Alt 6 | — | — | Yes | — |
| QSPI1A_DQS | weim.DATA[7] | Alt 6 | — | — | Yes | — |
| QSPI1B_SCLK | weim.DATA[8] | Alt 6 | — | — | Yes | — |

Table 109. NOR/OneNAND Boot through EIM (continued)

| Ball Name | Signal Name | Mux Mode | Common | ADH16 Non-Mux | ADL16 Non-Mux | AD16 Mux |
|--------------|---------------|----------|--------|---------------|---------------|----------|
| QSPI1B_SS0_B | weim.DATA[9] | Alt 6 | — | — | Yes | — |
| QSPI1B_SS1_B | weim.DATA[10] | Alt 6 | — | — | Yes | — |
| QSPI1B_DATA3 | weim.DATA[11] | Alt 6 | — | — | Yes | — |
| QSPI1B_DATA2 | weim.DATA[12] | Alt 6 | — | — | Yes | — |
| QSPI1B_DATA1 | weim.DATA[13] | Alt 6 | — | — | Yes | — |
| QSPI1B_DATA0 | weim.DATA[14] | Alt 6 | — | — | Yes | — |
| QSPI1B_DQS | weim.DATA[15] | Alt 6 | — | — | Yes | — |
| CSI_DATA07 | weim.DATA[16] | Alt 6 | — | Yes | — | — |
| CSI_DATA06 | weim.DATA[17] | Alt 6 | — | Yes | — | — |
| CSI_DATA05 | weim.DATA[18] | Alt 6 | — | Yes | — | — |
| CSI_DATA04 | weim.DATA[19] | Alt 6 | — | Yes | — | — |
| CSI_DATA03 | weim.DATA[20] | Alt 6 | — | Yes | — | — |
| CSI_DATA02 | weim.DATA[21] | Alt 6 | — | Yes | — | — |
| CSI_DATA01 | weim.DATA[22] | Alt 6 | — | Yes | — | — |
| CSI_DATA00 | weim.DATA[23] | Alt 6 | — | Yes | — | — |
| CSI_VSYNC | weim.DATA[24] | Alt 6 | — | Yes | — | — |
| CSI_HSYNC | weim.DATA[25] | Alt 6 | — | Yes | — | — |
| CSI_MCLK | weim.DATA[26] | Alt 6 | — | Yes | — | — |
| CSI_PIXCLK | weim.DATA[27] | Alt 6 | — | Yes | — | — |
| KEY_COL3 | weim.DATA[28] | Alt 6 | — | Yes | — | — |
| KEY_ROW2 | weim.DATA[29] | Alt 6 | — | Yes | — | — |
| KEY_COL2 | weim.DATA[30] | Alt 6 | — | Yes | — | — |
| KEY_ROW1 | weim.DATA[31] | Alt 6 | — | Yes | — | — |
| NAND_WP_B | weim.EB_B[0] | Alt 6 | — | — | Yes | Yes |
| NAND_READY_B | weim.EB_B[1] | Alt 6 | — | — | Yes | Yes |
| LCD1_DATA06 | weim.EB_B[2] | Alt 1 | — | Yes | — | — |
| LCD1_DATA07 | weim.EB_B[3] | Alt 1 | — | Yes | — | — |
| NAND_CE0_B | weim.LBA_B | Alt 6 | Yes | — | — | — |
| NAND_CE1_B | weim.OE | Alt 6 | Yes | — | — | — |
| NAND_RE_B | weim.RW | Alt 6 | Yes | — | — | — |

6 Package Information and Contact Assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 i.MX 6SoloX Signal Availability by Package

The i.MX 6SoloX is available in multiple packages. Not all signals are available in all packages. [Table 110](#) summarizes the signal differences and their implications. Signals available on all packages are not shown in this table. This table only shows signals impacted that are not available through another IOMUX option.

Table 110. i.MX 6SoloX Signal Availability by Package

| Affected Module | Package | | | | SoC Capability Implication |
|-----------------|-----------------|----------------------------|---------------------------------|---------------|--|
| | 19x19 mm [VM] | 17x17 mm NP (no PCIe) [VO] | 17x17 mm WP (with PCIe) [VN] | 14x14 mm [VK] | |
| ADC | ADC1_IN0 | ADC1_IN0 | ADC1_IN0 | ADC1_IN0 | — |
| | ADC1_IN1 | ADC1_IN1 | ADC1_IN1 | ADC1_IN1 | — |
| | ADC1_IN2 | ADC1_IN2 | — | ADC1_IN2 | — |
| | ADC1_IN3 | ADC1_IN3 | — | ADC1_IN3 | — |
| | ADC2_IN0 | ADC2_IN0 | — | ADC2_IN0 | — |
| | ADC2_IN1 | ADC2_IN1 | — | ADC2_IN1 | — |
| | ADC2_IN2 | ADC2_IN2 | — | ADC2_IN2 | — |
| | ADC2_IN3 | ADC2_IN3 | — | ADC2_IN3 | — |
| | ADC_VREFL | ADC_VREFL | Tied internally to VSS | ADC_VREFL | 17x17NP low reference voltage is not controllable. |
| | ADC_VREFH | ADC_VREFH | Tied internally to VDDA_ADC_3P3 | ADC_VREFH | 17x17NP high reference voltage is not controllable. |
| ECSPI4 | ECSPI4_RDY | — | — | — | Master mode flow control cannot be used without ECSPI4_RDY |
| EIM | EIM_DATA[27:16] | — | — | — | Reduced EIM throughput on the smaller packages |
| ENET1 | 1588_EVENT1_IN | — | — | — | — |
| | 1588_EVENT1_OUT | — | — | — | — |
| ENET2 | 1588_EVENT1_IN | — | — | — | — |
| | 1588_EVENT1_OUT | — | — | — | — |

Table 110. i.MX 6SoloX Signal Availability by Package (continued)

| Affected Module | Package | | | | SoC Capability Implication |
|-----------------|---------------|----------------------------|------------------------------|---------------|----------------------------|
| | 19x19 mm [VM] | 17x17 mm NP (no PCIe) [VO] | 17x17 mm WP (with PCIe) [VN] | 14x14 mm [VK] | |
| GPIO | GPIO1_IO[21] | — | — | — | — |
| | GPIO1_IO[20] | — | — | — | — |
| | GPIO1_IO[19] | — | — | — | — |
| | GPIO1_IO[18] | — | — | — | — |
| | GPIO1_IO[17] | — | — | — | — |
| | GPIO1_IO[16] | — | — | — | — |
| | GPIO1_IO[15] | — | — | — | — |
| | GPIO1_IO[14] | — | — | — | — |
| | GPIO1_IO[25] | — | — | — | — |
| | GPIO1_IO[22] | — | — | — | — |
| | GPIO1_IO[23] | — | — | — | — |
| | GPIO1_IO[24] | — | — | — | — |
| | GPIO6_IO[2] | — | — | — | — |
| | GPIO6_IO[3] | — | — | — | — |
| | GPIO6_IO[1] | — | — | — | — |
| | GPIO6_IO[0] | — | — | — | — |
| | GPIO6_IO[4] | — | — | — | — |
| | GPIO6_IO[5] | — | — | — | — |
| GPT | GPT_CAPTURE1 | — | — | — | — |
| | GPT_CAPTURE2 | — | — | — | — |
| | GPT_COMPARE1 | — | — | — | — |
| | GPT_CLK | — | — | — | — |
| | GPT_COMPARE2 | — | — | — | — |
| | GPT_COMPARE3 | — | — | — | — |
| | GPT_CAPTURE1 | — | — | — | — |
| LVDS I/F | LVDS_CLK_N | — | — | — | — |
| | LVDS_CLK_P | — | — | — | — |
| | LVDS_DATA0_N | — | — | — | — |
| | LVDS_DATA0_P | — | — | — | — |
| | LVDS_DATA1_N | — | — | — | — |
| | LVDS_DATA1_P | — | — | — | — |
| | LVDS_DATA2_N | — | — | — | — |
| | LVDS_DATA2_P | — | — | — | — |
| | LVDS_DATA3_N | — | — | — | — |
| | LVDS_DATA3_P | — | — | — | — |
| | LVDS_CLK_N | — | — | — | — |

Table 110. i.MX 6SoloX Signal Availability by Package (continued)

| Affected Module | Package | | | | SoC Capability Implication |
|-----------------|---------------|----------------------------|------------------------------|---------------|---|
| | 19x19 mm [VM] | 17x17 mm NP (no PCIe) [VO] | 17x17 mm WP (with PCIe) [VN] | 14x14 mm [VK] | |
| MMDC | DRAM_ADDR15 | — | — | — | Address space is limited to 2GB on the smaller packages vs.4 GB on the 19x19 package. |
| PCIe | PCIe_REXT | — | PCIe_REXT | — | — |
| | PCIe_RX_N | — | PCIe_RX_N | — | — |
| | PCIe_RX_P | — | PCIe_RX_P | — | — |
| | PCIe_TX_N | — | PCIe_TX_N | — | — |
| | PCIe_TX_P | — | PCIe_TX_P | — | — |
| | PCIe_VP | — | PCIe_VP | — | — |
| | — | PCIe_VP_CAP | — | PCIe_VP_CAP | — |
| | PCIe_VPH | — | PCIe_VPH | — | — |
| | PCIe_VPTX | — | PCIe_VPTX | — | — |
| UART6 | UART6_DCD_B | — | — | — | — |
| | UART6_DTR_B | — | — | — | — |
| | UART6_DSR_B | — | — | — | — |
| | UART6_RI_B | — | — | — | — |
| uSDHC1 | SD1_DATA0 | — | — | — | Entire interface not available on the smaller packages |
| | SD1_DATA1 | — | — | — | — |
| | SD1_CMD | — | — | — | — |
| | SD1_CLK | — | — | — | — |
| | SD1_DATA2 | — | — | — | — |
| | SD1_DATA3 | — | — | — | — |

6.2 Signals with Different States During Reset and After Reset

For most of the signals, the state during reset is the same as the state after reset as listed in the “Out of Reset Condition” column of the Functional Contact Assignment tables for the various packages (Table 113, Table 117, Table 120, and Table 123). However, there are a few signals for which the state during reset is different from the state after reset. These signals along with their state during reset are given in Table 111.

Table 111. Signals with Different States During Reset and After Reset

| Ball Name | State During Reset (POR_B Asserted) | |
|------------|-------------------------------------|---|
| | Input/Output | Value |
| GPIO1_IO06 | Output | Drive state unknown. This signal should not be used for system functions that will require it to be an input or stable output during reset. |
| GPIO1_IO09 | Output | Drive state unknown. This signal should not be used for system functions that will require it to be an input or stable output during reset. |

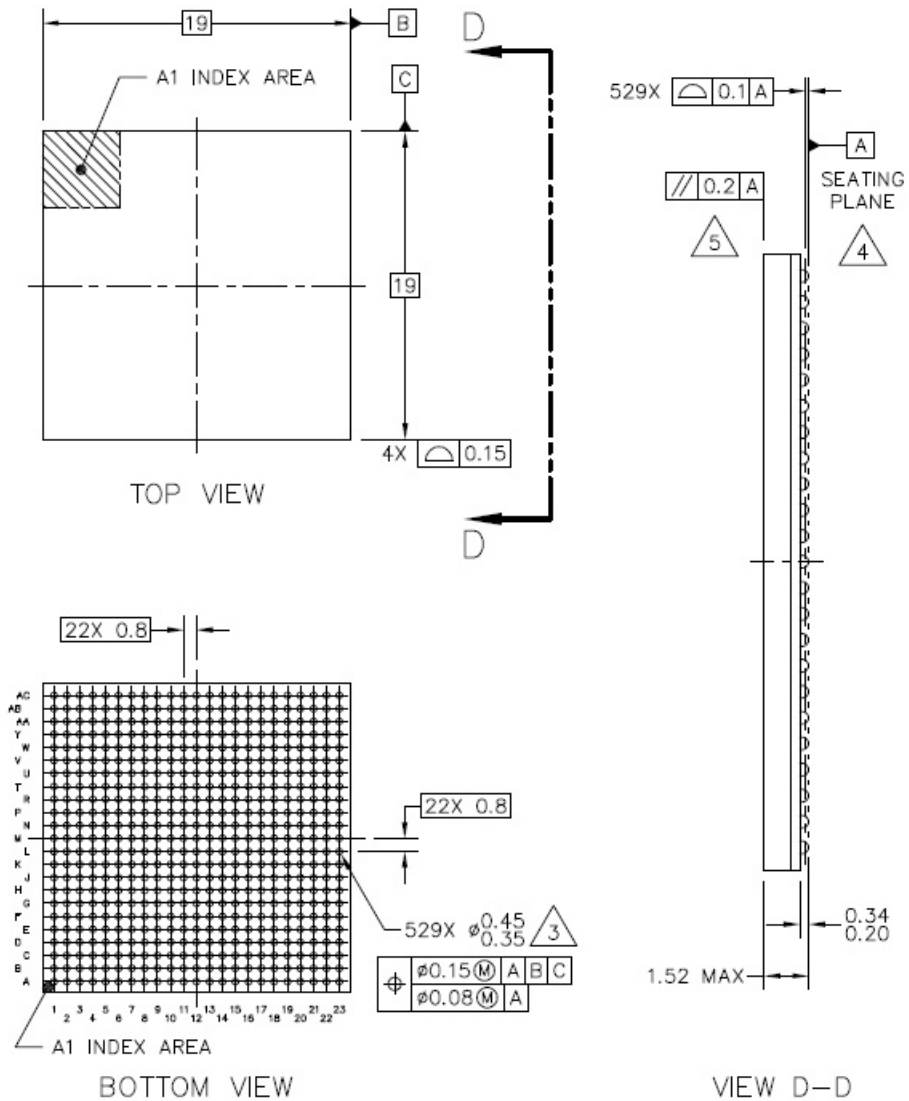
Table 111. Signals with Different States During Reset and After Reset (continued)

| Ball Name | State During Reset (POR_B Asserted) | |
|-------------|-------------------------------------|---|
| | Input/Output | Value |
| RGMI2_TD3 | Output | Drive state unknown. This signal should not be used for system functions that will require it to be an input or stable output during reset. |
| LCD1_DATA00 | Input | BT_CFG[0] with 100K Pull Down |
| LCD1_DATA01 | Input | BT_CFG[1] with 100K Pull Down |
| LCD1_DATA02 | Input | BT_CFG[2] with 100K Pull Down |
| LCD1_DATA03 | Input | BT_CFG[3] with 100K Pull Down |
| LCD1_DATA04 | Input | BT_CFG[4] with 100K Pull Down |
| LCD1_DATA05 | Input | BT_CFG[5] with 100K Pull Down |
| LCD1_DATA06 | Input | BT_CFG[6] with 100K Pull Down |
| LCD1_DATA07 | Input | BT_CFG[7] with 100K Pull Down |
| LCD1_DATA08 | Input | BT_CFG[8] with 100K Pull Down |
| LCD1_DATA09 | Input | BT_CFG[9] with 100K Pull Down |
| LCD1_DATA10 | Input | BT_CFG[10] with 100K Pull Down |
| LCD1_DATA11 | Input | BT_CFG[11] with 100K Pull Down |
| LCD1_DATA12 | Input | BT_CFG[12] with 100K Pull Down |
| LCD1_DATA13 | Input | BT_CFG[13] with 100K Pull Down |
| LCD1_DATA14 | Input | BT_CFG[14] with 100K Pull Down |
| LCD1_DATA15 | Input | BT_CFG[15] with 100K Pull Down |
| LCD1_DATA16 | Input | BT_CFG[24] with 100K Pull Down |
| LCD1_DATA17 | Input | BT_CFG[25] with 100K Pull Down |
| LCD1_DATA18 | Input | BT_CFG[26] with 100K Pull Down |
| LCD1_DATA19 | Input | BT_CFG[27] with 100K Pull Down |
| LCD1_DATA20 | Input | BT_CFG[28] with 100K Pull Down |
| LCD1_DATA21 | Input | BT_CFG[29] with 100K Pull Down |
| LCD1_DATA22 | Input | BT_CFG[30] with 100K Pull Down |
| LCD1_DATA23 | Input | BT_CFG[31] with 100K Pull Down |

6.3 19x19 mm Package Information

6.3.1 19x19 mm, 0.8 mm Pitch, 23x23 Ball Matrix

Figure 84 shows the top, bottom, and side views of the 19x19 mm BGA package.



| | | |
|--|-------------------------------|----------------------------|
| © NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |
| TITLE: MAPBGA, 19 X 19 X 1.37 PKG, 0.8 MM PITCH, 529 I/O | DOCUMENT NO: 98ASA00646D | REV: B |
| | STANDARD: JEDEC MO-275 PPAC-1 | |
| | SOT1526-1 | 12 JAN 2016 |

Figure 84. 19x19 mm BGA Package—Top, Bottom, and Side Views



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

| | | |
|---|-------------------------------|----------------------------|
| © NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |
| TITLE: MAPBGA, 19 X 19 X 1.37 PKG, 0.8 MM PITCH, 529 I/O | DOCUMENT NO: 98ASA00646D | REV: B |
| | STANDARD: JEDEC MO-275 PPAC-1 | |
| | SOT1526-1 | 12 JAN 2016 |

Figure 85. 19x19 mm BGA Package Notes

6.3.2 19x19 mm Supplies Contact Assignments and Functional Contact Assignments

Table 112 shows supplies contact assignments for the 19x19 mm package.

Table 112. 19x19 mm Supplies Contact Assignments

| Supply Rail Name | 19x19 Ball(s) Position(s) | Remark |
|------------------|--|---|
| ADC_VREFH | AA16 | ADC high reference voltage |
| ADC_VREFL | U16 | ADC low reference voltage |
| DRAM_VREF | M3 | DDR voltage reference input. Connect to a voltage source that is 50% of NVCC_DRAM. |
| DRAM_ZQPAD | C4 | DDR output buffer driver calibration reference voltage input. Connect DRAM_ZQPAD to an external 240 ohm 1% resistor to Vss. |
| GPANAIO | V18 | Analog output for NXP use only. This output must always be left unconnected. |
| NGND_KEL0 | R16 | Connect to Vss |
| NVCC_CSI | P18 | Supply input for the CSI interface |
| NVCC_DRAM | F5, G5, H5, J5, K5, L5, M5, N5, P5, R5, T5, U5, V5 | Supply input for the DDR I/O interface |
| NVCC_DRAM_2P5 | M6 | Supply input for the DDR interface |
| NVCC_ENET | F6 | Supply input for the ENET interfaces |
| NVCC_GPIO | G15 | Supply input for the GPIO interface |
| NVCC_HIGH | U12 | 3.3 V Supply input for the dual-voltage I/Os on the SD3 interface |
| NVCC_JTAG | U11 | Supply input for the JTAG interface |
| NVCC_KEY | G16 | Supply input for the Key Pad Port (KPP) interface |
| NVCC_LCD1 | G17 | Supply input for the LCD interface |
| NVCC_LOW | V11 | 1.8 V Supply input for the dual-voltage IOs on the SD3 interface |
| NVCC_LVDS | T18 | Supply input for the LVDS interface |
| NVCC_NAND | U8 | Supply input for the Raw NAND flash memories interface |
| NVCC_PLL | Y23 | Supply input for the PLLs |
| NVCC_QSPI | G14 | Supply input for the QSPI interface |
| NVCC_RGMII1 | F8 | Supply input for the RGMII1 interface |
| NVCC_RGMII2 | G9 | Supply input for the RGMII2 interface |
| NVCC_SD1 | G12 | Supply input for the SD1 interface |
| NVCC_SD2 | G11 | Supply input for the SD2 interface |
| NVCC_SD4 | U10 | Supply input for the SD4 interface |
| NVCC_USB_H | AA6 | Supply input for the USB HSIC interface |
| PCIE_REXT | M21 | PCIe impedance calibration resistor. Connect PCIE_REXT to an external 200 ohm 1% resistor to Vss. |
| PCIE_VP | L18 | Supply input for the PCIe PHY |
| PCIE_VPH | R18 | Supply input for the PCIe PHY |

Table 112. 19x19 mm Supplies Contact Assignments (continued)

| Supply Rail Name | 19x19 Ball(s) Position(s) | Remark |
|------------------|---|--|
| PCIE_VPTX | M18 | Supply input for the PCIe PHY |
| RSVD | E5 | Reserved. Do not connect. |
| USB_OTG1_VBUS | W20 | VBUS input for USB_OTG1 |
| USB_OTG2_VBUS | Y18 | VBUS input for USB_OTG2 |
| Reserved | K21 | Reserved. Leave unconnected. |
| Reserved | L21 | Reserved. Connect to ground through a 10 kΩ resistor. |
| Reserved | N18 | Reserved. Connect to ground through a 10 kΩ resistor. |
| VDD_ARM_CAP | C18, J12, J13, J14, J15, J16, K16, L16, M16 | Supply voltage output from internal LDO_ARM. Requires external capacitor(s). |
| VDD_ARM_IN | K12, K13, K14, K15, J21, L15, M15 | Supply voltage input for internal LDO_ARM. |
| VDD_HIGH_CAP | U17, U18 | Supply voltage output from internal LDO_2P5. Requires external capacitor(s). |
| VDD_HIGH_IN | U14, U15 | Supply voltage input to internal LDO_2P5, LDO_1P1 and LDO_SNVS. |
| VDD_SNVS_CAP | Y22 | Supply voltage output from internal LDO_SNVS. Requires external capacitor(s). |
| VDD_SNVS_IN | V15 | Supply voltage input to the SNVS voltage domain |
| VDD_SOC_CAP | J7, J8, J9, J10, J11, K7, L7, M7, N7, N16, P7, P16, R7, R8, R9, R10, R11, R12, R13, R14, R15, Y10, AA10 | Supply voltage output from internal LDO_SOC. Requires external capacitor(s). |
| VDD_SOC_IN | C9, K8, K9, K10, K11, L8, M8, N8, N15, P8, P9, P10, P11, P12, P13, P14, P15 | Supply voltage input to internal LDO_SOC and LDO_PCIE |
| VDD_USB_CAP | AA17 | Supply voltage output from internal LDO_USB. Requires external capacitor(s). |
| VDDA_ADC_3P3 | U13 | Supply voltage input to the ADC. This supply must be provided even if the ADC is not used. |
| VSS | A1, A6, A23, B3, B6, C2, C3, C5, D7, D9, D11, D13, D15, D17, D19, F2, F3, F20, G6, G7, G8, H6, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, H17, J2, J3, J6, J17, J20, K6, K17, L2, L3, L6, L9, L10, L11, L12, L13, L14, L17, M9, M10, M11, M12, M13, M14, M17, M20, M22, M23, N2, N3, N6, N9, N10, N11, N12, N13, N14, N17, P6, P17, R2, R3, R6, R17, R20, R21, R22, R23, T6, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, T17, U6, U7, U20, U21, V2, V3, V8, V9, W19, W21, W22, W23, Y7, Y11, Y13, Y15, Y17, Y20, AA2, AA3, AA5, AA18, AA20, AB3, AB6, AB19, AB21, AB23, AC1, AC6, AC19, AC21, AC23 | Ground |

Table 113 shows an alpha-sorted list of functional contact assignments for the 19x19 mm package.

Table 113. 19x19 mm Functional Contact Assignments

| Ball Name | 19x19 Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|-------------------|------------|--------------|-----------|------------------------|-------------------|--------------|--------------------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| ADC1_IN0 | AC15 | VDDA_ADC_3P3 | — | — | ADC1_IN0 | Input | — |
| ADC1_IN1 | AB15 | VDDA_ADC_3P3 | — | — | ADC1_IN1 | Input | — |
| ADC1_IN2 | AC16 | VDDA_ADC_3P3 | — | — | ADC1_IN2 | Input | — |
| ADC1_IN3 | AB16 | VDDA_ADC_3P3 | — | — | ADC1_IN3 | Input | — |
| ADC2_IN0 | AC17 | VDDA_ADC_3P3 | — | — | ADC2_IN0 | Input | — |
| ADC2_IN1 | AB17 | VDDA_ADC_3P3 | — | — | ADC2_IN1 | Input | — |
| ADC2_IN2 | AC18 | VDDA_ADC_3P3 | — | — | ADC2_IN2 | Input | — |
| ADC2_IN3 | AB18 | VDDA_ADC_3P3 | — | — | ADC2_IN3 | Input | — |
| BOOT_MODE0 | W14 | VDD_SNVS_IN | GPIO | — | BOOT_MODE0 | Input | 100 k Ω pull-down |
| BOOT_MODE1 | W15 | VDD_SNVS_IN | GPIO | — | BOOT_MODE1 | Input | 100 k Ω pull-down |
| CCM_CLK1_N | AA22 | VDD_HIGH_CAP | — | — | CCM_CLK1_N | — | — |
| CCM_CLK1_P | AA23 | VDD_HIGH_CAP | — | — | CCM_CLK1_P | — | — |
| CCM_CLK2 | W18 | VDD_HIGH_CAP | — | — | CCM_CLK2 | — | — |
| CCM_PMIC_STBY_REQ | V16 | VDD_SNVS_IN | GPIO | — | CCM_PMIC_STBY_REQ | Output | 0 |
| CSI_DATA00 | P21 | NVCC_CSI | GPIO | ALT5 | GPIO1_IO14 | Input | Keeper |
| CSI_DATA01 | P20 | NVCC_CSI | GPIO | ALT5 | GPIO1_IO15 | Input | Keeper |
| CSI_DATA02 | P19 | NVCC_CSI | GPIO | ALT5 | GPIO1_IO16 | Input | Keeper |
| CSI_DATA03 | N21 | NVCC_CSI | GPIO | ALT5 | GPIO1_IO17 | Input | Keeper |
| CSI_DATA04 | N19 | NVCC_CSI | GPIO | ALT5 | GPIO1_IO18 | Input | Keeper |
| CSI_DATA05 | N20 | NVCC_CSI | GPIO | ALT5 | GPIO1_IO19 | Input | Keeper |
| CSI_DATA06 | M19 | NVCC_CSI | GPIO | ALT5 | GPIO1_IO20 | Input | Keeper |
| CSI_DATA07 | L19 | NVCC_CSI | GPIO | ALT5 | GPIO1_IO21 | Input | Keeper |
| CSI_HSYNC | L20 | NVCC_CSI | GPIO | ALT5 | GPIO1_IO22 | Input | Keeper |
| CSI_MCLK | R19 | NVCC_CSI | GPIO | ALT5 | GPIO1_IO23 | Input | Keeper |
| CSI_PIXCLK | T19 | NVCC_CSI | GPIO | ALT5 | GPIO1_IO24 | Input | Keeper |
| CSI_VSYNC | U19 | NVCC_CSI | GPIO | ALT5 | GPIO1_IO25 | Input | Keeper |
| DRAM_ADDR00 | N4 | NVCC_DRAM | DDR | — | DRAM_ADDR00 | Output | 100 k Ω pull-up |
| DRAM_ADDR01 | Y4 | NVCC_DRAM | DDR | — | DRAM_ADDR01 | Output | 100 k Ω pull-up |

Table 113. 19x19 mm Functional Contact Assignments (continued)

| Ball Name | 19x19 Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|-------------|------------|-------------|-----------|------------------------|------------------|--------------|----------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| DRAM_ADDR02 | G4 | NVCC_DRAM | DDR | — | DRAM_ADDR02 | Output | 100 kΩ pull-up |
| DRAM_ADDR03 | H3 | NVCC_DRAM | DDR | — | DRAM_ADDR03 | Output | 100 kΩ pull-up |
| DRAM_ADDR04 | R4 | NVCC_DRAM | DDR | — | DRAM_ADDR04 | Output | 100 kΩ pull-up |
| DRAM_ADDR05 | G3 | NVCC_DRAM | DDR | — | DRAM_ADDR05 | Output | 100 kΩ pull-up |
| DRAM_ADDR06 | Y3 | NVCC_DRAM | DDR | — | DRAM_ADDR06 | Output | 100 kΩ pull-up |
| DRAM_ADDR07 | F4 | NVCC_DRAM | DDR | — | DRAM_ADDR07 | Output | 100 kΩ pull-up |
| DRAM_ADDR08 | T3 | NVCC_DRAM | DDR | — | DRAM_ADDR08 | Output | 100 kΩ pull-up |
| DRAM_ADDR09 | P3 | NVCC_DRAM | DDR | — | DRAM_ADDR09 | Output | 100 kΩ pull-up |
| DRAM_ADDR10 | U4 | NVCC_DRAM | DDR | — | DRAM_ADDR10 | Output | 100 kΩ pull-up |
| DRAM_ADDR11 | T4 | NVCC_DRAM | DDR | — | DRAM_ADDR11 | Output | 100 kΩ pull-up |
| DRAM_ADDR12 | W3 | NVCC_DRAM | DDR | — | DRAM_ADDR12 | Output | 100 kΩ pull-up |
| DRAM_ADDR13 | P4 | NVCC_DRAM | DDR | — | DRAM_ADDR13 | Output | 100 kΩ pull-up |
| DRAM_ADDR14 | W4 | NVCC_DRAM | DDR | — | DRAM_ADDR14 | Output | 100 kΩ pull-up |
| DRAM_ADDR15 | E4 | NVCC_DRAM | DDR | — | DRAM_ADDR15 | Output | 100 kΩ pull-up |
| DRAM_CAS_B | K4 | NVCC_DRAM | DDR | — | DRAM_CAS_B | Output | 100 kΩ pull-up |
| DRAM_CS0_B | J4 | NVCC_DRAM | DDR | — | DRAM_CS0_B | Output | 100 kΩ pull-up |
| DRAM_CS1_B | D3 | NVCC_DRAM | DDR | — | DRAM_CS1_B | Output | 100 kΩ pull-up |
| DRAM_DATA00 | U2 | NVCC_DRAM | DDR | — | DRAM_DATA00 | Input | 100 kΩ pull-up |
| DRAM_DATA01 | W2 | NVCC_DRAM | DDR | — | DRAM_DATA01 | Input | 100 kΩ pull-up |
| DRAM_DATA02 | V1 | NVCC_DRAM | DDR | — | DRAM_DATA02 | Input | 100 kΩ pull-up |

Table 113. 19x19 mm Functional Contact Assignments (continued)

| Ball Name | 19x19 Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|-------------|------------|-------------|-----------|------------------------|------------------|--------------|----------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| DRAM_DATA03 | W1 | NVCC_DRAM | DDR | — | DRAM_DATA03 | Input | 100 kΩ pull-up |
| DRAM_DATA04 | P1 | NVCC_DRAM | DDR | — | DRAM_DATA04 | Input | 100 kΩ pull-up |
| DRAM_DATA05 | N1 | NVCC_DRAM | DDR | — | DRAM_DATA05 | Input | 100 kΩ pull-up |
| DRAM_DATA06 | R1 | NVCC_DRAM | DDR | — | DRAM_DATA06 | Input | 100 kΩ pull-up |
| DRAM_DATA07 | P2 | NVCC_DRAM | DDR | — | DRAM_DATA07 | Input | 100 kΩ pull-up |
| DRAM_DATA08 | J1 | NVCC_DRAM | DDR | — | DRAM_DATA08 | Input | 100 kΩ pull-up |
| DRAM_DATA09 | L1 | NVCC_DRAM | DDR | — | DRAM_DATA09 | Input | 100 kΩ pull-up |
| DRAM_DATA10 | K2 | NVCC_DRAM | DDR | — | DRAM_DATA10 | Input | 100 kΩ pull-up |
| DRAM_DATA11 | G2 | NVCC_DRAM | DDR | — | DRAM_DATA11 | Input | 100 kΩ pull-up |
| DRAM_DATA12 | K1 | NVCC_DRAM | DDR | — | DRAM_DATA12 | Input | 100 kΩ pull-up |
| DRAM_DATA13 | F1 | NVCC_DRAM | DDR | — | DRAM_DATA13 | Input | 100 kΩ pull-up |
| DRAM_DATA14 | E2 | NVCC_DRAM | DDR | — | DRAM_DATA14 | Input | 100 kΩ pull-up |
| DRAM_DATA15 | E1 | NVCC_DRAM | DDR | — | DRAM_DATA15 | Input | 100 kΩ pull-up |
| DRAM_DATA16 | AB1 | NVCC_DRAM | DDR | — | DRAM_DATA16 | Input | 100 kΩ pull-up |
| DRAM_DATA17 | AB5 | NVCC_DRAM | DDR | — | DRAM_DATA17 | Input | 100 kΩ pull-up |
| DRAM_DATA18 | AC5 | NVCC_DRAM | DDR | — | DRAM_DATA18 | Input | 100 kΩ pull-up |
| DRAM_DATA19 | AB4 | NVCC_DRAM | DDR | — | DRAM_DATA19 | Input | 100 kΩ pull-up |
| DRAM_DATA20 | Y2 | NVCC_DRAM | DDR | — | DRAM_DATA20 | Input | 100 kΩ pull-up |
| DRAM_DATA21 | AC3 | NVCC_DRAM | DDR | — | DRAM_DATA21 | Input | 100 kΩ pull-up |
| DRAM_DATA22 | AA1 | NVCC_DRAM | DDR | — | DRAM_DATA22 | Input | 100 kΩ pull-up |

Table 113. 19x19 mm Functional Contact Assignments (continued)

| Ball Name | 19x19 Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|-------------|------------|-------------|-----------|------------------------|------------------|--------------|------------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| DRAM_DATA23 | Y1 | NVCC_DRAM | DDR | — | DRAM_DATA23 | Input | 100 kΩ pull-up |
| DRAM_DATA24 | B4 | NVCC_DRAM | DDR | — | DRAM_DATA24 | Input | 100 kΩ pull-up |
| DRAM_DATA25 | D1 | NVCC_DRAM | DDR | — | DRAM_DATA25 | Input | 100 kΩ pull-up |
| DRAM_DATA26 | B2 | NVCC_DRAM | DDR | — | DRAM_DATA26 | Input | 100 kΩ pull-up |
| DRAM_DATA27 | D2 | NVCC_DRAM | DDR | — | DRAM_DATA27 | Input | 100 kΩ pull-up |
| DRAM_DATA28 | B1 | NVCC_DRAM | DDR | — | DRAM_DATA28 | Input | 100 kΩ pull-up |
| DRAM_DATA29 | A4 | NVCC_DRAM | DDR | — | DRAM_DATA29 | Input | 100 kΩ pull-up |
| DRAM_DATA30 | B5 | NVCC_DRAM | DDR | — | DRAM_DATA30 | Input | 100 kΩ pull-up |
| DRAM_DATA31 | A5 | NVCC_DRAM | DDR | — | DRAM_DATA31 | Input | 100 kΩ pull-up |
| DRAM_DQM0 | T2 | NVCC_DRAM | DDR | — | DRAM_DQM0 | Output | 100 kΩ pull-up |
| DRAM_DQM1 | G1 | NVCC_DRAM | DDR | — | DRAM_DQM1 | Output | 100 kΩ pull-up |
| DRAM_DQM2 | AC4 | NVCC_DRAM | DDR | — | DRAM_DQM2 | Output | 100 kΩ pull-up |
| DRAM_DQM3 | C1 | NVCC_DRAM | DDR | — | DRAM_DQM3 | Output | 100 kΩ pull-up |
| DRAM_ODT0 | AA4 | NVCC_DRAM | DDR | — | DRAM_ODT0 | Output | 100 kΩ pull-down |
| DRAM_RAS_B | L4 | NVCC_DRAM | DDR | — | DRAM_RAS_B | Output | 100 kΩ pull-up |
| DRAM_RESET | D4 | NVCC_DRAM | DDR | — | DRAM_RESET | Output | 100 kΩ pull-down |
| DRAM_SDBA0 | H4 | NVCC_DRAM | DDR | — | DRAM_SDBA0 | Output | 100 kΩ pull-up |
| DRAM_SDBA1 | U3 | NVCC_DRAM | DDR | — | DRAM_SDBA1 | Output | 100 kΩ pull-up |
| DRAM_SDBA2 | M4 | NVCC_DRAM | DDR | — | DRAM_SDBA2 | Output | 100 kΩ pull-up |
| DRAM_SDCKE0 | V4 | NVCC_DRAM | DDR | — | DRAM_SDCKE0 | Output | 100 kΩ pull-down |

Table 113. 19x19 mm Functional Contact Assignments (continued)

| Ball Name | 19x19 Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|---------------|------------|-------------|-----------|------------------------|------------------|--------------|------------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| DRAM_SDCKE1 | E3 | NVCC_DRAM | DDR | — | DRAM_SDCKE1 | Output | 100 kΩ pull-down |
| DRAM_SDCLK0_N | M1 | NVCC_DRAM | DDRCLK | — | DRAM_SDCLK0_N | — | — |
| DRAM_SDCLK0_P | M2 | NVCC_DRAM | DDRCLK | — | DRAM_SDCLK0_P | Output | Low |
| DRAM_SDQS0_N | U1 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS0_N | — | — |
| DRAM_SDQS0_P | T1 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS0_P | Input | — |
| DRAM_SDQS1_N | H2 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS1_N | — | — |
| DRAM_SDQS1_P | H1 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS1_P | Input | — |
| DRAM_SDQS2_N | AC2 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS2_N | — | — |
| DRAM_SDQS2_P | AB2 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS2_P | Input | — |
| DRAM_SDQS3_N | A2 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS3_N | — | — |
| DRAM_SDQS3_P | A3 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS3_P | Input | — |
| DRAM_SDWE_B | K3 | NVCC_DRAM | DDR | — | DRAM_SDWE_B | Output | 100 kΩ pull-up |
| ENET1_COL | E6 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO00 | Input | Keeper |
| ENET1_CRS | C7 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO01 | Input | Keeper |
| ENET1_MDC | F9 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO02 | Input | Keeper |
| ENET1_MDIO | E7 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO03 | Input | Keeper |
| ENET1_RX_CLK | B7 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO04 | Input | Keeper |
| ENET1_TX_CLK | A7 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO05 | Input | Keeper |
| ENET2_COL | F7 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO06 | Input | Keeper |
| ENET2_CRS | D6 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO07 | Input | Keeper |
| ENET2_RX_CLK | D5 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO08 | Input | Keeper |
| ENET2_TX_CLK | C6 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO09 | Input | Keeper |
| GPIO1_IO00 | A20 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO00 | Input | Keeper |
| GPIO1_IO01 | B20 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO01 | Input | Keeper |
| GPIO1_IO02 | C20 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO02 | Input | Keeper |
| GPIO1_IO03 | D20 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO03 | Input | Keeper |
| GPIO1_IO04 | A19 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO04 | Input | Keeper |
| GPIO1_IO05 | B19 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO05 | Input | Keeper |
| GPIO1_IO06 | C19 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO06 | Input | Keeper |
| GPIO1_IO07 | A18 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO07 | Input | Keeper |
| GPIO1_IO08 | B18 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO08 | Input | Keeper |
| GPIO1_IO09 | D18 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO09 | Input | Keeper |

Table 113. 19x19 mm Functional Contact Assignments (continued)

| Ball Name | 19x19 Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|-------------|------------|-------------|-----------|------------------------|------------------|--------------|----------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| GPIO1_IO10 | E19 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO10 | Input | Keeper |
| GPIO1_IO11 | E18 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO11 | Input | Keeper |
| GPIO1_IO12 | A17 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO12 | Input | Keeper |
| GPIO1_IO13 | B17 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO13 | Input | Keeper |
| JTAG_MOD | U9 | NVCC_JTAG | GPIO | — | JTAG_MOD | Input | 100 kΩ pull-up |
| JTAG_TCK | V10 | NVCC_JTAG | GPIO | — | JTAG_TCK | Input | 47 kΩ pull-up |
| JTAG_TDI | V12 | NVCC_JTAG | GPIO | — | JTAG_TDI | Input | 47 kΩ pull-up |
| JTAG_TDO | W9 | NVCC_JTAG | GPIO | — | JTAG_TDO | Output | Keeper |
| JTAG_TMS | W12 | NVCC_JTAG | GPIO | — | JTAG_TMS | Input | 47 kΩ pull-up |
| JTAG_TRST_B | V13 | NVCC_JTAG | GPIO | — | JTAG_TRST_B | Input | 47 kΩ pull-up |
| KEY_COL0 | C23 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO10 | Input | Keeper |
| KEY_COL1 | C22 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO11 | Input | Keeper |
| KEY_COL2 | B23 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO12 | Input | Keeper |
| KEY_COL3 | B22 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO13 | Input | Keeper |
| KEY_COL4 | A22 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO14 | Input | Keeper |
| KEY_ROW0 | A21 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO15 | Input | Keeper |
| KEY_ROW1 | B21 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO16 | Input | Keeper |
| KEY_ROW2 | C21 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO17 | Input | Keeper |
| KEY_ROW3 | D21 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO18 | Input | Keeper |
| KEY_ROW4 | D22 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO19 | Input | Keeper |
| LCD1_CLK | H21 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO00 | Input | Keeper |
| LCD1_DATA00 | J23 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO01 | Input | Keeper |
| LCD1_DATA01 | J22 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO02 | Input | Keeper |
| LCD1_DATA02 | K20 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO03 | Input | Keeper |
| LCD1_DATA03 | K19 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO04 | Input | Keeper |
| LCD1_DATA04 | K18 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO05 | Input | Keeper |
| LCD1_DATA05 | J19 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO06 | Input | Keeper |
| LCD1_DATA06 | J18 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO07 | Input | Keeper |
| LCD1_DATA07 | H23 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO08 | Input | Keeper |
| LCD1_DATA08 | H22 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO09 | Input | Keeper |

Table 113. 19x19 mm Functional Contact Assignments (continued)

| Ball Name | 19x19 Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|--------------|------------|-------------|-----------|------------------------|------------------|--------------|--------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| LCD1_DATA09 | H20 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO10 | Input | Keeper |
| LCD1_DATA10 | H19 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO11 | Input | Keeper |
| LCD1_DATA11 | H18 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO12 | Input | Keeper |
| LCD1_DATA12 | G23 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO13 | Input | Keeper |
| LCD1_DATA13 | G22 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO14 | Input | Keeper |
| LCD1_DATA14 | G21 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO15 | Input | Keeper |
| LCD1_DATA15 | G19 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO16 | Input | Keeper |
| LCD1_DATA16 | G18 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO17 | Input | Keeper |
| LCD1_DATA17 | F23 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO18 | Input | Keeper |
| LCD1_DATA18 | F22 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO19 | Input | Keeper |
| LCD1_DATA19 | F21 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO20 | Input | Keeper |
| LCD1_DATA20 | G20 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO21 | Input | Keeper |
| LCD1_DATA21 | F19 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO22 | Input | Keeper |
| LCD1_DATA22 | F18 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO23 | Input | Keeper |
| LCD1_DATA23 | E20 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO24 | Input | Keeper |
| LCD1_ENABLE | E21 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO25 | Input | Keeper |
| LCD1_HSYNC | D23 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO26 | Input | Keeper |
| LCD1_RESET | E22 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO27 | Input | Keeper |
| LCD1_VSYNC | E23 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO28 | Input | Keeper |
| LVDS_CLK_N | T20 | NVCC_LVDS | LVDS | — | LVDS_CLK_N | — | — |
| LVDS_CLK_P | T21 | NVCC_LVDS | LVDS | ALT0 | LVDS_CLK_P | Input | — |
| LVDS_DATA0_N | V22 | NVCC_LVDS | LVDS | — | LVDS_DATA0_N | — | — |
| LVDS_DATA0_P | V23 | NVCC_LVDS | LVDS | ALT0 | LVDS_DATA0_P | Input | — |
| LVDS_DATA1_N | V20 | NVCC_LVDS | LVDS | — | LVDS_DATA1_N | — | — |
| LVDS_DATA1_P | V21 | NVCC_LVDS | LVDS | ALT0 | LVDS_DATA1_P | Input | — |
| LVDS_DATA2_N | U22 | NVCC_LVDS | LVDS | — | LVDS_DATA2_N | — | — |
| LVDS_DATA2_P | U23 | NVCC_LVDS | LVDS | ALT0 | LVDS_DATA2_P | Input | — |
| LVDS_DATA3_N | T22 | NVCC_LVDS | LVDS | — | LVDS_DATA3_N | — | — |
| LVDS_DATA3_P | T23 | NVCC_LVDS | LVDS | ALT0 | LVDS_DATA3_P | Input | — |
| NAND_ALE | AB7 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO00 | Input | Keeper |
| NAND_CE0_B | AB8 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO01 | Input | Keeper |
| NAND_CE1_B | AC9 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO02 | Input | Keeper |
| NAND_CLE | AB9 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO03 | Input | Keeper |

Table 113. 19x19 mm Functional Contact Assignments (continued)

| Ball Name | 19x19 Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|--------------|------------|-------------|-----------|------------------------|------------------|--------------|----------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| NAND_DATA00 | V7 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO04 | Input | Keeper |
| NAND_DATA01 | AA8 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO05 | Input | Keeper |
| NAND_DATA02 | W8 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO06 | Input | Keeper |
| NAND_DATA03 | V6 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO07 | Input | Keeper |
| NAND_DATA04 | W7 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO08 | Input | Keeper |
| NAND_DATA05 | W5 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO09 | Input | Keeper |
| NAND_DATA06 | Y8 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO10 | Input | Keeper |
| NAND_DATA07 | W6 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO11 | Input | Keeper |
| NAND_RE_B | AA9 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO12 | Input | Keeper |
| NAND_READY_B | AC7 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO13 | Input | Keeper |
| NAND_WE_B | AA7 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO14 | Input | Keeper |
| NAND_WP_B | AC8 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO15 | Input | Keeper |
| ONOFF | W17 | VDD_SNV5_IN | GPIO | — | ONOFF | Input | 100 kΩ pull-up |
| PCIE_RX_N | N22 | PCIE_VPH | — | — | PCIE_RX_N | — | — |
| PCIE_RX_P | N23 | PCIE_VPH | — | — | PCIE_RX_P | — | — |
| PCIE_TX_N | P22 | PCIE_VPH | — | — | PCIE_TX_N | — | — |
| PCIE_TX_P | P23 | PCIE_VPH | — | — | PCIE_TX_P | — | — |
| POR_B | V17 | VDD_SNV5_IN | GPIO | — | POR_B | Input | 100 kΩ pull-up |
| QSPI1A_DATA0 | C16 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO16 | Input | Keeper |
| QSPI1A_DATA1 | E16 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO17 | Input | Keeper |
| QSPI1A_DATA2 | D16 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO18 | Input | Keeper |
| QSPI1A_DATA3 | C17 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO19 | Input | Keeper |
| QSPI1A_DQS | E13 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO20 | Input | Keeper |
| QSPI1A_SCLK | E17 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO21 | Input | Keeper |
| QSPI1A_SS0_B | F16 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO22 | Input | Keeper |
| QSPI1A_SS1_B | F17 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO23 | Input | Keeper |
| QSPI1B_DATA0 | C14 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO24 | Input | Keeper |
| QSPI1B_DATA1 | E14 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO25 | Input | Keeper |
| QSPI1B_DATA2 | D14 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO26 | Input | Keeper |
| QSPI1B_DATA3 | C15 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO27 | Input | Keeper |
| QSPI1B_DQS | C13 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO28 | Input | Keeper |
| QSPI1B_SCLK | E15 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO29 | Input | Keeper |

Table 113. 19x19 mm Functional Contact Assignments (continued)

| Ball Name | 19x19 Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|--------------|------------|--------------|-----------|------------------------|------------------|--------------|--------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| QSPI1B_SS0_B | F14 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO30 | Input | Keeper |
| QSPI1B_SS1_B | F15 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO31 | Input | Keeper |
| RGMI1_RD0 | D8 | NVCC_RGMII1 | GPIO | ALT5 | GPIO5_IO00 | Input | Keeper |
| RGMI1_RD1 | E9 | NVCC_RGMII1 | GPIO | ALT5 | GPIO5_IO01 | Input | Keeper |
| RGMI1_RD2 | C8 | NVCC_RGMII1 | GPIO | ALT5 | GPIO5_IO02 | Input | Keeper |
| RGMI1_RD3 | E8 | NVCC_RGMII1 | GPIO | ALT5 | GPIO5_IO03 | Input | Keeper |
| RGMI1_RX_CTL | E10 | NVCC_RGMII1 | GPIO | ALT5 | GPIO5_IO04 | Input | Keeper |
| RGMI1_RXC | D10 | NVCC_RGMII1 | GPIO | ALT5 | GPIO5_IO05 | Input | Keeper |
| RGMI1_TD0 | C12 | NVCC_RGMII1 | GPIO | ALT5 | GPIO5_IO06 | Input | Keeper |
| RGMI1_TD1 | D12 | NVCC_RGMII1 | GPIO | ALT5 | GPIO5_IO07 | Input | Keeper |
| RGMI1_TD2 | E12 | NVCC_RGMII1 | GPIO | ALT5 | GPIO5_IO08 | Input | Keeper |
| RGMI1_TD3 | C11 | NVCC_RGMII1 | GPIO | ALT5 | GPIO5_IO09 | Input | Keeper |
| RGMI1_TX_CTL | C10 | NVCC_RGMII1 | GPIO | ALT5 | GPIO5_IO10 | Input | Keeper |
| RGMI1_TXC | E11 | NVCC_RGMII1 | GPIO | ALT5 | GPIO5_IO11 | Input | Keeper |
| RGMI2_RD0 | A9 | NVCC_RGMII2 | GPIO | ALT5 | GPIO5_IO12 | Input | Keeper |
| RGMI2_RD1 | B9 | NVCC_RGMII2 | GPIO | ALT5 | GPIO5_IO13 | Input | Keeper |
| RGMI2_RD2 | A8 | NVCC_RGMII2 | GPIO | ALT5 | GPIO5_IO14 | Input | Keeper |
| RGMI2_RD3 | B8 | NVCC_RGMII2 | GPIO | ALT5 | GPIO5_IO15 | Input | Keeper |
| RGMI2_RX_CTL | B10 | NVCC_RGMII2 | GPIO | ALT5 | GPIO5_IO16 | Input | Keeper |
| RGMI2_RXC | A10 | NVCC_RGMII2 | GPIO | ALT5 | GPIO5_IO17 | Input | Keeper |
| RGMI2_TD0 | A12 | NVCC_RGMII2 | GPIO | ALT5 | GPIO5_IO18 | Input | Keeper |
| RGMI2_TD1 | B12 | NVCC_RGMII2 | GPIO | ALT5 | GPIO5_IO19 | Input | Keeper |
| RGMI2_TD2 | A13 | NVCC_RGMII2 | GPIO | ALT5 | GPIO5_IO20 | Input | Keeper |
| RGMI2_TD3 | B13 | NVCC_RGMII2 | GPIO | ALT5 | GPIO5_IO21 | Input | Keeper |
| RGMI2_TX_CTL | B11 | NVCC_RGMII2 | GPIO | ALT5 | GPIO5_IO22 | Input | Keeper |
| RGMI2_TXC | A11 | NVCC_RGMII2 | GPIO | ALT5 | GPIO5_IO23 | Input | Keeper |
| RTC_XTALI | AB20 | VDD_SNVS_CAP | — | — | RTC_XTALI | — | — |
| RTC_XTALO | AC20 | VDD_SNVS_CAP | — | — | RTC_XTALO | — | — |
| SD1_CLK | A15 | NVCC_SD1 | GPIO | ALT5 | GPIO6_IO00 | Input | Keeper |
| SD1_CMD | B15 | NVCC_SD1 | GPIO | ALT5 | GPIO6_IO01 | Input | Keeper |
| SD1_DATA0 | B16 | NVCC_SD1 | GPIO | ALT5 | GPIO6_IO02 | Input | Keeper |
| SD1_DATA1 | A16 | NVCC_SD1 | GPIO | ALT5 | GPIO6_IO03 | Input | Keeper |
| SD1_DATA2 | B14 | NVCC_SD1 | GPIO | ALT5 | GPIO6_IO04 | Input | Keeper |

Table 113. 19x19 mm Functional Contact Assignments (continued)

| Ball Name | 19x19 Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|-----------|------------|-----------------------|-----------|------------------------|------------------|--------------|---------------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| SD1_DATA3 | A14 | NVCC_SD1 | GPIO | ALT5 | GPIO6_IO05 | Input | Keeper |
| SD2_CLK | F12 | NVCC_SD2 | GPIO | ALT5 | GPIO6_IO06 | Input | Keeper |
| SD2_CMD | F11 | NVCC_SD2 | GPIO | ALT5 | GPIO6_IO07 | Input | Keeper |
| SD2_DATA0 | G13 | NVCC_SD2 | GPIO | ALT5 | GPIO6_IO08 | Input | Keeper |
| SD2_DATA1 | F13 | NVCC_SD2 | GPIO | ALT5 | GPIO6_IO09 | Input | Keeper |
| SD2_DATA2 | F10 | NVCC_SD2 | GPIO | ALT5 | GPIO6_IO10 | Input | Keeper |
| SD2_DATA3 | G10 | NVCC_SD2 | GPIO | ALT5 | GPIO6_IO11 | Input | Keeper |
| SD3_CLK | Y12 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO00 | Input | 100 kΩ pull-down |
| SD3_CMD | W13 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO01 | Input | 100 kΩ pull-down |
| SD3_DATA0 | AA11 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO02 | Input | 100 kΩ pull-down |
| SD3_DATA1 | W10 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO03 | Input | 100 kΩ pull-down |
| SD3_DATA2 | AA15 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO04 | Input | 100 kΩ pull-down |
| SD3_DATA3 | Y14 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO05 | Input | 100 kΩ pull-down |
| SD3_DATA4 | AA14 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO06 | Input | 100 kΩ pull-down |
| SD3_DATA5 | AA13 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO07 | Input | 100 kΩ pull-down |
| SD3_DATA6 | AA12 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO08 | Input | 100 kΩ pull-down |
| SD3_DATA7 | W11 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO09 | Input | 100 kΩ pull-down |
| SD4_CLK | AB12 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO12 | Input | Keeper |
| SD4_CMD | AB13 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO13 | Input | Keeper |
| SD4_DATA0 | AC10 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO14 | Input | Keeper |
| SD4_DATA1 | AB10 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO15 | Input | Keeper |
| SD4_DATA2 | AC14 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO16 | Input | Keeper |
| SD4_DATA3 | AB14 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO17 | Input | Keeper |
| SD4_DATA4 | AC13 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO18 | Input | Keeper |
| SD4_DATA5 | AC12 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO19 | Input | Keeper |
| SD4_DATA6 | AC11 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO20 | Input | Keeper |

Table 113. 19x19 mm Functional Contact Assignments (continued)

| Ball Name | 19x19 Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|-------------------------------|------------|-------------|-----------|------------------------|------------------|--------------|------------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| SD4_DATA7 | AB11 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO21 | Input | Keeper |
| SD4_RESET_B | Y9 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO22 | Input | Keeper |
| SNVS_PMIC_ON_REQ ¹ | W16 | VDD_SNVS_IN | GPIO | — | SNVS_PMIC_ON_REQ | Output | 100 kΩ pull-up |
| SNVS_TAMPER | V14 | VDD_SNVS_IN | GPIO | — | SNVS_TAMPER | Input | 100 kΩ pull-down |
| TEST_MODE | Y16 | VDD_SNVS_IN | — | — | TEST_MODE | Input | 100 kΩ pull-down |
| USB_H_DATA | Y5 | NVCC_USB_H | GPIO | ALT5 | GPIO7_IO10 | Input | 100 kΩ pull-down |
| USB_H_STROBE | Y6 | NVCC_USB_H | GPIO | ALT5 | GPIO7_IO11 | Input | 100 kΩ pull-down |
| USB_OTG1_CHD_B | V19 | VDD_USB_CAP | — | — | USB_OTG1_CHD_B | — | — |
| USB_OTG1_DN | Y21 | VDD_USB_CAP | — | — | USB_OTG1_DN | — | — |
| USB_OTG1_DP | AA21 | VDD_USB_CAP | — | — | USB_OTG1_DP | — | — |
| USB_OTG2_DN | Y19 | VDD_USB_CAP | — | — | USB_OTG2_DN | — | — |
| USB_OTG2_DP | AA19 | VDD_USB_CAP | — | — | USB_OTG2_DP | — | — |
| Reserved | L23 | — | — | — | — | — | — |
| Reserved | L22 | — | — | — | — | — | — |
| Reserved | K23 | — | — | — | — | — | — |
| Reserved | K22 | — | — | — | — | — | — |
| XTALI | AB22 | NVCC_PLL | — | — | XTALI | — | — |
| XTALO | AC22 | NVCC_PLL | — | — | XTALO | — | — |

¹ On silicon revisions prior to 1.2, the SNVS_PMIC_ON_REQ may briefly go low and then return high during POR. SNVS_PMIC_ON_REQ should be high during POR. An external 100k pull-up is required.

6.3.3 19x19 mm, 0.8 mm Pitch, 23x23 Ball Map

Table 114 shows the 19x19 mm, 0.8 mm pitch ball map for the i.MX 6SoloX.

Table 114. 19x19 mm, 0.8 mm Pitch, 23x23 Ball Map

| G | F | E | D | C | B | A |
|-------------|--------------|---------------|--------------|---------------|---------------|--------------|
| DRAM_DQM1 | DRAM_DATA13 | DRAM_DATA15 | DRAM_DATA25 | DRAM_DQM3 | DRAM_DATA28 | VSS |
| DRAM_DATA11 | VSS | DRAM_DATA14 | DRAM_DATA27 | VSS | DRAM_DATA26 | DRAM_SDQS3_N |
| DRAM_ADDR05 | VSS | DRAM_SDCKE1 | DRAM_CS1_B | VSS | VSS | DRAM_SDQS3_P |
| DRAM_ADDR02 | DRAM_ADDR07 | DRAM_ADDR15 | DRAM_RESET | DRAM_ZQPAD | DRAM_DATA24 | DRAM_DATA29 |
| NVCC_DRAM | NVCC_DRAM | RSVD | ENET2_RX_CLK | VSS | DRAM_DATA30 | DRAM_DATA31 |
| VSS | NVCC_ENET | ENET1_COL | ENET2_CRS | ENET2_TX_CLK | VSS | VSS |
| VSS | ENET2_COL | ENET1_MDIO | VSS | ENET1_CRS | ENET1_RX_CLK | ENET1_TX_CLK |
| VSS | NVCC_RGMII1 | RGMI11_RD3 | RGMI11_RD0 | RGMI11_RD2 | RGMI12_RD3 | RGMI12_RD2 |
| NVCC_RGMII2 | ENET1_MDC | RGMI11_RD1 | VSS | VDD_SOC_IN | RGMI12_RD1 | RGMI12_RD0 |
| SD2_DATA3 | SD2_DATA2 | RGMI11_RX_CTL | RGMI11_RXC | RGMI11_TX_CTL | RGMI12_RX_CTL | RGMI12_RXC |
| NVCC_SD2 | SD2_CMD | RGMI11_TXC | VSS | RGMI11_TD3 | RGMI12_TX_CTL | RGMI12_TXC |
| NVCC_SD1 | SD2_CLK | RGMI11_TD2 | RGMI11_TD1 | RGMI11_TD0 | RGMI12_TD1 | RGMI12_TD0 |
| SD2_DATA0 | SD2_DATA1 | QSPI1A_DQS | VSS | QSPI1B_DQS | RGMI12_TD3 | RGMI12_TD2 |
| NVCC_QSPI | QSPI1B_SS0_B | QSPI1B_DATA1 | QSPI1B_DATA2 | QSPI1B_DATA0 | SD1_DATA2 | SD1_DATA3 |
| NVCC_GPIO | QSPI1B_SS1_B | QSPI1B_SCLK | VSS | QSPI1B_DATA3 | SD1_CMD | SD1_CLK |
| NVCC_KEY | QSPI1A_SS0_B | QSPI1A_DATA1 | QSPI1A_DATA2 | QSPI1A_DATA0 | SD1_DATA0 | SD1_DATA1 |
| NVCC_LCD1 | QSPI1A_SS1_B | QSPI1A_SCLK | VSS | QSPI1A_DATA3 | GPIO1_IO13 | GPIO1_IO12 |
| LCD1_DATA16 | LCD1_DATA22 | GPIO1_IO11 | GPIO1_IO09 | VDD_ARM_CAP | GPIO1_IO08 | GPIO1_IO07 |
| LCD1_DATA15 | LCD1_DATA21 | GPIO1_IO10 | VSS | GPIO1_IO06 | GPIO1_IO05 | GPIO1_IO04 |
| LCD1_DATA20 | VSS | LCD1_DATA23 | GPIO1_IO03 | GPIO1_IO02 | GPIO1_IO01 | GPIO1_IO00 |
| LCD1_DATA14 | LCD1_DATA19 | LCD1_ENABLE | KEY_ROW3 | KEY_ROW2 | KEY_ROW1 | KEY_ROW0 |
| LCD1_DATA13 | LCD1_DATA18 | LCD1_RESET | KEY_ROW4 | KEY_COL1 | KEY_COL3 | KEY_COL4 |
| LCD1_DATA12 | LCD1_DATA17 | LCD1_VSYNC | LCD1_HSYNC | KEY_COL0 | KEY_COL2 | VSS |
| G | F | E | D | C | B | A |

Table 114. 19x19 mm, 0.8 mm Pitch, 23x23 Ball Map (continued)

| AA | Y | W | V | U | T | R |
|-------------|---------------|------------------|-------------------|--------------|--------------|-------------|
| DRAM_DATA22 | DRAM_DATA23 | DRAM_DATA03 | DRAM_DATA02 | DRAM_SDQS0_N | DRAM_SDQS0_P | DRAM_DATA06 |
| VSS | DRAM_DATA20 | DRAM_DATA01 | VSS | DRAM_DATA00 | DRAM_DQM0 | VSS |
| VSS | DRAM_ADDR06 | DRAM_ADDR12 | VSS | DRAM_SDBA1 | DRAM_ADDR08 | VSS |
| DRAM_ODT0 | DRAM_ADDR01 | DRAM_ADDR14 | DRAM_SDCKE0 | DRAM_ADDR10 | DRAM_ADDR11 | DRAM_ADDR04 |
| VSS | USB_H_DATA | NAND_DATA05 | NVCC_DRAM | NVCC_DRAM | NVCC_DRAM | NVCC_DRAM |
| NVCC_USB_H | USB_H_STROBE | NAND_DATA07 | NAND_DATA03 | VSS | VSS | VSS |
| NAND_WE_B | VSS | NAND_DATA04 | NAND_DATA00 | VSS | VSS | VDD_SOC_CAP |
| NAND_DATA01 | NAND_DATA06 | NAND_DATA02 | VSS | NVCC_NAND | VSS | VDD_SOC_CAP |
| NAND_RE_B | SD4_RESET_B | JTAG_TDO | VSS | JTAG_MOD | VSS | VDD_SOC_CAP |
| VDD_SOC_CAP | VDD_SOC_CAP | SD3_DATA1 | JTAG_TCK | NVCC_SD4 | VSS | VDD_SOC_CAP |
| SD3_DATA0 | VSS | SD3_DATA7 | NVCC_LOW | NVCC_JTAG | VSS | VDD_SOC_CAP |
| SD3_DATA6 | SD3_CLK | JTAG_TMS | JTAG_TDI | NVCC_HIGH | VSS | VDD_SOC_CAP |
| SD3_DATA5 | VSS | SD3_CMD | JTAG_TRST_B | VDDA_ADC_3P3 | VSS | VDD_SOC_CAP |
| SD3_DATA4 | SD3_DATA3 | BOOT_MODE0 | SNVS_TAMPER | VDD_HIGH_IN | VSS | VDD_SOC_CAP |
| SD3_DATA2 | VSS | BOOT_MODE1 | VDD_SNVS_IN | VDD_HIGH_IN | VSS | VDD_SOC_CAP |
| ADC_VREFH | TEST_MODE | SNVS_PMIC_ON_REQ | CCM_PMIC_STBY_REQ | ADC_VREFL | VSS | NGND_KEL0 |
| VDD_USB_CAP | VSS | ONOFF | POR_B | VDD_HIGH_CAP | VSS | VSS |
| VSS | USB_OTG2_VBUS | CCM_CLK2 | GANAIO | VDD_HIGH_CAP | NVCC_LVDS | PCIE_VPH |
| USB_OTG2_DP | USB_OTG2_DN | VSS | USB_OTG1_CHD_B | CSI_VSYNC | CSI_PIXCLK | CSI_MCLK |
| VSS | VSS | USB_OTG1_VBUS | LVDS_DATA1_N | VSS | LVDS_CLK_N | VSS |
| USB_OTG1_DP | USB_OTG1_DN | VSS | LVDS_DATA1_P | VSS | LVDS_CLK_P | VSS |
| CCM_CLK1_N | VDD_SNVS_CAP | VSS | LVDS_DATA0_N | LVDS_DATA2_N | LVDS_DATA3_N | VSS |
| CCM_CLK1_P | NVCC_PLL | VSS | LVDS_DATA0_P | LVDS_DATA2_P | LVDS_DATA3_P | VSS |
| AA | Y | W | V | U | T | R |

Table 115. Pinout Differences Between 17x17 NP and 17x17 WP Packages (continued)

| 17x17 NP Package (No PCIe) | 17x17 WP Package (With PCIe) | Ball Name |
|-------------------------------|---------------------------------|--------------------------|
| W16 | Not in this package | ADC2_IN1 |
| T16 | Not in this package | ADC2_IN2 |
| U16 | Not in this package | ADC2_IN3 |
| N15 | U20 | BOOT_MODE0 |
| P14 | U19 | BOOT_MODE1 |
| P19 | P16 | CCM_CLK1_N |
| P20 | R16 | CCM_CLK1_P |
| T14 | R15 | CCM_CLK2 |
| N16 | P15 | CCM_PMIC_STBY_REQ |
| T15 | U16 | GPANAIO |
| U18 | W20 | NVCC_PLL |
| R15 | N15 | ONOFF |
| Not in this package | N18 | PCIE_REXT |
| Not in this package | P19 | PCIE_RX_N |
| Not in this package | P20 | PCIE_RX_P |
| Not in this package | R19 | PCIE_TX_N |
| Not in this package | R20 | PCIE_TX_P |
| Not in this package | P18 | PCIE_VP |
| L18 | Not in this package | PCIE_VP_CAP ² |
| Not in this package | R18 | PCIE_VPH |
| Not in this package | P17 | PCIE_VPTX |
| R16 | P14 | POR_B |
| V19 | W19 | RTC_XTALI |
| V20 | Y19 | RTC_XTALO |
| P16 | N16 | SNVS_PMIC_ON_REQ |
| P15 | R14 | SNVS_TAMPER |
| W20 | T17 | USB_OTG1_CHD_B |
| W19 | W17 | USB_OTG1_DN |
| Y19 | Y17 | USB_OTG1_DP |
| T17 | T16 | USB_OTG1_VBUS |
| W17 | W15 | USB_OTG2_DN |
| Y17 | Y15 | USB_OTG2_DP |

Table 115. Pinout Differences Between 17x17 NP and 17x17 WP Packages (continued)

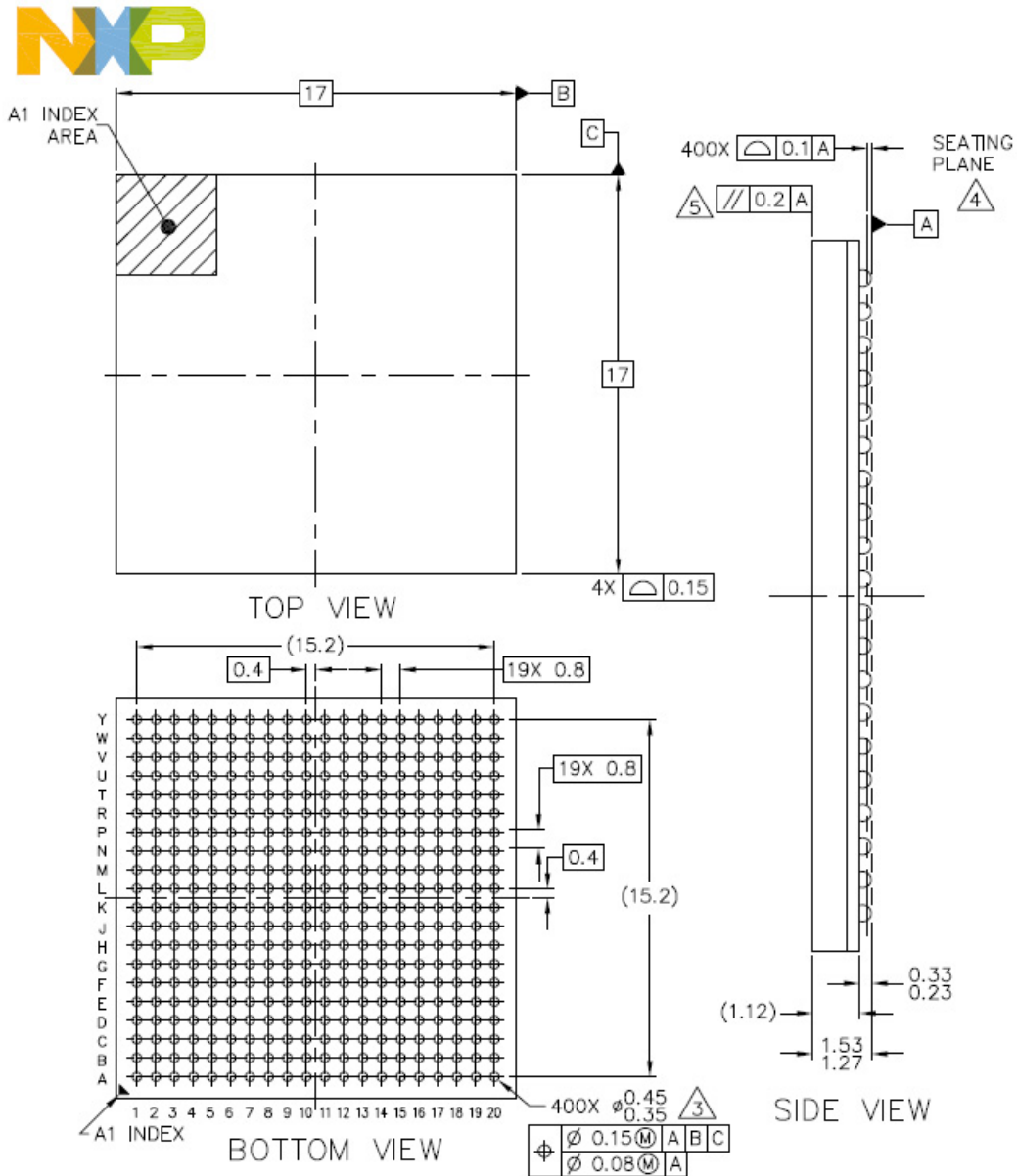
| 17x17 NP Package (No PCIe) | 17x17 WP Package (With PCIe) | Ball Name |
|-------------------------------|---------------------------------|---------------|
| U17 | T15 | USB_OTG2_VBUS |
| N17 | V17 | VDD_HIGH_CAP |
| N18 | V18 | VDD_HIGH_CAP |
| P17 | U17 | VDD_HIGH_IN |
| P18 | U18 | VDD_HIGH_IN |
| T18 | V16 | VDD_SNVS_CAP |
| R18 | T18 | VDD_SNVS_IN |
| V17 | V15 | VDD_USB_CAP |
| R19 | N19 | VSS |
| R20 | N20 | VSS |
| U19 | T19 | VSS |
| U20 | T20 | VSS |
| V18 | Not in this package | VSS |
| Not in this package | W16 | VSS |
| Not in this package | Y16 | VSS |
| T19 | V19 | XTALI |
| T20 | V20 | XTALO |

¹ In the 17x17 WP package, ADC_VREFL is connected internally to VSS. ADC_VREFH is connected internally to VDDA_ADC_3P3.

² In the 17x17 NP package, PCIE_VP_CAP must be connected to an external 4.7uF filter capacitor.

6.4.2 17x17 mm, 0.8 mm Pitch, 20x20 Ball Matrix

Figure 86 shows the top, bottom, and side views of the 17x17 mm BGA package.



| | | |
|---|--------------------------|----------------------------|
| © NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |
| TITLE: 400 I/O, FINE PITCH, PBGA, 17 X 17 PKG, 0.8MM PITCH (STD MAP) | DOCUMENT NO: 98ASA10507D | REV: B |
| | STANDARD: NON-JEDEC | |
| | SOT1512-1 | 29 FEB 2016 |

Figure 86. 17x17 mm BGA Package—Top, Bottom, and Side Views



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- ③ MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
- ④ DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
- ⑤ PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

| | | | |
|---|--------------------------|----------------------------|-------------|
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| TITLE: 400 I/O, FINE PITCH, PBGA, 17 X 17 PKG. 0.8MM PITCH (STD MAP) | DOCUMENT NO: 98ASA10507D | | REV: B |
| | STANDARD: NON-JEDEC | | |
| | SOT1512-1 | | 29 FEB 2016 |

Figure 87. 17x17 mm BGA Package Notes

6.4.3 17x17 mm NP (No PCIe) Supplies Contact Assignments and Functional Contact Assignments

Table 116 shows supplies contact assignments for the 17x17 mm NP (No PCIe) package.

Table 116. 17x17 mm NP (no PCIe) Supplies Contact Assignments

| Supply Rail Name | 17x17 NP [No PCIe] Ball(s) Position(s) | Remark |
|------------------|---|---|
| ADC_VREFH | V16 | ADC high reference voltage |
| ADC_VREFL | R14 | ADC low reference voltage |
| DRAM_VREF | J3 | DDR voltage reference input. Connect to a voltage source that is 50% of NVCC_DRAM. |
| DRAM_ZQPAD | C5 | DDR output buffer driver calibration reference voltage input. Connect DRAM_ZQPAD to an external 240 ohm 1% resistor to Vss. |
| GPANAIO | T15 | Analog output for NXP use only. This output must always be left unconnected. |
| NGND_KELO | P13 | Connect to Vss |
| NVCC_DRAM | G6, H6, J6, K6, L6, M6, N6, P6 | Supply input for the DDR I/O interface |
| NVCC_DRAM_2P5 | K7 | Supply input for the DDR interface |
| NVCC_ENET | F6 | Supply input for the ENET interfaces |
| NVCC_GPIO | F15 | Supply input for the GPIO interface |
| NVCC_HIGH | R12 | 3.3 V Supply input for the dual-voltage I/Os on the SD3 interface |
| NVCC_JTAG | R11 | Supply input for the JTAG interface |
| NVCC_KEY | G15 | Supply input for the Key Pad Port (KPP) interface |
| NVCC_LCD1 | H15 | Supply input for the LCD interface |
| NVCC_LOW | V13 | 1.8 V Supply input for the dual-voltage I/Os on the SD3 interface |
| NVCC_NAND | R6 | Supply input for the Raw NAND flash memories interface |
| NVCC_PLL | U18 | Supply input for the PLLs |
| NVCC_QSPI | F14 | Supply input for the QSPI interface |
| NVCC_RGMII1 | F8 | Supply input for the RGMII1 interface |
| NVCC_RGMII2 | F9 | Supply input for the RGMII2 interface |
| NVCC_SD2 | F13 | Supply input for the SD2 interface |
| NVCC_SD4 | V10 | Supply input for the SD4 interface |
| NVCC_USB_H | V5 | Supply input for the USB HSIC interface |
| PCI_VP_CAP | L18 | PCIe LDO output |
| USB_OTG1_VBUS | T17 | VBUS input for USB_OTG1 |

Table 116. 17x17 mm NP (no PCIe) Supplies Contact Assignments (continued)

| Supply Rail Name | 17x17 NP [No PCIe] Ball(s) Position(s) | Remark |
|------------------|--|--|
| USB_OTG2_VBUS | U17 | VBUS input for USB_OTG2 |
| VDD_ARM_CAP | C16, D16, H10, H11, H12, H13, J13, K13, L13 | Supply voltage output from internal LDO_ARM. Requires external capacitor(s). |
| VDD_ARM_IN | H18, J10, J11, J12, K12, L12 | Supply voltage input for internal LDO_ARM. |
| VDD_HIGH_CAP | N17, N18 | Supply voltage output from internal LDO_2P5. Requires external capacitor(s). |
| VDD_HIGH_IN | P17, P18 | Supply voltage input to internal LDO_2P5, LDO_1P1 and LDO_SNVS. |
| VDD_SNVS_CAP | T18 | Supply voltage output from internal LDO_SNVS. Requires external capacitor(s). |
| VDD_SNVS_IN | R18 | Supply voltage input to the SNVS voltage domain |
| VDD_SOC_CAP | H8, H9, J8, K8, L8, M8, M13, N8, N9, N10, N11, N12, V8 | Supply voltage output from internal LDO_SOC. Requires external capacitor(s). |
| VDD_SOC_IN | C7, C8, J9, K9, L9, M9, M10, M11, M12 | Supply voltage input to internal LDO_SOC and LDO_PCIE |
| VDD_USB_CAP | V17 | Supply voltage output from internal LDO_USB. Requires external capacitor(s). |
| VDDA_ADC_3P3 | R13 | Supply voltage input to the ADC. This supply must be provided even if the ADC is not used. |
| VSS | A1, A20, C3, C4, C18, D6, D9, D12, D15, E3, F3, F5, F17, G7, G8, G9, G10, G11, G12, G13, G14, H3, H7, H14, J7, J14, J17, K3, K10, K11, K14, L3, L7, L10, L11, L14, M7, M14, M17, N3, N7, N13, P7, P8, P9, P10, P11, P12, R3, R5, R17, R19, R20, T3, U6, U9, U12, U15, U19, U20, V3, V4, V18, W18, Y1, Y18, Y20 | Ground |

Table 117 shows an alpha-sorted list of functional contact assignments for the 17x17 mm NP (No PCIe) package.

Table 117. 17x17 mm NP (No PCIe) Functional Contact Assignments

| Ball Name | 17x17 NP Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|-----------|---------------|--------------|-----------|------------------------|------------------|--------------|-------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| ADC1_IN0 | Y14 | VDDA_ADC_3P3 | — | — | ADC1_IN0 | Input | — |
| ADC1_IN1 | W14 | VDDA_ADC_3P3 | — | — | ADC1_IN1 | Input | — |
| ADC1_IN2 | Y15 | VDDA_ADC_3P3 | — | — | ADC1_IN2 | Input | — |

Table 117. 17x17 mm NP (No PCIe) Functional Contact Assignments (continued)

| Ball Name | 17x17 NP Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|-------------------|---------------|--------------|-----------|------------------------|-------------------|--------------|------------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| ADC1_IN3 | W15 | VDDA_ADC_3P3 | — | — | ADC1_IN3 | Input | — |
| ADC2_IN0 | Y16 | VDDA_ADC_3P3 | — | — | ADC2_IN0 | Input | — |
| ADC2_IN1 | W16 | VDDA_ADC_3P3 | — | — | ADC2_IN1 | Input | — |
| ADC2_IN2 | T16 | VDDA_ADC_3P3 | — | — | ADC2_IN2 | Input | — |
| ADC2_IN3 | U16 | VDDA_ADC_3P3 | — | — | ADC2_IN3 | Input | — |
| BOOT_MODE0 | N15 | VDD_SNVS_IN | GPIO | — | BOOT_MODE0 | Input | 100 kΩ pull-down |
| BOOT_MODE1 | P14 | VDD_SNVS_IN | GPIO | — | BOOT_MODE1 | Input | 100 kΩ pull-down |
| CCM_CLK1_N | P19 | VDD_HIGH_CAP | — | — | CCM_CLK1_N | — | — |
| CCM_CLK1_P | P20 | VDD_HIGH_CAP | — | — | CCM_CLK1_P | — | — |
| CCM_CLK2 | T14 | VDD_HIGH_CAP | — | — | CCM_CLK2 | — | — |
| CCM_PMIC_STBY_REQ | N16 | VDD_SNVS_IN | GPIO | — | CCM_PMIC_STBY_REQ | Output | 0 |
| DRAM_ADDR00 | L4 | NVCC_DRAM | DDR | — | DRAM_ADDR00 | Output | 100 kΩ pull-up |
| DRAM_ADDR01 | U4 | NVCC_DRAM | DDR | — | DRAM_ADDR01 | Output | 100 kΩ pull-up |
| DRAM_ADDR02 | K5 | NVCC_DRAM | DDR | — | DRAM_ADDR02 | Output | 100 kΩ pull-up |
| DRAM_ADDR03 | G5 | NVCC_DRAM | DDR | — | DRAM_ADDR03 | Output | 100 kΩ pull-up |
| DRAM_ADDR04 | M3 | NVCC_DRAM | DDR | — | DRAM_ADDR04 | Output | 100 kΩ pull-up |
| DRAM_ADDR05 | G4 | NVCC_DRAM | DDR | — | DRAM_ADDR05 | Output | 100 kΩ pull-up |
| DRAM_ADDR06 | T4 | NVCC_DRAM | DDR | — | DRAM_ADDR06 | Output | 100 kΩ pull-up |
| DRAM_ADDR07 | F4 | NVCC_DRAM | DDR | — | DRAM_ADDR07 | Output | 100 kΩ pull-up |
| DRAM_ADDR08 | M5 | NVCC_DRAM | DDR | — | DRAM_ADDR08 | Output | 100 kΩ pull-up |
| DRAM_ADDR09 | L5 | NVCC_DRAM | DDR | — | DRAM_ADDR09 | Output | 100 kΩ pull-up |
| DRAM_ADDR10 | N5 | NVCC_DRAM | DDR | — | DRAM_ADDR10 | Output | 100 kΩ pull-up |

Table 117. 17x17 mm NP (No PCIe) Functional Contact Assignments (continued)

| Ball Name | 17x17 NP Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|-------------|---------------|-------------|-----------|------------------------|------------------|--------------|----------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| DRAM_ADDR11 | N4 | NVCC_DRAM | DDR | — | DRAM_ADDR11 | Output | 100 kΩ pull-up |
| DRAM_ADDR12 | P4 | NVCC_DRAM | DDR | — | DRAM_ADDR12 | Output | 100 kΩ pull-up |
| DRAM_ADDR13 | M4 | NVCC_DRAM | DDR | — | DRAM_ADDR13 | Output | 100 kΩ pull-up |
| DRAM_ADDR14 | R4 | NVCC_DRAM | DDR | — | DRAM_ADDR14 | Output | 100 kΩ pull-up |
| DRAM_CAS_B | J4 | NVCC_DRAM | DDR | — | DRAM_CAS_B | Output | 100 kΩ pull-up |
| DRAM_CS0_B | H4 | NVCC_DRAM | DDR | — | DRAM_CS0_B | Output | 100 kΩ pull-up |
| DRAM_CS1_B | D3 | NVCC_DRAM | DDR | — | DRAM_CS1_B | Output | 100 kΩ pull-up |
| DRAM_DATA00 | R1 | NVCC_DRAM | DDR | — | DRAM_DATA00 | Input | 100 kΩ pull-up |
| DRAM_DATA01 | T2 | NVCC_DRAM | DDR | — | DRAM_DATA01 | Input | 100 kΩ pull-up |
| DRAM_DATA02 | T1 | NVCC_DRAM | DDR | — | DRAM_DATA02 | Input | 100 kΩ pull-up |
| DRAM_DATA03 | R2 | NVCC_DRAM | DDR | — | DRAM_DATA03 | Input | 100 kΩ pull-up |
| DRAM_DATA04 | M1 | NVCC_DRAM | DDR | — | DRAM_DATA04 | Input | 100 kΩ pull-up |
| DRAM_DATA05 | M2 | NVCC_DRAM | DDR | — | DRAM_DATA05 | Input | 100 kΩ pull-up |
| DRAM_DATA06 | L2 | NVCC_DRAM | DDR | — | DRAM_DATA06 | Input | 100 kΩ pull-up |
| DRAM_DATA07 | N1 | NVCC_DRAM | DDR | — | DRAM_DATA07 | Input | 100 kΩ pull-up |
| DRAM_DATA08 | H1 | NVCC_DRAM | DDR | — | DRAM_DATA08 | Input | 100 kΩ pull-up |
| DRAM_DATA09 | F2 | NVCC_DRAM | DDR | — | DRAM_DATA09 | Input | 100 kΩ pull-up |
| DRAM_DATA10 | K2 | NVCC_DRAM | DDR | — | DRAM_DATA10 | Input | 100 kΩ pull-up |
| DRAM_DATA11 | J2 | NVCC_DRAM | DDR | — | DRAM_DATA11 | Input | 100 kΩ pull-up |

Table 117. 17x17 mm NP (No PCIe) Functional Contact Assignments (continued)

| Ball Name | 17x17 NP Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|-------------|---------------|-------------|-----------|------------------------|------------------|--------------|------------------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| DRAM_DATA12 | J1 | NVCC_DRAM | DDR | — | DRAM_DATA12 | Input | 100 k Ω pull-up |
| DRAM_DATA13 | F1 | NVCC_DRAM | DDR | — | DRAM_DATA13 | Input | 100 k Ω pull-up |
| DRAM_DATA14 | E2 | NVCC_DRAM | DDR | — | DRAM_DATA14 | Input | 100 k Ω pull-up |
| DRAM_DATA15 | E1 | NVCC_DRAM | DDR | — | DRAM_DATA15 | Input | 100 k Ω pull-up |
| DRAM_DATA16 | V1 | NVCC_DRAM | DDR | — | DRAM_DATA16 | Input | 100 k Ω pull-up |
| DRAM_DATA17 | W4 | NVCC_DRAM | DDR | — | DRAM_DATA17 | Input | 100 k Ω pull-up |
| DRAM_DATA18 | Y4 | NVCC_DRAM | DDR | — | DRAM_DATA18 | Input | 100 k Ω pull-up |
| DRAM_DATA19 | U2 | NVCC_DRAM | DDR | — | DRAM_DATA19 | Input | 100 k Ω pull-up |
| DRAM_DATA20 | W3 | NVCC_DRAM | DDR | — | DRAM_DATA20 | Input | 100 k Ω pull-up |
| DRAM_DATA21 | Y2 | NVCC_DRAM | DDR | — | DRAM_DATA21 | Input | 100 k Ω pull-up |
| DRAM_DATA22 | U1 | NVCC_DRAM | DDR | — | DRAM_DATA22 | Input | 100 k Ω pull-up |
| DRAM_DATA23 | V2 | NVCC_DRAM | DDR | — | DRAM_DATA23 | Input | 100 k Ω pull-up |
| DRAM_DATA24 | A2 | NVCC_DRAM | DDR | — | DRAM_DATA24 | Input | 100 k Ω pull-up |
| DRAM_DATA25 | D1 | NVCC_DRAM | DDR | — | DRAM_DATA25 | Input | 100 k Ω pull-up |
| DRAM_DATA26 | C1 | NVCC_DRAM | DDR | — | DRAM_DATA26 | Input | 100 k Ω pull-up |
| DRAM_DATA27 | D2 | NVCC_DRAM | DDR | — | DRAM_DATA27 | Input | 100 k Ω pull-up |
| DRAM_DATA28 | C2 | NVCC_DRAM | DDR | — | DRAM_DATA28 | Input | 100 k Ω pull-up |
| DRAM_DATA29 | B3 | NVCC_DRAM | DDR | — | DRAM_DATA29 | Input | 100 k Ω pull-up |
| DRAM_DATA30 | B4 | NVCC_DRAM | DDR | — | DRAM_DATA30 | Input | 100 k Ω pull-up |

Table 117. 17x17 mm NP (No PCIe) Functional Contact Assignments (continued)

| Ball Name | 17x17 NP Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|---------------|---------------|-------------|-----------|------------------------|------------------|--------------|--------------------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| DRAM_DATA31 | A4 | NVCC_DRAM | DDR | — | DRAM_DATA31 | Input | 100 k Ω pull-up |
| DRAM_DQM0 | N2 | NVCC_DRAM | DDR | — | DRAM_DQM0 | Output | 100 k Ω pull-up |
| DRAM_DQM1 | G2 | NVCC_DRAM | DDR | — | DRAM_DQM1 | Output | 100 k Ω pull-up |
| DRAM_DQM2 | Y3 | NVCC_DRAM | DDR | — | DRAM_DQM2 | Output | 100 k Ω pull-up |
| DRAM_DQM3 | A3 | NVCC_DRAM | DDR | — | DRAM_DQM3 | Output | 100 k Ω pull-up |
| DRAM_ODT0 | U3 | NVCC_DRAM | DDR | — | DRAM_ODT0 | Output | 100 k Ω pull-down |
| DRAM_RAS_B | H5 | NVCC_DRAM | DDR | — | DRAM_RAS_B | Output | 100 k Ω pull-up |
| DRAM_RESET | D4 | NVCC_DRAM | DDR | — | DRAM_RESET | Output | 100 k Ω pull-down |
| DRAM_SDBA0 | G3 | NVCC_DRAM | DDR | — | DRAM_SDBA0 | Output | 100 k Ω pull-up |
| DRAM_SDBA1 | P3 | NVCC_DRAM | DDR | — | DRAM_SDBA1 | Output | 100 k Ω pull-up |
| DRAM_SDBA2 | K4 | NVCC_DRAM | DDR | — | DRAM_SDBA2 | Output | 100 k Ω pull-up |
| DRAM_SDCKE0 | P5 | NVCC_DRAM | DDR | — | DRAM_SDCKE0 | Output | 100 k Ω pull-down |
| DRAM_SDCKE1 | E4 | NVCC_DRAM | DDR | — | DRAM_SDCKE1 | Output | 100 k Ω pull-down |
| DRAM_SDCLK0_N | L1 | NVCC_DRAM | DDRCLK | — | DRAM_SDCLK0_N | — | — |
| DRAM_SDCLK0_P | K1 | NVCC_DRAM | DDRCLK | — | DRAM_SDCLK0_P | Output | Low |
| DRAM_SDQS0_N | P2 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS0_N | — | — |
| DRAM_SDQS0_P | P1 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS0_P | Input | — |
| DRAM_SDQS1_N | H2 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS1_N | — | — |
| DRAM_SDQS1_P | G1 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS1_P | Input | — |
| DRAM_SDQS2_N | W1 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS2_N | — | — |
| DRAM_SDQS2_P | W2 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS2_P | Input | — |
| DRAM_SDQS3_N | B2 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS3_N | — | — |
| DRAM_SDQS3_P | B1 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS3_P | Input | — |

Table 117. 17x17 mm NP (No PCIe) Functional Contact Assignments (continued)

| Ball Name | 17x17 NP Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|--------------|---------------|-------------|-----------|------------------------|------------------|--------------|----------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| DRAM_SDWE_B | J5 | NVCC_DRAM | DDR | — | DRAM_SDWE_B | Output | 100 kΩ pull-up |
| ENET1_COL | B5 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO00 | Input | Keeper |
| ENET1_CRS | C6 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO01 | Input | Keeper |
| ENET1_MDC | B6 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO02 | Input | Keeper |
| ENET1_MDIO | A6 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO03 | Input | Keeper |
| ENET1_RX_CLK | A5 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO04 | Input | Keeper |
| ENET1_TX_CLK | F7 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO05 | Input | Keeper |
| ENET2_COL | E7 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO06 | Input | Keeper |
| ENET2_CRS | E6 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO07 | Input | Keeper |
| ENET2_RX_CLK | E5 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO08 | Input | Keeper |
| ENET2_TX_CLK | D5 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO09 | Input | Keeper |
| GPIO1_IO00 | C19 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO00 | Input | Keeper |
| GPIO1_IO01 | D19 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO01 | Input | Keeper |
| GPIO1_IO02 | C20 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO02 | Input | Keeper |
| GPIO1_IO03 | D20 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO03 | Input | Keeper |
| GPIO1_IO04 | A18 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO04 | Input | Keeper |
| GPIO1_IO05 | B18 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO05 | Input | Keeper |
| GPIO1_IO06 | D18 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO06 | Input | Keeper |
| GPIO1_IO07 | A17 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO07 | Input | Keeper |
| GPIO1_IO08 | B17 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO08 | Input | Keeper |
| GPIO1_IO09 | A19 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO09 | Input | Keeper |
| GPIO1_IO10 | B19 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO10 | Input | Keeper |
| GPIO1_IO11 | B20 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO11 | Input | Keeper |
| GPIO1_IO12 | B16 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO12 | Input | Keeper |
| GPIO1_IO13 | A16 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO13 | Input | Keeper |
| JTAG_MOD | R7 | NVCC_JTAG | GPIO | — | JTAG_MOD | Input | 100 kΩ pull-up |
| JTAG_TCK | R9 | NVCC_JTAG | GPIO | — | JTAG_TCK | Input | 47 kΩ pull-up |
| JTAG_TDI | R10 | NVCC_JTAG | GPIO | — | JTAG_TDI | Input | 47 kΩ pull-up |

Table 117. 17x17 mm NP (No PCIe) Functional Contact Assignments (continued)

| Ball Name | 17x17 NP Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|-------------|---------------|-------------|-----------|------------------------|------------------|--------------|---------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| JTAG_TDO | R8 | NVCC_JTAG | GPIO | — | JTAG_TDO | Output | Keeper |
| JTAG_TMS | T10 | NVCC_JTAG | GPIO | — | JTAG_TMS | Input | 47 kΩ pull-up |
| JTAG_TRST_B | T9 | NVCC_JTAG | GPIO | — | JTAG_TRST_B | Input | 47 kΩ pull-up |
| KEY_COL0 | G20 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO10 | Input | Keeper |
| KEY_COL1 | F20 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO11 | Input | Keeper |
| KEY_COL2 | G18 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO12 | Input | Keeper |
| KEY_COL3 | E20 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO13 | Input | Keeper |
| KEY_COL4 | E19 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO14 | Input | Keeper |
| KEY_ROW0 | F16 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO15 | Input | Keeper |
| KEY_ROW1 | E18 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO16 | Input | Keeper |
| KEY_ROW2 | F18 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO17 | Input | Keeper |
| KEY_ROW3 | F19 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO18 | Input | Keeper |
| KEY_ROW4 | G19 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO19 | Input | Keeper |
| LCD1_CLK | L17 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO00 | Input | Keeper |
| LCD1_DATA00 | M20 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO01 | Input | Keeper |
| LCD1_DATA01 | M18 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO02 | Input | Keeper |
| LCD1_DATA02 | M19 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO03 | Input | Keeper |
| LCD1_DATA03 | N19 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO04 | Input | Keeper |
| LCD1_DATA04 | N20 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO05 | Input | Keeper |
| LCD1_DATA05 | M16 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO06 | Input | Keeper |
| LCD1_DATA06 | M15 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO07 | Input | Keeper |
| LCD1_DATA07 | L20 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO08 | Input | Keeper |
| LCD1_DATA08 | K18 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO09 | Input | Keeper |
| LCD1_DATA09 | L16 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO10 | Input | Keeper |
| LCD1_DATA10 | L19 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO11 | Input | Keeper |
| LCD1_DATA11 | L15 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO12 | Input | Keeper |
| LCD1_DATA12 | K16 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO13 | Input | Keeper |
| LCD1_DATA13 | K15 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO14 | Input | Keeper |
| LCD1_DATA14 | K17 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO15 | Input | Keeper |
| LCD1_DATA15 | H16 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO16 | Input | Keeper |

Table 117. 17x17 mm NP (No PCIe) Functional Contact Assignments (continued)

| Ball Name | 17x17 NP Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|--------------|---------------|-------------|-----------|------------------------|------------------|--------------|----------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| LCD1_DATA16 | H20 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO17 | Input | Keeper |
| LCD1_DATA17 | K19 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO18 | Input | Keeper |
| LCD1_DATA18 | K20 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO19 | Input | Keeper |
| LCD1_DATA19 | J20 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO20 | Input | Keeper |
| LCD1_DATA20 | H17 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO21 | Input | Keeper |
| LCD1_DATA21 | G17 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO22 | Input | Keeper |
| LCD1_DATA22 | H19 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO23 | Input | Keeper |
| LCD1_DATA23 | G16 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO24 | Input | Keeper |
| LCD1_ENABLE | J19 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO25 | Input | Keeper |
| LCD1_HSYNC | J16 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO26 | Input | Keeper |
| LCD1_RESET | J18 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO27 | Input | Keeper |
| LCD1_VSYNC | J15 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO28 | Input | Keeper |
| NAND_ALE | W6 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO00 | Input | Keeper |
| NAND_CE0_B | U7 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO01 | Input | Keeper |
| NAND_CE1_B | V9 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO02 | Input | Keeper |
| NAND_CLE | T8 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO03 | Input | Keeper |
| NAND_DATA00 | V6 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO04 | Input | Keeper |
| NAND_DATA01 | W8 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO05 | Input | Keeper |
| NAND_DATA02 | Y7 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO06 | Input | Keeper |
| NAND_DATA03 | U5 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO07 | Input | Keeper |
| NAND_DATA04 | W7 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO08 | Input | Keeper |
| NAND_DATA05 | T5 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO09 | Input | Keeper |
| NAND_DATA06 | Y8 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO10 | Input | Keeper |
| NAND_DATA07 | T6 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO11 | Input | Keeper |
| NAND_RE_B | U8 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO12 | Input | Keeper |
| NAND_READY_B | Y6 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO13 | Input | Keeper |
| NAND_WE_B | T7 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO14 | Input | Keeper |
| NAND_WP_B | V7 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO15 | Input | Keeper |
| ONOFF | R15 | VDD_SNVS_IN | GPIO | — | ONOFF | Input | 100 kΩ pull-up |
| POR_B | R16 | VDD_SNVS_IN | GPIO | — | POR_B | Input | 100 kΩ pull-up |

Table 117. 17x17 mm NP (No PCIe) Functional Contact Assignments (continued)

| Ball Name | 17x17 NP Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|---------------|---------------------|----------------|--------------|------------------------|---------------------|------------------|--------|
| | | | | Default Mode | Default Function | Input/ Output | Value |
| QSPI1A_DATA0 | E15 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO16 | Input | Keeper |
| QSPI1A_DATA1 | C15 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO17 | Input | Keeper |
| QSPI1A_DATA2 | D14 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO18 | Input | Keeper |
| QSPI1A_DATA3 | E16 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO19 | Input | Keeper |
| QSPI1A_DQS | A13 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO20 | Input | Keeper |
| QSPI1A_SCLK | D17 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO21 | Input | Keeper |
| QSPI1A_SS0_B | C17 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO22 | Input | Keeper |
| QSPI1A_SS1_B | E17 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO23 | Input | Keeper |
| QSPI1B_DATA0 | B14 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO24 | Input | Keeper |
| QSPI1B_DATA1 | A14 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO25 | Input | Keeper |
| QSPI1B_DATA2 | D13 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO26 | Input | Keeper |
| QSPI1B_DATA3 | C13 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO27 | Input | Keeper |
| QSPI1B_DQS | B13 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO28 | Input | Keeper |
| QSPI1B_SCLK | B15 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO29 | Input | Keeper |
| QSPI1B_SS0_B | C14 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO30 | Input | Keeper |
| QSPI1B_SS1_B | A15 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO31 | Input | Keeper |
| RGIII1_RD0 | D8 | NVCC_RGIII1 | GPIO | ALT5 | GPIO5_IO00 | Input | Keeper |
| RGIII1_RD1 | C9 | NVCC_RGIII1 | GPIO | ALT5 | GPIO5_IO01 | Input | Keeper |
| RGIII1_RD2 | D7 | NVCC_RGIII1 | GPIO | ALT5 | GPIO5_IO02 | Input | Keeper |
| RGIII1_RD3 | E8 | NVCC_RGIII1 | GPIO | ALT5 | GPIO5_IO03 | Input | Keeper |
| RGIII1_RX_CTL | C10 | NVCC_RGIII1 | GPIO | ALT5 | GPIO5_IO04 | Input | Keeper |
| RGIII1_RXC | E9 | NVCC_RGIII1 | GPIO | ALT5 | GPIO5_IO05 | Input | Keeper |
| RGIII1_TD0 | D11 | NVCC_RGIII1 | GPIO | ALT5 | GPIO5_IO06 | Input | Keeper |
| RGIII1_TD1 | C12 | NVCC_RGIII1 | GPIO | ALT5 | GPIO5_IO07 | Input | Keeper |
| RGIII1_TD2 | E11 | NVCC_RGIII1 | GPIO | ALT5 | GPIO5_IO08 | Input | Keeper |
| RGIII1_TD3 | D10 | NVCC_RGIII1 | GPIO | ALT5 | GPIO5_IO09 | Input | Keeper |
| RGIII1_TX_CTL | E10 | NVCC_RGIII1 | GPIO | ALT5 | GPIO5_IO10 | Input | Keeper |
| RGIII1_TXC | C11 | NVCC_RGIII1 | GPIO | ALT5 | GPIO5_IO11 | Input | Keeper |
| RGIII2_RD0 | A8 | NVCC_RGIII2 | GPIO | ALT5 | GPIO5_IO12 | Input | Keeper |
| RGIII2_RD1 | B8 | NVCC_RGIII2 | GPIO | ALT5 | GPIO5_IO13 | Input | Keeper |
| RGIII2_RD2 | A7 | NVCC_RGIII2 | GPIO | ALT5 | GPIO5_IO14 | Input | Keeper |

Table 117. 17x17 mm NP (No PCIe) Functional Contact Assignments (continued)

| Ball Name | 17x17 NP Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|---------------|---------------|-----------------------|-----------|------------------------|------------------|--------------|---------------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| RGMII2_RD3 | B7 | NVCC_RGMII2 | GPIO | ALT5 | GPIO5_IO15 | Input | Keeper |
| RGMII2_RX_CTL | B9 | NVCC_RGMII2 | GPIO | ALT5 | GPIO5_IO16 | Input | Keeper |
| RGMII2_RXC | A9 | NVCC_RGMII2 | GPIO | ALT5 | GPIO5_IO17 | Input | Keeper |
| RGMII2_TD0 | A11 | NVCC_RGMII2 | GPIO | ALT5 | GPIO5_IO18 | Input | Keeper |
| RGMII2_TD1 | B11 | NVCC_RGMII2 | GPIO | ALT5 | GPIO5_IO19 | Input | Keeper |
| RGMII2_TD2 | A12 | NVCC_RGMII2 | GPIO | ALT5 | GPIO5_IO20 | Input | Keeper |
| RGMII2_TD3 | B12 | NVCC_RGMII2 | GPIO | ALT5 | GPIO5_IO21 | Input | Keeper |
| RGMII2_TX_CTL | B10 | NVCC_RGMII2 | GPIO | ALT5 | GPIO5_IO22 | Input | Keeper |
| RGMII2_TXC | A10 | NVCC_RGMII2 | GPIO | ALT5 | GPIO5_IO23 | Input | Keeper |
| RTC_XTALI | V19 | VDD_SNVS_CAP | — | — | RTC_XTALI | — | — |
| RTC_XTALO | V20 | VDD_SNVS_CAP | — | — | RTC_XTALO | — | — |
| SD2_CLK | E12 | NVCC_SD2 | GPIO | ALT5 | GPIO6_IO06 | Input | Keeper |
| SD2_CMD | F12 | NVCC_SD2 | GPIO | ALT5 | GPIO6_IO07 | Input | Keeper |
| SD2_DATA0 | E13 | NVCC_SD2 | GPIO | ALT5 | GPIO6_IO08 | Input | Keeper |
| SD2_DATA1 | E14 | NVCC_SD2 | GPIO | ALT5 | GPIO6_IO09 | Input | Keeper |
| SD2_DATA2 | F10 | NVCC_SD2 | GPIO | ALT5 | GPIO6_IO10 | Input | Keeper |
| SD2_DATA3 | F11 | NVCC_SD2 | GPIO | ALT5 | GPIO6_IO11 | Input | Keeper |
| SD3_CLK | V11 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO00 | Input | 100 kΩ pull-down |
| SD3_CMD | T13 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO01 | Input | 100 kΩ pull-down |
| SD3_DATA0 | U10 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO02 | Input | 100 kΩ pull-down |
| SD3_DATA1 | T11 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO03 | Input | 100 kΩ pull-down |
| SD3_DATA2 | V15 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO04 | Input | 100 kΩ pull-down |
| SD3_DATA3 | V14 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO05 | Input | 100 kΩ pull-down |
| SD3_DATA4 | U14 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO06 | Input | 100 kΩ pull-down |
| SD3_DATA5 | U13 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO07 | Input | 100 kΩ pull-down |

Table 117. 17x17 mm NP (No PCIe) Functional Contact Assignments (continued)

| Ball Name | 17x17 NP Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|------------------|---------------|-----------------------|-----------|------------------------|------------------|--------------|---------------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| SD3_DATA6 | V12 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO08 | Input | 100 kΩ pull-down |
| SD3_DATA7 | U11 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO09 | Input | 100 kΩ pull-down |
| SD4_CLK | W11 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO12 | Input | Keeper |
| SD4_CMD | W12 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO13 | Input | Keeper |
| SD4_DATA0 | Y9 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO14 | Input | Keeper |
| SD4_DATA1 | W9 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO15 | Input | Keeper |
| SD4_DATA2 | Y13 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO16 | Input | Keeper |
| SD4_DATA3 | W13 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO17 | Input | Keeper |
| SD4_DATA4 | Y12 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO18 | Input | Keeper |
| SD4_DATA5 | Y11 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO19 | Input | Keeper |
| SD4_DATA6 | Y10 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO20 | Input | Keeper |
| SD4_DATA7 | W10 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO21 | Input | Keeper |
| SD4_RESET_B | T12 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO22 | Input | Keeper |
| SNVS_PMIC_ON_REQ | P16 | VDD_SNVS_IN | GPIO | — | SNVS_PMIC_ON_REQ | Output | 100 kΩ pull-up |
| SNVS_TAMPER | P15 | VDD_SNVS_IN | GPIO | — | SNVS_TAMPER | Input | 100 kΩ pull-down |
| TEST_MODE | N14 | VDD_SNVS_IN | — | — | TEST_MODE | Input | 100 kΩ pull-down |
| USB_H_DATA | Y5 | NVCC_USB_H | GPIO | ALT5 | GPIO7_IO10 | Input | 100 kΩ pull-down |
| USB_H_STROBE | W5 | NVCC_USB_H | GPIO | ALT5 | GPIO7_IO11 | Input | 100 kΩ pull-down |
| USB_OTG1_CHD_B | W20 | VDD_USB_CAP | — | — | USB_OTG1_CHD_B | — | — |
| USB_OTG1_DN | W19 | VDD_USB_CAP | — | — | USB_OTG1_DN | — | — |
| USB_OTG1_DP | Y19 | VDD_USB_CAP | — | — | USB_OTG1_DP | — | — |
| USB_OTG2_DN | W17 | VDD_USB_CAP | — | — | USB_OTG2_DN | — | — |
| USB_OTG2_DP | Y17 | VDD_USB_CAP | — | — | USB_OTG2_DP | — | — |
| XTALI | T19 | NVCC_PLL | — | — | XTALI | — | — |
| XTALO | T20 | NVCC_PLL | — | — | XTALO | — | — |

Table 118. 17x17 mm (No PCIe), 0.8 mm Pitch, 20x20 Ball Map (continued)

| N | M | L | K | J | H |
|-------------------|-------------|---------------|---------------|-------------|--------------|
| DRAM_DATA07 | DRAM_DATA04 | DRAM_SDCLK0_N | DRAM_SDCLK0_P | DRAM_DATA12 | DRAM_DATA08 |
| DRAM_DQM0 | DRAM_DATA05 | DRAM_DATA06 | DRAM_DATA10 | DRAM_DATA11 | DRAM_SDQS1_N |
| VSS | DRAM_ADDR04 | VSS | VSS | DRAM_VREF | VSS |
| DRAM_ADDR11 | DRAM_ADDR13 | DRAM_ADDR00 | DRAM_SDBA2 | DRAM_CAS_B | DRAM_CS0_B |
| DRAM_ADDR10 | DRAM_ADDR08 | DRAM_ADDR09 | DRAM_ADDR02 | DRAM_SDWE_B | DRAM_RAS_B |
| NVCC_DRAM | NVCC_DRAM | NVCC_DRAM | NVCC_DRAM | NVCC_DRAM | NVCC_DRAM |
| VSS | VSS | VSS | NVCC_DRAM_2P5 | VSS | VSS |
| VDD_SOC_CAP | VDD_SOC_CAP | VDD_SOC_CAP | VDD_SOC_CAP | VDD_SOC_CAP | VDD_SOC_CAP |
| VDD_SOC_CAP | VDD_SOC_IN | VDD_SOC_IN | VDD_SOC_IN | VDD_SOC_IN | VDD_SOC_CAP |
| VDD_SOC_CAP | VDD_SOC_IN | VSS | VSS | VDD_ARM_IN | VDD_ARM_CAP |
| VDD_SOC_CAP | VDD_SOC_IN | VSS | VSS | VDD_ARM_IN | VDD_ARM_CAP |
| VDD_SOC_CAP | VDD_SOC_IN | VDD_ARM_IN | VDD_ARM_IN | VDD_ARM_IN | VDD_ARM_CAP |
| VSS | VDD_SOC_CAP | VDD_ARM_CAP | VDD_ARM_CAP | VDD_ARM_CAP | VDD_ARM_CAP |
| TEST_MODE | VSS | VSS | VSS | VSS | VSS |
| BOOT_MODE0 | LCD1_DATA06 | LCD1_DATA11 | LCD1_DATA13 | LCD1_VSYNC | NVCC_LCD1 |
| CCM_PMIC_STBY_REQ | LCD1_DATA05 | LCD1_DATA09 | LCD1_DATA12 | LCD1_HSYNC | LCD1_DATA15 |
| VDD_HIGH_CAP | VSS | LCD1_CLK | LCD1_DATA14 | VSS | LCD1_DATA20 |
| VDD_HIGH_CAP | LCD1_DATA01 | PCIE_VP_CAP | LCD1_DATA08 | LCD1_RESET | VDD_ARM_IN |
| LCD1_DATA03 | LCD1_DATA02 | LCD1_DATA10 | LCD1_DATA17 | LCD1_ENABLE | LCD1_DATA22 |
| LCD1_DATA04 | LCD1_DATA00 | LCD1_DATA07 | LCD1_DATA18 | LCD1_DATA19 | LCD1_DATA16 |
| N | M | L | K | J | H |

Table 118. 17x17 mm (No PCIe), 0.8 mm Pitch, 20x20 Ball Map (continued)

| | Y | W | V | U | T | R | P |
|----|--------------|----------------|-------------|---------------|---------------|--------------|------------------|
| 1 | VSS | DRAM_SDQS2_N | DRAM_DATA16 | DRAM_DATA22 | DRAM_DATA02 | DRAM_DATA00 | DRAM_SDQS0_P |
| 2 | DRAM_DATA21 | DRAM_SDQS2_P | DRAM_DATA23 | DRAM_DATA19 | DRAM_DATA01 | DRAM_DATA03 | DRAM_SDQS0_N |
| 3 | DRAM_DQM2 | DRAM_DATA20 | VSS | DRAM_ODT0 | VSS | VSS | DRAM_SDBA1 |
| 4 | DRAM_DATA18 | DRAM_DATA17 | VSS | DRAM_ADDR01 | DRAM_ADDR06 | DRAM_ADDR14 | DRAM_ADDR12 |
| 5 | USB_H_DATA | USB_H_STROBE | NVCC_USB_H | NAND_DATA03 | NAND_DATA05 | VSS | DRAM_SDCKE0 |
| 6 | NAND_READY_B | NAND_ALE | NAND_DATA00 | VSS | NAND_DATA07 | NVCC_NAND | NVCC_DRAM |
| 7 | NAND_DATA02 | NAND_DATA04 | NAND_WP_B | NAND_CE0_B | NAND_WE_B | JTAG_MOD | VSS |
| 8 | NAND_DATA06 | NAND_DATA01 | VDD_SOC_CAP | NAND_RE_B | NAND_CLE | JTAG_TDO | VSS |
| 9 | SD4_DATA0 | SD4_DATA1 | NAND_CE1_B | VSS | JTAG_TRST_B | JTAG_TCK | VSS |
| 10 | SD4_DATA6 | SD4_DATA7 | NVCC_SD4 | SD3_DATA0 | JTAG_TMS | JTAG_TDI | VSS |
| 11 | SD4_DATA5 | SD4_CLK | SD3_CLK | SD3_DATA7 | SD3_DATA1 | NVCC_JTAG | VSS |
| 12 | SD4_DATA4 | SD4_CMD | SD3_DATA6 | VSS | SD4_RESET_B | NVCC_HIGH | VSS |
| 13 | SD4_DATA2 | SD4_DATA3 | NVCC_LOW | SD3_DATA5 | SD3_CMD | VDDA_ADC_3P3 | NGND_KEL0 |
| 14 | ADC1_IN0 | ADC1_IN1 | SD3_DATA3 | SD3_DATA4 | CCM_CLK2 | ADC_VREFL | BOOT_MODE1 |
| 15 | ADC1_IN2 | ADC1_IN3 | SD3_DATA2 | VSS | GPANAIO | ONOFF | SNVS_TAMPER |
| 16 | ADC2_IN0 | ADC2_IN1 | ADC_VREFH | ADC2_IN3 | ADC2_IN2 | POR_B | SNVS_PMIC_ON_REQ |
| 17 | USB_OTG2_DP | USB_OTG2_DN | VDD_USB_CAP | USB_OTG2_VBUS | USB_OTG1_VBUS | VSS | VDD_HIGH_IN |
| 18 | VSS | VSS | VSS | NVCC_PLL | VDD_SNV5_CAP | VDD_SNV5_IN | VDD_HIGH_IN |
| 19 | USB_OTG1_DP | USB_OTG1_DN | RTC_XTALI | VSS | XTALI | VSS | CCM_CLK1_N |
| 20 | VSS | USB_OTG1_CHD_B | RTC_XTALO | VSS | XTALO | VSS | CCM_CLK1_P |
| | Y | W | V | U | T | R | P |

6.4.5 17x17 mm WP (with PCIe) Supplies Contact Assignments and Functional Contact Assignments

Table 119 shows supplies contact assignments for the 17x17 mm WP (with PCIe) package.

Table 119. 17x17 mm WP (with PCIe) Supplies Contact Assignments

| Supply Rail Name | 17x17 WP [with PCIe] Ball(s) Position(s) | Remark |
|------------------|--|---|
| DRAM_VREF | J3 | DDR voltage reference input. Connect to a voltage source that is 50% of NVCC_DRAM. |
| DRAM_ZQPAD | C5 | DDR output buffer driver calibration reference voltage input. Connect DRAM_ZQPAD to an external 240 ohm 1% resistor to Vss. |
| GPANAIO | U16 | Analog output for NXP use only. This output must always be left unconnected. |
| NGND_KELO | P13 | Connect to Vss |
| NVCC_DRAM | G6, H6, J6, K6, L6, M6, N6, P6 | Supply input for the DDR I/O interface |
| NVCC_DRAM_2P5 | K7 | Supply input for the DDR interface |
| NVCC_ENET | F6 | Supply input for the ENET interfaces |
| NVCC_GPIO | F15 | Supply input for the GPIO interface |
| NVCC_HIGH | R12 | 3.3 V Supply input for the dual-voltage I/Os on the SD3 interface |
| NVCC_JTAG | R11 | Supply input for the JTAG interface |
| NVCC_KEY | G15 | Supply input for the Key Pad Port (KPP) interface |
| NVCC_LCD1 | H15 | Supply input for the LCD interface |
| NVCC_LOW | V13 | 1.8 V Supply input for the dual-voltage I/Os on the SD3 interface |
| NVCC_NAND | R6 | Supply input for the Raw NAND flash memories interface |
| NVCC_PLL | W20 | Supply input for the PLLs |
| NVCC_QSPI | F14 | Supply input for the QSPI interface |
| NVCC_RGMII1 | F8 | Supply input for the RGMII1 interface |
| NVCC_RGMII2 | F9 | Supply input for the RGMII2 interface |
| NVCC_SD2 | F13 | Supply input for the SD2 interface |
| NVCC_SD4 | V10 | Supply input for the SD4 interface |
| NVCC_USB_H | V5 | Supply input for the USB HSIC interface |
| PCIE_REXT | N18 | PCIe impedance calibration resistor. Connect PCIE_REXT to an external 200 ohm 1% resistor to Vss. |
| PCIE_VP | P18 | Supply input for the PCIe PHY |
| PCIE_VPH | R18 | Supply input for the PCIe PHY |
| PCIE_VPTX | P17 | Supply input for the PCIe PHY |

Table 119. 17x17 mm WP (with PCIe) Supplies Contact Assignments (continued)

| Supply Rail Name | 17x17 WP [with PCIe] Ball(s) Position(s) | Remark |
|------------------|---|--|
| USB_OTG1_VBUS | T16 | VBUS input for USB_OTG1 |
| USB_OTG2_VBUS | T15 | VBUS input for USB_OTG2 |
| VDD_ARM_CAP | C16, D16, H10, H11, H12, H13, J13, K13, L13 | Supply voltage output from internal LDO_ARM. Requires external capacitor(s). |
| VDD_ARM_IN | H18, J10, J11, J12, K12, L12 | Supply voltage input for internal LDO_ARM. |
| VDD_HIGH_CAP | V17, V18 | Supply voltage output from internal LDO_2P5. Requires external capacitor(s). |
| VDD_HIGH_IN | U17, U18 | Supply voltage input to internal LDO_2P5, LDO_1P1 and LDO_SNVS. |
| VDD_SNVS_CAP | V16 | Supply voltage output from internal LDO_SNVS. Requires external capacitor(s). |
| VDD_SNVS_IN | T18 | Supply voltage input to the SNVS voltage domain |
| VDD_SOC_CAP | H8, H9, J8, K8, L8, M8, M13, N8, N9, N10, N11, N12, V8 | Supply voltage output from internal LDO_SOC. Requires external capacitor(s). |
| VDD_SOC_IN | C7, C8, J9, K9, L9, M9, M10, M11, M12 | Supply voltage input to internal LDO_SOC and LDO_PCIE |
| VDD_USB_CAP | V15 | Supply voltage output from internal LDO_USB. Requires external capacitor(s). |
| VDDA_ADC_3P3 | R13 | Supply voltage input to the ADC. This supply must be provided even if the ADC is not used. |
| VSS | A1, A20, C3, C4, C18, D6, D9, D12, D15, E3, F3, F5, F17, G7, G8, G9, G10, G11, G12, G13, G14, H3, H7, H14, J7, J14, J17, K3, K10, K11, K14, L3, L7, L10, L11, L14, M7, M14, M17, N3, N7, N13, N19, N20, P7, P8, P9, P10, P11, P12, R3, R5, R17, T3, T19, T20, U6, U9, U12, U15, V3, V4, W16, W18, Y1, Y16, Y18, Y20 | Ground |

Table 120 shows an alpha-sorted list of functional contact assignments for the 17x17 mm WP (with PCIe) package.

Table 120. 17x17 WP (with PCIe) Functional Contact Assignments

| Ball Name | 17x17 WP Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|-----------|---------------|--------------|-----------|------------------------|------------------|--------------|-------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| ADC1_IN0 | Y14 | VDDA_ADC_3P3 | — | — | ADC1_IN0 | Input | — |
| ADC1_IN1 | W14 | VDDA_ADC_3P3 | — | — | ADC1_IN1 | Input | — |

Table 120. 17x17 WP (with PCIe) Functional Contact Assignments (continued)

| Ball Name | 17x17 WP Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|-------------------|---------------|--------------|-----------|------------------------|-------------------|--------------|--------------------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| BOOT_MODE0 | U20 | VDD_SNVIS_IN | GPIO | — | BOOT_MODE0 | Input | 100 k Ω pull-down |
| BOOT_MODE1 | U19 | VDD_SNVIS_IN | GPIO | — | BOOT_MODE1 | Input | 100 k Ω pull-down |
| CCM_CLK1_N | P16 | VDD_HIGH_CAP | — | — | CCM_CLK1_N | — | — |
| CCM_CLK1_P | R16 | VDD_HIGH_CAP | — | — | CCM_CLK1_P | — | — |
| CCM_CLK2 | R15 | VDD_HIGH_CAP | — | — | CCM_CLK2 | — | — |
| CCM_PMIC_STBY_REQ | P15 | VDD_SNVIS_IN | GPIO | — | CCM_PMIC_STBY_REQ | Output | 0 |
| DRAM_ADDR00 | L4 | NVCC_DRAM | DDR | — | DRAM_ADDR00 | Output | 100 k Ω pull-up |
| DRAM_ADDR01 | U4 | NVCC_DRAM | DDR | — | DRAM_ADDR01 | Output | 100 k Ω pull-up |
| DRAM_ADDR02 | K5 | NVCC_DRAM | DDR | — | DRAM_ADDR02 | Output | 100 k Ω pull-up |
| DRAM_ADDR03 | G5 | NVCC_DRAM | DDR | — | DRAM_ADDR03 | Output | 100 k Ω pull-up |
| DRAM_ADDR04 | M3 | NVCC_DRAM | DDR | — | DRAM_ADDR04 | Output | 100 k Ω pull-up |
| DRAM_ADDR05 | G4 | NVCC_DRAM | DDR | — | DRAM_ADDR05 | Output | 100 k Ω pull-up |
| DRAM_ADDR06 | T4 | NVCC_DRAM | DDR | — | DRAM_ADDR06 | Output | 100 k Ω pull-up |
| DRAM_ADDR07 | F4 | NVCC_DRAM | DDR | — | DRAM_ADDR07 | Output | 100 k Ω pull-up |
| DRAM_ADDR08 | M5 | NVCC_DRAM | DDR | — | DRAM_ADDR08 | Output | 100 k Ω pull-up |
| DRAM_ADDR09 | L5 | NVCC_DRAM | DDR | — | DRAM_ADDR09 | Output | 100 k Ω pull-up |
| DRAM_ADDR10 | N5 | NVCC_DRAM | DDR | — | DRAM_ADDR10 | Output | 100 k Ω pull-up |
| DRAM_ADDR11 | N4 | NVCC_DRAM | DDR | — | DRAM_ADDR11 | Output | 100 k Ω pull-up |
| DRAM_ADDR12 | P4 | NVCC_DRAM | DDR | — | DRAM_ADDR12 | Output | 100 k Ω pull-up |
| DRAM_ADDR13 | M4 | NVCC_DRAM | DDR | — | DRAM_ADDR13 | Output | 100 k Ω pull-up |

Table 120. 17x17 WP (with PCIe) Functional Contact Assignments (continued)

| Ball Name | 17x17 WP Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|-------------|---------------|-------------|-----------|------------------------|------------------|--------------|----------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| DRAM_ADDR14 | R4 | NVCC_DRAM | DDR | — | DRAM_ADDR14 | Output | 100 kΩ pull-up |
| DRAM_CAS_B | J4 | NVCC_DRAM | DDR | — | DRAM_CAS_B | Output | 100 kΩ pull-up |
| DRAM_CS0_B | H4 | NVCC_DRAM | DDR | — | DRAM_CS0_B | Output | 100 kΩ pull-up |
| DRAM_CS1_B | D3 | NVCC_DRAM | DDR | — | DRAM_CS1_B | Output | 100 kΩ pull-up |
| DRAM_DATA00 | R1 | NVCC_DRAM | DDR | — | DRAM_DATA00 | Input | 100 kΩ pull-up |
| DRAM_DATA01 | T2 | NVCC_DRAM | DDR | — | DRAM_DATA01 | Input | 100 kΩ pull-up |
| DRAM_DATA02 | T1 | NVCC_DRAM | DDR | — | DRAM_DATA02 | Input | 100 kΩ pull-up |
| DRAM_DATA03 | R2 | NVCC_DRAM | DDR | — | DRAM_DATA03 | Input | 100 kΩ pull-up |
| DRAM_DATA04 | M1 | NVCC_DRAM | DDR | — | DRAM_DATA04 | Input | 100 kΩ pull-up |
| DRAM_DATA05 | M2 | NVCC_DRAM | DDR | — | DRAM_DATA05 | Input | 100 kΩ pull-up |
| DRAM_DATA06 | L2 | NVCC_DRAM | DDR | — | DRAM_DATA06 | Input | 100 kΩ pull-up |
| DRAM_DATA07 | N1 | NVCC_DRAM | DDR | — | DRAM_DATA07 | Input | 100 kΩ pull-up |
| DRAM_DATA08 | H1 | NVCC_DRAM | DDR | — | DRAM_DATA08 | Input | 100 kΩ pull-up |
| DRAM_DATA09 | F2 | NVCC_DRAM | DDR | — | DRAM_DATA09 | Input | 100 kΩ pull-up |
| DRAM_DATA10 | K2 | NVCC_DRAM | DDR | — | DRAM_DATA10 | Input | 100 kΩ pull-up |
| DRAM_DATA11 | J2 | NVCC_DRAM | DDR | — | DRAM_DATA11 | Input | 100 kΩ pull-up |
| DRAM_DATA12 | J1 | NVCC_DRAM | DDR | — | DRAM_DATA12 | Input | 100 kΩ pull-up |
| DRAM_DATA13 | F1 | NVCC_DRAM | DDR | — | DRAM_DATA13 | Input | 100 kΩ pull-up |
| DRAM_DATA14 | E2 | NVCC_DRAM | DDR | — | DRAM_DATA14 | Input | 100 kΩ pull-up |

Table 120. 17x17 WP (with PCIe) Functional Contact Assignments (continued)

| Ball Name | 17x17 WP Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|-------------|---------------|-------------|-----------|------------------------|------------------|--------------|------------------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| DRAM_DATA15 | E1 | NVCC_DRAM | DDR | — | DRAM_DATA15 | Input | 100 k Ω pull-up |
| DRAM_DATA16 | V1 | NVCC_DRAM | DDR | — | DRAM_DATA16 | Input | 100 k Ω pull-up |
| DRAM_DATA17 | W4 | NVCC_DRAM | DDR | — | DRAM_DATA17 | Input | 100 k Ω pull-up |
| DRAM_DATA18 | Y4 | NVCC_DRAM | DDR | — | DRAM_DATA18 | Input | 100 k Ω pull-up |
| DRAM_DATA19 | U2 | NVCC_DRAM | DDR | — | DRAM_DATA19 | Input | 100 k Ω pull-up |
| DRAM_DATA20 | W3 | NVCC_DRAM | DDR | — | DRAM_DATA20 | Input | 100 k Ω pull-up |
| DRAM_DATA21 | Y2 | NVCC_DRAM | DDR | — | DRAM_DATA21 | Input | 100 k Ω pull-up |
| DRAM_DATA22 | U1 | NVCC_DRAM | DDR | — | DRAM_DATA22 | Input | 100 k Ω pull-up |
| DRAM_DATA23 | V2 | NVCC_DRAM | DDR | — | DRAM_DATA23 | Input | 100 k Ω pull-up |
| DRAM_DATA24 | A2 | NVCC_DRAM | DDR | — | DRAM_DATA24 | Input | 100 k Ω pull-up |
| DRAM_DATA25 | D1 | NVCC_DRAM | DDR | — | DRAM_DATA25 | Input | 100 k Ω pull-up |
| DRAM_DATA26 | C1 | NVCC_DRAM | DDR | — | DRAM_DATA26 | Input | 100 k Ω pull-up |
| DRAM_DATA27 | D2 | NVCC_DRAM | DDR | — | DRAM_DATA27 | Input | 100 k Ω pull-up |
| DRAM_DATA28 | C2 | NVCC_DRAM | DDR | — | DRAM_DATA28 | Input | 100 k Ω pull-up |
| DRAM_DATA29 | B3 | NVCC_DRAM | DDR | — | DRAM_DATA29 | Input | 100 k Ω pull-up |
| DRAM_DATA30 | B4 | NVCC_DRAM | DDR | — | DRAM_DATA30 | Input | 100 k Ω pull-up |
| DRAM_DATA31 | A4 | NVCC_DRAM | DDR | — | DRAM_DATA31 | Input | 100 k Ω pull-up |
| DRAM_DQM0 | N2 | NVCC_DRAM | DDR | — | DRAM_DQM0 | Output | 100 k Ω pull-up |
| DRAM_DQM1 | G2 | NVCC_DRAM | DDR | — | DRAM_DQM1 | Output | 100 k Ω pull-up |

Table 120. 17x17 WP (with PCIe) Functional Contact Assignments (continued)

| Ball Name | 17x17 WP Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|---------------|---------------|-------------|-----------|------------------------|------------------|--------------|------------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| DRAM_DQM2 | Y3 | NVCC_DRAM | DDR | — | DRAM_DQM2 | Output | 100 kΩ pull-up |
| DRAM_DQM3 | A3 | NVCC_DRAM | DDR | — | DRAM_DQM3 | Output | 100 kΩ pull-up |
| DRAM_ODT0 | U3 | NVCC_DRAM | DDR | — | DRAM_ODT0 | Output | 100 kΩ pull-down |
| DRAM_RAS_B | H5 | NVCC_DRAM | DDR | — | DRAM_RAS_B | Output | 100 kΩ pull-up |
| DRAM_RESET | D4 | NVCC_DRAM | DDR | — | DRAM_RESET | Output | 100 kΩ pull-down |
| DRAM_SDBA0 | G3 | NVCC_DRAM | DDR | — | DRAM_SDBA0 | Output | 100 kΩ pull-up |
| DRAM_SDBA1 | P3 | NVCC_DRAM | DDR | — | DRAM_SDBA1 | Output | 100 kΩ pull-up |
| DRAM_SDBA2 | K4 | NVCC_DRAM | DDR | — | DRAM_SDBA2 | Output | 100 kΩ pull-up |
| DRAM_SDCKE0 | P5 | NVCC_DRAM | DDR | — | DRAM_SDCKE0 | Output | 100 kΩ pull-down |
| DRAM_SDCKE1 | E4 | NVCC_DRAM | DDR | — | DRAM_SDCKE1 | Output | 100 kΩ pull-down |
| DRAM_SDCLK0_N | L1 | NVCC_DRAM | DDRCLK | — | DRAM_SDCLK0_N | — | — |
| DRAM_SDCLK0_P | K1 | NVCC_DRAM | DDRCLK | — | DRAM_SDCLK0_P | Output | Low |
| DRAM_SDQS0_N | P2 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS0_N | — | — |
| DRAM_SDQS0_P | P1 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS0_P | Input | — |
| DRAM_SDQS1_N | H2 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS1_N | — | — |
| DRAM_SDQS1_P | G1 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS1_P | Input | — |
| DRAM_SDQS2_N | W1 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS2_N | — | — |
| DRAM_SDQS2_P | W2 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS2_P | Input | — |
| DRAM_SDQS3_N | B2 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS3_N | — | — |
| DRAM_SDQS3_P | B1 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS3_P | Input | — |
| DRAM_SDWE_B | J5 | NVCC_DRAM | DDR | — | DRAM_SDWE_B | Output | 100 kΩ pull-up |
| ENET1_COL | B5 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO00 | Input | Keeper |
| ENET1_CRS | C6 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO01 | Input | Keeper |
| ENET1_MDC | B6 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO02 | Input | Keeper |

Table 120. 17x17 WP (with PCIe) Functional Contact Assignments (continued)

| Ball Name | 17x17 WP Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|--------------|---------------|-------------|-----------|------------------------|------------------|--------------|----------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| ENET1_MDIO | A6 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO03 | Input | Keeper |
| ENET1_RX_CLK | A5 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO04 | Input | Keeper |
| ENET1_TX_CLK | F7 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO05 | Input | Keeper |
| ENET2_COL | E7 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO06 | Input | Keeper |
| ENET2_CRS | E6 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO07 | Input | Keeper |
| ENET2_RX_CLK | E5 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO08 | Input | Keeper |
| ENET2_TX_CLK | D5 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO09 | Input | Keeper |
| GPIO1_IO00 | C19 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO00 | Input | Keeper |
| GPIO1_IO01 | D19 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO01 | Input | Keeper |
| GPIO1_IO02 | C20 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO02 | Input | Keeper |
| GPIO1_IO03 | D20 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO03 | Input | Keeper |
| GPIO1_IO04 | A18 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO04 | Input | Keeper |
| GPIO1_IO05 | B18 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO05 | Input | Keeper |
| GPIO1_IO06 | D18 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO06 | Input | Keeper |
| GPIO1_IO07 | A17 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO07 | Input | Keeper |
| GPIO1_IO08 | B17 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO08 | Input | Keeper |
| GPIO1_IO09 | A19 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO09 | Input | Keeper |
| GPIO1_IO10 | B19 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO10 | Input | Keeper |
| GPIO1_IO11 | B20 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO11 | Input | Keeper |
| GPIO1_IO12 | B16 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO12 | Input | Keeper |
| GPIO1_IO13 | A16 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO13 | Input | Keeper |
| JTAG_MOD | R7 | NVCC_JTAG | GPIO | — | JTAG_MOD | Input | 100 kΩ pull-up |
| JTAG_TCK | R9 | NVCC_JTAG | GPIO | — | JTAG_TCK | Input | 47 kΩ pull-up |
| JTAG_TDI | R10 | NVCC_JTAG | GPIO | — | JTAG_TDI | Input | 47 kΩ pull-up |
| JTAG_TDO | R8 | NVCC_JTAG | GPIO | — | JTAG_TDO | Output | Keeper |
| JTAG_TMS | T10 | NVCC_JTAG | GPIO | — | JTAG_TMS | Input | 47 kΩ pull-up |
| JTAG_TRST_B | T9 | NVCC_JTAG | GPIO | — | JTAG_TRST_B | Input | 47 kΩ pull-up |
| KEY_COL0 | G20 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO10 | Input | Keeper |

Table 120. 17x17 WP (with PCIe) Functional Contact Assignments (continued)

| Ball Name | 17x17 WP Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|-------------|---------------|-------------|-----------|------------------------|------------------|--------------|--------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| KEY_COL1 | F20 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO11 | Input | Keeper |
| KEY_COL2 | G18 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO12 | Input | Keeper |
| KEY_COL3 | E20 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO13 | Input | Keeper |
| KEY_COL4 | E19 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO14 | Input | Keeper |
| KEY_ROW0 | F16 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO15 | Input | Keeper |
| KEY_ROW1 | E18 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO16 | Input | Keeper |
| KEY_ROW2 | F18 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO17 | Input | Keeper |
| KEY_ROW3 | F19 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO18 | Input | Keeper |
| KEY_ROW4 | G19 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO19 | Input | Keeper |
| LCD1_CLK | L17 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO00 | Input | Keeper |
| LCD1_DATA00 | M20 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO01 | Input | Keeper |
| LCD1_DATA01 | L18 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO02 | Input | Keeper |
| LCD1_DATA02 | M19 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO03 | Input | Keeper |
| LCD1_DATA03 | M18 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO04 | Input | Keeper |
| LCD1_DATA04 | N17 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO05 | Input | Keeper |
| LCD1_DATA05 | M16 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO06 | Input | Keeper |
| LCD1_DATA06 | M15 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO07 | Input | Keeper |
| LCD1_DATA07 | L20 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO08 | Input | Keeper |
| LCD1_DATA08 | K18 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO09 | Input | Keeper |
| LCD1_DATA09 | L16 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO10 | Input | Keeper |
| LCD1_DATA10 | L19 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO11 | Input | Keeper |
| LCD1_DATA11 | L15 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO12 | Input | Keeper |
| LCD1_DATA12 | K16 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO13 | Input | Keeper |
| LCD1_DATA13 | K15 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO14 | Input | Keeper |
| LCD1_DATA14 | K17 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO15 | Input | Keeper |
| LCD1_DATA15 | H16 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO16 | Input | Keeper |
| LCD1_DATA16 | H20 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO17 | Input | Keeper |
| LCD1_DATA17 | K19 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO18 | Input | Keeper |
| LCD1_DATA18 | K20 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO19 | Input | Keeper |
| LCD1_DATA19 | J20 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO20 | Input | Keeper |
| LCD1_DATA20 | H17 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO21 | Input | Keeper |

Table 120. 17x17 WP (with PCIe) Functional Contact Assignments (continued)

| Ball Name | 17x17 WP Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|--------------|---------------|-------------|-----------|------------------------|------------------|--------------|----------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| LCD1_DATA21 | G17 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO22 | Input | Keeper |
| LCD1_DATA22 | H19 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO23 | Input | Keeper |
| LCD1_DATA23 | G16 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO24 | Input | Keeper |
| LCD1_ENABLE | J19 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO25 | Input | Keeper |
| LCD1_HSYNC | J16 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO26 | Input | Keeper |
| LCD1_RESET | J18 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO27 | Input | Keeper |
| LCD1_VSYNC | J15 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO28 | Input | Keeper |
| NAND_ALE | W6 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO00 | Input | Keeper |
| NAND_CE0_B | U7 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO01 | Input | Keeper |
| NAND_CE1_B | V9 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO02 | Input | Keeper |
| NAND_CLE | T8 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO03 | Input | Keeper |
| NAND_DATA00 | V6 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO04 | Input | Keeper |
| NAND_DATA01 | W8 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO05 | Input | Keeper |
| NAND_DATA02 | Y7 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO06 | Input | Keeper |
| NAND_DATA03 | U5 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO07 | Input | Keeper |
| NAND_DATA04 | W7 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO08 | Input | Keeper |
| NAND_DATA05 | T5 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO09 | Input | Keeper |
| NAND_DATA06 | Y8 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO10 | Input | Keeper |
| NAND_DATA07 | T6 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO11 | Input | Keeper |
| NAND_RE_B | U8 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO12 | Input | Keeper |
| NAND_READY_B | Y6 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO13 | Input | Keeper |
| NAND_WE_B | T7 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO14 | Input | Keeper |
| NAND_WP_B | V7 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO15 | Input | Keeper |
| ONOFF | N15 | VDD_SNVS_IN | GPIO | — | ONOFF | Input | 100 kΩ pull-up |
| PCIE_RX_N | P19 | PCIE_VPH | — | — | PCIE_RX_N | — | — |
| PCIE_RX_P | P20 | PCIE_VPH | — | — | PCIE_RX_P | — | — |
| PCIE_TX_N | R19 | PCIE_VPH | — | — | PCIE_TX_N | — | — |
| PCIE_TX_P | R20 | PCIE_VPH | — | — | PCIE_TX_P | — | — |
| POR_B | P14 | VDD_SNVS_IN | GPIO | — | POR_B | Input | 100 kΩ pull-up |
| QSPI1A_DATA0 | E15 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO16 | Input | Keeper |

Table 120. 17x17 WP (with PCIe) Functional Contact Assignments (continued)

| Ball Name | 17x17 WP Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|--------------|---------------|-------------|-----------|------------------------|------------------|--------------|--------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| QSPI1A_DATA1 | C15 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO17 | Input | Keeper |
| QSPI1A_DATA2 | D14 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO18 | Input | Keeper |
| QSPI1A_DATA3 | E16 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO19 | Input | Keeper |
| QSPI1A_DQS | A13 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO20 | Input | Keeper |
| QSPI1A_SCLK | D17 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO21 | Input | Keeper |
| QSPI1A_SS0_B | C17 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO22 | Input | Keeper |
| QSPI1A_SS1_B | E17 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO23 | Input | Keeper |
| QSPI1B_DATA0 | B14 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO24 | Input | Keeper |
| QSPI1B_DATA1 | A14 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO25 | Input | Keeper |
| QSPI1B_DATA2 | D13 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO26 | Input | Keeper |
| QSPI1B_DATA3 | C13 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO27 | Input | Keeper |
| QSPI1B_DQS | B13 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO28 | Input | Keeper |
| QSPI1B_SCLK | B15 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO29 | Input | Keeper |
| QSPI1B_SS0_B | C14 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO30 | Input | Keeper |
| QSPI1B_SS1_B | A15 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO31 | Input | Keeper |
| RGMI1_RD0 | D8 | NVCC_RGMI1 | GPIO | ALT5 | GPIO5_IO00 | Input | Keeper |
| RGMI1_RD1 | C9 | NVCC_RGMI1 | GPIO | ALT5 | GPIO5_IO01 | Input | Keeper |
| RGMI1_RD2 | D7 | NVCC_RGMI1 | GPIO | ALT5 | GPIO5_IO02 | Input | Keeper |
| RGMI1_RD3 | E8 | NVCC_RGMI1 | GPIO | ALT5 | GPIO5_IO03 | Input | Keeper |
| RGMI1_RX_CTL | C10 | NVCC_RGMI1 | GPIO | ALT5 | GPIO5_IO04 | Input | Keeper |
| RGMI1_RXC | E9 | NVCC_RGMI1 | GPIO | ALT5 | GPIO5_IO05 | Input | Keeper |
| RGMI1_TD0 | D11 | NVCC_RGMI1 | GPIO | ALT5 | GPIO5_IO06 | Input | Keeper |
| RGMI1_TD1 | C12 | NVCC_RGMI1 | GPIO | ALT5 | GPIO5_IO07 | Input | Keeper |
| RGMI1_TD2 | E11 | NVCC_RGMI1 | GPIO | ALT5 | GPIO5_IO08 | Input | Keeper |
| RGMI1_TD3 | D10 | NVCC_RGMI1 | GPIO | ALT5 | GPIO5_IO09 | Input | Keeper |
| RGMI1_TX_CTL | E10 | NVCC_RGMI1 | GPIO | ALT5 | GPIO5_IO10 | Input | Keeper |
| RGMI1_TXC | C11 | NVCC_RGMI1 | GPIO | ALT5 | GPIO5_IO11 | Input | Keeper |
| RGMI2_RD0 | A8 | NVCC_RGMI2 | GPIO | ALT5 | GPIO5_IO12 | Input | Keeper |
| RGMI2_RD1 | B8 | NVCC_RGMI2 | GPIO | ALT5 | GPIO5_IO13 | Input | Keeper |
| RGMI2_RD2 | A7 | NVCC_RGMI2 | GPIO | ALT5 | GPIO5_IO14 | Input | Keeper |
| RGMI2_RD3 | B7 | NVCC_RGMI2 | GPIO | ALT5 | GPIO5_IO15 | Input | Keeper |

Table 120. 17x17 WP (with PCIe) Functional Contact Assignments (continued)

| Ball Name | 17x17 WP Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|--------------|---------------|-----------------------|-----------|------------------------|------------------|--------------|-----------------------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| RGMI2_RX_CTL | B9 | NVCC_RGMI2 | GPIO | ALT5 | GPIO5_IO16 | Input | Keeper |
| RGMI2_RXC | A9 | NVCC_RGMI2 | GPIO | ALT5 | GPIO5_IO17 | Input | Keeper |
| RGMI2_TD0 | A11 | NVCC_RGMI2 | GPIO | ALT5 | GPIO5_IO18 | Input | Keeper |
| RGMI2_TD1 | B11 | NVCC_RGMI2 | GPIO | ALT5 | GPIO5_IO19 | Input | Keeper |
| RGMI2_TD2 | A12 | NVCC_RGMI2 | GPIO | ALT5 | GPIO5_IO20 | Input | Keeper |
| RGMI2_TD3 | B12 | NVCC_RGMI2 | GPIO | ALT5 | GPIO5_IO21 | Input | Keeper |
| RGMI2_TX_CTL | B10 | NVCC_RGMI2 | GPIO | ALT5 | GPIO5_IO22 | Input | Keeper |
| RGMI2_TXC | A10 | NVCC_RGMI2 | GPIO | ALT5 | GPIO5_IO23 | Input | Keeper |
| RTC_XTALI | W19 | VDD_SNV5_CAP | — | — | RTC_XTALI | — | — |
| RTC_XTALO | Y19 | VDD_SNV5_CAP | — | — | RTC_XTALO | — | — |
| SD2_CLK | E12 | NVCC_SD2 | GPIO | ALT5 | GPIO6_IO06 | Input | Keeper |
| SD2_CMD | F12 | NVCC_SD2 | GPIO | ALT5 | GPIO6_IO07 | Input | Keeper |
| SD2_DATA0 | E13 | NVCC_SD2 | GPIO | ALT5 | GPIO6_IO08 | Input | Keeper |
| SD2_DATA1 | E14 | NVCC_SD2 | GPIO | ALT5 | GPIO6_IO09 | Input | Keeper |
| SD2_DATA2 | F10 | NVCC_SD2 | GPIO | ALT5 | GPIO6_IO10 | Input | Keeper |
| SD2_DATA3 | F11 | NVCC_SD2 | GPIO | ALT5 | GPIO6_IO11 | Input | Keeper |
| SD3_CLK | V11 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO00 | Input | 100 k Ω pull-down |
| SD3_CMD | T13 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO01 | Input | 100 k Ω pull-down |
| SD3_DATA0 | U10 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO02 | Input | 100 k Ω pull-down |
| SD3_DATA1 | T11 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO03 | Input | 100 k Ω pull-down |
| SD3_DATA2 | U14 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO04 | Input | 100 k Ω pull-down |
| SD3_DATA3 | V14 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO05 | Input | 100 k Ω pull-down |
| SD3_DATA4 | T14 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO06 | Input | 100 k Ω pull-down |
| SD3_DATA5 | U13 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO07 | Input | 100 k Ω pull-down |
| SD3_DATA6 | V12 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO08 | Input | 100 k Ω pull-down |

Table 120. 17x17 WP (with PCIe) Functional Contact Assignments (continued)

| Ball Name | 17x17 WP Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|------------------|---------------|-----------------------|-----------|------------------------|------------------|--------------|-----------------------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| SD3_DATA7 | U11 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO09 | Input | 100 k Ω pull-down |
| SD4_CLK | W11 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO12 | Input | Keeper |
| SD4_CMD | W12 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO13 | Input | Keeper |
| SD4_DATA0 | Y9 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO14 | Input | Keeper |
| SD4_DATA1 | W9 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO15 | Input | Keeper |
| SD4_DATA2 | Y13 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO16 | Input | Keeper |
| SD4_DATA3 | W13 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO17 | Input | Keeper |
| SD4_DATA4 | Y12 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO18 | Input | Keeper |
| SD4_DATA5 | Y11 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO19 | Input | Keeper |
| SD4_DATA6 | Y10 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO20 | Input | Keeper |
| SD4_DATA7 | W10 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO21 | Input | Keeper |
| SD4_RESET_B | T12 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO22 | Input | Keeper |
| SNVS_PMIC_ON_REQ | N16 | VDD_SNVS_IN | GPIO | — | SNVS_PMIC_ON_REQ | Output | 100 k Ω pull-up |
| SNVS_TAMPER | R14 | VDD_SNVS_IN | GPIO | — | SNVS_TAMPER | Input | 100 k Ω pull-down |
| TEST_MODE | N14 | VDD_SNVS_IN | — | — | TEST_MODE | Input | 100 k Ω pull-down |
| USB_H_DATA | Y5 | NVCC_USB_H | GPIO | ALT5 | GPIO7_IO10 | Input | 100 k Ω pull-down |
| USB_H_STROBE | W5 | NVCC_USB_H | GPIO | ALT5 | GPIO7_IO11 | Input | 100 k Ω pull-down |
| USB_OTG1_CHD_B | T17 | VDD_USB_CAP | — | — | USB_OTG1_CHD_B | — | — |
| USB_OTG1_DN | W17 | VDD_USB_CAP | — | — | USB_OTG1_DN | — | — |
| USB_OTG1_DP | Y17 | VDD_USB_CAP | — | — | USB_OTG1_DP | — | — |
| USB_OTG2_DN | W15 | VDD_USB_CAP | — | — | USB_OTG2_DN | — | — |
| USB_OTG2_DP | Y15 | VDD_USB_CAP | — | — | USB_OTG2_DP | — | — |
| XTALI | V19 | NVCC_PLL | — | — | XTALI | — | — |
| XTALO | V20 | NVCC_PLL | — | — | XTALO | — | — |

Table 121. 17x17 mm WP (with PCIe), 0.8 mm Pitch, 20x20 Ball Map (continued)

| N | M | L | K | J | H |
|------------------|-------------|---------------|---------------|-------------|--------------|
| DRAM_DATA07 | DRAM_DATA04 | DRAM_SDCLK0_N | DRAM_SDCLK0_P | DRAM_DATA12 | DRAM_DATA08 |
| DRAM_DQM0 | DRAM_DATA05 | DRAM_DATA06 | DRAM_DATA10 | DRAM_DATA11 | DRAM_SDQS1_N |
| VSS | DRAM_ADDR04 | VSS | VSS | DRAM_VREF | VSS |
| DRAM_ADDR11 | DRAM_ADDR13 | DRAM_ADDR00 | DRAM_SDBA2 | DRAM_CAS_B | DRAM_CS0_B |
| DRAM_ADDR10 | DRAM_ADDR08 | DRAM_ADDR09 | DRAM_ADDR02 | DRAM_SDWE_B | DRAM_RAS_B |
| NVCC_DRAM | NVCC_DRAM | NVCC_DRAM | NVCC_DRAM | NVCC_DRAM | NVCC_DRAM |
| VSS | VSS | VSS | NVCC_DRAM_2P5 | VSS | VSS |
| VDD_SOC_CAP | VDD_SOC_CAP | VDD_SOC_CAP | VDD_SOC_CAP | VDD_SOC_CAP | VDD_SOC_CAP |
| VDD_SOC_CAP | VDD_SOC_IN | VDD_SOC_IN | VDD_SOC_IN | VDD_SOC_IN | VDD_SOC_CAP |
| VDD_SOC_CAP | VDD_SOC_IN | VSS | VSS | VDD_ARM_IN | VDD_ARM_CAP |
| VDD_SOC_CAP | VDD_SOC_IN | VSS | VSS | VDD_ARM_IN | VDD_ARM_CAP |
| VDD_SOC_CAP | VDD_SOC_IN | VDD_ARM_IN | VDD_ARM_IN | VDD_ARM_IN | VDD_ARM_CAP |
| VSS | VDD_SOC_CAP | VDD_ARM_CAP | VDD_ARM_CAP | VDD_ARM_CAP | VDD_ARM_CAP |
| TEST_MODE | VSS | VSS | VSS | VSS | VSS |
| ONOFF | LCD1_DATA06 | LCD1_DATA11 | LCD1_DATA13 | LCD1_VSYNC | NVCC_LCD1 |
| SNVS_PMIC_ON_REQ | LCD1_DATA05 | LCD1_DATA09 | LCD1_DATA12 | LCD1_HSYNC | LCD1_DATA15 |
| LCD1_DATA04 | VSS | LCD1_CLK | LCD1_DATA14 | VSS | LCD1_DATA20 |
| PCIE_REXT | LCD1_DATA03 | LCD1_DATA01 | LCD1_DATA08 | LCD1_RESET | VDD_ARM_IN |
| VSS | LCD1_DATA02 | LCD1_DATA10 | LCD1_DATA17 | LCD1_ENABLE | LCD1_DATA22 |
| VSS | LCD1_DATA00 | LCD1_DATA07 | LCD1_DATA18 | LCD1_DATA19 | LCD1_DATA16 |
| N | M | L | K | J | H |

Table 121. 17x17 mm WP (with PCIe), 0.8 mm Pitch, 20x20 Ball Map (continued)

| | Y | W | V | U | T | R | P |
|----|--------------|--------------|--------------|-------------|----------------|--------------|-------------------|
| 1 | VSS | DRAM_SDQS2_N | DRAM_DATA16 | DRAM_DATA22 | DRAM_DATA02 | DRAM_DATA00 | DRAM_SDQS0_P |
| 2 | DRAM_DATA21 | DRAM_SDQS2_P | DRAM_DATA23 | DRAM_DATA19 | DRAM_DATA01 | DRAM_DATA03 | DRAM_SDQS0_N |
| 3 | DRAM_DQM2 | DRAM_DATA20 | VSS | DRAM_ODT0 | VSS | VSS | DRAM_SDBA1 |
| 4 | DRAM_DATA18 | DRAM_DATA17 | VSS | DRAM_ADDR01 | DRAM_ADDR06 | DRAM_ADDR14 | DRAM_ADDR12 |
| 5 | USB_H_DATA | USB_H_STROBE | NVCC_USB_H | NAND_DATA03 | NAND_DATA05 | VSS | DRAM_SDCKE0 |
| 6 | NAND_READY_B | NAND_ALE | NAND_DATA00 | VSS | NAND_DATA07 | NVCC_NAND | NVCC_DRAM |
| 7 | NAND_DATA02 | NAND_DATA04 | NAND_WP_B | NAND_CE0_B | NAND_WE_B | JTAG_MOD | VSS |
| 8 | NAND_DATA06 | NAND_DATA01 | VDD_SOC_CAP | NAND_RE_B | NAND_CLE | JTAG_TDO | VSS |
| 9 | SD4_DATA0 | SD4_DATA1 | NAND_CE1_B | VSS | JTAG_TRST_B | JTAG_TCK | VSS |
| 10 | SD4_DATA6 | SD4_DATA7 | NVCC_SD4 | SD3_DATA0 | JTAG_TMS | JTAG_TDI | VSS |
| 11 | SD4_DATA5 | SD4_CLK | SD3_CLK | SD3_DATA7 | SD3_DATA1 | NVCC_JTAG | VSS |
| 12 | SD4_DATA4 | SD4_CMD | SD3_DATA6 | VSS | SD4_RESET_B | NVCC_HIGH | VSS |
| 13 | SD4_DATA2 | SD4_DATA3 | NVCC_LOW | SD3_DATA5 | SD3_CMD | VDDA_ADC_3P3 | NGND_KEL0 |
| 14 | ADC1_IN0 | ADC1_IN1 | SD3_DATA3 | SD3_DATA2 | SD3_DATA4 | SNVS_TAMPER | POR_B |
| 15 | USB_OTG2_DP | USB_OTG2_DN | VDD_USB_CAP | VSS | USB_OTG2_VBUS | CCM_CLK2 | CCM_PMIC_STBY_REQ |
| 16 | VSS | VSS | VDD_SNV5_CAP | GANAIO | USB_OTG1_VBUS | CCM_CLK1_P | CCM_CLK1_N |
| 17 | USB_OTG1_DP | USB_OTG1_DN | VDD_HIGH_CAP | VDD_HIGH_IN | USB_OTG1_CHD_B | VSS | PCIE_VPTX |
| 18 | VSS | VSS | VDD_HIGH_CAP | VDD_HIGH_IN | VDD_SNV5_IN | PCIE_VPH | PCIE_VP |
| 19 | RTC_XTALO | RTC_XTALI | XTALI | BOOT_MODE1 | VSS | PCIE_TX_N | PCIE_RX_N |
| 20 | VSS | NVCC_PLL | XTALO | BOOT_MODE0 | VSS | PCIE_TX_P | PCIE_RX_P |
| | Y | W | V | U | T | R | P |



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

| | | |
|--|--------------------------|----------------------------|
| © NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |
| TITLE: MAPBGA, THIN PROFILE, 14 X 14 X 1.165 PKG, 0.65 MM PITCH, 400 I/O | DOCUMENT NO: 98ASA00783D | REV: A |
| | STANDARD: NON-JEDEC | |
| | SOT1559-1 | 17 FEB 2016 |

Figure 89. 14x14 mm BGA Package Notes

6.5.2 14x14 mm Supplies Contact Assignments and Functional Contact Assignments

Table 122 shows supplies contact assignments for the 14x14 mm package and Table 123 shows the functional contact assignments.

Table 122. 14x14 mm Supplies Contact Assignments

| Supply Rail Name | 14x14 mm Ball Position(s) | Comments |
|------------------|--------------------------------|---|
| ADC_VREFH | Y15 | ADC high reference voltage |
| ADC_VREFL | V14 | ADC low reference voltage |
| DRAM_VREF | K4 | DDR voltage reference input. Connect to a voltage source that is 50% of NVCC_DRAM. |
| DRAM_ZQPAD | H2 | DDR output buffer driver calibration reference voltage input. Connect DRAM_ZQPAD to an external 240 ohm 1% resistor to Vss. |
| GPANAIO | P16 | Analog output for NXP use only. This output must always be left unconnected. |
| NVCC_DRAM | G6, H6, J6, K6, L6, M6, N6, P6 | Supply input for the DDR I/O interface |
| NVCC_DRAM_2P5 | K7 | Supply input for the DDR interface |
| NVCC_ENET | F6 | Supply input for the ENET interfaces |
| NVCC_GPIO | F15 | Supply input for the GPIO interface |
| NVCC_HIGH | R12 | 3.3 V Supply input for the dual-voltage I/Os on the SD3 interface |
| NVCC_JTAG | T9 | Supply input for the JTAG interface |
| NVCC_KEY | G15 | Supply input for the Key Pad Port (KPP) interface |
| NVCC_CSI_LCD1 | H15 | Supply input for the LCD interface |
| NVCC_LOW | V13 | 1.8 V Supply input for the dual-voltage I/Os on the SD3 interface |
| NVCC_NAND | R6 | Supply input for the Raw NAND flash memories interface |
| NVCC_PLL | U18 | Supply input for the PLLs |
| NVCC_QSPI | F14 | Supply input for the QSPI interface |
| NVCC_RGMII1 | F8 | Supply input for the RGMII1 interface |
| NVCC_RGMII2 | E11 | Supply input for the RGMII2 interface |
| NVCC_SD1_SD2 | F13 | Supply input for the SD2 interface |
| NVCC_SD4 | T12 | Supply input for the SD4 interface |
| NVCC_USB_H | V5 | Supply input for the USB HSIC interface |
| NGND_KEL0 | T16 | Ground |
| PCIE_VP_CAP | L18 | PCIe LDO output. Although this package does not support PCIe, this output requires a 4.7uF capacitor to ground unless the PCIe LDO is disabled. |
| USB_OTG1_VBUS | W20 | VBUS input for USB_OTG1 |
| USB_OTG2_VBUS | U17 | VBUS input for USB_OTG2 |

Table 122. 14x14 mm Supplies Contact Assignments (continued)

| Supply Rail Name | 14x14 mm Ball Position(s) | Comments |
|------------------|--|--|
| VDD_ARM_CAP | C16, D16, H10, H11, H12, H13, J13, K13, L13 | Supply voltage output from internal LDO_ARM. Requires external capacitor(s). |
| VDD_ARM_IN | H18, J10, J11, J12, K12, L12 | Supply voltage input for internal LDO_ARM. |
| VDD_HIGH_CAP | N17, N18 | Supply voltage output from internal LDO_2P5. Requires external capacitor(s). |
| VDD_HIGH_IN | P17, P18 | Supply voltage input to internal LDO_2P5, LDO_1P1 and LDO_SNV5. |
| VDD_SNV5_CAP | T18 | Supply voltage output from internal LDO_SNV5. Requires external capacitor(s). |
| VDD_SNV5_IN | R18 | Supply voltage input to the SNV5 voltage domain |
| VDD_SOC_CAP | H8, H9, J8, K8, L8, M8, M13, N8, N9, N10, N11, N12, V9 | Supply voltage output from internal LDO_SOC. Requires external capacitor(s). |
| VDD_SOC_IN | D7, D8, J9, K9, L9, M9, M10, M11, M12 | Supply voltage input to internal LDO_SOC and LDO_PCIE |
| VDD_USB_CAP | V17 | Supply voltage output from internal LDO_USB. Requires external capacitor(s). |
| VDDA_ADC_3P3 | R13 | Supply voltage input to the ADC. This supply must be provided even if the ADC is not used. |
| VSS | A1, A20, C3, C4, C18, D6, D9, D12, D15, E3, F3, F5, F17, G7, G8, G9, G10, G11, G12, G13, G14, H3, H7, H14, J7, J14, J17, K3, K10, K11, K14, L3, L7, L10, L11, L14, M7, M14, M17, N3, N7, N13, P7, P8, P9, P10, P11, P12, R3, R5, R17, R19, R20, T3, U6, U9, U12, U15, U19, U20, V3, V4, V18, W18, Y1, Y18, Y20 | Ground |

Table 123. 14 x 14 Functional Contact Assignments

| Ball Name | 14x14 Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|-------------------|------------|--------------|-----------|------------------------|--------------------|--------------|------------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| ADC1_IN0 | N14 | VDDA_ADC_3P3 | — | — | ADC1_IN0 | Input | — |
| ADC1_IN1 | T15 | VDDA_ADC_3P3 | — | — | ADC1_IN1 | Input | — |
| ADC1_IN2 | W14 | VDDA_ADC_3P3 | — | — | ADC1_IN2 | Input | — |
| ADC1_IN3 | P13 | VDDA_ADC_3P3 | — | — | ADC1_IN3 | Input | — |
| ADC2_IN0 | W15 | VDDA_ADC_3P3 | — | — | ADC2_IN0 | Input | — |
| ADC2_IN1 | R14 | VDDA_ADC_3P3 | — | — | ADC2_IN1 | Input | — |
| ADC2_IN2 | N15 | VDDA_ADC_3P3 | — | — | ADC2_IN2 | Input | — |
| ADC2_IN3 | R15 | VDDA_ADC_3P3 | — | — | ADC2_IN3 | Input | — |
| BOOT_MODE0 | Y16 | VDD_SNVS_IN | GPIO | — | BOOT_MODE0 | Input | 100 kΩ pull-down |
| BOOT_MODE1 | W16 | VDD_SNVS_IN | GPIO | — | BOOT_MODE1 | Input | 100 kΩ pull-down |
| CCM_CLK1_N | P20 | VDD_HIGH_CAP | — | — | CCM_CLK1_N | — | — |
| CCM_CLK1_P | P19 | VDD_HIGH_CAP | — | — | CCM_CLK1_P | — | — |
| CCM_CLK2 | V16 | VDD_HIGH_CAP | — | — | CCM_CLK2 | — | — |
| CCM_PMIC_STBY_REQ | N16 | VDD_SNVS_IN | GPIO | — | CCM_PMIC_STB Y_REQ | Output | 0 |
| DRAM_ADDR00 | N5 | NVCC_DRAM | DDR | — | DRAM_ADDR00 | Output | 100 kΩ pull-up |
| DRAM_ADDR01 | P5 | NVCC_DRAM | DDR | — | DRAM_ADDR01 | Output | 100 kΩ pull-up |
| DRAM_ADDR02 | M4 | NVCC_DRAM | DDR | — | DRAM_ADDR02 | Output | 100 kΩ pull-up |
| DRAM_ADDR03 | K5 | NVCC_DRAM | DDR | — | DRAM_ADDR03 | Output | 100 kΩ pull-up |
| DRAM_ADDR04 | H5 | NVCC_DRAM | DDR | — | DRAM_ADDR04 | Output | 100 kΩ pull-up |
| DRAM_ADDR05 | F4 | NVCC_DRAM | DDR | — | DRAM_ADDR05 | Output | 100 kΩ pull-up |
| DRAM_ADDR06 | N4 | NVCC_DRAM | DDR | — | DRAM_ADDR06 | Output | 100 kΩ pull-up |
| DRAM_ADDR07 | G5 | NVCC_DRAM | DDR | — | DRAM_ADDR07 | Output | 100 kΩ pull-up |
| DRAM_ADDR08 | J4 | NVCC_DRAM | DDR | — | DRAM_ADDR08 | Output | 100 kΩ pull-up |
| DRAM_ADDR09 | L2 | NVCC_DRAM | DDR | — | DRAM_ADDR09 | Output | 100 kΩ pull-up |
| DRAM_ADDR10 | H4 | NVCC_DRAM | DDR | — | DRAM_ADDR10 | Output | 100 kΩ pull-up |
| DRAM_ADDR11 | M3 | NVCC_DRAM | DDR | — | DRAM_ADDR11 | Output | 100 kΩ pull-up |
| DRAM_ADDR12 | M5 | NVCC_DRAM | DDR | — | DRAM_ADDR12 | Output | 100 kΩ pull-up |
| DRAM_ADDR13 | J3 | NVCC_DRAM | DDR | — | DRAM_ADDR13 | Output | 100 kΩ pull-up |
| DRAM_ADDR14 | R1 | NVCC_DRAM | DDR | — | DRAM_ADDR14 | Output | 100 kΩ pull-up |

Table 123. 14 x 14 Functional Contact Assignments (continued)

| Ball Name | 14x14 Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|-------------|------------|-------------|-----------|------------------------|------------------|--------------|----------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| DRAM_CAS_B | N2 | NVCC_DRAM | DDR | — | DRAM_CAS_B | Output | 100 kΩ pull-up |
| DRAM_CS0_B | L4 | NVCC_DRAM | DDR | — | DRAM_CS0_B | Output | 100 kΩ pull-up |
| DRAM_CS1_B | K2 | NVCC_DRAM | DDR | — | DRAM_CS1_B | Output | 100 kΩ pull-up |
| DRAM_DATA00 | T2 | NVCC_DRAM | DDR | — | DRAM_DATA00 | Input | 100 kΩ pull-up |
| DRAM_DATA01 | U2 | NVCC_DRAM | DDR | — | DRAM_DATA01 | Input | 100 kΩ pull-up |
| DRAM_DATA02 | U1 | NVCC_DRAM | DDR | — | DRAM_DATA02 | Input | 100 kΩ pull-up |
| DRAM_DATA03 | R2 | NVCC_DRAM | DDR | — | DRAM_DATA03 | Input | 100 kΩ pull-up |
| DRAM_DATA04 | U3 | NVCC_DRAM | DDR | — | DRAM_DATA04 | Input | 100 kΩ pull-up |
| DRAM_DATA05 | R4 | NVCC_DRAM | DDR | — | DRAM_DATA05 | Input | 100 kΩ pull-up |
| DRAM_DATA06 | P3 | NVCC_DRAM | DDR | — | DRAM_DATA06 | Input | 100 kΩ pull-up |
| DRAM_DATA07 | P4 | NVCC_DRAM | DDR | — | DRAM_DATA07 | Input | 100 kΩ pull-up |
| DRAM_DATA08 | F1 | NVCC_DRAM | DDR | — | DRAM_DATA08 | Input | 100 kΩ pull-up |
| DRAM_DATA09 | F2 | NVCC_DRAM | DDR | — | DRAM_DATA09 | Input | 100 kΩ pull-up |
| DRAM_DATA10 | G3 | NVCC_DRAM | DDR | — | DRAM_DATA10 | Input | 100 kΩ pull-up |
| DRAM_DATA11 | E2 | NVCC_DRAM | DDR | — | DRAM_DATA11 | Input | 100 kΩ pull-up |
| DRAM_DATA12 | E4 | NVCC_DRAM | DDR | — | DRAM_DATA12 | Input | 100 kΩ pull-up |
| DRAM_DATA13 | D1 | NVCC_DRAM | DDR | — | DRAM_DATA13 | Input | 100 kΩ pull-up |
| DRAM_DATA14 | E1 | NVCC_DRAM | DDR | — | DRAM_DATA14 | Input | 100 kΩ pull-up |
| DRAM_DATA15 | D2 | NVCC_DRAM | DDR | — | DRAM_DATA15 | Input | 100 kΩ pull-up |
| DRAM_DATA16 | Y4 | NVCC_DRAM | DDR | — | DRAM_DATA16 | Input | 100 kΩ pull-up |
| DRAM_DATA17 | W4 | NVCC_DRAM | DDR | — | DRAM_DATA17 | Input | 100 kΩ pull-up |
| DRAM_DATA18 | Y3 | NVCC_DRAM | DDR | — | DRAM_DATA18 | Input | 100 kΩ pull-up |
| DRAM_DATA19 | U4 | NVCC_DRAM | DDR | — | DRAM_DATA19 | Input | 100 kΩ pull-up |
| DRAM_DATA20 | W3 | NVCC_DRAM | DDR | — | DRAM_DATA20 | Input | 100 kΩ pull-up |
| DRAM_DATA21 | Y2 | NVCC_DRAM | DDR | — | DRAM_DATA21 | Input | 100 kΩ pull-up |
| DRAM_DATA22 | T4 | NVCC_DRAM | DDR | — | DRAM_DATA22 | Input | 100 kΩ pull-up |
| DRAM_DATA23 | W2 | NVCC_DRAM | DDR | — | DRAM_DATA23 | Input | 100 kΩ pull-up |
| DRAM_DATA24 | D3 | NVCC_DRAM | DDR | — | DRAM_DATA24 | Input | 100 kΩ pull-up |
| DRAM_DATA25 | B3 | NVCC_DRAM | DDR | — | DRAM_DATA25 | Input | 100 kΩ pull-up |
| DRAM_DATA26 | A3 | NVCC_DRAM | DDR | — | DRAM_DATA26 | Input | 100 kΩ pull-up |
| DRAM_DATA27 | C2 | NVCC_DRAM | DDR | — | DRAM_DATA27 | Input | 100 kΩ pull-up |

Table 123. 14 x 14 Functional Contact Assignments (continued)

| Ball Name | 14x14 Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|---------------|------------|-------------|-----------|------------------------|------------------|--------------|------------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| DRAM_DATA28 | A2 | NVCC_DRAM | DDR | — | DRAM_DATA28 | Input | 100 kΩ pull-up |
| DRAM_DATA29 | C5 | NVCC_DRAM | DDR | — | DRAM_DATA29 | Input | 100 kΩ pull-up |
| DRAM_DATA30 | B4 | NVCC_DRAM | DDR | — | DRAM_DATA30 | Input | 100 kΩ pull-up |
| DRAM_DATA31 | A4 | NVCC_DRAM | DDR | — | DRAM_DATA31 | Input | 100 kΩ pull-up |
| DRAM_DQM0 | N1 | NVCC_DRAM | DDR | — | DRAM_DQM0 | Output | 100 kΩ pull-up |
| DRAM_DQM1 | G2 | NVCC_DRAM | DDR | — | DRAM_DQM1 | Output | 100 kΩ pull-up |
| DRAM_DQM2 | W1 | NVCC_DRAM | DDR | — | DRAM_DQM2 | Output | 100 kΩ pull-up |
| DRAM_DQM3 | C1 | NVCC_DRAM | DDR | — | DRAM_DQM3 | Output | 100 kΩ pull-up |
| DRAM_ODT0 | T1 | NVCC_DRAM | DDR | — | DRAM_ODT0 | Output | 100 kΩ pull-down |
| DRAM_RAS_B | J1 | NVCC_DRAM | DDR | — | DRAM_RAS_B | Output | 100 kΩ pull-up |
| DRAM_RESET | D4 | NVCC_DRAM | DDR | — | DRAM_RESET | Output | 100 kΩ pull-down |
| DRAM_SDBA0 | G4 | NVCC_DRAM | DDR | — | DRAM_SDBA0 | Output | 100 kΩ pull-up |
| DRAM_SDBA1 | M2 | NVCC_DRAM | DDR | — | DRAM_SDBA1 | Output | 100 kΩ pull-up |
| DRAM_SDBA2 | J2 | NVCC_DRAM | DDR | — | DRAM_SDBA2 | Output | 100 kΩ pull-up |
| DRAM_SDCKE0 | L5 | NVCC_DRAM | DDR | — | DRAM_SDCKE0 | Output | 100 kΩ pull-down |
| DRAM_SDCKE1 | J5 | NVCC_DRAM | DDR | — | DRAM_SDCKE1 | Output | 100 kΩ pull-down |
| DRAM_SDCLK0_N | L1 | NVCC_DRAM | DDRCLK | — | DRAM_SDCLK0_N | — | — |
| DRAM_SDCLK0_P | K1 | NVCC_DRAM | DDRCLK | — | DRAM_SDCLK0_P | Output | Low |
| DRAM_SDQS0_N | P2 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS0_N | — | — |
| DRAM_SDQS0_P | P1 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS0_P | Input | — |
| DRAM_SDQS1_N | H1 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS1_N | — | — |
| DRAM_SDQS1_P | G1 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS1_P | Input | — |
| DRAM_SDQS2_N | V2 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS2_N | — | — |
| DRAM_SDQS2_P | V1 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS2_P | Input | — |
| DRAM_SDQS3_N | B1 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS3_N | — | — |

Table 123. 14 x 14 Functional Contact Assignments (continued)

| Ball Name | 14x14 Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|--------------|------------|-------------|-----------|------------------------|------------------|--------------|------------------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| DRAM_SDQS3_P | B2 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS3_P | Input | — |
| DRAM_SDWE_B | M1 | NVCC_DRAM | DDR | — | DRAM_SDWE_B | Output | 100 k Ω pull-up |
| ENET1_COL | B5 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO00 | Input | Keeper |
| ENET1_CRS | C6 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO01 | Input | Keeper |
| ENET1_MDC | B6 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO02 | Input | Keeper |
| ENET1_MDIO | A6 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO03 | Input | Keeper |
| ENET1_RX_CLK | A5 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO04 | Input | Keeper |
| ENET1_TX_CLK | F7 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO05 | Input | Keeper |
| ENET2_COL | E7 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO06 | Input | Keeper |
| ENET2_CRS | E6 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO07 | Input | Keeper |
| ENET2_RX_CLK | E5 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO08 | Input | Keeper |
| ENET2_TX_CLK | D5 | NVCC_ENET | GPIO | ALT5 | GPIO2_IO09 | Input | Keeper |
| GPIO1_IO00 | B20 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO00 | Input | Keeper |
| GPIO1_IO01 | D19 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO01 | Input | Keeper |
| GPIO1_IO02 | C19 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO02 | Input | Keeper |
| GPIO1_IO03 | D20 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO03 | Input | Keeper |
| GPIO1_IO04 | E16 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO04 | Input | Keeper |
| GPIO1_IO05 | B18 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO05 | Input | Keeper |
| GPIO1_IO06 | D18 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO06 | Input | Keeper |
| GPIO1_IO07 | A17 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO07 | Input | Keeper |
| GPIO1_IO08 | E17 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO08 | Input | Keeper |
| GPIO1_IO09 | A19 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO09 | Input | Keeper |
| GPIO1_IO10 | B19 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO10 | Input | Keeper |
| GPIO1_IO11 | C20 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO11 | Input | Keeper |
| GPIO1_IO12 | D17 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO12 | Input | Keeper |
| GPIO1_IO13 | A16 | NVCC_GPIO | GPIO | ALT5 | GPIO1_IO13 | Input | Keeper |
| JTAG_MOD | R8 | NVCC_JTAG | GPIO | — | JTAG_MOD | Input | 100 k Ω pull-up |
| JTAG_TCK | R9 | NVCC_JTAG | GPIO | — | JTAG_TCK | Input | 47 k Ω pull-up |
| JTAG_TDI | R10 | NVCC_JTAG | GPIO | — | JTAG_TDI | Input | 47 k Ω pull-up |
| JTAG_TDO | Y9 | NVCC_JTAG | GPIO | — | JTAG_TDO | Output | Keeper |
| JTAG_TMS | W9 | NVCC_JTAG | GPIO | — | JTAG_TMS | Input | 47 k Ω pull-up |

Table 123. 14 x 14 Functional Contact Assignments (continued)

| Ball Name | 14x14 Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|-------------|------------|-------------|-----------|------------------------|------------------|--------------|---------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| JTAG_TRST_B | V8 | NVCC_JTAG | GPIO | — | JTAG_TRST_B | Input | 47 kΩ pull-up |
| KEY_COL0 | F18 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO10 | Input | Keeper |
| KEY_COL1 | F19 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO11 | Input | Keeper |
| KEY_COL2 | G17 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO12 | Input | Keeper |
| KEY_COL3 | E20 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO13 | Input | Keeper |
| KEY_COL4 | E19 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO14 | Input | Keeper |
| KEY_ROW0 | F16 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO15 | Input | Keeper |
| KEY_ROW1 | E18 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO16 | Input | Keeper |
| KEY_ROW2 | F20 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO17 | Input | Keeper |
| KEY_ROW3 | G20 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO18 | Input | Keeper |
| KEY_ROW4 | H19 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO19 | Input | Keeper |
| LCD1_CLK | L19 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO00 | Input | Keeper |
| LCD1_DATA00 | M19 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO01 | Input | Keeper |
| LCD1_DATA01 | L17 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO02 | Input | Keeper |
| LCD1_DATA02 | M18 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO03 | Input | Keeper |
| LCD1_DATA03 | N20 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO04 | Input | Keeper |
| LCD1_DATA04 | N19 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO05 | Input | Keeper |
| LCD1_DATA05 | M15 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO06 | Input | Keeper |
| LCD1_DATA06 | M16 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO07 | Input | Keeper |
| LCD1_DATA07 | J19 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO08 | Input | Keeper |
| LCD1_DATA08 | K18 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO09 | Input | Keeper |
| LCD1_DATA09 | L15 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO10 | Input | Keeper |
| LCD1_DATA10 | K19 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO11 | Input | Keeper |
| LCD1_DATA11 | L16 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO12 | Input | Keeper |
| LCD1_DATA12 | K15 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO13 | Input | Keeper |
| LCD1_DATA13 | K16 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO14 | Input | Keeper |
| LCD1_DATA14 | K17 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO15 | Input | Keeper |
| LCD1_DATA15 | H16 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO16 | Input | Keeper |
| LCD1_DATA16 | H20 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO17 | Input | Keeper |
| LCD1_DATA17 | M20 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO18 | Input | Keeper |
| LCD1_DATA18 | L20 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO19 | Input | Keeper |

Table 123. 14 x 14 Functional Contact Assignments (continued)

| Ball Name | 14x14 Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|--------------|------------|-------------|-----------|------------------------|------------------|--------------|------------------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| LCD1_DATA19 | J20 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO20 | Input | Keeper |
| LCD1_DATA20 | H17 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO21 | Input | Keeper |
| LCD1_DATA21 | G18 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO22 | Input | Keeper |
| LCD1_DATA22 | G19 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO23 | Input | Keeper |
| LCD1_DATA23 | G16 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO24 | Input | Keeper |
| LCD1_ENABLE | K20 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO25 | Input | Keeper |
| LCD1_HSYNC | J15 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO26 | Input | Keeper |
| LCD1_RESET | J18 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO27 | Input | Keeper |
| LCD1_VSYNC | J16 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO28 | Input | Keeper |
| NAND_ALE | W6 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO00 | Input | Keeper |
| NAND_CE0_B | U7 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO01 | Input | Keeper |
| NAND_CE1_B | T8 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO02 | Input | Keeper |
| NAND_CLE | R7 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO03 | Input | Keeper |
| NAND_DATA00 | V6 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO04 | Input | Keeper |
| NAND_DATA01 | W8 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO05 | Input | Keeper |
| NAND_DATA02 | Y7 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO06 | Input | Keeper |
| NAND_DATA03 | U5 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO07 | Input | Keeper |
| NAND_DATA04 | W7 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO08 | Input | Keeper |
| NAND_DATA05 | T5 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO09 | Input | Keeper |
| NAND_DATA06 | Y8 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO10 | Input | Keeper |
| NAND_DATA07 | T6 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO11 | Input | Keeper |
| NAND_RE_B | U8 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO12 | Input | Keeper |
| NAND_READY_B | Y6 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO13 | Input | Keeper |
| NAND_WE_B | T7 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO14 | Input | Keeper |
| NAND_WP_B | V7 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO15 | Input | Keeper |
| ONOFF | U16 | VDD_SNVS_IN | GPIO | — | ONOFF | Input | 100 k Ω pull-up |
| POR_B | R16 | VDD_SNVS_IN | GPIO | — | POR_B | Input | 100 k Ω pull-up |
| QSPI1A_DATA0 | E15 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO16 | Input | Keeper |
| QSPI1A_DATA1 | C15 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO17 | Input | Keeper |
| QSPI1A_DATA2 | D14 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO18 | Input | Keeper |
| QSPI1A_DATA3 | A18 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO19 | Input | Keeper |

Table 123. 14 x 14 Functional Contact Assignments (continued)

| Ball Name | 14x14 Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|--------------|------------|-------------|-----------|------------------------|------------------|--------------|--------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| QSPI1A_DQS | A13 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO20 | Input | Keeper |
| QSPI1A_SCLK | B16 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO21 | Input | Keeper |
| QSPI1A_SS0_B | C17 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO22 | Input | Keeper |
| QSPI1A_SS1_B | B17 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO23 | Input | Keeper |
| QSPI1B_DATA0 | A15 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO24 | Input | Keeper |
| QSPI1B_DATA1 | A14 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO25 | Input | Keeper |
| QSPI1B_DATA2 | C13 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO26 | Input | Keeper |
| QSPI1B_DATA3 | D13 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO27 | Input | Keeper |
| QSPI1B_DQS | B13 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO28 | Input | Keeper |
| QSPI1B_SCLK | B14 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO29 | Input | Keeper |
| QSPI1B_SS0_B | C14 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO30 | Input | Keeper |
| QSPI1B_SS1_B | B15 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO31 | Input | Keeper |
| RGMI1_RD0 | E8 | NVCC_RGMI1 | GPIO | ALT5 | GPIO5_IO00 | Input | Keeper |
| RGMI1_RD1 | A7 | NVCC_RGMI1 | GPIO | ALT5 | GPIO5_IO01 | Input | Keeper |
| RGMI1_RD2 | C7 | NVCC_RGMI1 | GPIO | ALT5 | GPIO5_IO02 | Input | Keeper |
| RGMI1_RD3 | C8 | NVCC_RGMI1 | GPIO | ALT5 | GPIO5_IO03 | Input | Keeper |
| RGMI1_RX_CTL | B7 | NVCC_RGMI1 | GPIO | ALT5 | GPIO5_IO04 | Input | Keeper |
| RGMI1_RXC | C10 | NVCC_RGMI1 | GPIO | ALT5 | GPIO5_IO05 | Input | Keeper |
| RGMI1_TD0 | E10 | NVCC_RGMI1 | GPIO | ALT5 | GPIO5_IO06 | Input | Keeper |
| RGMI1_TD1 | A8 | NVCC_RGMI1 | GPIO | ALT5 | GPIO5_IO07 | Input | Keeper |
| RGMI1_TD2 | F9 | NVCC_RGMI1 | GPIO | ALT5 | GPIO5_IO08 | Input | Keeper |
| RGMI1_TD3 | E9 | NVCC_RGMI1 | GPIO | ALT5 | GPIO5_IO09 | Input | Keeper |
| RGMI1_TX_CTL | D10 | NVCC_RGMI1 | GPIO | ALT5 | GPIO5_IO10 | Input | Keeper |
| RGMI1_TXC | B8 | NVCC_RGMI1 | GPIO | ALT5 | GPIO5_IO11 | Input | Keeper |
| RGMI2_RD0 | C11 | NVCC_RGMI2 | GPIO | ALT5 | GPIO5_IO12 | Input | Keeper |
| RGMI2_RD1 | A9 | NVCC_RGMI2 | GPIO | ALT5 | GPIO5_IO13 | Input | Keeper |
| RGMI2_RD2 | A11 | NVCC_RGMI2 | GPIO | ALT5 | GPIO5_IO14 | Input | Keeper |
| RGMI2_RD3 | D11 | NVCC_RGMI2 | GPIO | ALT5 | GPIO5_IO15 | Input | Keeper |
| RGMI2_RX_CTL | B9 | NVCC_RGMI2 | GPIO | ALT5 | GPIO5_IO16 | Input | Keeper |
| RGMI2_RXC | A12 | NVCC_RGMI2 | GPIO | ALT5 | GPIO5_IO17 | Input | Keeper |
| RGMI2_TD0 | A10 | NVCC_RGMI2 | GPIO | ALT5 | GPIO5_IO18 | Input | Keeper |

Table 123. 14 x 14 Functional Contact Assignments (continued)

| Ball Name | 14x14 Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|---------------|------------|-----------------------|-----------|------------------------|------------------|--------------|---------------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| RGMII2_TD1 | C12 | NVCC_RGMII2 | GPIO | ALT5 | GPIO5_IO19 | Input | Keeper |
| RGMII2_TD2 | B10 | NVCC_RGMII2 | GPIO | ALT5 | GPIO5_IO20 | Input | Keeper |
| RGMII2_TD3 | B12 | NVCC_RGMII2 | GPIO | ALT5 | GPIO5_IO21 | Input | Keeper |
| RGMII2_TX_CTL | C9 | NVCC_RGMII2 | GPIO | ALT5 | GPIO5_IO22 | Input | Keeper |
| RGMII2_TXC | B11 | NVCC_RGMII2 | GPIO | ALT5 | GPIO5_IO23 | Input | Keeper |
| RTC_XTALI | Y17 | VDD_SNV5_CAP | — | — | RTC_XTALI | — | — |
| RTC_XTALO | W17 | VDD_SNV5_CAP | — | — | RTC_XTALO | — | — |
| SD2_CLK | E12 | NVCC_SD1_SD2 | GPIO | ALT5 | GPIO6_IO06 | Input | Keeper |
| SD2_CMD | F12 | NVCC_SD1_SD2 | GPIO | ALT5 | GPIO6_IO07 | Input | Keeper |
| SD2_DATA0 | E13 | NVCC_SD1_SD2 | GPIO | ALT5 | GPIO6_IO08 | Input | Keeper |
| SD2_DATA1 | E14 | NVCC_SD1_SD2 | GPIO | ALT5 | GPIO6_IO09 | Input | Keeper |
| SD2_DATA2 | F10 | NVCC_SD1_SD2 | GPIO | ALT5 | GPIO6_IO10 | Input | Keeper |
| SD2_DATA3 | F11 | NVCC_SD1_SD2 | GPIO | ALT5 | GPIO6_IO11 | Input | Keeper |
| SD3_CLK | V11 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO00 | Input | 100 kΩ pull-down |
| SD3_CMD | T13 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO01 | Input | 100 kΩ pull-down |
| SD3_DATA0 | R11 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO02 | Input | 100 kΩ pull-down |
| SD3_DATA1 | T11 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO03 | Input | 100 kΩ pull-down |
| SD3_DATA2 | Y14 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO04 | Input | 100 kΩ pull-down |
| SD3_DATA3 | T14 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO05 | Input | 100 kΩ pull-down |
| SD3_DATA4 | U14 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO06 | Input | 100 kΩ pull-down |
| SD3_DATA5 | U13 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO07 | Input | 100 kΩ pull-down |
| SD3_DATA6 | V12 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO08 | Input | 100 kΩ pull-down |
| SD3_DATA7 | U11 | NVCC_LOW NVCC_HIGH | GPIO | ALT5 | GPIO7_IO09 | Input | 100 kΩ pull-down |
| SD4_CLK | T10 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO12 | Input | Keeper |
| SD4_CMD | W12 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO13 | Input | Keeper |

Table 123. 14 x 14 Functional Contact Assignments (continued)

| Ball Name | 14x14 Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|------------------|------------|-------------|-----------|------------------------|------------------|--------------|--------------------------|
| | | | | Default Mode | Default Function | Input/Output | Value |
| SD4_DATA0 | Y10 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO14 | Input | Keeper |
| SD4_DATA1 | Y11 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO15 | Input | Keeper |
| SD4_DATA2 | Y13 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO16 | Input | Keeper |
| SD4_DATA3 | W13 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO17 | Input | Keeper |
| SD4_DATA4 | Y12 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO18 | Input | Keeper |
| SD4_DATA5 | W10 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO19 | Input | Keeper |
| SD4_DATA6 | U10 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO20 | Input | Keeper |
| SD4_DATA7 | W11 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO21 | Input | Keeper |
| SD4_RESET_B | V10 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO22 | Input | Keeper |
| SNVS_PMIC_ON_REQ | P15 | VDD_SNVS_IN | GPIO | — | SNVS_PMIC_ON_REQ | Output | 100 k Ω pull-up |
| SNVS_TAMPER | P14 | VDD_SNVS_IN | GPIO | — | SNVS_TAMPER | Input | 100 k Ω pull-down |
| TEST_MODE | V15 | VDD_SNVS_IN | — | — | TEST_MODE | Input | 100 k Ω pull-down |
| USB_H_DATA | Y5 | NVCC_USB_H | GPIO | ALT5 | GPIO7_IO10 | Input | 100 k Ω pull-down |
| USB_H_STROBE | W5 | NVCC_USB_H | GPIO | ALT5 | GPIO7_IO11 | Input | 100 k Ω pull-down |
| USB_OTG1_CHD_B | T17 | VDD_USB_CAP | — | — | USB_OTG1_CHD_B | — | — |
| USB_OTG1_DN | V19 | VDD_USB_CAP | — | — | USB_OTG1_DN | — | — |
| USB_OTG1_DP | V20 | VDD_USB_CAP | — | — | USB_OTG1_DP | — | — |
| USB_OTG2_DN | Y19 | VDD_USB_CAP | — | — | USB_OTG2_DN | — | — |
| USB_OTG2_DP | W19 | VDD_USB_CAP | — | — | USB_OTG2_DP | — | — |
| XTALI | T19 | NVCC_PLL | — | — | XTALI | — | — |
| XTALO | T20 | NVCC_PLL | — | — | XTALO | — | — |

6.5.3 14 x 14 mm, 0.65 mm pitch, 20 x 20 Ball Map

Table 124 shows the 14 x 14 mm, 0.65 mm pitch, 20 x 20 ball map for the i.MX 6SoloX.

Table 124. 14 x 14 mm Ball Map

| G | F | E | D | C | B | A |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| DRAM_SDQS1_P | DRAM_DATA08 | DRAM_DATA14 | DRAM_DATA13 | DRAM_DQM3 | DRAM_SDQS3_N | VSS |
| DRAM_DQM1 | DRAM_DATA09 | DRAM_DATA11 | DRAM_DATA15 | DRAM_DATA27 | DRAM_SDQS3_P | DRAM_DATA28 |
| DRAM_DATA10 | VSS | VSS | DRAM_DATA24 | VSS | DRAM_DATA25 | DRAM_DATA26 |
| DRAM_SDBA0 | DRAM_ADDR05 | DRAM_DATA12 | DRAM_RESET | VSS | DRAM_DATA30 | DRAM_DATA31 |
| DRAM_ADDR07 | VSS | ENET2_RX_CLK | ENET2_TX_CLK | DRAM_DATA29 | ENET1_COL | ENET1_RX_CLK |
| NVCC_DRAM | NVCC_ENET | ENET2_CRCS | VSS | ENET1_CRCS | ENET1_MDC | ENET1_MDIO |
| VSS | ENET1_TX_CLK | ENET2_COL | VDD_SOC_IN | RGMI1_RD2 | RGMI1_RX_CTL | RGMI1_RD1 |
| VSS | NVCC_RGMI1 | RGMI1_RD0 | VDD_SOC_IN | RGMI1_RD3 | RGMI1_TXC | RGMI1_TD1 |
| VSS | RGMI1_TD2 | RGMI1_TD3 | VSS | RGMI2_TX_CTL | RGMI2_RX_CTL | RGMI2_RD1 |
| VSS | SD2_DATA2 | RGMI1_TD0 | RGMI1_TX_CTL | RGMI1_RXC | RGMI2_TD2 | RGMI2_TD0 |
| VSS | SD2_DATA3 | NVCC_RGMI2 | RGMI2_RD3 | RGMI2_RD0 | RGMI2_TXC | RGMI2_RD2 |
| VSS | SD2_CMD | SD2_CLK | VSS | RGMI2_TD1 | RGMI2_TD3 | RGMI2_RXC |
| VSS | NVCC_SD1_SD2 | SD2_DATA0 | QSPI1B_DATA3 | QSPI1B_DATA2 | QSPI1B_DQS | QSPI1A_DQS |
| VSS | NVCC_QSPI | SD2_DATA1 | QSPI1A_DATA2 | QSPI1B_SS0_B | QSPI1B_SCLK | QSPI1B_DATA1 |
| NVCC_KEY | NVCC_GPIO | QSPI1A_DATA0 | VSS | QSPI1A_DATA1 | QSPI1B_SS1_B | QSPI1B_DATA0 |
| LCD1_DATA23 | KEY_ROW0 | GPIO1_IO04 | VDD_ARM_CAP | VDD_ARM_CAP | QSPI1A_SCLK | GPIO1_IO13 |
| KEY_COL2 | VSS | GPIO1_IO08 | GPIO1_IO12 | QSPI1A_SS0_B | QSPI1A_SS1_B | GPIO1_IO07 |
| LCD1_DATA21 | KEY_COL0 | KEY_ROW1 | GPIO1_IO06 | VSS | GPIO1_IO05 | QSPI1A_DATA3 |
| LCD1_DATA22 | KEY_COL1 | KEY_COL4 | GPIO1_IO01 | GPIO1_IO02 | GPIO1_IO10 | GPIO1_IO09 |
| KEY_ROW3 | KEY_ROW2 | KEY_COL3 | GPIO1_IO03 | GPIO1_IO11 | GPIO1_IO00 | VSS |

Table 124. 14 x 14 mm Ball Map (continued)

| N | M | L | K | J | H |
|-------------------|-------------|---------------|---------------|-------------|------------------|
| DRAM_DQM0 | DRAM_SDWE_B | DRAM_SDCLK0_N | DRAM_SDCLK0_P | DRAM_RAS_B | DRAM_SDQS1_N 1 |
| DRAM_CAS_B | DRAM_SDBA1 | DRAM_ADDR09 | DRAM_CS1_B | DRAM_SDBA2 | DRAM_ZQPAD 2 |
| VSS | DRAM_ADDR11 | VSS | VSS | DRAM_ADDR13 | VSS 3 |
| DRAM_ADDR06 | DRAM_ADDR02 | DRAM_CS0_B | DRAM_VREF | DRAM_ADDR08 | DRAM_ADDR10 4 |
| DRAM_ADDR00 | DRAM_ADDR12 | DRAM_SDCKE0 | DRAM_ADDR03 | DRAM_SDCKE1 | DRAM_ADDR04 5 |
| NVCC_DRAM | NVCC_DRAM | NVCC_DRAM | NVCC_DRAM | NVCC_DRAM | NVCC_DRAM 6 |
| VSS | VSS | VSS | NVCC_DRAM_2P5 | VSS | VSS 7 |
| VDD_SOC_CAP | VDD_SOC_CAP | VDD_SOC_CAP | VDD_SOC_CAP | VDD_SOC_CAP | VDD_SOC_CAP 8 |
| VDD_SOC_CAP | VDD_SOC_IN | VDD_SOC_IN | VDD_SOC_IN | VDD_SOC_IN | VDD_SOC_CAP 9 |
| VDD_SOC_CAP | VDD_SOC_IN | VSS | VSS | VDD_ARM_IN | VDD_ARM_CAP 10 |
| VDD_SOC_CAP | VDD_SOC_IN | VSS | VSS | VDD_ARM_IN | VDD_ARM_CAP 11 |
| VDD_SOC_CAP | VDD_SOC_IN | VDD_ARM_IN | VDD_ARM_IN | VDD_ARM_IN | VDD_ARM_CAP 12 |
| VSS | VDD_SOC_CAP | VDD_ARM_CAP | VDD_ARM_CAP | VDD_ARM_CAP | VDD_ARM_CAP 13 |
| ADC1_IN0 | VSS | VSS | VSS | VSS | VSS 14 |
| ADC2_IN2 | LCD1_DATA05 | LCD1_DATA09 | LCD1_DATA12 | LCD1_HSYNC | NVCC_CSI_LCD1 15 |
| CCM_PMIC_STBY_REQ | LCD1_DATA06 | LCD1_DATA11 | LCD1_DATA13 | LCD1_VSYNC | LCD1_DATA15 16 |
| VDD_HIGH_CAP | VSS | LCD1_DATA01 | LCD1_DATA14 | VSS | LCD1_DATA20 17 |
| VDD_HIGH_CAP | LCD1_DATA02 | PCIE_VP_CAP | LCD1_DATA08 | LCD1_RESET | VDD_ARM_IN 18 |
| LCD1_DATA04 | LCD1_DATA00 | LCD1_CLK | LCD1_DATA10 | LCD1_DATA07 | KEY_ROW4 19 |
| LCD1_DATA03 | LCD1_DATA17 | LCD1_DATA18 | LCD1_ENABLE | LCD1_DATA19 | LCD1_DATA16 20 |

Table 124. 14 x 14 mm Ball Map (continued)

| Y | W | V | U | T | R | P |
|--------------|---------------|--------------|---------------|----------------|--------------|------------------|
| VSS | DRAM_DQM2 | DRAM_SDQS2_P | DRAM_DATA02 | DRAM_ODT0 | DRAM_ADDR14 | DRAM_SDQS0_P |
| DRAM_DATA21 | DRAM_DATA23 | DRAM_SDQS2_N | DRAM_DATA01 | DRAM_DATA00 | DRAM_DATA03 | DRAM_SDQS0_N |
| DRAM_DATA18 | DRAM_DATA20 | VSS | DRAM_DATA04 | VSS | VSS | DRAM_DATA06 |
| DRAM_DATA16 | DRAM_DATA17 | VSS | DRAM_DATA19 | DRAM_DATA22 | DRAM_DATA05 | DRAM_DATA07 |
| USB_H_DATA | USB_H_STROBE | NVCC_USB_H | NAND_DATA03 | NAND_DATA05 | VSS | DRAM_ADDR01 |
| NAND_READY_B | NAND_ALE | NAND_DATA00 | VSS | NAND_DATA07 | NVCC_NAND | NVCC_DRAM |
| NAND_DATA02 | NAND_DATA04 | NAND_WP_B | NAND_CE0_B | NAND_WE_B | NAND_CLE | VSS |
| NAND_DATA06 | NAND_DATA01 | JTAG_TRST_B | NAND_RE_B | NAND_CE1_B | JTAG_MOD | VSS |
| JTAG_TDO | JTAG_TMS | VDD_SOC_CAP | VSS | NVCC_JTAG | JTAG_TCK | VSS |
| SD4_DATA0 | SD4_DATA5 | SD4_RESET_B | SD4_DATA6 | SD4_CLK | JTAG_TDI | VSS |
| SD4_DATA1 | SD4_DATA7 | SD3_CLK | SD3_DATA7 | SD3_DATA1 | SD3_DATA0 | VSS |
| SD4_DATA4 | SD4_CMD | SD3_DATA6 | VSS | NVCC_SD4 | NVCC_HIGH | VSS |
| SD4_DATA2 | SD4_DATA3 | NVCC_LOW | SD3_DATA5 | SD3_CMD | VDDA_ADC_3P3 | ADC1_IN3 |
| SD3_DATA2 | ADC1_IN2 | ADC_VREFL | SD3_DATA4 | SD3_DATA3 | ADC2_IN1 | SNVS_TAMPER |
| ADC_VREFH | ADC2_IN0 | TEST_MODE | VSS | ADC1_IN1 | ADC2_IN3 | SNVS_PMIC_ON_REQ |
| BOOT_MODE0 | BOOT_MODE1 | CCM_CLK2 | ONOFF | NGND_KEL0 | POR_B | GPANAIO |
| RTC_XTALI | RTC_XTALO | VDD_USB_CAP | USB_OTG2_VBUS | USB_OTG1_CHD_B | VSS | VDD_HIGH_IN |
| VSS | VSS | VSS | NVCC_PLL | VDD_SNVS_CAP | VDD_SNVS_IN | VDD_HIGH_IN |
| USB_OTG2_DN | USB_OTG2_DP | USB_OTG1_DN | VSS | XTALI | VSS | CCM_CLK1_P |
| VSS | USB_OTG1_VBUS | USB_OTG1_DP | VSS | XTALO | VSS | CCM_CLK1_N |

7 Revision History

Table 125 provides a revision history for this data sheet.

Table 125. i.MX 6SoloX Data Sheet Document Revision History

| Rev. Number | Date | Substantive Change(s) |
|-------------|---------|---|
| 4 | 10/2018 | <p>Changes for this revision include:</p> <ul style="list-style-type: none"> • Table 1, “Part Number Nomenclature—i.MX 6SoloX,” on page 4, – Part Differentiator section: Removed VADC column.” • Section 4.12.6.1.1, “MII Receive Signal Timing (ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER, and ENET_RX_CLK)” on page 83, and Section 4.12.6.1.2, “MII Transmit Signal Timing (ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER, and ENET_TX_CLK)” on page 83 – Removed sentence: Additionally, the processor clock frequency must exceed twice the ENET_RX_CLK frequency.” • Table 6, “Absolute Maximum Ratings,” on page 21, – Row VDD_SNVS_IN: Corrected maximum value from 3.4V to 3.6V. • Table 24, “XTALI and RTC_XTALI DC Parameters,” on page 39, – Row: XTALI input leakage current at startup, I_{XTALI_STARTUP}: Changed from “... driven 32KHz RTC clock @ 1.1V” to “...driven 24 MHz clock at 1.1V.” • Table 56, “eMMC4.4/4.41 Interface Timing Specification,” on page 80, – Row: SD2, uSDHC Output Delay: Changed t_{OD} from 2.5ns minimum to 2.8ns and 7.1ns maximum to 6.8ns. • Table 67, “LCDIF Display Interface Signal Mapping,” on page 90, – Rows LCD_D23 and LCD_D22: Corrected Column 24-bit DOTCLK LCD IF from G[7] to R[7] and G[6] to R[6]. |

Table 125. i.MX 6SoloX Data Sheet Document Revision History (continued)

| Rev. Number | Date | Substantive Change(s) |
|-------------|---------|---|
| 3 | 09/2017 | <ul style="list-style-type: none"> • Minor formatting updates and editorial corrections throughout. • Removed references of 'NTSC/PAL analog video input interface' from features and throughout. • Removed support of Video ADC (VADC) and TVDECODE throughout. • Replaced ipp_dse with DSE throughout. • Section 1, "Introduction": Replaced LVDDR3 with DDR3L in text description. • Table 1: Added orderable part numbers in the Ordering Information table. • Figure 1: <ul style="list-style-type: none"> – Changed the Part Differentiator table's ADC column to include channel count. – Included Rev 1.4 in Silicon Revision section • Figure 2: Removed VADC and TV Decoder blocks from the block diagram. • Section 1.2, "Features": <ul style="list-style-type: none"> – Modified "Displays" information <i>from</i> "Total two interfaces available" <i>to</i> "Total three interfaces available". Also added "Two parallel 24-bit display ports, each up to 1080P at 60 Hz" to the list. Removed "One Parallel 24-bit display port, up to dual WXGA at 60 Hz". – Clarified the Miscellaneous interfaces <i>from</i> "Two 4-channel ...(ADC)" <i>to</i> "Up to two 4-channel ...(ADC)". • Table 6: <ul style="list-style-type: none"> – IO Supply for DDR Interface row, added the footnote "The absolute maximum voltage includes an allowance for 400 mV of overshoot on the IO pins. Per JEDEC standards, the allowed signal overshoot must be de-rated if NVCC_DRAM exceeds 1.575V." – IO Supply for RGMII Interface row, maximum value <i>from</i> 2.725 V <i>to</i> 3.7 V. – Input/Output Voltage Range row, split the row into DDR and non-DDR and added the corresponding details. – 1.2V supply for video A/D converter row, removed – 3.3V supply for video A/D converter row, parameter name changed to 3.3V supply for analog circuitry. • Table 10: <ul style="list-style-type: none"> – GPIO supplies row, added NVCC_NAND to the Symbol column. – Video A/D converter supply row, removed • Table 13: Following rows removed: VDD_AFE_1P2, VDDA_AFE_3P3 • Table 57: SDR50/SDR104 Interface Timing Specification table, changed duplicate SD2 to SD3. Minor format changes to minimum and maximum columns for SD2 and SD3 rows. • Updated introductory text of the following sections: Section 4.6.4.1, "LPDDR2 Mode I/O DC Parameters", Section 4.6.4.2, "DDR3/DDR3L Mode I/O DC Parameters", Section 4.7.2, "DDR I/O AC Parameters", Section 4.8.3, "DDR I/O Output Buffer Impedance". • Corrected Figure 19, "Asynchronous A/D Muxed Write Access," on page 58 • Table 56: Minimum value of 'uSDHC Input Setup Time' corrected to 1.7ns. • Added Section 4.12.5.4, "HS200 Mode Timing". • Added Section 4.12.9.1, "LCDIF Display Interface Signal Mapping". • Removed phrase "Case x" from figure titles of all package diagrams. Also updated the diagrams with NXP branding. • Table 112: <ul style="list-style-type: none"> – Made the following ball positions Reserved: K21, L21, N18. • Table 113: <ul style="list-style-type: none"> – Made the following balls Reserved: L23, L22, K23, and K22. • Table 114: <ul style="list-style-type: none"> – Made the following balls Reserved: K21, K22, K23, L21, L22, L23, N18. |

Table 125. i.MX 6SoloX Data Sheet Document Revision History (continued)

| Rev. Number | Date | Substantive Change(s) |
|-------------|---------|---|
| 2 | 06/2016 | <ul style="list-style-type: none"> • Changed throughout: <ul style="list-style-type: none"> - VDD_AFE_3P3 to VDDA_AFE_3P3 - VDDAD to VDDA_ADC_3P3 • Table 1, changed all instances of “2N19K” to “2N19K or 3N19K”. • Figure 1, added new row under Silicon Rev, “Rev 1.3 Production...” • Table 2, i.MX 6SoloX Modules List: <ul style="list-style-type: none"> - BCH, deleted “encryption/decryption” in Brief Description column - eCSPI1-eCSPI5: deleted “with data rate...” in Brief Description column - uSDHC1-uSDHC4: added “Conforms to the SD...” - uSDHC1-uSDHC4: deleted 7th and 8th paragraphs - uSDHC1-uSDHC4: added “Each port is placed...” • Table 3, Special Signal Considerations <ul style="list-style-type: none"> - Signal Name, GPANAI0: updated text to “Analog output for NXP...” - Signal Name, POR_B: deleted second sentence • Section 3.2, “Recommended Connections for Unused Analog Interfaces”, removed text and original table, Recommended Connections for Unused Analog Interfaces, and referred reader to the Hardware Development Guide. • Section 4.1.1, “Absolute Maximum Ratings” <ul style="list-style-type: none"> - added new CAUTION - updated Table 6, Absolute Maximum Ratings • Section 4.1.2, “Thermal Resistance”, added NOTE • Table 7, 19x19 mm (VM)...., corrected Junction to Package Top value 0.2 to 2 • Table 8, 17x17 mm NP (VO)...., corrected Junction to Package Top value 0.2 to 2 • Table 9, 14x14 mm (VK)...., updated Junction to Package Top value 0.2 to 2 • Table 10, Operating ranges, USB supply voltages: changed 5.25 to 5.5 • Table 13, Maximum Supply Currents <ul style="list-style-type: none"> - added text: Use Maximum IO equation - added footnotes • Section 4.2.1, “Power-Up Sequence”, - Removed references to the internal POR function. Internal POR is not supported on the i.MX 6SoloX.” <ul style="list-style-type: none"> - Deleted bullets 4 and 5 • Section 4.3.2.3, “LDO_USB”, changed 5.25 to 5.5 • Section 4.6.1, “XTALI and RTC_XTALI (Clock Inputs) DC Parameters”, added new NOTE. • Table 24, XTALI and RTC_XTALI DC Parameters, added new footnote, “This voltage specification...” • Section 4.10, “Multi-mode DDR Controller (MMDC)” this new section added, replacing the original section 4.9.4 DDR SRAM Specific Parameters (DDR3/DDR3L and LPDDR2). • Table 57, SDR50/SDR104 Interface...., changed SD2 Min and max values to 0.46 and 0.54. Changed SD5 Max to 0.74. • Table 64, RGMII Signal Switching Specifications, deleted footnote 1. • Table 79, Master Mode SAI Timing: <ul style="list-style-type: none"> - changed S1 Min value to 20 - changed S3 Min value to 2 x S1 <p><i>(continued on next page)</i></p> |

Table 125. i.MX 6SoloX Data Sheet Document Revision History (continued)

| Rev. Number | Date | Substantive Change(s) |
|-------------|---------|---|
| 2 | 06/2016 | <p><i>(continued from previous next page)</i></p> <ul style="list-style-type: none"> • Table 80, Slave Mode SAI Timing: <ul style="list-style-type: none"> - changed title from Master Mode Timing to Slave Mode SAI Timing - changed S11 Min value to 20 - added new row, S19 - added new footnote • Figure 63, SAI Timing — Slave Modes: added S19 • Table 94, 12-bit ADC Operating Conditions: changed Supply Voltage Min value to 3.0 • Table 108, SD/MMC boot through USDHC4, changed Signal Names from usdhc3.DATA4 - usdhc3.DATA7, to usdhc4.DATA4 - usdhc4.DATA7 • Table 112, 19x19 mm Supplies Contact Assignments: changed GPANAIO Remark from “Test signal...” to “Analog output for NXP use...” • Table 113, 19x19 mm Functional Contact Assignments: DRAM_SDCLK_0, updated “Input” to “Output” and Value to “0” • Table 116, 17x17 mm NP (no PCIe) supplies contact assignments: <ul style="list-style-type: none"> - GPANAIO: changed remark from “Test signal...” to “Analog output for NXP use...” - VDD_SOC_CAP: deleted L9 - VDD_SOC_IN: added L9 - DRAM_SDCLK0_P: updated “Input” to “Output” and Value to “Low” • Table 119, 17x17 mm WP (with PCIe) supplies contact assignments: <ul style="list-style-type: none"> - GPANAIO: changed remark from “Test signal...” to “Analog output for NXP use...” - VDD_SOC_IN: added L9 • Table 120 17x17 mm WP (with PCIe) Functional Contact Assignments, DRAM_SDCLK0_P: updated “Input” to “Output” and Value to “Low” • Table 122 14x14 mm supplies contact assignments: <ul style="list-style-type: none"> - added rows ADC_VREFL and PCIE_CP_CAP - VDD_HIGH_CAP: added N18 - VDD_HIGH_IN: added P18 - VDD_SOC_IN: added L9 • Table 123, 14x14 mm Functional Contact Assignments, DRAM_SDCLK0_P: updated “Input” to “Output” and Value to “Low” <ul style="list-style-type: none"> - RGMII1_TX_CTL: updated to D10 |

Table 125. i.MX 6SoloX Data Sheet Document Revision History (continued)

| Rev. Number | Date | Substantive Change(s) |
|-------------|--------|---|
| 1 | 7/2015 | <ul style="list-style-type: none"> • Throughout: <ul style="list-style-type: none"> – Updated Arm Cortex-M4 core operation speed as 227 MHz – Corrected signal name from NVCC_LVDS_2P5 to NVCC_LVDS – For supply rail NVCC_LOW, corrected supply input voltage from 3.3 V to 1.8 V • On page 2, in the list of i.MX 6SoloX features, updated the first bullet, adding that FreeRTOS can be run on the Cortex-M4. • Table 1, “Ordering Information,” on page 3: <ul style="list-style-type: none"> – Updated Cortex-M4 core operation speed as 227 MHz – Added footnote on “Cortex-A9 Speed” column • In Section 1.2, “Features”: <ul style="list-style-type: none"> – Corrected second bullet under “External memory interfaces” to say, “16-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size, BA-NAND, PBA-NAND, LBA-NAND, OneNAND and others. BCH ECC up to 62 bits. 16-bit boot is supported from OneNAND. 8-bit boot is supported from other NAND types.” – Corrected second bullet under “USB” to say, “One HS-IC USB (High Speed Inter-Chip USB) host” – Corrected first bullet under “Miscellaneous IPs and interfaces” to say, “Three SSIs and two SAls supporting up to five I2S or AC97 ports” – Updated ninth bullet under “Miscellaneous IPs and interfaces” to say, “Two Gigabit Ethernet Controllers (designed to be compatible with IEEE AVB standards and IEEE Std 1588®), 10/100/1000 Mbps” • Updated Section 2.1, “Block Diagram”: <ul style="list-style-type: none"> – In “Shared Peripherals” block, corrected from UART(5) to UART(1) and added ASRC and ESAI. In “AP Peripherals” block, added UART(5) and eCSPI(1). – Updated note regarding number of module instances • Updated Table 2, “i.MX 6SoloX Modules List,” on page 10 • In Table 3, “Special Signal Considerations,” on page 18: <ul style="list-style-type: none"> – In XTALI/XTALO row, added references to engineering bulletin and reference manual – In row for NVCC_LVDS_2P5, corrected signal name to NVCC_LVDS and updated remarks • Updated Table 5, “Recommended Connections for Unused Analog Interfaces,” on page 21: <ul style="list-style-type: none"> – Deleted row for RTC – Added row for NVCC_USB_H – Updated footnote pertaining to PCIe • Updated Table 6, “Absolute Maximum Ratings,” on page 21: <ul style="list-style-type: none"> – Added footnote pertaining to “Symbol” column – Updated maximum value for VDD_SNV5_IN supply voltage • Updated Table 10, “Operating Ranges,” on page 26. Table reformatted since previous release; not a specification change. • In Section 4.1.4, “External Clock Sources,” added caution about use of the internal RTC oscillator vs. an external crystal. • Updated Table 14, “Low Power Mode Current and Power Consumption (LDO Bypass Mode),” on page 31 • In Section 4.5.2, “OSC32K,” <ul style="list-style-type: none"> – Added caution about use of the internal RTC oscillator vs. an external crystal – Updated description of result when the clock monitor determines that the OSC32K is not present – Removed text pertaining to ~3 V coin-cell battery • Updated Table 24, “XTALI and RTC_XTALI DC Parameters,” on page 39 <p><i>(continued on next page)</i></p> |

Table 125. i.MX 6SoloX Data Sheet Document Revision History (continued)

| Rev. Number | Date | Substantive Change(s) |
|-------------|--------|--|
| 1 | 7/2015 | <p><i>(continued from previous page)</i></p> <ul style="list-style-type: none"> • Updated Table 45, "EIM Asynchronous Timing Parameters Relative to Chip Select," on page 59. Elaborated to show results of calculations. No specification change. • In Table 64, "DDR3/DDR3L Read Cycle," on page 93, updated minimum value for DDR26 • Added note regarding ECSPiX_MOSI to Figure 36, "ECSPI Master Mode Timing Diagram," on page 73 • Added note regarding ECSPiX_MISO to Figure 37, "ECSPI Slave Mode Timing Diagram," on page 74 • Updated Figure 42, "SDR50/SDR104 Timing," on page 81 • In Table 68, "LVDS Display Bridge (LDB) Electrical Specification," on page 92: <ul style="list-style-type: none"> – Corrected units for V_{OH} values from 'mV' to 'V' – Corrected units for V_{OL} values from 'mV' to 'V' • In Section 4.12.21, "USB PHY Parameters," in list of amendments to Rev. 2 of the The USB PHY meets the electrical compliance requirements defined in revision 2.0 of the <i>USB On-The-Go and Embedded Host Supplement to the USB 2.0 Specification</i>, added "Portable device only" under "Battery Charging Specification" • Added Table 111, "Signals with Different States During Reset and After Reset," on page 131 • In Table 113, "19x19 mm Functional Contact Assignments," on page 137, corrected GPIO signal names • In Table 116, "17x17 mm NP (no PCIe) Supplies Contact Assignments," on page 156, added ball L9 to the VDD_SOC_CAP row • In Table 123, "14 x 14 Functional Contact Assignments," on page 190, corrected power group for SD2 ball names to 'NVCC_SD1_SD2' |
| 0 | 2/2015 | <ul style="list-style-type: none"> • Initial public release |