S12ZVM High Current Evaluation Board

High Performance High Current Motor Control

by: NXP Semiconductors

1. Introduction

This user guide introduces the High Current Evaluation Board for motor control applications based on the S12ZVMx MCU. This board is designed to drive 3-Phase BLDC / PMSM motors in power range up to 1kW. The MCSXSR1CS12ZVM offers low cost development solution for motor control applications enabling implementation of various motor control techniques.

- Sensorless control
 - PMSM field-oriented control using BEMF observer for mid- and high-speed operation
 - BLDC block commutation using non-active phase voltage monitoring for zero-crossing using an internal GDU channel
 - BLDC block commutation using zerocrossing comparators
- Sensor-based control
 - Resolver signal monitoring including reference signal generation
 - o Hall-switch sensor signal monitoring

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1.1. EVB features

The MCSXSR1CS12ZVM Board provides the following functionalities:

- S12ZVMx MCU with integrated Gate Driver Unit
- Phase current capability up to 75 A_(RMS)
- Automotive connectivity interfaces LIN/CAN
- Reverse polarity protection circuitry
- Conditioning circuitry for the motor control specific values measurement
- Headers for MCU pin accessibility
- Resolver / Hall position sensor interfaces.
- LEDs indicators and debugging headers
- DC-link shunt configuration for BLDC or for PMSM phase current reconstruction.
- OSBDM debugging interface
- USB-to-SCI serial port interface for the application control monitoring
- Robust high current screw terminals for DC-link input and 3-Phase output
- Boost option to support supply voltage range down to 3.5 V

1.2. MCSXSR1CS12ZVM board architecture

The MCSXSR1CS12ZVM Board contains the basic building blocks shown in *Figure 1*.

The various block colors differentiate a block functionality:

- Blue MCU and application software download, and the debug interface
- Green Motor control related hardware + 3-Phase power bridge
- Red Board power supply
- Violet Application control
- Gray Interfaces & terminals

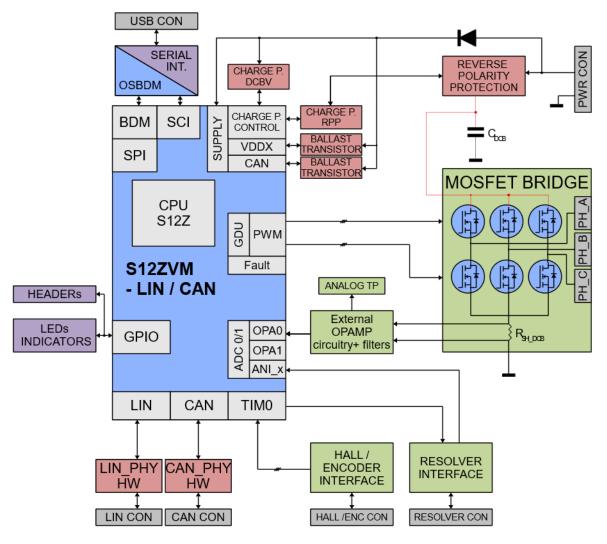


Figure 1. MCSXSR1CS12ZVM block diagram

The MCSXSR1CS12ZVM evaluation board is supplied by power bolt terminals in the range of 8 to 18 Volts (3.5 V - 18 V if the boost option is enabled). The board includes reverse polarity protection circuit, boost inverter for low voltage operation (VBAT < 10 V), charge pump for the Gate Driver Unit (GDU). Implementation of the ballast transistors increases the power output of the internal voltage regulators and helps to reduce thermal stress of the MCU. The MCU also integrates a Gate Driver Unit to drive the power MOSFETs directly from the MCU pins, using external bootstrap capacitors and diodes on the high side FETs. The GDU module includes a Charge Pump to enable 100% duty cycle driving on the high side FETs. The GDU outputs are internally controlled by the Pulse Width Modulator (PWM) with Fault Protection module (PMF) inside the MCU. DC-link current signal is connected to the MCU-integrated operational amplifier with externally adjusted gain to fit -125 A to 125 A range. For the on-board block location, see *Figure 3*.



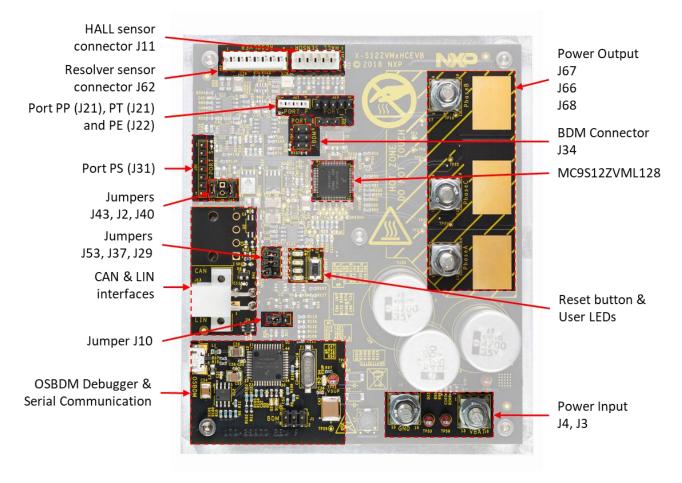
Figure 2. MCSXSR1CS12ZVM

Table 1.	S12ZVML128 specifications
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Parameter	Value	Parameter	Value
FLASH 128 kB		EVDD	1 ch. 5 V / 10 mA (source)
RAM	8 kB	PMF	6ch, 15-bit PWM
EEPROM	512 B	12 V VREG	12 V / 70 mA, 170 mA with
Core	S12Z		ballast, 3.5 – 20 V capable
Package	LQFP-64	ADC	2x16 ch, 12-bit SAR
LIN-Phy	1	Trigger Unit	2x PTU
Comms	2x SCI, 1xSPI	GDU	3/3
Temp	+175°C Tj (Grade 0)		

Table 2. MCSXSR1CS12ZVM specifications

Parameter	Min	Typical	Max
Supply voltage (*boost option enabled)	3.5* / 8 V	12 V	18 V
Phase current	-	75 A(rms)	105 A(peak)
Ambient temperature	0°C	20°C	45°C
Board temperature (passive heat sink mounted)	-	-	150°C
Communications (**S12ZVMC used)	LIN / CAN**, USB (as virtual RS232), SCI, SPI, BDM		
Rotor speed or position sensors	3 Hall-switch sensors, Resolver		
Digital I/O, debugging	15		



2. MCSXSR1CS12ZVM PCB Description

Figure 3. MCSXSR1CS12ZVM block locations on PCB

2.1. Default jumpers configuration

The following table show the proper jumper configuration.

Table 3.	MCSXSR1CS12ZVM board configuration
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Jumper	Function	Description	Default state
J2	CAN Voltage regulator jumper	Connect VSUP voltage to ballast transistor of the CAN voltage regulator Note: Applicable for S12ZVMC version of MCU	Open
J10	BOOTLOADER enable jumper	Switch the OSBDM to BOOT mode for OSBDM programing	Open
J29	VDDX_BDM supply jumper	Connect VDDX voltage to supply OSBDM circuitry	Open
J37	User LED _2 jumper	Connect USER LED_2 [D14] to PS[5] pin	Closed

Jumper	Function	Description	Default state
J40	VDDX regulator jumper	Connect VSUP voltage to ballast transistor of the CAN voltage regulator	Closed
J43	VSUP2 regulator jumper	Connect VSUP voltage to VSUP2 voltage regulator for resolver circuit	Closed
J53	User LED _1 jumper	Connect USER LED_1 [D15] to PS[4] pin	Closed

Table 3. MCSXSR1CS12ZVM board configuration

NOTE

For the jumpers location, see Figure 3.

MCSXSR1CS12ZVM supports all LQFP-64 package versions of the MCU. Depending on the MCU S12ZVMC / S12ZVML, the board should be populated with zero-ohm resistors for the proper functionality and work condition. For more information, see Section *3.9 Automotive communication interfaces*.

2.2. Headers and connectors

The following sub sections summarize the on-board headers, connectors and their pin-outs and signal meanings.

2.2.1. Programming interfaces

The MCSXSR1CS12ZVM is equipped with two programming / debugging connectors. Connector J34 is dedicated for the application programming and extended debugging purposes of S12ZVM microcontroller. Connector J1 is dedicated for downloading and updating the firmware for the built-in MC9S08JM based OSBDM debugger / serial communication interface. Both programing interfaces use standard six pin dual row header is shown in the following figure.



Figure 4. BDM programming header

In most of the cases, it is sufficient to use built-in OSBDM interface for programming and debugging the S12ZVM. It is necessary to flash the OSBDM bootloader firmware first in order to use this interface. For more details, please see chapter *4 On-board OSBDM Debugging Interface*.

Table 4. 514. 5122 via programming and debugging connector description					
J34 pin	BDM Signal Name	S12ZVM Package Signal	Description		
1	BKGD	MODC/BKGD	Bidirectional		
2	GND	-	Ground		
3	PDO	PS5/PDO/~SS0/KWS5	Bidirectional		
4	RESET_B	RST	Input		
5	PDOCLK	PS4/PDOCLK/SCK0/KWS4	Bidirectional		
6	VDDX_BDM	-	Power pin		

Table 4.	134. G127\/M	programming and	debugging c	onnector description
Table 4.	J34. 3122 V IVI	programming and	a debugging co	Simector description

J1 pin	BDM Signal Name	S12ZVM Package Signal	Description
1 BKGD		BKGD	Bidirectional
2	GND	-	Ground
3	-	-	Not connected
4	U_RESET	RST	Input
5	-	-	Not connected
6	+5VU	-	Power pin

Table 5. J1: OSBDM programming connector description

2.2.2. Power supply and power output

In order to reduce power losses and to overcome heating of terminals, The MCSXSR1CS12ZVM board is populated with power bolts with metric screw M5 for wiring ring-eye terminal. Please use appropriate wires (max 10 A/mm²) and high conductivity terminals to connect your power source and load. See the following figure for more information.



Würth Elektronik, part No.96285

Figure 5. Power bolt

Table 6. J3, J4, J66-J68 power input and output terminals

Terminal	Signal Name	Description
J3	VBAT	Power supply (+) pin
J4	GND	Power supply (-) pin
J66 PHASE_A		Power output Phase A
J67	PHASE_B	Power output Phase B
J68	PHASE_C	Power output Phase C

2.2.3. Rotor position sensors interface

There are two interfaces for rotor position sensors on the MCSXSR1CS12ZVM:

- 3-channel Hall-switch sensor interface with 5 V / up to 10 mA supply, see 3.8 Hall sensors
- 5 V Resolver interface with reference signal generator and signal processing, see 3.7 Resolver



Molex, part No.22-27-2061 Mating connector: part No.22-01-2061

22-01-2067

22-01-3067

Figure 6. Hall sensor connector

MCSXSR1CS12ZVM PCB Description

Terminal	Signal Name	S12ZVM Package Signal	Description
1	VCC	EVDD	Supply (+) pin
2	GND	-	Supply (-) pin
3	HALL_A	PT1	Input signal Hall A
4	HALL_B	PT2	Input signal Hall B
5	HALL_C	PT3	Input signal Hall C
6	-	-	Not connected

Table 7. J11: Hall-switch Sensor Interface Connecto



Molex, part No.22-27-2081 Mating connector: part No.22-01-2087 22-01-3087

Figure 7. Resolver sensor connector

Table 8.	J62: resolver Sensor Interface Connector	
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Terminal	Signal Name	S12ZVM Package Signal Description	
1	RES_GENP	-	Square signal 10kHz output
2	RES_GENM		Generated by PT0 pin
3	RES_SIN	-	Resolver sine signal input
4	RES_SIN_REF		Connected to POS_SIN signal and to PAD3
5	RES_COS	-	Resolver cosine signal input
6	RES_COS_REF		Connected to POS_COS signal and to PAD8
7	GND	-	Supply (-) pin
8	+5VA	-	Supply (+) pin

2.2.4. USB OSBDM / Serial Interface

USB interface features OSBDM connection for programming and debugging S12ZVM application and a virtual serial communication driver e.g. for runtime debugging using the FreeMASTER tool.



Molex, part No.47589-0001 Mating connector: USB Micro-B

Table 9.	J7: USB OSBDM/Serial	connector
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Terminal	Signal Name	MC9S08JM Package Signal	Description
1	+5VU	VDD1 / VDDAD	Supply 5V
2	OSBDM_USB_DN	USBDN	USB Data +
3	OSBDM_USB_DP	USBDP	USB Data -
4	-	-	-
5	GND	GND	Supply (-)

2.2.5. LIN communication interface

The LIN communication interface is connected with the S12ZVML LIN-physical layer, therefore it can be used only with S12ZVML128, S12ZVML64, S12ZVML32 or S12ZVML31 (all in LQFP-64 package). By default, the MCSXSR1CS12ZVM is populated with S12ZVML128.



Molex, part No.39-29-5043 Mating connector: part No. 39-01-2040 39-01-2045 39-01-3042 39-01-3045

Figure 9. LIN connector

Table 10. J3: L	N connector
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Terminal	Signal Name	S12ZVML Package Signal	Description
1	LGND	LGND	LIN ground pin
2	LGND	LGND	LIN ground pin
3	NC	-	-
4	LIN	LINO	LIN data signal

2.2.6. CAN communication interface

The CAN communication interface is connected with the S12ZVMC version featuring CAN VREG, therefore it can be used only with S12ZVMC128 or S12ZVMC64 (both in LQFP-64 package). By default, the MCSXSR1CS12ZVM is populated with S12ZVML128 and CAN-related components are not populated. Thus, changes in the PCB configuration have to be done in order to use the CAN interface (see *3.9 Automotive communication interfaces*).



Molex, part No.39-30-3047 Mating connector: part No. 39-01-4040

Figure 10. CAN connector

Table 11.	J8:	CAN	connector

Terminal	Signal Name	S12ZVML Package Signal	Description
1	MSCAN_H	CANH	CAN-Hi signal
2	MSCAN_L	CANL	CAN-Lo signal
3	GND	-	Ground
4	NC	-	-

3. Application Consideration

This chapter provides additional information about the functional blocks of the MCSXSR1CS12ZVM board. All design considerations can be found in details in *AN5207: Hardware Design Guidelines for S12ZVM Microcontrollers*. For details on the circuitry and design, please refer to the www.nxp.com/MCSXSR1CS12ZVM.

3.1. MC9S12ZVM family

The MC9S12ZVM-Family is an automotive 16-bit microcontroller family using the NVM + UHV technology that offers the capability to integrate 40 V analog components. This family reuses many features from the existing S12/S12X portfolio. The particular differentiating features of this family are the enhanced S12Z core, the combination of dual-ADC synchronized with PWM generation and the integration of "high-voltage" analog modules, including the voltage regulator (VREG), Gate Drive Unit (GDU), and either Local Interconnect Network (LIN) physical layer or CAN Physical layer. These features enable a fully integrated single chip solution to drive up to six external power MOSFETs for BLDC or PMSM motor drive applications.

By default, MCSXSR1CS12ZVM features MC9S12ZVML128 in LQFP-64 package. Thanks to the pin compatibility inside the family, following members can be used and evaluated with this board.

FLASH Size	RAM Size	LIN-Phy Enabled	CAN Enabled	
128kB	8kB	ZVML128	ZVMC128	
64kB	4kB	ZVML64	ZVMC64	
32kB	4kB	ZVML32, ZVML31	-	

Table 12. MC9S12ZVM Family for MCSXSR1CS12ZVM

Please be aware of differences between part numbers and mask sets. For more information, please refer to the *MC9S12ZVM-Family Reference Manual and Datasheet*.

The MCSXSR1CS12ZVM is designed to highlight various features of MC9S12ZVM family, especially:

- S12Z core with 100 MHz core / 50 MHz bus frequency, optimized for motor control algorithms in fixed point, supporting six-step control of BLDC or field-oriented control (FOC) of PMSM motors in sensor or sensorless configuration
- Scalable memory options from 32 kB to 128 kB of FLASH to support applications from compact up to complex algorithms
- Internal oscillator for cost sensitive applications or external crystal option for CAN node applications
- On-chip voltage regulator (VREG) for regulation of input supply and all internal voltages Optional VREG ballast transistor control output to support more power consumption on the output. Optional boost converter to support operation down to 3.5 V of VBAT
- Controllable 10 mA high-current output (EVDD1) for use as Hall sensor or other 5 V supplied sensors/devices
- Dedicated 6-channel 15-bit pulse-width modulator with fault protection (PMF module) supporting variable edge placement or double-switching
- Integrated gate drive unit (GDU) capable of switching 73 nC MOSFETs @20 kHz PWM using double-switching pattern for phase current reconstruction

- Integrated operational amplifiers and ADCs with 12-bit resolution, with synchronization and sample scheduling using programmable trigger unit (PTU) and PMF
- Battery voltage and phase voltages monitors (using ADC) for more robust sensorless BLDC control or detecting rotor position of unpowered motor (windmilling)
- LIN physical interface with capability of PWM interface
- MSCAN module (1 Mbit/s, CAN 2.0 A, B software compatible) with dedicated CAN VREG (S12ZVMC versions only)
- Resolver / Hall sensor support for sensor-based motor control applications

Full list of features is available in the MC9S12ZVM-Family Reference Manual and Datasheet.

3.2. Power input and reverse battery protection

Input power is connected to the board using J3 and J4. The MCU is supplied via input L-C filter (C44 – L7), polarity protection diodes (D6 for the boost option, D7 for the MCU) and the decoupling capacitors (C43 and C38) to VSUP bus (TP43). The power traces are routed to the reverse battery protection MOSFET (Q9), which is controlled by the charge pump and protected by the transistor Q10.

Charge pump of D16, D17, C35 and C40 is protected by R-C filter R4-C7 from voltage peaks generated on the HD pin.

DC-bus consists of three 4.7 mF capacitors and a 22 μ F decoupling capacitor and creates the main source of voltage for the power converter. DC-bus capacitors can be replaced for debugging purposes (C28 and C118 placeholders).

3.3. 3-phase power bridge

Power bridge is designed for supplying 3-phase AC motors up to 75 A(rms) or 105 A(peak) phase current (up to 120 A(peak) for protection, ± 125 A scale), which is approx. 1 kW of electric input power to the motor. The power bridge consists of three complementary MOSFET legs (half-bridges).

Low-side (bottom) MOSFETs are driven by low-side drivers of the GDU; each gate is connected to the LGx pin of the MCU via gate resistor to limit the gate current. LSx pins are connected to I_DCB bus bar. Please be aware that the I_DCB (-) potential relative to the GND floats with the voltage drop on the shunt resistor R71. Optionally, gate capacitors can be populated to increase the gate capacitance in order to slow down the switching process.

High-side (top) MOSFETs are driven by high-side drivers of the GDU. The gates are connected to the HGx pins via gate resistors with optional gate capacitors. HSx pins are connected to the source pins of the MOSFETs via decoupling resistor, which helps to protect the drivers from ringing on the motor phases.

High-side drivers are supplied by a bootstrap circuits connected to the VLS, VBSx and HSx pins of the MCU. R-C filters are implemented to protect the bootstrap circuitry and especially the internal voltage regulator from voltage peaks on the PHASE_x signals.

In order to start switching in complementary mode correctly, the bootstrap circuitry should be initialized by switching on the low-side MOSFETs first. Otherwise, the high-side driver might be unable to switch on the high-side MOSFET until the low-side MOSFET is switched on for the first time. Please note that in an off-state of the MOSFETs, the bootstrap capacitors discharge over time (depending on the capacitance, parasitic and intrinsic resistance of the circuitry).

Each MOSFET is equipped with a snubber circuit consisting of two parallel resistors and a capacitor. The two parallel resistor placeholders enable more precise tuning of the snubber.

VBSx pins are protected by R-C filters R225-C141, R227-C142 and R229-C143 from voltage peaks generated during the MOSFET switching. If not populated, high voltage may pass through the bootstrap capacitors C25, C19 and C22 and damage the VLS circuitry in high voltage / high current situations as shown on *Figure 14*. Resistors R225, R227 a R229 can be used to tune the bootstrap capacitors charging.





Figure 11. MOSFET BUK7J1R4-40H

Table	13.	BUK7J1R4-40H	basic pa	rameters	

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{DS}	Drain-to-source voltage	25° C≪Tj≪175° C	-	-	40	V
ID	Drain current	V _{GS} =10V; T _{mb} =25°C	-	-	190	Α
P _{TOT}	Total power dissipation	T _{mb} =25° C	-	-	395	W
RDSon	Drain-to-source resistance	V _{GS} =10V; I _D =25A; T _j =25°C	0.74	1.06	1.4	mΩ
Q _{G(TOT)}	Total gate charge	I _D =25 A; V _{DS} =32 V; V _{GS} =10 V	-	73	103	nC

3.4. Boost option

The GDU module integrates the necessary hardware to build a boost converter with external components in case of low voltage condition. The external components needed are two Schottky diodes, one coil, and capacitors. The boost converter clock which is driving the internal transistor T1 is derived from the bus clock. This clock can be divided down as described in the *MC9S12ZVM-Family Reference Manual and Datasheet*, Table 18-10. The boost converter also includes a circuit to limit the current through coil. This current limit can be adjusted with the bits GBCL[3:0] in the GDUBCL register. For more details, see GDU electrical parameters and *MC9S12ZVM-Family Reference Manual and Datasheet*.

The boost circuitry is shown in *Figure 12*. It is designed according to the example given in the *AN5207: Hardware Design Guidelines for S12ZVM Microcontrollers*, Chapter 7.7.1. The switching frequency should be set to 500 kHz, while the current limitation is 70 mA and the operation is enabled down to 3.5 V. Register settings recommended for MCSXSR1CS12ZVM is shown in *Table 14*. Please note that the inductor is being switched and may induce some additional heating, acoustic noise or EMC issues during operation (typically below 10.1 V). The circuitry is provided for evaluation purposes.

To enable the boost circuitry, a set of register settings has to be done with proper values.

Table 14.	MC9S12ZVM register settings	for MCSXSR1CS12ZVM boost optic	on

Register	Bit	Setting	Notes
GDUE	GFDE	1	Set by default
GDUE	GBOE	1	Enables the boost option

Register	Bit	Setting	Notes
GDUCLK1	GBOCD[4:0]	10110	f _{bus} / 100 = 50 MHz / 100 = 500 kHz
GDUCLK1	GBODC[1:0]	00	50% duty cycle
GDUBCL	GBCL[3:0]	0000	ILIM_typ = 190 mA (see RM, GDU Electrical Specifications, Table E-1, rows 25)

Table 14. MC9S12ZVM register settings for MCSXSR1CS12ZVM boost option

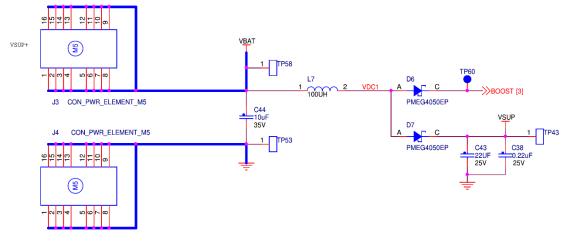


Figure 12. Boost circuit

3.5. Ballast transistor Option

MC9S12ZVM Family features an external ballast device support to reduce internal power dissipation. External circuitry is implemented on MCSXSR1CS12ZVM according to the *AN5207: Hardware Design Guidelines for S12ZVM Microcontrollers*, Chapter 3.2.3, and can be seen on *Figure 13* in combination with VSUP part on *Figure 12*. Similar circuitry is provided for the VDDC CAN power supply.

On MCSXSR1CS12ZVM, the VDDX domain supplies the device I/O pins including EVDD and VDDA, where VDDA supplies the ADC and internal bias current generators. Typically, external ballast transistor option is needed if the EVDD pin requires high current (up to 10 mA). Since the usage of external ballast is derived from the power dissipation calculation, it is recommended to follow the guidance in *MC9S12ZVM-Family Reference Manual and Datasheet*, Appendix A.1.8.

In order to use the external ballast, jumper J40 must be closed (jumper J2 for VDDC option respectively). In software, following register bits of the CPMUVREGCTL must be configured after the system startup. Voltage is then controlled automatically. Please note that on MCSXSR1CS12ZVM, the VDDX domain provides supply to all the digital I/O pins, LED diodes D3, D5, D14 and D15, EVDD1 pin (Hall sensors) and resolver input circuitry.

Register	Bit	Setting	Notes
CPMUVREGCTL	EXTXON	1	Set by default – enables external ballast
CPMUVREGCTL	INTXON	1	Set by default – enables internal regulator

Table 15. MC9S12ZVM register settings for MCSXSR1CS12ZVM ballast option

Application Consideration

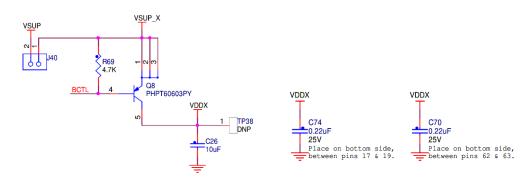


Figure 13. Ballast option circuit

3.6. Current sensing

Current sensing circuitry is designed for DC-link current sampling according to the *MTRCKTSPNZVM128 Three-phase Sensorless Single-Shunt Current-Sensing PMSM Motor Control Application with MagniV MC9S12ZVM (AN5327).* Current scaling is ±125 A(peak) with usable range up to 105 A(peak) or 75 A(rms) continuously. Dedicated shunt resistor is used to convert current into a voltage signal, which is then amplified using an integrated operational amplifier.

In field-oriented control (FOC), all three legs of the power converter are active and the DC-link current is then a combination of the phase currents, which in general can flow in both directions. Therefore, an offset reference circuit is implemented to shift the signal in the single-ended range.

Power inverter circuit involves many parasitic parameters, which influence overall performance. Some of these parameters can be reduced by proper design (PCB layout and tracing), careful component selection, tuning of the switching and additional circuitry (RC filters, snubbers, etc.).

In case some of the parasitic components are not reduced sufficiently, ringing and voltage peaks may be induced mainly around the power path. Considering complementary switching, the power path can be simplified to the DC bus capacitor, MOSFET switches and the shunt resistor. Only parasitic inductance is introduced, thus sharp changes to the voltages can induce voltage peaks or ringing, which is then propagated to the current sensing circuitry as well as superposed to different stages of the power bridge, as indicated on *Figure 14*. In specific conditions (e.g. high temperature, high current), overvoltage limits may be violated even if it stays within the limits in normal operational conditions.

Voltage peaks over parasitic inductances sum up from the GND up to the overall peak, which compromises external capacitors as well as internal circuitry of the S12ZVM GDU and its voltage regulator.

Typical parasitic components (Mainly inductance):

- Self-inductance of shunt resistor
- Self and mutual inductance of PCB power traces
- Self and mutual inductance of wires and connectors

Application Consideration

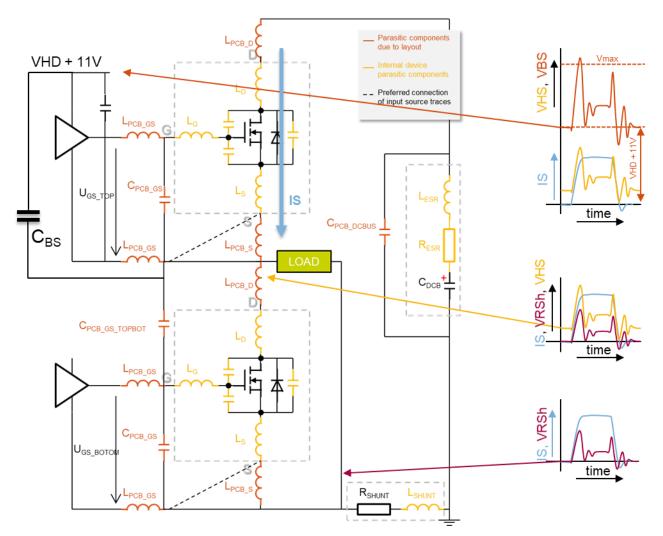
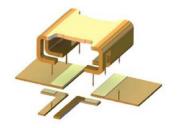


Figure 14. Parasitic components of one leg of a power stage

Optional filters are introduced in the *MC9S12ZVM-Family Reference Manual and Datasheet* as well as in the hardware design guidelines. These are implemented in the MCSXSR1CS12ZVM design and were discussed earlier.

3.6.1. Shunt resistor parameters

Resistive current sensor with Kelvin connection is used to sense the DC-link current. The Kelvin connection helps to improve precision of the measurement due to the reduced effect of the solder joint between PCB and shunt resistor terminals. High accuracy current measurement is required for the field oriented motor control techniques and other advanced motor control algorithms. Selected type also introduces very low parasitic inductance of the active part of the shunt resistor.



Isabellenhütte BVB-M-R001-0.2

Figure 15. Shunt resistor BVB-M-R001-0.2

3.6.2. Current sensing circuitry

Current sensing circuitry takes benefit of the internal operational amplifier of the MCU and provides signal conditioning for bipolar current sensing using the shunt resistor. The gain of the amplifier is scaled to fit in ± 2.5 V and shifted by $U_{REF} = 2.5$ V to fit the ADC input range of 0 - 5 V. The current scale of the MCSXSR1CS12ZVM is set to $I_{MAX} = \pm 125$ A (peak).

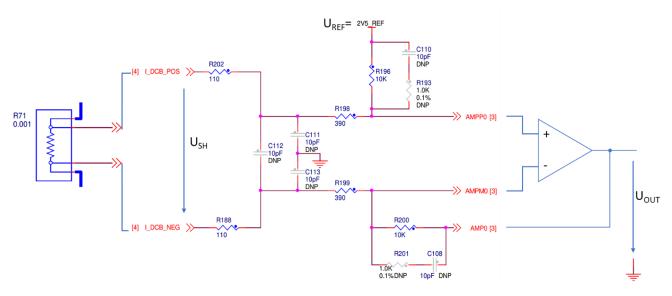


Figure 16. Current sensing circuitry

Eqn. 1 $U_{OUT} = A \cdot U_{SH} + U_{REF} = I_{MAX} \cdot R_{71} \cdot Gain + U_{REF}$

Eqn. 2
$$R_{71} \le \frac{\Delta P_{MAX}}{I_{RMS}^2}$$
 $R_{71} \le \frac{12W}{100A^2} = 0.0012\Omega \rightarrow R_{71} = 0.001\Omega$

Eqn. 3
$$Gain = \frac{U_{OUT} - U_{REF}}{I_{MAX'}R_{71}} = \frac{5 - 2.5}{125 \cdot 0.001} = 20$$

The current scale should be derived from the maximal current of the system including fault range of the current (acceptable overcurrent). Amplified signal is internally processed by the overcurrent comparator (see *MC9S12ZVM-Family Reference Manual and Datasheet*, chapter 18.4.8). Based on the GDUOCn_GOCT0 register settings, the threshold can be set from 3.75 V (2.5 V for GDUV5 and V6) to

5 V, which corresponds to +125 A (0 A for GDUV5 and V6) to +125 A for given scale. Nevertheless, due to the ringing on the signal as described previously, voltage peaks induced on the parasitic inductance of the shunt resistor may trigger the overcurrent fault even if the current is below the limit. False overcurrent detection depends on many factors, mainly the shape of the overvoltage peak. Since the parasitic inductance cannot be neglected, the aim of the following paragraphs is to make the peak as short as possible to be positioned beyond the bandwidth of the operational amplifier and/or with minimal amplitude.

Basic current sensing circuitry is provided by default. However, in specific cases, troubleshooting or benchmarking, additional signal conditioning may be required. Some guidance is provided on custom design of the circuitry and on-board configuration tuning. *Figure 17* shows layout of the shunt resistor signals on the MCSXSR1CS12ZVM board.

- Parasitic inductance of the shunt resistor in power electronics applications is determined by the mutual inductance of sensing wire loop and the power current loop.
- The sensing wires, from shunt resistor to RC network and op. amplifier must be thick i.e. (20-30) mils
- The length of sensing wires, from shunt resistor to op. amplifier must be as short as possible and crossing these wires with another noise wires (charge pump etc.) must be avoided/minimized.
- Suitable type of a shunt resistor shall be used, targeting as low parasitic inductance as possible.
- Dimensions of a shunt resistor also play an important role in its parasitic inductance.
- Number of vias in the sensing path should be minimized. Each via contributes to the total parasitic inductance.

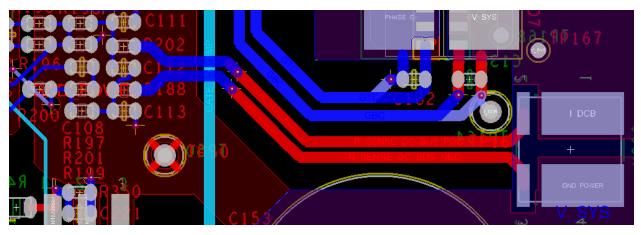


Figure 17. Layout of Shunt Resistor Signal Path

Placement of the C111, C112, C113 is optional. Recommended value of C112 is 100 pF; the capacitors C111 and C113 should be approx. 10 times lower than C112 (thus 10 pF). Together with R202 and R188, the RC network is understood as an input impedance. The purpose of this input impedance is to compensate the influence of parasitic inductance, mainly by capacitors. The change of R202 and R188 resistance contributes to the character of input impedance, but it influences the gain of the sensing circuit. In case of high value of parasitic inductance, the compensation using capacitors may be insufficient. Wrong selection of resistors and capacitors values can cause additional noise. If the sensing signal does not consist any or just a small noise, the capacitors can be skipped. Input impedance tuning is based on trial & error method.

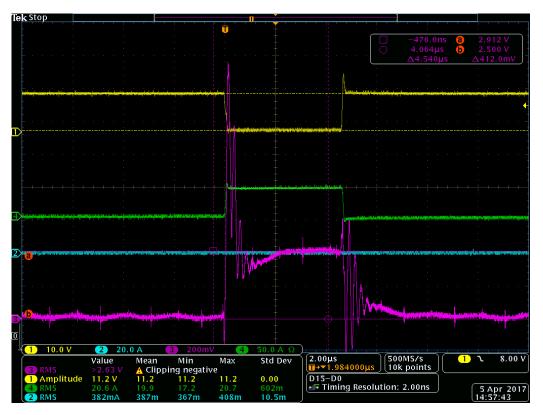


Figure 18. Noise on a Shunt Resistor with Wrong Input Impedance

Figure 18 introduces a test of an initial setup. The violet waveform represents induced voltage on a shunt resistor, amplified by the S12ZVM internal op amp. The ringing of the signal is caused by wrong values of capacitors C111, C112, C113. The yellow waveform represents U_{DS} voltage of the top MOSFET.



Figure 19. Noise on a Shunt Resistor with Tuned Input Impedance

After tuning of the input impedance, the noise in signal is mitigated (*Figure 19*). (C111 and C113 = 10pF and C112 = 100pF) The transient time of the violet signal depends mainly on the parasitic inductance and parameters of the operational amplifier.

Evaluation was performed using a simple switching algorithm, where first leg of the inverter was switched in complementary mode and bottom MOSFET of the second leg was switched-on. The top MOSFET of the second leg was switched-off and the R-L load was connected between the two phases.

3.7. Resolver

Resolver hardware can be viewed as two inductive position sensors, which, upon a supplied sinusoidal shaped signal on the input, generate two sinusoidal signals on the output. The output signals' amplitudes depend on the position of the shaft. The amplitude of one signal is proportional to the sine. The amplitude of the other signal is proportional to the cosine of the shaft angle position.

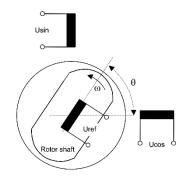


Figure 20. Resolver Principle Schematic

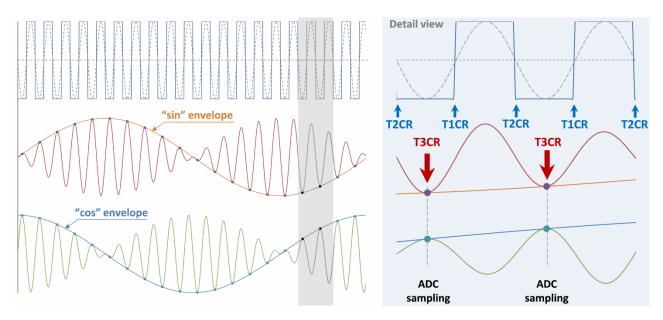


Figure 21. Resolver Operation Principle

The input (excitation) signal to a resolver, called a resolver reference voltage, and the output signals can be computed according to a few simple equations:

Eqn. 4 $U_{ref} = U_{amp} \sin(\omega t)$

Eqn. 5
$$U_{sin} = K. U_{ref} \sin(\Theta)$$

Eqn. 6
$$U_{cos} = K. U_{ref} \cos(\Theta)$$

As the sine and cosine of the shaft angle position are provided, it can be computed directly by applying the inverse tangent function to the amplitudes of the resolver output voltages. The calculation needs to take into account the signs of the measured amplitudes in order to place the computed angle position correctly within a single 360 degree rotation:

Eqn. 7
$$\Theta = \operatorname{atan}\left(\frac{U_{sin}}{U_{cos}}\right)$$

The second method (algorithm), widely used for estimation of the rotor angle and speed, is generally known as an Angle Tracking Observer, see *56F80x Resolver Driver and Hardware Interface*.

Figure 21 shows resolver operation principle in details. Sine and cosine signals contain the 10 kHz carrier (excitation) frequency, which can be easily removed when the sampling is synchronized with the excitation signal generator. Further information on application software design can be found in *56F80x Resolver Driver and Hardware Interface.*

In order to use the resolver circuitry, jumper J43 must be closed. The excitation signal circuitry is supplied by VSUP. Please note that the input signal conditioning circuitry is supplied from VDDX domain.

3.7.1. Hardware interface

An interface for direct connection of the resolver position sensor with the S12ZVMx is discussed here. This interface circuit generates/shapes the signal for the resolver reference winding and conditions signals from sin/cos windings for measurement by the on chip ADC module.

The interface circuit consists of two main parts:

- Resolver driving circuits, see *Figure 22*
- Resolver sin/cos signals conditioning circuits, see *Figure 23*

The resolver driving circuitry shapes a rectangular reference signal from the controller Timer Module (channel IOC0) output to a sinusoidal waveform. The U22A stage is a 3rd order Sallen-Key Low-pass filter which transforms the rectangular signal into a sinusoidal wave with DC offset. The U22B stage generates a virtual ground as a reference for the input signal to achieve symmetrical voltage supply for operational amplifiers. The U10A stage is a voltage-follower, i.e. buffer, to increase the output current for the resolver reference winding. The U10B stage is a differential amplifier for removal of a direct current voltage component in sinusoidal reference signal. The resolver reference winding is connected between output U10A and U10B. The resistors R191 and R192 control the Q factor of filter. The cut-off frequency for filter is set by R92, R94, R195, C48, C49 and C114 components.

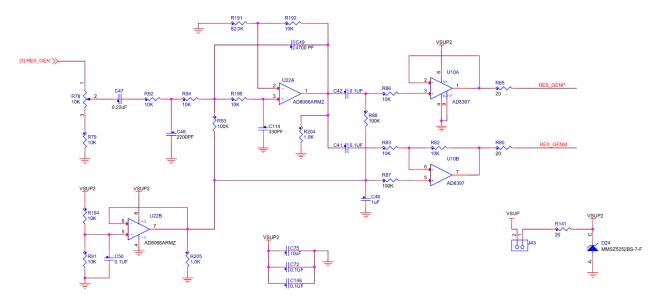


Figure 22. Resolver Driving Circuits

The resolver sin/cos signals conditioning circuitry adjusts voltage levels from resolver sin/cos signals to the range acceptable by the on-chip ADC module. It also carries out level shifting, which places a zero level of the signals to the middle of the ADC range. U9A, U9B amplifiers act as differential unity amplifiers with output level referenced to virtual ground (middle of the VCCA 5V). U9A, B amplifiers are rail-to-rail (AD8656) or similar ones capable of 5V single supply operation. The capacitors C31, C94 and C30, C94, C96 add low pass filtering to suppress unwanted high frequency noise, which is often present in systems with power electronics. For measurement sin/cos signals from resolver circuits are used ADC0 (AN0_3) and ADC1 (AN1_1).

The cut-off frequency of the U9A and U9B amplifiers is set according to the resolver reference frequency and should be well above it not to affect resolver signals. U9A, B amplifiers should be placed as close as possible to the ADC inputs to avoid noise crosstalk from other components.

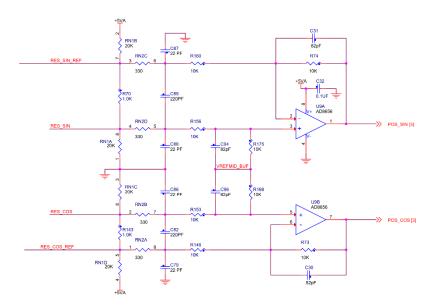


Figure 23. Resolver Sin/Cos signals conditioning circuits

All values of the schematics component given in *Figure 22* and *Figure 23* are designed for 10 kHz resolver reference frequency (half of the usual motor control PWM frequency), resolver ratio 2:1. This interface might be adjusted in cases when reference signal frequency or the resolver transformation ratio is different. The gain of the resolver signal conditioning circuitry is unity and therefore the levels on the sin/cos signal inputs must have peak-to-peak amplitude up to the ADC reference voltage (with small headroom to avoid limiting).

Driving circuitry introduces a phase shift between timer output signal and resulting resolver reference waveform. This phase shift together with resolver phase shift and signal conditioning circuitry phase shift are corrected in Programable Trigger Unit (PTU) relative to the ADC sampling point, which is in most motor control applications synchronized to PWM. In this way, the sampling at peaks of the sin/cos signals is ensured, resulting in better achieved resolution. See *Figure 24*.

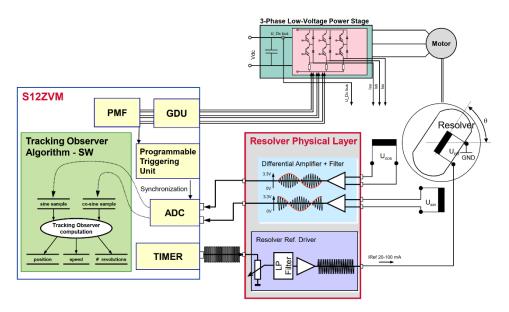


Figure 24. Resolver signal processing on S12ZVM

3.8. Hall sensors

Hall sensors are used to obtain speed and position of the BLDC motors. Because the rotor is a permanent magnet, it is a very simple matter to determinate where the physical pole edge. For speed calculation using Hall sensors see *BLDC six-step control speed scaling using S12ZVM*.

3.8.1. Hardware interface

For processing signals from Hall sensors or Encoder sensor are using passive low pass filters for removing alternating components of the signals. RC filter composed of R121, C62, R128, C64 and R130, C66. For power supply Hall sensors is used EVDD1 pin (PP0). This is a high current, low voltage drop output intended for supplying external devices in a range of up to 10mA. Configuring the pin direction as output automatically enables the high current capability.

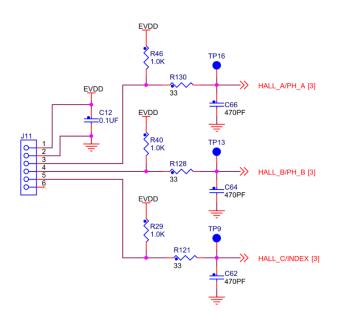


Figure 25. Hall sensors circuits

3.9. Automotive communication interfaces

MCSXSR1CS12ZVM board introduces two major automotive edge-node communication interfaces: LIN and CAN. The S12ZVM family supports both interfaces with two family members. Dedicated family member shall be populated along with certain external components. LIN configuration is populated by default. More details are summarized in the following table.

Component	LIN	CAN
U7	S912ZVML12F3MKH (default)	S912ZVMC12F3MKH
	S912ZVML12F3WKH	S912ZVMC12F3WKH
	S912ZVML64F3MKH	S912ZVMC64F3MKH
	S912ZVML64F3WKH	S912ZVMC64F3WKH
	S912ZVML32F3MKH	
	S912ZVML32F3WKH	
R32	DNP ¹	0R
R33	0R (default)	DNP (default)
R41	0R (default)	DNP (default)
R42	DNP	0R
R34	DNP	0R
R35	DNP	0R

Table 16.	LIN and CAN Hardware Interface Configuration	
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¹ DNP = Do not populate

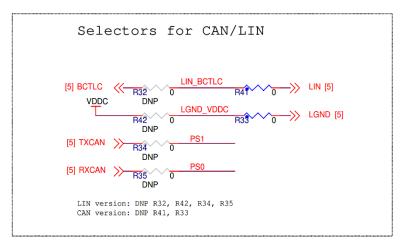


Figure 26. LIN/CAN Interface Selection

3.9.1. LIN physical interface

LIN (Local Interconnect Network) provides simple, single wire serial communication interface compliant with LIN Physical Layer 2.2 specification and with the SAE J2602-2 LIN standard. The LIN communication interface can be used only if the S12ZVML version of the assembled MCU.

The same physical interface can be used as SAE J1850 or a simple PWM command interface by routing the LIN signal to the internal timer channel in capture mode.

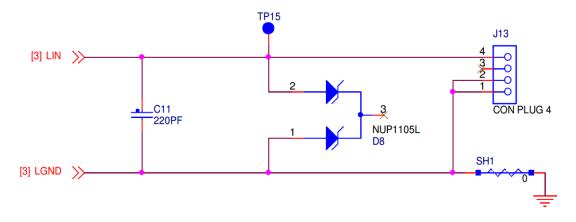
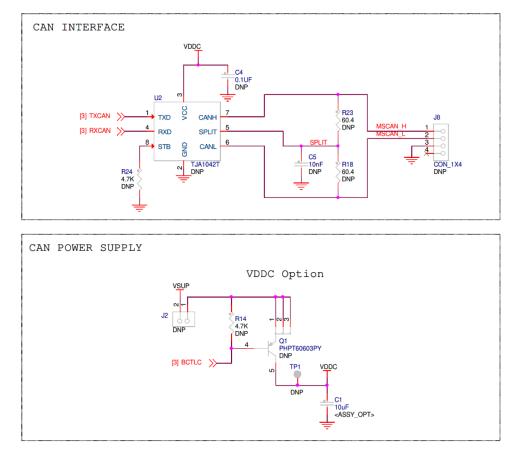


Figure 27. LIN physical interface schematics

3.9.2. CAN physical interface

The CAN (Controller Area Network) communication interface extends the functionality of the board and provides two-wire CAN-bus connectivity for the standard automotive hi-speed data transfer applications up to 5 Mbit/s. Used transceiver is fully compliant with ISO 11898-2:2003 and ISO 11898-5:2007 standard. The CAN communication interface can be used only if the S12ZVMC version of the



MCU is assembled. A set of CAN-related components have to be populated. It is recommended to populate VDDC ballast option as well. See *3.5 Ballast transistor Option* for more details.

Figure 28. CAN Physical Interface Related Schematics

4. On-board OSBDM Debugging Interface

Built-in OSBDM debugging interface is provided to support debugging or flashing the software and to implement the USB-to-Serial communication interface using single USB cable. The OSBDM microcontroller (U1, MC9S08JM60CLD) is preloaded with the necessary OSBDM software. In case of damage and replacement of the microcontroller, the software has to be flashed using connector J1 and external BDM debugger first (e.g. P&E MICRO Multilink and CodeWarrior Flash command). The OSBDM software package is available at http://www.pemicro.com/osbdm/.

In normal operation, jumper J10 is open and the OSBDM is ready to flash, debug or create a virtual serial communication interface with connected PC. In case the OSBDM software is outdated, the P&E driver will prompt you to close the J10, disconnect and reconnect the USB connector and follow the update process (follow instructions on the screen).

When connected to the computer, USB device installs virtual serial communication port as well. If not recognized by your system, please download the latest drivers for your system at <u>http://www.pemicro.com/osbdm/</u>.

NOTE

For some versions of the OSBDM software, debugging session should not be active at the same time as the virtual serial communication. If using FreeMASTER or other serial communication interface via OSBDM driver, please make sure that the communication is stopped and resources released before the debugging session is initiated.

5. Application Support

5.1. Toolset

NXP Semiconductors provides a set of documentation and software tools to speed up your development. More documents and software can be found at <u>S12ZVM web page</u>.

ΤοοΙ	Description
https://www.nxp.com/magniv	S12Z MagniV web page
MC9S12ZVMRM	MC9S12ZVM-Family Reference Manual and Datasheet
S12ZCPURM	CPU S12Z Reference Manual – Core Reference Manual
AN5207	Hardware Design Guidelines for S12ZVM Microcontrollers
CodeWarrior Legacy Suite	CodeWarrior for MCUs (Eclipse IDE) – Development Environment for S12 MagniV
AN5330	Migration Guide for S12ZVM Devices: Migrating between family members
AN5327	MTRCKTSPNZVM128 Three-phase Sensorless Single-Shunt Current-Sensing
	PMSM Motor Control Application with MagniV MC9S12ZVM
AN5327SW	AN5327 MTRCKTSPNZVM128 Application note software
www.nxp.com/MCSXSR1CS12ZVM	MCSXSR1CS12ZVM software package (Single-shunt PMSM FOC sensorless
	control, BLDC six-step sensorless control)
www.nxp.com/MCSXSR1CS12ZVM	MCSXSR1CS12ZVM board schematics and design files
https://www.nxp.com/automcdevkits	Automotive Development Kits web page
https://www.nxp.com/ammclib	Automotive Math and Motor Control Library Set web page
https://nxp.com/freemaster	FreeMASTER Run-time debug tool
MCAT	MCAT: Motor Control Application Tuning tool
AN4912	Tuning 3-Phase PMSM Sensorless control application using MCAT Tool
AN5122	Using NXP's LIN Driver with the MagniV Family
AN5201	Integrating the LIN driver with BLDC sensorless motor controller
AN5176	Using the High Voltage Physical Layer – PWM communication
AN4975	Using MSCAN on the MagniV Family

Table 17. Recommended documentation and software tools

5.2. Step-by-step instructions

- 1. Download and install software
 - 1.1. CodeWarrior for MCUs (Eclipse IDE) v11.x
 - 1.2. FreeMASTER 3.0 or higher
 - 1.3. MCSXSR1CS12ZVM_SW package (includes the latest AMMCLib installation)
- 2. Check the jumper settings (see *Table 3*)
- 3. Connect the power supply

- 3.1. Use 12 V power supply with stabilized output and appropriate power range. Laboratory DC power supply of 12 V / 20 A is a good fit for 200 W application. Please note that charging the DC-bus capacitors may induce high current peak
- 3.2. Voltage source can be adjustable within range of 8 to 18 V (or 3.5 to 18 V in case the boost option of S12ZVM is enabled)
- 3.3. Use M5 ring-eye connectors and proper wiring (recommended current density is 10 A/mm²). Use shielded cables or other methods to prevent emission if needed
- 3.4. The power-on sequence may induce high charging current to charge the DC-bus capacitors.
- 3.5. LED D4 (yellow) indicates the supply voltage (12 V input). Integrated voltage regulator working properly is indicated by LED D3 (green)
- 4. Connect the USB Cable
 - 4.1. Connect MCSXSR1CS12ZVM to the PC using the USB cable. Allow the PC to automatically configure the USB drivers if needed. In case of drivers not found, please visit http://www.pemicro.com/osbdm/ and follow the instructions to install proper drivers
 - 4.2. When the OSBDM is properly connected to the PC, both LED D1 (green) and D2 (yellow) are lightning
- 5. Re-program the MCU using CodeWarrior for MCUs
 - 5.1. Start CodeWarrior for MCUs
 - 5.2. Click File Import
 - 5.3. Select General Existing Projects into Workspace and click Next
 - 5.4. Select root directory: Navigate to the installed application software directory: ${InstallPath}\MC_DevKits\MCSXSR1CS12ZVM\sw$
 - 5.5. Select either MCSXSR1CS12ZVM_PMSM or MCSXSR1CS12ZVM_BLDC
 - 5.6. Select Copy project into workspace
 - 5.7. Click Finish
 - 5.8. **Build and Run** the software using **Debug** button. When the application is downloaded, the debugger stops at the first line of the code. Click **Run** to continue the program and then click **Disconnect** to release the USB resources
 - 5.9. In case of error, try to reconnect the USB cable or check the P&E Micro drivers are installed properly. If the MCU is not responding, check the LED indicators and voltages using a multimeter or an oscilloscope
- 6. Start the FreeMASTER application
 - 6.1. Open FreeMASTER project <selected project> FreeMASTER_control\MCSXSR1CS12ZVM_PMSM_SW_CW11.pmp by clicking File – Open Project
 - 6.2. Click the green **GO** button in the FreeMASTER toolbar or press CTRL+G to enable the communication

- 6.3. Successful communication is signalized in the status bar at the very bottom as "RS232 UART Communication;COMn; speed = 19200"
- 6.4. Check the system voltage indicated on the **App Control** panel of the MCAT window. It should correspond with the DC power source voltage. On the App Control panel, check the
- 6.5. In case of board not responding, please make sure the program is running and the debugger is not active (in CodeWarrior: Debug-Run-Disconnect). Check the FreeMASTER project **Options** for RS232 settings as indicated above
- 7. Connect and run the motor
 - 7.1. Switch off the power
 - 7.2. Connect the motor to the J66-J68 terminals. Please note that the order of phases impacts the direction of rotation. See *Figure 29*
 - 7.3. Use M5 ring-eye connectors and proper wiring (recommended current density is 10 A/mm²). Use shielded cables or other methods to prevent emission if needed
 - 7.4. Switch on the power and reconnect the USB connection using FreeMASTER
 - 7.5. Follow the AN5327 MTRCKTSPNZVM128 Three-phase Sensorless Single-Shunt Current-Sensing PMSM Motor Control Application with MagniV MC9S12ZVM and AN4912 Tuning 3-Phase PMSM Sensorless control application using MCAT Tool to start with the motor control application tuning. Please note that the default algorithm settings are not generic to any motor. The motor parameters and control loop settings shall be set before the motor is started
 - 7.6. Typical initial test requires at least
 - Parameters tab: Align voltage set to 0 V, see *Figure 30*
 - Control Structure tab: Scalar control enabled, see Figure 31
 - Control Structure tab: V/rpm_factor set to the lowest value of 25%, see *Figure 31*
 - Control Structure tab: Speed_req set to a small speed (e.g. 100 RPM), see Figure 31
 - Turn on the switch and check the current waveforms using FreeMASTER Recorder. If no current is induced, then either increase the V/rpm_factor or Speed_req by small steps, see Figure 32



Figure 29. Motor Connection to the MCSXSR1CS12ZVM

Motor 1: PMSM O						Tuning	Mode:	Expert	~
ntroduction Parameters C	Current Loop	Speed Loop	Sensorless	Control Struc	Output File	App Co	ontrol		
		Input App	olication P	arameters					
Motor Parameters			SW F	ault Triggers					
pp	2	[-]	UDO	B trip		16	M		
Rs		[Ω]	UDO	B under	The state	1100	M		
Ld	0.000375	[H]	UDO	Bover		17	M		
Lq	0.000435	[H]	I ph	over		5	[A]		
ke	0.0135281	[V.sec/rad]	Tem	p over		110	[°C]		
J	0.12e-4	[kg.m2]							
lph nom	2.3	[A]	1986	ication Scales					
Uph nom	17	[V]	kt		0.010614 [Nm/A				
N nom	2000	[rpm]	N ma		State Card		[rpm]		
Hardware Scales			Ema	ix		36	[V]		
	105		— Aligr	ment					
I max	00000	[A]	Alig	voltage		0	IVI		
U DCB max		[V]		duration		to and	[sec]		
Temp max	645.2	[.c]							
Update Target			Reload Data			Store			

Figure 30. MCAT Parameters Page with Align Voltage Set to 0 V

Expert 🗸	ning Mode:	Tuni					PMSM O	Motor 1:
	p Control	Output File App	Control Struc	Sensorless	Speed Loop	Current Loop	Parameters	ntroduction
			Structure	on Control	Applicatio			
			e Composition	ontrol Structure	- Cascade Co		ntrol	- State Co
[%]	25 ↑↓	V/rpm_factor		atrol	Scalar Cor		ON	
[V]	0.213	Uq_req			Scalar CO			
[rpm]	100	Speed_req			view			
[V]	0	Ud_req	DISABLED	oc	Voltage F		0	
[V]	0	Uq_req	DISABLED		view		OFF	
[A]	0	ld_req		oc 🖌	Current F			
[A]	0	lq_req	DISABLED		view	ate	olication St	App
			C	oc 🖉	Speed F		READY	
[rpm]	0	Speed_req	DISABLED		view			1
~	sensories	Position & Speed	DISABLED		Position & S			

Figure 31. MCAT Control Structure Page with Initial Scalar Control Settings

Application Support

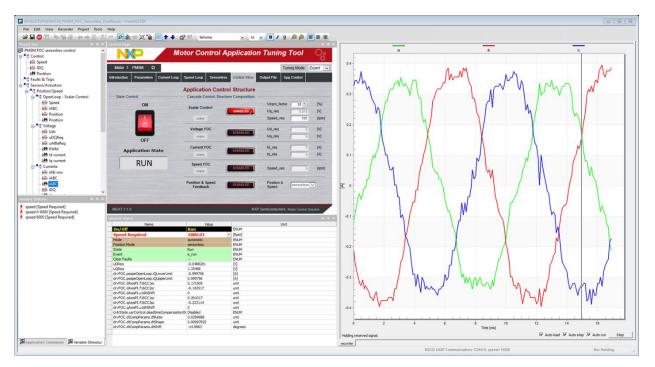


Figure 32. FreeMASTER iABC Current Waveforms in Recorder