MEST2G-020-15

Pin Diode Switch Element

Rev. V1

Features

- Supports up to 20 W Power
- Low Insertion Loss: 0.2 dB up to 2.7 GHz
- High Isolation: 18 dB up to 2.7 GHz
- RoHS* Compliant

(2012)
Plastic Molded DFN

Description

A broadband medium power switch element in a 1.9 x 1.1 mm DFN package. This device is electrical series and thermal direct to ground (EST2G). This device is designed for wireless infrastructure applications and test instruments. It is also suited for other applications from 100 MHz up to 6 GHz.

Electrical Specifications: T_C = +25°C (unless otherwise specified)

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Breakdown Voltage (V_{BR})	I_R = 10 µA	V	100	—	—
Lifetime (t)	I_F = 10 mA, I_R = 6 mA, 10% / 90%	ns	—	50	—
Series Resistance (R_S)	I_F = 100 mA, 50 MHz	Ω	—	1.2	—
Junction Capacitance (C_J)	V_R = -10 V, 1 MHz	pF	—	0.08	—
Insertion Loss (I_L)	I_F = 50 mA, 2.3 ~ 2.7 GHz I_F = 50 mA, <6 GHz	dB	—	0.2 0.3	0.3 —
Input Return Loss (IR_L)	I_F = 50 mA, 2.3 ~ 2.7 GHz I_F = 50 mA, <6 GHz	dB	23 18	27 22	—
Isolation (I_{SO})	V_R = -10 mA, 2.3 ~ 2.7 GHz V_R = -10 mA, <6 GHz	dB	15 10	18 12	—

* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

Absolute Maximum Ratings[1,2]

Parameter	Absolute Maximum
Breakdown Voltage (V_R)	100 V
Forward Current (I_F)	100 mA
Theta (θ_{JC})	65°C/W
Junction Temperature (T_J)	175°C
Storage Temperature (T_{STG})	-65°C to +150°C
Mounting Temperature (T_{MTG})	+260°C per JEDEC STD-J-20C

1. Exceeding any one or combination of these limits may cause permanent damage to this device.
2. MACOM does not recommend sustained operation near these survivability limits.

Handling Procedures

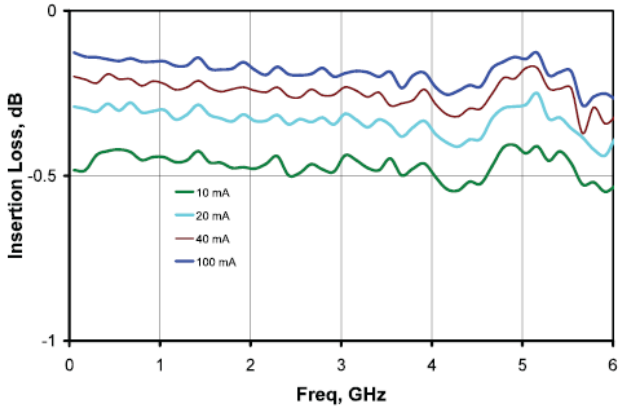
Please observe the following precautions to avoid damage:

Static Sensitivity

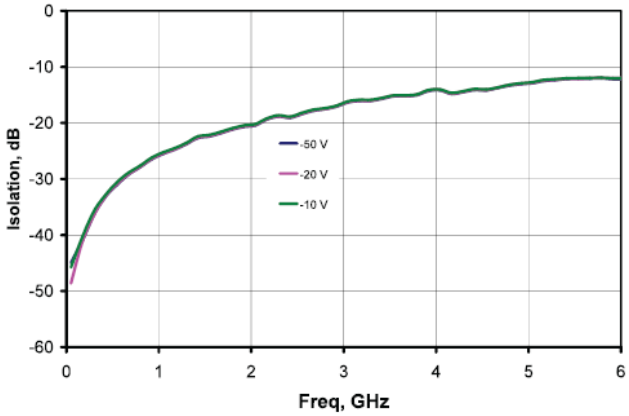
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these Class 0 (HBM) devices.

Typical Performance Curves: T_A = 25°C, Z_O = 50 Ω, Small Signal

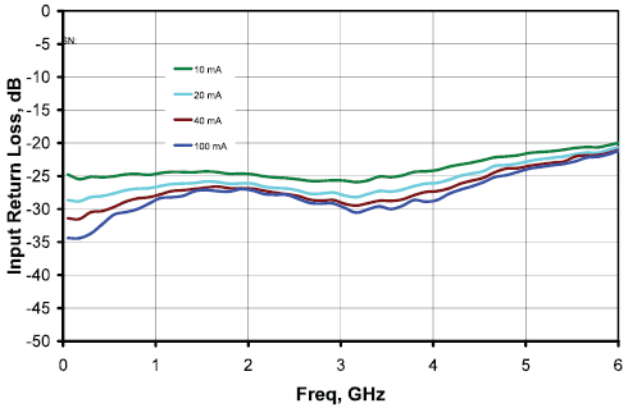
Insertion Loss



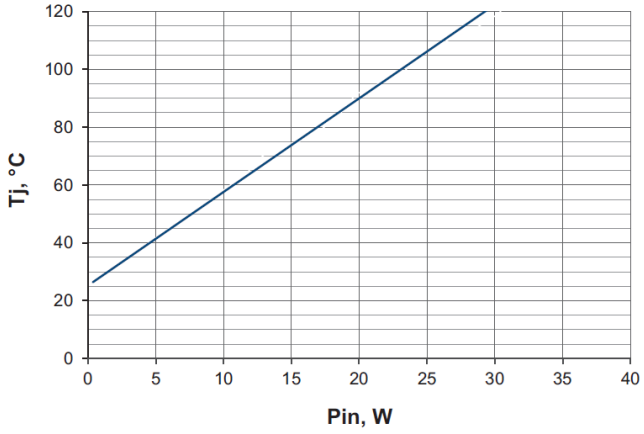
Isolation



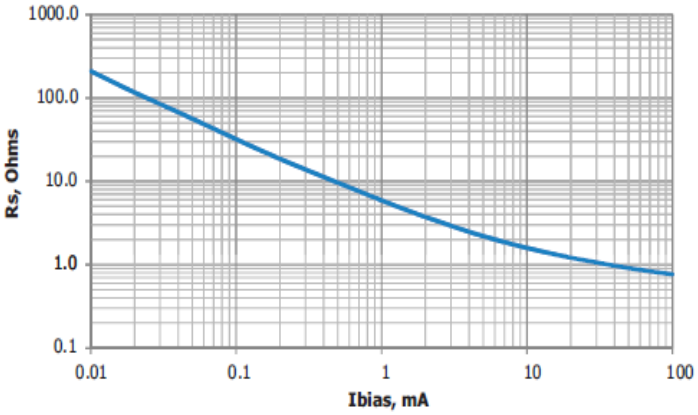
Input Return Loss



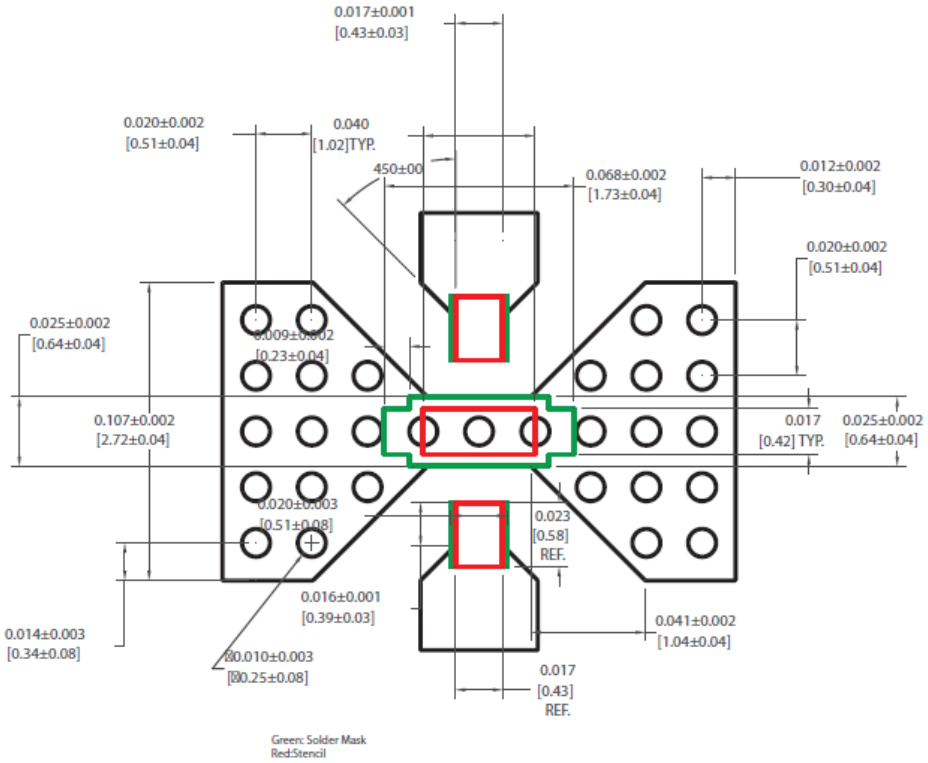
Junction Temperature vs. P_{IN}
(Mounted on Heat Sink @ +25°C, 1.3 GHz, 100 mA Bias)



Series Resistance vs. Current



Printed Circuit Board Layout (Soldering Footprint)[3,4,5,6,7]



3. Unless otherwise specified: Tolerance ±0.10 mm
4. If possible, use copper filled vias underneath pin 3 for better thermals; otherwise, use vias that are plated through, filled and plated over.
5. Solder mask should provide a 60 µm clearance between copper pad and soldermask. Rounded package pads should have matching rounded solder mask openings.
6. Use circles or squares for thermal land stencil such that there is only 50% to 80% solder paste coverage
7. 20 mils Rogers RO4350B with 1 oz. copper clad and 10 mil diameter plated thru vias on 20 mil centers underneath package.

Package Outline