

# FS5600

Automotive buck regulator and controller with voltage monitors and watchdog timer

Rev. 2 — 1 June 2021

Product data sheet



## 1 General Description

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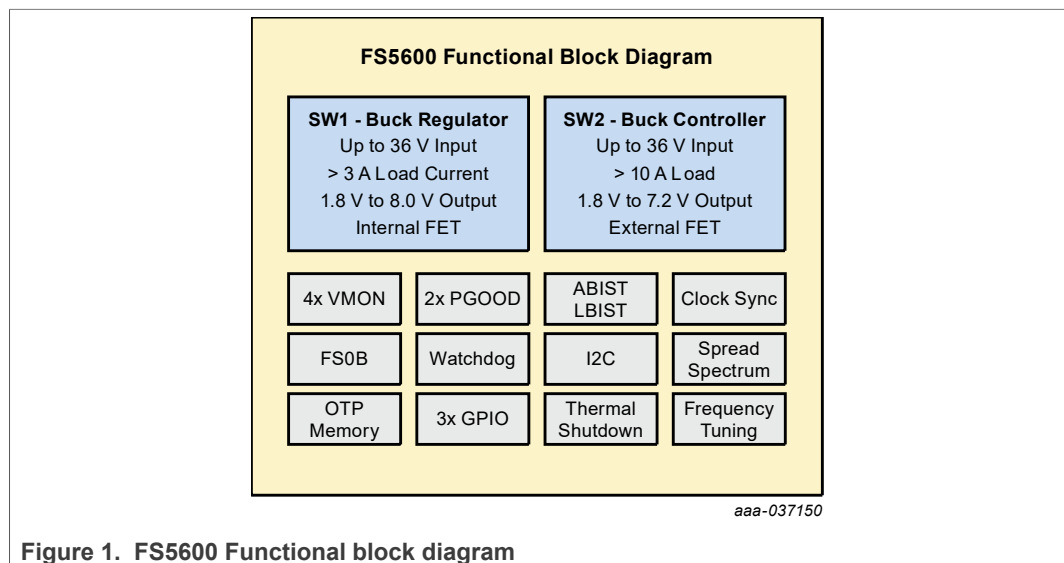
The FS5600 integrates a battery connected DC-DC controller with external FETs and a battery connected DC-DC converter with internal FETs. In addition, it offers functional safety features such as independent voltage monitors, windowed watchdog timer, I/O monitoring via ERRMON and FCCU and built-in self-test.



## 2 Features and Benefits

- 2 x High-Voltage Buck Converters:
  - Buck Controller - External FETs - 900 mA gate drive current
  - Buck Regulator - Internal FETs - 3 A+ load capability
  - $\pm 2\%$  Output Accuracy
  - 250 kHz to 3 MHz switching frequency
- High-efficiency PFM mode
- Safety Features:
  - Available in Enhanced ASIL B, ASIL B, and QM variations
  - 2 internal and up to 4 high-accuracy external voltage monitors
  - Windowed Watchdog Timer
  - ERRMON and FCCU monitoring
  - 2 x PGOOD and 1 x FS0B outputs
  - ABIST and LBIST for latest failure check
- GPIOs for seamless operation with PF PMICs
- Rated from  $-40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$   $T_J$
- 32-Ld 5 mm x 5 mm QFN
- AEC-Q100 Grade-1 Qualified

### 2.1 Overview



### 3 Applications

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QM to ASIL D automotive applications such as:

- Infotainment / Cluster / Driver Awareness
- Telematics
- V2X
- Radar
- Vision
- ADAS
- Sensor fusion

Additional safety mechanisms may be needed for ASIL D compliance in the system level. FS5600 is developed to meet ASIL B requirements.

## 4 Ordering Information

The FS5600 is offered in QM, ASIL B, and Enhanced ASIL B versions. The Enhanced ASIL B version features a Challenger Watchdog and Logic BIST (LBIST) which may be used to achieve ASIL D functional safety at the system level. Additional safety mechanisms may be needed at the system level for ASIL D compliance.

Table 1. Device options

Feature	QM Version	ASIL B Version	Enhanced ASIL B Version
SW1 – Integrated FET buck converter	Yes	Yes	Yes
SW2 – External FET buck controller	Yes	Yes	Yes
GPOs for system sequence control	Yes	Yes	Yes
PGOOD1 and PGOOD2 output	Yes	Yes	Yes
Windowed Watchdog Timer	No	Yes (Simple)	Yes (Challenger)
4 External Voltage Monitors (VMON)	No	Yes	Yes
ERRMON Monitoring (muxed with VMON)	No	Yes	Yes
FCCU Monitoring (muxed with VMON)	No	Yes	Yes
FS0B output	No	Yes	Yes
ABIST	No	Yes	Yes
LBIST	No	No	Yes
I <sup>2</sup> C CRC	No	Yes	Yes

Table 2. Ordering information

Part number	Target market	Safety grade	OTP ID	SW1	SW2	Package drawing
MFS5600AMMA0ES	Automotive	QM	A0 – Non-programmed	—	—	SOT617-24(SC)
MFS5600AMBA0ES	Automotive	ASIL B	A0 – Non-programmed	—	—	SOT617-24(SC)
MFS5600AMEA0ES	Automotive	Enhanced ASIL B	A0 – Non-programmed	—	—	SOT617-24(SC)
MFS5600AVMA0EP	Industrial	QM	A0 – Non-programmed	—	—	SOT617-24
MFS5600AMMA7ES	Automotive	QM	<a href="https://www.nxp.com/MFS5600A7ES-OTP-Report">https://www.nxp.com/MFS5600A7ES-OTP-Report</a>	5.0 V 450 kHz	3.3 V 450 kHz	SOT617-24(SC)
MFS5600AMMA8ES	Automotive	QM	<a href="https://www.nxp.com/MFS5600A8ES-OTP-Report">https://www.nxp.com/MFS5600A8ES-OTP-Report</a>	3.3 V 450 kHz	5.0 V 450 kHz	SOT617-24(SC)

5 FS5600 Internal Block Diagram

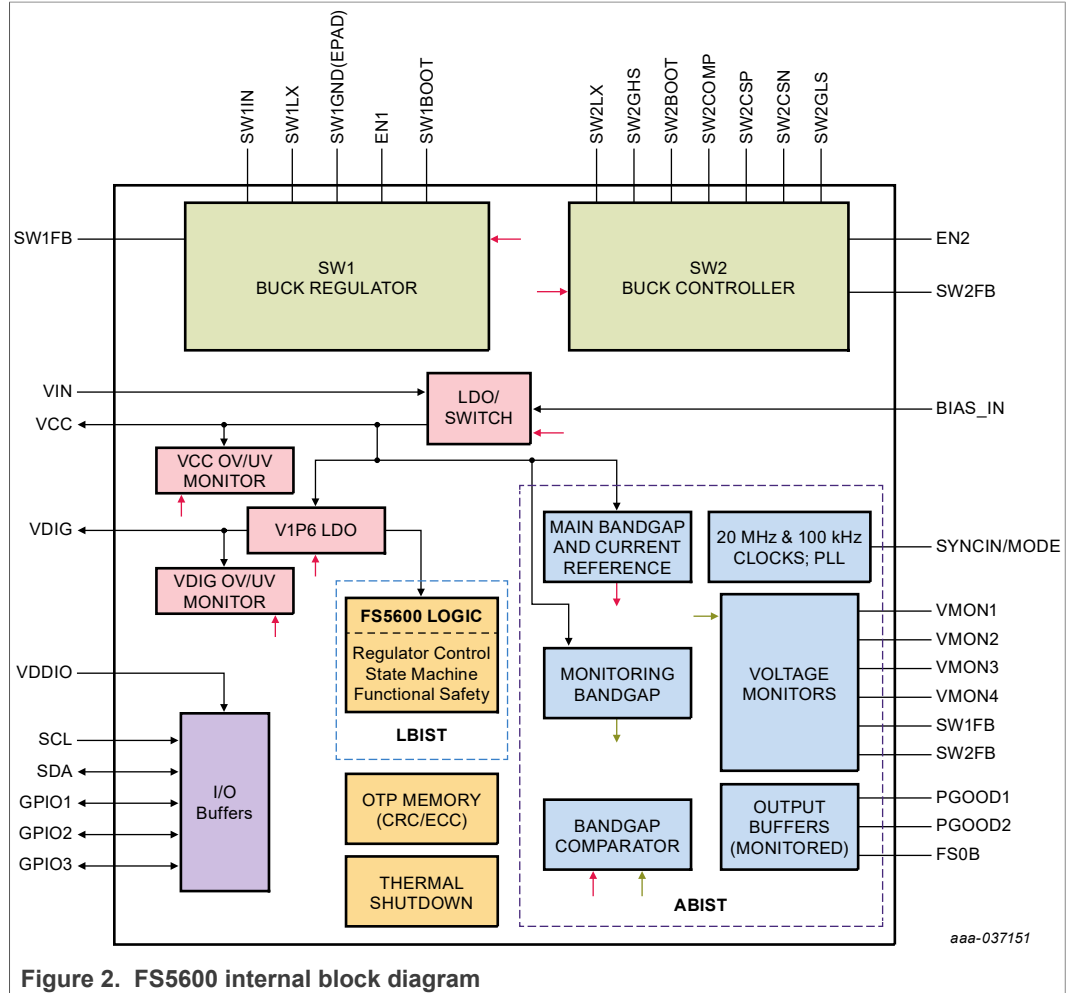
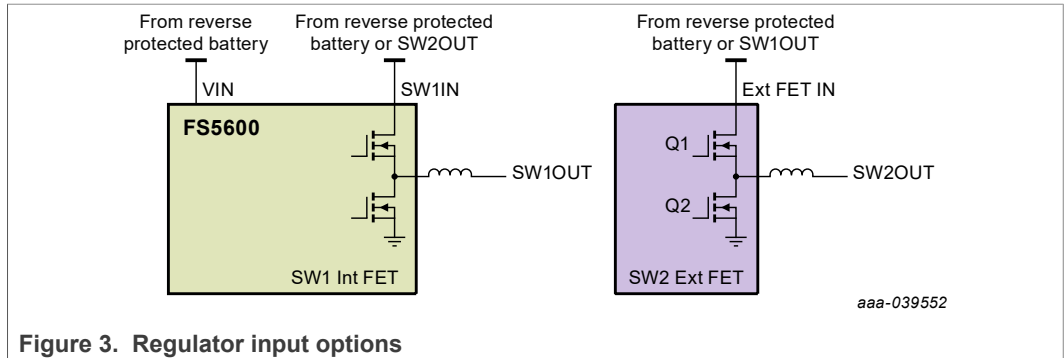


Figure 2. FS5600 internal block diagram

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## 6 Regulator Input Configurations

Input to SW1 and SW2 may be applied directly from a reverse protected automotive battery, or from the output of the other regulator as shown below. Ensure that Enable for the regulator goes high after its input is stable for proper soft-start operation.





## Automotive buck regulator and controller with voltage monitors and watchdog timer

Table 3. Pin description

Pin number	Pin name	Description	Absolute maximum voltage rating	Connection if not used
1	VDDIO	I <sup>2</sup> C I/O driver supply. Connect to 1.8 V or 3.3 V on the board. Bypass with 0.1 $\mu$ F capacitor.	-0.3 V to 5.5 V	Connect to VCC
2	SCL	I <sup>2</sup> C clock line. Pullup to VDDIO on board.	-0.3 V to 5.5 V	Connect to ground
3	SDA	I <sup>2</sup> C data line. Pullup to VDDIO on board.	-0.3 V to 5.5 V	Connect to ground
4	GPIO1/VDDOTP	General-purpose input/output pin. Used as VDDOTP during development.	-0.3 V to 10 V	Connect to ground
5	SW2COMP	SW2 compensation pin. Connect to external compensation network.	-0.3 V to 5.5 V	Connect to ground
6	SW2FB	SW2 output voltage feedback. Use external or internal resistor divider for SW2 outputs $\leq$ 5.5 V. Use external resistor divider for SW2 outputs > 5.5 V.	-0.3 V to 7.5 V	Connect to ground
7	SW2CSN	SW2 current sense feedback (-ve). Route differentially with SW2CSP to sense circuitry.	-0.3 V to 7.5 V	Connect to ground
8	SW2CSP	SW2 current sense feedback (+ve). Route differentially with SW2CSN to sense circuitry.	-0.3 V to 7.5 V	Connect to ground
9	SW2GLS	SW2 low side MOSFET gate output. Connect to gate of external low side MOSFET.	-0.3 V to 5.5 V	Leave floating
10	SW2LX	SW2 switching node. High side gate drive return path. Route parallel to SW2GHS trace on the board.	-0.3 V to 40 V	Leave floating
11	SW2GHS	SW2 high side MOSFET gate output. Connect to gate of external high side MOSFET.	-0.3 V to (SW2BOOT + 0.3 V)	Leave floating
12	SW2BOOT	SW2 bootstrap pin. Connect bootstrap capacitor between SW2BOOT and SW2LX.	-0.3 V to $V_{SW2LX} + 6$ V	Leave floating
13	VMON4/GPIO3 (GPO3 for QM version)	General-purpose input/output pin. Also selectable as voltage monitoring input via OTP. Only general-purpose output (GPO3) available in QM version.	-0.3 V to 5.5 V	Connect to ground
14	VMON3/GPIO2 (GPO2 for QM version)	General-purpose input/output pin. Also selectable as voltage monitoring input via OTP. Only general-purpose output (GPO2) available in QM version.	-0.3 V to 5.5 V	Connect to ground
15	VMON2 (NA for QM version)	Voltage Monitor 2 input. Not available in QM version. Connect to ground for QM version.	-0.3 V to 5.5 V	Connect to ground
16	VMON1 (NA for QM version)	Voltage Monitor 1 input. Not available in QM version. Connect to ground for QM version.	-0.3 V to 10 V	Connect to ground
17	SW1BOOT	SW1 bootstrap pin. Connect bootstrap capacitor between SW1BOOT and SW1LX.	-0.3 V to $V_{SW1LX} + 6$ V	Leave floating
18, 19	SW1IN	SW1 input voltage. Bypass with at least 10 $\mu$ F capacitor for both pins together.	-0.3 V to 40 V	Connect to VIN
20, 21	SW1LX	SW1 switching node. Connect to inductor.	-0.3 V to 40 V	Leave floating



## Automotive buck regulator and controller with voltage monitors and watchdog timer

Table 3. Pin description...continued

Pin number	Pin name	Description	Absolute maximum voltage rating	Connection if not used
22	EN2	SW2 enable input pin.	-0.3 V to 40 V	Connect to ground
23	EN1	SW1 enable input pin.	-0.3 V to 40 V	Connect to ground
24	FS0B (NA for QM version)	Fail-Safe Output pin. Open drain. Connect to ground for QM version.	-0.3 V to 40 V	Connect to ground
25	SW1FB	SW1 output voltage feedback. Use external or internal resistor divider for SW1 outputs $\leq 5.5$ V. Use external resistor divider for SW1 outputs $> 5.5$ V.	-0.3 V to 7 V	Connect to ground
26	PGOOD1	PGOOD1 output from monitoring of selected voltage monitors. Open-drain.	-0.3 V to 5.5 V	Connect to ground
27	PGOOD2	PGOOD2 output from monitoring of selected voltage monitors. Open-drain.	-0.3 V to 5.5 V	Connect to ground
28	VDIG	Output of internal regulator for powering logic. Bypass with 2.2 $\mu$ F capacitor. No external loading permitted.	-0.3 V to 2.0 V	N/A
29	BIAS_IN	Input pin for external bias supply. Bypass with 1 $\mu$ F capacitor. Connect to external bias supply $< 5.5$ V.	-0.3 V to 5.5 V	Connect to ground
30	VCC	VCC regulator/switch output. Bypass with 10 $\mu$ F capacitor. No external loading permitted. Nominally regulated at 4.7 V in the absence of BIAS_IN.	-0.3 V to 5.5 V	N/A
31	MODE/SYNCIN	Selectable via OTP to be used for external clock synchronization or to select between PFM and PWM modes of operation.	-0.3 V to 5.5 V	Connect to ground
32	VIN	Input to internal circuitry. Connect to battery input.	-0.3 V to 40 V	N/A
—	EPAD	Connect to ground with sufficient number of thermal vias.	—	N/A

## 8 ESD Ratings

Table 4. ESD ratings

Symbol	Rating	Min	Unit
V <sub>ESD</sub>	Human Body Model – all pins <sup>[1][2]</sup>	±2000	V
	Charge Device Model – All pins <sup>[3][2]</sup>	±500	
	GUN discharged contact test – 2 kΩ/150 pF; 2 kΩ/300 pF; 300 Ω/150 pF – Global pins <sup>[4]</sup>	±8000	

[1] ESD testing is performed in accordance with the Human Body Model (HBM) (CZAP = 100 pF, RZAP = 1500 Ω), and the Charge Device Model (CDM), Robotic (CZAP = 4.0 pF)

[2] In accordance with AEC-Q-100 Rev H

[3] ESD testing is performed in accordance with the Human Body Model (HBM) (CZAP = 100 pF, RZAP = 1500 Ω), and the Charge Device Model (CDM), Robotic (CZAP = 4.0 pF)

[4] In accordance with IEC61000-4-2 and ISO10605.2008



**Caution**

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.



**Caution**

This is an ESD sensitive device, improper handling can cause permanent damage to the part.

## 9 Thermal Characteristics

Table 5. Temperature range

Symbol	Description (Rating)	Min	Max	Unit
T <sub>A</sub>	Ambient Operating Temperature Range (Automotive)	-40	125	°C
T <sub>A</sub>	Ambient Operating Temperature Range (Industrial)	-40	105	°C
T <sub>J</sub>	Operating Junction Temperature Range	-40	150	°C
T <sub>PPRT</sub>	Peak package reflow temperature	—	260	°C
T <sub>ST</sub>	Storage Temperature Range	-55	150	°C

Table 6. QFN32 thermal resistance and package dissipation ratings

Rating	Board Type	Symbol	Value	Unit
Junction to Ambient Thermal Resistance <sup>[1]</sup>	JESD51-9, 2s2p	R <sub>θJA</sub>	36.3	°C/W
Junction-to-Top of Package Thermal Characterization Parameter <sup>[1]</sup>	JESD51-9, 2s2p	Ψ <sub>JT</sub>	4.5	°C/W
Junction to Ambient Thermal Resistance <sup>[1]</sup>	Customized, 2s4p	R <sub>θJA</sub>	31.7	°C/W
Junction-to-Top of Package Thermal Characterization Parameter <sup>[1]</sup>	Customized, 2s4p	Ψ <sub>JT</sub>	4.4	°C/W
Junction to Ambient Thermal Resistance <sup>[1]</sup>	Customized, 2s6p	R <sub>θJA</sub>	29.4	°C/W
Junction-to-Top of Package Thermal Characterization Parameter <sup>[1]</sup>	Customized, 2s6p	Ψ <sub>JT</sub>	4.4	°C/W

[1] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment. Normal practice assumes uniform heating on the die. When higher power density occurs in localized areas, there are significant hot spots on the die.

## 10 Device Level Electrical Parameters

All parameters are specified at  $T_A = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ ,  $V_{IN} = 14\text{ V}$ ,  $ENx = 12\text{ V}$ ,  $VCC = 5.0\text{ V}$ , No Load on regulators,  $F_{sw} = 450\text{ kHz}$ , typical external component values, unless otherwise noted. Typical values are specified at  $25\text{ }^{\circ}\text{C}$ , unless otherwise noted.

**Table 7. Device level electrical parameters**

Parameter	Symbol	Min	Typ	Max	Unit
VIN Rising Threshold (minimum VIN for FS5600 to turn on)	VIN_r	—	—	5.7	V
VIN and SW1/2IN recommended operating voltage (after crossing VIN_r). BIAS_IN = 5 V powers VCC	VIN	2.7	—	36	V
VIN and SW1/2IN recommended operating voltage (after crossing VIN_r). BIAS_IN = 0 V.	VIN	4.4	—	36	V
Quiescent Current (non-switching), SW1 & SW2 in PFM. BIAS_IN connected to 5 V. ULPM Mode. Current measured at VIN Current measured at BIAS_IN	Iq1	—	16 140	—	$\mu\text{A}$
Quiescent Current (non-switching), SW1 in PFM. SW2 disabled. BIAS_IN connected to 5 V. ULPM Mode. Current measured at VIN Current measured at BIAS_IN	Iq2	—	12.5 105	—	$\mu\text{A}$
Quiescent Current (non-switching), SW2 in PFM. SW1 disabled. BIAS_IN connected to 5 V. ULPM Mode. Current measured at VIN Current measured at BIAS_IN	Iq3	—	10 100	—	$\mu\text{A}$
Shutdown Mode quiescent current	Iq4	—	7.5	—	$\mu\text{A}$

## 11 SW1: 36 V Integrated FET DC-DC Converter

SW1 is a 3 A integrated FET DC DC converter. Load currents of up to 3.5 A may be drawn without entering current limit. The [Figure 6](#) shows a high-level block diagram of SW1.

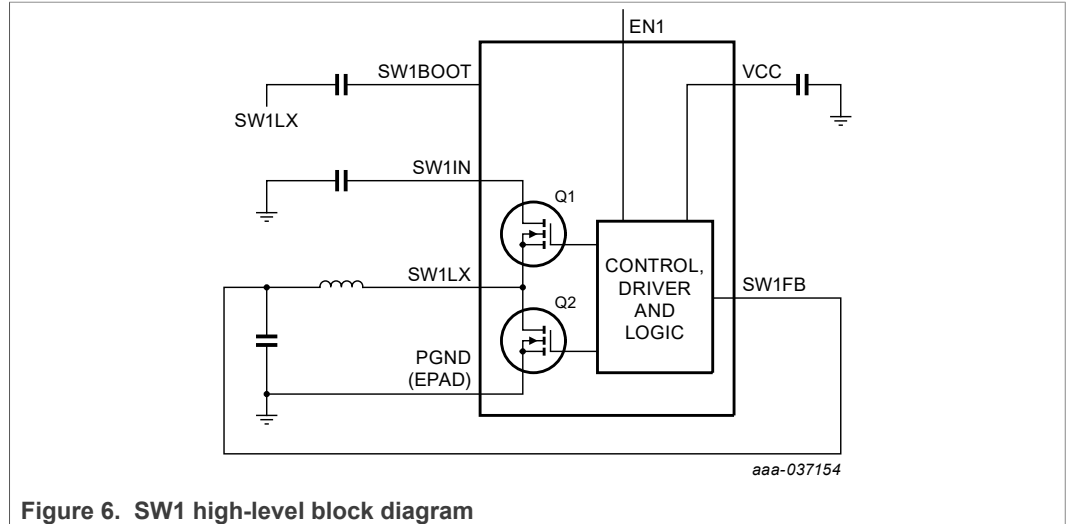


Figure 6. SW1 high-level block diagram

SW1IN pins provide input power to the MOSFETs and VCC provides the voltage needed to drive the MOSFET gates. EN1 controls the enable of the SW1 regulator.

### 11.1 SW1 electrical specifications

All parameters are specified at  $T_j = -40\text{ }^\circ\text{C}$  to  $150\text{ }^\circ\text{C}$ ,  $V_{SW1IN} = 6\text{ V}$  to  $18\text{ V}$ ,  $V_{out} = 5\text{ V}$ , typical external component values, unless otherwise noted. Typical parameters are specified at  $V_{SW1IN} = 12\text{ V}$ ,  $T_j = 25\text{ }^\circ\text{C}$  unless otherwise noted.

Table 8. SW1 electrical specifications

Parameter	Symbol	Min	Typical	Max	Units
Output Voltage Accuracy (PWM mode, SW1IN = 6 V to 18 V, 0 A ≤ ISW ≤ Rated A, minimum 2 V headroom, Vout = 1.8 V to 5.5 V using internal resistor divider)	$V_{SW1ACC}$	-2	—	2	%
Output Voltage Accuracy in Dropout: (PWM mode, SW1IN = 6 V to (Vout+2 V), 0 A ≤ ISW ≤ Rated A, 25C, Vout ≤ 5 V, 450 kHz)	$V_{SW1ACCDO}$	-3	—	3	%
Output Voltage Accuracy (Internal resistor divider, PFM mode, Load = 10 mA)	$V_{SW1ACC}$	-3	—	3	%
Reference accuracy when using external resistor divider	$V_{SW1ACC}$	0.99	1	1.01	V
Rated load current (PWM mode)	$V_{SW1LOAD}$	3	—	—	A
Soft-start time (all output voltages) (Measured from 0 % to 90 % of Vout) OTP_SW1_SS = 00 OTP_SW1_SS = 01 OTP_SW1_SS = 10 OTP_SW1_SS = 11	$t_{ss}$	—	337 675 1350 2700	500 1000 2000 4000	us

Table 8. SW1 electrical specifications...continued

Parameter	Symbol	Min	Typical	Max	Units
Operating frequency range (selectable via OTP)	SW1 <sub>FSW</sub>	250	—	3000	kHz
Peak current limit					
OTP_SW1_ILIM_SEL[1:0] = 00	SW1 <sub>ILIM</sub>	1.5	2.5	3.5	A
OTP_SW1_ILIM_SEL[1:0] = 01		3	4.1	5.2	
OTP_SW1_ILIM_SEL[1:0] = 10		3.8	4.9	6.5	
OTP_SW1_ILIM_SEL[1:0] = 11		5	6.5	8	
High side MOSFET R <sub>DS(on)</sub> (V <sub>in</sub> = 12 V, V <sub>CC</sub> = 5 V, I <sub>D</sub> = 2.5 A), including bondwires	HSR <sub>DS(ON)</sub>	—	105	—	mΩ
Low side MOSFET R <sub>DS(on)</sub> (V <sub>in</sub> = 12 V, V <sub>CC</sub> = 5 V, I <sub>D</sub> = 2.5 A), including bondwires	LSR <sub>DS(ON)</sub>	—	46	—	mΩ
EN1 pin rising threshold	EN1 <sub>RTH</sub>	1.4	—	—	V
EN1 pin falling threshold	EN1 <sub>FTH</sub>	—	—	0.95	V
SW1 monitor over voltage threshold (% of nominal)	—	5	—	15	%
SW1 monitor under voltage threshold (% of nominal)	—	-15	—	-5	%
SW1 monitoring hysteresis (measured at mid-point of resistor divider)	—	—	5	—	mV
SW1 monitoring debounce	—	—	40	—	us

## 11.2 SW1 external component selection

Table 9 provides the recommended external components for the SW1 regulator.

Table 9. SW1 external component selection

Components	Switching frequency < 1 MHz	Switching frequency > 1 MHz
Inductor	6.8 μH	1.5 μH
Output Capacitor	2 x 22 μF to 5 x 22 μF X5R/X7R	2 x 22 μF to 5 x 22 μF X5R/X7R
Bootstrap Capacitor	0.1 μF	0.1 μF
Input Capacitor	2 x 10 μF X5R/X7R	1 x 10 μF X5R/X7R

See Section 14.4 for switching frequency selection.

## 11.3 SW1 operation

SW1 is a peak current mode controlled regulator with internal current sense. It integrates low R<sub>ds(on)</sub> N-FETs for high efficiency and low solution cost.

### 11.3.1 Output voltage selection

Output voltage of SW1 may be set via OTP using the OTP\_SW1\_VOLT[7:0] bits.

OTP\_SW1\_VOLT[7] = 0b0 sets the output voltage using an internal resistor divider via OTP. Connect the SW1FB pin directly to the output voltage in this case.

OTP\_SW1\_VOLT[7] = 0b1 allows using an external resistor divider to set the output voltage. In this case, connect the SW1FB pin to the output voltage via a resistor divider. The gain of the resistor divider sets the output voltage as shown in Figure 7. Set R1 = 10 kΩ and calculate R2 such that  $V_{OUT} \times [R2 / (R1 + R2)] = 1$  V. Ensure

Automotive buck regulator and controller with voltage monitors and watchdog timer

that OTP\_SW1\_VOLT[7:0] is set to the appropriate value from [Table 10](#) as the slope compensation is calculated internally based on the output voltage.

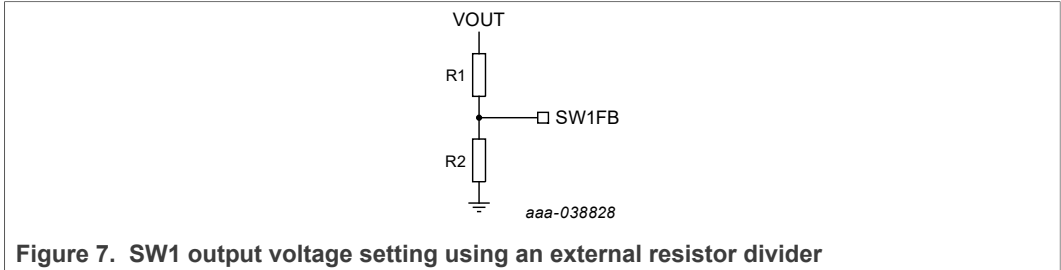


Figure 7. SW1 output voltage setting using an external resistor divider

Table 10. OTP\_SW1\_VOLT[7:0] selection

OTP_SW1_VOLT[7:0]	Vout Setting (V)
00010000	1.8
00010001	1.85
00010010	1.9
00010011	1.95
00010100	2
00010101	2.05
00010110	2.1
00010111	2.15
00011000	2.2
00011001	2.25
00011010	2.3
00011011	2.35
00011100	2.4
00011101	2.45
00011110	2.5
00011111	2.55
00100000	2.6
00100001	2.65
00100010	2.7
00100011	2.75
00100100	2.8
00100101	2.85
00100110	2.9
00100111	2.95
00101000	3
00101001	3.05
00101010	3.1
00101011	3.15

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Table 10. OTP\_SW1\_VOLT[7:0] selection...continued

OTP_SW1_VOLT[7:0]	Vout Setting (V)
00101100	3.2
00101101	3.25
00101110	3.3
00101111	3.35
00110000	3.4
00110001	3.45
00110010	3.5
00110011	3.55
00110100	3.6
00110101	3.65
00110110	3.7
00110111	3.75
00111000	3.8
00111001	3.85
00111010	3.9
00111011	3.95
00111100	4
00111101	4.05
00111110	4.1
00111111	4.15
01000000	4.2
01000001	4.25
01000010	4.3
01000011	4.35
01000100	4.4
01000101	4.45
01000110	4.5
01000111	4.55
01001000	4.6
01001001	4.65
01001010	4.7
01001011	4.75
01001100	4.8
01001101	4.85
01001110	4.9
01001111	4.95



## Automotive buck regulator and controller with voltage monitors and watchdog timer

Table 10. OTP\_SW1\_VOLT[7:0] selection...continued

OTP_SW1_VOLT[7:0]	Vout Setting (V)
01010000	5
01010001	5.05
01010010	5.1
01010011	5.15
01010100	5.2
01010101	5.25
01010110	5.3
01010111	5.35
01011000	5.4
01011001	5.45
01011010	5.5
01011011	5.55
01011100	5.6
01011101	5.65
01011110	5.7
01011111	5.75
01100000	5.8
01100001	5.85
01100010	5.9
01100011	5.95
01100100	6
01100101	6.05
01100110	6.1
01100111	6.15
01101000	6.2
01101001	6.25
01101010	6.3
01101011 to 01111111	Reserved. Do not use.
10010xxx	1.8 V - 2.15 V with external resistor divider
10011xxx	2.2 V - 2.55 V with external resistor divider
10100xxx	2.6 V - 2.95 V with external resistor divider
10101xxx	3 V - 3.35 V with external resistor divider
10110xxx	3.4 V - 3.75 V with external resistor divider
10111xxx	3.8 V - 4.15 V with external resistor divider
11000xxx	4.2 V - 4.55 V with external resistor divider
11001xxx	4.6 V - 4.95 V with external resistor divider

Automotive buck regulator and controller with voltage monitors and watchdog timer

Table 10. OTP\_SW1\_VOLT[7:0] selection...continued

OTP_SW1_VOLT[7:0]	Vout Setting (V)
11010xxx	5 V - 5.35 V with external resistor divider
11011xxx	5.4 V - .5.75 with external resistor divider
11100xxx	5.8 V - 6.15 V with external resistor divider
11101xxx	6.2 V - 6.55 V with external resistor divider
11110xxx	6.6 V - 6.95 V with external resistor divider
11111xxx	7 V - 8 V with external resistor divider

11.3.2 PFM and pulse skipping operation

At high VIN/VOUT ratio with high switching frequency, the controller may start to skip pulses to maintain regulation. The minimum on-time of high side FET is programmable via the OTP\_SW1\_MIN\_TON[1:0] bits. OTP\_SW1\_MIN\_TON[1:0] = 0b01 is the recommended default value that is optimal for most applications.

Table 11. OTP\_SW1\_MIN\_TON[1:0] selection

OTP_SW1_MIN_TON[1:0]	SW1 minimum on-time (ns)
00	40
01	60 (recommended)
10	80
11	100

In addition, the controller starts to switch at half of the selected frequency when the VIN/VOUT ratio is above 6. This allows reduced ripple operation compared to pulse-skipping.

11.3.3 PFM operation

When the OTP\_MODE\_SYNCINB bit = 0, the MODE/SYNCIN pin is configured as a SYNCIN input. In this case, switching mode of SW1 can be selected using the SW1\_MODE[1:0] bits. Default value of SW1\_MODE[1:0] is loaded from OTP\_SW1\_MODE[1:0].

Table 12. SW1\_MODE[1:0] selection.

OTP_SW1_MODE[1:0] SW1_MODE[1:0]	SW1 operating mode
00	PFM
01	Reserved. Do not use.
10	Reserved. Do not use.
11	PWM

When the OTP\_MODE\_SYNCINB bit = 1, the MODE/SYNCIN pin is configured as a MODE input that can be used to select the operating mode of SW1 between PWM (MODE = 0) and PFM (MODE = 1). Do not use the SW1\_MODE[1:0] to change the operating mode to avoid conflicts between the pin and the register bits.

## Automotive buck regulator and controller with voltage monitors and watchdog timer

On-time of the pulses in PFM mode is configurable using the OTP\_SW1\_PFM\_TON[1:0] bits. OTP\_SW1\_PFM\_TON[1:0] = 0b10 offers a good compromise between quiescent current and the output ripple for most applications.

Table 13. OTP\_SW1\_PFM\_TON[1:0] selection

OTP_SW1_PFM_TON[1:0]	SW1 PFM on-time (ns)
00	160
01	320
10	640
11	800

### 11.3.4 Soft-start

Startup of SW1 is internally controlled to eliminate overshoot and control the inrush current. Soft-start time is programmable via OTP using the OTP\_SW1\_SS[1:0] bits. See [Table 8](#) for values.

### 11.3.5 Current limit protection

Cycle-by-cycle current limit is utilized to limit the total permissible output current. Output voltage returns to regulation when the overcurrent is removed. Current limit value is programmable to four different values via OTP using the OTP\_SW1\_ILIM\_SEL[1:0] bits. See [Table 8](#) for values.

### 11.3.6 Compensation selection

OTP\_SW1\_SLOPECOMP[1:0], OTP\_SW1\_PWM\_R\_COMP[2:0], and OTP\_SW1\_GM\_COMP[1:0] select the loop parameters for SW1. See [Table 14](#) for recommended values for different operating conditions. Use interpolation for values between the ones shown in [Table 14](#).

Table 14. SW1 compensation selection

Switching frequency	Output voltage	Output capacitance	OTP_SW1_SLOPECOMP[1:0]	OTP_SW1_PWM_R_COMP[2:0]	OTP_SW1_GM_COMP[1:0]
450 kHz	3.3 V	2 x 22 $\mu$ F	10	000	10
450 kHz	3.3 V	5 x 22 $\mu$ F	10	000	10
2.2 MHz	3.3 V	2 x 22 $\mu$ F	10	000	10
2.2 MHz	3.3 V	5 x 22 $\mu$ F	10	010	10
450 kHz	4.0 V	2 x 22 $\mu$ F	10	000	10
450 kHz	4.0 V	5 x 22 $\mu$ F	10	000	10
2.2 MHz	4.0 V	2 x 22 $\mu$ F	10	000	10
2.2 MHz	4.0 V	5 x 22 $\mu$ F	10	010	10
450 kHz	5.0 V	2 x 22 $\mu$ F	10	000	10
450 kHz	5.0 V	5 x 22 $\mu$ F	10	000	10
2.2 MHz	5.0 V	2 x 22 $\mu$ F	10	010	10
2.2 MHz	5.0 V	5 x 22 $\mu$ F	10	010	10

Table 14. SW1 compensation selection...continued

Switching frequency	Output voltage	Output capacitance	OTP_SW1_SLOPECOMP[1:0]	OTP_SW1_PWM_R_COMP[2:0]	OTP_SW1_GM_COMP[1:0]
450 kHz	7.2 V	2 x 22 $\mu$ F	10	000	10
450 kHz	7.2 V	5 x 22 $\mu$ F	10	000	10
2.2 MHz	7.2 V	2 x 22 $\mu$ F	10	010	10
2.2 MHz	7.2 V	5 x 22 $\mu$ F	10	100	10

Table 15. OTP\_SW1\_SLOPECOMP[1:0] Value

OTP_SW1_SLOPECOMP[1:0]	Slope compensation (mV/ $\mu$ s)
00	45
01	67.5
10	90
11	112.5

Table 16. OTP\_SW1\_GM\_COMP[1:0] Value

OTP_SW1_GM_COMP[1:0]	Transconductance ( $\mu$ S)
00	14
01	21
10	28
11	35

Table 17. OTP\_SW1\_PWM\_R\_COMP[2:0] Value

OTP_SW1_PWM_R_COMP[2:0]	Compensation resistor (k $\Omega$ )
000	150
001	300
010	450
011	600
100	750
101	900
110	1050
111	1200

### 11.3.7 SW1 fault monitoring

SW1FB pin voltage is compared against an internal reference to detect undervoltage and overvoltage faults in SW1. See [Table 8](#) for monitoring thresholds.

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When `OTP_SW1_OV_PGOOD1 = 1`, an overvoltage fault on SW1 asserts `PGOOD1`. Similarly, when `OTP_SW1_OV_PGOOD2 = 1`, an overvoltage fault on SW1 asserts `PGOOD2`.

When `OTP_SW1_UV_PGOOD1 = 1`, an undervoltage fault on SW1 asserts `PGOOD1`. Similarly, when `OTP_SW1_UV_PGOOD2 = 1`, an undervoltage fault on SW1 asserts `PGOOD2`.

The `SW1_UV_I` and `SW1_OV_I` bits are latched to 1 respectively if undervoltage and overvoltage faults are detected. The latch bits can be cleared by writing a 1 to them.

`SW1_UV_RT` and `SW1_OV_RT` read-only bits indicate the real-time status of the faults.



Table 18. SW2 electrical characteristics...continued

Parameter	Symbol	Min	Typ	Max	Unit
Current Limiter-Inductor Peak Current Sense Voltage in CCM (Sense Resistor 10 mΩ to 20 mΩ) in the reverse direction	VSW2CSL IM	35	50	65	mV
PWM Switching Frequency Range (Programmable via OTP)	fsw	300	—	2400	kHz
Error Amplifier Transconductance (COMP = 0.9 V)	GM	1	1.5	2.3	ms
N-Channel MOSFET Gate Drivers					
High/ Low Side Driver Pull-up Resistance at Vds = 0.5 V OTP_SW2_HS_SR[3:2]/OTP_SW2_LS_SR[1:0] = 00 OTP_SW2_HS_SR[3:2]/OTP_SW2_LS_SR[1:0] = 01 OTP_SW2_HS_SR[3:2]/OTP_SW2_LS_SR[1:0] = 10 OTP_SW2_HS_SR[3:2]/OTP_SW2_LS_SR[1:0] = 11	RSW2PUP	—	11 5.6 2.8 1.6	—	Ω
High/ Low Side Driver Pull-Down Resistance at Vds = 0.5 V OTP_SW2_HS_SR[1:0]/OTP_SW2_LS_SR[1:0] = 00 OTP_SW2_HS_SR[1:0]/OTP_SW2_LS_SR[1:0] = 01 OTP_SW2_HS_SR[1:0]/OTP_SW2_LS_SR[1:0] = 10 OTP_SW2_HS_SR[1:0]/OTP_SW2_LS_SR[1:0] = 11	RSW2PDN	—	6.8 3.4 1.7 1	—	Ω
Discharge Resistance (at the output) during regulator disable	RSW2DIS	—	500	—	Ω
EN2 pin rising threshold	EN2 <sub>RTH</sub>	1.4	—	—	V
EN2 pin falling threshold	EN2 <sub>FTH</sub>	—	—	0.95	V
SW2 monitor over voltage threshold (% of nominal)	—	5	—	15	%
SW2 monitor under voltage threshold (% of nominal)	—	-15	—	-5	%
SW2 monitoring hysteresis (measured at mid-point of resistor divider)	—	—	5	—	mV
SW2 monitoring debounce	—	—	40	—	μs

## 12.2 SW2 external component selection

Table 19 provides the recommended external components for the SW2 regulator.

Table 19. SW2 recommended external components

Components	Switching frequency < 1 MHz	Switching frequency > 1 MHz
Inductor	4.7 μH	1.5 μH
Output Capacitor	3 x 22 μF to 5 x 22 μF X5R/X7R	3 x 22 μF to 5 x 22 μF X5R/X7R
Bootstrap Capacitor	0.1 μF	0.1 μF
Input Capacitor	2 x 10 μF X5R/X7R	1 x 10 μF X5R/X7R

Choose VDS > 40 V for 12 V automotive applications. At high current (> 8 A), each MOSFETs should be selected in a single package to limit the heat exchange between HS and LS. Dual MOSFETs in the same package are practical for low and mid current (< 8 A).

See Table 20 for guidance on the MOSFET selection.

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Table 20. MOSFET selection

Switching frequency	Load current	High-side MOSFET	Low-side MOSFET
450 kHz	< 5 A	Qg < 10 nC Rds(on) < 40 mΩ Example: BUK9K18-40E	Qg < 20 nC Rds(on) < 20 mΩ Example: BUK9K18-40E
	< 8 A	Qg < 10 nC Rds(on) < 25 mΩ Example: NVTFS5C471NL	Qg < 20 nC Rds(on) < 15 mΩ Example: NVTFS5C471NL
	> 8 A	Qg < 10 nC Rds(on) < 10 mΩ Example: BUK9M9R5-40H	Qg < 20 nC Rds(on) < 4 mΩ Example: BUK9M3R3-40H
2.2 MHz	< 5 A	Qg < 10 nC Rds(on) < 30 mΩ Example: BUK9M20-40H	Qg < 20 nC Rds(on) < 20 mΩ Example: BUK9M20-40H

See [Section 14.4](#) for switching frequency selection.

12.2.1 Compensation network

SW2 is compensated externally using an R-C ( $R_{comp}$ - $C_{comp}$ ) network from SW2COMP to Ground. A high frequency capacitor ( $C_{hf}$ ) placed from SW2COMP to Ground can be additionally used. Refer to the table below for recommended compensation values for typical use case conditions.

Table 21. SW2 Compensation selection

Vout(V)	Switching frequency (kHz)	Slope compensation (OTP_SW2_SLOPECOMP[5:0])	$R_{comp}$ kΩ	$C_{comp}$ nF	$C_{hf}$ pF
3.3	450	0x04	1.5	20	20
5.0	450	0x08	2.3	20	20
3.3	2200	0x0D	8.0	20	Open
5.0	2200	0x20	22	20	Open
1.8	450	0x02	0.8	100	150

Select logical level NMOS (threshold voltage < 2.5 V). Gate drive comes from VCC (5 V).

12.3 SW2 operation

SW2 is a peak current-mode controller plus driver with external current sense. The driver is built to drive low Rds(on) N-channel high and low side MOSFETs for low cost and high efficiency.

12.3.1 Output voltage selection

Output voltage of SW2 may be set via OTP using the OTP\_SW2\_VOLT[5:0] bits.

OTP\_SW2\_VOLT[5:0] = 0b111000 configures the device to use an external resistor divider to set the output voltage. Use the same equation for the external divider as for SW1.



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Table 22. OTP\_SW2\_VOLT[5:0] Selection

OTP_SW2_VOLT[5:0]	SW2 voltage setting (V)
000000	1.8
000001	1.9
000010	2
000011	2.1
000100	2.2
000101	2.3
000110	2.4
000111	2.5
001000	2.6
001001	2.7
001010	2.8
001011	2.9
001100	3
001101	3.1
001110	3.2
001111	3.3
010000	3.4
010001	3.5
010010	3.6
010011	3.7
010100	3.8
010101	3.9
010110	4
010111	4.1
011000	4.2
011001	4.3
011010	4.4
011011	4.5
011100	4.6
011101	4.7
011110	4.8
011111	4.9
100000	5
100001	5.1
100010	5.2
100011	5.3

Table 22. OTP\_SW2\_VOLT[5:0] Selection...continued

OTP_SW2_VOLT[5:0]	SW2 voltage setting (V)
100100	5.4
100101	5.5
100110	5.6
100111	5.7
101000	5.8
101001	5.9
101010	6
101011	6.1
101100	6.2
101101	6.3
101110	6.4
101111	6.5
110000	6.6
110001	6.7
110010	6.8
110011	6.9
110100	7
110101	7.1
110110	7.2
110111	Reserved. Do not use.
111000	1 (Use External Resistor Divider)
111001	Reserved. Do not use.
111010	Reserved. Do not use.
111011	Reserved. Do not use.
111100	Reserved. Do not use.
111101	Reserved. Do not use.
111110	Reserved. Do not use.
111111	Reserved. Do not use.

### 12.3.2 Pulse skipping operation

At high VIN/VOUT ratio with high switching frequency, the controller may start to skip pulses to maintain regulation. The minimum on-time of high side FET is programmable via the OTP\_SW2\_TON\_MIN[1:0] bits.

Table 23. OTP\_SW2\_TON\_MIN[1:0] Selection

OTP_SW2_TON_MIN[1:0]	SW2 minimum on-time (ns)
00	45 (recommended for 450 kHz operation)
01	65

Table 23. OTP\_SW2\_TON\_MIN[1:0] Selection...continued

OTP_SW2_TON_MIN[1:0]	SW2 minimum on-time (ns)
10	25 (recommended for 2.2 MHz operation)
11	45

### 12.3.3 PFM operation

When the OTP\_MODE\_SYNCINB bit = 0, the MODE/SYNCIN pin is configured as a SYNCIN input. In this case, switching mode of SW2 can be selected using the SW2\_MODE[1:0] bits. The default value of SW2\_MODE[1:0] is loaded from OTP\_SW2\_MODE[1:0].

Table 24. SW2\_MODE[2:0] selection

OTP_SW2_MODE[1:0] SW2_MODE[1:0]	SW2 operating mode
00	PFM
01	Reserved. Do not use.
10	Reserved. Do not use.
11	PWM

When the OTP\_MODE\_SYNCINB bit = 1, the MODE/SYNCIN pin is configured as a MODE input that can be used to select the operating mode of SW2 between PWM (MODE = 0) and PFM (MODE = 1). Do not use the SW2\_MODE[1:0] to change the operating mode to avoid conflicts between the pin and the register bits.

On-time of the pulses in PFM mode is configurable using the OTP\_SW2\_PFM\_TON[1:0] bits. OTP\_SW2\_PFM\_TON[1:0] = 0b10 offers a good compromise between quiescent current and the output ripple for most applications.

Table 25. OTP\_SW2\_PFM\_TON[1:0] Selection

OTP_SW2_PFM_TON[1:0]	SW2 PFM on-time (ns)
00	120
01	210
10	300
11	550

### 12.3.4 Soft-Start

Startup of SW2 is internally controlled to eliminate overshoot and control the inrush current. Soft-start time is programmable via OTP using the OTP\_SW2\_SS bit. See [Table 18](#) for values.

### 12.3.5 Current limit protection

Cycle-by-cycle current limit is utilized to limit the total permissible output current. Output voltage returns to regulation when the overcurrent is removed. Current limit value is programmable to 4 different values via OTP using the OTP\_SW2\_ILIM[1:0] bits. See [Table 18](#) for values.

### 12.3.6 Slope compensation

Slope compensation for the controller is set via OTP using the OTP\_SW2\_SLOPECOMP[5:0] bits. See [Section 12.2 "SW2 external component selection"](#) for values to use based on operating conditions.

Table 26. OTP\_SW2\_SLOPECOMP[5:0] selection

OTP_SW2_SLOPECOMP[5:0]	SW2 slope compensation (mV/μs)
000000	0
000001	10
000010	20
000011	31
000100	41
000101	51
000110	62
000111	72
001000	82
001001	92
001010	103
001011	113
001100	123
001101	134
001110	144
001111	154
010000	175
010001	195
010010	216
010011	237
010100	258
010101	279
010110	299
010111	320
011000	340
011001	361
011010	381
011011	402
011100	423
011101	444
011110	464
011111	485

Table 26. OTP\_SW2\_SLOPECOMP[5:0] selection...continued

OTP_SW2_SLOPECOMP[5:0]	SW2 slope compensation (mV/ $\mu$ s)
100000	504
100001	525
100010	546
100011	566
100100	587
100101	608
100110	628
100111	649
101000	669
101001	690
101010	710
101011	731
101100	752
101101	772
101110	793
101111	814
110000	834
110001	855
110010	876
110011	917
110100	938
110101	958
110110	979
110111	999
111000	1020
111001	1041
111010	1061
111011	1082
111100	1103
111101	1124
111110	1124
111111	1144

### 12.3.7 SW2 fault monitoring

SW2FB pin voltage is compared against an internal reference to detect overvoltage and undervoltage faults in SW2. See [Table 18](#) for monitoring thresholds.

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When `OTP_SW2_OV_PGOOD1 = 1`, an overvoltage fault on SW2 asserts `PGOOD1`. Similarly, when `OTP_SW2_OV_PGOOD2 = 1`, an overvoltage fault on SW2 asserts `PGOOD2`.

When `OTP_SW2_UV_PGOOD1 = 1`, an undervoltage fault on SW2 asserts `PGOOD1`. Similarly, when `OTP_SW2_UV_PGOOD2 = 1`, an undervoltage fault on SW2 asserts `PGOOD2`.

The `SW2_UV_I` and `SW2_OV_I` bits are latched to 1 respectively if undervoltage and overvoltage faults are detected. The latch bits can be cleared by writing a 1 to them.

`SW2_UV_RT` and `SW2_OV_RT` read-only bits indicate the real-time status of the faults.

## 13 BIAS\_IN Input

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An external voltage between 3.7 V and 5.5 V can be applied at the BIAS\_IN pin to reduce power consumption in the FS5600. When a valid voltage at BIAS\_IN is detected, VCC is powered directly from the BIAS\_IN path eliminating the power dissipation in the high-voltage LDO from VIN to VCC.

In the application, if either SW1 or SW2 is set to 5.0 V on the output, it is recommended to connect that output to BIAS\_IN. If an external 5 V is available in the system, that may be connected to BIAS\_IN. Ensure that the BIAS\_IN voltage does not exceed 5.5 V.

## 14 FS5600 Clock Management

The clock management provides a top-level management control scheme of internal clock and external synchronization intended to be primarily used for the switching regulators. The clock management incorporates various sub-blocks:

- Low-power 100 kHz clock
- Internal high frequency clock with programmable frequency
- Phase-Locked Loop (PLL)
- A digital clock management interface is in-charge of supporting interaction among these blocks.

Figure 9 shows a high-level block diagram of the clock management system.

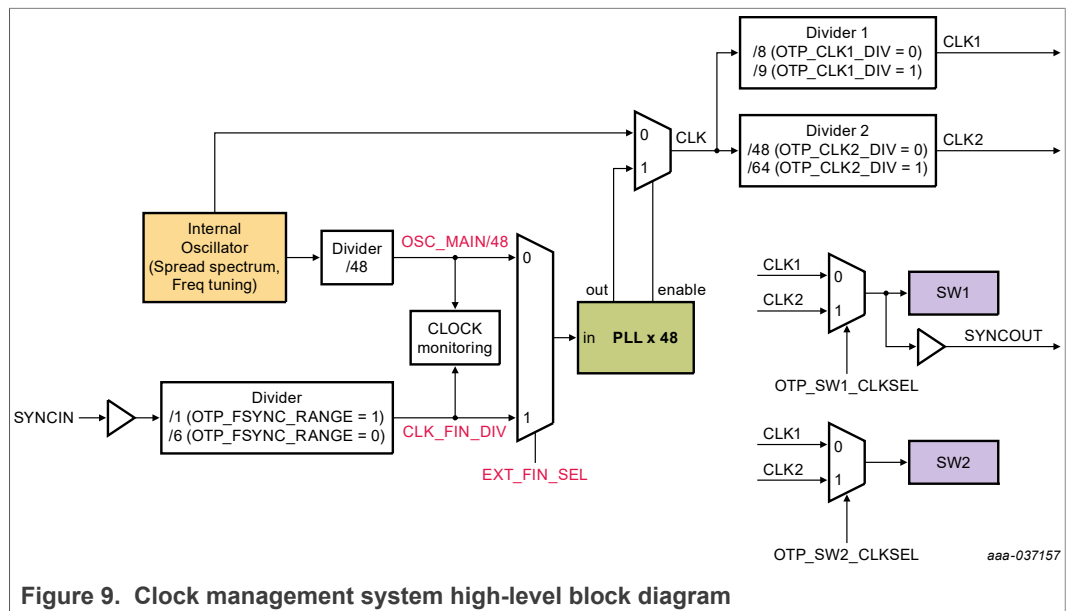


Figure 9. Clock management system high-level block diagram

### 14.1 FS5600 clock electrical characteristics

All parameters are specified at  $T_j = -40\text{ }^\circ\text{C}$  to  $150\text{ }^\circ\text{C}$ ,  $V_{IN} = 12\text{ V}$ ,  $V_{CC} = 5\text{ V}$ , unless otherwise noted. Typical parameters are specified at  $V_{IN} = 12\text{ V}$ ,  $T_j = 25\text{ }^\circ\text{C}$  unless otherwise noted.

Table 27. FS5600 clock electrical characteristics

Parameter	Symbol	Min	Typ	Max	Unit
High Frequency clock accuracy (20 MHz setting)	$F_{20\text{ MHz}}$	18.8	20	21.2	MHz
Spread Spectrum Frequency modulation frequency (FSS_FMOD = 0)	$F_{ss\_mod\_f}$	—	23.5	—	kHz
Spread Spectrum Frequency modulation frequency (FSS_FMOD = 1)	$F_{ss\_mod\_f}$	—	94	—	kHz
Spread Spectrum modulation range	$F_{ss\_mod\_range}$	—	5	—	%
SYNCIN input falling threshold	$V_{IL\_SYNCIN}$	0.35	—	—	V
SYNCIN input rising threshold	$V_{IH\_SYNCIN}$	—	—	1.25	V



Table 27. FS5600 clock electrical characteristics...continued

Parameter	Symbol	Min	Typ	Max	Unit
SYNCIN input clock frequency range (OTP_FSYNC_RANGE = 0)	F <sub>SYNCIN</sub>	2000	—	3000	kHz
SYNCIN input clock frequency range (OTP_FSYNC_RANGE = 1)	F <sub>SYNCIN</sub>	333	—	500	kHz
SYNCIN input accepted duty cycle of signal (set internal oscillator frequency closest to the resulting high frequency clock from external clock source)	F <sub>duty</sub>	40	—	60	%
SYNCOUT output logic level low	V <sub>OL_SYNCOUT</sub>	0	—	0.3 x VDDIO	V
SYNCOUT output logic level high	V <sub>OH_SYNCOUT</sub>	0.7 x VDDIO	—	VDDIO	V

### 14.2 High frequency oscillator

The FS5600 features a high frequency clock with nominal frequency of 20 MHz. The clock frequency can be adjusted using the CLK\_FREQ[3:0] bits via I<sup>2</sup>C. Initial value of CLK\_FREQ[3:0] is loaded from OTP memory from OTP\_CLK\_FREQ[3:0] bits. The high frequency oscillator is referred to as the 20 MHz clock in this document for simplicity.

Table 28. Internal oscillator frequency selection

OTP_CLK_FREQ[3:0] CLK_FREQ[3:0]	Clock frequency (MHz)
0000	20
0001	21
0010	22
0011	23
0100	24
0101	Not used
0110	Not used
0111	Not used
1000	Not used
1001	16
1010	17
1011	18
1100	19
1101	Not used
1110	Not used
1111	Not used

### 14.3 Spread spectrum

The internal oscillator provides a programmable frequency spread spectrum to help manage EMC in automotive applications. Spread spectrum is enabled by setting

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the FSS\_EN bit. Initial value of FSS\_EN is loaded from OTP\_FSS\_EN and can be subsequently changed via I<sup>2</sup>C.

**14.4 SW1 and SW2 switching frequency selection**

The switching frequency of SW1 and SW2 are derived from the 20 MHz clock. SW1 and SW2 use clock pulses that are shifted by one 20 MHz clock period (50 ns) with respect to each other to allow interleaving of the switching edges.

The 20 MHz clock is divided internally to form CLK1 and CLK2 as shown in the block diagram.

CLK1 uses a divide ratio of 8 if OTP\_CLK1\_DIV = 0 and a divide ratio of 9 if OTP\_CLK1\_DIV = 1.

CLK2 uses a divide ratio of 48 if OTP\_CLK2\_DIV = 0 and a divide ratio of 64 if OTP\_CLK2\_DIV = 1.

Using the OTP\_SW1\_CLKSEL and OTP\_SW2\_CLKSEL, switching frequency SW1 and SW2 regulators can be assigned to either CLK1 or CLK2. Refer to the table below for the available combinations.

**Table 29. SW1 and SW2 switching frequency selection**

OTP_SW1/2_CLKSEL selection	Switching frequency OTP_SW1_CLKSEL = 0; OTP_SW2_CLKSEL = 0;		Switching frequency OTP_SW1_CLKSEL = 1; OTP_SW2_CLKSEL = 1;	
	OTP_CLK1_DIV = 0	OTP_CLK1_DIV = 1	OTP_CLK2_DIV = 0	OTP_CLK2_DIV = 1
CLK1/CLK2 Selection				
SW1/SW2 Fsw at 16 MHz clock	2.0000 MHz	1.7778 MHz	0.3333 MHz	0.25 MHz
SW1/SW2 Fsw at 17 MHz clock	2.1250 MHz	1.8889 MHz	0.3542 MHz	0.265625 MHz
SW1/SW2 Fsw at 18 MHz clock	2.2500 MHz	2.0000 MHz	0.3570 MHz	0.28125 MHz
SW1/SW2 Fsw at 19 MHz clock	2.375 MHz	2.1111 MHz	0.3958 MHz	0.296875 MHz
SW1/SW2 Fsw at 20 MHz clock	2.5000 MHz	2.2222 MHz	0.4167 MHz	0.3125 MHz
SW1/SW2 Fsw at 21 MHz clock	2.6250 MHz	2.3333 MHz	0.4375 MHz	0.328125 MHz
SW1/SW2 Fsw at 22 MHz clock	2.7500 MHz	2.4444 MHz	0.4583 MHz	0.34375 MHz
SW1/SW2 Fsw at 23 MHz clock	2.8750 MHz	2.5556 MHz	0.4792 MHz	0.359375 MHz
SW1/SW2 Fsw at 24 MHz clock	3.0000 MHz	2.6667 MHz	0.500 MHz	0.375 MHz

**14.5 External clock synchronization**

The MODE/SYNCIN pin can be configured as SYNCIN via OTP by setting OTP\_MODE\_SYNCINB = 0. SYNCIN can be used to synchronize the FS5600 to an

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external clock source. The FS5600 can use either the internal high frequency oscillator or the SYNCIN pin as its source based on the validity of the external clock.

A frequency watchdog monitors the external clock at SYNCIN pin. If the external clock is not present or invalid, the device automatically switches to the internal clock. The device switches back to the external clock if the frequency watchdog detects a valid input.

When the external clock is selected, the switching regulators should be set in PWM mode at the application level to ensure clock synchronization.

## 14.6 SYNCOUT function settings

GPIO2 pin may be configured as SYNCOUT via OTP by setting `OTP_GPIO2_CFG[1:0] = 0b10`. When configured as SYNCOUT, GPIO2 outputs the clock that SW1 regulator uses (in terms of phasing and frequency) in a push-pull mode railing to VDDIO and ground.

## 15 I/O Pins in FS5600

The FS5600 has several I/O pins for system control and monitoring. These are described in [Section 15.1](#) through [Section 15.6](#). Parametric requirements for all the IO's are summarized in [Section 15.1](#).

### 15.1 I/O pins electrical specifications

All parameters are specified at  $T_A = -40\text{ }^\circ\text{C}$  to  $125\text{ }^\circ\text{C}$ ,  $V_{IN} = 12\text{ V}$ , typical external component values, unless otherwise noted. Typical values are specified at  $25\text{ }^\circ\text{C}$ , unless otherwise noted.

Table 30. I/O pin electrical specifications

Parameter	Symbol	Min	Typ	Max	Unit
EN1, EN2 Rising Threshold	ENx_r	1.40	—	—	V
EN1, EN2 Falling Threshold	ENx_f	—	—	0.95	V
EN1, EN2 Debounce	ENx_db	—	70	—	$\mu\text{s}$
SDA/SCL Rising Threshold (2.2k k $\Omega$ pullup to VDDIO)	I2C_r	—	—	0.7*VDDIO	V
SDA/SCL Falling Threshold (2.2k k $\Omega$ pullup to VDDIO)	I2C_f	0.3*VDDIO	—	—	V
PGOOD1/2_VOH (10 k $\Omega$ pullup to VDDIO)	PG_VOH	—	—	VDDIO – 0.5	V
PGOOD1/2_VOL(10 k $\Omega$ pullup to VDDIO)	PG_VOL	0.4	—	—	V
MODE Rising Threshold	MODE_r	—	—	1.25	V
MODE Falling Threshold	MODE_f	0.35	—	—	V
MODE Debounce: Rising Edge (OTP_MODE_DB = 0)	MODE_db	—	40	—	$\mu\text{s}$
MODE Debounce: Rising Edge (OTP_MODE_DB = 1)	MODE_db	—	10	—	ms
MODE Debounce Falling Edge (OTP_MODE_DB = 0/1)	MODE_db	—	70	—	$\mu\text{s}$
GPIOx_VOH (10 k $\Omega$ pullup to VDDIO)	GPIO_VOH	—	—	VDDIO - 0.5	V
GPIOx_VOL (10k $\Omega$ pullup to VDDIO)	GPIO_VOL	0.4	—	—	V
SYNCOUT_VOH (push-pull)	SYNCOUT_VOH	—	—	0.7*VDDIO	V
SYNCOUT_VOL (push-pull)	SYNCOUT_VOL	0.3*VDDIO	—	—	V

### 15.2 EN1 and EN2

EN1 and EN2 pins are used to enable SW1 and SW2 respectively. In addition to the EN1 and EN2 pins, the bits SW1\_EN and SW2\_EN ultimately determine if SW1 or SW2 are enabled. This allows enable and disable of SW1 and SW2 to be performed through their respective ENx pin, or via the respective I<sup>2</sup>C bit SWx\_EN.

SW1 regulator is disabled if (EN1 pin = LOW).

SW1 regulator is disabled if (EN1 pin = HIGH AND SW1\_EN = 0).

SW1 regulator is enabled if (EN1 pin = HIGH AND SW1\_EN = 1).

SW2 regulator is disabled if (EN2 pin = LOW).

SW2 regulator is disabled if (EN2 pin = HIGH AND SW2\_EN = 0).

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SW2 regulator is enabled if (EN2 pin = HIGH AND SW2\_EN = 1).

SW1/2\_EN are initialized to 1.

When OTP\_SW1\_PULLDN\_B = 0, a pulldown resistor of 500  $\Omega$  is engaged on the output if SW1 is disabled. Similarly, when OTP\_SW2\_PULLDN\_B = 0, a pulldown resistor of 500 ohm is engaged on the output if SW2 is disabled. The output is disabled in high-Z if OTP\_SWx\_PULLDN\_B = 1.

**15.2.1 Programming turn-off delay**

When OTP\_SW1\_OFF\_DELAY = 0, SW1 is turned off after EN1 goes low.

When OTP\_SW2\_OFF\_DELAY = 0, SW2 is turned off after EN2 goes low.

When OTP\_SW1\_OFF\_DELAY = 1, SW1 is turned off 32 ms after EN1 goes low.

When OTP\_SW2\_OFF\_DELAY = 1, SW2 is turned off 32 ms after EN2 goes low.

The 32 ms setting is useful when other devices are to be powered down in the system prior to turning off the pre-regulators.

**15.3 PGOOD1 and PGOOD2**

For the QM variation of FS5600, PGOOD1 is used to indicate the voltage regulation status of SW1 and PGOOD2 is used to indicate the voltage regulation state of SW2.

PGOOD1 is asserted low when the OV or UV monitor for SW1 indicates a faulty voltage. See [Table 8](#) for OV/UV thresholds. PGOOD2 is asserted low when the OV or UV monitor for SW2 indicates a faulty voltage. See [Table 18](#) for OV/UV thresholds.

The delay from SW1/2 reaching regulation to PGOOD1/2 being released high is programmable. See [Section 15.4](#) for details.

PGOOD1 and PGOOD2 are open-drain outputs and need an external pullup resistor.

For the ASIL B, and Enhanced ASIL B variations, behavior of PGOOD1 and PGOOD2 can be programmed to indicate status of other safety functions. See [Section 17.6](#) for details.

**15.4 GPIO1/2/3**

Pins 4, 14 and 13 are available as GPO1, GPO2, and GPO3 respectively in the QM variation. They can be sequenced as part of the device power up to control external devices. The pins can be configured to perform other functions in the ASIL B, and Enhanced ASIL B versions.

OTP\_GPO1/2/3\_DELAY[2:0] sets delay from SW1 or SW2's soft-start ramp start (which occurs first) to GPO1/2/3 being released high.

GPIO1/2/3\_OUTPUT bit is set high internally if programmed as part of the start-up based on the OTP\_GPO1/2/3\_DELAY[2:0] bits and can be changed by the user via I<sup>2</sup>C after power-up. After power-up, the GPIO1/2/3 pins may be toggled via I<sup>2</sup>C using the bits GPIO1\_OUTPUT, GPIO2\_OUTPUT and GPIO3\_OUTPUT respectively. When both EN1 and EN2 are brought low, the GPOs power down in the reverse sequence of their power-up delays.

GPO1/2/3 pins are open-drain and need an external pullup resistor. GPIO2 pin can be configured as SYNCOUT in a push-pull mode. See [Section 14.6](#) for details.

PGOOD1/2 can also be delayed during start-up as shown in [Table 31](#).

Table 31. PGOOD1/2, GPIO1/2/3 delay selection

OTP_PGOOD1_DELAY[2:0] OTP_PGOOD2_DELAY[2:0] OTP_GPO1_DELAY[2:0] OTP_GPO2_DELAY[2:0] OTP_GPO3_DELAY[2:0]	Delay duration (µs)
000	GPO1/2/3 held low through power-up. No additional delay for PGOOD1/2 release.
001	250
010	500
011	1000
100	2000
101	4000
110	8000
111	16000

### 15.5 MODE pin

The MODE/SYNCIN pin can be configured as a MODE input via OTP by setting OTP\_MODE\_SYNCINB = 1. Switching mode of SW1 and SW2 regulators can be changed by toggling with MODE pin.

When MODE = 0, SW1 and SW2 operate in continuous PWM mode.

When MODE = 1, SW1 and SW2 operate in PFM mode. In this condition, several internal circuits are turned off to achieve low quiescent current operation. PGOOD1 and PGOOD2 outputs indicate regulation status of SW1 and SW2 respectively in this condition.

Note: OTP\_ULPM\_EN = 1 for all QM devices to achieve the low quiescent current. OTP\_ULPM\_EN may be set to 0 or 1 for ASIL B, and Enhanced ASIL B variations to achieve different behavior. See [Section 17.13.9](#) for details.

### 15.6 I<sup>2</sup>C communication

Communication with the FS5600 is done through I<sup>2</sup>C and it supports high-speed operation mode with up to 3.4 MHz operation. SDA and SCL are pulled up to VDDIO typically with 2.2 kΩ resistors for 400 kHz operation, and 500 Ω for 3.4 MHz operation.

Refer to [UM10204, I<sup>2</sup>C-bus specification and user manual](#) for detailed information on the digital I<sup>2</sup>C communication protocol implementation. The FS5600 is designed to operate as a slave device during I<sup>2</sup>C communication. The default I<sup>2</sup>C device address is set by the OTP\_I2C\_ADD[2:0].

Table 32. I<sup>2</sup>C address selection

OTP_I2C_ADD[2:0]	Device address
000	0x18
001	0x19

Table 32. I<sup>2</sup>C address selection...continued

OTP_I2C_ADD[2:0]	Device address
010	0x1A
011	0x1B
100	0x1C
101	0x1D
110	0x1E
111	0x1F

## 16 Thermal Protection

A thermal sensor placed at the center of the die monitors the temperature of the die and triggers a shutdown if the die temperature exceeds 165 °C. When thermal shut-down is entered, the TSD\_I latch bit is set to notify the processor during subsequent power-up.

SW1 and SW2 regulators will immediately power down and GPIOs asserted low immediately upon entering the thermal shutdown state (no power down sequence).

All parameters are specified at TA = -40 °C to 125 °C, VIN = 12 V, VCC = 5.0 V, No Load on regulators, Fsw = 2 MHz, typical external component values, unless otherwise noted. Typical values are specified at 25 °C, unless otherwise noted.

**Table 33. Thermal protection characteristics**

Parameter	Symbol	Min	Typ	Max	Unit
Thermal shutdown temperature	TSD	155	165	175	°C
Thermal shutdown hysteresis	TSD_HYST	—	10	—	°C
Thermal shutdown debounce	TSD_DB	—	100	—	µs



## 17 Functional safety features in FS5600

The FS5600 is offered in QM, ASIL B, and Enhanced ASIL B variations. This section describes the features of the ASIL B, and Enhanced ASIL B variations. The content in this document prior to this section applies to all device variations.

The FS5600 offers comprehensive monitoring and self-test capabilities to achieve high diagnostic coverage at the system level. The functional safety features of FS5600 include:

- 4 high precision voltage monitors (in addition to monitoring of SW1 and SW2 internally)
- Challenger windowed watchdog timer
- FCCU monitoring
- 2x ERRMON monitoring for external signal monitoring
- Fail-Safe Output (FS0B) with programmable fault reaction
- PGOOD1 and PGOOD2 outputs with programmable fault reaction
- Stuck-at-fault detection on PGOOD1, PGOOD2, and FS0B outputs
- State machine with programmable fault reactions
- Redundant band gap with band gap comparator for self-test
- Internal oscillator self-test
- Built-in self-test (ABIST and LBIST) of analog and digital monitoring functions for latent failure diagnostics
- On-Demand ABIST
- CRC on OTP bits in the device
- I<sup>2</sup>C with CRC
- NOT register functionality to prevent accidental writes to critical registers
- Monitoring of internal voltages such as VCC and VDIG for over and under voltage faults

### 17.1 GPIO1/2/3 feature selection

The GPIO1/2/3 are multipurpose pins. Specific feature selection on these pins should be selected via OTP using the OTP\_GPIO1\_CFG[1:0], OTP\_GPIO2\_CFG[1:0] and OTP\_GPIO3\_CFG[1:0] bits as shown below in [Table 34](#), [Table 35](#), and [Table 36](#).

**Table 34. GPIO1 function selection**

OTP_GPIO1_CFG[1:0]	GPIO1 configuration
00	Output is high Z
01	GPO (output)
10	ERRMON1 (input)
11	Reserved (do not use)

**Table 35. GPIO2 function selection**

OTP_GPIO2_CFG[1:0]	GPIO2 configuration
00	GPO (output)
01	FCCU1 (input)
10	SYNCOU (output)

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Table 35. GPIO2 function selection...continued

OTP_GPIO2_CFG[1:0]	GPIO2 configuration
11	VMON3

Table 36. GPIO3 function selection

OTP_GPIO3_CFG[1:0]	GPIO3 configuration
00	GPO (output)
01	FCCU2 (input)
10	ERRMON2 (input)
11	VMON4

## 17.2 OV/UV monitors

VMON1, VMON2, VMON3, and VMON4 pins are monitored for under and over voltage faults and can be used to monitor critical voltages in the system. Status of the VMON1-4 monitored voltages can be routed to PGOOD1 and/or PGOOD2 as well as can be polled by I<sup>2</sup>C. See [Section 17.6](#) for details on selecting desired PGOOD1/2 reactions.

OTP\_VMONx\_UVTH[3:0] bits control the under voltage threshold and OTP\_VMONx\_OVTH[3:0] set the over voltage threshold for VMON1, VMON2, VMON3, and VMON4.

Debounce timing on the under and over voltage thresholds is also programmable between 5 μs and 125 μs using the OTP\_VMONx\_UV\_DB[1:0] and OTP\_VMONx\_UV\_DB[1:0] bits.

An external resistor divider must be used to set the mid-point of the resistor divider to 0.6 V nominally.

The OV and UV thresholds shown below are with respect to 0.6 V.

The VMONx\_OV\_I and VMONx\_UV\_I bits are set upon detection of an over or under voltage on VMONx and can be cleared in by writing a logic 1 to them. The VMONx\_OV\_RT and VMONx\_UV\_RT indicate real-time status of the faults.

### 17.2.1 VMON1-4 electrical specifications

All parameters are specified at T<sub>A</sub> = -40 °C to 125 °C, V<sub>IN</sub> = 12 V, ENx = 12 V, VCC = 5.0 V, no load on regulators, Fsw = 2.2 MHz, typical external component values, unless otherwise noted. Typical values are specified at 25 °C, unless otherwise noted.

Table 37. VMON1-4 electrical specifications

Parameter	Symbol	Min	Typ	Max	Unit
Nominal voltage at VMON1/2/3/4 (no fault)	VMONx_NOM		0.6		V
OTP_VMONx_UVTH[3:0]: Set point Accuracy OTP_VMONx_UVTH[3:0] = 0000	VMONx_UVTH	95.5	97	98.5	%
OTP_VMONx_UVTH[3:0]: Set point Accuracy OTP_VMONx_UVTH[3:0] = 0001	VMONx_UVTH	95	96.5	98	%
OTP_VMONx_UVTH[3:0]: Set point Accuracy OTP_VMONx_UVTH[3:0] = 0010	VMONx_UVTH	94.5	96	97.5	%

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Table 37. VMON1-4 electrical specifications...continued

Parameter	Symbol	Min	Typ	Max	Unit
OTP_VMONx_UVTH[3:0]: Set point Accuracy OTP_VMONx_UVTH[3:0] = 0011	VMONx_UVTH	94	95.5	97	%
OTP_VMONx_UVTH[3:0]: Set point Accuracy OTP_VMONx_UVTH[3:0] = 0100	VMONx_UVTH	93.5	95	96.5	%
OTP_VMONx_UVTH[3:0]: Set point Accuracy OTP_VMONx_UVTH[3:0] = 0101	VMONx_UVTH	93	94.5	96	%
OTP_VMONx_UVTH[3:0]: Set point Accuracy OTP_VMONx_UVTH[3:0] = 0110	VMONx_UVTH	92.5	94	95.5	%
OTP_VMONx_UVTH[3:0]: Set point Accuracy OTP_VMONx_UVTH[3:0] = 0111	VMONx_UVTH	92	93.5	95	%
OTP_VMONx_UVTH[3:0]: Set point Accuracy OTP_VMONx_UVTH[3:0] = 1000	VMONx_UVTH	91.5	93	94.5	%
OTP_VMONx_UVTH[3:0]: Set point Accuracy OTP_VMONx_UVTH[3:0] = 1001	VMONx_UVTH	91	92.5	94	%
OTP_VMONx_UVTH[3:0]: Set point Accuracy OTP_VMONx_UVTH[3:0] = 1010	VMONx_UVTH	90.5	92	93.5	%
OTP_VMONx_UVTH[3:0]: Set point Accuracy OTP_VMONx_UVTH[3:0] = 1011	VMONx_UVTH	90	91.5	93	%
OTP_VMONx_UVTH[3:0]: Set point Accuracy OTP_VMONx_UVTH[3:0] = 1100	VMONx_UVTH	89.5	91	92.5	%
OTP_VMONx_UVTH[3:0]: Set point Accuracy OTP_VMONx_UVTH[3:0] = 1101	VMONx_UVTH	89	90.5	92	%
OTP_VMONx_UVTH[3:0]: Set point Accuracy OTP_VMONx_UVTH[3:0] = 1110	VMONx_UVTH	88.5	90	91.5	%
OTP_VMONx_UVTH[3:0]: Set point Accuracy OTP_VMONx_UVTH[3:0] = 1111	VMONx_UVTH	88	89.5	91	%
OTP_VMONx_OVTH[3:0]: Set point Accuracy OTP_VMONx_OVTH[3:0] = 0000	VMONx_OVTH	101.5	103	104.5	%
OTP_VMONx_OVTH[3:0]: Set point Accuracy OTP_VMONx_OVTH[3:0] = 0001	VMONx_OVTH	102	103.5	105	%
OTP_VMONx_OVTH[3:0]: Set point Accuracy OTP_VMONx_OVTH[3:0] = 0010	VMONx_OVTH	102.5	104	105.5	%
OTP_VMONx_OVTH[3:0]: Set point Accuracy OTP_VMONx_OVTH[3:0] = 0011	VMONx_OVTH	103	104.5	106	%
OTP_VMONx_OVTH[3:0]: Set point Accuracy OTP_VMONx_OVTH[3:0] = 0100	VMONx_OVTH	103.5	105	106.5	%
OTP_VMONx_OVTH[3:0]: Set point Accuracy OTP_VMONx_OVTH[3:0] = 0101	VMONx_OVTH	104	105.5	107	%
OTP_VMONx_OVTH[3:0]: Set point Accuracy OTP_VMONx_OVTH[3:0] = 0110	VMONx_OVTH	104.5	106	107.5	%
OTP_VMONx_OVTH[3:0]: Set point Accuracy OTP_VMONx_OVTH[3:0] = 0111	VMONx_OVTH	105	106.5	108	%
OTP_VMONx_OVTH[3:0]: Set point Accuracy OTP_VMONx_OVTH[3:0] = 1000	VMONx_OVTH	105.5	107	108.5	%

Table 37. VMON1-4 electrical specifications...continued

Parameter	Symbol	Min	Typ	Max	Unit
OTP_VMONx_OVTH[3:0]: Set point Accuracy OTP_VMONx_OVTH[3:0] = 1001	VMONx_OVTH	106	107.5	109	%
OTP_VMONx_OVTH[3:0]: Set point Accuracy OTP_VMONx_OVTH[3:0] = 1010	VMONx_OVTH	106.5	108	109.5	%
OTP_VMONx_OVTH[3:0]: Set point Accuracy OTP_VMONx_OVTH[3:0] = 1011	VMONx_OVTH	107	108.5	110	%
OTP_VMONx_OVTH[3:0]: Set point Accuracy OTP_VMONx_OVTH[3:0] = 1100	VMONx_OVTH	107.5	109	110.5	%
OTP_VMONx_OVTH[3:0]: Set point Accuracy OTP_VMONx_OVTH[3:0] = 1101	VMONx_OVTH	108	109.5	111	%
OTP_VMONx_OVTH[3:0]: Set point Accuracy OTP_VMONx_OVTH[3:0] = 1110	VMONx_OVTH	108.5	110	111.5	%
OTP_VMONx_OVTH[3:0]: Set point Accuracy OTP_VMONx_OVTH[3:0] = 1111	VMONx_OVTH	109	110.5	112	%
UV Debounce OTP_VMONx_UV_DB[1:0] = 00	VMONx_UVDB	4	5	6	us
UV Debounce OTP_VMONx_UV_DB[1:0] = 01	VMONx_UVDB	12	15	18	us
UV Debounce OTP_VMONx_UV_DB[1:0] = 10	VMONx_UVDB	24	30	36	us
UV Debounce OTP_VMONx_UV_DB[1:0] = 11	VMONx_UVDB	32	40	48	us
OV Debounce OTP_VMONx_OV_DB[1:0] = 00	VMONx_OVDB	24	30	36	us
OV Debounce OTP_VMONx_OV_DB[1:0] = 01	VMONx_OVDB	40	50	60	us
OV Debounce OTP_VMONx_OV_DB[1:0] = 10	VMONx_OVDB	64	80	96	us
OV Debounce OTP_VMONx_OV_DB[1:0] = 11	VMONx_OVDB	100	125	150	us

### 17.3 Watchdog

The FS5600 offers a windowed watchdog with Simple and Challenger schemes. The Challenger scheme is available only in the Enhanced ASIL B version. The Watchdog timer is enabled by setting OTP\_WD\_DIS = 0. The Watchdog timer is disabled if OTP\_WD\_DIS = 1.

When OTP\_WD\_SELECTION = 0, the Simple scheme is selected. When OTP\_WD\_SELECTION = 1, the Challenger scheme is selected.

In the windowed watchdog, the watchdog duration is split into OPEN and CLOSED windows. The first half of the duration (window) is CLOSED and the second half of the duration (window) is OPEN. A good watchdog refresh must occur during the OPEN window.

The following constitute a bad (erroneous) watchdog refresh:

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- Wrong watchdog answer during the OPEN window
- No watchdog refresh during the OPEN window
- Good or bad watchdog answer during the CLOSED window.

For a watchdog refresh to be considered valid (good), the refresh must occur with the right answer during the right time (OPEN window). This is represented on the figure below.

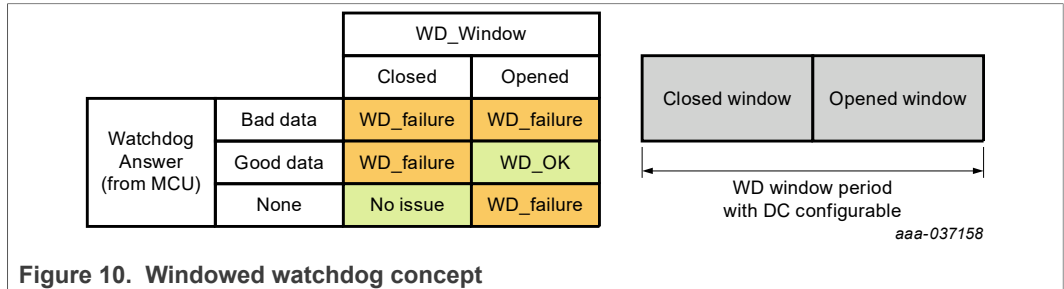


Figure 10. Windowed watchdog concept

After a good or a bad watchdog refresh, a new window period starts immediately.

When an error occurs on the Watchdog refresh with an error on the timing, the bit "BAD\_WD\_TIMING" is set for diagnostics.

When an error occurs on the Watchdog refresh with an error on the data, the bit "BAD\_WD\_DATA" is set for diagnostics.

The duration of the watchdog window is configurable from 1 ms to 1024 ms with the WD\_WINDOW [3:0] bits. The new watchdog window is effective after the next watchdog refresh. The watchdog window may be set to infinite.

The WD\_WINDOW[3:0] has a complimentary register NOT\_WD\_WINDOW[3:0] which must be written with the complimentary value for the input to take effect. This is to prevent erroneous communication from causing negative system impact.

The initial watchdog window is set to 1024 ms until the first refresh by default. This is to allow time for the MCU to boot up and refresh the watchdog for the first time. The 1024 ms initial window is available every time the Watchdog starts.

Table 38. Watchdog window period configuration

WD_WINDOW[3:0]	Watchdog window period
0000	DISABLE (during INIT_FS only)
0001	1.0 ms
0010	2.0 ms
<b>0011 (default)</b>	<b>3.0 ms</b>
0100	4.0 ms
0101	6.0 ms
0110	8.0 ms
0111	12 ms
1000	16 ms
1001	24 ms
1010	32 ms
1011	64 ms

Table 38. Watchdog window period configuration...continued

WD_WINDOW[3:0]	Watchdog window period
1100	128 ms
1101	256 ms
1110	512 ms
1111	1024 ms

The duty cycle of the watchdog window is configurable from 31.25 % to 68.75 % with the WDW\_DC [2:0] bits. The new duty cycle is effective after the next watchdog refresh.

Table 39. Watchdog window duty cycle configuration

WDW_DC [2:0]	CLOSED window	OPEN window
000	31.25 %	68.75 %
001	37.5 %	62.5 %
<b>010 (default)</b>	<b>50 %</b>	<b>50 %</b>
011	62.5 %	37.5 %
100	68.75 %	31.25 %
Others	50 %	50 %

### 17.3.1 Simple watchdog

The simple watchdog uses a seed value that must be used to ‘pet’ the watchdog. The MCU can send its own seed in WD\_SEED register or use the default seed value 0x5AB2. This seed must be written in the WD\_ANSWER register during the OPEN watchdog window.

When the result is right, the watchdog window is restarted. When the result is wrong, a watchdog error counter is incremented and the watchdog window is restarted. See [Section 17.3.3](#) for watchdog error counter.

In case the watchdog answer from MCU is wrong, the “WD\_BAD\_DATA” bit is set to 1. In case the watchdog answer (temporal domain) is wrong (timeout or refresh during closed window), the “WD\_BAD\_TIMING” bit is set to 1.

In simple watchdog configuration, it is not possible to write 0xFFFF and 0x0000 in WD\_SEED register. A communication error (I2C\_REQ\_ERR = 1) is reported in case of 0x0000 and 0xFFFF are attempted.

### 17.3.2 Challenger watchdog

The challenger watchdog is based on a question/answer process with the MCU. A 16-bits pseudo-random word is generated by implementing a Linear Feedback Shift Register (LFSR) in the FS5600. The MCU can send the seed of the LFSR or use the LFSR generated by the FS5600 and will perform a pre-defined calculation. The result should be sent through I<sup>2</sup>C during the OPEN watchdog window and is verified by the FS5600. When the result is right, the watchdog window is restarted and a new LFSR is generated. When the result is wrong, the WD error counter is incremented, the watchdog window is restarted and the LFSR value is not changed.

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In case the watchdog answer from MCU is wrong, the “WD\_BAD\_DATA” bit is set to 1. In case the watchdog answer (temporal domain) is wrong (timeout or refresh during closed window), the “WD\_BAD\_TIMING” bit is set to 1.

During the initialization phase (INIT\_RUN), the MCU can send the seed for the LFSR by writing to the WD\_SEED register, or use the default LFSR value generated by the FS5600 (0x5AB2). It is not possible to write 0x0000 in the WD\_SEED register when in the challenger mode. The I2C\_REQ\_ERR bit is set when writing a 0x0000 is attempted.

Using the seed value, the MCU should perform a simple calculation based on below formula and send the results in the WD\_ANSWER register in the OPEN window for a valid watchdog refresh.

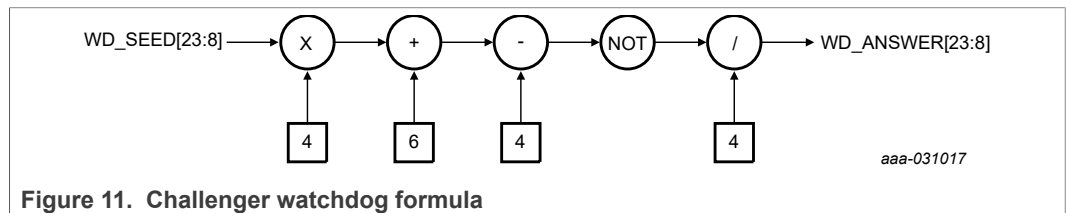


Figure 11. Challenger watchdog formula

17.3.3 Watchdog error counter and error impact

The watchdog error counter is available for the Challenger and Simple watchdog schemes. The watchdog error counter is used to count the number of bad watchdog refreshes (data and temporal errors).

Each time a watchdog failure occurs, the device increments this counter by 2. The watchdog error counter decrements by 1 each time the watchdog is correctly refreshed. This principle ensures a cyclic 'OK/NOK' behavior converges to a failure detection.

To allow flexibility in the application, the maximum value of this counter is configurable with the WD\_ERR\_LIMIT[1:0] register as shown in the table below.

Table 40. Watchdog error counter

WD_ERR_LIMIT[1:0]	Watchdog error counter value
00	8
<b>01 (reset value)</b>	<b>6</b>
10	4
11	2

The watchdog error counter value can be read by the MCU for diagnostic with the WD\_ERR\_CNT[3:0] register.

When the watchdog error counter reaches or exceeds its maximum value, the counter resets to “0” value and induces a system reaction based on WD\_FAIL\_IMPACT[1:0] configuration. Initial value of WD\_FAIL\_IMPACT[1:0] is loaded from OTP\_WD\_FAIL\_IMPACT[1:0]. Use WD\_FAIL\_IMPACT[1:0] = 01 or 10 only if OTP\_WD\_PGOOD1/2 = 1.

Table 41. WD\_FAIL\_IMPACT[1:0] description

WD_FAIL_IMPACT[1:0]	Watchdog failure reaction
00	Stay in NORMAL STATE
01	Transition to INIT_RUN state or Remain in INIT_RUN

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Table 41. WD\_FAIL\_IMPACT[1:0] description...continued

WD_FAIL_IMPACT[1:0]	Watchdog failure reaction
10	Transition to DEEP FAIL-SAFE state
11	Stay in NORMAL STATE

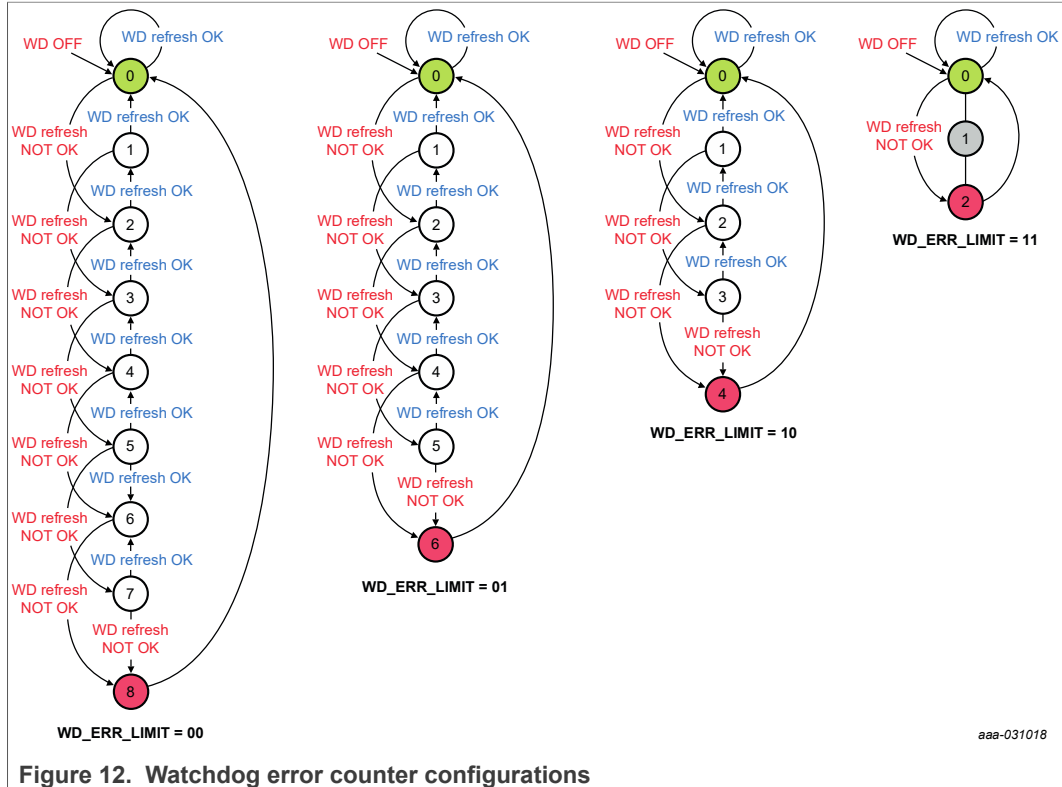


Figure 12. Watchdog error counter configurations

17.3.4 Watchdog refresh counter

The watchdog refresh strategy is available for the challenger and simple watchdog schemes. Each time the watchdog is properly refreshed, the watchdog refresh counter is incremented by '1'. Each time the watchdog refresh counter reaches its maximum value ('6' by default) and if next WD refresh is also good, the fault error counter (FLT\_ERR\_CNT) is decremented by '1'. Whatever the position the watchdog refresh counter is in, each time there is a wrong refresh watchdog, the watchdog refresh counter is reset to '0'.

To allow flexibility in the application, the maximum value of this watchdog refresh counter is configurable with the WD\_RFR\_LIMIT[1:0] register.

Table 42. Watchdog refresh counter configuration

WD_RFR_LIMIT[1:0]	Watchdog refresh counter value
00 (reset)	6
01	4
10	2
11	1



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The watchdog refresh counter value can be read by the MCU for diagnostic with the WD\_RFR\_CNT[2:0] bits.

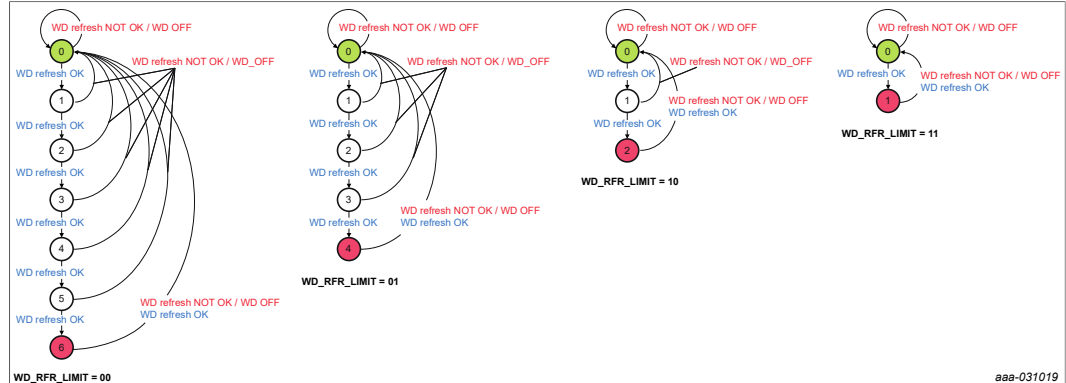


Figure 13. Watchdog refresh counter configurations

See [Section 17.11](#) on Fault Error Counter for impact of watchdog refresh on the fault error counter value.

### 17.4 FCCU monitoring

GPIO2 and GPIO3 pins can be configured as FCCU1 and FCCU2 respectively via OTP. OTP\_GPIO2\_CFG[1:0] = 0b01 configures GPIO2 as FCCU1. OTP\_GPIO3\_CFG[1:0] = 0b01 configures GPIO3 as FCCU2.

The FCCU1/2 input pins are in charge of monitoring HW failure from an NXP MCU or any other error output coming from other MCUs. FCCU can be configured by pair, or single independent inputs.

Monitoring the FCCU pins is active when the state machine is in the NORMAL STATE. See [Section 17.13](#) on state machine for reactions based on FCCU monitoring.

#### 17.4.1 BI\_STABLE protocol with FCCU1 and FCCU2

When both GPIO2 and GPIO3 are configured as FCCU1 and FCCU2 respectively and FCCU12\_BISTABLE = 1, a bi-stable protocol used in the NXP MCUs for FCCU is enabled.

Bi-stable protocol representation is shown in [Figure 14](#).

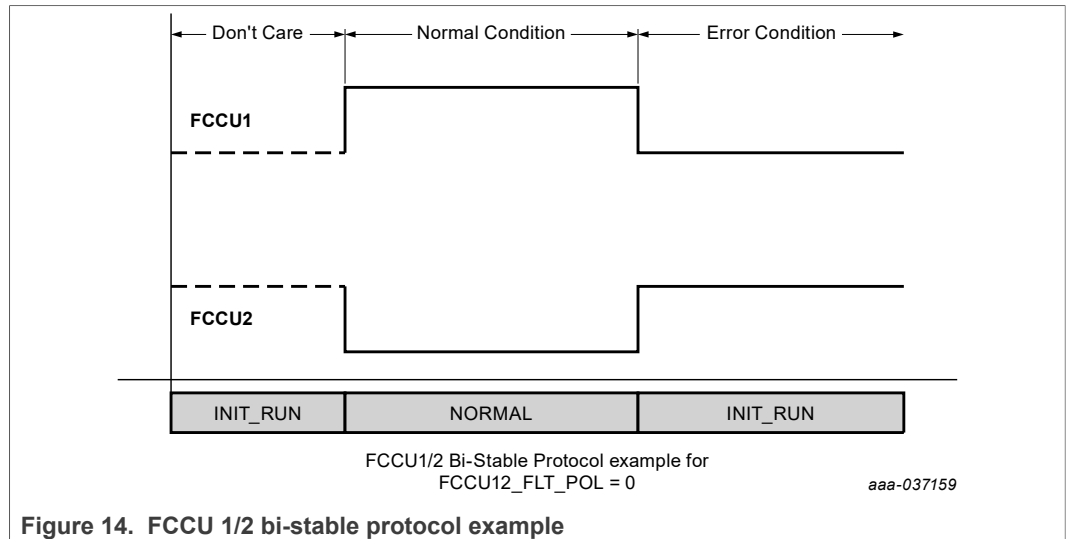


Figure 14. FCCU 1/2 bi-stable protocol example

The polarity of the fault signals is configurable using FCCU12\_FLT\_POL register:

- When FCCU12\_FLT\_POL = 0, FCCU1 = 0 or FCCU2 = 1 is a fault
- When FCCU12\_FLT\_POL = 1, FCCU1 = 1 or FCCU2 = 0 is a fault

The FS0B is asserted when an FCCU fault is detected and the state machine returns to INIT\_RUN state.

It is possible to program the PGOOD1 and PGOOD2 pins to also toggle during an FCCU fault if they are programmed to do so via OTP. PGOOD1/2 may be used to assert RESET of the MCU in this case. See [Section 17.6](#) on PGOOD for details.

### 17.4.2 Single/independent FCCU monitoring

When FCCU12\_BISTABLE = 0, FCCU1 and FCCU2 may be used for independent signal monitoring.

Either or both FCCU pins may be used in this configuration.

For FCCU1/2 the polarity of the fault signal is configurable using FCCU1/2\_FLT\_POL register:

- When FCCUx\_FLT\_POL = 0, LOW level on FCCUx is a fault
- When FCCUx\_FLT\_POL = 1, HIGH-level on FCCUx is a fault

The FS0B pin is asserted when an FCCU fault is detected and the state machine returns to INIT\_RUN state.

It is possible to program the PGOOD1 and PGOOD2 pins also to assert during an FCCU fault if they are programmed to do so. PGOOD1/2 may be used to assert RESET of the MCU in this case.

### 17.4.3 FCCU status reporting via interrupt register

FCCU12\_ERR bit is set high when an error in FCCU12 (bi-stable) is detected. FCCU1\_ERR bit is set high when an error in FCCU1 is detected. FCCU2\_ERR bit is set high when an error in FCCU2 is detected. [Table 43](#) summarizes the error scenarios for FCCU1/2.

Table 43. FCCU1/2 status reporting error scenarios

FCCU1/2FLT_POL	FCCU1 pin	FCCU2 pin	Status
0	0	0	Error
0	0	1	Error
0	1	0	No Error
0	1	1	Error
1	0	0	Error
1	0	1	No Error
1	1	0	Error
1	1	1	Error

### 17.5 External signal monitoring using ERRMON

GPIO1 and GPIO3 may be configured as ERRMON1 and ERRMON2 by setting OTP\_GPIO1\_CFG[1:0] = 0b10 and OTP\_GPIO3\_CFG[1:0] = 0b10 respectively. When used as ERRMON1/2, GPIO1/3 may be used to monitor an external signal on the application that is indicative of an error outside the FS56. For example, ERRMON1 could be connected to the PGOOD output of a PMIC and ERRMON2 could be connected to the PGOOD of a secondary PMIC.

The ERRMON1/2 input is activated on entering the INIT\_RUN state.

Once in the INIT\_RUN state, the ERRMON1/2 pin is monitored to decide whether to the transition to the NORMAL STATE.

Once in the NORMAL STATE a high or low on ERRMON1/2 (as selected by OTP), is used to assert the FS0B pin as described below.

When OTP\_ERRMON1/2\_FLT\_POL = 0, a low level on the ERRMON1/2 pin is detected as a fault.

When OTP\_ERRMON1/2\_FLT\_POL = 1, a high level on the ERRMON1/2 pin is detected as a fault.

Upon detect of a fault, the ERRMONx\_I bit is set in the FS5600. There is a programmable timer (set by OTP\_ERRMON1/2\_ACK\_TIME[1:0]) to allow the system microcontroller to acknowledge the ERRMON fault.

The acknowledge is performed by writing 0b1 to the ERRMON1/2\_I bit which in-turn clears the bit.

If the ERRMON1/2\_I bit is not cleared before the timer expires, the FS0B pin is asserted.

The below diagram shows an example of the ERRMON function.

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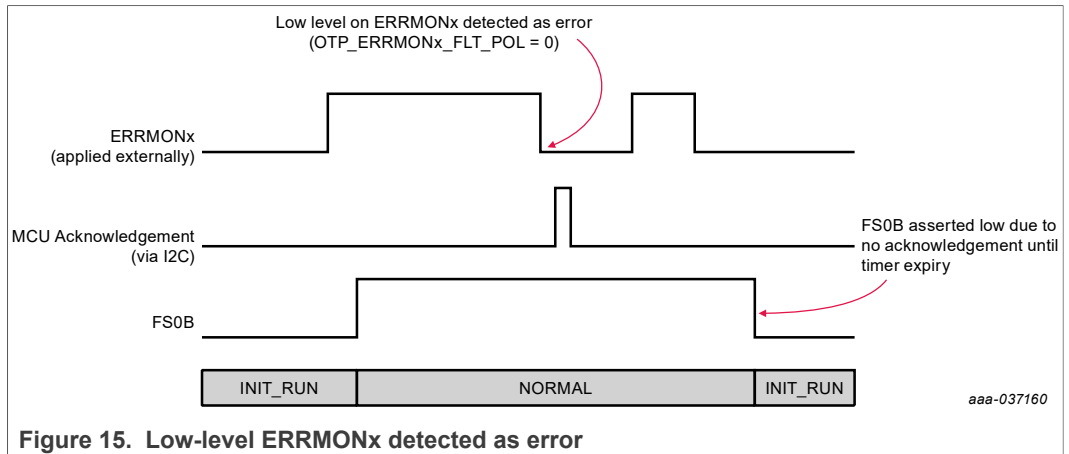


Table 44. ERRMON acknowledge timer selection

OTP_ERRMON1_ACK_TIME[1:0] OTP_ERRMON2_ACK_TIME[1:0]	Acknowledge timer
00	1 ms
01	8 ms
10	16 ms
11	32 ms

17.6 PGOOD1/2 programmable reactions for ASIL B and Enhanced ASIL B versions

While PGOOD1 and PGOOD2 are limited to providing the status of SW1 and SW2 in the QM version of FS5600, PGOOD1 and PGOOD2 reactions are fully programmable for the ASIL B and Enhanced ASIL B versions.

PGOOD1 and PGOOD2 have identical functions and options available via OTP. They may be configured differently using OTP to provide varied functions at the system level. For simplicity, PGOODx is used in place of PGOOD1 and PGOOD2.

Table 45. PGOOD1/2 programmable reactions

Function	Option
When OTP_SW1_OV_PGOODx = 1	an over-voltage event on SW1 causes PGOODx to be asserted.
When OTP_SW1_UV_PGOODx = 1	an under-voltage event on SW1 causes PGOODx to be asserted.
When OTP_SW2_OV_PGOODx = 1	an over-voltage event on SW2 causes PGOODx to be asserted.
When OTP_SW2_UV_PGOODx = 1	an under-voltage event on SW2 causes PGOODx to be asserted.
When OTP_VMON1_OV_PGOODx = 1	an over-voltage event on VMON1 causes PGOODx to be asserted.
When OTP_VMON1_UV_PGOODx = 1	an under-voltage event on VMON1 causes PGOODx to be asserted.

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Table 45. PGOOD1/2 programmable reactions...continued

Function	Option
When OTP_VMON2_OV_PGOODx = 1	an over-voltage event on VMON2 causes PGOODx to be asserted.
When OTP_VMON2_UV_PGOODx = 1	an under-voltage event on VMON2 causes PGOODx to be asserted.
When OTP_VMON3_OV_PGOODx = 1	an over-voltage event on VMON3 causes PGOODx to be asserted.
When OTP_VMON3_UV_PGOODx = 1	an under-voltage event on VMON3 causes PGOODx to be asserted.
When OTP_VMON4_OV_PGOODx = 1	an over-voltage event on VMON4 causes PGOODx to be asserted.
When OTP_VMON4_UV_PGOODx = 1	an under-voltage event on VMON4 causes PGOODx to be asserted.
When OTP_FCCU_ERR_PGOODx = 1	an FCCU error (FCCU1, FCCU2, or FCCU12) causes PGOODx to be pulsed low for 8 ms.

When any of the OTP bits listed above is set to 0, corresponding fault on the regulator/monitor has no impact on the PGOODx pin.

The delay for conditions to be satisfied and PGOODx being released is programmable using the OTP\_PGOODx\_DELAY[2:0] bits. See [Table 31](#) for details.

After PGOODx is de-asserted and there is an OV or UV fault, the fault is de-bounced and PGOODx is asserted.

17.6.1 Watchdog impact on PGOOD1/2

When OTP\_WD\_PGOODx = 1, a watchdog failure causes the PGOODx pin to toggle low for 10 ms. The watchdog is stopped when PGOODx is low and is reset at the end of the 10 ms.

The FLT\_ERR\_CNT is incremented by 1 for every watchdog failure.

During the initial 1024 ms window, a single watchdog error (bad refresh or no refresh for 1024ms) is considered a Watchdog failure and the assigned PGOODx pin is toggled.

After the initial 1024 ms window, a 'watchdog failure' when WD\_ERR\_CNT >= WD\_ERR\_LIMIT.

Example behavior: Suppose OTP\_WD\_PGOODx = 1; if a watchdog error occurs during the 1024 ms initial period, PGOODx pin is toggled, the FLT\_ERR\_CNT incremented, and the watchdog restarted. This allows system MCU to reset and try refreshing the watchdog again. If the MCU fails continuously, the FLT\_ERR\_CNT reaches its limit and FS5600 may transition to the deep fail-safe state (if enabled) to prevent a continuous fault loop. While in the NORMAL STATE, if a watchdog failure occurs (watchdog error count reaches limit), PGOODx is toggled, FLT\_ERR\_CNT incremented and the watchdog restarted. State machine will return to INIT\_RUN state or Deep Fail-Safe based on the watchdog fault impact settings (independent of PGOODx behavior).

17.7 FS0B pin

The FS0B pin indicates to the system status of the various safety mechanisms being handled by the FS5600. This includes indication of health of internal circuitry (via ABIST),

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a valid watchdog, valid SW1, SW2, VMON1, VMON2, VMON3, and VMON4, valid ERRMON, valid FCCU, and monitoring of PGOOD1/2.

The FS0B pin is released high in the NORMAL state. It is asserted low in all other states.

FS0B pin is internally held low when a valid VIN is present with EN1 and EN2 = Low. It is also asserted low if VIN pin has a disconnection provided SW1IN pin is connected.

FS0B is a global pin and can be pulled up to VIN if required in the system.

17.7.1 FS0B pin electrical specifications

All parameters are specified at T<sub>A</sub> = -40 °C to 125 °C, V<sub>IN</sub> = 12 V, typical external component values, unless otherwise noted. Typical values are specified at 25 °C, unless otherwise noted.

Table 46. FS0B pin electrical specifications

Parameter	Symbol	Min	Typ	Max	Unit
FS0B_VOH (10 kohm pullup to VDDIO)	FS0B_VOH	—	—	VDDIO - 0.5	V
FS0B_VOL(10 kohm pullup to VDDIO)	FS0B_VOL	0.4	—	—	V

17.8 PGOOD1, PGOOD2, FS0B stuck at fault check

PGOOD1, PGOOD2, and FS0B pins are continually monitored by digital to catch 'stuck-at' faults. The output at these pins is compared to the internal digital command in real time.

PGOOD1\_STUCK\_AT\_1 = 1 indicates that PGOOD1 pin is stuck at 1.

PGOOD1\_STUCK\_AT\_0 = 1 indicates that PGOOD1 pin is stuck at 0.

PGOOD2\_STUCK\_AT\_1 = 1 indicates that PGOOD2 pin is stuck at 1.

PGOOD2\_STUCK\_AT\_0 = 1 indicates that PGOOD2 pin is stuck at 0.

FS0B\_STUCK\_AT\_1 = 1 indicates that FS0B pin is stuck at 1.

FS0B\_STUCK\_AT\_0 = 1 indicates that FS0B pin is stuck at 0.

During ABIST, the PGOOD1, PGOOD2, and FS0B are to be checked to ensure they are at logic low. If any of them is not at logic low during ABIST, the corresponding 'STUCK\_AT\_1' bit is set.

When the FS56 releases PGOOD1, PGOOD2 or FS0B high, it monitors the pin to ensure it is at logic high. If not, the corresponding 'STUCK\_AT\_0' bit is set set.

**Note:** There is no state transition due to stuck-at-faults. The FS5600 only reports stuck at faults via the corresponding I<sup>2</sup>C bits. System software should evaluate the status of these bits to control state transitions.

17.9 I<sup>2</sup>C robustness

17.9.1 I<sup>2</sup>C CRC verification

When this feature is enabled, a selectable CRC verification is performed on each I<sup>2</sup>C transaction.

When OTP\_I2C\_CRC\_EN = 0, the CRC verification mechanism is disabled.

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When `OTP_I2C_CRC_EN = 1`, the CRC verification mechanism is enabled.

After each I<sup>2</sup>C transaction, the device calculates the corresponding CRC byte to ensure the configuration command has not been corrupted.

When a CRC fault is detected, the FS5600 ignores the erroneous configuration command and sets the `CRC_I` bit.

The `CRC_I` is cleared by writing a 1 to it.

The FS5600 implements a CRC-8-SAE, per the SAE J1850 specification.

Polynomial = 0x11D

Initial value = 0xFF

Figure 16 shows the 8-bit CRC polynomial per SAE J1850.

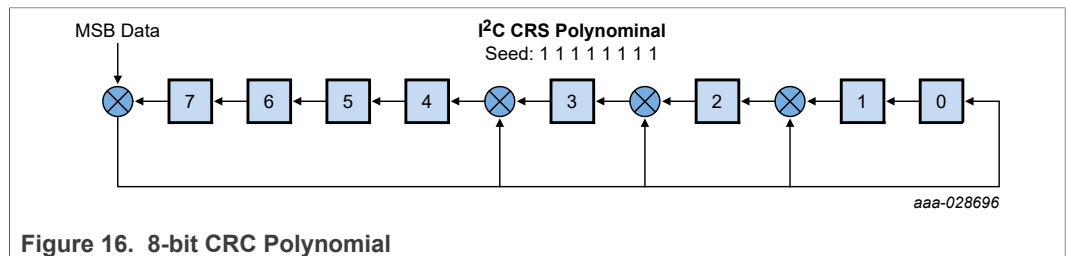


Figure 16. 8-bit CRC Polynomial

### 17.9.2 NOT logic registers

To prevent unintended writes to critical registers, a required two-step writing process must be followed.

1. Write the desired data in the REGISTER
2. Write the NOT value of [Step 1](#) to the corresponding NOT\_REGISTER

For example,

- SWx regulator will be enabled if ((SWx\_EN = 1 AND NOT\_SWx\_EN = 0) AND (ENx pin = HIGH)).
- SWx regulator will be disabled if ((SWx\_EN = 0 AND NOT\_SWx\_EN = 1) OR (ENx pin = LOW)).

A real-time XOR is performed to ensure that only complimentary register values are accepted. Refer to [Section 18](#) for list of registers where this feature is applicable.

### 17.10 I<sup>2</sup>C Write protection

To prevent unintended writes to critical registers during system NORMAL state, certain registers may be modified only in the INIT\_RUN state. These are:

Table 47. List of registers modifiable only during INIT\_RUN state

Register name	Register names (Continued)
FCCU12_BISTABLE	FCCU2_FLT_POL
FCCU1_FLT_POL	NOT_FCCU12_FLT_POL
NOT_FCCU12_BISTABLE	NOT_FCCU2_FLT_POL
NOT_FCCU1_FLT_POL	NOT_SW1_EN
SW1_EN	NOT_SW2_EN

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Table 47. List of registers modifiable only during INIT\_RUN state...continued

Register name	Register names (Continued)
SW2_EN	NOT_FLT_ERR_CNT_LIMIT[1:0]
FLT_ERR_CNT_LIMIT[1:0]	NOT_WD_ERR_LIMIT[1:0]
WD_ERR_LIMIT[1:0]	NOT_WD_RFR_LIMIT[1:0]
WD_RFR_LIMIT[1:0]	NOT_WD_FAIL_IMPACT[1:0]
WD_FAIL_IMPACT[1:0]	CLR_FLT_ERR_CNT
FCCU12_FLT_POL	NOT_CLR_FLT_ERR_CNT

The following registers are protected after the first WD\_OK in the INIT\_RUN if the watchdog is enabled. These are:

Table 48. INIT\_RUN protected registers after first WD\_OK if watchdog enabled.

Register name	Register names (Continued)
FLT_ERR_CNT_LIMIT[1:0]	NOT_FLT_ERR_CNT_LIMIT[1:0]
WD_ERR_LIMIT[1:0]	NOT_WD_ERR_LIMIT[1:0]
WD_RFR_LIMIT[1:0]	NOT_WD_RFR_LIMIT[1:0]
WD_FAIL_IMPACT[1:0]	NOT_WD_FAIL_IMPACT[1:0]
CLR_FLT_ERR_CNT	NOT_CLR_FLT_ERR_CNT

### 17.11 Fault error counter

A fault error counter is implemented to count the number of faults occurring in the application and based on system reaction. The limit value of the fault error counter is programmable using the FLT\_ERR\_CNT\_LIMIT[1:0] bits.

**Note:** “FLT\_ERR\_CNT\_LIMIT[1:0]” should be initialized in the application once during system power-up. Changing it during normal operation may reset the FLT\_ERR\_CNT value.

Table 49. FLT\_ERR\_CNT\_LIMIT[1:0] description

FLT_ERR_CNT_LIMIT[1:0]	Configure the maximum value of the Fault error counter
00	Max value = 1
01 (Reset State)	Max value = 2
10	Max value = 6
11	Max value = 12

The fault error counter value is stored in the FLT\_ERR\_CNT[3:0] bits and start at “0” after a POR. The FLT\_ERR\_CNT[3:0] may be cleared in the application via I<sup>2</sup>C by writing 0b1 to the CLR\_FLT\_ERR\_CNT bit and 0b0 to the NOT\_CLR\_FLT\_ERR\_CNT bit.

The FLT\_ERR\_CNT[3:0] decrements by '1' when the watchdog timer is refreshed after the watchdog refresh counter reaches its maximum value.

**Note:** Use the CLR\_FLT\_ERR\_CNT bit only if the watchdog is disabled. If watchdog is enabled, use that to decrement the FLT\_ERR\_CNT[3:0]. Using the CLR\_FLT\_ERR\_CNT when watchdog is enabled is not recommended.



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The fault error counter is incremented each time an assigned fault occurs.

Table 50. Fault counter source assignment

OTP bit	Fault counter configuration
OTP_SW1_FLT_CNT_EN = 1	enables SW1 OV and/or UV faults to increment FLT_ERR_CNT if the SW1 OV and/or UV faults are assigned to either of the PGOODx pins.
OTP_SW2_FLT_CNT_EN = 1	enables SW2 OV and/or UV faults to increment FLT_ERR_CNT if the SW2 OV and/or UV faults are assigned to either of the PGOODx pins.
OTP_VMON1_FLT_CNT_EN = 1	enables VMON1 OV and/or UV faults to increment FLT_ERR_CNT if the VMON1 OV and/or UV faults are assigned to either of the PGOODx pins.
OTP_VMON2_FLT_CNT_EN = 1	enables VMON2 OV and/or UV faults to increment FLT_ERR_CNT if the VMON2 OV and/or UV faults are assigned to either of the PGOODx pins.
OTP_VMON3_FLT_CNT_EN = 1	enables VMON3 OV and/or UV faults to increment FLT_ERR_CNT if the VMON3 OV and/or UV faults are assigned to either of the PGOODx pins.
OTP_VMON4_FLT_CNT_EN = 1	enables VMON4 OV and/or UV faults to increment FLT_ERR_CNT if the VMON4 OV and/or UV faults are assigned to either of the PGOODx pins.
OTP_ERRMON1_FLT_CNT_EN = 1 <sup>[1]</sup>	increments FLT_ERR_CNT if a valid fault on the ERRMON1 pin is detected.
OTP_ERRMON2_FLT_CNT_EN = 1 <sup>[1]</sup>	increments FLT_ERR_CNT if a valid fault on the ERRMON2 pin is detected.
OTP_FCCU_FLT_CNT_EN = 1	increments FLT_ERR_CNT if a valid fault on the FCCU1/FCCU2 pin is detected

[1] FLT\_ERR\_CNT increment due to an ERRMON1/2 fault occurs only in the NORMAL STATE. If a fault occurs in the ERRMON1/2 in the INIT\_RUN state, the FLT\_ERR\_CNT is not incremented.

## 17.12 Latent failure detection

### 17.12.1 Analog built-in self-test (ABIST)

Analog Built In Self-test (ABIST) may be enabled via OTP by setting the OTP\_ABIST\_EN bit. ABIST is bypassed if OTP\_ABIST\_EN = 0. If enabled, the following actions are performed.

- CRC check on mirror registers
- Checking internal oscillator's is within 15 % tolerance
- Checking main band gap and monitoring band gap are within 12 % of each other
- ABIST on SW1, SW2, VMON1, VMON2, VMON3, VMON4 voltage monitors.
- Check on PGOOD1, PGOOD2, and FS0B pins (check if PGOOD1, PGOOD2, and FS0B pins are low during ABIST)

GPIO pins when used as inputs (FCCU/ERRMON) can be checked at the system level using real-time status registers (GPIO1/2/3\_RT).

Results from ABIST are stored in registers for evaluation by the processor.

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The system microcontroller shall be responsible to evaluate the ABIST results and determine if the FS5600 can proceed to the NORMAL STATE.

Table 51. ABIST flag bits

Flag name	Description
ABIST_CRC_ERR = 1	indicates that there was an error with the CRC values in the mirror register.
ABIST_OSC_ERR = 1	indicates that the 20 MHz oscillator is not within 15 % of its nominal value.
BG_ERR = 1	indicates that the main and monitoring band gaps are not within 12 % of each other.
ABIST_VMON1_OV_ERR = 1	indicates that the VMON1's over voltage monitor is not operating in the expected range.
ABIST_VMON1_UV_ERR = 1	indicates that the VMON1's under voltage monitor is not operating in the expected range.
ABIST_VMON2_OV_ERR = 1	indicates that the VMON2's over voltage monitor is not operating in the expected range.
ABIST_VMON2_UV_ERR = 1	indicates that the VMON2's under voltage monitor is not operating in the expected range.
ABIST_VMON3_OV_ERR = 1	indicates that the VMON3's over voltage monitor is not operating in the expected range.
ABIST_VMON3_UV_ERR = 1	indicates that the VMON3's under voltage monitor is not operating in the expected range.
ABIST_VMON4_OV_ERR = 1	indicates that the VMON4's over voltage monitor is not operating in the expected range.
ABIST_VMON4_UV_ERR = 1	indicates that the VMON4's under voltage monitor is not operating in the expected range.
ABIST_SW1_OV_ERR = 1	indicates that the SW1's over voltage monitor is not operating in the expected range.
ABIST_SW1_UV_ERR = 1	indicates that the SW1's under voltage monitor is not operating in the expected range.
ABIST_SW2_OV_ERR = 1	indicates that the SW2's over voltage monitor is not operating in the expected range.
ABIST_SW2_UV_ERR = 1	indicates that the SW2's under voltage monitor is not operating in the expected range.

The above bits are all 0 if ABIST test is successful.

### 17.12.2 On-demand ABIST

When in the NORMAL STATE or INIT\_RUN state, application can request an on-demand ABIST to be performed by setting the OD\_ABIST bit. This OD\_ABIST bit is self-clearing after completing the on-demand ABIST.

FS0B is asserted low during on-demand ABIST if initiated in the INIT\_RUN state.

FS0B remains high during on-demand ABIST if initiated in the NORMAL state.

**17.12.3 Logical Built-In Self-Test (LBIST)**

The FS5600 includes a Logical Built-In Self-Test (LBIST) feature to verify functionality of logic block in the FS5600.

LBIST can be disabled by setting the OTP\_LBIST\_DIS[7:0] to 0b0011\_0110.

LBIST is enabled for all other values of OTP\_LBIST\_DIS[7:0]. If LBIST is disabled via OTP, the following conditions should be valid for LBIST to be truly disabled:

- No boot error (from OTP controller)
- No CRC error (from OTP controller)
- No ECC error (from OTP controller)

If one of these conditions are not satisfied LBIST is enabled. LBIST\_PASS bit in the I<sup>2</sup>C map is set when LBIST is completed successfully and passes.

**17.12.4 VCC and VDIG monitoring**

VCC and VDIG voltages are monitored for over and under voltage faults. The part is powered down if any of these faults is detected. See state transition table for specific transitions.

All parameters are specified at TA = -40 to 125 °C, VIN = 12 V, ENx = 12 V, VCC = 5.0 V, No Load on regulators, Fsw = 2.2 MHz, typical external component values, unless otherwise noted. Typical values are specified at 25 °C, unless otherwise noted.

Table 52. POR Thresholds

Parameter	Symbol	Min	Typ	Max	Unit
VDIG Rising POR	VDIG_POR		1.44		V
VDIG Falling POR	VDIG_POR		1.40		V
VDIG Overvoltage Threshold	VDIG_OV		1.95		V
VCC Rising POR	VCC_POR		3.2		V
VCC Falling POR	VCC_POR		2.6		V
VCC Overvoltage Threshold	VCC_OV		5.8		V

**17.13 FS5600 operation states and state machine**

Figure 17 shows the high-level operation states of the FS5600 ASIL B, and Enhanced ASIL B versions.

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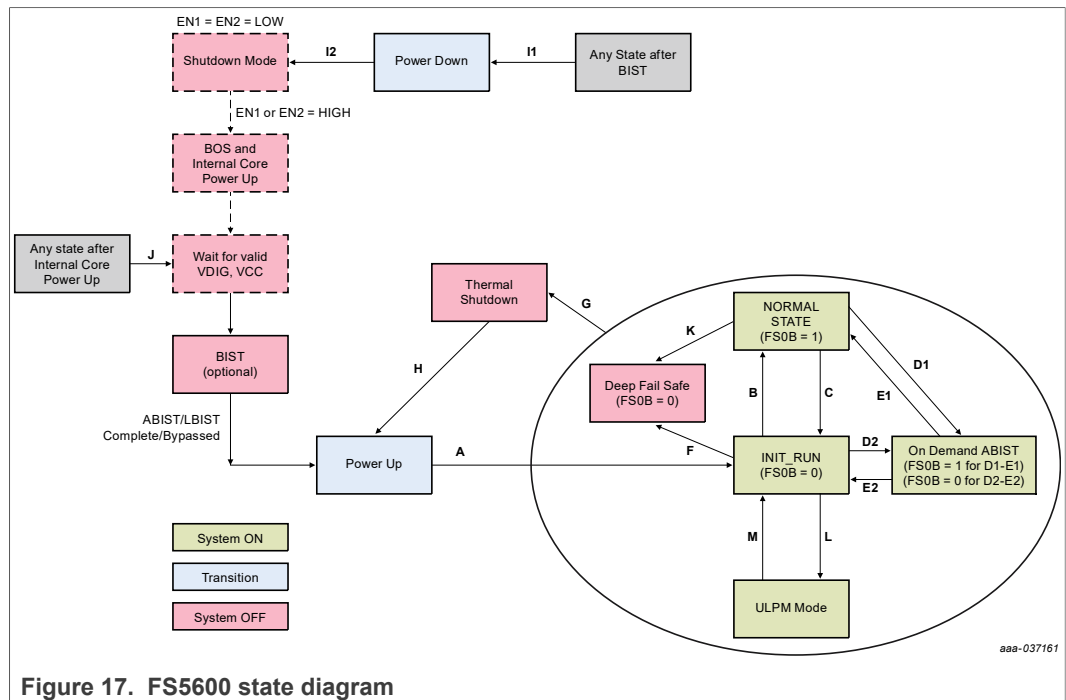


Figure 17. FS5600 state diagram

17.13.1 Shut-down mode

This is the state of the FS5600 when a valid VIN is applied, but EN1 and EN2 pins are held low.

From one of the operation modes, (INIT\_RUN/NORMAL STATE/On Demand ABIST, Deep Fail-Safe), when EN1 and EN2 = 0, the IC enters the shut-down mode through the 'Power Down' state.

When entering the shut-down mode from INIT\_RUN, NORMAL STATE or on-demand ABIST states, the FS5600 sequences the GPOs in the reverse order of the power-up at the appropriate time. See [Section 17.13.8](#) for details.

For example, if OTP\_GPO1\_DELAY is set to 1 ms, and OTP\_GPO2\_DELAY is set to 5 ms:

- When EN1 = EN2 = 0, GPO2 is asserted low immediately, 4 ms after which GPO1 is asserted low, 1 ms after which SW1 and SW2 regulators are disabled.
- FS0B is asserted low immediately after NORMAL STATE is exited.

17.13.2 Built-in self-test (BIST)

Analog Built-in self-test (ABIST) and logical built-in self-test (LBIST) are executed in this state if enabled. This state is bypassed if both are disabled.

17.13.3 Power-up

SW1, SW2, and the various GPO's in FS5600 are powered up in this state. SW1 and SW2 are enabled after exiting BIST or thermal shutdown and if their respective ENx pin is held high. The power-up state exits upon completion of the highest delay among OTP\_GPO1\_DELAY[2:0], OTP\_GPO2\_DELAY[2:0] and OTP\_GPO3\_DELAY[2:0].

---

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The OTP\_PGOOD1\_DELAY[2:0] and OTP\_PGOOD2\_DELAY[2:0] timers run in parallel to the GPO timers and do not need to expire to exit the power-up state. PGOOD1 and PGOOD2 may be released high even in the INIT\_RUN state.

#### 17.13.4 Power-up in Debug Mode

The FS5600 offers a Debug Mode of operation that is useful during system bring up and/or development. When in Debug Mode, the following restrictions are in place:

- Deep Fail-Safe transition is disabled
- Watchdog window duration is set to infinite

To power up in Debug Mode, apply VDDOTP\_GPIO1 = 8 V before EN1 or EN2 go high or before VIN is applied. In this condition, the FS5600 pauses power-up and waits for VDDOTP\_GPIO1 < 1 V before continuing to power up in Debug Mode. Ensure that there is board-level isolation on the VDDOTP\_GPIO1 bus if the GPIO1 function is used at a lower voltage level.

While VDDOTP\_GPIO1 is maintained at 8 V, the following I<sup>2</sup>C commands can be sent to open access to the OTP mirror registers:

```
SET_REG:FS5600:Functional:TM_ENTRY:0xD5A7
```

```
SET_REG:FS5600:Functional:TM_ENTRY:0xB8EE
```

```
SET_REG:FS5600:Functional:TM_ENTRY:0x0F37
```

The mirror registers modified in this fashion take effect during power-up when VDDOTP\_GPIO < 1 V. Contact your NXP representative for commands needed to access the mirror registers.

#### 17.13.5 INIT\_RUN

The INIT\_RUN state is entered after the power-up state. Either or both SW1 and SW2 may be enabled to enter the INIT\_RUN state. The state machine can remain in the INIT\_RUN state indefinitely. In this state, the state machine waits for conditions to transition to the normal state if enabled to do so. Alternatively, the state machine may proceed to power down to the Deep Fail-Safe state if conditions enabling this are met.

INIT\_RUN state may also be entered from the normal state by setting the GOTO\_INIT\_RUN and clearing the NOT\_GOTO\_INIT\_RUN bits.

#### 17.13.6 Normal state

In normal state, the FS0B pin is de-asserted to indicate to the system that essential parameters monitored by the FS5600 are in expected range. Normal state is entered from the INIT\_RUN provided conditions for this transition are met. OTP\_NORMAL\_STATE\_EN bit should be set to 1 to enable transition to the normal state.

OTP\_ERRMON1\_SAFE = 1 is an enabling condition for a valid ERRMON1 signal to control transition to the normal state. OTP\_ERRMON2\_SAFE = 1 is an enabling condition for a valid ERRMON2 signal to control transition to the normal state.

OTP\_PGOOD1\_SAFE = 1 is an enabling condition for a valid PGOOD1 output to control transition to the normal state. OTP\_PGOOD2\_SAFE = 1 is an enabling condition for a valid PGOOD2 output to control transition to the normal state.

See [Section 17.13.10](#) for conditions to transition to the normal state.

### 17.13.7 Deep fail-safe state

In the deep fail-safe state, the FS5600 is shut down. All the regulators are turned off and signal outputs are asserted low. The only way to exit deep fail-safe state is through a power cycle on the VIN input, or if both EN1 and EN2 are pulled low in the application.

Deep fail-safe can be entered when the fault error counter reaches its maximum value, or when a watchdog failure is programmed to go to deep fail-safe. OTP\_DFN\_EN must be set to 1 to enable transition to the Deep Fail-Safe state. See [Section 17.13.10](#) for detailed conditions.

### 17.13.8 Power-down

The FS56 enters a graceful power-down when both EN1 and EN2 are asserted low in the application.

The power-down follows a reverse of the power-up sequence for the GPOs (each following the OTP\_GPOx\_DELAY[2:0] setting) followed by SW1 and/or SW2.

If entering power-down from deep fail-safe, thermal shut-down, or power-up, the state machine immediately enters shut-down mode after SW1, SW2, and GPIOs are asserted low (no power-down sequence).

### 17.13.9 Low-power operation

There are several ways to reduce the quiescent current consumption of the FS5600. These are:

- Turning off SW1 and SW2 (via I<sup>2</sup>C, or using EN1/2 pins)
- Changing SW1 and SW2 operation mode from PWM to Auto Skip or PFM mode.

Operation mode of SW1 and SW2 may be changed using I<sup>2</sup>C or by using the MODE pin.

#### 17.13.9.1 Ultra low-power operation

When (MODE pin =1) AND (OTP\_MODE\_SYNCINB\_SEL[1:0] = 00) AND (OTP\_ULPM\_EN = 1), the FS5600 achieves further reduction in quiescent current by turning off the internal 20 MHz clock. In this condition, I<sup>2</sup>C access is not available, the watchdog timer function is not available and external voltage monitors (VMON1-4) are disabled. PGOOD pins assigned to the external voltage monitors (VMON1-4) are asserted low. If the respective regulator is enabled, voltage monitors for SW1 and SW2 regulators remain enabled. The OTP\_ULPM\_EN bit is set to 1 in the QM version of FS5600. User may choose its value in ASIL B and Enhanced ASIL B versions.

17.13.10 State transition table

Table 53. State transition table

Transition	Description	Transition conditions
A	Power up to INIT_RUN	Completion of SW1 soft-start (if EN1 = high) && Completion of SW2 soft-start (if EN2 = high) && Expiration of largest delay among OTP_GPOx_DELAY[2:0] (if GPIOx pin used as GPO AND OTP_GPOx_DELAY[2:0] NOT EQUAL to 0b000) <b>Note:</b> If one regulator is disabled, its soft-start completion signal is ignored as a condition for this state transition.
B	INIT_RUN to NORMAL STATE	OTP_NORMAL_STATE_EN = 1 && [ (PGOOD1 released high internally && OTP_PGOOD1_SAFE = 1) OR (OTP_PGOOD1_SAFE = 0) && (PGOOD2 released high internally && OTP_PGOOD2_SAFE = 1) OR (OTP_PGOOD2_SAFE = 0) && (OTP_GPIO1_CFG[1:0] = 0b10 && (OTP_ERRMON1_FLT_POL XOR ERRMON1_pin) && OTP_ERRMON1_SAFE = 1) OR (OTP_GPIO1_CFG[1:0] = 0b10 && OTP_ERRMON1_SAFE = 0) OR (OTP_GPIO1_CFG[1:0] != 0b10) && (OTP_GPIO3_CFG[1:0] = 0b10 && (OTP_ERRMON2_FLT_POL XOR ERRMON2_pin) && OTP_ERRMON2_SAFE = 1) OR (OTP_GPIO3_CFG[1:0] = 0b10 && OTP_ERRMON2_SAFE = 0) OR (OTP_GPIO3_CFG[1:0] != 0b10) ] && [ (OTP_MODE_SYNCINB = 1 && OTP_ULPM_EN = 1 && MODE_SYNCIN pin = Low) OR (OTP_MODE_SYNCINB = 1 && OTP_ULPM_EN = 0) OR (OTP_MODE_SYNCINB = 0) ] && [ OTP_WD_DIS = 1 OR (Valid WD (WD_ERR_CNT = 0) && WD refreshed at least once) ] && GOTO_NORMAL = 1 (set by system software)
C	NORMAL STATE to INIT_RUN	Condition 1: (PGOOD1 asserted low internally && OTP_PGOOD1_SAFE = 1)
C	NORMAL STATE to INIT_RUN	Condition 2: (PGOOD2 asserted low internally && OTP_PGOOD2_SAFE = 1)

## Automotive buck regulator and controller with voltage monitors and watchdog timer

Table 53. State transition table...continued

Transition	Description	Transition conditions
C	NORMAL STATE to INIT_RUN	Condition 3: (WD_Error_Limit_Reached (WD_ERR_CNT[1:0] >= WD_ERR_LIMIT[1:0]) && WD_FAIL_IMPACT[1:0] = 01)
C	NORMAL STATE to INIT_RUN	Condition 4: (OTP_GPIO1_CFG[1:0] = 0b10 && OTP_ERRMON1_SAFE = 1 && Fault Detected and no ACK)
C	NORMAL STATE to INIT_RUN	Condition 5: (OTP_GPIO3_CFG[1:0] = 0b10 && OTP_ERRMON2_SAFE = 1 && Fault Detected and no ACK)
C	NORMAL STATE to INIT_RUN	Condition 6: (OTP_MODE_SYNCINB = 1 && OTP_ULPM_EN = 1 && MODE_SYNCIN pin = High)
C	NORMAL STATE to INIT_RUN	Condition 7: (FCCUxx_ERR = 1)
C	NORMAL STATE to INIT_RUN	Condition 8: (GOTO_INIT_RUN = 1 set by system software)
D1	NORMAL STATE to On-Demand ABIST	OD_ABIST = 1
E1	On-Demand ABIST to NORMAL STATE	OD_ABIST = 0 (upon self-clearing after completion of On Demand ABIST)
D2	INIT_RUN to On-Demand ABIST	OD_ABIST = 1
E2	On-Demand ABIST to INIT_RUN	OD_ABIST = 0 (upon self-clearing after completion of On Demand ABIST)
F	INIT_RUN to Deep Fail-Safe	OTP_DFS_EN = 1 && FLT_ERR_CNT[3:0] reaches limit
G	NORMAL STATE/INIT_RUN/On-Demand ABIST/ Deep Fail-Safe to Thermal Shutdown	$T_j > T_{jmax\_rise}$
H	Thermal Shut-down to Power Up	$T_j < T_{jmax\_fall}$
I1	Any State after BIST to Power Down	EN1 and EN2 = 0
I2	Power Down to Shutdown Mode	Completion of Power Down
J	Any state after Internal Core Power Up up to Wait for valid VDIG, VCC	Condition 1: VCC_UV_F (VCC under-voltage)
J	Any state after Internal Core Power Up up to Wait for valid VDIG, VCC	Condition 2: VCC_OV_R (VCC over-voltage)



Table 53. State transition table...continued

Transition	Description	Transition conditions
J	Any state after Internal Core Power Up up to Wait for valid VDIG, VCC	Condition 3: VCC_POR
J	Any state after Internal Core Power Up up to Wait for valid VDIG, VCC	Condition 4: VDIG_POR (includes UV on VDIG)
J	Any state after Internal Core Power Up up to Wait for valid VDIG, VCC	Condition 5: VDIG_OV
K	NORMAL STATE to Deep Fail Safe	OTP_DFS_EN = 1 && WD_ERR_CNT[1:0] >= WD_ERR_LIMIT[1:0] && WD_FAIL_IMPACT[1:0] = 0b10
L	INIT_RUN to ULPM Mode	(OTP_MODE_SYNCINB = 1 && OTP_ULPM_EN = 1 && MODE_SYNCIN pin = High)
M	ULPM Mode to INIT_RUN	(OTP_MODE_SYNCINB = 1 && OTP_ULPM_EN = 1 && MODE_SYNCIN pin = Low)

## 18 I<sup>2</sup>C Register Map

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Table 54. I<sup>2</sup>C register map

ADDRESS	Register Name	Default	BIT15 BIT7	BIT14 BIT6	BIT13 BIT5	BIT12 BIT4	BIT11 BIT3	BIT10 BIT2	BIT9 BIT1	BIT8 BIT0	
0x00	SW1CTRL	MSB	—	—	—	—	—	—	—	—	
		0000_0000	—	—	—	—	—	—	—	—	
		LSB	—	—	—	—	—	SW1_EN	SW1_MODE[1:0]		
		0000_0000	—	—	—	—	—	RWOTP	RWOTP	RWOTP	
0x01	NOT_SW1CTRL	MSB	—	—	—	—	—	—	—	—	
		0000_0000	—	—	—	—	—	—	—	—	
		LSB	—	—	—	—	—	NOT_SW1_EN	NOT_SW1_MODE[1:0]		
		0000_0111	—	—	—	—	—	RWOTP	RWOTP	RWOTP	
0x02	BLANK	MSB	—	—	—	—	—	—	—	—	
		0000_0000	—	—	—	—	—	—	—	—	
		LSB	—	—	—	—	—	—	—	—	
		0000_0000	—	—	—	—	—	—	—	—	
0x03	SW2CTRL	MSB	—	—	—	—	—	—	—	—	
		0000_0000	—	—	—	—	—	—	—	—	
		LSB	—	—	—	—	—	SW2_EN	SW2_MODE[1:0]		
		0000_0000	—	—	—	—	—	RWOTP	RWOTP	RWOTP	
0x04	NOT_SW2CTRL	MSB	—	—	—	—	—	—	—	—	
		0000_0000	—	—	—	—	—	—	—	—	
		LSB	—	—	—	—	—	NOT_SW2_EN	NOT_SW2_MODE[1:0]		
		0000_0111	—	—	—	—	—	RWOTP	RWOTP	RWOTP	

Table 54. I<sup>2</sup>C register map...continued

ADDRESS	Register Name	Default	BIT15 BIT7	BIT14 BIT6	BIT13 BIT5	BIT12 BIT4	BIT11 BIT3	BIT10 BIT2	BIT9 BIT1	BIT8 BIT0
0x06	GPIO_CTRL	MSB	—	—	—	—	—	—	—	MODE_RT
		0000_0000	—	—	—	—	—	—	—	RO
		LSB	—	—	GPIO3_RT	GPIO2_RT	GPIO1_RT	GPIO3_OUTPUT	GPIO2_OUTPUT	GPIO1_OUTPUT
		0000_0000	—	—	RO	RO	RO	RWOTP	RWOTP	RWOTP
0x07	NOT_GPIO_CTRL	MSB	—	—	—	—	—	—	—	—
		0000_0000	—	—	—	—	—	—	—	—
		LSB	—	—	—	—	—	NOT_GPIO3_OUTPUT	NOT_GPIO2_OUTPUT	NOT_GPIO1_OUTPUT
		0000_0111	—	—	—	—	—	RWOTP	RWOTP	RWOTP
0x09	CLOCK_CTRL	MSB	—	—	—	—	—	—	—	—
		0000_0000	—	—	—	—	—	—	—	—
		LSB	—	—	FSS_FMOD	FSS_EN	CLK_FREQ[3:0]			
		0000_0000	—	—	RWOTP	RWOTP	RWOTP	RWOTP	RWOTP	RWOTP
0x0A	NOT_CLOCK_CTRL	MSB	—	—	—	—	—	—	—	—
		0000_0000	—	—	—	—	—	—	—	—
		LSB	—	—	—	—	NOT_CLK_FREQ[3:0]			
		0000_0000	—	—	—	—	RWOTP	RWOTP	RWOTP	RWOTP
0x0C	WATCHDOG_CTRL1	MSB	WD_ERR_LIMIT[1:0]		—	WD_RFR_LIMIT[1:0]		—	WD_FAIL_IMPACT[1:0]	
		0100_0010	RW	RW	—	RW	RW	—	RWOTP	RWOTP
		LSB	—	WD_RFR_CNT[2:0]			WD_ERR_CNT[3:0]			
		0000_0000	—	RO	RO	RO	RO	RO	RO	RO

Table 54. I<sup>2</sup>C register map...continued

ADDRESS	Register Name	Default	BIT15 BIT7	BIT14 BIT6	BIT13 BIT5	BIT12 BIT4	BIT11 BIT3	BIT10 BIT2	BIT9 BIT1	BIT8 BIT0	
0x0D	NOT_WATCHDOG_CTRL1	MSB	NOT_WD_ERR_LIMIT[1:0]		—	NOT_WD_RFR_LIMIT[1:0]		—	NOT_WD_FAIL_IMPACT[1:0]		
		1001_1001	RW	RW	—	RW	RW	—	RWOTP	RWOTP	
		LSB	—	—	—	—	—	—	—	—	
		0000_0000	—	—	—	—	—	—	—	—	
0x0F	WATCHDOG_CTRL2	MSB	WD_WINDOW[3:0]				—	WDW_DC[2:0]			
		0011_0010	RW	RW	RW	RW	—	RW	RW	RW	
		LSB	—	—	—	—	—	—	—	—	
		0000_0000	—	—	—	—	—	—	—	—	
0x10	NOT_WATCHDOG_CTRL2	MSB	NOT_WD_WINDOW[3:0]				—	NOT_WDW_DC[2:0]			
		1100_0101	RWP	RWP	RWP	RWP	—	RWP	RWP	RWP	
		LSB	—	—	—	—	—	—	—	—	
		0000_0100	—	—	—	—	—	—	—	—	
0x11	WATCHDOG_SEED	MSB	WD_SEED[15:8]								
		0101_1010	EXTRW	EXTRW	EXTRW	EXTRW	EXTRW	EXTRW	EXTRW	EXTRW	
		LSB	WD_SEED[7:0]								
		1011_0010	EXTRW	EXTRW	EXTRW	EXTRW	EXTRW	EXTRW	EXTRW	EXTRW	
0x12	WATCHDOG_ANSWER	MSB	WD_ANSWER[15:8]								
		0000_0000	EXTRW	EXTRW	EXTRW	EXTRW	EXTRW	EXTRW	EXTRW	EXTRW	
		LSB	WD_ANSWER[7:0]								
		0000_0000	EXTRW	EXTRW	EXTRW	EXTRW	EXTRW	EXTRW	EXTRW	EXTRW	

Table 54. I<sup>2</sup>C register map...continued

ADDRESS	Register Name	Default	BIT15 BIT7	BIT14 BIT6	BIT13 BIT5	BIT12 BIT4	BIT11 BIT3	BIT10 BIT2	BIT9 BIT1	BIT8 BIT0
0x14	OD_ABIST_CTRL	MSB	—	—	—	—	—	—	—	—
		0000_0000	—	—	—	—	—	—	—	—
		LSB	—	—	—	—	—	—	—	OD_ABIST
		0000_0000	—	—	—	—	—	—	—	EXTRW
0x15	NOT_OD_ABIST	MSB	—	—	—	—	—	—	—	—
		0000_0000	—	—	—	—	—	—	—	—
		LSB	—	—	—	—	—	—	—	NOT_OD_ABIST
		0000_0001	—	—	—	—	—	—	—	EXTRW
0x16	BIST_STATUS1	MSB	—	BG_ERR	ABIST_SW2_UV_ERR	ABIST_SW2_OV_ERR	ABIST_SW1_UV_ERR	ABIST_SW1_OV_ERR	ABIST_VMON4_UV_ERR	ABIST_VMON4_OV_ERR
		0000_0000	—	RO	RO	RO	RO	RO	RO	RO
		LSB	ABIST_VMON3_UV_ERR	ABIST_VMON3_OV_ERR	ABIST_VMON2_UV_ERR	ABIST_VMON2_OV_ERR	ABIST_VMON1_UV_ERR	ABIST_VMON1_OV_ERR	ABIST_OSC_ERR	ABIST_CRC_ERR
		0000_0000	RO	RO	RO	RO	RO	RO	RO	RO
0x17	BIST_STATUS2	MSB	—	—	FS0B_STUCK_AT_0	FS0B_STUCK_AT_1	PGOOD2_STUCK_AT_0	PGOOD2_STUCK_AT_1	PGOOD1_STUCK_AT_0	PGOOD1_STUCK_AT_1
		0000_0000	—	—	FLGWC	FLGWC	FLGWC	FLGWC	FLGWC	FLGWC
		LSB	—	—	—	—	—	—	LBIST_DONE	LBIST_PASS
		0000_0000	—	—	—	—	—	—	RO	RO

Table 54. I<sup>2</sup>C register map...continued

ADDRESS	Register Name	Default	BIT15 BIT7	BIT14 BIT6	BIT13 BIT5	BIT12 BIT4	BIT11 BIT3	BIT10 BIT2	BIT9 BIT1	BIT8 BIT0
0x19	FAULT_CTRL	MSB	—	—	—	—	—	—	—	—
		0000_0000	—	—	—	—	—	—	—	—
		LSB	—	CLR_FLT_ERR_CNT	FLT_ERR_CNT[3:0]				FLT_ERR_CNT_LIMIT[1:0]	
		0000_0001	—	EXTRW	RO	RO	RO	RO	RW	RW
0x1A	NOT_FAULT_CTRL	MSB	—	—	—	—	—	—	—	—
		0000_0000	—	—	—	—	—	—	—	—
		LSB	—	NOT_CLR_FLT_ERR_CNT	—	—	—	—	NOT_FLT_ERR_CNT_LIMIT[1:0]	
		0100_0010	—	EXTRW	—	—	—	—	RW	RW
0x1C	VMON_STS	MSB	—	SW2_ILIM_I	SW1_ILIM_I	TSD_I	SW2_UV_I	SW1_UV_I	VMON4_UV_I	VMON3_UV_I
		0000_0000	—	FLGWC	FLGWC	FLGWC	FLGWC	FLGWC	FLGWC	FLGWC
		LSB	VMON2_UV_I	VMON1_UV_I	SW2_OV_I	SW1_OV_I	VMON4_OV_I	VMON3_OV_I	VMON2_OV_I	VMON1_OV_I
		0000_0000	FLGWC	FLGWC	FLGWC	FLGWC	FLGWC	FLGWC	FLGWC	FLGWC
0x1D	VMON_RT	MSB	—	SW2_ILIM_RT	SW1_ILIM_RT	TSD_RT	SW2_UV_RT	SW1_UV_RT	VMON4_UV_RT	VMON3_UV_RT
		0000_0000	—	RO	RO	RO	RO	RO	RO	RO
		LSB	VMON2_UV_RT	VMON1_UV_RT	SW2_OV_RT	SW1_OV_RT	VMON4_OV_RT	VMON3_OV_RT	VMON2_OV_RT	VMON1_OV_RT
		0000_0000	RO	RO	RO	RO	RO	RO	RO	RO

Table 54. I<sup>2</sup>C register map...continued

ADDRESS	Register Name	Default	BIT15 BIT7	BIT14 BIT6	BIT13 BIT5	BIT12 BIT4	BIT11 BIT3	BIT10 BIT2	BIT9 BIT1	BIT8 BIT0
0x1E	GPIO_STS	MSB	—	FCCU2_ERR	FCCU1_ERR	FCCU12_ERR	—	—	ERRMON2_I	ERRMON1_I
		0000_0000	—	FLGWC	FLGWC	FLGWC	—	—	FLGWC	FLGWC
		LSB	—	—	BAD_WD_TIMING	BAD_WD_DATA	—	—	I2C_CRC_ERR	I2C_REQ_ERR
		0000_0000	—	—	FLGWC	FLGWC	—	—	FLGWC	FLGWC
0x21	FCCU_CFG	MSB	—	FCCU12_FLT_POL	FCCU1_FLT_POL	FCCU2_FLT_POL	—	—	—	FCCU12_BISTABLE
		0000_0001	—	RW	RW	RW	—	—	—	RW
		LSB	—	—	—	—	—	—	—	—
		0000_0000	—	—	—	—	—	—	—	—
0x22	NOT_FCCU_CFG	MSB	—	NOT_FCCU12_FLT_POL	NOT_FCCU1_FLT_POL	NOT_FCCU2_FLT_POL	—	—	—	NOT_FCCU12_BISTABLE
		0111_0000	—	RW	RW	RW	—	—	—	RW
		LSB	—	—	—	—	—	—	—	—
		0000_0000	—	—	—	—	—	—	—	—
0x24	STATE_CTRL	MSB	DBG_EXIT	—	—	—	—	—	—	—
		0000_0000	WP	—	—	—	—	—	—	—
		LSB	—	—	—	—	—	—	GOTO_INIT_RUN	GOTO_NORMAL
		0000_0000	—	—	—	—	—	—	EXTRW	EXTRW



Table 54. I<sup>2</sup>C register map...continued

ADDRESS	Register Name	Default	BIT15 BIT7	BIT14 BIT6	BIT13 BIT5	BIT12 BIT4	BIT11 BIT3	BIT10 BIT2	BIT9 BIT1	BIT8 BIT0	
0x25	NOT_STATE_CTRL	MSB	—	—	—	—	—	—	—	—	
		0000_0000	—	—	—	—	—	—	—	—	
		LSB	—	—	—	—	—	—	NOT_GOTO_INIT_RUN	NOT_GOTO_NORMAL	
		0000_0011	—	—	—	—	—	—	EXTRW	EXTRW	
0x26	STATE	MSB	—	—	—	—	—	—	—	—	
		0000_0000	—	—	—	—	—	—	—	—	
		LSB	—	—	—	PMIC_FSM[4:0]					
		0000_0000	—	—	—	RO	RO	RO	RO	RO	
0x27	ID1	MSB	—	—	FULL_LAYER_REV[2:0]			METAL_LAYER_REV[2:0]			
		0000_0000	—	—	RO	RO	RO	RO	RO	RO	
		LSB	FAM_ID[3:0]				DEVICEID[3:0]				
		1011_0000	RO	RO	RO	RO	RO	RO	RO	RO	
0x28	ID2	MSB	Reserved for NXP use.								
		0000_0000	Reserved for NXP use.								
		LSB	Reserved for NXP use.								
		1011_0000	Reserved for NXP use.								

## 18.1 Register descriptions

The following bit-types are used in the FS5600 register map.

Table 55. FS5600 register map bit-types

Bit type	Description
RWOTP	Read-write bit with default value loaded from OTP
RO	Read-only
RW	Read-write capable
FLGWC	Write 1 to clear flag bit
EXTRW	Read-write bit with self-set/reset capability

### 18.1.1 SW1CTRL register

Table 56. SW1CTRL register description

Bit	Symbol	Description
2	SW1_EN	Switcher enable. Applied to the switcher only when SW1_EN = NOT(NOT_SW1_EN). 1b'0 — Disable SW1. 1b'1 — SW1 Enabled provided EN1 is high. Reset Condition — POR
1 to 0	SW1_MODE[1:0]	SW1 Operating mode. Applied to the switcher only when SW1_MODE[1:0] = NOT(NOT_SW1_MODE[1:0]). 2b'00 — SW1 in PFM Mode. 2b'01 — Reserved. 2b'10 — Reserved. 2b'11 — SW1 in PWM mode. Reset Condition — POR

### 18.1.2 NOT\_SW1CTRL register

Table 57. NOT\_SW1CTRL register description

Bit	Symbol	Description
2	NOT_SW1_EN	Switcher enable. Applied to the switcher only when SW1_EN = NOT(NOT_SW1_EN). 1b'0 — See SW1_EN in SW1CTRL register. 1b'1 — See SW1_EN in SW1CTRL register. Reset Condition — POR
1 to 0	NOT_SW1_MODE[1:0]	— SW1 Operating Mode. Applied to the switcher only when SW1_MODE[1:0] = NOT(NOT_SW1_MODE[1:0]) 2b'00 — See SW1_MODE[1:0] in SW1CTRL register. 2b'01 — See SW1_MODE[1:0] in SW1CTRL register. 2b'10 — See SW1_MODE[1:0] in SW1CTRL register. 2b'11 — See SW1_MODE[1:0] in SW1CTRL register. Reset — Condition POR

### 18.1.3 SW2CTRL register

Table 58. SW2CTRL register description

Bit	Symbol	Description
2	SW2_EN	Switcher enable. Applied to the switcher only when SW2_EN = NOT(NOT_SW2_EN). 1b'0 — Disable SW2. 1b'1 — SW2 Enabled provided EN2 is high. Reset Condition — POR
1 to 0	SW2_MODE[1:0]	SW2 Operating mode. Applied to the switcher only when SW2_MODE[1:0] = NOT(NOT_SW2_MODE[1:0]). 2b'00 — SW2 in PFM Mode. 2b'01 — Reserved. 2b'10 — Reserved. 2b'11 — SW2 in PWM Mode. Reset Condition — POR

### 18.1.4 NOT\_SW2CTRL register

Table 59. NOT\_SW2CTRL register description

Bit	Symbol	Description
2	NOT_SW2_EN	Switcher enable. Applied to the switcher only when SW2_EN = NOT(NOT_SW2_EN). 1b'0 — See SW2_EN in SW2CTRL register. 1b'1 — See SW2_EN in SW2CTRL register. Reset Condition — POR
1 to 0	NOT_SW2_MODE[1:0]	SW2 Operating mode. Applied to the switcher only when SW2_MODE[1:0] = NOT(NOT_SW2_MODE[1:0]). 2b'00 — See SW2_MODE[1:0] in SW2CTRL register. 2b'01 — See SW2_MODE[1:0] in SW2CTRL register. 2b'10 — See SW2_MODE[1:0] in SW2CTRL register. 2b'11 — See SW2_MODE[1:0] in SW2CTRL register. Reset Condition — POR

### 18.1.5 GPIO\_CTRL register

Table 60. GPIO\_CTRL register description

Bit	Symbol	Description
8	MODE_RT	SYNCIN_MODE input state (after deglitcher). 1b'0 — SYNCIN_MODE pin is low. 1b'1 — SYNCIN_MODE pin is high. Reset Condition — POR
5	GPIO3_RT	GPIO3 input state (after deglitcher). 1b'0 — GPIO3 pin is low. 1b'1 — GPIO3 pin is high. Reset Condition — POR

Table 60. GPIO\_CTRL register description...continued

Bit	Symbol	Description
4	GPIO2_RT	GPIO2 input state (after deglitcher). 1b'0 — GPIO2 pin is low. 1b'1 — GPIO2 pin is high. Reset Condition — POR
3	GPIO1_RT	GPIO1 input state (after deglitcher). 1b'0 — GPIO1_VDDOTP pin is low. 1b'1 — GPIO1_VDDOTP pin is high. Reset Condition — POR
2	GPIO3_OUTPUT	GPIO3 output control if programmed as output by OTP_GPIO3_CFG[1:0]. Applied to the output only when GPIO3_OUTPUT = NOT(NOT_GPIO3_OUTPUT). 1b'0 — GPIO3 pin output driven low. 1b'1 — GPIO3 pin output HZ (pull-up). Reset Condition — POR
1	GPIO2_OUTPUT	GPIO2 output control if programmed as output by OTP_GPIO2_CFG[1:0]. Applied to the output only when GPIO2_OUTPUT = NOT(NOT_GPIO2_OUTPUT). 1b'0 — GPIO2 pin output driven low. 1b'1 — GPIO2 pin output HZ (pull-up). Reset Condition — POR
0	GPIO1_OUTPUT	GPIO1 output control if programmed as output by OTP_GPIO1_CFG[1:0]. Applied to the output only when GPIO1_OUTPUT = NOT(NOT_GPIO1_OUTPUT). 1b'0 — GPIO1_VDDOTP pin output driven low. 1b'1 — GPIO1_VDDOTP pin output HZ (pull-up) Reset Condition — POR.

### 18.1.6 NOT\_GPIO\_CTRL register

Table 61. NOT\_GPIO\_CTRL register description

Bit	Symbol	Description
2	NOT_GPIO3_OUTPUT	GPIO3 output control. 1b'0 — See GPIO3_OUTPUT in GPIO_CTRL register. 1b'1 — See GPIO3_OUTPUT in GPIO_CTRL register. Reset Condition — POR
1	NOT_GPIO2_OUTPUT	GPIO2 output control 1b'0 — See GPIO2_OUTPUT in GPIO_CTRL register. 1b'1 — See GPIO2_OUTPUT in GPIO_CTRL register. Reset Condition — POR
0	NOT_GPIO1_OUTPUT	GPIO1 output control 1b'0 — See GPIO1_OUTPUT in GPIO_CTRL register. 1b'1 — See GPIO1_OUTPUT in GPIO_CTRL register. Reset Condition — POR

18.1.7 CLOCK\_CTRL register

Table 62. CLOCK\_CTRL register description

Bit	Symbol	Description
5	FSS_FMOD	Frequency (triangular period) of internal 20 MHz oscillator frequency spread spectrum. 1b'0 — 23.5 kHz 1b'1 — 94 kHz Reset Condition — POR
4	FSS_EN	Internal 20 MHz oscillator frequency spread spectrum control. 1b'0 — Frequency spread spectrum disabled. 1b'1 — Frequency spread spectrum enabled. Reset Condition — POR
3 to 0	CLK_FREQ[3:0]	Internal 20 MHz oscillator frequency selection (Unit MHz). Applied to the oscillator only when CLK_FREQ[3:0] = NOT(NOT_CLK_FREQ[3:0]) 4b'0000 — 20 4b'0001 — 21 4b'0010 — 22 4b'0011 — 23 4b'0100 — 24 4b'0101 — NA 4b'0110 — NA 4b'0111 — NA 4b'1000 — NA 4b'1001 — 16 4b'1010 — 17 4b'1011 — 18 4b'1100 — 19 4b'1101 — NA 4b'1110 — NA 4b'1111 — NA Reset Condition — POR

18.1.8 NOT\_CLOCK\_CTRL register

Table 63. NOT\_CLOCK\_CTRL register description

Bit	Symbol	Description
3 to 0	NOT_CLK_FREQ[3:0]	Internal 20 MHz oscillator frequency programming (Unit MHz). 4b'0000 - 4b'1111 — See CLK_FREQ[3:0] in CLK_CTRL register. Reset Condition — POR

## 18.1.9 WATCHDOG\_CTRL1 register

Table 64. WATCHDOG\_CTRL1 register description

Bit	Symbol	Description
15 to 14	WD_ERR_LIMIT[1:0]	Watchdog error counter limit. Applied only when WD_ERR_LIMIT[1:0] = NOT(NOT_WD_ERR_LIMIT[1:0]) 00 — Max value is 8. 01 — Max value is 6. 10 — Max value is 4. 11 — Max value is 2. Reset Condition — POR
12 to 11	WD_RFR_LIMIT[1:0]	Watchdog refresh counter limit. Applied only when WD_RFR_LIMIT[1:0] = NOT(NOT_WD_RFR_LIMIT[1:0]) 00 — Max value is 6. 01 — Max value is 4. 10 — Max value is 2. 11 — Max value is 1. Reset Condition — POR
9 to 8	WD_FAIL_IMPACT[1:0]	Watchdog fail impact. Applied only when WD_FAIL_IMPACT[1:0] = NOT(NOT_WD_FAIL_IMPACT[1:0]) 00 — No impact on FSM : stay in NORMAL state. 01 — Transition to INIT_RUN or remain in INIT_RUN state. 10 — Transition to DEEP_FAIL_SAFE state. 11 — No impact on FSM : stay in NORMAL state. Reset Condition — POR
6 to 4	WD_RFR_CNT[2:0]	Watchdog refresh counter value. Resets on overflow. 3b'000 — Counter Value = 0. 3b'001 — Counter Value = 1. 3b'010 — Counter Value = 2. 3b'011 — Counter Value = 3. 3b'100 — Counter Value = 4. 3b'101 — Counter Value = 5. 3b'110 — Counter Value = 6. 3b'111 — Counter Value = 7. Reset Condition — POR

Table 64. WATCHDOG\_CTRL1 register description...continued

Bit	Symbol	Description
3 to 0	WD_ERR_CNT[3:0]	Watchdog error counter value 4b'0000 — Counter Value = 0. 4b'0001 — Counter Value = 1. 4b'0010 — Counter Value = 2. 4b'0011 — Counter Value = 3. 4b'0100 — Counter Value = 4. 4b'0101 — Counter Value = 5. 4b'0110 — Counter Value = 6. 4b'0111 — Counter Value = 7. 4b'1000 — Counter Value = 8. 4b'1001 — Counter Value = 9. 4b'1010 — Counter Value = 10. 4b'1011 — Counter Value = 11. 4b'1100 — Counter Value = 12. 4b'1101 — Counter Value = 13. 4b'1110 — Counter Value = 14. 4b'1111 — Counter Value = 15. Reset Condition — POR

### 18.1.10 NOT\_WATCHDOG\_CTRL1 register

Table 65. NOT\_WATCHDOG\_CTRL1 register description

Bit	Symbol	Description
15 to 14	NOT_WD_ERR_LIMIT[1:0]	Watchdog error counter limit. 2b'00 — See WD_ERR_LIMIT[1:0] in WATCHDOG_CTRL1 register. 2b'01 — See WD_ERR_LIMIT[1:0] in WATCHDOG_CTRL1 register. 2b'10 — See WD_ERR_LIMIT[1:0] in WATCHDOG_CTRL1 register. 2b'11 — See WD_ERR_LIMIT[1:0] in WATCHDOG_CTRL1 register. Reset Condition — POR
12 to 11	NOT_WD_RFR_LIMIT[1:0]	Watchdog refresh counter limit. 2b'00 — See WD_RFR_LIIMIT[1:0] in WATCHDOG_CTRL1 register. 2b'01 — See WD_RFR_LIIMIT[1:0] in WATCHDOG_CTRL1 register. 2b'10 — See WD_RFR_LIIMIT[1:0] in WATCHDOG_CTRL1 register. 2b'11 — See WD_RFR_LIIMIT[1:0] in WATCHDOG_CTRL1 register. Reset Condition — POR
9 to 8	NOT_WD_FAIL_IMPACT[1:0]	Watchdog fail impact. 2b'00 — See WD_FAIL_IMPACT[1:0] in WATCHDOG_CTRL1 register. 2b'01 — See WD_FAIL_IMPACT[1:0] in WATCHDOG_CTRL1 register. 2b'10 — See WD_FAIL_IMPACT[1:0] in WATCHDOG_CTRL1 register. 2b'11 — See WD_FAIL_IMPACT[1:0] in WATCHDOG_CTRL1 register. Reset Condition — POR

## 18.1.11 WATCHDOG\_CTRL2 register

Table 66. WATCHDOG\_CTRL2 register description

Bit	Symbol	Description
15 to 12	WD_WINDOW[3:0]	Watchdog window duration, Applied only when WD_WD_WINDOW[3:0] = NOT(NOT_WD_WINDOW[3:0]) 4b'0000 — Infinite. 4b'0001 — 1 ms. 4b'0010 — 2 ms. 4b'0011 — 3 ms. 4b'0100 — 4 ms. 4b'0101 — 6 ms. 4b'0110 — 8 ms. 4b'0111 — 12 ms. 4b'1000 — 16 ms. 4b'1001 — 24 ms. 4b'1010 — 32 ms. 4b'1011 — 64 ms. 4b'1100 — 128 ms. 4b'1101 — 256 ms. 4b'1110 — 512 ms. 4b'1111 — 1024 ms. Reset Condition — POR
10 to 8	WDW_DC[2:0]	Watchdog window duty cycle. Applied only when WDW_DC[2:0] = NOT(NOT_WDW_DC[2:0]). 3b'000 — Closed window 31.25 % Open window 68.75 %. 3b'001 — Closed window 37.5 % Open window 62.5 %. 3b'010 — Closed window 50 % Open window 50 %. 3b'011 — Closed window 62.5 % Open window 37.5 %. 3b'100 — Closed window 68.75 % Open window 31.25 %. 3b'101 — Closed window 50 % Open window 50 %. 3b'110 — Closed window 50 % Open window 50 %. 3b'111 — Closed window 50 % Open window 50 %. Reset Condition — POR

## 18.1.12 NOT\_WATCHDOG\_CTRL2 register

Table 67. NOT\_WATCHDOG\_CTRL2 register description

Bit	Symbol	Description
15 to 12	NOT_WD_WINDOW[3:0]	Watchdog window duration. 4b'0000 - 4b'1111 — See WD_WINDOW[3:0] in WATCHDOG_CTRL2 register. Reset Condition — POR
10 to 8	NOT_WDW_DC[2:0]	Watchdog window duty cycle. 3b'000 - 3b'111 — See WDW_DC[2:0] in WATCHDOG_CTRL2 register. Reset Condition — POR



18.1.13 WATCHDOG\_SEED register

Table 68. WATCHDOG\_SEED register description

Bit	Symbol	Description
15 to 0	WD_SEED[15:0]	Watchdog seed. WD_SEED[15:0] — Default value (after reset) is 16'h5AB2 for simple or challenger watchdog. It is impossible to write 16'hFFFF for challenger watchdog. It is impossible to write 16'h0000 or 16'hFFFF for simple watchdog. Reset Condition — POR

18.1.14 WATCHDOG\_ANSWER register

Table 69. WATCHDOG\_ANSWER register description

Bit	Symbol	Description
15 to 0	WD_ANSWER[15:0]	Watchdog answer. WD_ANSWER[15:0] — For good data refresh: <ul style="list-style-type: none"> <li>• For simple watchdog WD_ANSWER = WD_SEED.</li> <li>• For challenger watchdog WD_ANSWER = ~WD_SEED.</li> </ul> Reset Condition — POR

18.1.15 OD\_ABIST\_CTRL register

Table 70. OD\_ABIST\_CTRL register description

Bit	Symbol	Description
0	OD_ABIST	On-demand ABIST. 1b'0 — No action. 1b'1 — Start on-demand ABIST if OD_ABIST = NOT(NOT_OD_ABIST), self cleared when ABIST is finished. Reset Condition — POR

18.1.16 NOT\_OD\_ABIST register

Table 71. NOT\_OD\_ABIST register description

Bit	Symbol	Description
0	NOT_OD_ABIST	On-demand ABIST. 1b'0 — See OD_ABIST in OD_ABIST_CTRL register. 1b'1 — See OD_ABIST in OD_ABIST_CTRL register. Reset Condition — POR

18.1.17 BIST\_STATUS1 register

Table 72. BIST\_STATUS1 register description

Bit	Symbol	Description
14	BG_ERR	Bandgap monitor ABIST status. 1b'0 — No error. 1b'1 — Error detected. Reset Condition — POR

## Automotive buck regulator and controller with voltage monitors and watchdog timer

Table 72. BIST\_STATUS1 register description...continued

Bit	Symbol	Description
13	ABIST_SW2_UV_ERR	Switcher SW2 undervoltage monitor ABIST status. 1b'0 — No error. 1b'1 — Error detected. Reset Condition — POR
12	ABIST_SW2_OV_ERR	Switcher SW2 overvoltage monitor ABIST status. 1b'0 — No error. 1b'1 — Error detected. Reset Condition — POR
11	ABIST_SW1_UV_ERR	Switcher SW1 undervoltage monitor ABIST status. 1b'0 — No error. 1b'1 — Error detected. Reset Condition — POR
10	ABIST_SW1_OV_ERR	Switcher SW1 overvoltage monitor ABIST status. 1b'0 — No error. 1b'1 — Error detected. Reset Condition — POR
9	ABIST_VMON4_UV_ERR	VMON4 undervoltage monitor ABIST status. 1b'0 — No error. 1b'1 — Error detected. Reset Condition — POR
8	ABIST_VMON4_OV_ERR	VMON4 overvoltage monitor ABIST status. 1b'0 — No error. 1b'1 — Error detected. Reset Condition — POR
7	ABIST_VMON3_UV_ERR	VMON3 undervoltage monitor ABIST status. 1b'0 — No error. 1b'1 — Error detected. Reset Condition — POR
6	ABIST_VMON3_OV_ERR	VMON3 overvoltage monitor ABIST status. 1b'0 — No error. 1b'1 — Error detected. Reset Condition — POR
5	ABIST_VMON2_UV_ERR	VMON2 undervoltage monitor ABIST status. 1b'0 — No error. 1b'1 — Error detected. Reset Condition — POR
4	ABIST_VMON2_OV_ERR	VMON2 overvoltage monitor ABIST status 1b'0 — No error. 1b'1 — Error detected. Reset Condition — POR
3	ABIST_VMON1_UV_ERR	VMON1 undervoltage monitor ABIST status. 1b'0 — No error. 1b'1 — Error detected. Reset Condition — POR

Table 72. BIST\_STATUS1 register description...continued

Bit	Symbol	Description
2	ABIST_VMON1_OV_ERR	VMON1 overvoltage monitor ABIST status. 1b'0 — No error. 1b'1 — Error detected. Reset Condition — POR
1	ABIST_OSC_ERR	Oscillators 20 MHz / 100 kHz monitor ABIST status. 1b'0 — No error. 1b'1 — Error detected POR
0	ABIST_CRC_ERR	OTP CRC status calculated during ABIST. 1b'0 — No error. 1b'1 — Error detected. Reset Condition — POR

### 18.1.18 BIST\_STATUS2 register

Table 73. BIST\_STATUS2 register description

Bit	Symbol	Description
13	FS0B_STUCK_AT_0	FS0B pin stuck at 0 flag. 1b'0 — No stuck at 0 detected. 1b'1 — Stuck at 0 detected. Reset Condition — POR
12	FS0B_STUCK_AT_1	FS0B pin stuck at 1 flag. 1b'0 — No error. 1b'1 — Stuck at 1 detected. Reset Condition — POR
11	PGOOD2_STUCK_AT_0	PGOOD2 pin stuck at 0 flag. 1b'0 — No stuck at 0 detected. 1b'1 — Stuck at 0 detected. Reset Condition — POR
10	PGOOD2_STUCK_AT_1	PGOOD2 pin stuck at 1 flag. 1b'0 — No error. 1b'1 — Stuck at 1 detected. Reset Condition — POR
9	PGOOD1_STUCK_AT_0	PGOOD1 pin stuck at 0 flag. 1b'0 — No stuck at 0 detected. 1b'1 — Stuck at 0 detected. Reset Condition — POR
8	PGOOD1_STUCK_AT_1	PGOOD1 pin stuck at 1 flag. 1b'0 — No stuck at 1 detected. 1b'1 — Stuck at 1 detected. Reset Condition — POR
1	LBIST_DONE	LBIST completion status. 1b'0 — LBIST did not run. 1b'1 — LBIST ran. Reset Condition — POR

Table 73. BIST\_STATUS2 register description...continued

Bit	Symbol	Description
0	LBIST_PASS	Logic BIST status. 1b'0 — Fail or not run. 1b'1 — Logic BIST done and pass. Reset Condition — POR

### 18.1.19 FAULT\_CTRL register

Table 74. FAULT\_CTRL register description

Bit	Symbol	Description
6	CLR_FLT_ERR_CNT	Clear fault error counter. 1b'0 — Nothing happens. 1b'1 — Clear fault error counter. Clear CLR_FLT_ERR_CNT bit. Reset Condition — POR
5 to 2	FLT_ERR_CNT[3:0]	Fault error counter value. 4b'0000 — Counter Value = 0. 4b'0001 — Counter Value = 1. 4b'0010 — Counter Value = 2. 4b'0011 — Counter Value = 3. 4b'0100 — Counter Value = 4. 4b'0101 — Counter Value = 5. 4b'0110 — Counter Value = 6. 4b'0111 — Counter Value = 7. 4b'1000 — Counter Value = 8. 4b'1001 — Counter Value = 9. 4b'1010 — Counter Value = 10. 4b'1011 — Counter Value = 11. 4b'1100 — Counter Value = 12. 4b'1101 — Counter Value = 13. 4b'1110 — Counter Value = 14. 4b'1111 — Counter Value = 15. Reset Condition — POR
1 to 0	FLT_ERR_CNT_LIMIT[1:0]	Fault error counter limit. Applied only when FLT_ERR_CNT_LIMIT[1:0] = NOT(NOT_FLT_ERR_CNT_LIMIT[1:0]). 2b'00 — Max value is 1. 2b'01 — Max value is 2. 2b'10 — Max value is 6. 2b'11 — Max value is 12. Reset Condition — POR

## 18.1.20 NOT\_FAULT\_CTRL register

Table 75. NOT\_FAULT\_CTRL register description

Bit	Symbol	Description
6	NOT_CLR_FLT_ERR_CNT	Clear fault error counter (NOT bit). 1b'0 — See CLR_FLT_ERR_CNT in FAULT_CTRL register. 1b'1 — See CLR_FLT_ERR_CNT in FAULT_CTRL register. Reset Condition — POR
1 to 0	NOT_FLT_ERR_CNT_LIMIT[1:0]	Fault error counter limit. 2b'00 — See FLT_ERR_CNT_LIMIT[1:0] in FAULT_CTRL register. 2b'01 — See FLT_ERR_CNT_LIMIT[1:0] in FAULT_CTRL register. 2b'10 — See FLT_ERR_CNT_LIMIT[1:0] in FAULT_CTRL register. 2b'11 — See FLT_ERR_CNT_LIMIT[1:0] in FAULT_CTRL register. Reset Condition — POR

## 18.1.21 VMON\_STS register

Table 76. VMON\_STS register description

Bit	Symbol	Description
14	SW2_ILIM_I	SW2 current limit fault. 1b'0 — No overvoltage. 1b'1 — Current limit detected. Reset Condition — POR
13	SW1_ILIM_I	SW1 current limit fault. 1b'0 — No overvoltage. 1b'1 — Current limit detected. Reset Condition — POR
12	TSD_I	Thermal shutdown indicator. 1b'0 — No thermal shutdown or cleared. 1b'1 — Thermal shutdown detected. Reset Condition — POR
11	SW2_UV_I	SW2 monitor undervoltage. 1b'0 — No overvoltage. 1b'1 — Overvoltage detected. Reset Condition — POR
10	SW1_UV_I	SW1 monitor undervoltage. 1b'0 — No overvoltage. 1b'1 — Overvoltage detected. Reset Condition — POR
9	VMON4_UV_I	VMON4 monitor undervoltage. 1b'0 — No overvoltage. 1b'1 — Overvoltage detected. Reset Condition — POR
8	VMON3_UV_I	VMON3 monitor undervoltage. 1b'0 — No overvoltage. 1b'1 — Overvoltage detected. Reset Condition — POR

Table 76. VMON\_STS register description...continued

Bit	Symbol	Description
7	VMON2_UV_I	VMON2 monitor undervoltage. 1b'0 — No overvoltage. 1b'1 — Overvoltage detected. Reset Condition — POR
6	VMON1_UV_I	VMON1 monitor undervoltage. 1b'0 — No overvoltage. 1b'1 — Overvoltage detected. Reset Condition — POR
5	SW2_OV_I	SW2 monitor overvoltage. 1b'0 — No overvoltage. 1b'1 — Overvoltage detected. Reset Condition — POR
4	SW1_OV_I	SW1 monitor overvoltage. 1b'0 — No overvoltage. 1b'1 — Overvoltage detected. Reset Condition — POR
3	VMON4_OV_I	VMON4 monitor overvoltage. 1b'0 — No overvoltage. 1b'1 — Overvoltage detected. Reset Condition — POR
2	VMON3_OV_I	VMON3 monitor overvoltage. 1b'0 — No overvoltage. 1b'1 — Overvoltage detected. Reset Condition — POR
1	VMON2_OV_I	VMON2 monitor overvoltage. 1b'0 — No overvoltage. 1b'1 — Overvoltage detected. Reset Condition — POR
0	VMON1_OV_I	VMON1 monitor overvoltage. 1b'0 — No overvoltage. 1b'1 — Overvoltage detected. Reset Condition — POR

### 18.1.22 VMON\_RT register

Table 77. VMON\_RT register description

Bit	Symbol	Description
14	SW2_ILIM_RT	SW2 current limit. 1b'0 — No current limit fault. 1b'1 — Current limit exists. Reset Condition — POR
13	SW1_ILIM_RT	SW1 current limit. 1b'0 — No current limit fault. 1b'1 — Current limit exists. Reset Condition — POR

Table 77. VMON\_RT register description...continued

Bit	Symbol	Description
12	TSD_RT	thermal shutdown indicator. 1b'0 — No thermal shutdown or cleared. 1b'1 — Thermal shutdown detected. Reset Condition — POR
11	SW2_UV_RT	SW2 monitor undervoltage. 1b'0 — No overvoltage. 1b'1 — Overvoltage detected. Reset Condition — POR
10	SW1_UV_RT	SW1 monitor undervoltage. 1b'0 — No overvoltage. 1b'1 — Overvoltage detected. Reset Condition — POR
9	VMON4_UV_RT	VMON4 monitor undervoltage. 1b'0 — No overvoltage. 1b'1 — Overvoltage detected. Reset Condition — POR
8	VMON3_UV_RT	VMON3 monitor undervoltage. 1b'0 — No overvoltage. 1b'1 — Overvoltage detected. Reset Condition — POR
7	VMON2_UV_RT	VMON2 monitor undervoltage. 1b'0 — No overvoltage. 1b'1 — Overvoltage detected. Reset Condition — POR
6	VMON1_UV_RT	VMON1 monitor undervoltage. 1b'0 — No overvoltage. 1b'1 — Overvoltage detected. Reset Condition — POR
5	SW2_OV_RT	SW2 monitor overvoltage. 1b'0 — No overvoltage. 1b'1 — Overvoltage detected. Reset Condition — POR
4	SW1_OV_RT	SW1 monitor overvoltage. 1b'0 — No overvoltage. 1b'1 — Overvoltage detected. Reset Condition — POR
3	VMON4_OV_RT	VMON4 monitor overvoltage. 1b'0 — No overvoltage. 1b'1 — Overvoltage detected. Reset Condition — POR
2	VMON3_OV_RT	VMON3 monitor overvoltage. 1b'0 — No overvoltage. 1b'1 — Overvoltage detected. Reset Condition — POR

Table 77. VMON\_RT register description...continued

Bit	Symbol	Description
1	VMON2_OV_RT	VMON2 monitor overvoltage. 1b'0 — No overvoltage. 1b'1 — Overvoltage detected. Reset Condition — POR
0	VMON1_OV_RT	VMON1 monitor overvoltage. 1b'0 — No overvoltage. 1b'1 — Overvoltage detected. Reset Condition — POR

### 18.1.23 GPIO\_STS register

Table 78. GPIO\_STS register description

Bit	Symbol	Description
14	FCCU2_ERR	FCCU2 error. 1b'0 — No error. 1b'1 — Error detected. Reset Condition — POR
13	FCCU1_ERR	FCCU1 error. 1b'0 — No error. 1b'1 — Error detected. Reset Condition — POR
12	FCCU12_ERR	FCCU12 error (bistable). 1b'0 — No error. 1b'1 — Error detected. Reset Condition — POR
9	ERRMON2_I	ERRMON2 error. 1b'0 — No error. 1b'1 — Error detected. Reset Condition — POR
8	ERRMON1_I	ERRMON1 error. 1b'0 — No error. 1b'1 — Error detected. Reset Condition — POR
5	BAD_WD_TIMING	Watchdog error bad timing. 1b'0 — No error. 1b'1 — Error detected, during watchdog refresh. Bad timing (wrote to answer register in closed window or timeout). Reset Condition — POR
4	BAD_WD_DATA	Watchdog error bad answer. 1b'0 — No error. 1b'1 — Error detected, during watchdog refresh. Bad data written in answer register. Reset Condition — POR



Table 78. GPIO\_STS register description...continued

Bit	Symbol	Description
1	I2C_CRC_ERR	I2C CRC error. 1b'0 — No error. 1b'1 — CRC error detected in write operation. Reset Condition — POR
0	I2C_REQ_ERR	I2C request error. 1b'0 — No error. 1b'1 — Request error. Reset Condition — POR

### 18.1.24 FCCU\_CFG register

Table 79. FCCU\_CFG register description

Bit	Symbol	Description
14	FCCU12_FLT_POL	FCCU bistable fault polarity. Applied only when FCCU12_FLT_POL = NOT(NOT_FCCU12_FLT_POL). 1b'0 — FCCU1 low or FCCU2 high is a fault. 1b'1 — FCCU1 high or FCCU2 low is a fault. Reset Condition — POR
13	FCCU1_FLT_POL	FCCU1 fault polarity. Applied only when FCCU1_FLT_POL = NOT(NOT_FCCU1_FLT_POL). 1b'0 — FCCU1 low is a fault. 1b'1 — FCCU1 high is a fault. Reset Condition — POR
12	FCCU2_FLT_POL	FCCU2 fault polarity. Applied only when FCCU2_FLT_POL = NOT(NOT_FCCU2_FLT_POL). 1b'0 — FCCU2 low is a fault. 1b'1 — FCCU2 high is a fault. Reset Condition — POR
8	FCCU12_BISTABLE	FCCU1/FCCU2 bistable control. Applied only when FCC12_BISTABLE = NOT(NOT_FCCU12_BISTABLE). 1b'0 — Independent FCCU1/FCCU2. 1b'1 — FCCU1/FCCU2 configured as bistable. Reset Condition — POR

### 18.1.25 NOT\_FCCU\_CFG register

Table 80. NOT\_FCCU\_CFG register description

Bit	Symbol	Description
14	NOT_FCCU12_FLT_POL	FCCU bistable fault polarity. See FCCU12_FLT_POL in FCCU_CFG register. Reset Condition — POR

Table 80. NOT\_FCCU\_CFG register description...continued

Bit	Symbol	Description
13	NOT_FCCU1_FLT_POL	FCCU1 fault polarity. See FCCU1_FLT_POL in FCCU_CFG register. Reset Condition — POR
12	NOT_FCCU2_FLT_POL	FCCU2 fault polarity. See FCCU2_FLT_POL in FCCU_CFG register. Reset Condition — POR
8	NOT_FCCU12_BISTABLE	FCCU1/FCCU2 bistable control. See FCCU12_BISTABLE in FCCU_CFG register. Reset Condition — POR

### 18.1.26 STATE\_CTRL register

Table 81. STATE\_CTRL register description

Bit	Symbol	Description
15	DBG_EXIT	Used to unlatch debug mode. 1b'0 — Nothing happens. 1b'1 — Exit debug mode. Reset Condition — POR
1	GOTO_INIT_RUN	Go to INIT_RUN state command. Applied only when GOTO_INIT_RUN = NOT(NOT_GOTO_INIT_RUN). 1b'0 — Nothing happens. 1b'1 — Go to INIT_RUN state (if current state is NORMAL, bit self-cleared when in state INIT_RUN). Reset Condition — POR
0	GOTO_NORMAL	Go to NORMAL state command. Applied only when GOTO_NORMAL = NOT(NOT_GOTO_NORMAL). 1b'0 — Nothing happens. 1b'1 — Go to NORMAL state (if current state is INIT_RUN, bit self-cleared when in state NORMAL). Reset Condition — POR

### 18.1.27 NOT\_STATE\_CTRL register

Table 82. NOT\_STATE\_CTRL register description

Bit	Symbol	Description
1	NOT_GOTO_INIT_RUN	Go to INIT_RUN state command. 1b'0 — See GOTO_INIT_RUN in STATE_CTRL register. 1b'1 — See GOTO_INIT_RUN in STATE_CTRL register. Reset Condition — POR
0	NOT_GOTO_NORMAL	Go to NORMAL state command. 1b'0 — See GOTO_NORMAL in STATE_CTRL register. 1b'1 — See GOTO_NORMAL in STATE_CTRL register. Reset Condition — POR

## 18.1.28 STATE register

Table 83. STATE register description

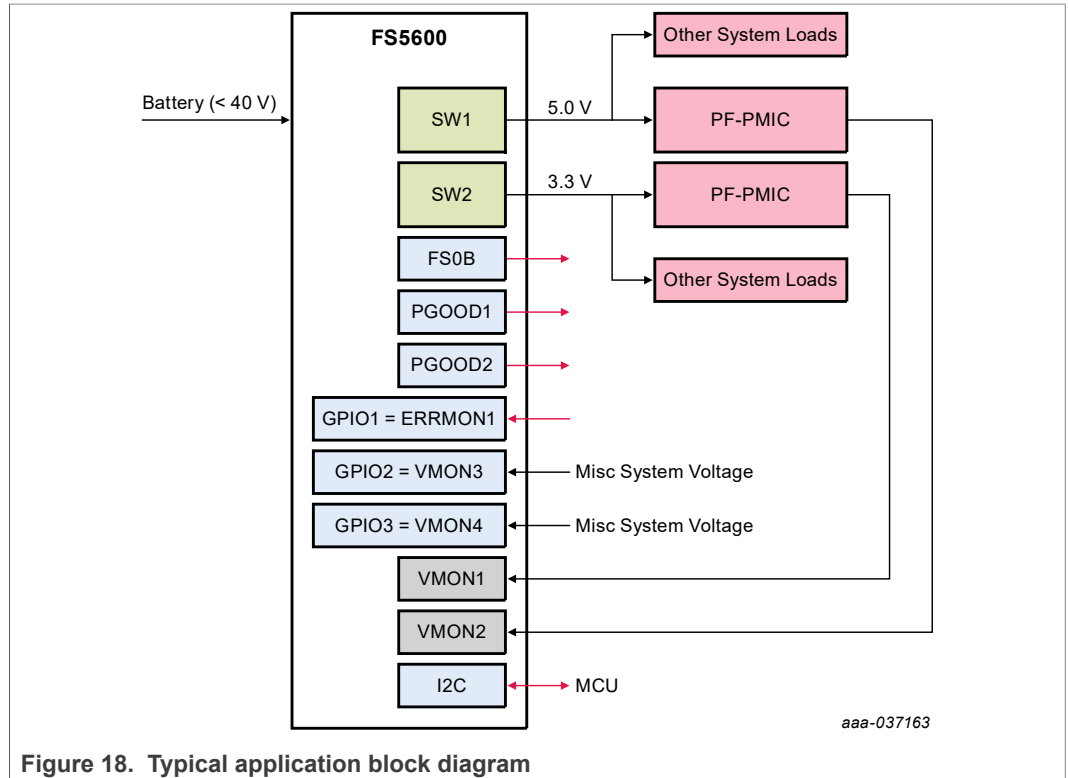
Bit	Symbol	Description
4 to 0	PMIC_FSM[4:0]	Indicates FSM State. 5b'00100 - ABIST 5b'00101 - Power Up 5b'01000 - Deep Fail-Safe 5b'01001 - INIT RUN 5b'01100 - NORMAL 5b'01101 - Thermal Shutdown 5b'10000 - Power Down 5b'10001 - POR Others - Reserved Reset Condition — POR

## 18.1.29 ID1 register

Table 84. ID1 register description

Bit	Symbol	Description
13 to 11	FULL_LAYER_REV[2:0]	Silicon revision identification
10 to 8	METAL_LAYER_REV[2:0]	Silicon revision identification
7 to 4	FAM_ID[3:0]	Family Id (1011 for FS56). 4b'1011 — Family Id (1011 for FS56). Reset Condition — POR
3 to 0	DEVICEID[3:0]	Device variation identification. Defaulted to 0.

### 19 Typical Application Block Diagram



19.1 Example power up and power down waveforms

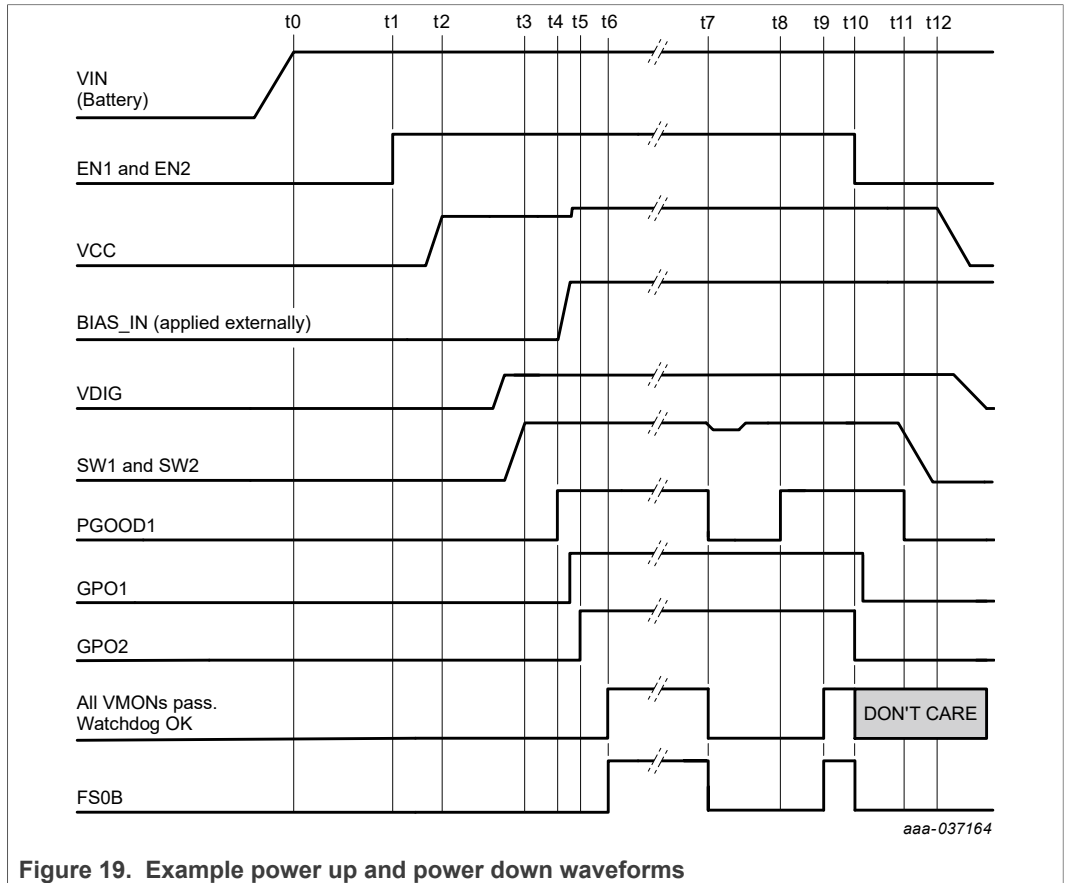


Figure 19. Example power up and power down waveforms

20 Typical Application Schematic

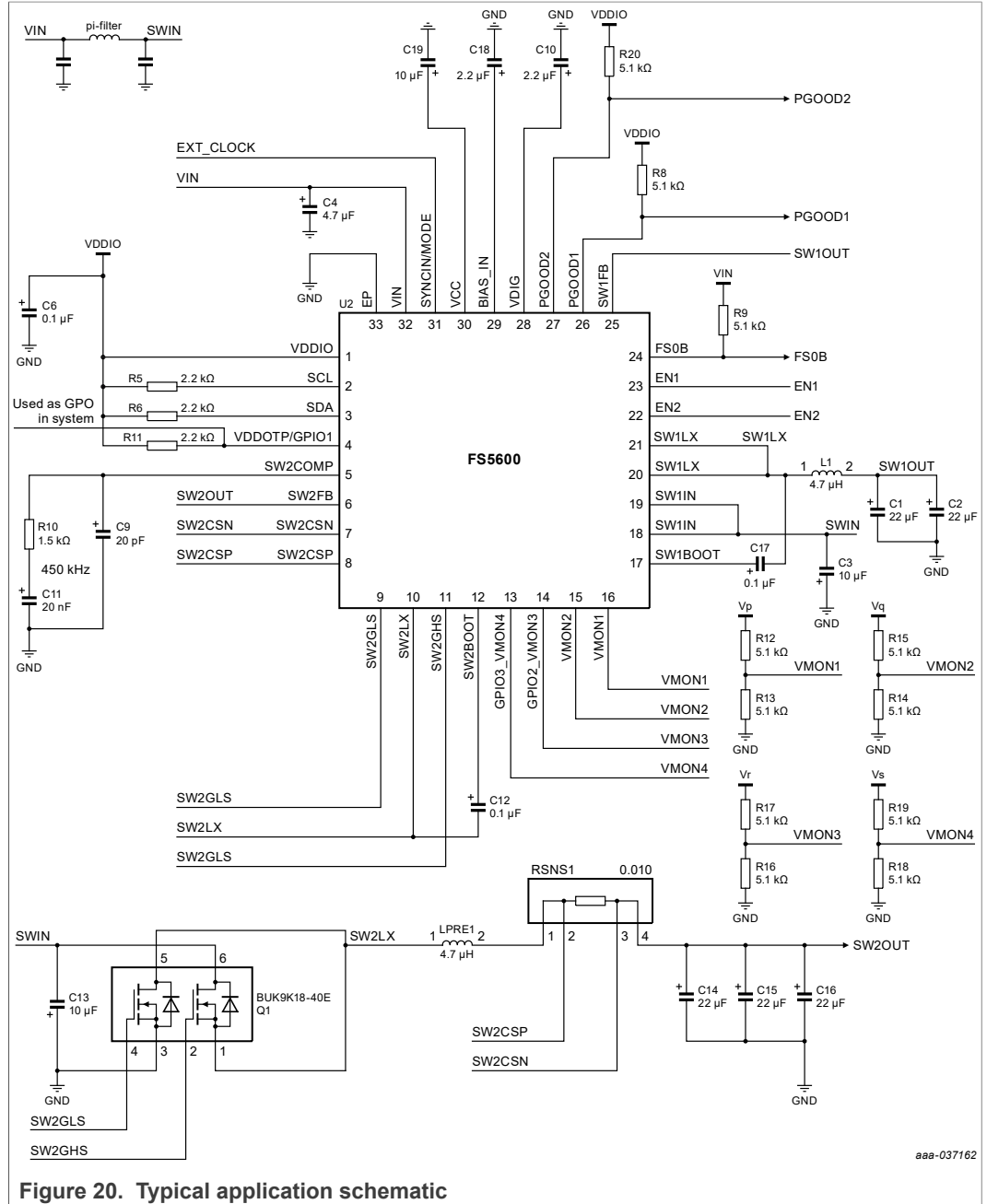
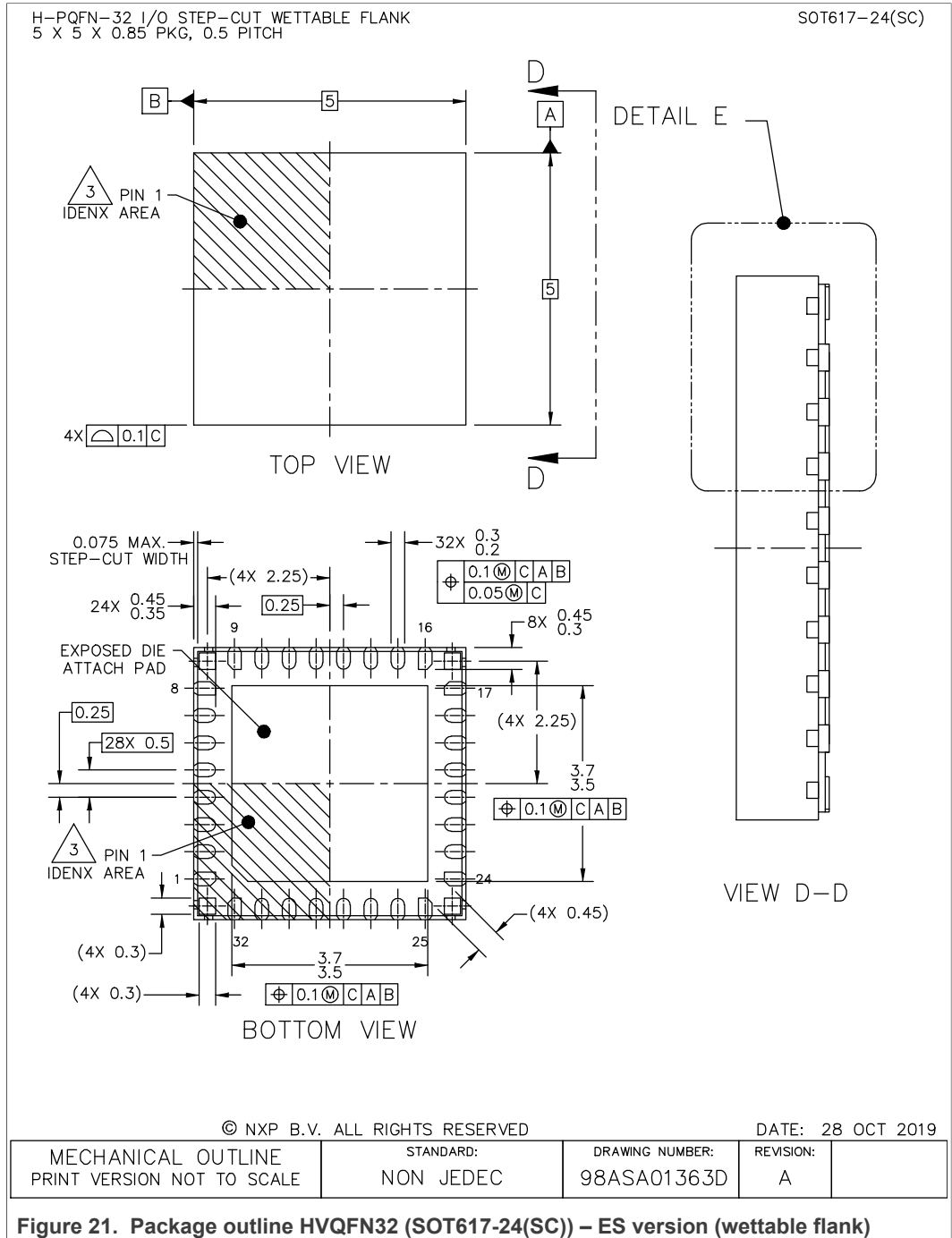


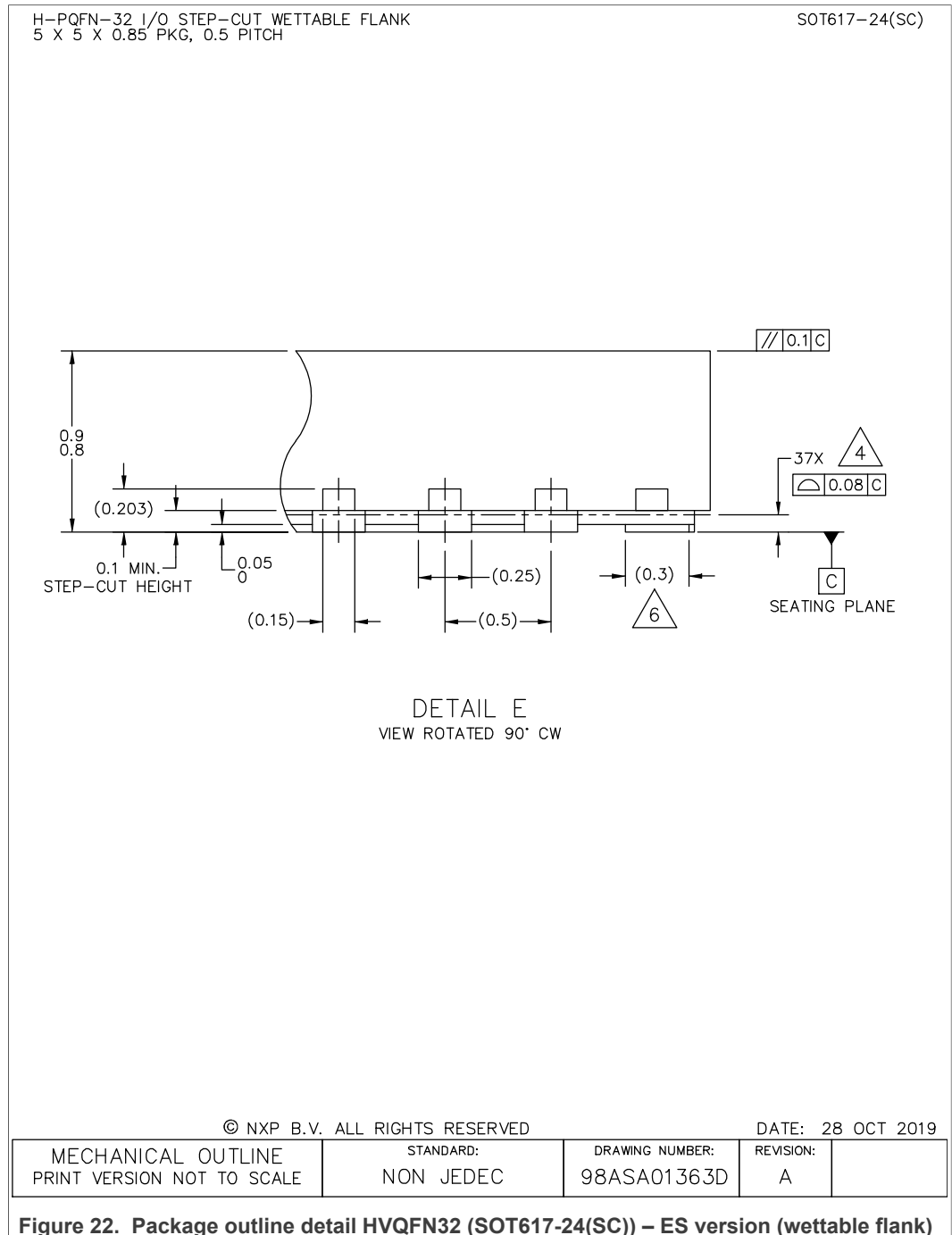
Figure 20. Typical application schematic

21 Package Outlines

21.1 Package outline – ES version (wetable flank)

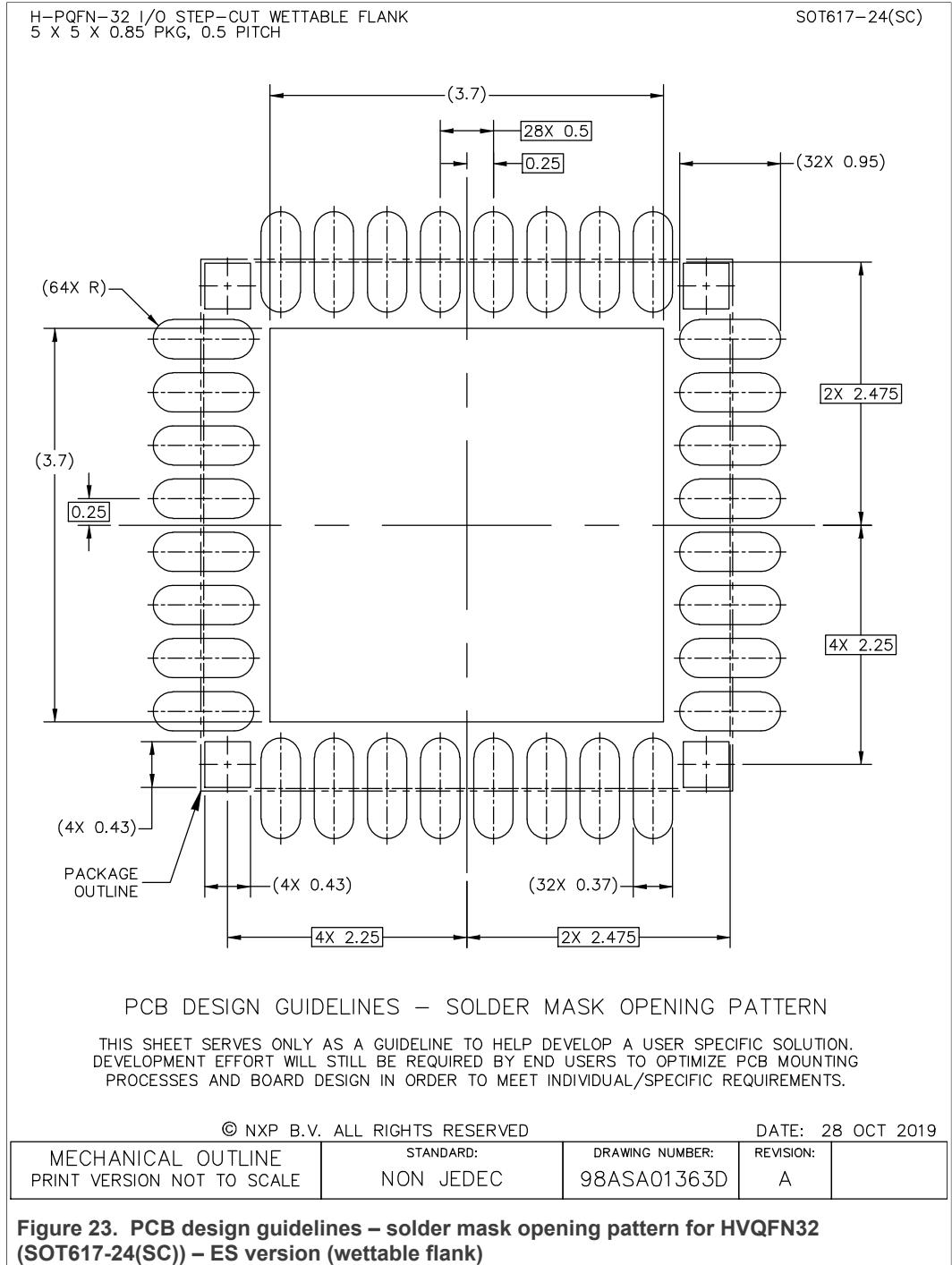


Automotive buck regulator and controller with voltage monitors and watchdog timer

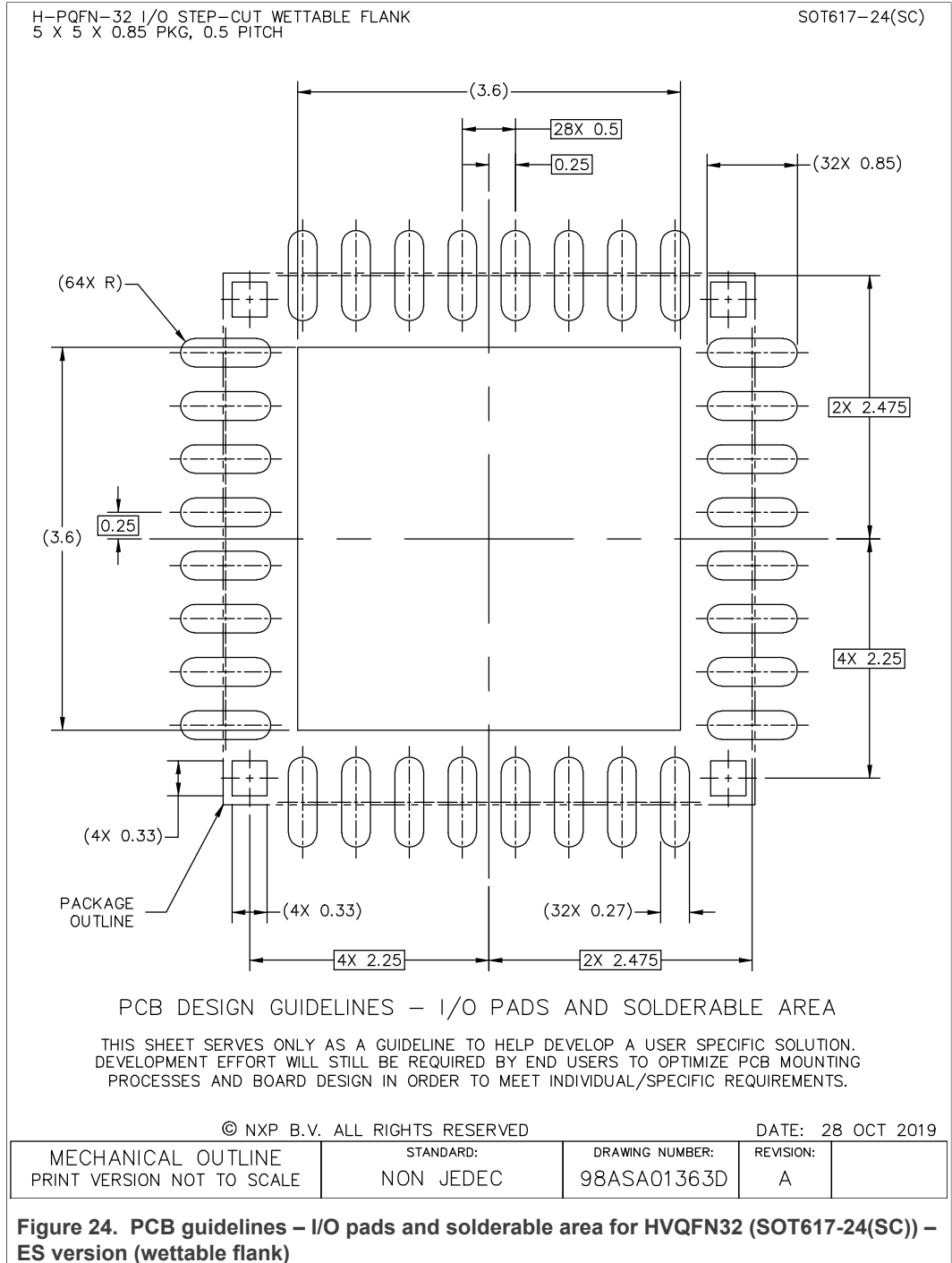




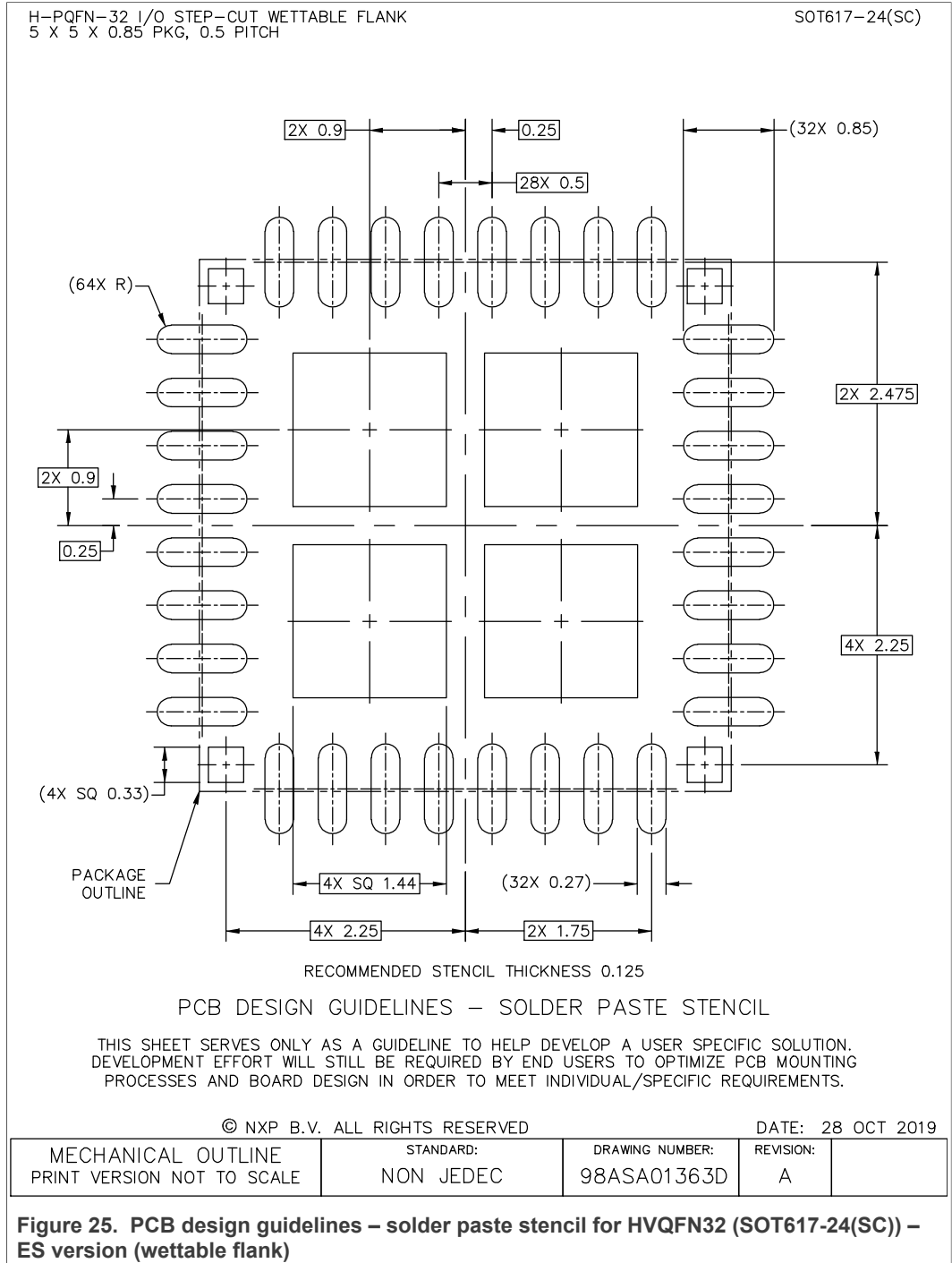
Automotive buck regulator and controller with voltage monitors and watchdog timer



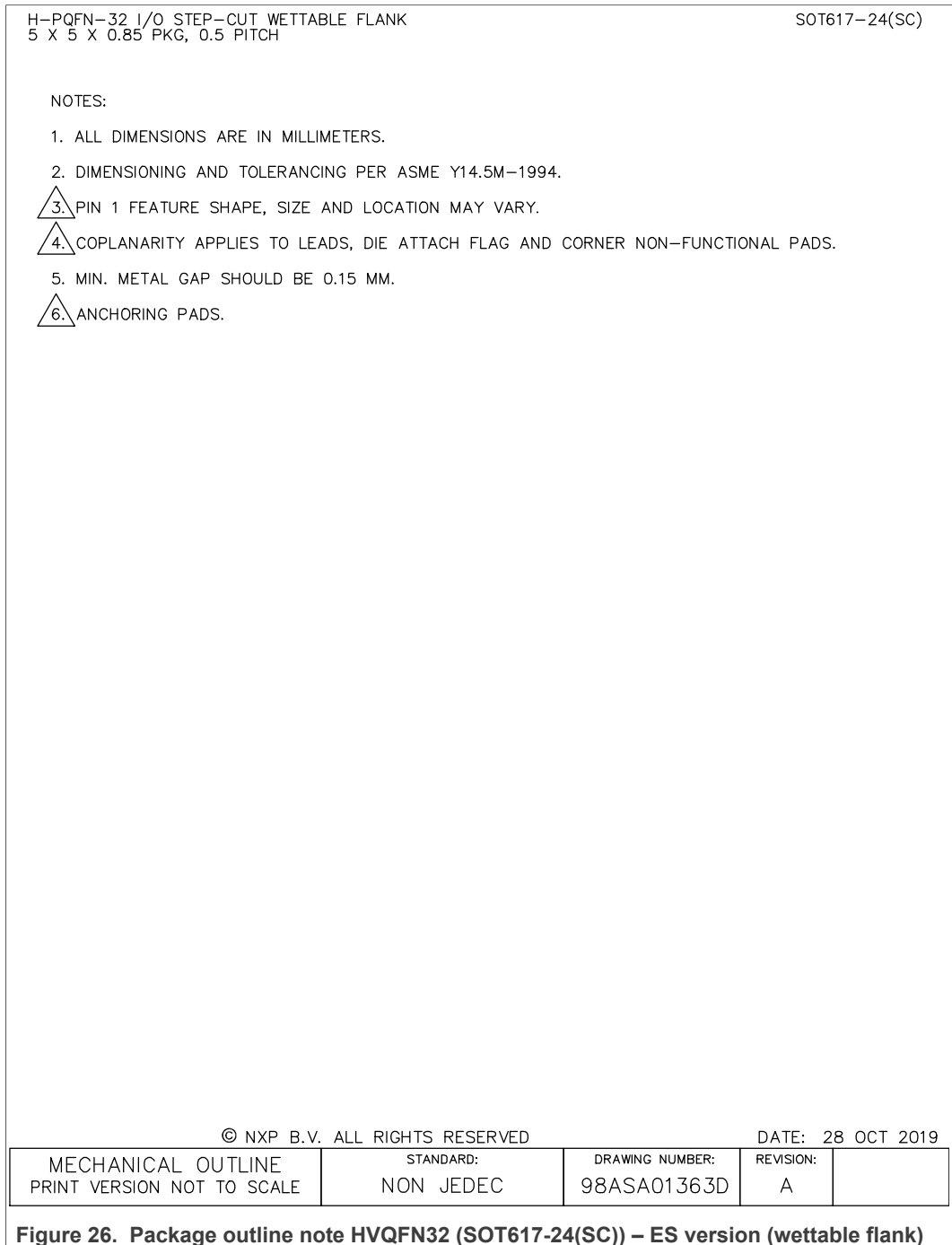
Automotive buck regulator and controller with voltage monitors and watchdog timer



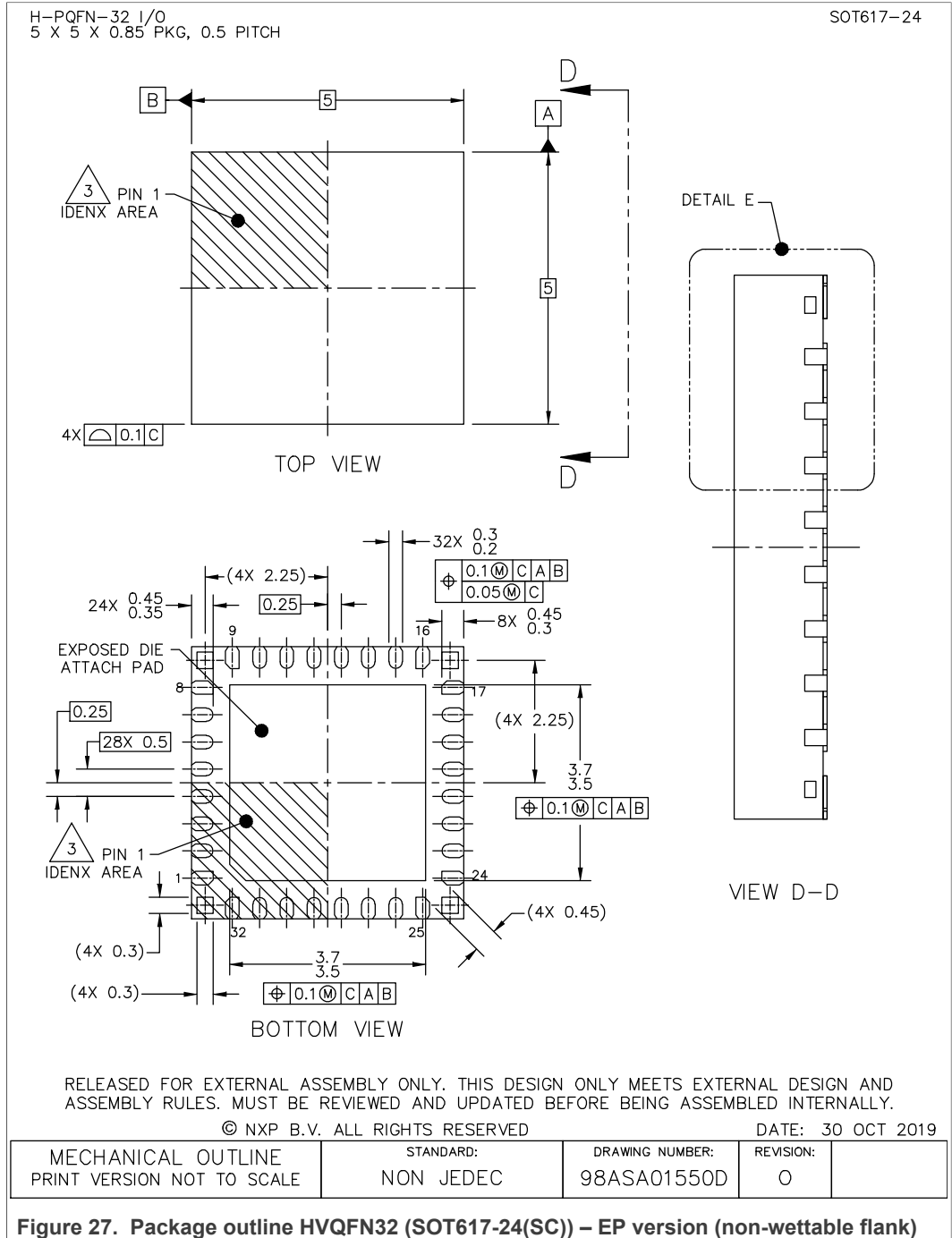
Automotive buck regulator and controller with voltage monitors and watchdog timer



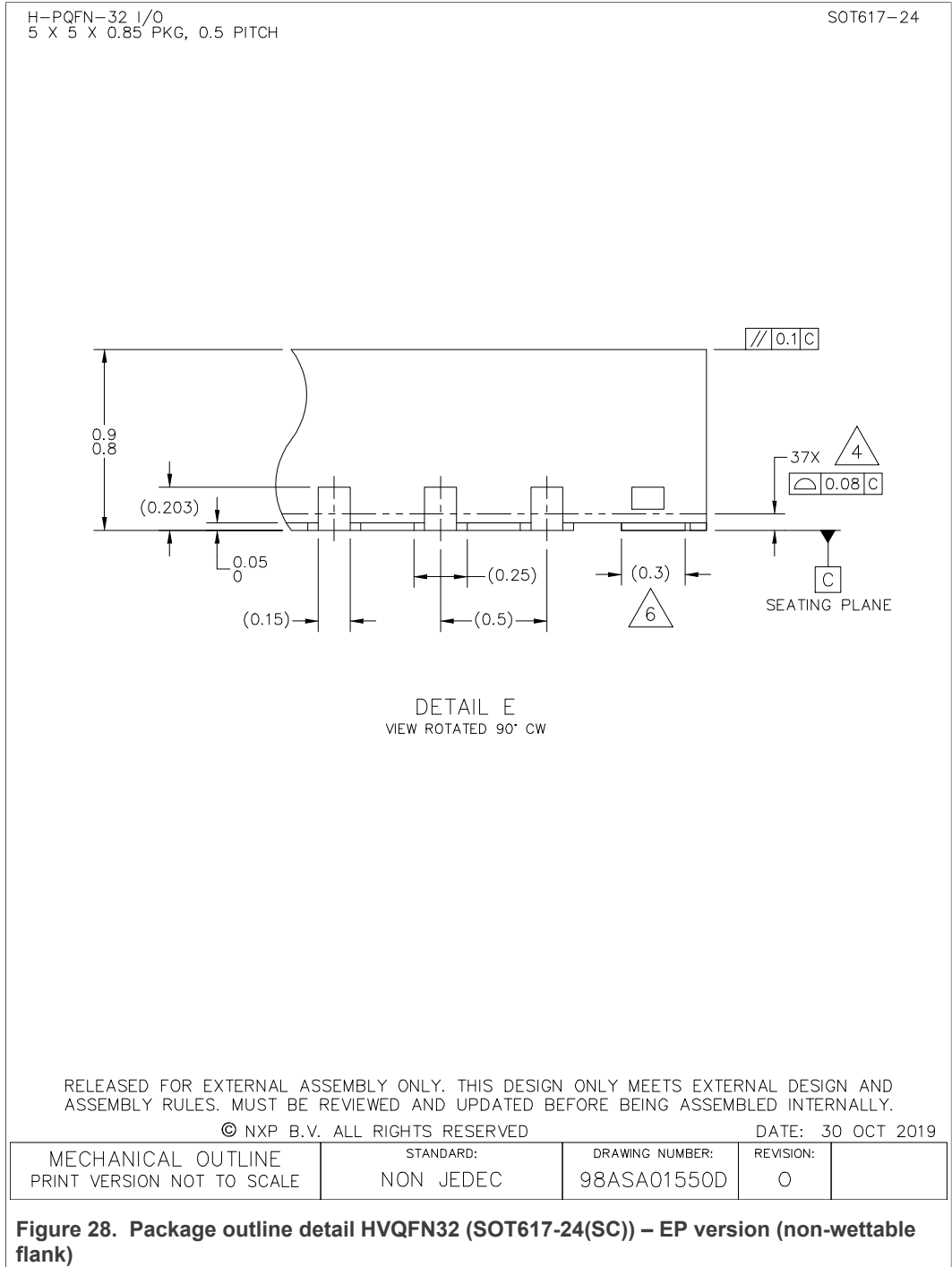
Automotive buck regulator and controller with voltage monitors and watchdog timer



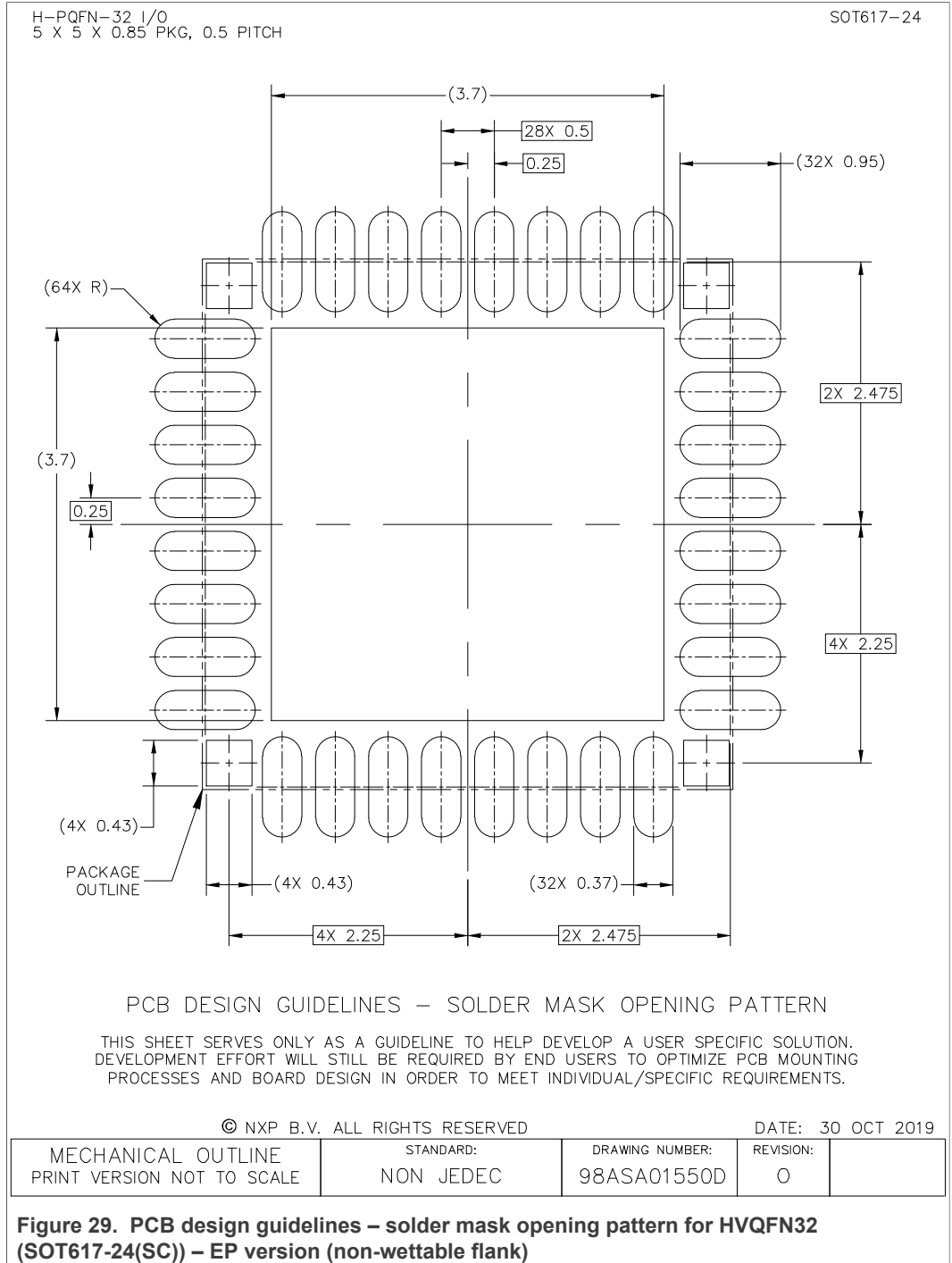
21.2 Package outlines – EP version (non-wettable flank)



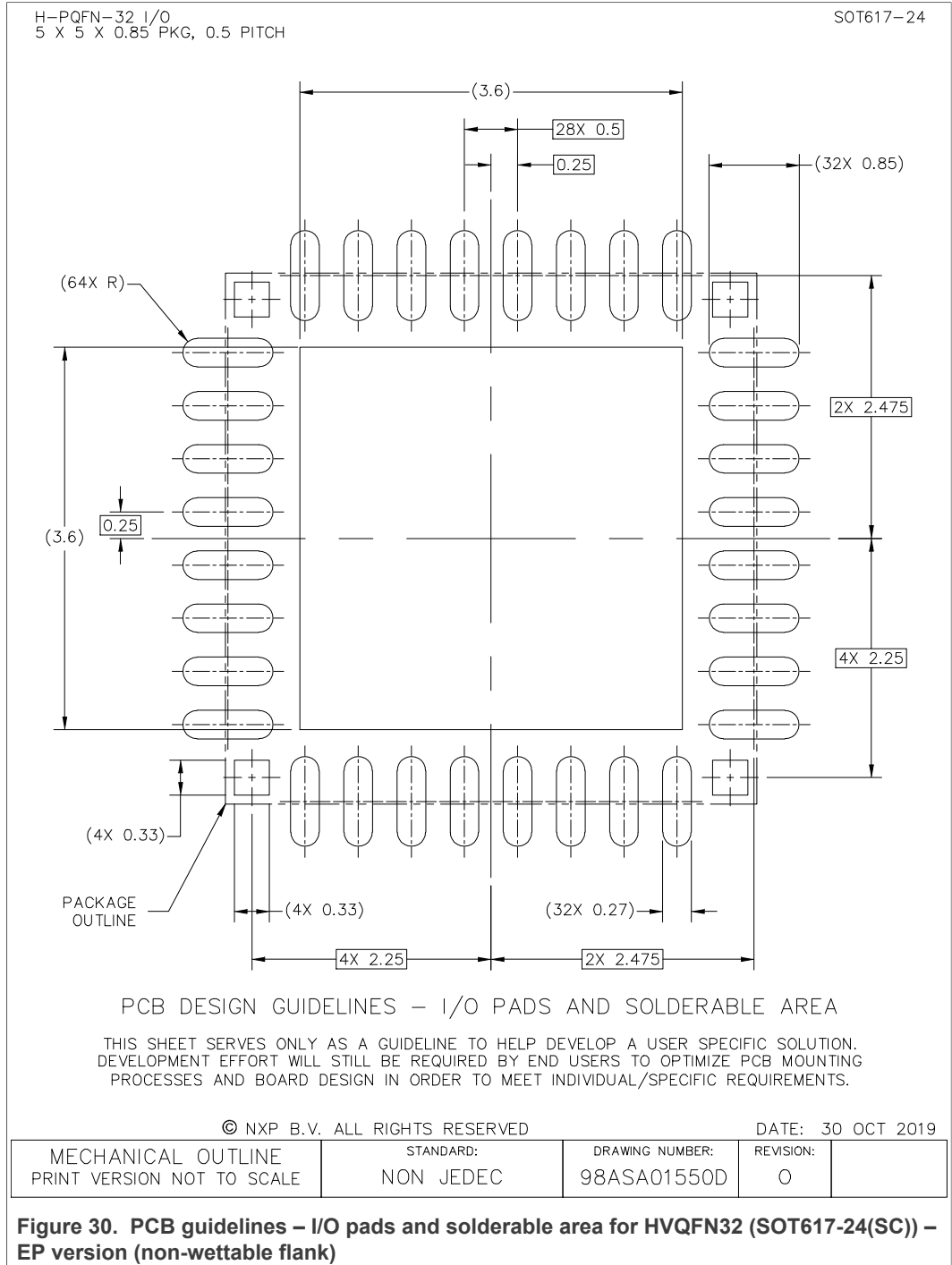
Automotive buck regulator and controller with voltage monitors and watchdog timer



Automotive buck regulator and controller with voltage monitors and watchdog timer

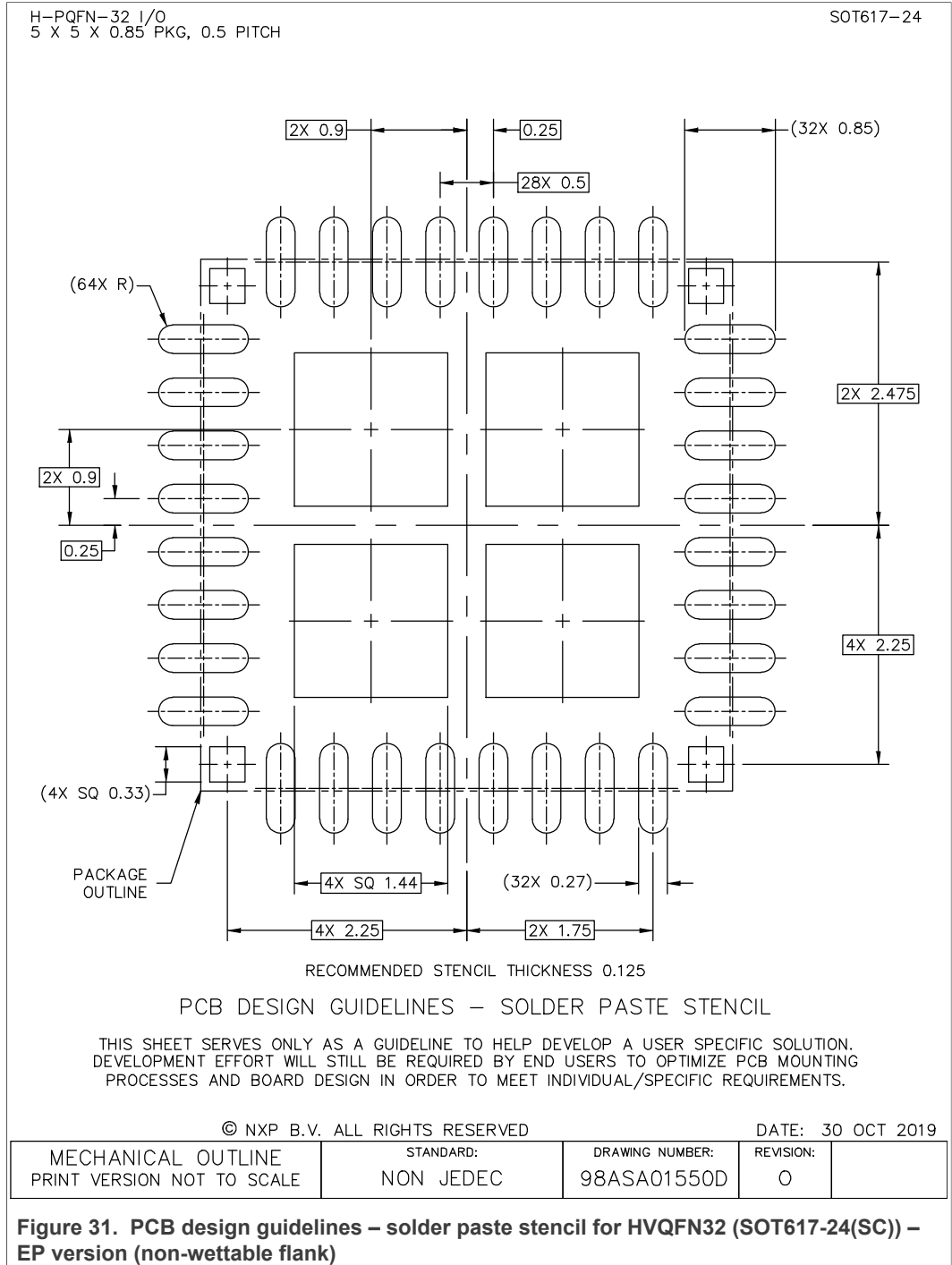


Automotive buck regulator and controller with voltage monitors and watchdog timer

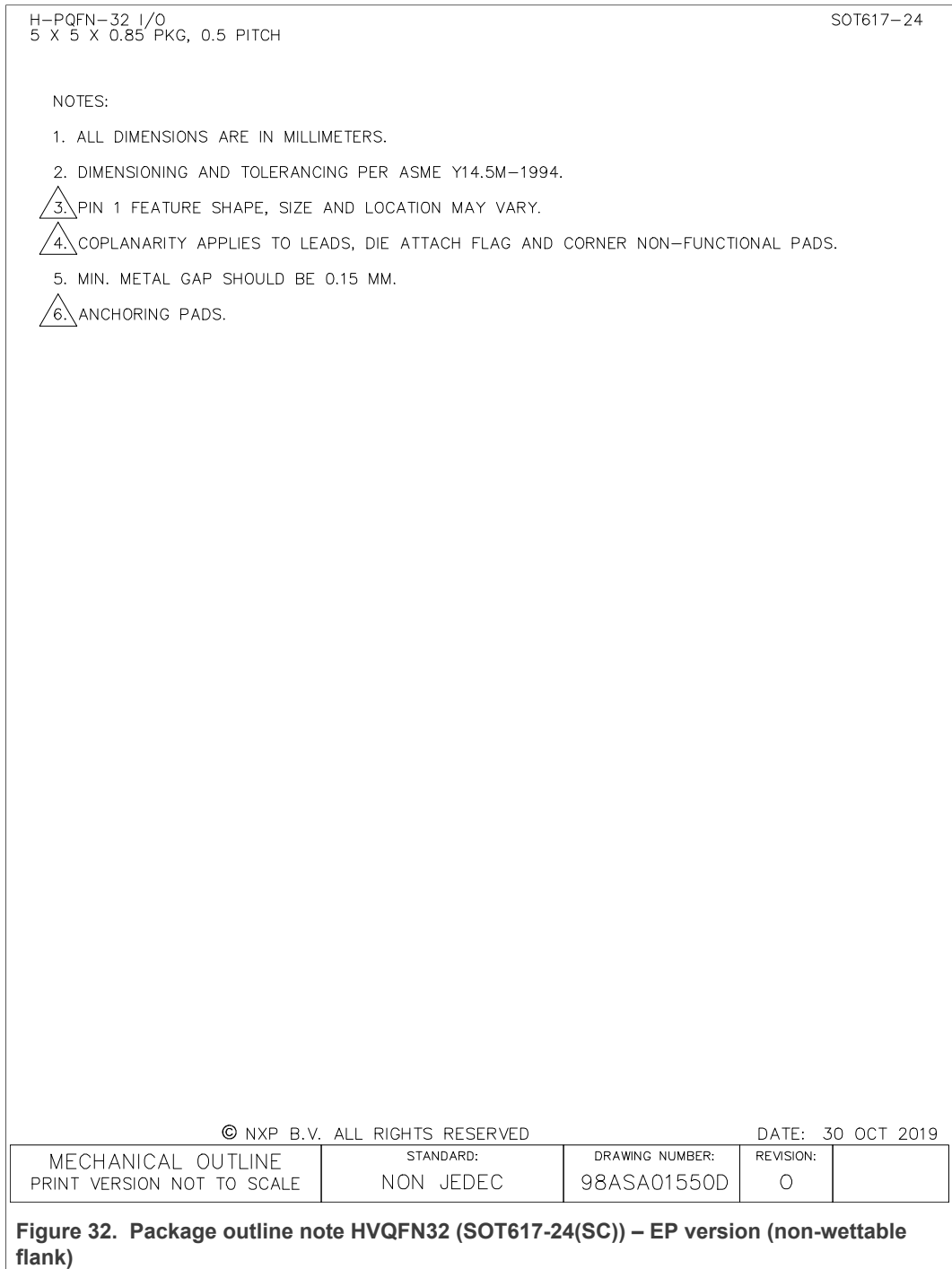




Automotive buck regulator and controller with voltage monitors and watchdog timer



Automotive buck regulator and controller with voltage monitors and watchdog timer



## 22 Revision History

Table 85. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
FS5600 v.2	20210601	Product data sheet	—	v.1
Modifications	Moved from Objective status to Product status			
FS5600 v.1	20201029	Objective data sheet	—	—
Modifications	Initial release			

## 23 Legal information

### 23.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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