# FS8600_SDS
## Fail-safe system basis chip with multiple SMPSs and LDOs
**Rev. 1.1 — 23 November 2021**          **Product short data sheet**

# 1   General description

The FS86 device family, SW compatible with FS84/85 family, expands the power capability, the safety integration and system scalability of domain controller applications to address the multiple MCU requirements present in ADAS and Electrification.

The FS86 includes multiple switch mode and linear voltage regulators and enhanced safety features with Fail-Safe outputs. The latest NXP HV Buck architecture features a 15 A capability with e-fuse protection to shut down the system power to prevent any damage in case of a harmful event. The ability to monitor ten voltages with +/-1% accuracy extends the system safety concept by allowing QM rails from others components to be monitored.

With its innovative synchronization feature, the FS86 is part of the BYLink System Power Platform, enabling a new smart approach to designing Safe System Power Management. It provides power, safety and system scalability to ease platform development strategies. Cascaded system SBC/PMICs behave as ONE with safety and sequencing synchronization.

The FS86 is part of a complete family of devices that offer scalability in power and safety, and provide pin-to-pin and software compatibility. It is developed in compliance with the ISO 26262 standard and is qualified according to AEC-Q100 requirements.

# 2   Features and benefits

**Operating Range**

- 60 V DC maximum input voltage for 24 V battery network applications
- 36 V DC maximum input voltage for 12 V battery network applications
- Support operating voltage range down to 4.5 V battery voltage with VPRE = 3.3 V
- Low Power OFF mode with low sleep current (10 μA typ.)

**Power Supplies**

- VPRE: Synchronous high voltage buck controller with external FETs
    - Configurable output voltage from 3.3 V to 5.0 V and current capability up to 15 A DC
    - Selectable switching frequency in force PWM with APS
- BOOST: Low voltage boost converter with integrated low-side FET
    - Configurable output voltage from 5 V to 6 V and current capability up to 1 A DC
- BUCK: Low voltage integrated synchronous BUCK converter
    - Configurable output voltage from 1.0 V to 3.3 V and current capability up to 2.5 A DC
- LDO1: Low voltage LDO regulator for MCU I/O and system peripheral support with load switch capability
    - Configurable output voltage from 1.5 V to 5.0 V and current capability up to 400 mA DC

- LDO2: Medium voltage LDO regulator for MCU I/O and system peripheral support
  - Configurable output voltage from 1.1 V to 5.0 V and current capability up to 400 mA DC

**System support**

- 2x input pins for wake-up detection, 3.3 V compatible and battery voltage sensing capability
- Analog Multiplexer with full System Voltages monitoring
- Enhanced leader/follower power up sequencing management thru XFAILB pin
- 10 ms optional RSTB release delay during power up for certain MCU compliancy
- Device control via 32 bits I2C interface with 8-bit CRC

**Compliancy**

- EMC optimization techniques on switching regulators including spread spectrum, slew rate control and manual frequency tuning
- EMI robustness supporting various automotive EMI Test standards
- Conducted Emission: IEC 61967-4
- Conducted Immunity: IEC 62132-4
- Radiated emission: FMC1278 rev. 3 from 2018
- Radiated immunity: FMC1278 from 2018 and ISO11452-4

**Functional Safety**

- Scalable portfolio to fit for ASIL B to ASIL D Automotive Safety Systems
- Independent voltage Monitoring Circuitry
- Up to 10 voltage monitoring input for FS86 and external PMIC voltage rails with 1 % target accuracy
- Dedicated interface for MCU monitoring with simple or challenger watchdog monitoring
- MCU hardware failure monitoring with PWM monitoring capability
- External IC failure monitoring
- Logical and Analog Built-in Self-Test
- Safety Outputs with latent fault detection mechanism (PGOOD, RSTB, FS0B)

**Configuration and Enablement**

- QFN 48 pins with exposed pad for optimized thermal management
- OTP programming for device customization

## 3   Applications

- Domain controller (ADAS, electrification, Infotainment, etc.)
- Radar (radar, imaging radar)
- Vision (mono camera, stereo camera, night vision, etc.)
- 24 V battery network (60 V maximum): Truck, bus, transportation
- 12 V battery network (36 V maximum): Automotive
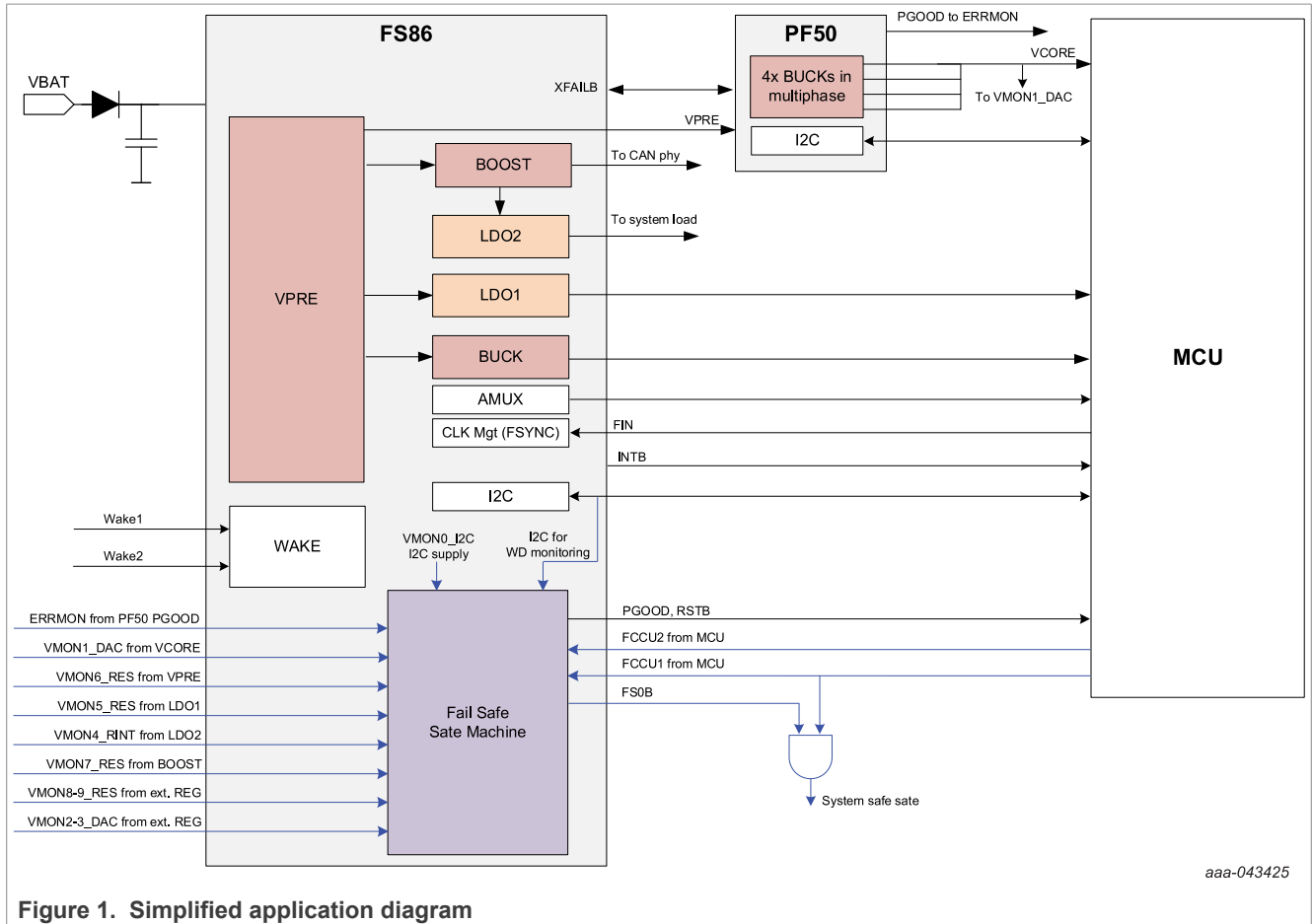
# 4 Simplified Application Diagram



**Figure 1. Simplified application diagram**

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# 5 Ordering information

## 5.1 Device family

FS8600 device family (called FS86 hereafter) provides selectable features based on part numbering and OTP configuration.

**Table 1. Device options**

| FS + Core ID | App-lication | VSUP max rating | VPRE | VBOOST | BUCK | LDOs | VMONs | Watchdog | FCCU | ERRMON | FIN |
|---|---|---|---|---|---|---|---|---|---|---|---|
| FS8600 | | 60 V | Yes | Yes | No | 2 | 4 | Yes[1] | Yes | Yes | Yes |
| FS8601 | | 60 V | Yes | Yes | No | 2 | 6 | | Yes | Yes | Yes |
| FS8602 | | 60 V | Yes | Yes | No | 2 | 8 | | Yes | Yes | Yes |
| FS8603 | 24 V battery network | 60 V | Yes | Yes | No | 2 | 10 | | Yes | Yes | No[2] |
| FS8610 | | 60 V | Yes | Yes | Yes | 2 | 4 | | Yes | Yes | Yes |
| FS8611 | | 60 V | Yes | Yes | Yes | 2 | 6 | | Yes | Yes | Yes |
| FS8612 | | 60 V | Yes | Yes | Yes | 2 | 8 | | Yes | Yes | Yes |
| FS8613 | | 60 V | Yes | Yes | Yes | 2 | 10 | | Yes | Yes | No[2] |
| FS8620 | | 36 V | Yes | Yes | No | 2 | 4 | | Yes | Yes | Yes |
| FS8621 | | 36 V | Yes | Yes | No | 2 | 6 | | Yes | Yes | Yes |
| FS8622 | | 36 V | Yes | Yes | No | 2 | 8 | | Yes | Yes | Yes |
| FS8623 | 12 V battery network | 36 V | Yes | Yes | No | 2 | 10 | | Yes | Yes | No[2] |
| FS8630 | | 36 V | Yes | Yes | Yes | 2 | 4 | | Yes | Yes | Yes |
| FS8631 | | 36 V | Yes | Yes | Yes | 2 | 6 | | Yes | Yes | Yes |
| FS8632 | | 36 V | Yes | Yes | Yes | 2 | 8 | | Yes | Yes | Yes |
| FS8633 | | 36 V | Yes | Yes | Yes | 2 | 10 | | Yes | Yes | No[2] |

[1] ASIL B: Watchdog Simple. ASIL D: Watchdog Challenger.
[2] FIN input shared with VMON9 input

## 5.2 Part numbering

| M | FS | 8600 | B | M | B | A0 | ES |
|---|---|---|---|---|---|---|---|
| P: prototype M: standard S: custom | HV PMIC | FS86 Core ID[1] | Silicon revision A: A0 B: A1 | Ambient temperature ($T_A$) M: –40 °C to 125 °C | ASIL B: ASIL B D: ASIL D | OTP code A0: OTP A0 xx: OTP xx | Package type ES: dimple wettable flank |

[1] See Table 1

**Table 2. Ordering information**

| Part Number[1] | Application | ASIL | Package | | |
|---|---|---|---|---|---|
| | | | Name | Description | Version |
| MFS8600BMBA0ES[2] | 24 V battery network | B | HPQFN48eP | HPQFN48, plastic, thermally enhanced very thin quad flat package, no lead, wettable flanks | SOT619-26 |
| MFS8601BMBA0ES[2] | | | | | |
| MFS8602BMBA0ES[2] | | | | | |
| MFS8603BMBA0ES[2] | | | | | |

**Table 2. Ordering information**...*continued*

| Part Number[1] | Application | ASIL | Package | | |
|---|---|---|---|---|---|
| | | | Name | Description | Version |
| **MFS8610BMBA0ES**[2] | | | | | |
| **MFS8611BMBA0ES**[2] | | | | | |
| **MFS8612BMBA0ES**[2] | | | | | |
| **MFS8613BMBA0ES**[2] | | | | | |
| **MFS8600BMDA0ES**[2] | | D | | | |
| **MFS8601BMDA0ES**[2] | | | | | |
| **MFS8602BMDA0ES**[2] | | | | | |
| **MFS8603BMDA0ES**[2] | | | | | |
| **MFS8610BMDA0ES**[2] | | | | | |
| **MFS8611BMDA0ES**[2] | | | | | |
| **MFS8612BMDA0ES**[2] | | | | | |
| **MFS8613BMDA0ES**[2] | | | | | |
| **MFS8620BMBA0ES**[2] | 12 V battery network | B | | | |
| **MFS8621BMBA0ES**[2] | | | | | |
| **MFS8622BMBA0ES**[2] | | | | | |
| **MFS8623BMBA0ES**[2] | | | | | |
| **MFS8630BMBA0ES**[2] | | | | | |
| **MFS8631BMBA0ES**[2] | | | | | |
| **MFS8632BMBA0ES**[2] | | | | | |
| **MFS8633BMBA0ES**[2] | | | | | |
| **MFS8620BMDA0ES**[2] | | D | | | |
| **MFS8621BMDA0ES** [2] | | | | | |
| **MFS8622BMDA0ES**[2] | | | | | |
| **MFS8623BMDA0ES**[2] | | | | | |
| **MFS8630BMDA0ES**[2] | | | | | |
| **MFS8631BMDA0ES**[2] | | | | | |
| **MFS8632BMDA0ES**[2] | | | | | |
| **MFS8633BMDA0ES**[2] | | | | | |
| **PFS8613AMDA0ES**[3] | 12 V or 24 V battery network | B or D | | | |
| **PFS8613BMDA0ES**[4] | | | | | |

[1]  To order parts in tape and reel, add the R2 suffix to the part number.
[2]  Production part number available only after product qualification (A1 silicon pass).
[3]  Superset part number that can cover all features for prototype ordering (A0 silicon pass/obsolete)..
[4]  Superset part number that can cover all features for prototype ordering (A1 silicon pass).

Part numbers ending with A0 OTP code are non-programmed OTP configuration. Pre-programmed OTP configurations are managed through part number extension. For a custom OTP configuration, please contact your local NXP sales representative.

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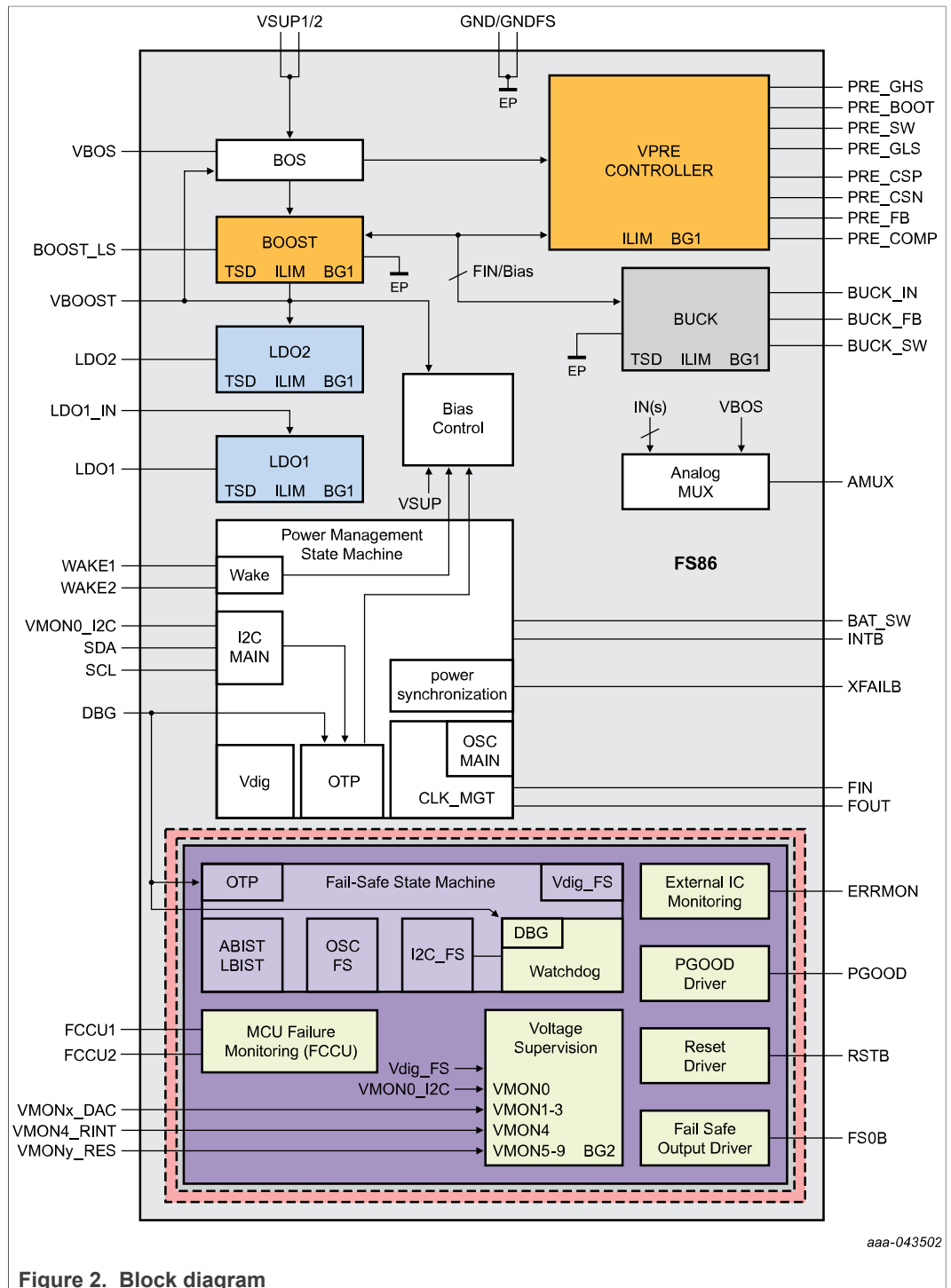All information provided in this document is subject to legal disclaimers.

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# 6    Internal block diagram



**Figure 2.  Block diagram**

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# 7 Pinout information

## 7.1 Pinout
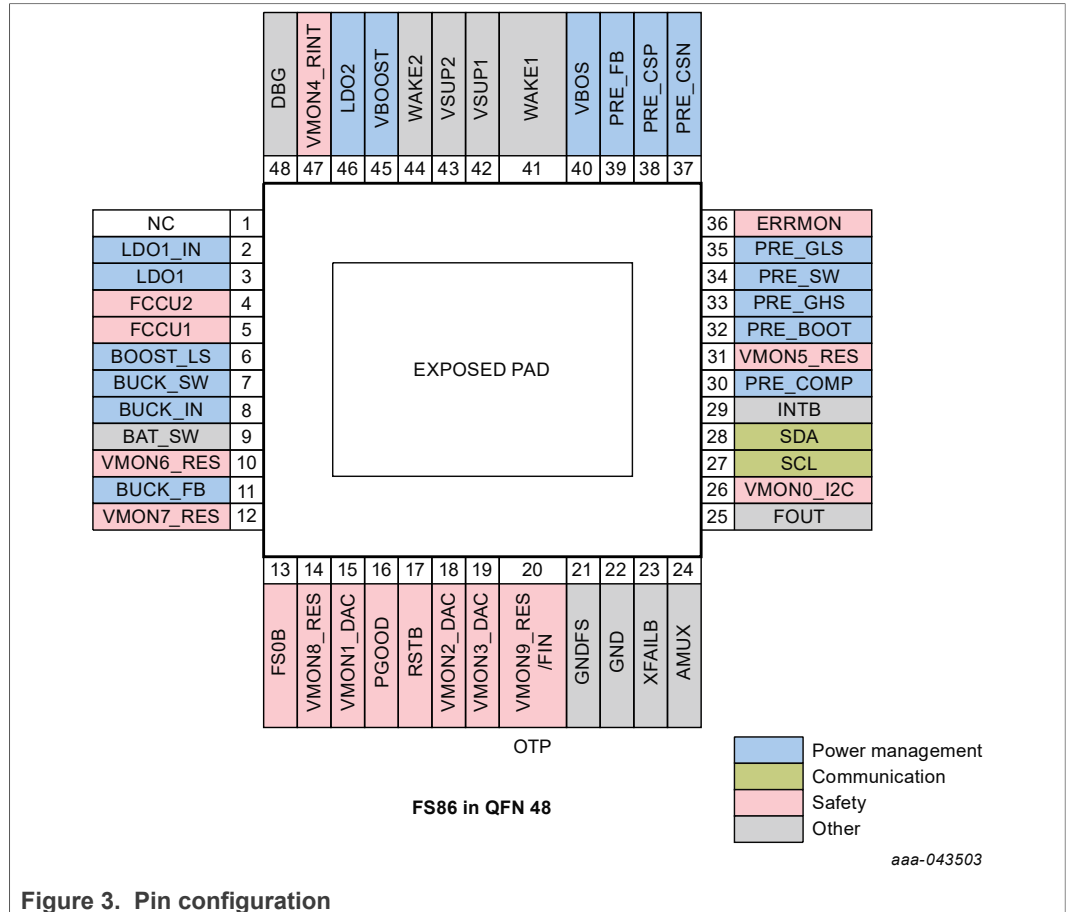


**Figure 3. Pin configuration**

## 7.2 Pin description

**Table 3. Pin description**

| Pin | Name | Type | Description |
|---|---|---|---|
| 1 | N/C | N/C | Not connected pin |
| 2 | LDO1_IN | Analog input | Linear regulator #1 input voltage |
| 3 | LDO1 | Analog output | Linear regulator #1 output voltage |
| 4 | FCCU2 | Digital input | MCU Error Monitoring input 2 |
| 5 | FCCU1 | Digital input | MCU Error Monitoring input 1 |
| 6 | BOOST_LS | Analog input | BOOST Low Side Drain of internal MOSFET |
| 7 | BUCK_SW | Analog output | Low Voltage Buck switching node |
| 8 | BUCK_IN | Analog input | Low Voltage Buck input voltage |
| 9 | BAT_SW | Digital output | Battery switch control output. Active Low. Open drain structure. |
| 10 | VMON6_RES | Analog input | External resistor bridge voltage monitoring input #6 |

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**Table 3. Pin description**...*continued*

| Pin | Name | Type | Description |
|-----|------|------|-------------|
| 11 | BUCK_FB | Analog input | Low Voltage Buck voltage feedback. |
| 12 | VMON7_RES | Analog input | External resistor bridge voltage monitoring input #7 |
| 13 | FS0B | Digital output | Fail Safe Output 0. Active Low. Open drain structure. |
| 14 | VMON8_RES | Analog input | External resistor bridge voltage monitoring input #8 |
| 15 | VMON1_DAC | Analog input | DAC voltage monitoring input #1 |
| 16 | PGOOD | Digital output | Power good output |
| 17 | RSTB | Digital input/output | Reset output. Active Low. The main function is to reset the MCU. Reset input voltage is monitored in order to detected external reset and fault condition |
| 18 | VMON2_DAC | Analog input | DAC voltage monitoring input #2 |
| 19 | VMON3_DAC | Analog input | DAC voltage monitoring input #3 |
| 20 | VMON9_RES | Analog input | External resistor bridge voltage monitoring input #9. Exclusive with FIN (OTP) |
| 20 | FIN | Digital input | Frequency synchronization input. Exclusive with VMON9_RES (OTP) |
| 21 | GNDFS | Ground | Fail Safe ground |
| 22 | GND | Ground | Main ground |
| 23 | XFAILB | Digital input/output | Power Synchronization input/output with NXP low voltage PMIC |
| 24 | AMUX | Analog output | Multiplexed output to be connected to an MCU ADC with selection of the analog parameter thru I2C. |
| 25 | FOUT | Digital output | Frequency synchronization output or digital output (OTP) |
| 26 | VMON0_I2C | Analog input | Input voltage for FIN, AMUX, I2C, INTB, FCCU, ERRMON. Internal resistor bridge voltage monitoring input #0 |
| 27 | SCL | Digital input | I2C Bus. Clock input |
| 28 | SDA | Digital input/output | I2C Bus. Bidirectional data line |
| 29 | INTB | Digital output | Interrupt output |
| 30 | PRE_COMP | Analog input | VPRE compensation network and negative current sense input |
| 31 | VMON5_RES | Analog input | External resistor bridge voltage monitoring input #5 |
| 32 | PRE_BOOT | Analog input/output | VPRE bootstrap capacitor |
| 33 | PRE_GHS | Analog output | VPRE High Side gate driver for external MOSFET |
| 34 | PRE_SW | Analog output | VPRE switching node |
| 35 | PRE_GLS | Analog output | VPRE Low Side gate driver for external MOSFET |
| 36 | ERRMON | Digital input | External IC error monitoring input |
| 37 | PRE_CSN | Analog input | VPRE negative current sense input |
| 38 | PRE_CSP | Analog input | VPRE positive current sense input |
| 39 | PRE_FB | Analog input | VPRE voltage feedback. |
| 40 | VBOS | Analog output | Best of supply output voltage |
| 41 | WAKE1 | Digital/Analog input | Wake up input 1 (thru ext. serial resistor) |

**Table 3.  Pin description**...*continued*

| Pin | Name | Type | Description |
|---|---|---|---|
| 42 | VSUP1 | Power Analog Input | Power supply of the device #1.<br>An external reverse battery protection diode in series is mandatory |
| 43 | VSUP2 | Power Analog Input | Power supply of the device #2.<br>An external reverse battery protection diode in series is mandatory |
| 44 | WAKE2 | Digital/Analog input | Wake up input 2 (thru ext. serial resistor) |
| 45 | VBOOST | Analog output | Boost output voltage |
| 46 | LDO2 | Analog output | Linear regulator #2 output voltage |
| 47 | VMON4_RINT | Analog input | Internal resistor bridge voltage monitoring input #4 |
| 48 | DBG | Analog input | DEBUG Mode entry and OTP input supply |
| EP | EP | Ground | Expose pad must be connected to GND |

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# 8   Maximum ratings

**Table 4. Maximum ratings**

*All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.*

| Symbol | Conditions | Parameter | Min | Max | Unit |
|---|---|---|---|---|---|
| **Voltage ratings of 24 V network application part numbers (see Table 2)** | | | | | |
| VSUP1/2 | DC Voltage | VSUP1,2 pins | −0.3 | 60 | V |
| WAKE1/2 | DC Voltage | WAKE1,2 pins (external series resistor mandatory) | −1.0 | 60 | V |
| FS0B | DC Voltage | FS0B pin | −0.3 | 60 | V |
| BAT_SW | DC Voltage | BAT_SW pin | −0.3 | 60 | V |
| PRE_SW | DC Voltage | PRE_SW pin | −2.0 | 60 | V |
| | Transient voltage < 20 ns | | −3.0 | 60 | |
| PRE_GHS, PRE_BOOT | DC Voltage | PRE_GHS, PRE_BOOT pins | −0.3 | 65.5V | V |
| **Voltage ratings of 12 V network application part numbers (see Table 2)** | | | | | |
| VSUP1/2 | DC Voltage | VSUP1,2 pins | −0.3 | 36 | V |
| WAKE1/2 | DC Voltage | WAKE1,2 pins (external series resistor mandatory) | −1.0 | 36 | V |
| FS0B | DC Voltage | FS0B pin | −0.3 | 36 | V |
| BAT_SW | DC Voltage | BAT_SW pin | −0.3 | 36 | V |
| PRE_SW | DC Voltage | PRE_SW pin | −2.0 | 36 | V |
| | Transient voltage < 20 ns | | −3.0 | 36 | |
| PRE_GHS, PRE_BOOT | DC Voltage | PRE_GHS, PRE_BOOT pins | −0.3 | 41.5 V | V |
| **Voltage ratings of general pins** | | | | | |
| BOOST_LS | DC Voltage | BOOST_LS pin | −0.3 | 8.5 | V |
| VBOOST | DC Voltage | VBOOST pin | −0.3 | 6.5 | V |
| BUCK_IN | DC Voltage | BUCK_IN pin | −1.0 | 5.5 | V |
| | Transient voltage < 3 µs | | −1.0 | 6.5 | |
| BUCK_SW | Transient voltage < 20 ns | BUCK_SW pin | −0.3 | 6.5 | V |
| VMONx | DC Voltage | VMON_DAC 1-3, VMON_RES 5-9 | −0.3 | 36 | V |
| DBG | DC Voltage | DBG pin | −0.3 | 10 | V |
| All other pins | DC Voltage | at all other pins | −0.3 | 5.5 | V |

## 9 Electrostatic discharge

### 9.1 Human body model (JESD22/A114)

The device is protected up to ±2 kV, according to the human body model standard with 100 pF and 1.5 kΩ. This protection is ensured at all pins.

### 9.2 Charged device model

The device is protected up to ±750 V on corner pins and up to ±500 V on all other pins, according to the AEC Q100 - 011 charged device model standard.

### 9.3 Discharged contact test

The device is protected up to ±8 kV, according to the following discharged contact tests.

- Discharged contact test (IEC61000-4-2) at 150 pF and 330 Ω
- Discharged contact test (ISO10605.2008) at 150 pF and 2 kΩ
- Discharged contact test (ISO10605.2008) at 330 pF and 2 kΩ

This protection is ensured at VSUP1, VSUP2, WAKE1, WAKE2, FS0B pins.

## 10 Thermal ratings

**Table 5. Thermal ratings**

| Symbol | Description (Rating) | Min | Max | Unit |
|---|---|---|---|---|
| **Thermal ratings** | | | | |
| $T_A$ | Ambient Temperature (Grade 1) | −40 | 125 | °C |
| $T_J$ | Junction Temperature (Grade 1) | −40 | 150 | °C |
| $T_{STG}$ | Storage Temperature | −55 | 150 | °C |
| **Thermal resistance** (per JEDEC JESD51-2 and JESD51-8) | | | | |
| $R_{\theta JA}$ | Thermal Resistance Junction to Ambient (2s2p) | — | 31 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance Junction to Ambient (2s6p) | — | 23 | °C/W |
| $R_{\theta JB}$ | Thermal Resistance Junction to Board (2s2p) | — | 15 | °C/W |
| $R_{\theta JB}$ | Thermal Resistance Junction to Board (2s6p) | — | 10 | °C/W |
| $R_{\theta JC\_BOT}$ | Thermal Resistance Junction to Case Bottom (between the die and the solder pad on the bottom of the package) | — | 1 | °C/W |
| $R_{\theta JP\_TOP}$ | Thermal Resistance Junction to Package Top (between package top and the junction temperature) | — | 3 | °C/W |

## 11 Revision History

**Table 6. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| FS8600_SDS v.1.1 | 20211123 | Product | — | — |
| Modifications: | • Initial Release | | | |

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| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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## Tables

## Figures

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