MIC23099 Evaluation Board

Single AA/AAA Cell Step-Up/Step-Down Regulators with Battery Monitoring

General Description

The MIC23099 is a high-efficiency, low-noise, dual-output, integrated power-management solution for single-cell alkaline or NiMH battery applications. The synchronous boost output voltage (V_{OUT1}) is enabled first and is powered from the battery. Next, the synchronous buck output (V_{OUT2}) – which is powered from the boost output voltage – is enabled. This configuration allows V_{OUT2} to be independent of battery voltage, thereby allowing the buck output voltage to be higher or lower than the battery voltage.

To minimize switching artifacts in the audio band, both the converters are design to operate with a minimum switching frequency of 80kHz for the buck and 100kHz for the boost. The high current boost has a maximum switching frequency of 1MHz, minimizing the solution foot-print.

The MIC23099 incorporates both battery-management functions and fault protection. The low-battery level is indicated by an external LED connected to the LED pin. In addition, a supervisory circuit monitors each output and asserts a power-good (PG) signal when the sequencing is done or de-asserted when a fault condition occurs.

The basic parameters of the evaluation board are:

- Input: 0.85V to 1.6V
- Output 1: 1.8V/0.2A
- Output 2: 1.0V/30mA

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Requirements

The MIC23099 evaluation board requires only a single power supply with at least 1A current capability. The output load can either be an active (electronic) or passive (resistive) load.

Precautions

The MIC23099 evaluation board does not have reverse polarity protection. Applying a negative voltage to the VIN and GND terminals may damage the device. The maximum operating rating for V_{IN} is 1.6V. Exceeding 1.6V on the VIN could damage the device.

Getting Started

1. **VIN Supply**

   Connect a supply to the VIN and GND terminals, paying careful attention to the polarity and the supply range (0V < VIN < 1.6V). Do not apply power until step 4.

2. **Connect Load and Monitor Output**

   Connect a load to the VOUT1 and VOUT2 and GND terminals. The load can be either a passive (resistive) or an active (as in an electronic load) type. A current meter may be placed between the output terminals and load to monitor the output current. Ensure that the output voltage is monitored at the output terminals.

3. **Enable Input**

   The EN pin has an internal 4MΩ pull-down resistor to GND, which allows the output to be turned off when the EN jumper is removed. Applying an external logic signal on the EN pin to pull it high or using a jumper to short the EN pin to VIN to turn the outputs on.

4. **Turn Power**

   Turn on the VIN supply and verify that the output voltages VOUT1 = 1.8V and VOUT2 = 1.0V.

5. **Power Good Output**

   This is on open drain output that is pulled high when V_{IN}, V_{FB1} and V_{FB2} are within their nominal voltage levels. The power good will be pulled low without delay when the enable pin is set low.

6. **LED Output**

   This is an open drain output that is used for a low battery indicator. Under normal conditions, the LED is always ON. If the battery voltage is between 1.2V to 0.85V, the external LED will blink with a duty cycle of 25% at 0.25Hz. The LED will be OFF if the battery voltage falls below 0.85V for more than 15 cool-off cycles or the EN pin is low.

7. **SW1 and SW2 Test Points**

   These are switch node test points.

Ordering Information

Part Number	Description
MIC23099YFT EB	MIC23099 Evaluation Board

Evaluation Board Features

Feedback Resistors

An external resistive divider network (R1 and R2) with its center tap connected to the feedback pin sets the output voltage for each regulator. R1 is the top resistor and R2 is the bottom resistor in the divider string. The resistor values for the desired output voltage are calculated as illustrated in Equation 1. Large resistor values are recommended to reduce light load operating current, and improve efficiency. The recommended resistor value for R1 should be around, R1 ≈ 400kΩ.

$$R2 = \frac{R1}{\left(\frac{V_{OUT}}{0.6V} - 1\right)} \qquad \text{Eq. 1}$$

In the case of the boost converter, Equation 1 sets the output voltage to its PWM value. The no-load PFM output voltage is 2% higher than the PWM value. This higher PFM output voltage value is necessary to prevent PFM to PWM mode skipping which can introduce noise into the audio band.

Boost Switching Frequency

To reduce switching artifacts in the audio band, the buck and boost regulators switching frequency are controlled to minimize overlap. Figure 1 shows the boost switching frequency versus output load current and Figure 2 shows the buck switching frequency versus output load current.

The boost regulator operates in either PWM or PFM mode. To avoid PWM to PFM chatter, the PWM entry and exit points are not the same. When in PFM mode the output current needs to reach 90mA to enter into PWM mode and exits at 30mA. The boost switching frequency is greater than 100kHz with loads greater than 20mW.

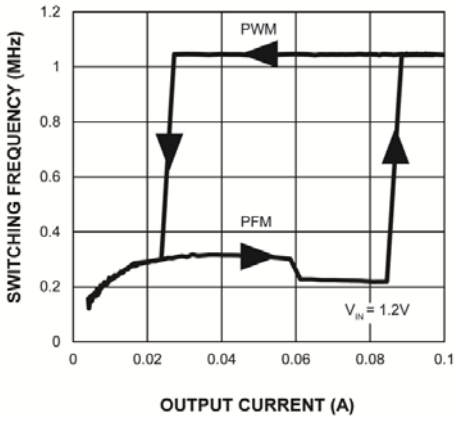


Figure 1. Boost Switching Frequency vs. Output Current

Buck Switching Frequency

The buck converter is designed to operate in PFM mode only. It has peak current control, which turns off the high-side switch when the inductor current hits the current limit threshold. The cycle repeats itself when the output voltage falls below its regulated value. As a result, the switching frequency varies linearly with output current as shown in Figure 2. The buck switching frequency is greater than 80kHz with loads greater than 8mW.

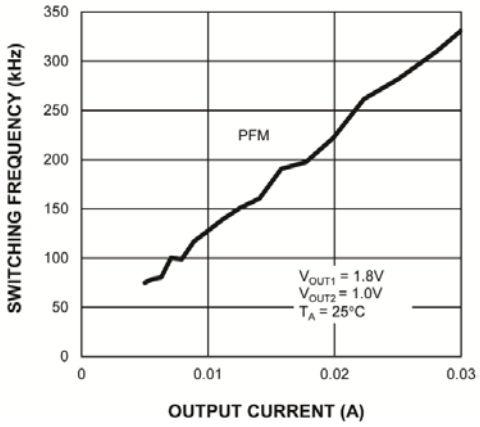


Figure 2. Buck Switching Frequency vs. Output Current

Power Good

The power good (PG) circuitry monitors the battery voltage and feedback pin voltage of the boost and buck regulators. The PG pin output goes logic high when FB1 and FB2 pin voltages are both greater than 92.5% (typical) of the internal reference voltage and the input voltage is greater than 0.85V (typical). To minimize false triggering, the power-good output has both a turn on delay and a falling deglitch delay.

Low-Battery Detection and Output Latch-Off

Figure 3 shows the low-battery power cycling operation. If the battery voltage (V_{IN}) drops below 0.85V for more than 100ms to 150ms, the PG de-asserts (goes low) and outputs V_{OUT1} and V_{OUT2} are disabled. Then the 500Ω active discharges resistors are enabled, discharges V_{OUT1} and V_{OUT2} to ground and finally the MIC23099 enters a cool off or sleep period. After a cool off period of about 1.3 seconds, if the battery voltage is above the 0.85V threshold, then the outputs will power up again. This cycle repeats itself until the end of the 15th cycle when both outputs are latched off for the last time.

The outputs can be turned back on by recycling the input power or by toggling the enable pin. If the battery voltage is still low, the MIC23099 will turn itself off again after 15 power-up cycles.

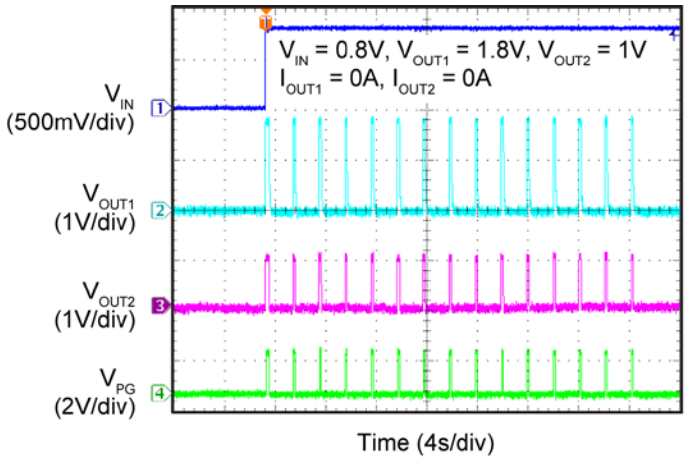


Figure 3. Low-Battery Power Cycling

Output Fault and Power Cycling

If either V_{OUT1} or V_{OUT2} outputs are out of tolerance for longer than the power good deglitch delay of between 60ms to 120ms, then both outputs are disabled. The power-down procedure is the same as the low-battery fault detection, as shown in Figure 3. The outputs can be turned back on by recycling the input power or by toggling the enable pin. The latch-off feature eliminates the thermal stress on the MIC23099 and the external inductors during a fault event.

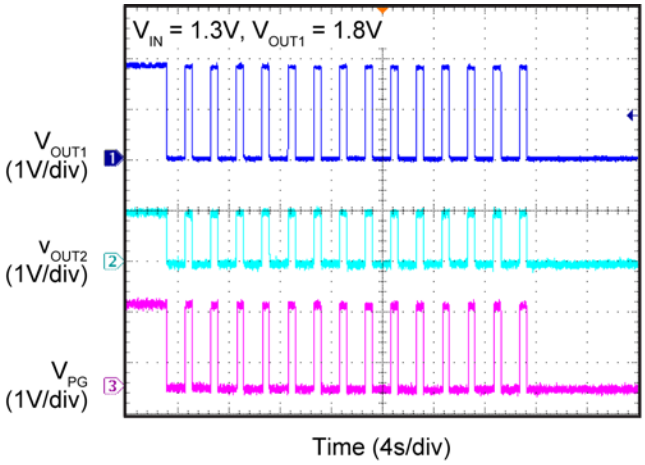


Figure 4. Output Fault Power Cycling

Boost Short-Circuit Protection

The low-side current limit protects the IC from transient-overload conditions, but not from a direct short-to-ground. The high-side MOSFET current limit provides the protection from a short-to-ground. In this fault condition, the high-side PMOS switch operates in linear mode and limits the current to approximately 80mA. If the short-circuit condition last for more than 30ms, the PMOS switch is latched off as shown in Figure 5. The outputs are not re-enabled until the input power is recycled or the enable pin is toggled.

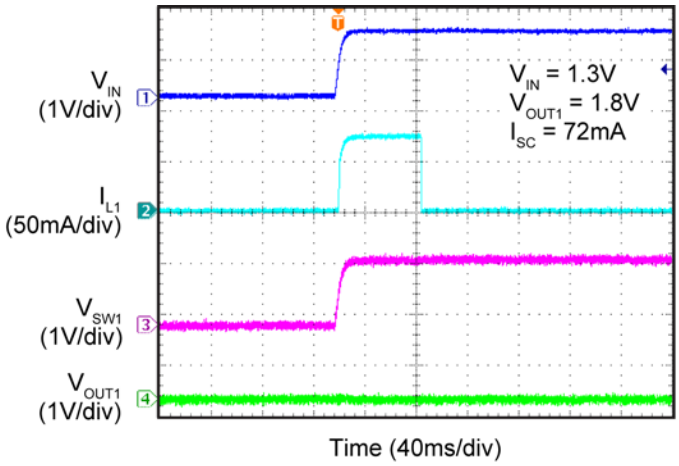


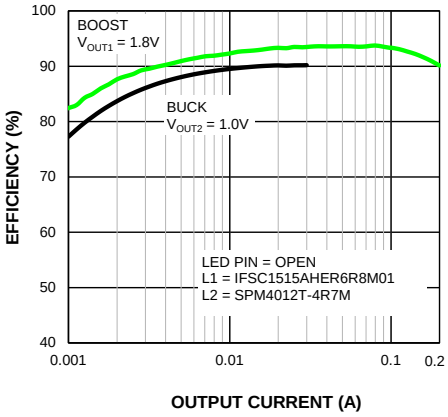
Figure 5. Power-Up into Short Circuit

Boost Overcurrent Protection

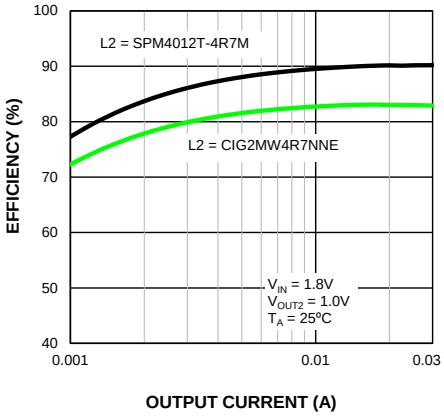
The boost converter has current-limit protection on both the high-side and low-side MOSFETs. The low-side MOSFET provides cycle-by-cycle current limiting. When the peak switch current exceeds the NMOS current limit threshold, then the low-side switch is immediately turned off and the high-side switch is turned on. Peak switch current is limited to approximately 1.5A. The low-side switch is allowed to turn on again on the next clock cycle. If the overload condition lasts more than 60ms to 120ms, then both outputs are disabled and the IC enters its power cycling mode.

Typical Characteristics

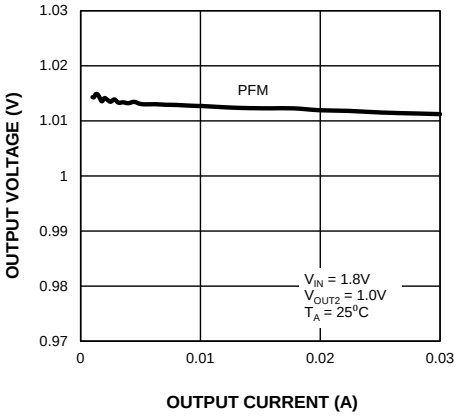
Efficiency (V_{IN} = 1.2V) vs. Output Current



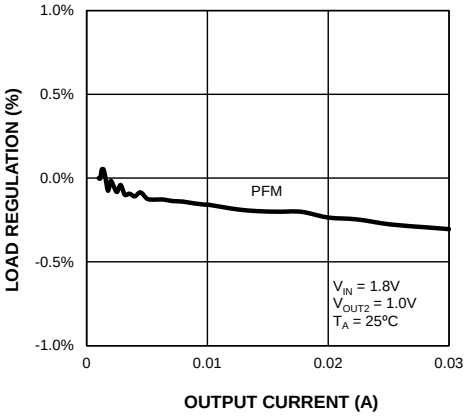
Buck Efficiency (V_{IN} = 1.8V) vs. Output Current



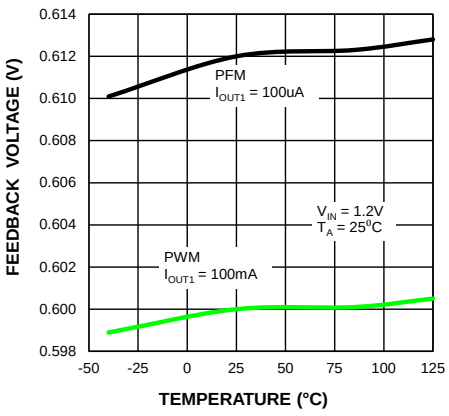
Buck Output Voltage vs. Output Current



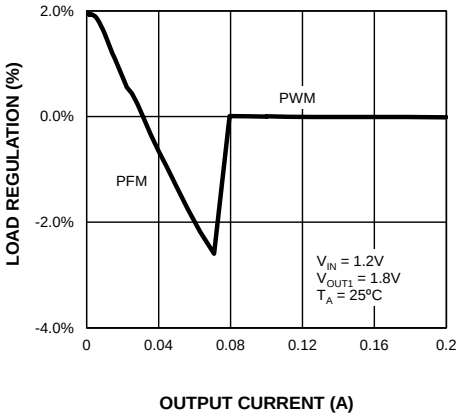
Buck Load Regulation vs. Output Current



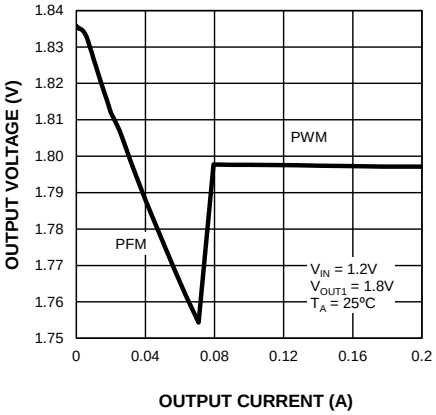
Boost Feeback Voltage vs. Temperature



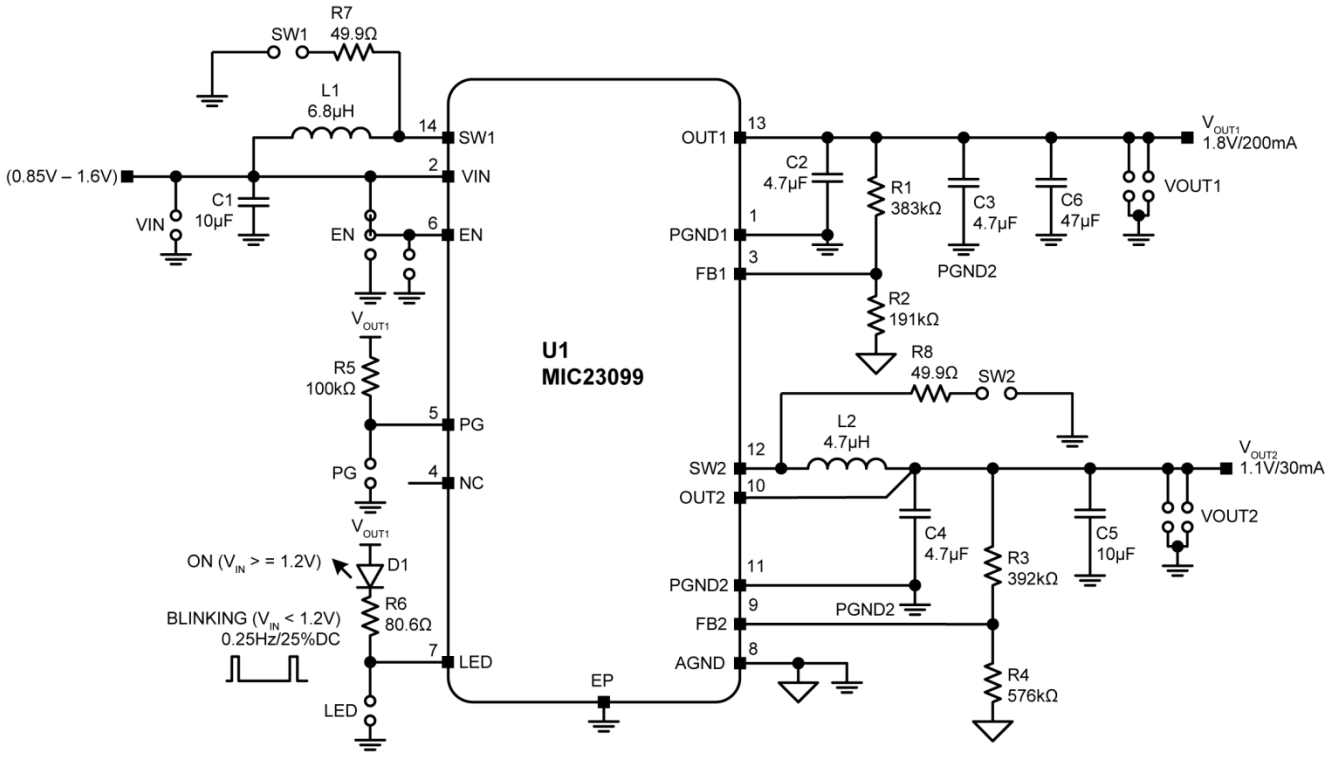
Boost Output Voltage vs. Output Current



Boost Output Voltage vs. Output Current

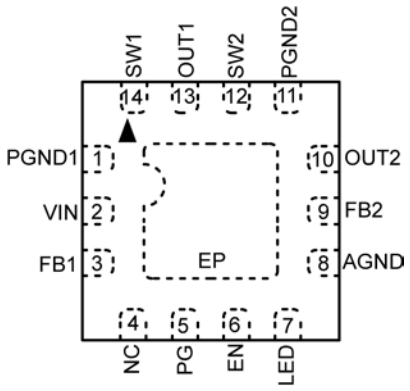


Typical Application Schematic



NOTE:
C5 AND C6 ARE THE SOC BYPASS CAPACITORS.

Pin Configuration



14-Pin 2.5mm × 2.5mm QFN (YFT)
(Top View)

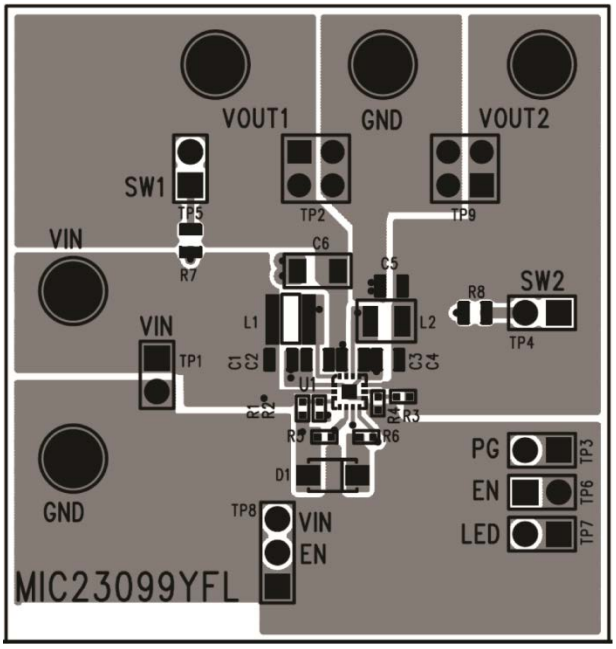
Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1, C5	GRM188R60J106ME47D	Murata[1]	10µF/6.3V, Ceramic Capacitor, X5R, 0603, ±20%	2
	CL10A106MQ8NNNC	Samsung[2]		
C2, C3, C4	GRM188R60J475ME19D	Murata	4.7µF/6.3V, Ceramic Capacitor, X5R, 0603, ±20%	3
	CL10A475MQ8NNNC	Samsung		
C6	GRM31CR60J476ME19L	Murata	47µF/6.3V, Ceramic Capacitor, X5R, 1206, ±20%	1
	CL31A476MQHNNNE	Samsung		
D1	SML-LXT1206SRC	Lumex[3]	1.7V/20mA, LED, 660NM RED WTR CLR, 1206	1
L1	IFSC1515AHER6R8M01	Vishay Dale[4]	6.8µH, 1.5A Inductor, 90mΩ, 3.8mm × 3.8mm × 1.8mm	1
L2	CIG2MW4R7NNE	Samsung	4.7µH, 1.1A Inductor, 140mΩ, 2.0mm × 1.6mm × 1.0mm	1
R1	RC1005F3833CS	Samsung	383kΩ Resistor, 0402, 1%	1
R2	RC1005F1913CS	Samsung	191kΩ Resistor, 0402, 1%	1
R3	RC1005F3923CS	Samsung	392kΩ Resistor, 0402, 1%	1
R4	RC1005F5763CS	Samsung	576kΩ Resistor, 0402, 1%	1
R5	RC1005F1003CS	Samsung	100kΩ Resistor, 0402, 1%	1
R6	RC1005F80R6CS	Samsung	80.6Ω Resistor, 0402, 1%	1
U1	**MIC23099YFT**	**Micrel[5]**	**Single AA/AAA Cell Step-Up/Step-Down Regulators with Battery Monitoring**	**1**

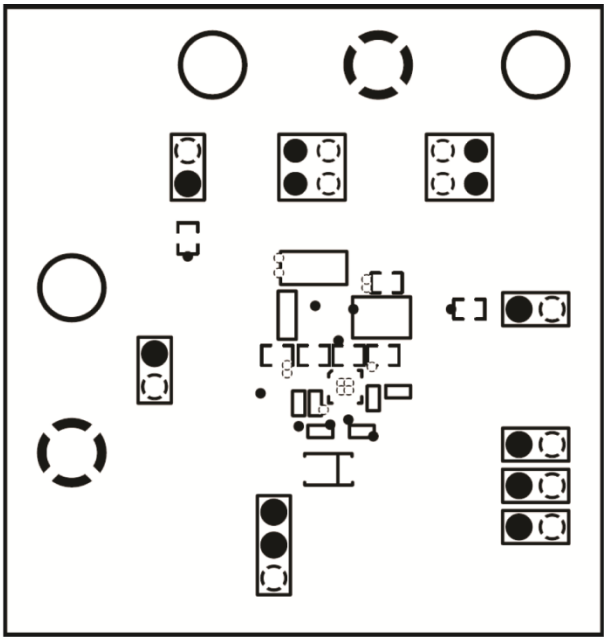
Notes:

1. Murata: www.murata.com.
2. Samsung: www.samsung.com.
3. Lumex: www.lumex.com.
4. Vishay Dale: www.vishay.com.
5. **Micrel, Inc.:** www.micrel.com.

PCB Layout Recommendations

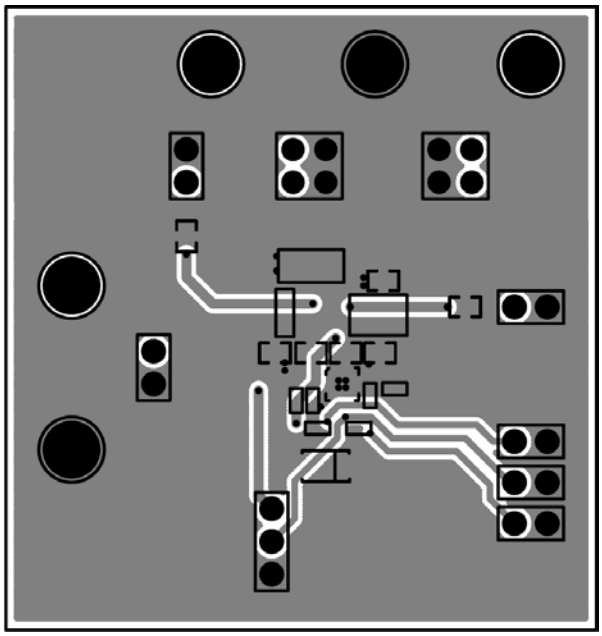


Top Layer (Power Trace Layer)

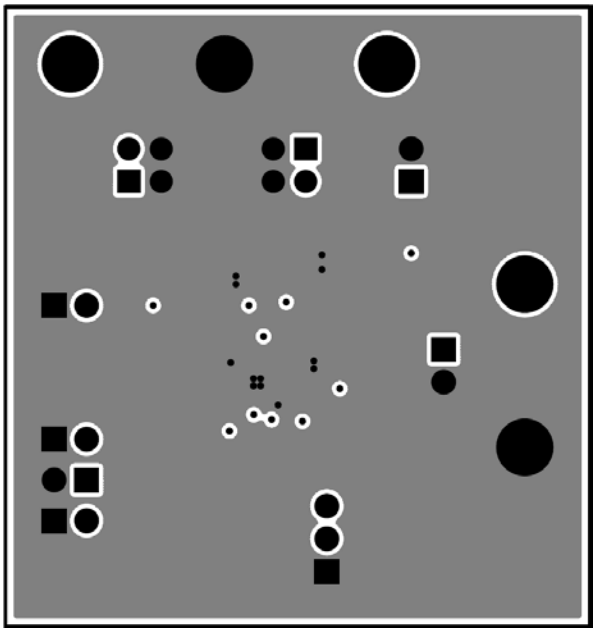


Layer 2 (Ground Plane)

PCB Layout Recommendations (Continued)

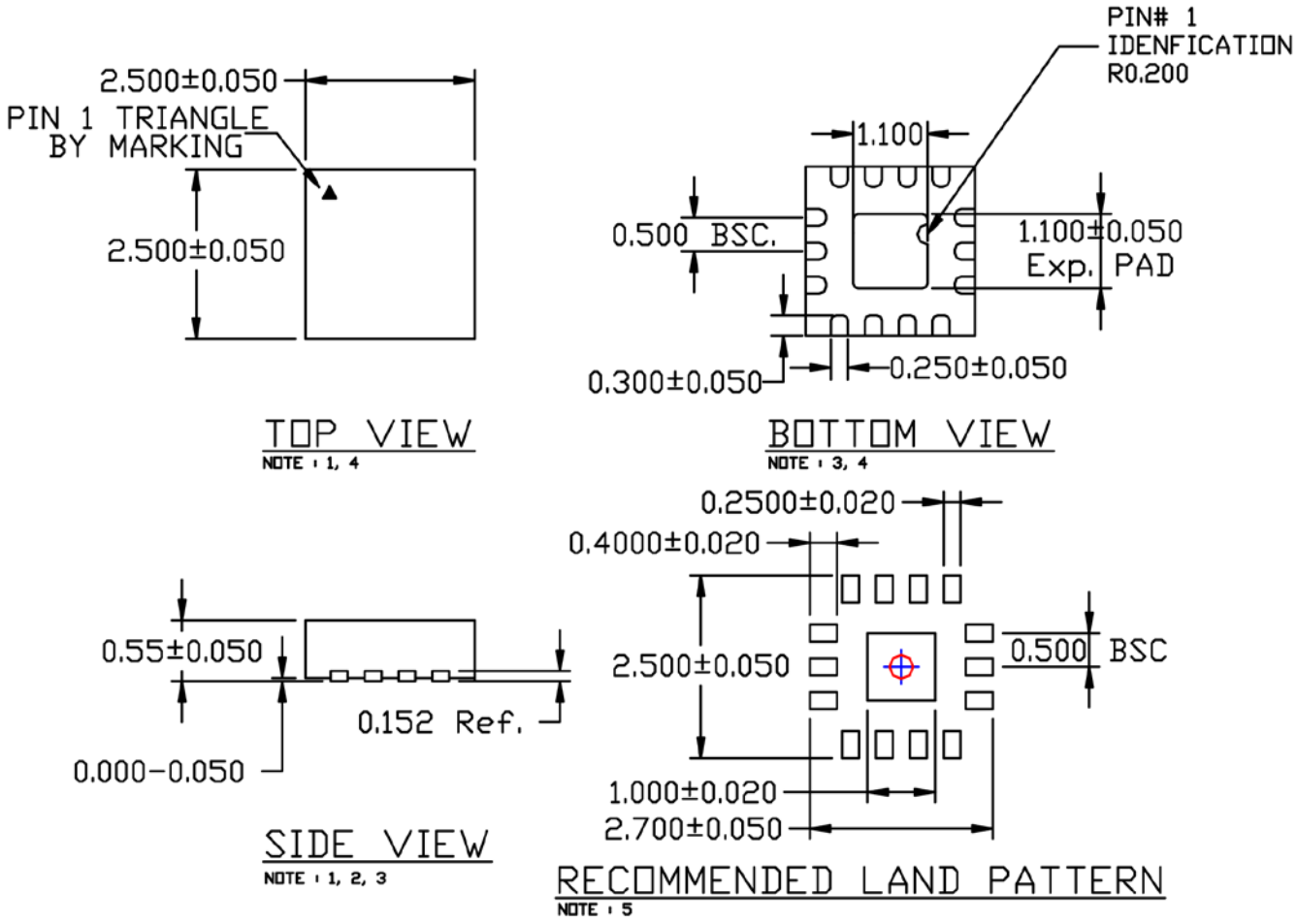


Layer 3 (Routing Layer)



Bottom Layer (Ground Plane)

Package Information and Recommended Landing Pattern[6]



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.08 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID WILL BE LASER MARKED.
5. RED CIRCLE INDICATE THERMAL VIA. SIZE IS 0.300-0.350 mm IN DIAMETER AND SHOULD BE CONNECTED TO GND PLANE FOR MAXIMUM THERMAL PERFORMANCE.

Note:

6. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.