MIC2550

Universal Serial Bus Transceiver

General Description

The MIC2550 is a single-chip transceiver that complies with the physical layer specifications for Universal Serial Bus (USB).

The MIC2550 supports full-speed (12Mbps) dual supply voltage operation (patent pending) and low-speed (1.5Mbps) operation.

A unique dual supply voltage operation allows the MIC2550 to reference the system I/F I/O signals to a supply voltage down to 2.5V while independently powered by the USB V_{BUS}. This allows the system interface to operate at its core voltage without addition of buffering logic and also reduce system operating current.

Features

- Compliant to USB Specification Revision 2.0 for low-speed (1.5Mbps) and full-speed (12Mbps) operation
- Compliant to IEC-61000-4.2 (Level 2)
- Operation down to 2.5V
- Dual supply voltage operation
- Integrated speed-select termination supply
- Very low power consumption meets USB suspend-current requirements
- Small 14-pin TSSOP and 16-pin MLF™ packages

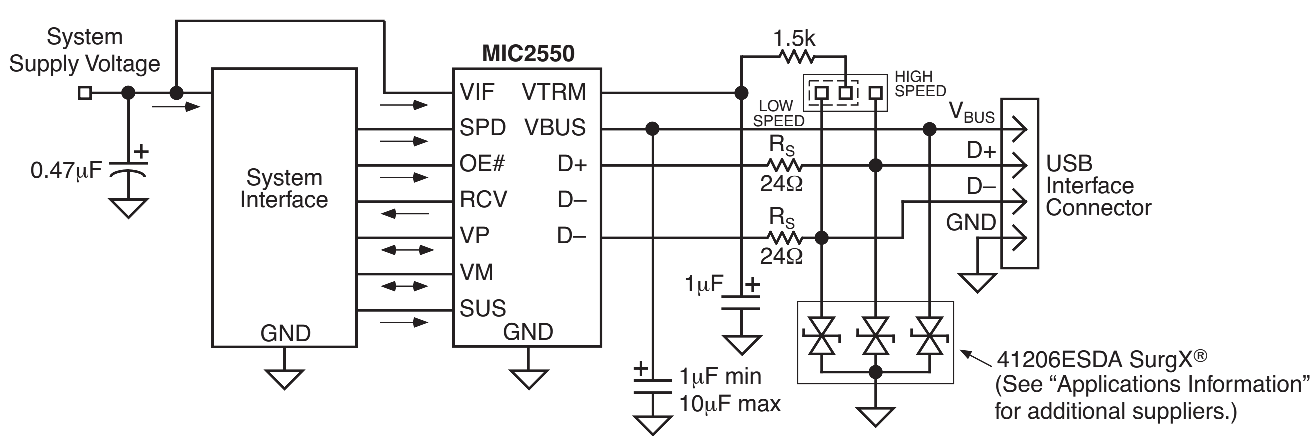
Applications

- Personal digital assistants (PDA)
- Palmtop computers
- Cellular telephones

Ordering Information

Part Number: Standard	Part Number: Pb-Free	Package
MIC2550BTS	MIC2550YTS	14-Pin TSSOP
MIC2550BML	MIC2550YML	16-Pin MLF™

System Diagram



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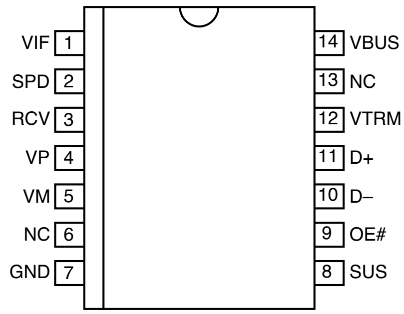
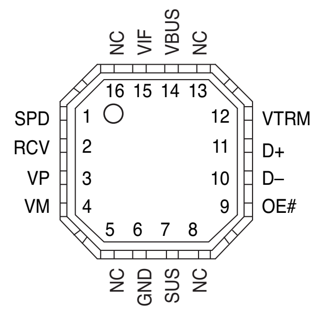
SurgX is a registered trademark of Cooper Electronics Technologies.

Pin Configuration



14-Pin TSSOP (TM)



16-Pin MLF™ (ML)

Pin Description

Pin Name	Pin Number MIC2550BTS	Pin Number MIC2550BML	Pin Function
VIF	1	15	System Interface Supply Voltage (Input): Determines logic voltage levels for system interface signaling to logic controller.
SPD	2	1	Speed (Input): Edge rate control. Logic high selects full-speed edge rates. Logic low selects low-speed edge rates.
RCV	3	2	Receive Data (Output): System interface receive data interface to logic controller.
VP	4	3	Plus (Input/Output): System interface signal to logic controller. If OE# is logic 1, VP is a receiver output (+); If OE# is logic 0, VP is a driver input (+).
VM	5	4	Minus (Input/Output): System interface signal to logic controller. If OE# is logic 1, VM is a receiver output (–); If OE# is logic 0, VM is a driver input (–).
NC	6, 13	5, 8, 13 16	Not internally connected.
GND	7	6	Ground: Power supply return and signal reference.
SUS	8	7	Suspend (Input): Logic high turns off internal circuits to reduce supply current.
OE#	9	9	Output Enable (Input): Active-low system interface input signal from logic controller. Logic low causes transceiver to transmit data onto the bus. Logic high causes the transceiver to receive data from the bus.
D–	10	10	USB Differential Data Line – (Input/Output)
D+	11	11	USB Differential Data Line + (Input/Output)
VTRM	12	12	Termination Supply (Output): 3.3V speed termination resistor supply output.
VBUS	14	14	USB Supply Voltage (Input): Transceiver supply.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{IF}) .... +6.5V
Input Voltage (V_{BUS}) .... –0.5V(min)/5.5V(max)
Output Current (I_{D+}, I_{D-}) .... ±50mA
Output Current (all others) .... ±15mA
Input Current .... ±50mA
Power Dissipation (P_D) .... TBD
Storage Temperature (T_S) .... –65° to +150°C
ESD, **Note 3**
  V_{BUS}, D+, D– .... ±10kV
  All other pins .... ±2kV

Operating Ratings (Note 2)

Supply Voltage (V_{BUS}) .... 4.0V to 5.25V
Temperature Range (T_A) .... –40°C to +85°C
Junction Temperature (T_J) .... 160°C
Package Thermal Resistance
  TSSOP (θ_{JA}) .... 100°C/W

Electrical Characteristics (Note 8)

T_A = 25°C, **bold** values indicate –40°C ≤ T_A ≤ +85°C; typical values at V_{BUS} = 5.0V, V_{IF} = 3.0V; minimum and maximum values at V_{BUS} = 4.0V to 5.25V, V_{IF} = 2.5V to 3.6V; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
System and USB Interface DC Characteristics						
V_{BUS}	USB Supply Voltage		4.0		5.25	V
V_{IF}	System I/F Supply Voltage		2.5		5.25	V
V_{IL}	Low-Level Input Voltage, **Note 4**				$0.15V_{IF}$	V
V_{IH}	High-Level Input Voltage, **Note 4**		$0.85V_{IF}$			V
V_{OH}	High-Level Output Voltage, **Note 4**	I_{OH} = 20µA	$0.9V_{IF}$			V
V_{OL}	Low-Level Output Voltage, **Note 4**	I_{OL} = 20µA			0.1	V
I_{IL}	Input Leakage Current, **Note 4**				±5	µA

Symbol	Parameter	Conditions					Min	Typ	Max	Units
		SPD	SUS	OE#	Voltage	Load				
I_{IF}	VIF Supply Current	1	0	1	VBUS = 5.25V VIF = 3.6V			1	**5**	µA
		1	0	0				1	**5**	µA
		0	0	1				1	**5**	µA
		0	0	0				1	**5**	µA
		0	1	0				1	**5**	µA
		1	0	0		f = 6MHz CLOAD = 50 pF, **Note 7**		325	**650**	µA
		0	0	0		f = 750kHz CLOAD = 600 pF **Note 7**		40	**75**	µA
I_{VBUS}	VBUS Supply Current	1	0	1	VBUS = 5.25V VIF = 3.6V			800	1100	µA
		1	0	0				3000	**5000**	µA
		0	0	1				230	**350**	µA
		0	0	0				400	700	µA
		0	1	0				130	200	µA
		1	0	0		f = 6MHz CLOAD = 50 pF, **Note 7**		7.3	**10**	mA
		0	0	0		f = 750kHz CLOAD = 600 pF **Note 7**		3.6	**5**	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TRM}	Termination Voltage	I_{TRM} = 2.5mA	3.0		3.6	V
ESD Protection						
IEC-1000-4-2	Air Discharge	10 pulses		±6		kV
(D+, D–, V_{BUS} only)	Contact Discharge	10 pulses		±6		kV

Symbol	Parameter	Condition	Min	Typ	Max	Units
Transceiver DC Characteristics						
I_{LO}	Hi-Z State Data Line Leakage	0V < V_{BUS} < 3.3V, D+, D–, OE# = 1 pins only	–10		+10	µA
V_{DI}	Differential Input Sensitivity	|(D+) – (D–)|, V_{IN} = 0.8V – 2.5V	0.2			V
V_{CM}	Differential Common-Mode Range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single-Ended Receiver Threshold		0.8		2.0	V
	Receiver Hysteresis, **Note 6**			200		mV
V_{OL}	Static Output Low, **Note 5**	OE# = 0, R_L = 1.5kΩ to 3.6V			0.3	V
V_{OH}	Static Output High, **Note 5**	OE# = 0, R_L = 15kΩ to GND	2.8		3.6	V
V_{CRS}	Output Signal Crossover Voltage **Note 6**		1.3		2.0	V
C_{IN}	Transceiver Capacitance, **Note 6**	Pin to GND			20	pF
Z_{DRV}	Driver Output Resistance	Steady state drive, **Note 6**	6		18	Ω
Low-Speed Driver Characteristics, Note 7						
t_R	Transition Rise Time	C_L = 50pF C_L = 600pF	75		 300	ns ns
t_F	Transition Fall Time	C_L = 50pF C_L = 600pF	75		 300	ns ns
t_R/t_F	Rise and Fall Time Matching	$T_R \div T_F$	80		125	%
V_{CRS}	Output Signal Crossover Voltage		1.3		2.0	V
Full-Speed Driver Characteristics, Note 7						
t_R	Transition Rise Time	C_L = 50pF	4		20	ns
t_F	Transition Fall Time	C_L = 50pF	4		20	ns
t_R/t_F	Rise and Fall Time Matching	$T_R \div T_F$	90		111.11	%
V_{CRS}	Output Signal Crossover Voltage		1.3		2.0	V
Transceiver Timing, Note 7						
t_{PVZ}	OE# to RCVR Tri-state Delay	Figure 1			15	ns
t_{PZD}	Receiver Tri-state to Transmit Delay	Figure 1	15			ns
t_{PDZ}	OE# to DRVR Tri-state Delay	Figure 1			15	ns
t_{PZV}	Driver Tri-state to Receiver Delay	Figure 1	15			ns
t_{PLH}	V+/V– to D+/D– Propagation Delay	Figure 4			15	ns
t_{PHL}	V+/V– to D+/D– Propagation Delay	Figure 4			15	ns
t_{PLH}	D+/D– to RCV Propagation Delay	Figure 3			15	ns
t_{PHL}	D+/D– to RCV Propagation Delay	Figure 3			15	ns
t_{PLH}	D+/D– to V+/D– Propagation Delay	Figure 3			8	ns
t_{PHL}	D+/D– to V+/D– Propagation Delay	Figure 3			8	ns

Note 1. Exceeding the absolute maximum rating may damage the device.

Note 2. The device is not guaranteed to function outside its operating rating.

Note 3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.

Note 4. Applies to the VP, VM, RCV, OE#, SPD, and SUS pins.

Note 5. Applies to D+, D–.

Note 6. Not production tested. Guaranteed by design.

Note 7. Characterized specification(s), but not production tested.

Note 8. Specification for packaged product only.

Timing Diagrams

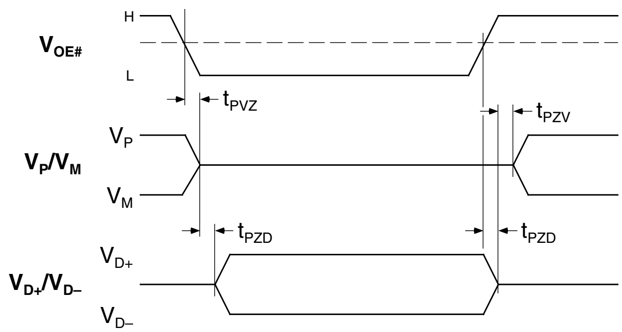


Figure 1. Enable and Disable Times

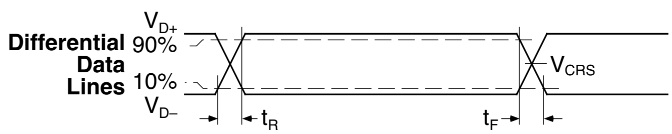


Figure 2. Rise and Fall Times

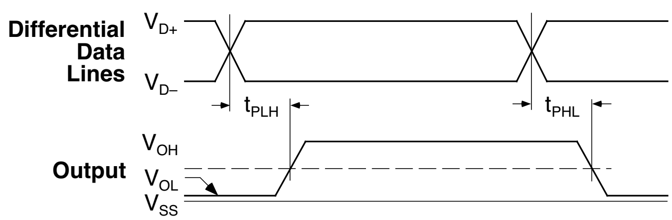


Figure 3. Receiver Propagation Delay D+/D– to RCV, V_P, and V_M

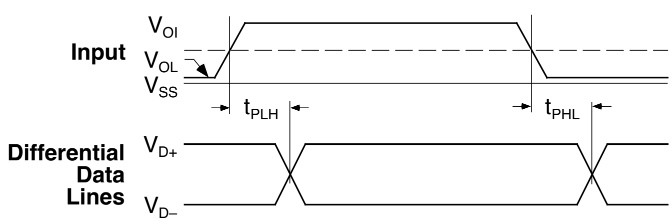
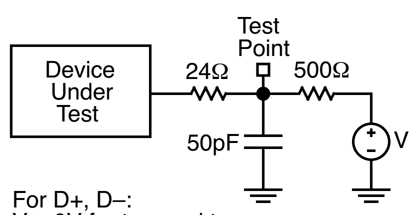


Figure 4. Driver Propagation Delay V_P and V_M to D+/D–

OE# = 0 (Transmit):					
Input		Output			Result
VP	VM	D+	D–	RCV	
0	0	0	0	X	SE0
0	1	0	1	0	Logic 0
1	0	1	0	1	Logic 1
1	1	1	1	X	Undefined
OE# = 1 (Receive):					
Input		Output			Result
D+	D–	VP	VM	RCV	
0	0	0	0	X	SE0
0	1	0	1	0	Logic 0
1	0	1	0	1	Logic 1
1	1	1	1	X	Undefined

Table 1. Truth Table

Test Circuits



For D+, D–:
V = 0V for t_{PZH} and t_{PHZ}
V = V_{BUS} for t_{PZL} and t_{PLZ}

Figure 5. Load for Enable and Disable Time (D+, D–)

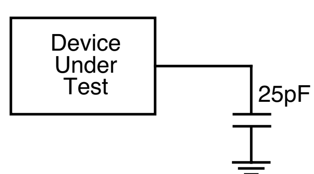
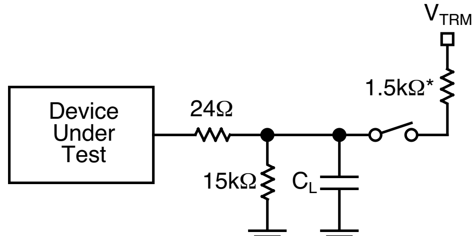


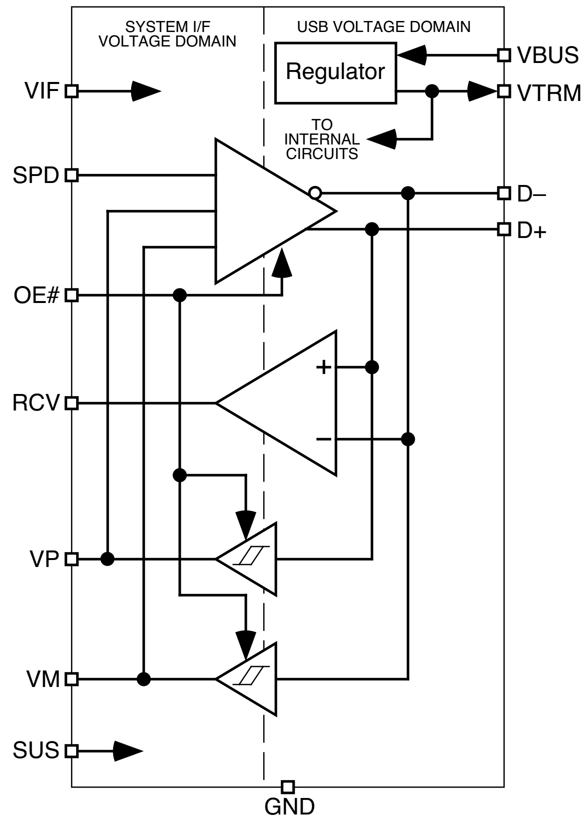
Figure 6. V_P, V_M and RCV Load



C_L = 50pF, full speed
C_L = 50pF, low speed (minimum timing)
C_L = 600pF, low speed (maximum timing)
*1.5k on D– for low speed or D+ for high speed

Figure 7. D+ and D– Load

Block Diagram



Applications Information

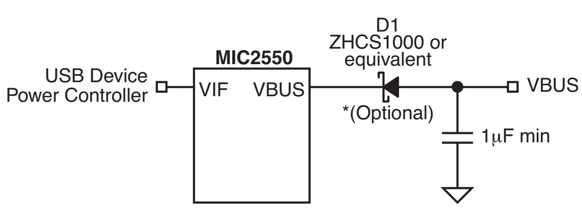
The MIC2550 is designed to provide USB connectivity in mobile systems where system supply voltages are not available to satisfy USB requirements. The MIC2550 can operate down to supply voltages of 2.5V and still meet USB physical layer specifications. As shown in the system diagram, the MIC2550 takes advantage of USB's supply voltage, V_{BUS}, to operate the transceiver. The system voltage, V_{IF}, is used to set the reference voltage used by the digital I/O lines (VP, VM, RCV, OE#, SPD, and SUS pins) interfacing to the system. Internal circuitry provides translation between the USB and system voltage domains. V_{IF} will typically be the main supply voltage rail for the system.

In addition, a 3.3V, 10% termination supply voltage, V_{TRM}, is provided to support speed selection. A 0.47µF (minimum) capacitor from V_{TRM} to ground is required to ensure stability. As shown in the typical application diagram, a 1µF capacitor is recommended. A 1.5K resistor is required between this pin and the D+ or D– lines to respectively specify full-speed or low-speed operation.

Power Supply Configurations

V_{IF}/V_{BUS} Switched

When the V_{BUS} input pin is pulled to ground a low impedance path between V_{IF} and V_{BUS} can cause a high current flow from V_{IF} to V_{BUS} thereby damaging the MIC2550. This issue can arise in systems where V_{BUS} is driven from a power supply that can be switched off such as in the case of a desktop PC. Adding a Schottky diode, such as the ZHCS1000 by Zetex, in series with V_{BUS} will prevent any current flow during this condition. A solution is shown in Figure 8 below.



Note: *(Optional) See Text - Power Supply Configurations

Figure 8. Solution to V_{IF}/V_{BUS} Switching

I/O Interface Using 3.3V

In systems where the I/O interface utilizes a 3.3V USB controller, an alternate solution is shown in Figure 9. This configuration has the advantage over Figure 8, in that no extra components are needed. Ensure that the load on V_{TRM} does not exceed 1mA total.

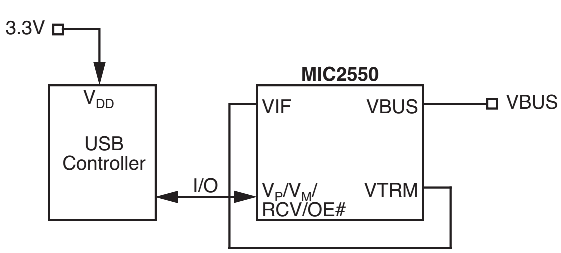


Figure 9. I/O Interface Uses 3.3V

Internal 3.3V Source

If the device is self-powered and has 3.3V available, the circuit in Figure 10 is yet another power supply configuration option. In this configuration, the internal regulator is disabled and the 3.3V source and not V_{BUS} powers the entire chip.

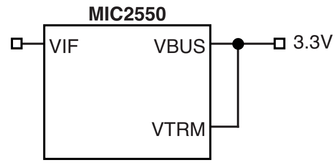


Figure 10. Powering Chip from Internal 3.3V Source

Suspend

When the suspend pin (SUS) is high, power consumption is reduced to a minimum. V_{TRM} is not disabled. RCV, V_P and V_M are still functional to enable the device to detect USB activity. For minimal current consumption in suspend mode, it is recommended that OE# = 1.

External ESD Protection

The use of ESD transient protection devices is not required for operation, but is recommended. We recommend the following devices or the equivalent:

Cooper Electronics Technologies (www.cooperet.com)
41206ESDA SurgX®
0805ESDA SurgX®

Littelfuse (www.littelfuse.com)
V0402MHS05
SP0503BAHT

Non-Multiplexed Bus

To save pin count for the USB logic controller interface, the MIC2550 was designed with V_P and V_M as bidirectional pins. To interface the MIC2550 with a non-multiplexed data bus, resistors can be used for low cost isolation as shown in Figure 11.

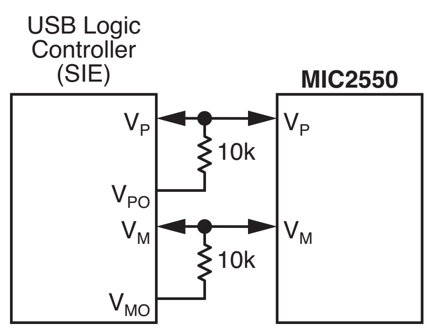


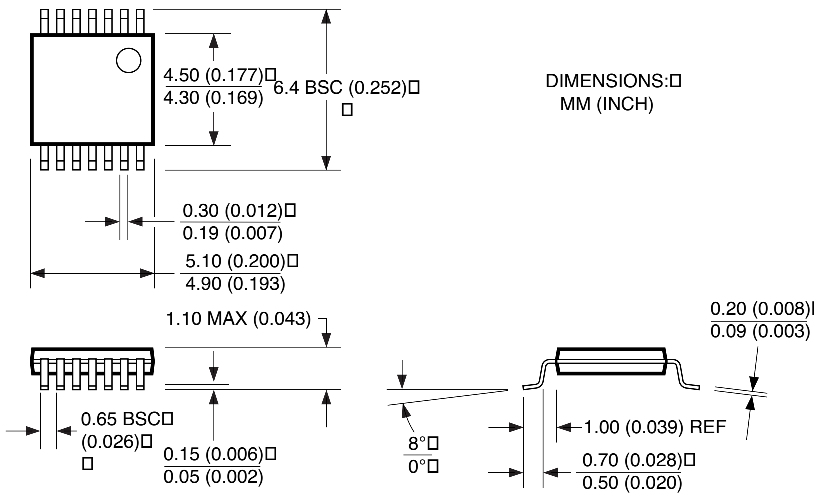
Figure 11. MIC2550 Interface to Non-Multiplexed Data Bus

PCB Layout Recommendations

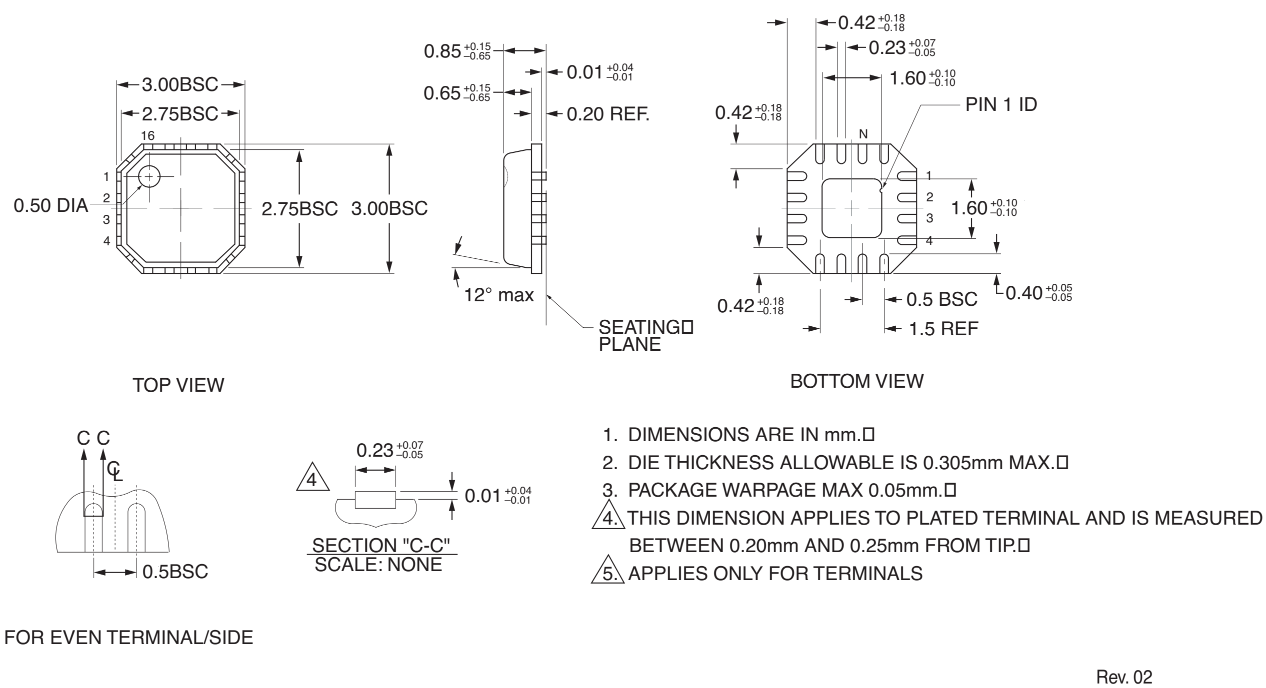
Although the USB standard and applications are not based in an impedance controlled environment, a properly designed PCB layout is recommended for optimal transceiver performance. The suggested PCB layout hints are as follows:

- Match signal line traces (VP/VM, D+, D–) to 40ps, approximately $^{1}/_{3}$ inch if possible. FR-4 PCB material propagation is about 150ps/inch, so to minimize skew try to keep VP/VM, D+/D– traces as short as possible.
- For every signal line trace width (w), separate the signal lines by 1.5–2 widths. Place all other traces at >2 widths from all signal line traces.
- Maintain the same number of vias on each differential trace, keeping traces approximately at same separation distance along the line.
- Control signal line impedances to ±10%.
- Keep R_S as close to the IC as possible, with equal distance between R_S and the IC for both D+ and D–.

Package Information



14-Pin TSSOP (TS)



16-Pin MLF™ (ML)