Product Document

Published by
ams OSRAM Group

Datasheet

DS000707

AS8579

Capacitive Sensor

v4-01 • 2022-Jun-08

Content Guide

1 General Description

The AS8579 is a capacitive sensor that detects the change of capacity in different applications. The capacitive sensor measures the relative change of the impedance (RealCapSense, due to our measurement principle), dependent on the circuit. This can be used for human being detection as well as many other applications

The IC capture the current of a metal object and applies algorithms to determine the capacitive and resistive information (Impedance). This information can be read via SPI Interface that can be also used for IC configuration.

This high precision performance sensor also supports a multitude of diagnostic features that meet standard functional safety requirements up to ASIL B. The capacitive sensing IC is specifically designed to work under high electromagnetic disturbances (EMC).

With this approach, the sensor can distinguish in a hands-on application if for example, a steering wheel is touched or not.

The AS8579 is available in an SSOP24 package and operates at a supply voltage of 5 V.

1.1 Key Benefits & Features

The benefits and features of AS8579, Capacitive Sensor, are listed below:

Figure 1:
Added Value of Using AS8579

Benefits	Features
Accurate capacitive measurement(including resistive information)	I/Q-signal demodulation
Higher durability and lower system costs	VAR_SEN & FIX_SEN function to avoid parasitic influences from cable and PCB
Enabler for safety critical applications	Processed according functional safety standard
Suitable for automotive applications	AEC-Q100 Grade 1 qualified

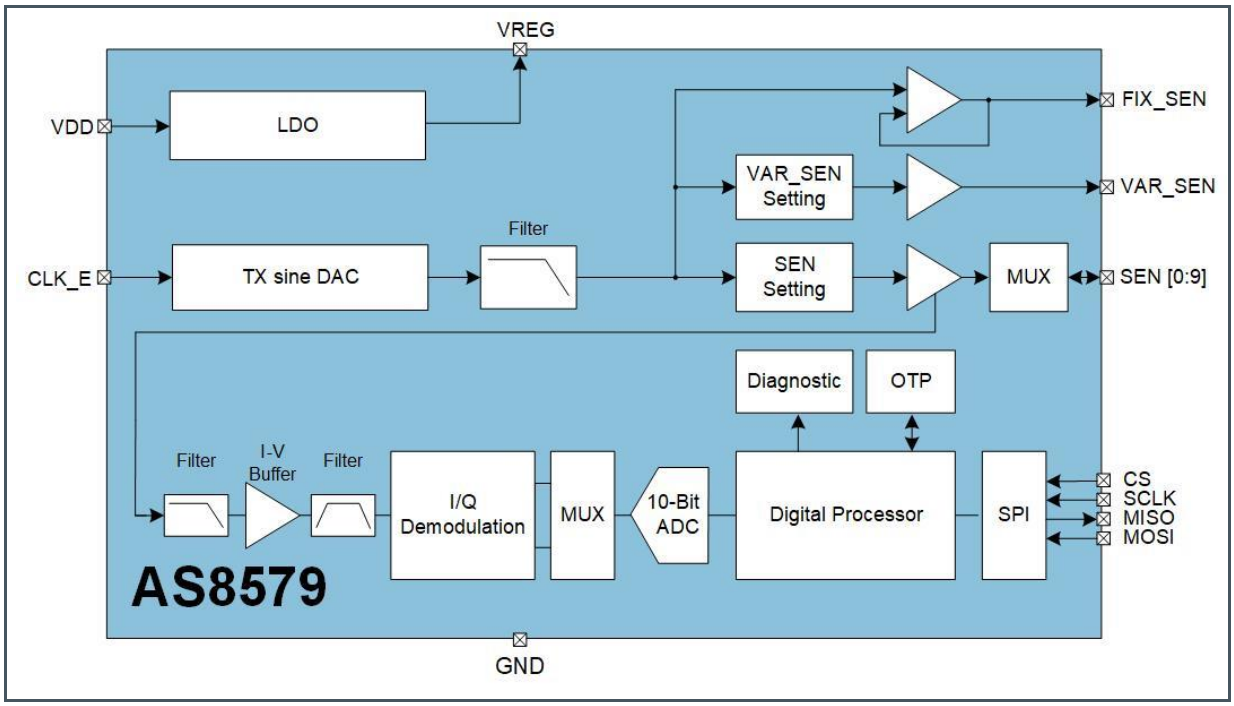
1.2 Applications

- Autonomous driving applications e.g.: Hands on steering wheel detection
- Detection of any human presence inside a vehicle
- Detection of any human presence exterior of vehicles e.g.: Automatic trunk opener (trunk opens automatically and touch-less by detection of human foot near the sensor only)

1.3 Block Diagram

The functional blocks of this device are shown below:

Figure 2 :
Functional Blocks of AS8579



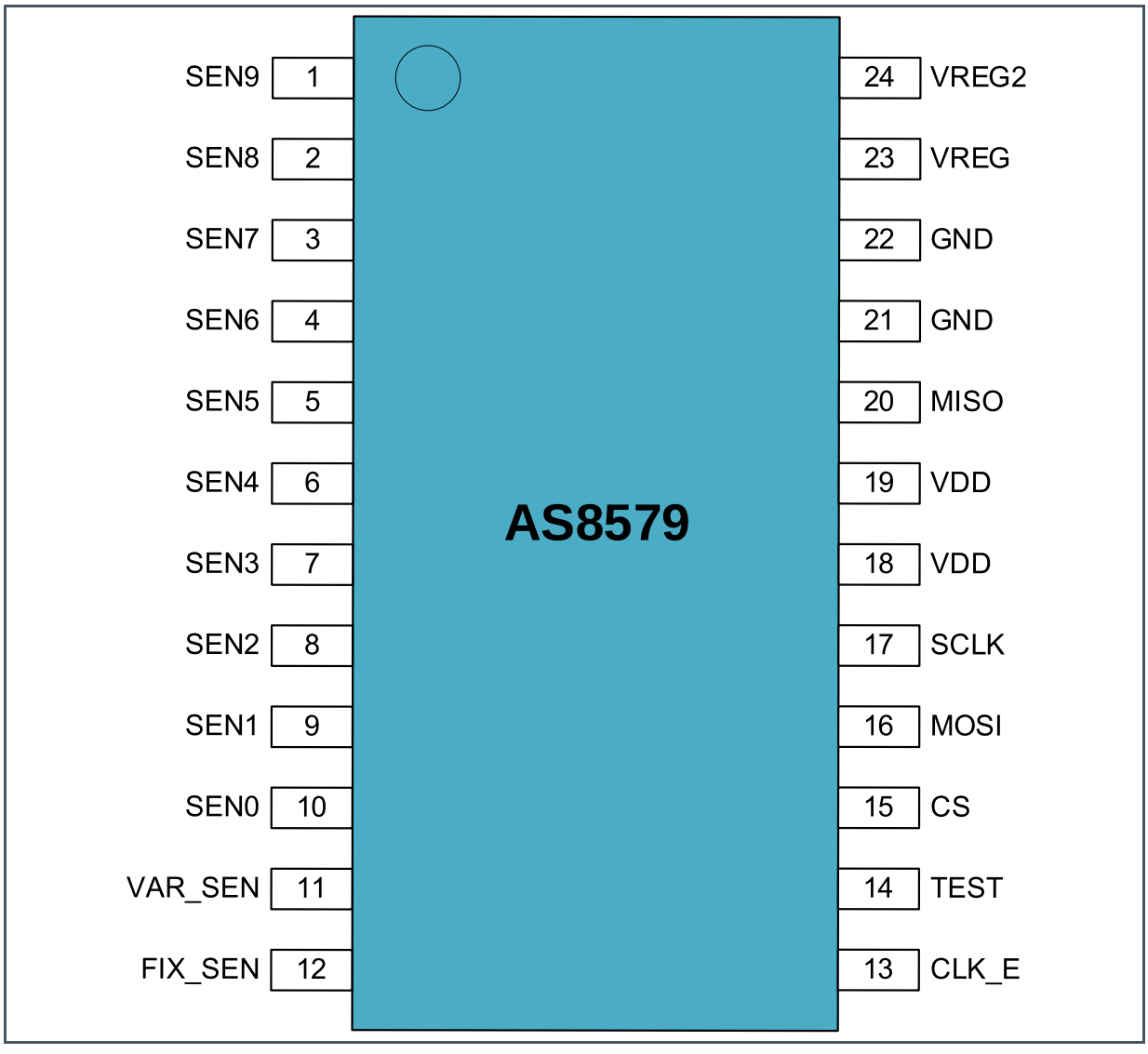
2 Ordering Information

Ordering Code	Package	Marking	Delivery Form	Delivery Quantity
AS8579-ASST	SSOP24	AS8579	Tape & Reel	2000 pcs/reel
AS8579-ASSM	SSOP24	AS8579	Tape & Reel	500 pcs/reel

3 Pin Assignment

3.1 Pin Diagram

Figure 3:
AS8579 Pin Assignment



3.2 Pin Description

Figure 4:
Pin Description of AS8579 (SSOP24 package)

Pin Number	Pin Name	Pin Type(1)	Description
1	SEN9	AIO 0 Ohm	Sensor Line 9
2	SEN8	AIO 0 Ohm	Sensor Line 8
3	SEN7	AIO 0 Ohm	Sensor Line 7
4	SEN6	AIO 0 Ohm	Sensor Line 6
5	SEN5	AIO 0 Ohm	Sensor Line 5
6	SEN4	AIO 0 Ohm	Sensor Line 4
7	SEN3	AIO 0 Ohm	Sensor Line 3
8	SEN2	AIO 0 Ohm	Sensor Line 2
9	SEN1	AIO 0 Ohm	Sensor Line 1
10	SEN0	AIO 0 Ohm	Sensor Line 0
11	VAR_SEN(2)	AIO 0 Ohm	Cable Shielding Driver
12	FIX_SEN(3)	AIO 0 Ohm	PCB Shielding Driver
13	CLK _E	DI_PD	System Clock
14	TEST		Factory Test Pin connect to GND
15	CS	DI_PD	SPI Chip Select (active high)
16	MOSI	DI_PD	SPI Data in
17	SCLK	DI_PD	SPI Clock
18	VDD	S	External 5 V Supply
19	VDD	S	External 5 V Supply
20	MISO	DO	SPI Data out
21	GND	S	Ground
22	GND	S	Ground
23	VREG	S	Internal 3.45 V Supply
24	VREG2	S	Connect to VREG

(1) Explanation of abbreviations:
AIO 0Ohm Analog Input/Output
DI_PD Digital Input with internal pull-down (see Electrical Characteristics)
DO Digital Output
S Supply
(2) VAR_SEN optionally connected to cable shielding to avoid parasitic capacitance influences from the shielding
(3) FIX_SEN optionally connected to PCB shield layer to avoid parasitic capacitance influences from PCB shield layer

4 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5
Absolute Maximum Ratings of AS8579

Symbol	Parameter	Min	Max	Unit	Comments
Electrical Parameters					
VDD	DC Supply Voltage at VDD Pin	-0.3	7	V	Non operational
VDC_ON	DC Voltage at Digital IO Pins	-0.3	VDD+0.3	V	
VDC_SEN	Sensor Analog Pins (SENx, VAR_SEN)	-0.3	20	V	
ISCR	Input Current (latch-up immunity)		±100	mA	AEC-Q100-004
Electrostatic Discharge					
ESD_HBM	Electrostatic Discharge HBM		±2	kV	AEC-Q100-002
ESD_MM	Electrostatic Discharge MM		±100	V	AEC-Q100-003
ESD_CDM	Electrostatic Discharge CDM		±500	V	AEC-Q100-011 ±750 V on corner pins only
Temperature Ranges and Storage Conditions					
T_{AMB}	Operating Ambient Temperature	-40	125	°C	
T_{STRG}	Storage Temperature Range	-55	150	°C	
T_{BODY}	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020(1)
RH_{NC}	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level		3		Represents a maximum floor life time of 168 hours

(1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.” The lead finish for Pb-free leaded packages is “Matte Tin” (100 % Sn)

5 Electrical Characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

All in this datasheet defined tolerances for external components need to be assured over the whole operation conditions range and also over lifetime.

Overall condition: T_{AMB} = -40 °C to 125 °C, VDD = 4.8 V to 5.2 V; components specification; unless otherwise noted

5.1 Operating Conditions

Figure 6:
Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD	VDD	Static condition	4.8	5.0	5.2	V
VREG	Regulator Voltage		3.0	3.45	3.6	V
IDD_1	Supply Current	Drivers enabled			50	mA
I_VL	Input Low Voltage	CLK, CS, SCLK, MOSI	GND		0.3*VDD	V
I_VH	Input High Voltage	CLK, CS, SCLK, MOSI	0.7*VDD		VDD	V
CLK_E	System CLK Frequency		3		50	MHz
SCLK	SPI_CLK Frequency				8	MHz
O_VL	Output Low Voltage	MISO	GND		0.4	V
O_VH	Output High Voltage	MISO	4.0		VDD	V
O_IOUT	Output Current	MISO			4	mA
O_PD	Pull-Down Value	DOUT	30		200	kΩ

5.2 Analog Front End

Figure 7:
Analog Front End

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SENS	System sensitivity	@PGA=0, CBG=0, TXV=2, FREQ=3	9.375	12.5	15.625	LSB/pF
C_{SENSE}	Sensing capacity range	Measuring range with 5 kOhm in parallel	20		2000	pF
C_{LOAD}	capacity of cable shielding		0		2000	pF
LIN	Overall system linearity	Sensor capacitance range 0 nF to 2 nF			1	%
NOISE	System noise	On I or Q registers 3σ noise referenced to full scale			±0.2	%
PSR	System power supply rejection				±20	LSB
VMM	Output voltage mismatch between drivers				1	%
PMM	Output phase mismatch between drivers				2	Deg
ROUT0	SENx output DC resistance	MODE=0	10			MΩ
ROUT1	SENx output DC resistance	MODE=1			10	Ω
ROUT2	SENx output DC resistance	MODE=2	3.5	5	6.5	kΩ
SCI	Sensor crosstalk impedance	Differential impedance between SENx pins	5			MΩ
CAP	Output capacitance of SEN line				8	pF
DCAP	Driver output capacitance drift over temp / lifetime				0.5	pF

5.3 Sensor Driver

The Sensor Driver has the ability to drive a continuously changing load of 20 pF to 2000 pF in parallel with 5 kΩ, with a 1.0 Vp-p AC term over a frequency range of 45 kHz – 125 kHz. The driver (gain 1 V/V) provides a low impedance output to drive the sensor lines (SEN0 – SEN9).

Figure 8:
Output Driver and Current Sensing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SD_VDC	Output DC voltage		1.18	1.23	1.28	V
SD_AC2	Output voltage, TXV=2		1.020	1.070	1.120	Vpp
SD_AC1	Output voltage, TXV=1		0.510	0.535	0.560	Vpp
IOUT_AC	Output AC peak current				8.5	mA
I_SHORT	Output short current to GND				50	mA
SD_GAIN	Gain closed loop		0.99	1	1.01	V/V
ROUT	Output impedance closed loop				10	Ω
CLOAD	Output total load capacitance		0		2000	pF

5.4 Diagnostic Thresholds

In Figure 9 the thresholds are shown, which will trigger setting the Diagnostics in the Status Register (see 7.2.2).

Positive Diagnostic threshold must be higher than max level of the diagnosed signal.

Negative Diagnostic threshold must be lower than min level of the diagnosed signal.

Figure 9:
Diagnostic Threshold Levels

Symbol	Parameter	Min	Typ	Max	Unit
REGF_L	VREG detection threshold low	3.0	3.15	3.3	V
REGF_H	VREG detection threshold high	3.6	3.8	4	V
BPFF_L	Detection threshold low	0.25	0.3	0.33	V
BPFF_H	Detection threshold high	VREG-0.33	VREG-0.30	VREG-0.25	V

Symbol	Parameter	Min	Typ	Max	Unit
OCSEN	Threshold sensor driver	7	8.5	10	mA
OCSLD	Threshold VAR_SEN	7	8.5	12	mA
TXF_H1	Threshold high (TXV=1)	1.61	1.70	1.79	V
TXF_H2	Threshold high (TXV=2)	1.85	1.95	2.05	V
TXF_L1	Threshold low (TXV=1)	0.75	0.80	0.85	V
TXF_L2	Threshold low (TXV=2)	0.46	0.50	0.54	V
TXF_MP	Margin between threshold high and TX positive peak	30			mVdc
TXF_MN	Margin between TX negative peak and threshold low	30			mVdc
PGA1F_L	Detection threshold low	0.2	0.25	0.28	V
PGA1F_H	Detection threshold high	VREG-0.28	VREG-0.25	VREG-0.2	V
PGA2F_L	Detection threshold low	0.2	0.25	0.28	V
PGA2F_H	Detection threshold high	VREG-0.28	VREG-0.25	VREG-0.2	V
CLKD_F	Frequency for flag	0.35	1	2	MHz
CBF_L	Detection threshold low	0.25	0.3	0.33	V
CBF_H	Detection threshold high	VREG-0.33	VREG-0.3	VREG-0.25	V
PPSF_R	Threshold resistance	10	20	30	kΩ

6 Functional Description

The transceiver Analog Front-End (AFE) architecture performs the primary function of the AS8579, which is to sense the impedance of the output load. This is done using transmitter and receiver blocks. The transmitter block supplies the load a sine wave across. Then the receiver block captures the current response of the load. Here the change of the current in phase and modulus will be sensed. The current response is converted to a voltage via trance-impedance amplifier and then demodulated into in-phase (I) and quadrature (Q) components. I and Q components are then filtered and converted to 10-bit digital words via ADC. These I and Q words are accumulated awaiting 16-bit SPI transmission.

Current response can be measured on any of the 10 SEN pins connected to the Sensor Driver through analog multiplexers (MUX). The external processor controls the MUX. The processor retrieves the I and Q components of each sensor from AS8579 and then determines the size of the impedance load of the external sensor(s).

There are four selectable non-harmonic sensor frequencies for generating the sensor driver output signal: 45.45 kHz, 71.43 kHz, 100 kHz and 125 kHz. This can be set in FREQ register (see 7.2.7)

6.1 Diagnostics

6.1.1 Safety Mechanism Overview

Figure 10:
Safety Mechanism Overview

SM	Diagnostic Name	Description/Safe State	Status Flag	Blanking
SM1	Regulator Fail	Low voltage or high voltage detected on 3.3 V regulator	REGF=1	Blanking not needed
SM2	Filter Fail	Voltage on internal bandpass filter is out of range	BPFF=1	Blanking required(1)
SM3	Overcurrent on VAR SEN	Overcurrent condition on the VAR_SEN Driver	OCSLD=1	Blanking required(1)
SM4	Overcurrent on SEN	Overcurrent condition on the sensor driver	OCSEN=1	Blanking required(1)
SM5	Signature	Signature calculation error of OTP content.	OTPF=1	Blanking not needed
SM6	Out of Range (SEN Lines)	Sensor driver output voltage outside operating range	TX1F=1	Blanking required(1)
SM7	Out of Range (VAR _SEN)	Shield driver output voltage outside operating range	TX2F=1	Blanking required(1)
SM8	PGA FAIL 1 (I-Path)	I - Channel is saturated high or low	PGA1F=1	Blanking required(1)
SM9	PGA FAIL 2 (Q-Path	Q - Channel is saturated high or low	PGA2F=1	Blanking required(1)
SM10	NCLK	CLK_E is missing or is invalid.	NCLK=1	Blanking not needed
SM11	CBF	Internal current buffer output is out of range - high or low.	CBF=1	Blanking required(1)
SM12	PPSF	Pin to Pin short diagnostic for MUX controlled outputs (SEN lines)	PPSF=1	Blanking not needed

(1) This signal requires to be synchronized and filtered to avoid a certain spike in MCLK domain. This signal must stay at ‘1’ for at least some MCLK cycles. The number of MCLK cycles is specified by the BLANK register (0x2B/0x3B). For this refer to 6.1.3

6.1.2 Safety Mechanism Explanation

For checking the thresholds and limits of the Safety Mechanism please refer to 5.4

SM1 Regulator Fail

The safety mechanism Regulator fail is monitoring the voltage on the Regulator.

The sensor provides an error flag REGF=1 in Status Register when the regulator voltage (VREG) is lower than voltage threshold REGF_L or higher than voltage threshold REGF_H.

SM2 Filter Fail

The safety mechanism Filter fail is monitoring the voltage of the internal Band-pass filter.

The sensor provides an error flag BPFF =1 in Status Register when the input voltage of the internal Band-pass filter is lower than voltage threshold BPFF_L or higher than voltage threshold BPFF_H.

SM3 Overcurrent on VAR SEN

The safety mechanism Overcurrent on VAR_SEN is monitoring output current of the VAR_SEN driver.

The sensor provides an error flag OCSLD=1in Status Register when the output current of driver higher than current threshold OCSLDT.

SM4 Overcurrent on SEN

The safety mechanism Overcurrent on SEN is monitoring output current of the sensor driver.

The sensor provides an error flag OCSEN=1in Status Register when the output current of driver higher than current threshold OCSENT.

SM5 Signature

A signature check is performed on all the OTP content after each OTP reset pulse, this happens also at power on and after each EDIV update. In case of signature error and until the signature calculation execution a diagnostic bit OTPF = 1 is latched in the SPI Status Register. The signature bits are calculated based on the OTP content.

SM6 Out of Range (SEN Lines)

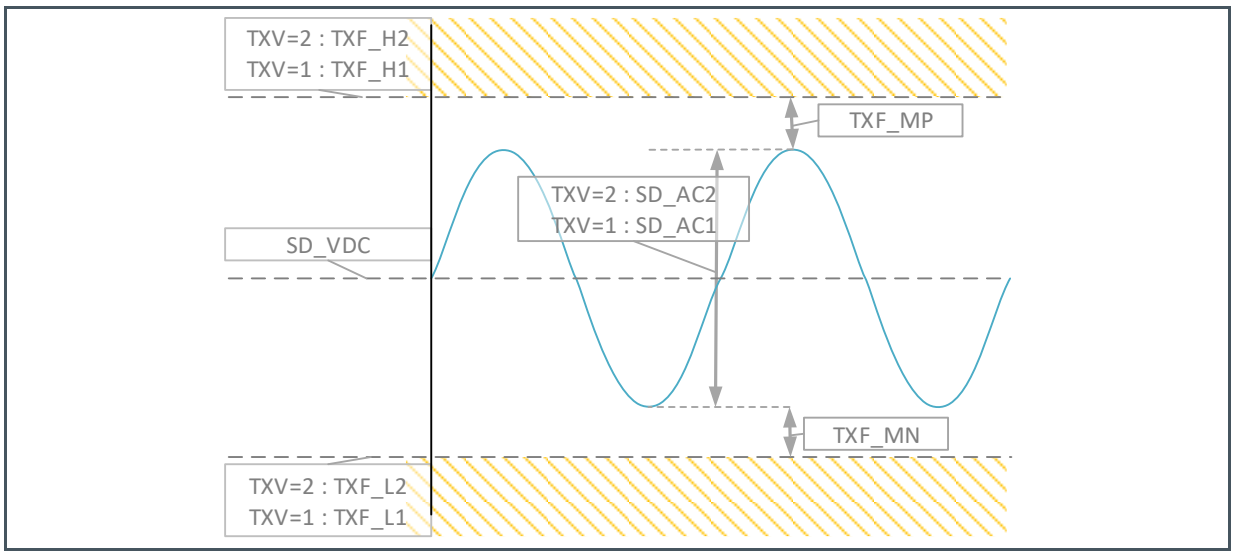
The safety mechanism Out of Range (SEN) is monitoring the voltage on the sensor driver output. The voltage threshold limits are depending on the configured transmitter voltage (SD_ACx). The sensor provides an error flag TX1F=1 in Status Register when the driver output voltage (SD_AC1) is lower than voltage threshold TXF_Lx or higher than voltage threshold TXF_Hx.

SM7 Out of Range (VAR_SEN & FIX_SEN)

The safety mechanism Out of Range (VAR_SEN & FIX_SEN) is monitoring the voltage on the VAR_SEN and FIX_SEN driver output. The voltage threshold limits are depending on the configured transmitter voltage (SD_ACx).

The sensor provides an error flag TX2F=1 in Status Register when the driver output voltage (TXDRV_AC1) is lower than voltage threshold TXF_Lx or higher than voltage threshold TXF_Hx.

Figure 11:
SM6 + SM7 Description



SM8 PGA FAIL 1 (I-channel)

The safety mechanism PGA FAIL 1 is monitoring if the I-channel is getting saturated high or low.

The sensor provides an error flag PGA1F=1 in Status Register when the output voltage of I channel is lower than voltage threshold PGA1F_L or higher than voltage threshold PGA1F_H.

SM9 PGA FAIL 2 (Q-channel)

The safety mechanism PGA FAIL 2 is monitoring if the Q-channel is getting saturated high or low.

The sensor provides an error flag PGA1F=1 in Status Register when the output voltage of Q channel is lower than voltage threshold PGA2F_L or higher than voltage threshold PGA2F_H.

SM10 Missing CLK_E Diagnostic

The missing CLK_E diagnostic (NCLK) monitors the system clock MCLK to ensure that it is running and therefore CLK_E is coming from the microprocessor. If CLK_E is not running or invalid, the NCLK

bit is set in the SPI Status register. In case of this error, the chip cannot guarantee the correct synchronization between SPI clock and MCLK.

SM11 CBF

The safety mechanism Current Buffer Fail is monitoring the output voltage of the current-to-voltage buffer. The sensor provides an error flag CBF=1 in Status Register when the output voltage is lower than voltage threshold CBF_L or higher than voltage threshold CBF_H.

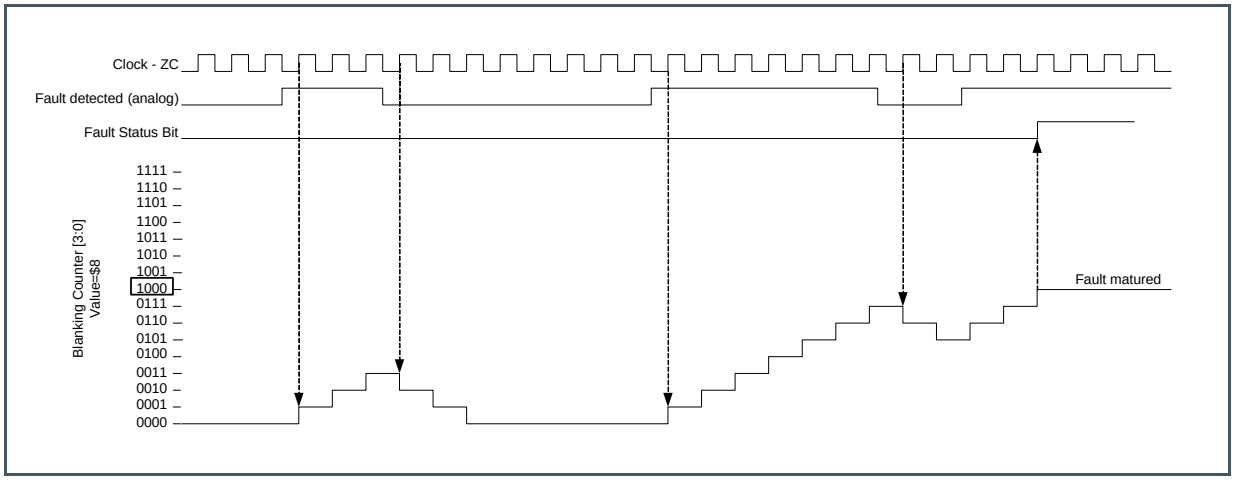
SM12 PPSF

The Pin-to-Pin Short diagnostic is realized with a pin-to-pin DC resistance measurement. For the pair of pins being tested, the main MUX is set to MODE=0 (open). Two diagnostic MUX can route any of the 11 tested pins (SEN lines & VAR_SEN to a comparator) programmed by PLUS/MINUS register (0x2C/0x3C), referenced by a resistive divider. In case the resistance is too low, the PPSF Flag is going high.

6.1.3 Blanking Error Flags

Each Safety Mechanism has its own Up/Down Counter (individually blanked). See 7.2.2 Status Register or 6.1.1 Safety Mechanism Overview for details on which diagnostic needs blanking. The 0x2B command is used to read the current value of the BLANK register. The counters are clocked from a signal synchronous with the transmitter sine wave. Effectively each Diagnostic is checked once per sine cycle. The diagnostic bits in the Status Register which need blanking, do not clear when Error is disappearing. They are latched until the Status Register is read through SPI.

Figure 12:
Example Diagnostic Maturity Using Blanking



Description in chapter “Diagnostic Blanking Register (Address 0x2B/0x3B)

6.2 SPI Interface

The sensor contains a single serial peripheral interface (SPI), consisting of Serial Clock (SCLK), Data Out (MISO), Data In (MOSI), and Chip Select (CS) pins. The AS8579 is configured as a SPI slave. The SPI interface is used to edit Register content, access Control and readout Sensor Values

The CS input selects this device for serial transfers. CS is active high. Register data is shifted in the MOSI pin and shifted out the MISO pin on each subsequent SCLK. The CS input has a pull-down internal to the IC, which pulls this pin to the negated state should an open circuit condition occur.

The SCLK input is the clock signal input for synchronization of serial data transfer. When CS is asserted, both the SPI master and the slave latch input data on the rising edge of SCLK. The SPI master typically shifts data out on the falling edge of SCLK, as does this device. SCLK input has a pull-down internal to the AS8579 which pulls this pin to the negated state should an open circuit condition occur. SCLK can idle in either state (high or low).

The MISO output pin is in a tri-state condition when CS is low. Data is transmitted on MISO MSB first. MISO has a weak pull-down to set the bus to a defined state when the output is in tri-state mode.

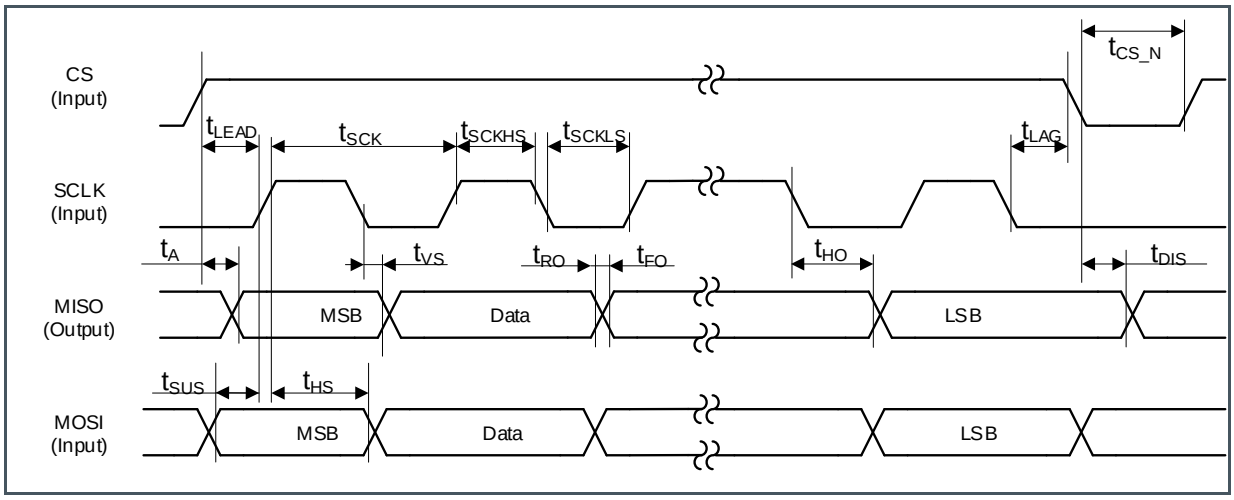
MOSI takes data from the master microprocessor while CS is asserted. Data is received MSB first. MOSI has a pull-down internal to the AS8579 which pulls this pin to the negated state should an open circuit condition occur.

Figure 13:
SPI TIMING

Symbol	Parameter	Min	Typ	Max	Unit
t_{SCK}	SCLK Period	125			ns
t_{LEAD}	Enable Lead Time	16.25			ns
t_{LAG}	Enable Lag Time	12.5			ns
t_{SCKHS}	SCLK High Time	25			ns
t_{SCKLS}	SCLK Low Time	25			ns
t_{SUS}	MOSI Input Setup Time	5			ns
t_{HS}	MOSI Input Hold Time	5			ns
t_{A}	MISO Access Time			50	ns
t_{DIS}	MISO Disable Time			25	ns
t_{VS}	MISO Output Valid Time			20	ns
t_{HO}	MISO Output Hold Time	0			ns

Symbol	Parameter	Min	Typ	Max	Unit
t_{RO}	Rise Time			7.2	ns
t_{FO}	Fall Time			7.5	ns
t_{CS_N}	CS_N Negated Time	50			ns
f_{OP}	Transfer Frequency	DC		8	MHz

Figure 14:
Timing Diagram



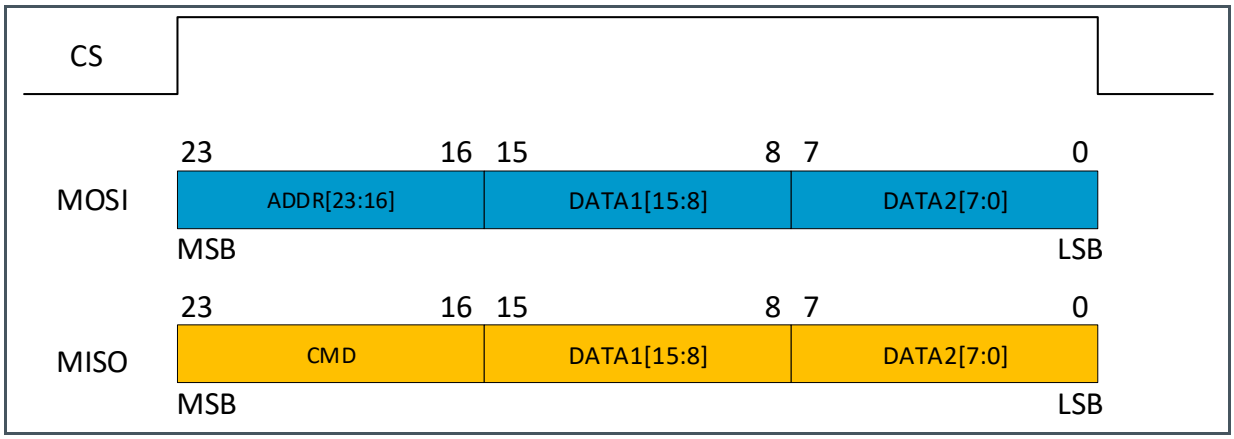
The serial communications shall be accomplished with the CS, SCLK, MOSI, and MISO pins. The host CPU selects the AS8579 with the CS signal and shifts data into the AS8579 MOSI input using the SCLK for synchronizing the bit shifts. Upon receiving SCLKs from the host CPU (when selected), the AS8579 shifts data out the MISO pin. Serial data from MOSI is latched into the shift register on the rising edge of SCLK. Data is shifted out to MISO on the falling edge of SCLK.

There are 3 types of commands for the SPI:

- Read
- Write
- “Quick Read”

All command and data bytes are 8 bits wide. Data bytes always sent and received MSB first.

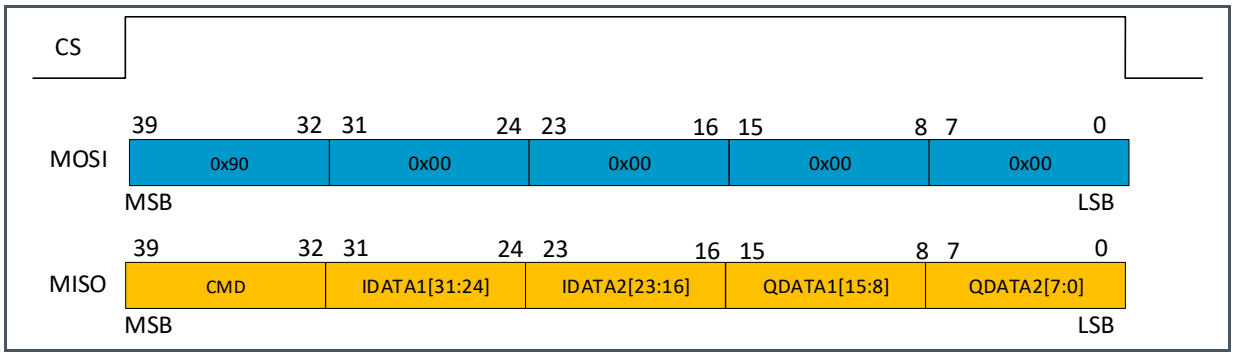
Figure 15:
Read/Write Command



All Write commands are 3 bytes long with the order: command, data high, data low. For these commands data will always be sent and received in Big Endian format; i.e. most significant byte first. Incoming data will be padded with zeros to fill the 2 data bytes. The first returned byte will be an echo of the command. The second and third bytes will return 0x00. Following the third byte, subsequent clocks will return a '0'.

Most Read commands are 3 bytes long with the order: command, data high, data low. When reading I and Q registers at the same time for a "quick read" 5 bytes are required in this order: command, I data, I data, Q data, Q data. For all Read commands data will always be sent and received in Big Endian format; i.e. most significant byte first. The 2 or 4 bytes of data from the host should all be 0x00. The first returned byte will be an echo of the command. The second through fifth bytes will return the data in the register(s) being read. Following the third/fifth byte, subsequent clocks will return the last data bit.

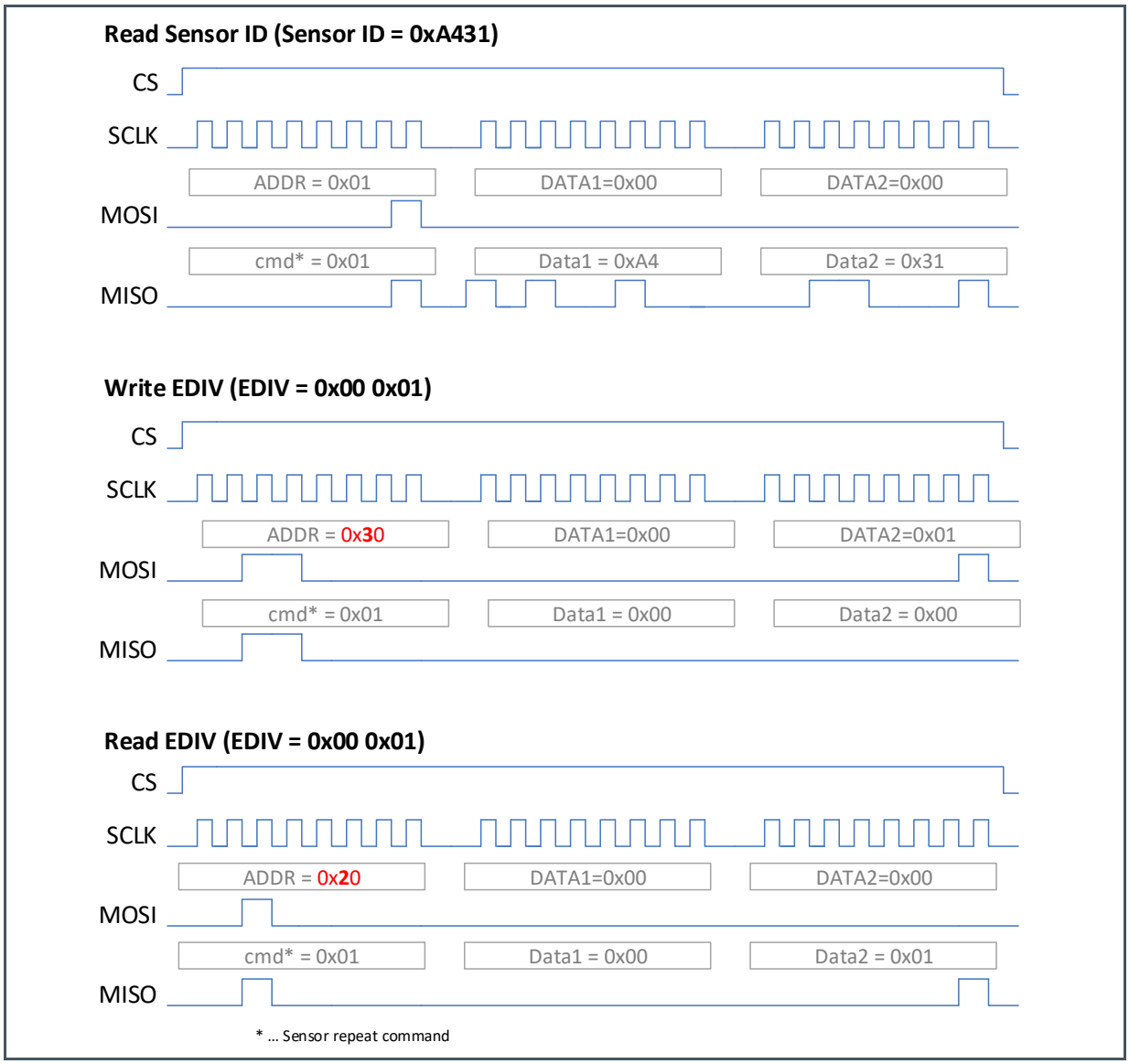
Figure 16:
Quick Read Command



Quick Read I and Q Data Register (0x03 and 0x04):

The 0x90 command allows for I and Q data to be read from the same sensor signal sample by doing a quick read on both I and Q data registers. This command links the I and Q registers together into a 32-bit word. This data is read back using a 40-bit word in this order: command byte, I data word, Q data word. I/Q data matching is guaranteed using the Quick Read command (i.e. – I and Q data will be from a matched sample). The I and Q data registers are reset to 0x00 after reading.

Figure 17:
SPI Example of Read Sensor ID, Write EDIV and Read EDIV Register



ADC Functional Description

For digitizing the I and Q values, a 10-bit ADC is used. Conversions are run using the internal system clock.

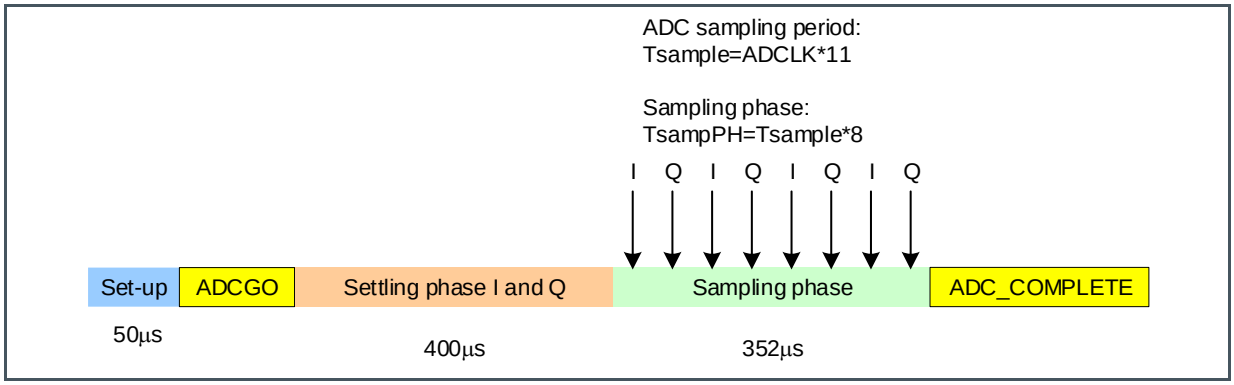
The ADC can do different conversion modes. This can be set in the ADCTL register (0x2A/0x3A). (see 7.2.16)

Single Conversion

“Single Conversion” causes the ADC to wait for the “system settling time" before starting sampling and then to accumulate the number of samples, specified in the register ADCTL [5:4]. I and Q samples arrive interleaved. The DSP control logic will provide the analog part the signal IQMUX to switch the ADC analog input between I channel and Q channel.

Once completed, I and Q results are moved to the SPI output registers and the “ADC_COMPLETE” bit in register 0x05 is set. Before another “Single Conversion” can be started, the ADC must be reset by either performing a Quick Read (0x90), or by issuing the “ADC Reset” command.

Figure 18:
Measuring Cycle

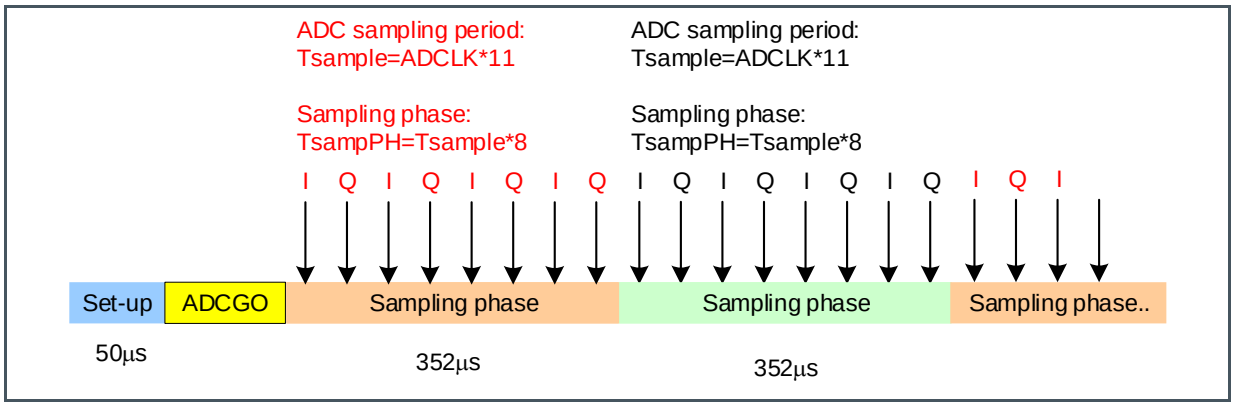


Continuous Conversion

“Continuous Conversion” mode causes the ADC to take successive samples accumulations of I and Q, again the number of samples taken is specified by ADCTL [5:4] register (0x2A/0x3A).

The ADC is time multiplexed between the I and Q channels (I and Q samples are interleaved). Each data point stored to the SPI output register is the accumulation of a programmed number of 10-bit ADC values, for each I and Q. Data is stored to the SPI as a complete I and Q set (data synchronicity is guaranteed by the Control Logic).

Figure 19:
Measuring Cycle



Before changing a parameter of the ADCTL [7:0] (0x2A/0x3A) the ADC and accumulators have to be reset, this operation is done by writing ADCTL [1:0] = 0. This resets the DSP and brings ADC to reset condition as well. In a next SPI access the command start of conversion are sent (single / continuous conversion)

7 Register Description

7.1 Register Overview

7.1.1 Position of the Read/Write Bit

The position of the Read/Write Bit is at Bit [4] of the command byte, which implies that the register address for reading a register is different as write the same register.

Figure 20:
Position of Read/Write Bit

Figure 21:
Register Overview

Read ADDR	Write ADDR	Name	Default	Description
0x01		Sensor ID	0xA431	ID of the Sensor
0x02		Status Reg	0x0000	Error Register
0x03		I_DATA	0x0000	I Data Information
0x04		Q_DATA	0x0000	Q Data Information
0x05		ADC_Status	0x0000	Bit is set when the ADC has completed
0x20	0x30	EDIV	0x0000	System CLK Divider Selection (CLK_E)
0x21	0x31	FREQ	0x0000	Frequency Selection

Read ADDR	Write ADDR	Name	Default	Description
0x22	0x32	TXV	0x0000	Sensor Driver Voltage Selection
0x23	0x33	SEN/MODE	0x0000	MUX control for the connected SENx Pins
0x24	0x34	SDG	0x0000	VAR_SEN Gain Selection
0x25	0x35	CBG	0x0000	Current Buffer Gain Selection
0x26	0x36	DCLK	0x0000	Demodulation Clock Selection
0x27	0x37	PGA	0x0000	Command sets the PGA voltage Gain. Adjusts the input voltage to the ADC to optimize its conversion resolution.
0x28	0x38	OFFSET_I PGA	0x0000	Command is used to program the offset DAC to compensate parasitic offsets
0x29	0x39	OFFSET_Q PGA	0x0000	Command is used to program the offset DAC to compensate parasitic offsets
0x2A	0x3A	ADCTL	0x0000	Controls the ADC converter cycles
0x2B	0x3B	BLANK	0x003F	This Register is used to program the 6-Bit register up/down counter used for blanking faults
0x2C	0x3C	PLUS/MINUS	0x00FF	Control the pin-to-pin short diagnostic MUX

7.2 Detailed Register Description

7.2.1 Sensor ID Register (Address 0x01)

The 0x01 command is used to read the ID Register. Reading this register will always return 0xA431. This is used by the microprocessor to validate the SPI communication to the sensor.

Figure 22:
SENSOR ID Register

AS8579 ID [15:0] Binary	Read/Write	Default Value
1010 0100 0011 0001	R	0xA431

7.2.2 Status Register (Address 0x02)

The 0x02 command is used to read the Status Register plus diagnostics.

Figure 23:
Status Register

Name	Bit Position	Read/Write	Description
R_EDIV	15:13	R	Bit [0:2] from EDIV Register (0x20/0x30)
OTPF	12	R	Occurs when signature of the OTP is wrong
PPSF	11	R	Pin-to-Pin short Error. Pins under test are shorted together. Blanking not needed.
BPFF	10	R	Occurs when voltage of internal filter is exceeding the operating range.
REGF	9	R	Error Flag (=1) occurs Regulator voltage is exceeding the operating range. Blanking not needed.
OCSLD	8	R	Error Flag (=1) occurs when current exceeds the maximum limit.
OCSEN	7	R	Error Flag (=1) occurs when current exceeds the maximum limit.
TEST	6	R	For internal use
TX1F	5	R	Error Flag (=1) occurs output voltage of sensor driver is exceeding the operating range.
TX2F	4	R	Error Flag (=1) occurs output voltage of VAR_SEN driver is exceeding the operating range.
PGA1F	3	R	PGA1F=1 when I channel is saturated high or low.
PGA2F	2	R	PGA2F=1 when Q channel is saturated high or low.
NCLK	1	R	NCLK=1 when the clock is missing or invalid on CLK_E
CBF	0	R	CBF=1 occurs when output voltage of current buffer is exceeding the operating range.

7.2.3 I-Channel Data (Address 0x03)

According to the register settings the Accumulated Data for the I-Channel. Dependent on the accumulation setting in the ADCTL register (0x2A/0x3A), the value can be from 12 up to 14 bits.

The content of the register can be read out with command 0x90.

Figure 24:
I-Channel Data

Name	Bit String (13:0)	Read/Write	Description
ACCU I	XX00 0000 0000 0000	R	Data Register

7.2.4 Q-Channel Data (Address 0x04)

According to the register settings the Accumulated Data for the Q-Channel. Dependent on the accumulation setting in the ADCTL register (0x2A/0x3A), the value can be from 12 up to 14 bits.

The content of the register can be read out with command 0x90.

Figure 25:
Q-Channel Data

Name	Bit String (13:0)	Read/Write	Description
ACCU Q	XX00 0000 0000 0000	R	Data Register

7.2.5 ADC Status Register (Address 0x05)

The 0x05 command is used to read the “ADC Complete” status bit (Bit [0] from Register 0x05). This bit is set when the ADC has completed the accumulation of the programmed samples of both the I and Q data signals and placed the data in the SPI output registers. The bit is cleared upon reading the combined data registers (0x90 command) or when a new ADC cycle is initiated.

Figure 26:
ADC Status

Name	Bit Position	Read/Write	Measurement Data
ADC complete	0	R	Bit is set (1) when ADC has completed accumulation.

7.2.6 CLK_E Timing Selection Register (Address 0x20/0x30)

The 0x30 command controls the division factor (EDIV [3:0]) applied to CLK_E pin to generate the internal system clock. The division factor is programmable from 1 to 12. Default value at power-up is 12. The 0x20 command is used to read the current value of EDIV. The applied system clock must be at 4 MHz after the CLK_E Frequency dividing factor. (e.g.48 MHz / 12 = 4 MHz)

Figure 27:
EDIV Register

EDIV [3:0] Binary	Read/Write	CLK_E Frequency Dividing Factor
0000	R/W	12
0001	R/W	11
0010	R/W	10
0011	R/W	9
0100	R/W	8
0101	R/W	7
0110	R/W	6
0111	R/W	5
1000	R/W	4
1001	R/W	3
1010	R/W	2
1011	R/W	1
1100	R/W	1
1101	R/W	1
1110	R/W	1
1111	R/W	1

The clock obtained by the frequency division of the CLK is called MCLK and is used to clock all the digital part except the SPI interface. Each time there is an EDIV change, an automatic OTP reset is generated to clean up the memory from possible timing error if the previous selected MCLK was higher than 4 MHz. The reload of the OTP memory takes less than 8190 MCLK clock cycles, during the reload phase it is possible to have SPI communication, but not possible to start sensing.

7.2.7 Frequency Selection Register (Address 0x21/0x31)

The 0x31 command is used to select the sine wave generator frequency for the sensor driver output. At power-up, FREQ default is set to 0x00. The 0x21 command is used to read the current value of FREQ.

Figure 28:
Frequency Selection

FREQ [1:0] Binary	Read/Write	Frequency [kHz]
00	R/W	45.45
01	R/W	71.4
10	R/W	100
11	R/W	125

7.2.8 Sensor Driver Voltage Selection Register (Address 0x22/0x32)

The 0x32 command sets the transmitter output AC voltage (TXV). At power-up, TXV defaults to 0x00. The 0x22 command is used to read the current value of TXV. TXF1 and TXF2 diagnostic bits are not valid when TXV=0x00 or TXV=0x03.

Figure 29:
Sensor Driver Voltage Selection

TXV [1:0] Binary	Read/Write	Output Voltage Peak-Peak [V]
00	R/W	0
01	R/W	0.5
10	R/W	1.0
11	R/W	0

7.2.9 MUX Control Register (Address 0x23/0x33)

The 0x33 command controls the ten 3-channel MUXES connected to the SENx pins. It also controls the 2-channel MUX connected to the VAR_SEN pin. The 0x23 command reads the current data in the channel select control register.

Figure 30:
MUX Control Register

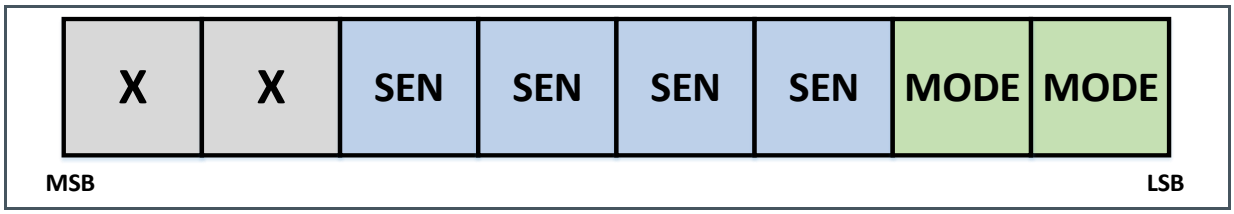


Figure 31:
MUX Control Register Description Settings

Name	Bit Number	Read/Write	Measurement Data
Mode	0:1	R/W	Mode Selection
SEN	2:5	R/W	Channel Selection
X	6:7	R	Not Used

Figure 32:
MUX Register Channel Selection (SEN)

SENx	MUX Selected
0000	SEN0
0001	SEN1
0010	SEN2
0011	SEN3
0100	SEN4
0101	SEN5
0110	SEN6
0111	SEN7
1000	SEN8
1001	SEN9
1010	None
1011	VAR_SEN
1100	None

Figure 33:
MUX Register Mode Selection (MODE)

MODE	SENx Connected To
00	Open
01	Sensor Driver
10	Common Mode through 5 kΩ resistor
11	No Operation

7.2.10 VAR_SEN Gain Selection (Address 0x24/0x34)

The VAR_SEN Driver Attenuator is used to scale down the VAR_SEN amplitude. The VAR_SEN amplitude is always related to the Sensor driver amplitude

Figure 34:
VAR_SEN Gain Selection

Current Buffer Gain	Program Parameter	Min	Typ	Max	Unit
SDG=0	00	.	1	.	V/V
SDG=1	01	0.931	0.95	0.969	V/V
SDG=2	10	0.882	0.9	0.918	V/V
SDG=3	11	0.833	0.85	0.867	V/V

7.2.11 Current Buffer Gain Selection (Address 0x25/0x35)

For the conversion from current to voltage, a trans-impedance amplifier is implemented. The upper range will be extended by programmable scaling factors.

Figure 35:
Current Buffer Gain Settings

Current Buffer Gain	Program Parameter	Min	Typ	Max	Unit
CBG=0	00	16.2	18	19.8	kOhm
CBG=1	01	8.1	9	9.9	kOhm
CBG=2	10	4.05	4.5	4.95	kOhm

Current Buffer Gain	Program Parameter	Min	Typ	Max	Unit
CBG=3	11	2.02	2.25	2.47	kOhm

7.2.12 Demodulation Clock Selection (Address 0x26/0x36)

In this register, you can set the demodulation clock frequency for I and Q-path

Figure 36:
DCLK Settings

DCLK Value	Program Parameter	Upper Path		Lower Path	
		Signal Clock	Clock Phase	Signal Clock	Clock Phase
DCLK=0	00	ICLK	In phase	QCLK	In phase
DCLK=1	01	QCLK	In phase	ICLK	In phase
DCLK=2	10	ICLK	180° out of phase	QCLK	180° out of phase
DCLK=3	11	QCLK	180° out of phase	ICLK	180° out of phase

7.2.13 PGA Voltage Gain Control (Address 0x27/0x37)

The 0x37 command sets the PGA voltage gain. This 3-bit number (PGA [2:0]) adjusts the input voltage level to the ADC to optimize its conversion resolution. The 0x27 command reads the PGA value. At power-up, PGA defaults to 0x00.The PGA is defined as an inverted amplifier.

Figure 37:
PGA Settings

PGA Value	PGA [2:0] Binary	Read/Write	PGA Gain
PGA_0	000	R/W	36
PGA_1	001	R/W	24
PGA_2	010	R/W	16
PGA_3	011	R/W	10.67
PGA_4	100	R/W	7.11
PGA_5	101	R/W	4.74
PGA_6	110	R/W	3.16

PGA Value	PGA [2:0] Binary	Read/Write	PGA Gain
PGA_7	111	R/W	2.11

7.2.14 PGA Offset Control I-Channel (Address 0x28/0x38)

The 0x38 command is used to program the offset DACs for the I-channel.

This offset compensates for the parasitic offsets in the sensor system and allows to shift DC operating point in order to maximize the ADC range. The 0x28 command reads the current values of OFFSET1. DAC outputs can be set to 256 settings (VREG/256) between GND and VREG. (8-bit)

The Offset DAC is used to change the DC operating point of the ADC input. Increasing the Offset DAC value one count will decrease the ADC input by 80 counts before the accumulation.

7.2.15 PGA Offset Control Q-Channel (Address 0x29/0x39)

The 0x39 command is used to program the offset DAC for the Q-channel.

This offset compensates for the parasitic offsets in the sensor system and allows to shift DC operating point in order to maximize the ADC range. The 0x29 command reads the current values of OFFSET2. DAC outputs can be set to 256 settings (VREG/256) between GND and VREG. (8-bit)

The Offset DAC is used to change the DC operating point of the ADC input. Increasing the Offset DAC value one count will decrease the ADC input by 80 counts before the accumulation.

7.2.16 ADC Control Register (Address 0x2A/0x3A)

The 0x3A command controls the ADC converter cycles. The 0x2A command reads out the ADCTL register.

Figure 38:
ADCTL Register Overview

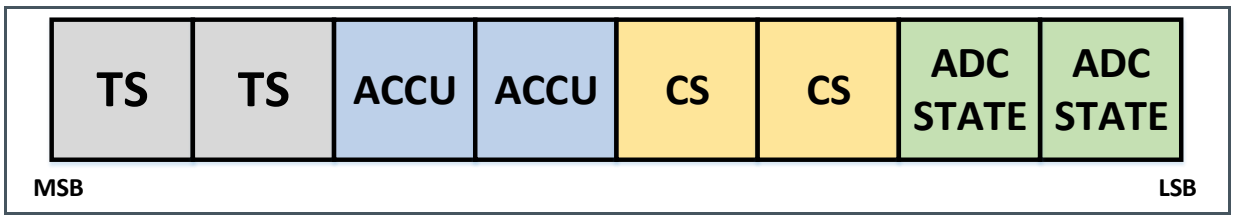


Figure 39:
ADC Settings

Name	Bit Number	Read/Write	Description
TS	6:7	R/W	Time selection
ACCU	4:5	R/W	Accumulation setting
CS	2:3	R/W	Clock selection
ADC state	0:1	R/W	ADC state selection

ADCTL [7:6] selects how many MCLK clock cycles are used to define the settling phase for the analog front end (AFE).

Figure 40:
MCLK Frequency Setting

ADCTL [7:6] Binary	System Settling Time in Periods	Time [µs]
00	1600 MCLK_p	400
01	2304 MCLK_p	576
10	2656 MCLK_p	664
11	1600 MCLK_p	400

ADCTL [5:4] selects how many samples are accumulated for each I and Q channel. Dependent on how many samples are calculated the I and Q Data varies between 12 & 14-bit. 4 samples = 12-bit, 8 samples = 13-bit, 16 samples = 14-bit

Figure 41:
Accumulation Samples Setting

ADCTL [5:4] Binary	Number of Samples Calculated for I and Q Channel
00	4
01	8
10	16
11	4

ADCTL [3:2] selects the ADC clock frequency.

Figure 42:
ADC Frequency Setting

ADCTL [3:2] Binary	System Settling Time in Periods	ADCLK Frequency [kHz]
00	16 * MCLK_p	250
01	8 * MCLK_p	500
10	4 * MCLK_p	1000
11	16 * MCLK_p	250

ADCTL [1:0] selects the ADC state

Figure 43:
ADC State

ADCTL [1:0] Binary	ADC State
00	RESET of DSP and ADC stop
01	Start single conversion
10	Start continuous conversions
11	Stop current conversions

Figure 44:
ADCTL vs System Timing

ADCTL			Selected Settings			System Timing		
Settling [7:6]	Samples [5:4]	Freq [3:2]	Settling Time (µs)	Number of I/Q Samples	ADC I/Q Sample Rate (kHz)	Settling Time (µs)	ADC Sampling Time (µs)	Total Time (µs)
00	00	00	400	4	11.36	400	352	752
00	00	01	400	4	22.73	400	176	576
00	00	10	400	4	45.45	400	88	488
00	01	00	400	8	11.36	400	704	1104
00	01	01	400	8	22.73	400	352	752
00	01	10	400	8	45.45	400	176	576
00	10	00	400	16	11.36	400	1408	1808

ADCTL			Selected Settings			System Timing		
Settling [7:6]	Samples [5:4]	Freq [3:2]	Settling Time (µs)	Number of I/Q Samples	ADC I/Q Sample Rate (kHz)	Settling Time (µs)	ADC Sampling Time (µs)	Total Time (µs)
00	10	01	400	16	22.73	400	704	1104
00	10	10	400	16	45.45	400	352	752
01	00	00	576	4	11.36	576	352	928
01	00	01	576	4	22.73	576	176	752
01	00	10	576	4	45.45	576	88	664
01	01	00	576	8	11.36	576	704	1280
01	01	01	576	8	22.73	576	352	928
01	01	10	576	8	45.45	576	176	752
01	10	00	576	16	11.36	576	1408	1984
01	10	01	576	16	22.73	576	704	1280
01	10	10	576	16	45.45	576	352	928
10	00	00	664	4	11.36	664	352	1016
10	00	01	664	4	22.73	664	176	840
10	00	10	664	4	45.45	664	88	752
10	01	00	664	8	11.36	664	704	1368
10	01	01	664	8	22.73	664	352	1016
10	01	10	664	8	45.45	664	176	840
10	10	00	664	16	11.36	664	1408	2072
10	10	01	664	16	22.73	664	704	1368
10	10	10	664	16	45.45	664	352	1016

7.2.17 Diagnostic Blanking Register (Address 0x2B/0x3B)

The 0x3B command is used to program the 6-bit register up/down counter used for blanking diagnostics. A diagnostic is not reported in the Status Register until the Up/Down Counter has reached the programmed terminal value (BLANK).

7.2.18 Diagnostic MUX Control (Address 0x2C/0x3C)

The 0x3C command is used to control the pin-to-pin short diagnostic MUX. This register is made up of two 4-bit registers PLUS[3:0] and MINUS[3:0]. PLUS controls the pin connected to the positive side of the comparator, MINUS to the negative side. The default value at POR is 0x00FF (all pin-to-pin short MUXes are OFF).

Figure 45:
Diagnostic Mux Control Register

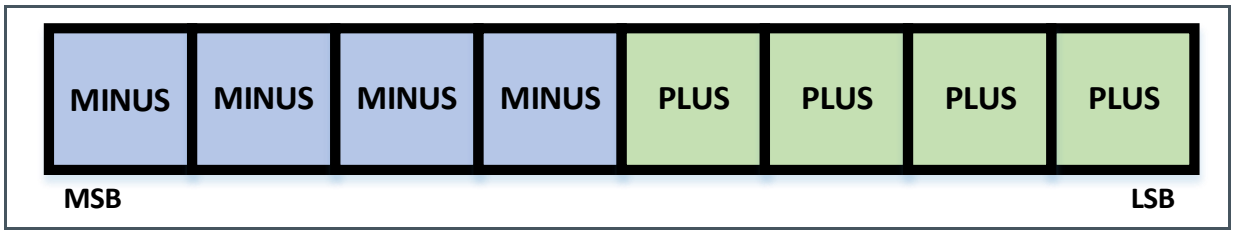
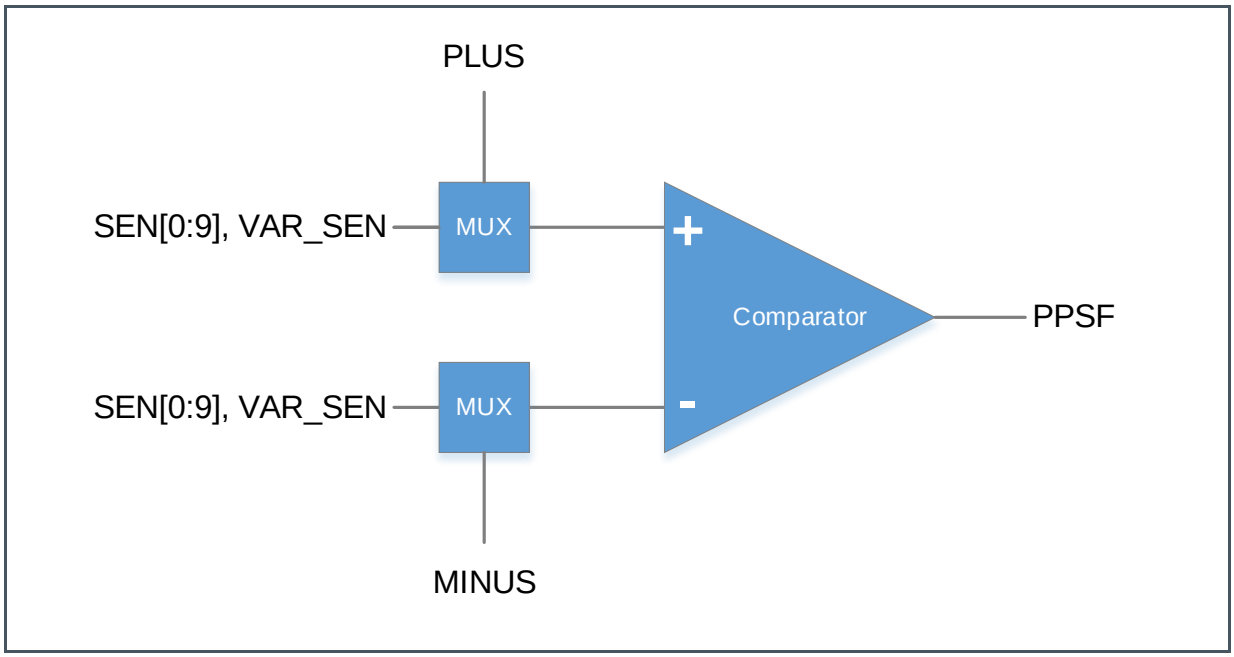


Figure 46:
MUX Diagnostics Control

PLUS/MINUS [3:0] Binary	Read/Write	Pin Connected to Comparator
0000	R/W	SEN0
0001	R/W	SEN1
0010	R/W	SEN2
0011	R/W	SEN3
0100	R/W	SEN4
0101	R/W	SEN5
0110	R/W	SEN6
0111	R/W	SEN7
1000	R/W	SEN8
1001	R/W	SEN9
1010	R/W	NONE

PLUS/MINUS [3:0] Binary	Read/Write	Pin Connected to Comparator
1011	R/W	VAR_SEN
1100	R/W	NONE
1101	R/W	NONE
1110	R/W	NONE
1111	R/W	NONE (default)

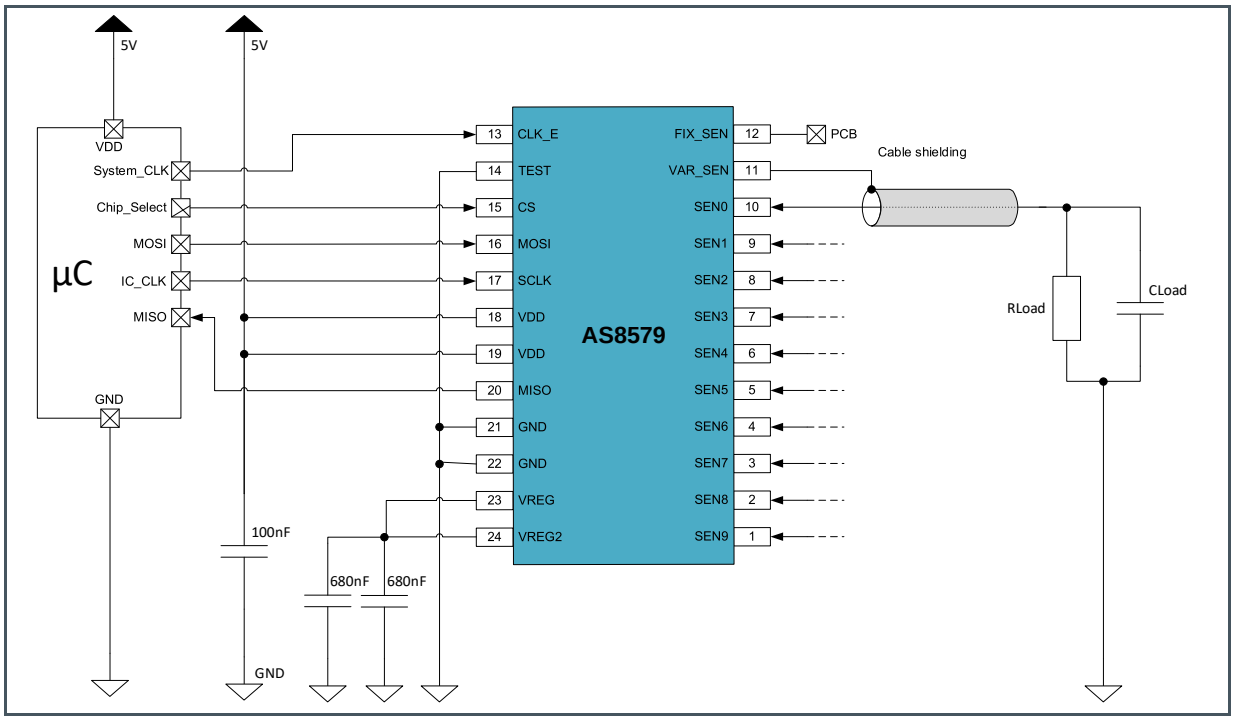
Figure 47:
Diagnostic MUX Control



8 Application Information

8.1 Typical Application Circuit

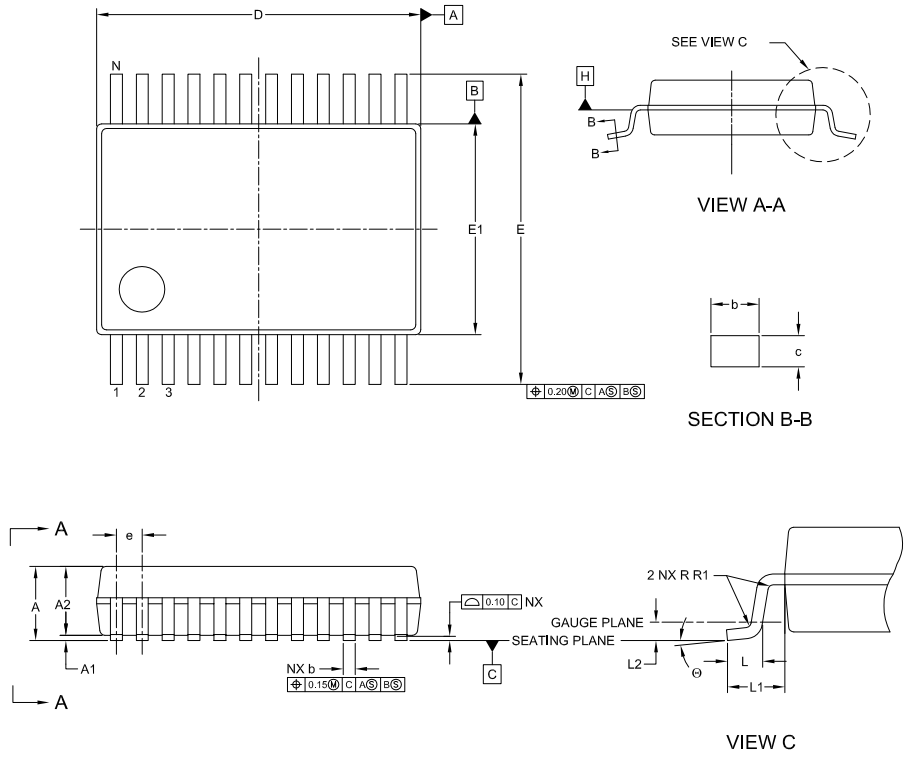
Figure 48:
Typical Application Circuit



The pin FIX_SEN is connected to the PCB that carries the AS8579. The VAR_SEN pin is connected to the shielding of the Sensor cable.

9 Package Drawings & Markings

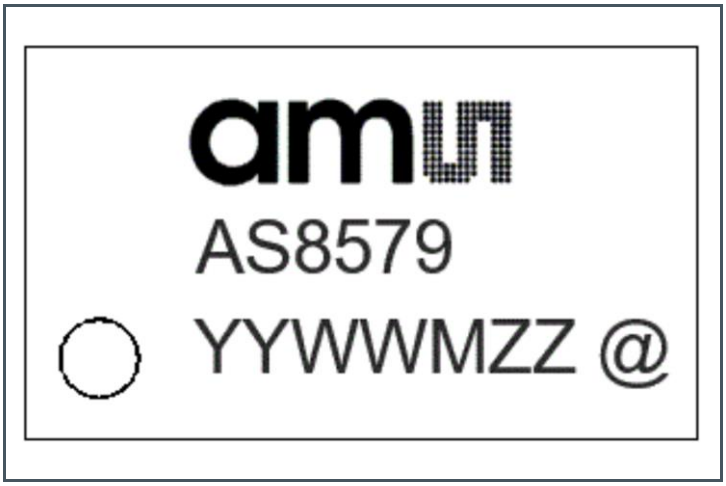
Figure 49:
SSOP24 Package Outline Drawing



Ref.	Min	Nom	Max
A	1.73	1.86	1.99
A1	0.05	0.13	0.21
A2	1.68	1.73	1.78
b	0.22	0.30	0.38
c	0.09	0.17	0.25
D	7.90	8.20	8.50
E	7.40	7.80	8.20
E1	5.00	5.3	5.6
e	0.65 BSC		
L	0.55	0.75	0.95
L1	1.25REF		
L2	0.25REF		
R	0.09	-	-
Θ	0°	4°	8°
N	24		

(1) All dimensions are in millimeters. Angles in degrees.
(2) Dimensioning and tolerancing conform to ASME Y14.5M-1994.
(3) N is the total number of terminals.
(4) This package contains no lead (Pb).
(5) This drawing is subject to change without notice.

Figure 50:
AS8579 Package Marking/Code



YY	Manufacturing Year
WW	Manufacturing Week
M	Assembly Plant Identifier
ZZ	Assembly Traceability Code
@	Sublot Identifier

10 Revision Information

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams-OSRAM AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams-OSRAM AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Changes from previous version to current revision v4-01	Page
Changes from v3-00 to v4-00	
Updated Figure 2	4
Changes from v4-00 to v4-01	
Updated comments for ESD_CDM, Figure 5	8