

GET TO KNOW THE NXP ROBUST MPU PORTFOLIO, WITH SPOTLIGHTS ON i.MX 8ULP CROSSOVER APPLICATIONS PROCESSOR

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MAY 2023



SECURE CONNECTIONS
FOR A SMARTER WORLD

PUBLIC

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ADVANCING EDGE PROCESSING FOR IoT

NXP unveils advanced i.MX applications processors with easy-to-deploy security and energy efficiency for the industrial and IoT Edge



EDGELOCK[®]
SECURE ENCLAVE

ENERGY FLEX
ARCHITECTURE

i.MX 8ULP FAMILY

i.MX 9 SERIES

i.MX 8ULP SOC

Very Low Power processing for use cases demanding a longer battery life

- FD-SOI 28nm Process Technology
- IP selection
- Heterogeneous architecture
- Low Power Mode enablement

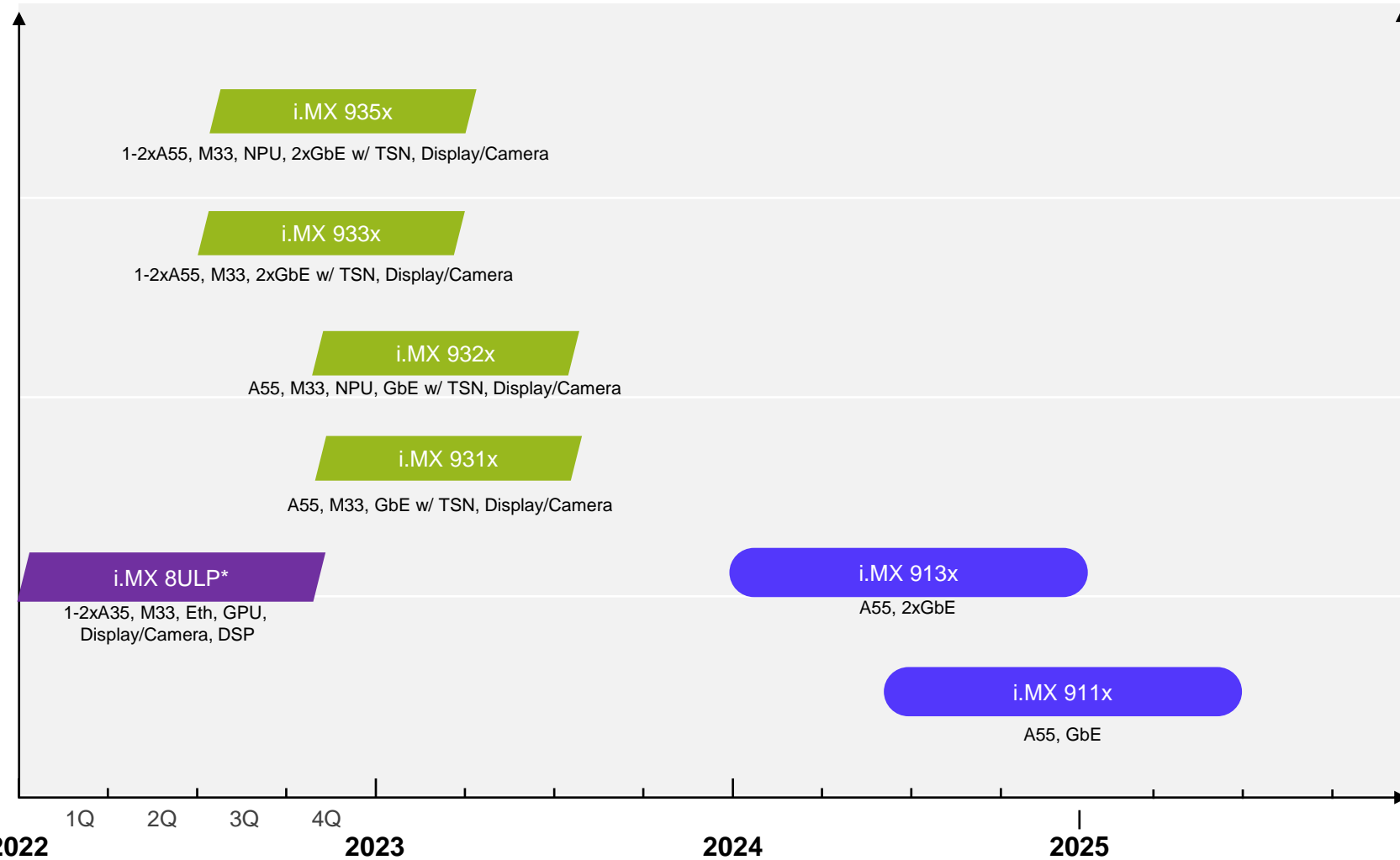
Arm® CORTEX® - A35
Arm® CORTEX® - M33

ENTRY-LEVEL i.MX APPLICATIONS PROCESSORS FOR EDGE PROCESSING

NDA Required
Preliminary, Subject to Change

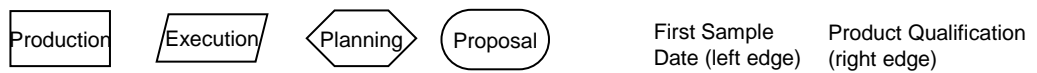
Compute Performance

- i.MX 8M NanoUL**
4xA53, M7, Camera
 - i.MX 7Dual**
2xA7, M4, 2xGbE, PCIe, Display/Camera
 - i.MX 7Solo**
A7, M4, GbE, Display/Camera, PCIe
 - i.MX 7ULP**
A7, M4, GPU, Display/Camera
 - i.MX 6UL**
A7, 2xEth, Automotive
 - i.MX 6ULL**
A7, 2xEth, Display/Camera
 - i.MX 6ULZ**
A7
- Production Now**

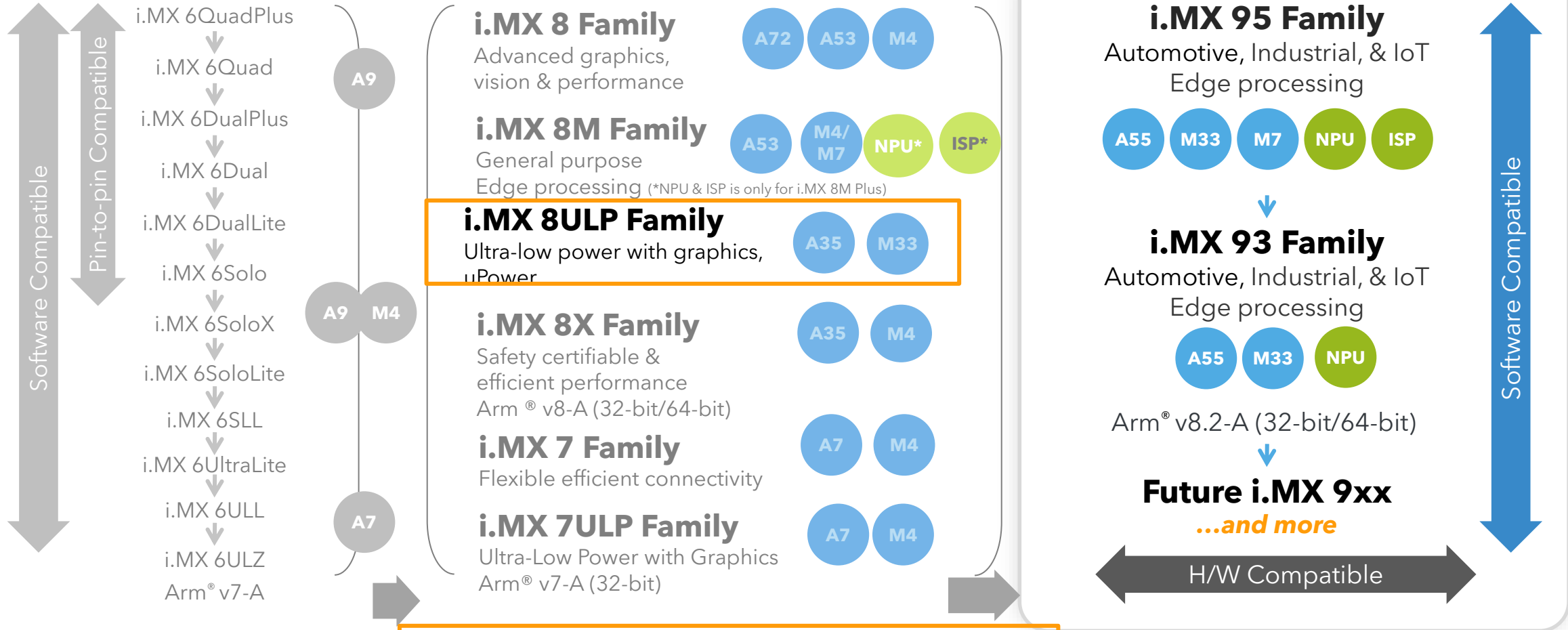


- Performance & Multimedia**
- Edge Aware**
- Energy Efficient States**
- Advanced Security**
- Scalable Platform**

NXP 15yr Product Longevity Program
* Alpha Sampling (now)



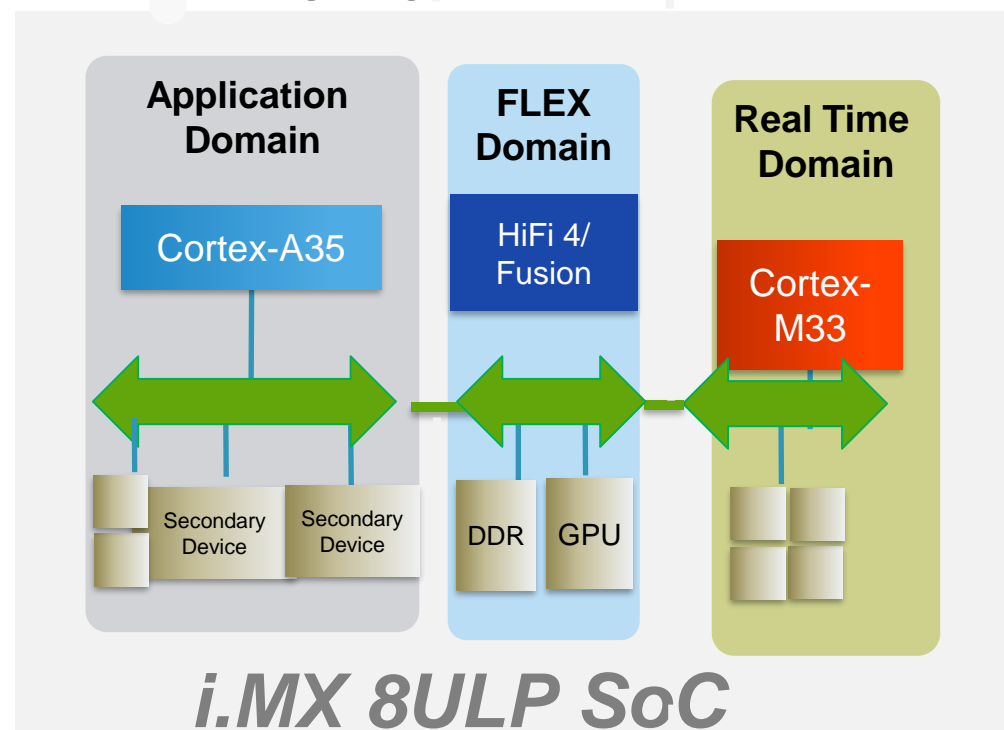
i.MX SERIES OF APPLICATIONS PROCESSORS



- Power Efficiency, First & Foremost (RVT v. LVT)
- Always choosing Low Power Connectivity
- Seeking Lowest Leakage Architecture and Technology

LEVERAGING MPU, MCU, DSP IN ONE DEVICE AND ADDING MORE FLEXIBILITY

- Each domain can be independently powered off, so that it only consumes power when needed:
 - **Application Domain** contains main high-performance application cores. Includes fine-grained control of number and operating frequency.
 - **Flex Domain** includes multimedia and neural processing accelerators
 - **Real Time Domain** includes low-power real-time core and peripherals to enable background processes such as wake-word detect to consume very little power.
 - **Peripheral Access** to any peripheral by any domain is allowed through eXtended Resource Domain Control (XRDC)
 - **Secure Communication** between domains is enabled by secure Messaging Units (MUs)



- High Core Processing Performance
- Rich OS support
- NEON Acceleration
- High Bandwidth
- MMU
- H/W MACs
- Support for emerging multi-channel object-based audio standards
- FIR, FFT, IIR acceleration
- Real Time Performance
- Right Sized Processing
- Extreme Low Power Modes

HETEROGENEOUS DOMAIN COMPUTING (HDC)

Shared Topology Split Power Domains... Split Buses...

i.MX 8ULP SOC



APPLICATION DOMAIN

REAL TIME DOMAIN

Arm Processor

On-chip Memory

Ext Mem Support

Security

| | Application processor domain | Real-time processor domain |
|-----------------|---|---|
| Arm Processor | Dual core Cortex®-A35 Frequency up to 900MHz* | Cortex®-M33F Nominal (RUN) frequency: 216 MHz |
| On-chip Memory | 32 KB instruction and 32 KB data cache | 32 KB instruction and 32 KB data cache |
| Ext Mem Support | Floating Point Unit (FPU) | Floating Point Unit (FPU) |
| Security | 512 KB of L2 cache with Snoop Control Unit (SCU) | Memory Protection Unit (MPU) |
| | NEON™ SIMD engine | Co-processor interface for • PowerQuad hardware accelerator (Fixed and floating point +FFT) DSP functions • CASPER Crypto/FFT engine |
| | — | Tensilica DSP Fusion F1 DSP processor Nominal frequency: 200 MHz |
| | 32 channel DMA | 32 channel DMA |
| | 64 KB of RAM | 768 KB of Shared Memory, zero wait state |
| | 192 KB of Boot ROM | 96 KB of Boot ROM |
| | FlexSPI Serial flash interface to quad/octalSPI flash device | Dual FlexSPI Serial flash interface to quad/octalSPI flash device |
| | 3 eMMC/SD host interfaces supporting eMMC5.1 and SD3.0 | — |
| | Cryptographic acceleration supporting • symmetric and asymmetric ciphering algorithms • SHA-256 hashing algorithm | EdgeLock secure enclave (ELka) as Root of Trust (RoT) • Core supporting up-to 216 MHz • Dedicated boot ROM with Advanced High Assurance boot(AHAB) • ECDSA P256 based signature verification • Support for symmetric Cryptographic acceleration (SGI) • Support for Asymmetric Cryptographic acceleration (PKC) • NIST compliant RNG with DRBG • PLF(Physically Unclonable Function) based Root Keys as option • One-Time Programmable electrical fuse used for security keys |
| | NIST-approved random number generator | On-The-Fly decryption of the encrypted code stored in external flash device |
| | 32 KB secure RAM | — |

DDR/GPU/DISPLAY/CAMERA/AUDIO

| | |
|--|--|
| External memory interfaces | LPDDR3, LPDDR4, LPDDR4x |
| Graphics, display and Camera Interface | GPU3D • Support for Open GL ES 3.1, Vulkan 1.1, Open CL 2.x and Open VG1.1 GPU2D Composition Processing Core (CPC) GPU 4-lane MIPI DSI interface Dual lane MIPI CSI interface Image Sensing interface (ISI) with one pixel link interface PXP E-Ink Display Engine Display controller (DCNano) that supports EPDC panels through MIPI, Smart Displays and Video mode Can be optionally powered off when not in use |
| Audio peripherals | 2 I2S ports |

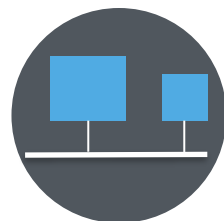
| Application processor domain | Real-time processor domain |
|--|----------------------------|
| 1x Watchdog (WDOG) timer | |
| Low Power Implementation | |
| uPower Sub-system for advanced Power measurement ¹ and control functionality | |
| <ul style="list-style-type: none"> RISC-V ISA compliant CPU core Dedicated code and data RAM Critical path and process monitors to provide device parameters Supports fully automated DVFS (Dynamic Voltage and Frequency Scaling) | |
| Multiple power domains and ultra-low power modes allow flexible power saving | |
| HiFi4 DSP can be power gated while keeping DSP domain operational for Voice trigger | |

BRINGING TOGETHER APPLICATIONS PROCESSOR PERFORMANCE AND MCU LOW POWER WITH DSP EFFICIENCY



Rich 3D and 2D Graphics

- **GC7000 nanoULTRA**
 - OpenGL ES 2.0/1.1
 - OpenVG 1.1
- **GC320 2D Composition**
 - Offloads tasks from 3D GPU
 - Stretch/Shrinking, rotation, GUI processing



Heterogeneous Computing

- **Multiple software execution:**
 - Powerful processing using **Arm® Cortex®-A35** and
 - Real-time perf with Cortex-M33
 - **Dual DSP enablement**
 - **Hif4** – High performance
 - **Fusion** – low power
- **System integrity and security**
 - Resource Domain Controller
 - Fast Low Power Boot
 - Safe Recovery of Application domain



Power Efficiency

- **FDSOI**
 - Effective control of the transistor channel through biasing
- **High Performance/mW** extending battery life for portable devices.
- **Performance on Demand** with fast wake up times

LOW POWER (EXAMPLES) AND HETEROGENOUS COMPUTING CONCEPT

Standby Power : 1mW << lowest among comparable MPUs in the market

• The use case is as follows:

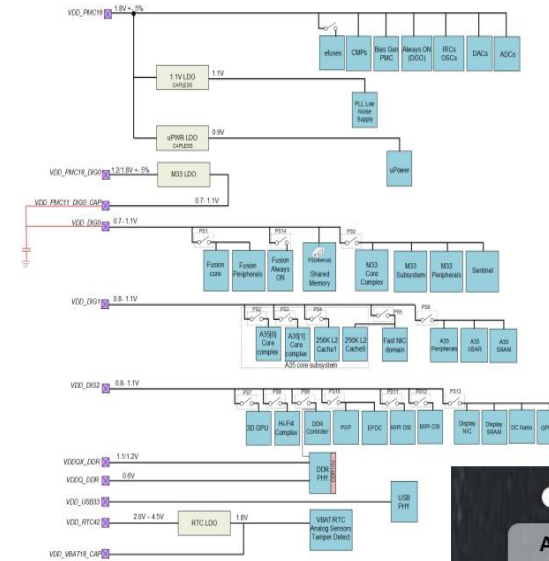
- 1. APD in Power Down mode (Linux enter suspend)
- 2. LPAV in Power Down mode with DDR in self-refresh mode
- 3. RTD in Power Down mode (M33 SDK enter power down with LPTMR as wakeup source)
- Smart watch, wearables, portables, eReader, Gateway, sensor hub, Low power voice, wake word, HMI – low power modes

• Wake Time : <50uS

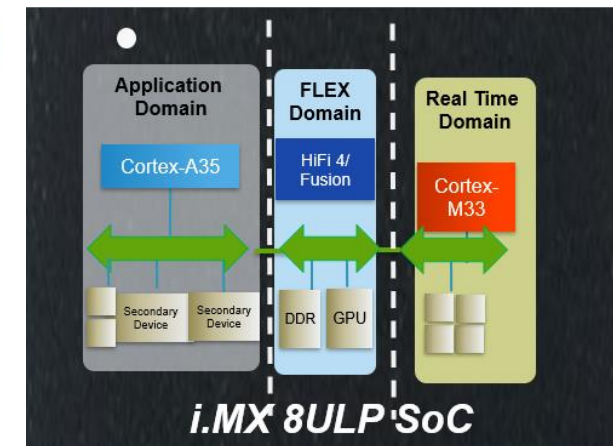
• Suspend Mode: <50mW

- APD in Power Down mode (Linux enter suspend), LPAV in Power Down mode with DDR in self-refresh mode, RTD in various low power modes.
 - Applications: Smart watch, wearables, portables, eReader, Gateway, Sensor Hub, Low power voice, wake word, HMI low power
- Display : 93mW
- Always on display, APD suspend, M33 display refresh every second
 - Smart Appliances , HMI, Portables, Wearables

TOP LEVEL POWER CONTROL



ENABLED VIA POWER SWITCHING and MODE CONTROL (FDSOI TECHNOLOGY)

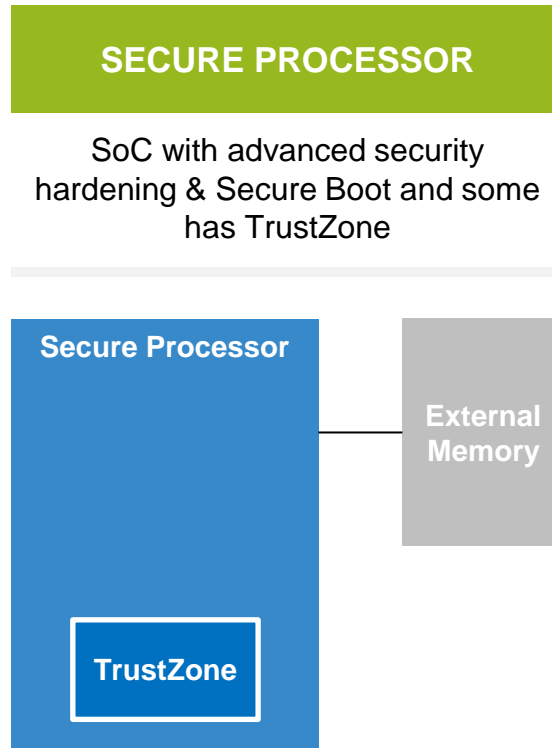
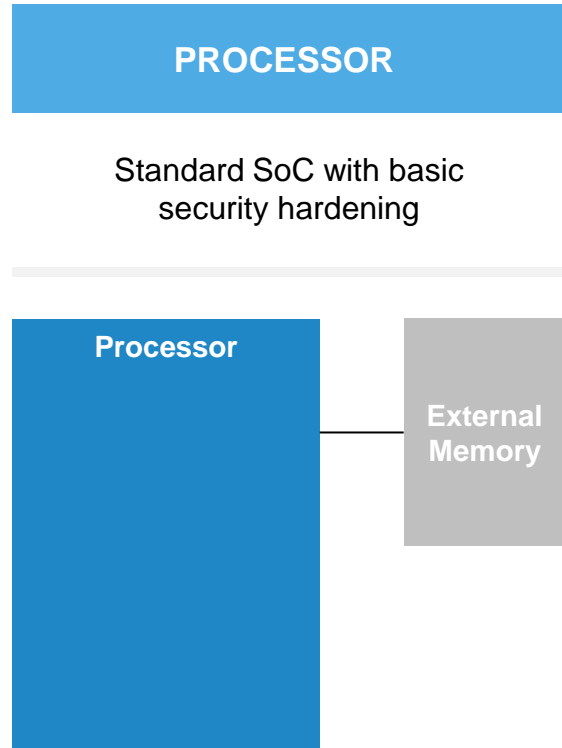


i.MX 8ULP SOC FEATURES AND USE CASES

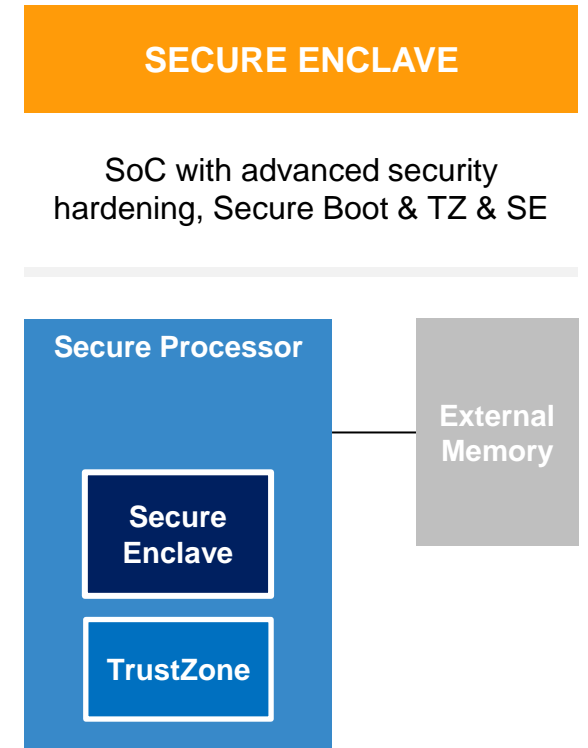
| | i.MX 8ULP* | Description | Examples |
|-----------------------|---|---|---|
| Main CPU | 1x/2xArm® Cortex®-A35 at 800Mhz* (max 900MHz (DVS, OD) | A35 core with several modes (with active biasing offered by the FDSOI technology) | Under Drive with Forward bias is suited for ultra low power |
| MCU | Arm Cortex-M33 @ 216MHz HiFi4/Fusion DSP | Wake from reset possible from M33 , Voice recognition Deep sleep power is 200uW | Lowest power of all the products for wake word detection RTD mode can be in deep sleep |
| DDR | 32-bit LPDDR3/LPDDR4/LPDDR4X, 1.056 GT/s | DDR control possible from LPAV or RTD | This allows a low power mode refresh, which is unique to the ULP family |
| GPU | 3D GPU includes Open GL® ES 3.1, OpenCL™, Vulkan® 2D GPU | High performance Graphics, while maintaining low power | Advanced 3D graphics with 2D accelerator |
| Security | Edge Lock Secure Enclave | The standard security features but with advanced separation of each domain (for low power wake, deep sleep) | Application Security Features Crypto Key storage with Fine Grain Policies Cryptography with Countermeasures Updateable/Customizable |
| AI/ML | A35 | | |
| Vision/Camera | 1x MIPI CSI (2-lane) with PHY | Camera Interface | Suitable for handheld scanners, low power wake , fast wake time |
| Display | 1x MIPI DSI (4-lane) with PHY Up-to 24-bit RGB /DPI) | EPDC , e-Ink Display | Supports displays that are critical for wearables, medical devices, e-readers while maintaining low power modes |
| Video Encode | No HW VPU | - | - |
| Audio | 6x I2S TDM, ASRC, 8ch PDM DMIC input), S/PDIF Tx+Rx | Low power enablement | Very low power wake word |
| High-Speed I/O | 2x USB 2.0 10/100 Ethernet3x SD/eMMC, OctalSPI | IO pins & HS interface | Sufficient for communication with an NXP Wi-Fi SOC such as IW416 |

Notes: A35 Fmax, DVS , OD_{AFBB}. DVS will be available after launch.

NXP SOC SCALABLE SECURITY ARCHITECTURE



i.MX RT1170



i.MX 8ULP

LINUX® POWER NUMBERS: FEBRUARY 2023, HIGHLIGHTS

NDA Required
Preliminary, Subject to Change

| Power_AN_Casename | Description | Measured #s (mW) | Application/customer use-case |
|--|---|------------------|---|
| Suspend Mode | | | APD in Power Down mode (Linux enter suspend),LPAV in Power Down mode with DDR in self-refresh mode, RTD in various low power modes. Smart watch, wearables, portables, eReader, Gateway, sensor hub, Low power voice, wake word, HMI – low power modes are applicable to all system use-cases. |
| Suspend Mode – RTD power down | Suspend to RAM_DSM | 1 | |
| Suspend Mode – RTD active | Suspend Mode RTD active | 54 | |
| Suspend Mode – RTD sleep | Suspend Mode RTD sleep | 46 | |
| Suspend Mode – RTD deep sleep | Suspend Mode RTD deep sleep | 46 | |
| System Idle | | | Modes with fast wake up from Idle mode |
| System Idle with screen on | User idle screen on | 433 | HMI |
| System Idle with screen off | IDLE_DDRC_25MHz | 244 | HMI |
| Core | | | |
| Coremark (Arm recommends Coremark over Dhrystone) | Coremark | 534 | Coremark – multithread set to 2. Reference for use-cases with full CPU loading. |
| core Dhryst + MM07 + HIFI4 + M33 coremark (heavy load) | dhry_hifi_mm07_m33coremark | 772 | Heavy load system use-case for reference – Loading A35, M33, GPU3D and HiFi4. |
| GPU | | | |
| GPU 2D + GPU 3D + CSI/DSI | gpu2d_gpu3d_csi | 723 | Heavy load use-case for reference – simple use-case without heavy loading would be HMI |
| Wake Word | | | |
| Audio | | | |
| Audio Playback | | 424 | Bluetooth speaker, HMI with audio playback. The A35 handles the mp3 audio decoding, and M33 handles the PCM playback through I2S. |
| Display | | | |
| Parallel Eink Page Flip | Parallel Eink Page Flip | 480 | eBook or eReader use-case; EPDC connected to a parallel BB3300-FOC Eink panel |
| Always-on Display, 1fps fresh rate | APD in suspend mode, M33 updating display every second. | 93 | Smart appliance, HMI, portables, wearables |

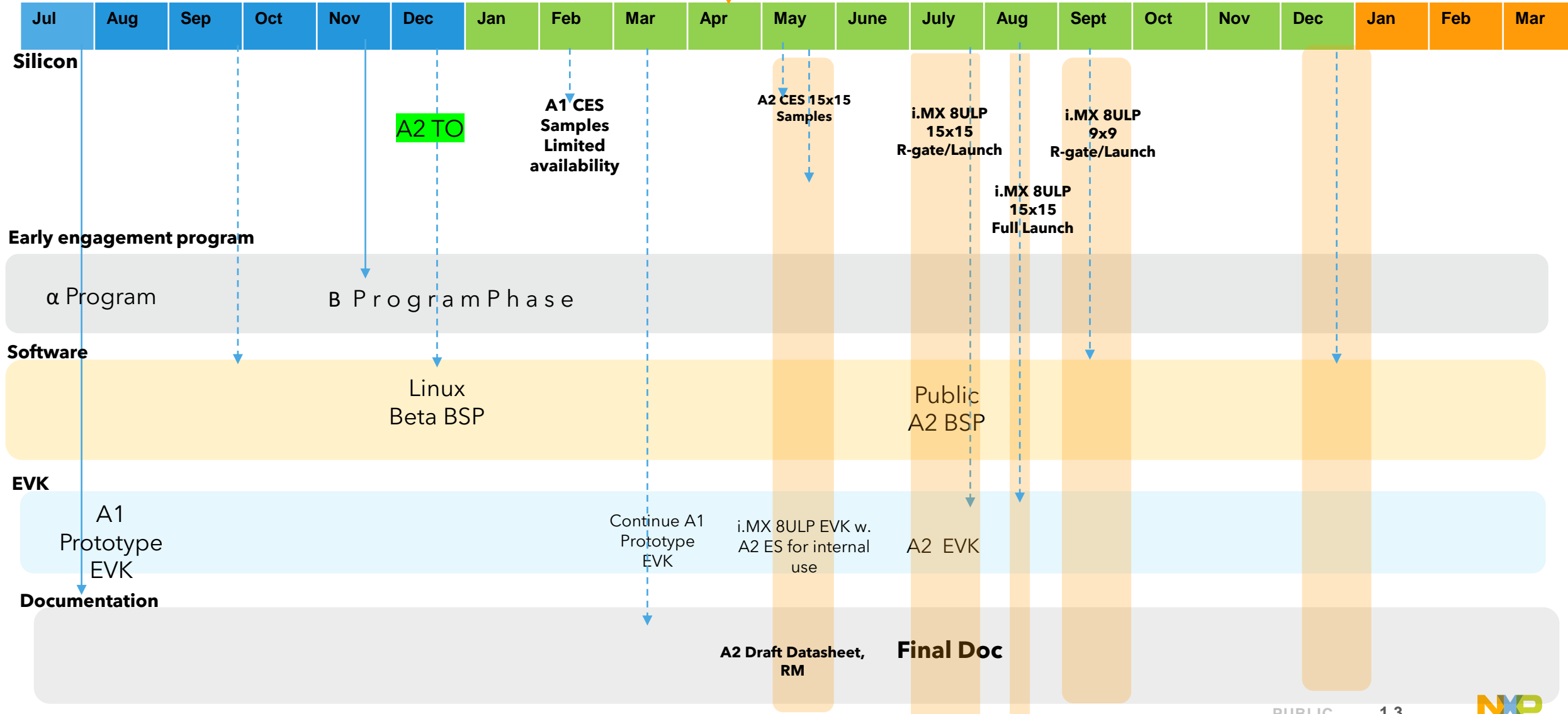
i.MX 8ULP SOC SCHEDULE OVERVIEW

2022

A1 Pre-production

2023

2024



SCHEDULE

Silicon

- A2 Silicon tape-out: Dec 2022 (Done)
- A1 CES (additional) & EVKs: Available now
- A2 Silicon received: Feb 6 , 2023 (Done)
- A2 Early samples: April 2023 (In progress)
- A2 CES (15x15) : May 2023
- A2 R-Gate (15x15): Q2 2023

LAUNCH 15x15 July 2023 (e-commerce active, parts orderable via nxp.com)

Full Market Launch: Aug 15, 2023 (full availability)

A2 CES (9.4x9.4): Early June 2023

- A2 R-Gate (9.4x9.4): August 2023

Full Market launch 9.4x9.4 September 2023 (full availability)

EVKs

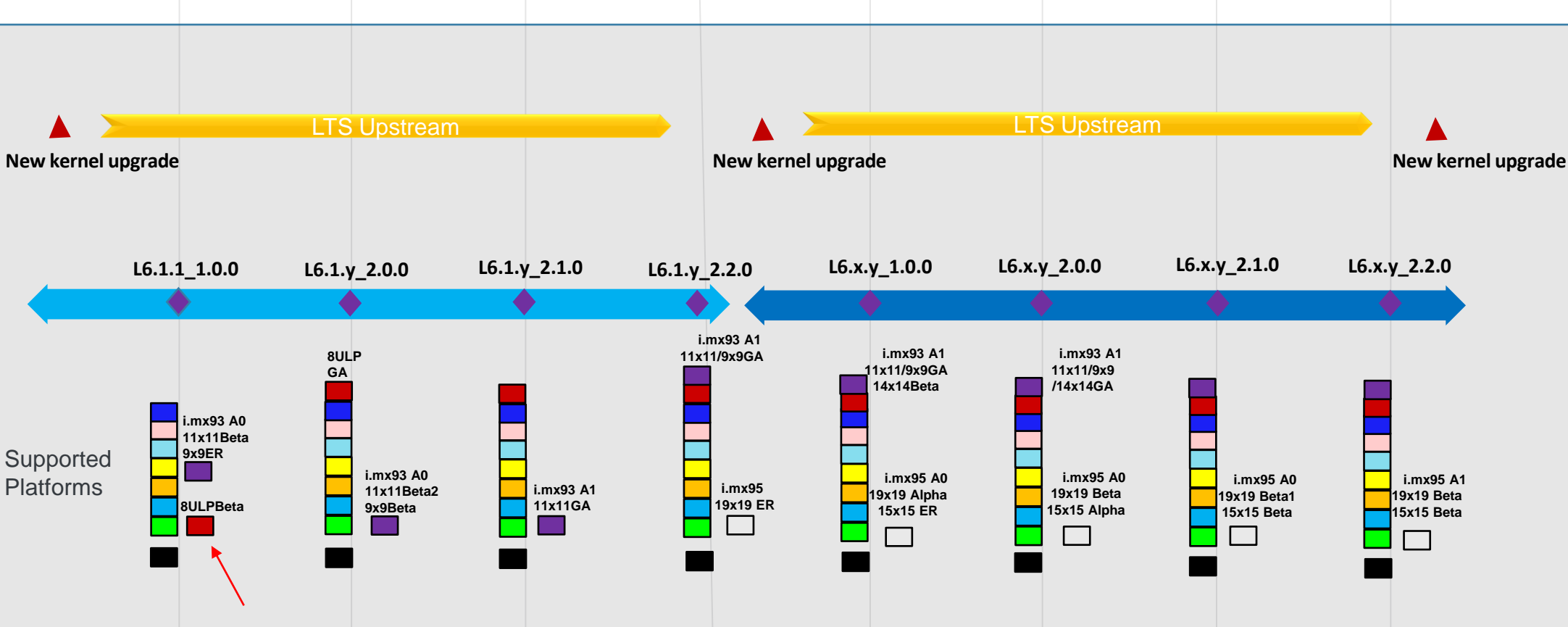
Currently : limited A1 CES based EVK

May 2023 : limited availability with A2 CES

July 2023 : Full availability

BSP/SDK (see next slide)

LINUX® BSP ROADMAP



| Release | Internal Release Date | External Release Date |
|-----------------------------------|-----------------------|-----------------------|
| LF6.1.1_2.0.0/SDK2.13 (Yocto 4.2) | Jun 23 2023 | Jun 30 2023 |
| Android-13.0.0_2.0.0 (L6.1.1) | Jul 24 2023 | Jul 31 2023 |

Legend

- i.MX 8M Nano
- i.MX 8QuadMax, i.MX 8QuadPlus
- i.MX 8DualXLite
- i.MX 8QuadXPlus
- Shipping (i.MX 8M Quad, and i.MX 8M Mini)
- Shipping i.MX 6 and i.MX 7
- Layerscape platforms
- i.MX 8M Plus
- i.MX 8ULP
- i.MX 93
- i.MX 95



i.MX SERIES ANDROID RELEASES 2023

Android 13/14

| Features | Android-13.0.0-1.2.0 | Android-13.0.0-2.0.0 | Android-13.0.0-2.2.0 | Android-14.0.0-1.0.0 |
|-----------------------|--|--|--|--|
| Release | Q1 2023 | Q2 2023 | Q3 2023 | Q4 2023 |
| Android | 13.0 | 13.0 | 13.0 | 14.0 |
| Kernel | 5.15 | 6.1 | 6.1 | 6.1 |
| U-Boot | 2022.04 | 2023.04 | 2023.04 | 2023.04 |
| Graphics | 6.4.3P4.0 | 6.4.11 | 6.4.11 | 6.4.11 |
| Display | MIPI, HDMI, LVDS | MIPI, HDMI, LVDS | MIPI, HDMI, LVDS | MIPI, HDMI, LVDS |
| Audio | ESAI | ESAI | ESAI | ESAI |
| Silicon not supported | i.MX 6 Series i.MX 7 Series | i.MX 6 Series i.MX 7 Series | i.MX 6 Series i.MX 7 Series | i.MX 6 Series i.MX 7 Series |
| Supported Silicon | .i.MX 8QuadMax i.MX 8QuadXPlus I.MX 8M Quad I.MX 8M Mini I.MX 8M Nano I.MX 8M Plus i.MX 8ULP | .i.MX 8QuadMax i.MX 8QuadXPlus I.MX 8M Quad I.MX 8M Mini I.MX 8M Nano I.MX 8M Plus i.MX 8ULP | .i.MX 8QuadMax i.MX 8QuadXPlus I.MX 8M Quad I.MX 8M Mini I.MX 8M Nano I.MX 8M Plus i.MX 8ULP | .i.MX 8QuadMax i.MX 8QuadXPlus I.MX 8M Quad I.MX 8M Mini I.MX 8M Nano I.MX 8M Plus i.MX 8ULP i.MX95 |

i.MX 8ULP TARGET APPLICATIONS

| Industrial/Energy | Consumer | IoT |
|--|---|--|
| <p>Lab electronics</p> <p>Medical electronics</p> <p>EV Chargers</p> <p>Base station</p> <p>Transportation</p> <p>HMI</p> <p>Energy metering</p> | <p>Consumer wearables</p> <p>eReaders</p> <p>2-way Radio</p> <p>Weighing scales</p> <p>Bike Computers</p> | <p>RF ID readers</p> <p>Printers</p> <p>Handheld Scanners</p> <p>Voice enabled devices</p> <p>NFC PoS attach</p> |



AVAILABLE PART NUMBERS (PRODUCTION*) : FULLY ORDERABLE JUNE 2023

| PART NUMBERS OFFERED (MIMX8UxxDxxxxxx)=Consumer (MIMX8UxxCxxxxxx)=Industrial | PKG | CPUs (A-35/M33/HiFi4/DSP) | Display/Camera | Network & Connectivity | Audio |
|--|---------|--------------------------------------|---|---|--|
| MIMX8UD7DVP08SC | 15x15 | 2xA35 , M33,HiFi4/DSP ,3D GPU , EPDC | 1. 4-lane 1x MIPI DSI with PHY Up-to 24-bit RGB /DPI) EPDC & e-Ink support 2. 1 MIPI CS1 | 2x USB 2.0 10/100 Ethernet 3x SD/eMMC, Octal SPI | 6x I2S TDM, ASRC, 8ch PDM DMIC input), S/PDIF Tx+Rx |
| MIMX8UD5DVP08SC | | 2xA35 , M33,HiFi4/DSP ,3D GPU | | | |
| MIMX8UD3DVP08SC | | 2xA35 , M33 | | | |
| MIMX8UD7CVP08SC | | 2xA35 , M33,HiFi4/DSP ,3D GPU , EPDC | | | |
| MIMX8US3DVP08SC | | 1x A35 , M33 | | | |
| MIMX8US5DVP08SC | | 1x A35 , M33,HiFi4/DSP ,3D GPU | | | |
| MIMX8UD3CVP08SC | | 2xA35 , M33 | | | |
| MIMX8UD5CVP08SC | | 2xA35 , M33,HiFi4/DSP ,3D GPU | | | |
| MIMX8US5CVP08SC | | 1x A35 , M33,HiFi4/DSP ,3D GPU | | | |
| MIMX8US3CVP08SC | | 1x A35, M33 | | | |
| MIMX8US5DVK08SC | 9.4x9.4 | 1x A35, M33,HiFi4/DSP ,3D GPU | 1. 2-lane 1x MIPI DSI with PHY Up-to 24-bit RGB /DPI) EPDC & e-Ink support 2. 1 MIPI CS1 | | |
| MIMX8US3DVK08SC | | 1x A35, M33 (consumer) | | | |
| MIMX8UD5CVK08SC | | 2xA35 , M33,HiFi4/DSP ,3D GPU | | | |
| MIMX8UD5DVK08SC | | 2xA35 , M33,HiFi4/DSP ,3D GPU | | | |
| MIMX8UD7DVK08SC | | 2xA35 , M33,HiFi4/DSP ,3D GPU , EPDC | | | |

**A2 (production) SAMPLES
orderable now! AVAILABLE end
of May 2023!**

PIMX8UD7CVP08SC (15x15)

PIMX8UD5DVK08SC (9x9)

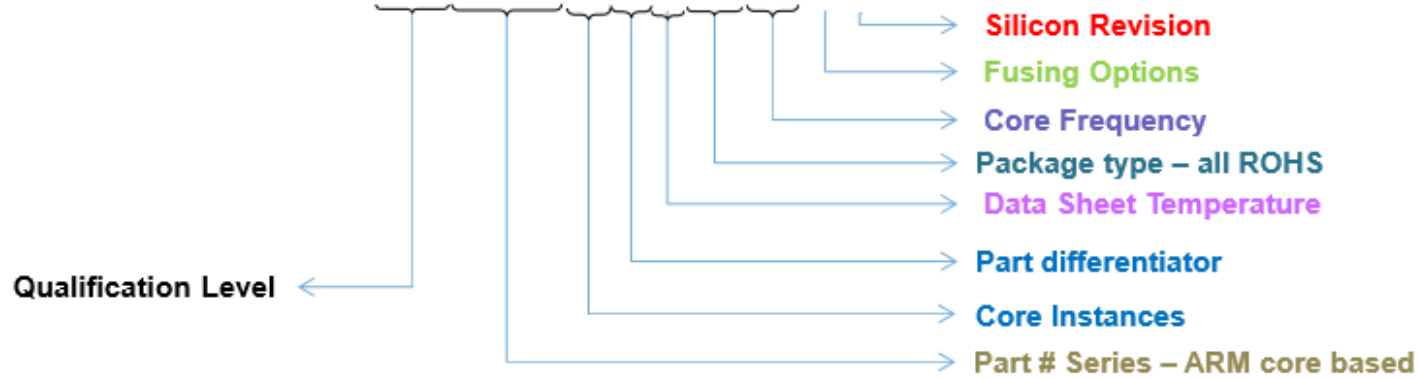
i.MX 8ULP VS. i.MX 932/1/0X COMPARISON

| | i.MX 930x | i.MX 932x/1x * | i.MX 8ULP* | Low power & feature highlights of 8ULP |
|---------------------|--|---|---|---|
| Main CPU | 1x/2x A55 900MHz Arm v8.2-A | 1x/2x A55 900MHz Arm v8.2-A | 1x/2xArm® Cortex®-A35 at 800Mhz | Low power deep sleep with DDR self-refresh |
| MCU | 1x M33 @ 250MHz | 1x M33 @ 250MHz | Arm Cortex-M33 @ 216MHz HiFi4/Fusion DSP (enables ML) | Lowest wake time and optimized voice wake word power |
| DDR | 1.6 GT/s x16 LPDDR4/4X | 1.6 GT/s x16 LPDDR4/4X | 1.06GT/s LPDDR3/LPDDR4/LPDDR4X | DDR self-refresh |
| GPU | 2D: PXP | 2D: PXP | •3D GPU includes Open GL® ES 3.1, OpenCL™, Vulkan® •2D GPU *rich graphics | Advanced Graphics |
| Security | Secure Enclave | Secure Enclave | Secure Enclave | Lowest power entry /exit/ during reset/boot with security enabled |
| Vision | No ISP | No ISP | No ISP | n/a |
| Display | 1080p60 MIPI DSI (4-lane) or 720p60 LVDS (4-lane) or 18-bit parallel RGB | None | 1080p60fps 4-lane MIPI DSI (4-lane) with PHY Up-to 24-bit RGB /DPI) | EPDC , e-Ink Display |
| Camera | MIPI-CS1 2-lane | None | MIPI CSI 2-lane | MIPI CSI 2-lane in all variants |
| Video Decode/Encode | No HW VPU | No HW VPU | No HW VPU | n/a- |
| Audio | 3x I2S TDM, SPDIF Tx+Rx PDM mic, MQS | 3x I2S TDM, SPDIF Tx+Rx PDM mic, MQS | 6x I2S TDM, ASRC, 8ch PDM DMIC input), S/PDIF Tx+Rx | Lowest power Wake word |
| High-Speed I/O | 1x USB 2.0 1x GbE (1 w/ TSN) 3x SD/eMMC <i>*comparable in pricing</i> | 1x USB 2.0 1x GbE (1 w/ TSN) 3x SD/eMMC | 2x USB2.0 10/100 Ethernet 3x SD/eMMC, OctalSPI | 2x USB 2.0 in all versions |

i.MX 8ULP FAMILY PART NUMBER DEFINITION

Preliminary

MIMX8U&@+PK\$\$%A



| Qualification Level | MC |
|---------------------|----|
| Samples | P |
| Mass Production | M |
| Special | S |

| Core instances | & |
|----------------|---|
| 2 x Cortex-A35 | D |
| 1 x Cortex-A35 | S |

| Temperature Tj | + |
|--------------------------|---|
| Consumer: 0 to +95C | D |
| Industrial: -40 to +105C | C |

| Frequency | \$\$ |
|-----------|------|
| 700 MHz | 07 |
| 800 MHz | 08 |
| 1GHz | 10 |

700M, 1G will not be offered

| Part # Series | |
|---------------|--------------------------------|
| IMX8U | i.MX 8ULP |
| IMX8L | i.XM 8ULP Lite: 384KB RTD SRAM |

| Part differentiator | @ |
|---------------------------|---|
| Full Featured | 7 |
| No DSPs | 6 |
| No EPDC | 5 |
| No GPU, No EPDC, no Hifi4 | 3 |

| Package Type | PK |
|---------------------|----|
| MAPBGA 15x15 0.5mm | VP |
| MAPBGA 9.4 x9.4.5mm | VK |

| Fusing | % |
|-------------------------------|---|
| NXP Secure Enclave Enabled | S |
| Pluton enabled secure enclave | A |

A needs to be removed

| Silicon Rev | A |
|-------------|---|
| Rev A0 | A |
| Rev A1 | B |

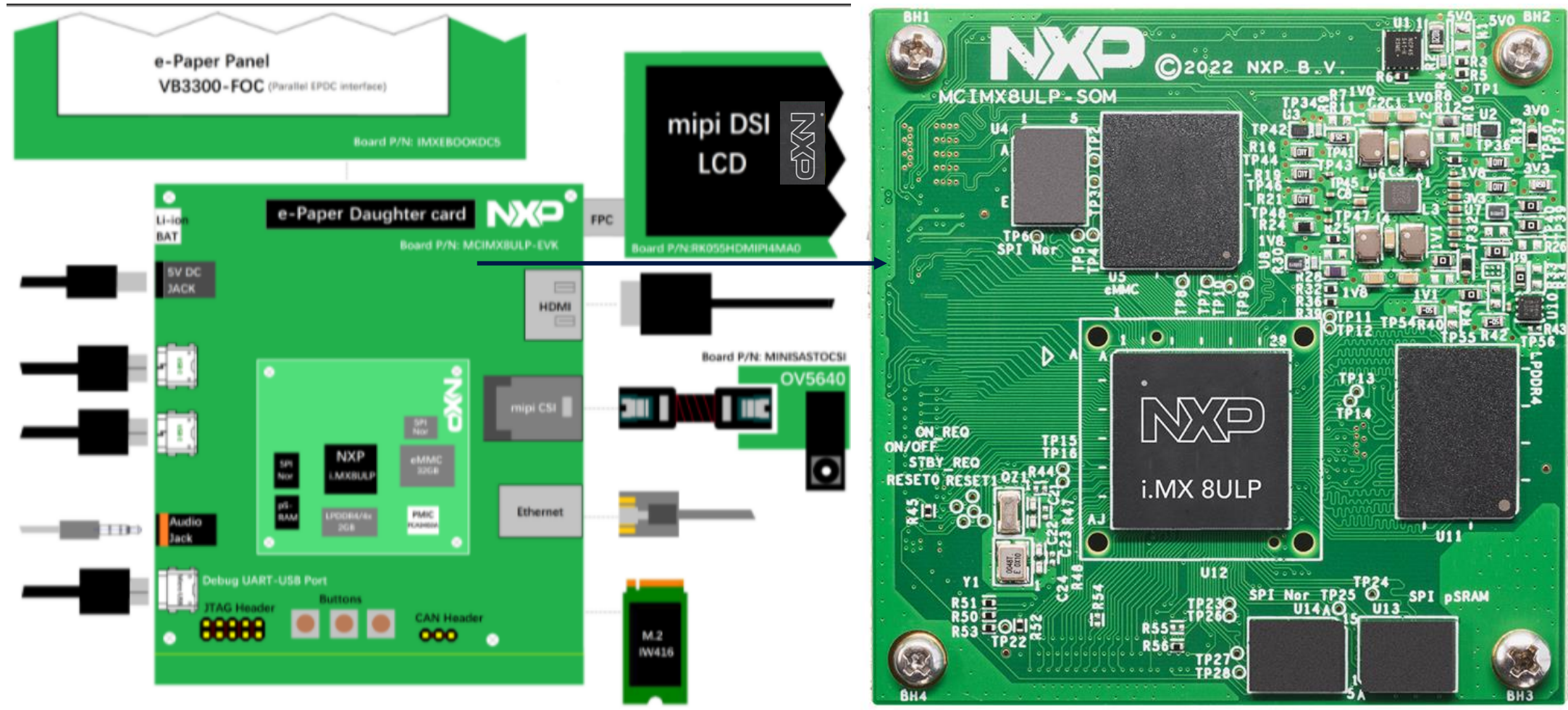
Rev A2 = C



8L will not be offered, but we will provide an app note if lower RTD SRAM is desired



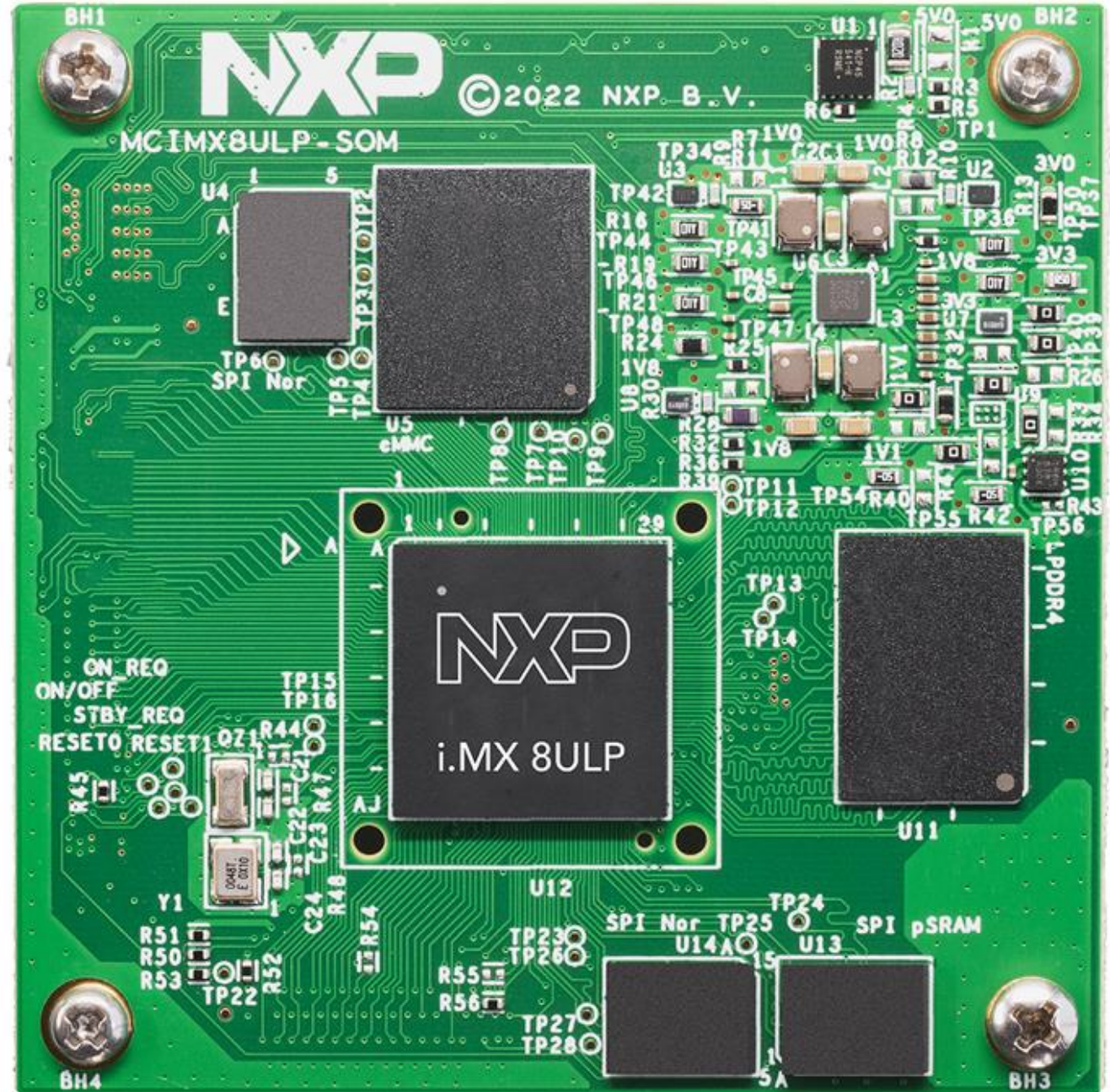
ACCESSORIES – MIPI-DSI PANEL, E-PANEL (RENAMED) , MIPI-CSI SUPPORT



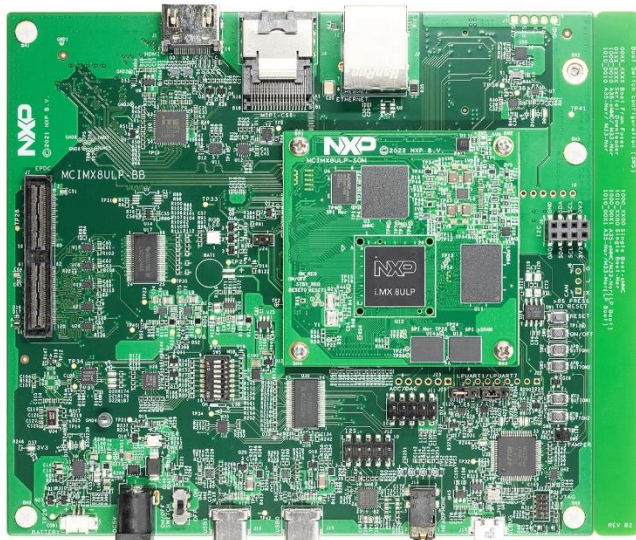
display P/N : VB3300- FOC , panel P/N in NXP :IMXEBOOKDC
Camera : MINISASTOCSI /OV5640

i.MX 8ULP EVK

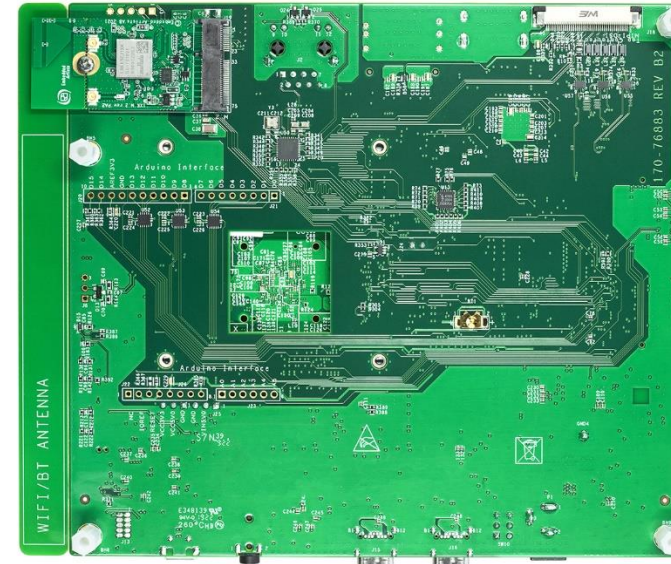
- Part # : MCIMX8ULP-EVK
- Enables fast use case evaluation through quick builds of dips customized base boards.
- Allows customers to leverage the critical features of SOM design including DDR and PMIC design/layout.
- M.2 Wi-Fi module included
- Arduino expansion socket
- Design Files provided
 - Schematics
 - Layout
 - BOM



FRONT AND BACK



FRONT

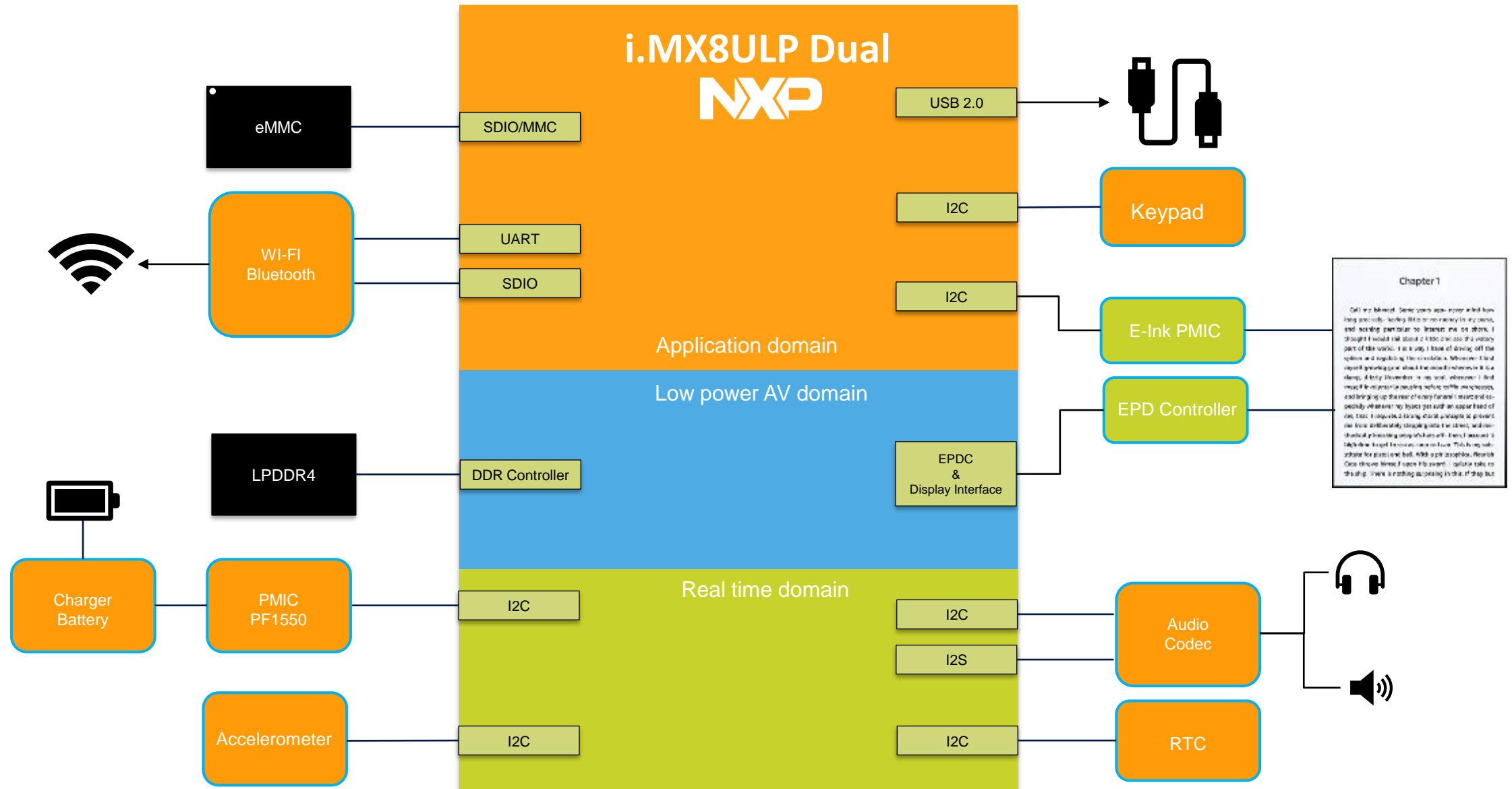


BACK



- Display panel P/N in NXP :IMXEBOOKDC
- Camera : MINISASTOCSI /OV5640

GENERIC E-READER BLOCK DIAGRAM



EBS Partners



SECURE CONNECTIONS
FOR A SMARTER WORLD

PUBLIC

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PARTNERS



Note: Press "Control" and click on image

Power Management IC



SECURE CONNECTIONS
FOR A SMARTER WORLD


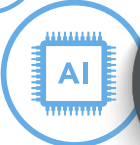
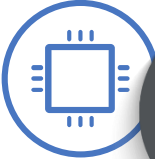




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POWER MANAGEMENT SOLUTIONS FOR NXP MCUS, MPUS, AND CROSSOVER DEVICES

REDUCED SOLUTION SIZE
INCREASED PERFORMANCE
QUICK TIME TO MARKET

-   **Industrial Temp Rated and Longevity Matched**
 - Industrial and Auto Temperature Rated
 - Longevity matched between Processor and Power
-  **Packages to Suit Application**
 - Low profile CSP
 - Robust QFN and BGA
 - Automotive friendly packages
-   **Power for the Whole System**
 - Multiple Rails To Support System Requirements
 - Scalable solutions using VR+ PMIC
-   **Battery Management**
 - Battery Charger and gauging functionality
 - Small solution size and high eff/Low Iq

CO-DESIGNED

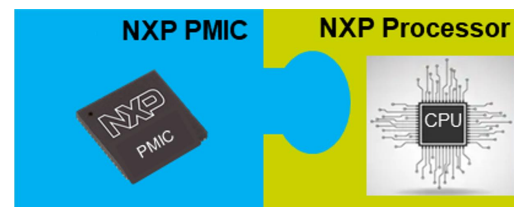
Co-designed keeping the end application in mind unlocking the performance

VALIDATED

Thoroughly validated together and supported by NXP throughout the customer lifecycle

SYSTEM LEVEL SUPPORT

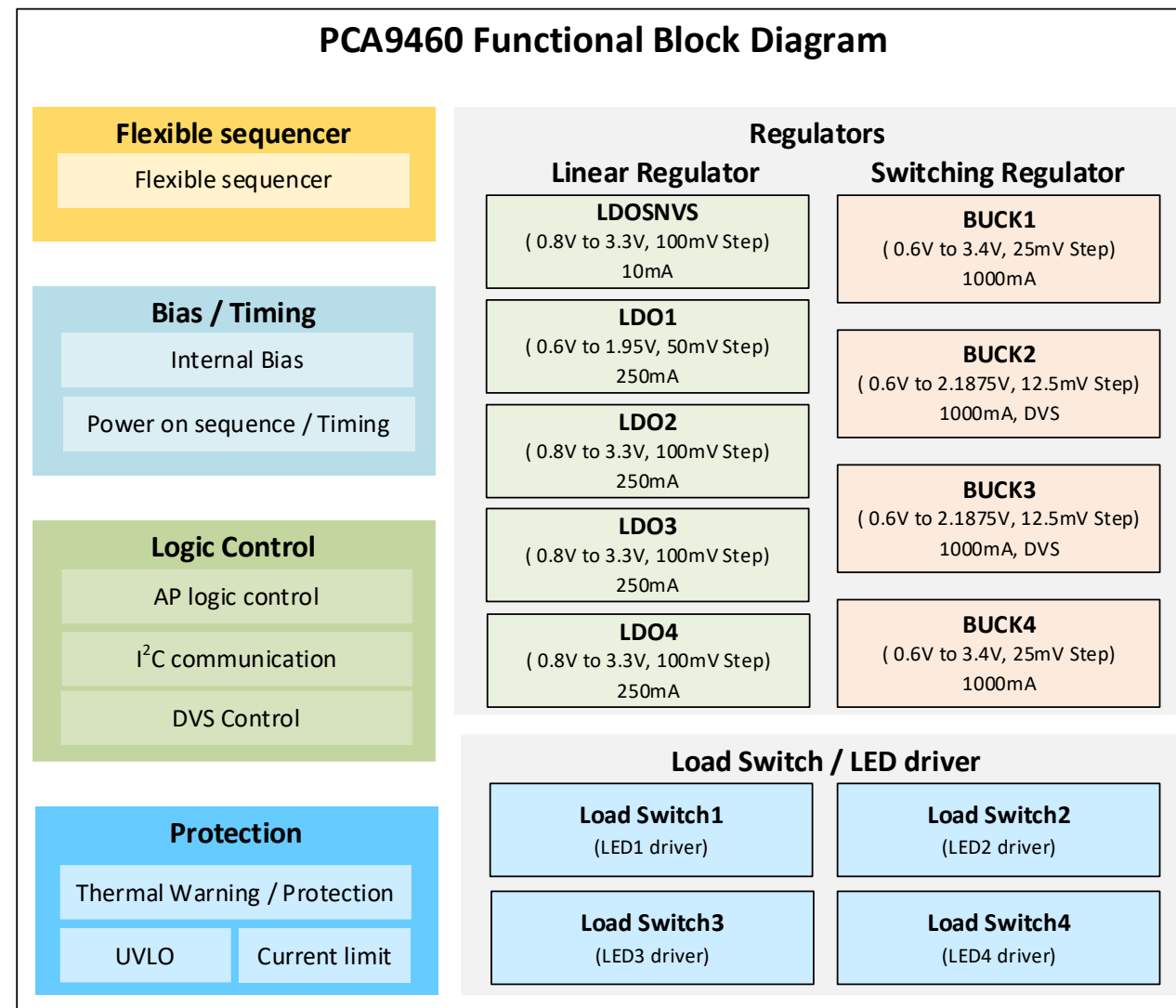
Often include system-level power support such as battery management, safety rating



PCA9460 PMIC (FOR I.MX 8ULP PROCESSOR)

Features List:

- **Four low Iq buck regulators**
 - 2 x 1 A buck regulators supporting DVS
 - 2 x 1 A general purpose buck regulators
 - Quiescent current:
 - 1 μ A low power mode
 - 5 μ A in normal mode
 - Smart DVS control
- **Five low Iq LDOs**
 - 1x 10 mA LDO
 - 4x 250 mA LDOs
 - 0.5 μ A quiescent current
- **Four load switches rated for**
 - 1.2 V ~ 5.5 V
 - 100 m Ω RDSON.
- Chip standby current = 10 μ A (typ)
- Flexible power up/down sequence
- Logic signals support 1.8 V I/O control
- Thermal protection
- 6 x 7 bump array, 0.4 mm pitch, WL-CSP, 2.86 x 2.46 mm
- KIT-PCA9460-EVB EVK: available



IN PRODUCTION

EXAMPLES OF TARGET APPLICATIONS

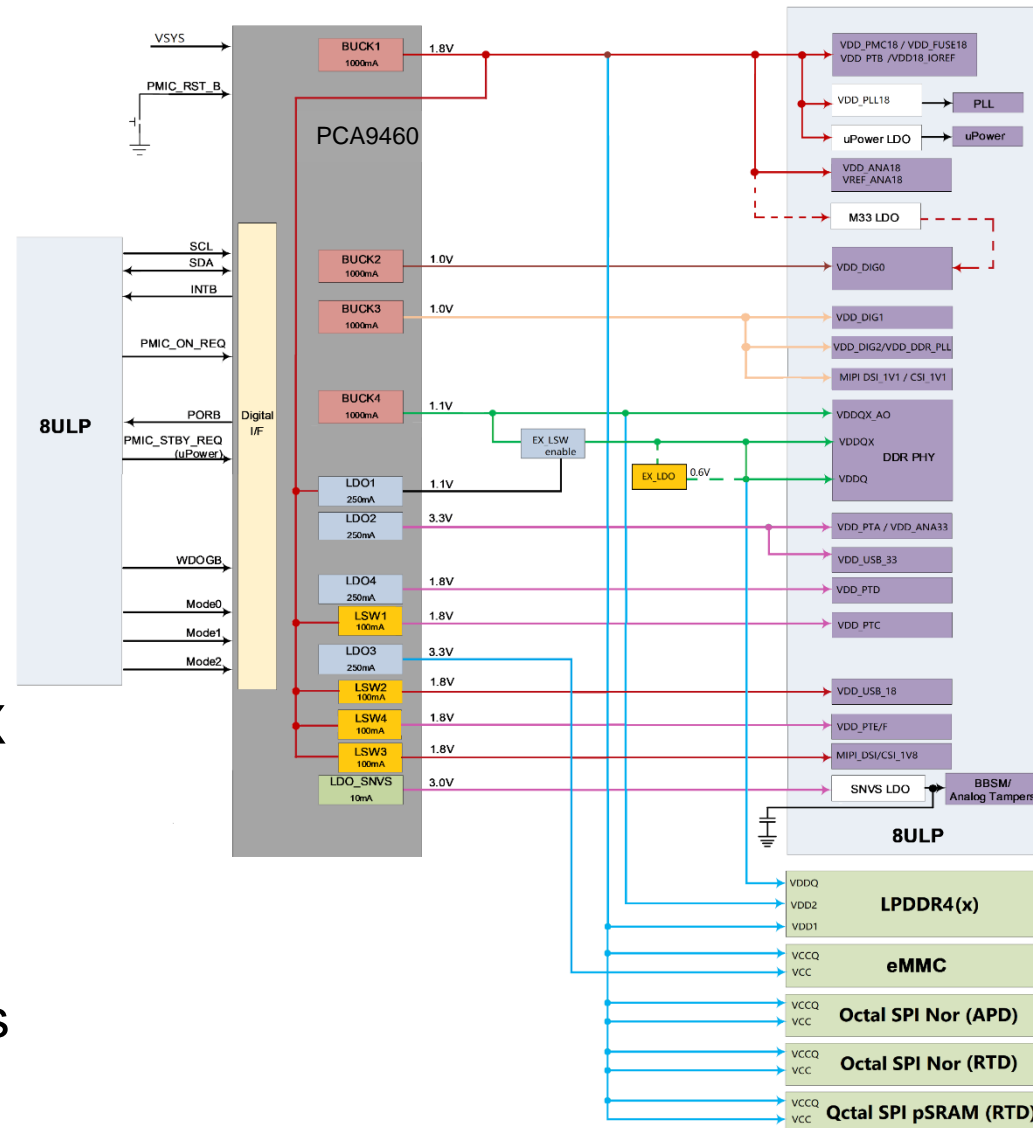
Low Power Devices



- Home control
- Wearables
- Portable healthcare
- Portable printing
- General embedded control
- IoT edge
- SOM board solutions

i.MX8 ULP + PCA9460 SUBSYSTEM: POWER AND CONTROL INTERACTION

- Logical control and interaction with i.MX 8ULP
 - IIC communication
 - Interrupt driven infrastructure
 - Simple ON and STANDBY entries.
 - Dynamic voltage scaling through ModeX pins or I2C
 - Watchdog timer
 - Fault detection and protection mechanisms



- Power supplies for i.MX 8ULP
 - Core and digital blocks
 - DDR PHY
 - Analog blocks
 - USB interface
 - I/O voltages
 - External memory supplies: DDR3/4/4X and eMMC/Octal SPI
 - Configurable load switches (PTC, VDD_USB, PTE and MIPI_CSI)

PCA9460 FAMILY MEMBERS – SUPPLY SELECTION GUIDE SUPPORTING DIFFERENT MEMORY TYPES

| Part number | Processor Platform | Buck1 (1A) | Buck2 (1A) | Buck3 (1A) | Buck4 (1A) | LDO1 (250mA) | LDO2 (250mA) | LDO3 (250mA) | LDO4 (250mA) | LDO_SNVS (10mA) | Memory application tradeoffs |
|-------------|---------------------|------------|------------|------------|------------|--------------|--------------|--------------|--------------|-----------------|---|
| PCA9460A | i.MX 8ULP + LPDDR4 | 1.8V | 1.0V | 1.0V | 1.1V | 1.1V | 3.3V | 3.3V | 1.8V | 3.0V | Best tradeoff between power, performance and cost |
| PCA9460B | i.MX 8ULP + LPDDR4X | 1.8V | 1.0V | 1.0V | 1.1V | 0.6V | 3.3V | 3.3V | 1.8V | 3.0V | Optimum performance and power consumption improved over LPDDR4. |
| PCA9460C | i.MX 8ULP + LPDDR3 | 1.8V | 1.0V | 1.0V | 1.2V | 1.2V | 3.3V | 3.3V | 1.8V | 3.0V | Most cost efficient, but least performing and higher power vs. LPDDR4 |

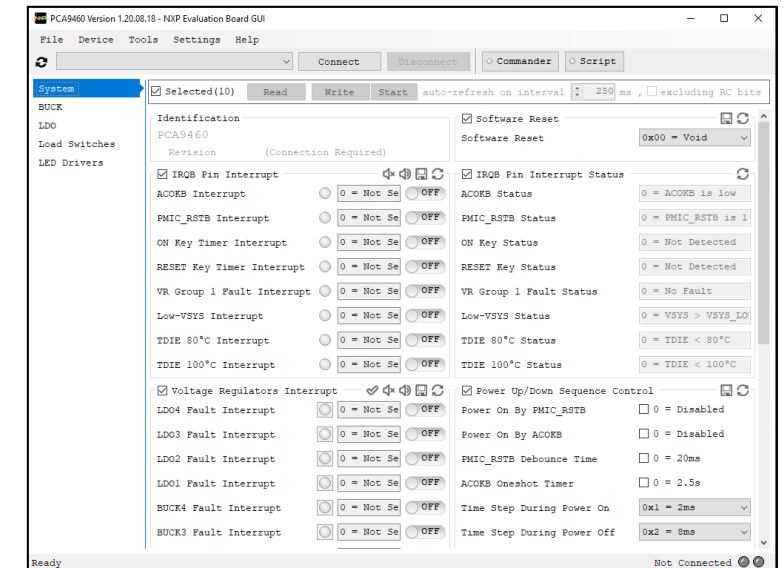
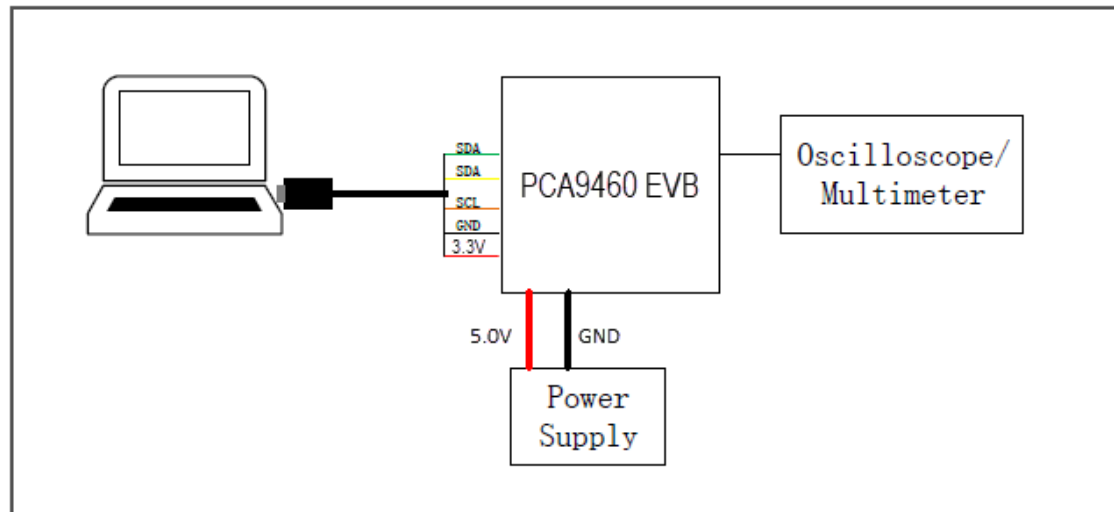
- Note:

- All these variants share the same turn-on and off sequencing.
- Output voltage can be changed with I2C command after device power up.

EVB AND TOOLS DOWNLOAD

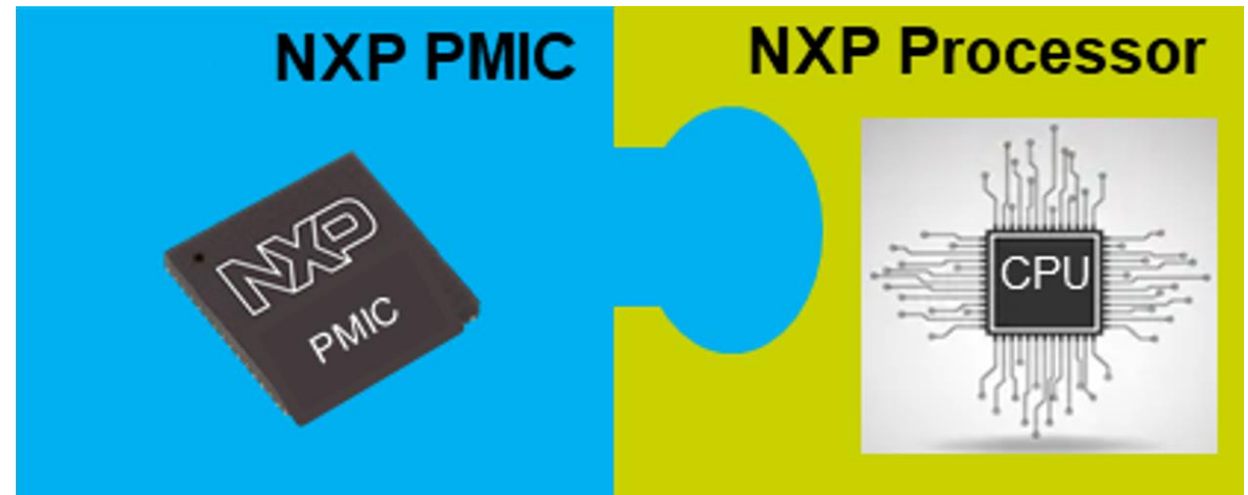
- Full flexibility and configurability to exercise the PMIC in several use cases independently

| | Status |
|-------------------------------------|---|
| PCA9460 EVB P/N: KIT-PCA9460-EVB | Available now in limited quantities. Reach out to your sales/FAE contact for more details |
| PCA9460 EVB User Manual | Preliminary version available now |
| PCA9460 Graphical User Interface | Preliminary version available now |
| FTDI Driver | https://www.ftdichip.com/Drivers/D2XX.htm |



NXP SYSTEM SOLUTION TOTAL QUALITY

Proven System Solution

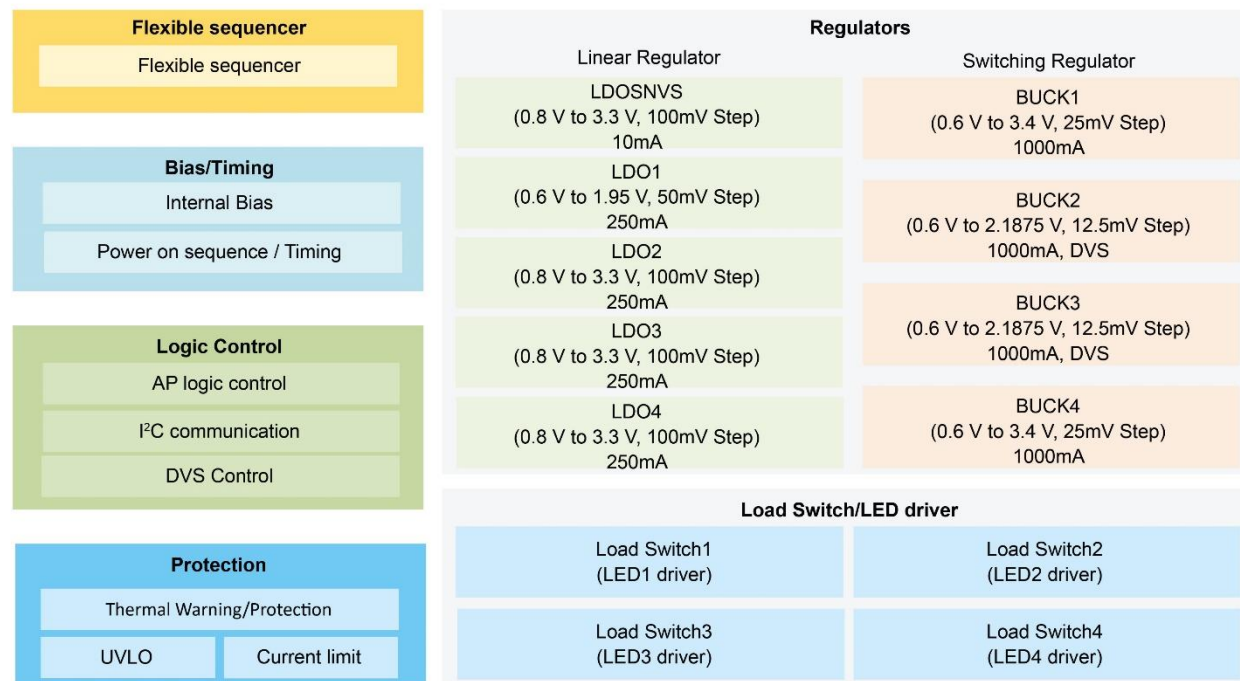


- Co-development for proven and robust system performance
 - In sync architecture aimed to optimize system performance and cost
 - Software development and support
 - Fully validated hardware and software implementation via reference designs
- Total quality with hardware and software optimized system solution
 - Lower risk and shorter time to market
 - NXP total system level support (Processor + PMIC)

PCA9460 PMIC (FOR i.MX 8ULP APPLICATIONS PROCESSOR)

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- Thermal protection
- 6 x 7 bump array, 0.4 mm pitch, WL-CSP, 2.86 x 2.46 mm
- Samples available, SOP Q1 2022
- EVK: Initial batch available



Device **SAMPLING**

PCA9460 EVB available

SOP Q1'2022