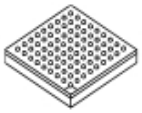
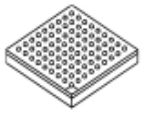
i.MX RT500 Low-Power Crossover Processor

MIMXRT5XXSFFOC
MIMXRT5XXSFFOCR
MIMXRT5XXSFAWCR

The i.MX RT500 is a family of dual-core microcontrollers for embedded applications featuring an Arm Cortex-M33 CPU combined with a Cadence® Xtensa® Fusion F1 Audio Digital Signal Processor CPU. The Cortex-M33 includes two hardware coprocessors providing enhanced performance for an array of complex algorithms along with a 2D Vector GPU with LCD Interface and MIPI DSI PHY. The family offers a rich set of peripherals and very low power consumption. The device has up to 5 MB SRAM, two FlexSPIs (Octal/Quad SPI Interfaces) each with 32 KB cache, one with dynamic decryption, high-speed USB device/host + PHY, 12-bit 1 MS/s ADC, Analog Comparator, Audio subsystems supporting up to 8 DMIC channels, 2D GPU and LCD Controller with MIPI DSI PHY, SDIO/eMMC; FlexIO; AES/SHA/Crypto M33 coprocessor and PUF key generation



249 FOWLP 7.0mm x 7.0mm x 0.725mm, 0.4mm pitch



141 WLCSP 4.525mm x 4.525mm x 0.49mm, 0.35mm pitch

Control processor core

- Arm Cortex-M33 processor, running at frequencies of up to 275 MHz
- Arm TrustZone
- Arm Cortex-M33 built-in Memory Protection Unit (MPU) supporting eight regions
- Single-precision Hardware Floating Point Unit (FPU).
- Arm Cortex-M33 built-in Nested Vectored Interrupt Controller (NVIC).
- Non-maskable Interrupt (NMI) input.
- Two coprocessors for the Cortex-M33: a hardware accelerator for fixed and floating point DSP functions (PowerQuad) and a Crypto/FFT engine (Casper). The DSP coprocessor uses a bank of four dedicated 8 KB SRAMs. The Crypto/FFT engine uses a bank of two 2 KB SRAMs that are also AHB accessible by the CPU and the DMA engine.
- Serial Wire Debug with eight break points, four watch points, and a debug timestamp counter. It includes Serial Wire Output (SWO) trace and ETM trace.
- Cortex-M33 System tick timer

DSP processor core

- Cadence Tensilica Fusion F1 DSP processor, running at frequencies of up to 275 MHz.
- Hardware Floating Point Unit.
- Serial Wire Debug (shared with Cortex-M33 Control Domain CPU).

Communication interface

- Up to 9-12 configurable universal serial interface modules (Flexcomm Interfaces). Each module contains an integrated FIFO and DMA support. Each of the nine modules can be configured as:
  - A USART with dedicated fractional baud rate generation and flow-control handshaking signals. The USART can optionally be clocked at 32 kHz and operated when the chip is in reduced power mode, using either the 32 kHz clock or an externally supplied clock. The USART also provides partial support for LIN2.2.
  - An I2C-bus interface with multiple address recognition, and a monitor mode. It supports 400 Kb/sec Fast-mode and 1 Mb/sec Fast-mode Plus. It also supports 3.4 Mb/sec high-speed when operating in slave mode.
  - An SPI interface.
  - An I2S (Inter-IC Sound) interface for digital audio input or output. Each I2S supports up to four channel-pairs.
- Two additional high-speed SPI interfaces supporting 50 MHz operation
- One additional I2C interface with open-drain pads
- Two I3C bus interfaces
- A digital microphone interface supporting up to 8 channels with associated decimators and Voice

Five I/O Power Rails

- Five independent supplies powering different clusters of pins to permit interfacing directly to off-chip peripherals operating at different supply levels.

On-chip memory

- Up to 5 MB of system SRAM accessible by both CPUs, both DMA engines, the Graphics Subsystem and all other AHB masters.
- Additional SRAMs for USB traffic (16 KB), Cortex-M33 co-processors (4 x 8 KB), SDIO FIFOs (2 x 512 B dual-port), PUF secure key generation (2 KB), FlexSPI caches (32 KB each), SmartDMA commands (32 KB), and a variety of dual and single port RAMs for graphics.
- 16 kbits OTP fuses
- Up to 192 KB ROM memory for factory-programmed drivers and APIs
- System boot from High-speed SPI, FlexSPI Flash, HS USB, I2C, UART or eMMC via on-chip bootloader software included in ROM. FlexSPI boot mode will include an option for Execute-in-place start-up for non-secure boot.

Digital peripherals

- Two general purpose DMA engines, each with 37 channels and up to 27 programmable request/trigger sources.
    - Can be configured such that one DMA is secure and the other non-secure and/or one can be designated for use by the M33 CPU and the other by the DSP
- Smart DMA Controller with dedicated 32KB code RAM
- USB high-speed host/device controller with on-chip PHY and dedicated DMA controller.
- Two FlexSPI (Octal/Quad) Interfaces up to 200 MHz DDR/SDR (target). 32 KB caches with selectable cache policies based on programmable address regions. One of the FlexSPI interface will include on-the-fly decryption for execute-in-place and address-remapping to support dual-image boot. DMA supported (both modules).
- Two SD/eMMC memory card interfaces with dedicated DMA controllers. One supports eMMC 5.0 with HS400/DDR operation.

Analog peripherals

- One 12-bit ADC with sampling rates of 1 Msamples/sec and an enhanced ADC controller. It supports up to 6 single-ended channels or 2 differential channels. The ADC supports DMA.
- Temperature sensor.
- Analog comparator

Activation Detect. One pair of channels can be streamed directly to I2S. The DMIC supports DMA.

Timers

- One 32-bit SCTimer/PWM module (SCT). Multi-purpose timer with extensive event-generation, match/compare, and complex PWM and output control features.
    - 10 general-purpose/PWM outputs, 8 general-purpose inputs
    - It supports DMA and can trigger external DMA events
    - It supports fractional match values for high resolution
- Five general purpose, 32-bit timer/counter modules with PWM capability
- 24-bit multi-rate timer module with 4 channels each capable of generating repetitive interrupts at different, programmable frequencies.
- Two Windowed Watchdog Timers (WDT) with dedicated watchdog oscillator (1 MHz LPOSC)
- Frequency measurement module to determine the frequency of a selection of on-chip or off-chip clock sources.
- Real-Time Clock (RTC) with independent power supply and dedicated oscillator. Integrated wake-up timer can be used to wake the device up from low-power modes. The RTC resides in the “always-on” voltage domain. RTC includes eight 32-bit general-purpose registers which can retain contents when power is removed from the rest of the chip.
- Ultra-low power micro-tick Timer running from the Watchdog oscillator with capture capability for timestamping. Can be used to wake up the device from low-power modes.
- 64-bit OS/Event Timer common to both processors with individual match/capture and interrupt generation logic.

Clocks

- Crystal oscillator with an operating range of 4 MHz to 32 MHz.
- Dual trim option: Internal 192/96 MHz FRO oscillator. Trimmed to 1% accuracy.
- FRO capable of being tuned using an accurate reference clock (eg. XTAL Osc) to 0.1% accuracy with 46% duty cycle.
- Internal 1 MHz low-power oscillator with 10% accuracy. Serves as the watchdog oscillator and clock for the OS/Event Timer and the Systick among others. Also available as the system clock to both domains.
- 32 kHz real-time clock (RTC) oscillator that can optionally be used as a system clock.
- Main System PLL:
    - allows CPU operation up to the maximum rate without the need for a high-frequency crystal.

Graphics/Multimedia

- 2D Vector Graphics Processing Unit, running at frequencies of up to 275 MHz.
- LCD Display Interface supporting smart LCD displays and video mode.
- MIPI DSI Interface with on-chip PHY supporting transfer rates up to 895.1 Mbps.
- FlexIO can be configured to provide a parallel interface to an LCD

I/O Peripherals

- Up to 136 general purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors. Ports can be written as words, half-words, bytes, or bits.
- Mirrored, secure GPIO0.
- Individual GPIO pins can be used as edge and level sensitive interrupt sources, each with its own interrupt vector.
- All GPIO pins can contribute to one of two ganged (OR'd) interrupts from the GPIO_HS module.
- A group of up to 7 GPIO pins (from Port0/1) can be selected for Boolean pattern matching which can generate interrupts and/or drive a "pattern-match" output.
- Adjustable output driver slew rates.
- JTAG boundary scan

Security

- **Secure Isolation:** Protection from software and remote attacks using Trustzone for armV8M. Hardware isolation of AES keys
- **Secure Boot:** firmware in ROM providing immutable root of trust
- **Secure Storage:** Physically Unclonable Function (PUF) based key store, On-the-fly-AES decryption (OTFAD) of off-chip flash for code storage
- **Secure Debug:** Certificate based debug authentication mechanism
- **Secure Loader:** Supports firmware update mechanism with authenticity (RSA signed) and confidentiality (AES-CTR encrypted) protection
- **Secure Identity:** 128-bit Universal Unique Identifier (UUID), 256-bit Compound Device Identifier (CDI) per TCG DICE specification
- **Cryptographic Accelerators**
    - Symmetric cryptography (AES) with 128/192/256-bit key strength and protection against Side-channel analysis (Differential Power Analysis and Template attacks)
    - Asymmetric cryptography acceleration using CASPER co-processor
    - NIST SP 800-90b compliant TRNG design with 512-bit output per call
    - Hash engine with SHA-256 and SHA1

May be run from the FRO, the crystal oscillator or the CLKIN pin.
    - a second, independent PLL output provides alternate high-frequency clock source for the DSP CPU if the required frequency is different from the main system clock. (Note: 2nd PFD output from Main System PLL)
    - two additional PLL outputs provide potential clock sources to various peripherals.
- Audio PLL for the audio subsystem.

Power Control

- Main external power supply: 1.8V ± 5%
- Vddcore supply (from PMIC or internal PMU): adjustable from 0.6 V to 1.1 V (including retention mode)
- Analog supply: 1.71-1.89 V
- Five VDDIO supplies (can be shared or independent)
- USB Supply: 3.0-3.6 V
- Reduced power modes:
    - Sleep mode: CPU clock shut down (each CPU independently)
    - Deep_sleep mode: User-selectable configuration via PDSLEEPCFG
    - Deep_powerdown mode: Internal power removed from entire chip except "always-on" domain
    - Each individual SRAM partition can be independently powered-off or put into a low-power retain mode
    - DSP Domain can be powered-off independently from the rest of the system.
    - Ability to operate the synchronous serial interfaces in sleep or deep-sleep as a slave or USART clocked by the 32 kHz RTC oscillator
    - Wake-up from low-power modes via interrupts from various peripherals including the RTC and the OS/Event timer
- RBB/FBB to provide additional control over power/performance trade-offs
- Power-On Reset (POR).

Operating characteristics

- Temperature range (ambient): -20 °C to +70 °C
- VDDCORE: 0.7 V - 1.155 V
- VDDIO_0/1/2/4: 1.71 V - 1.89 V
- VDDIO_3: 1.71 V - 3.6 V

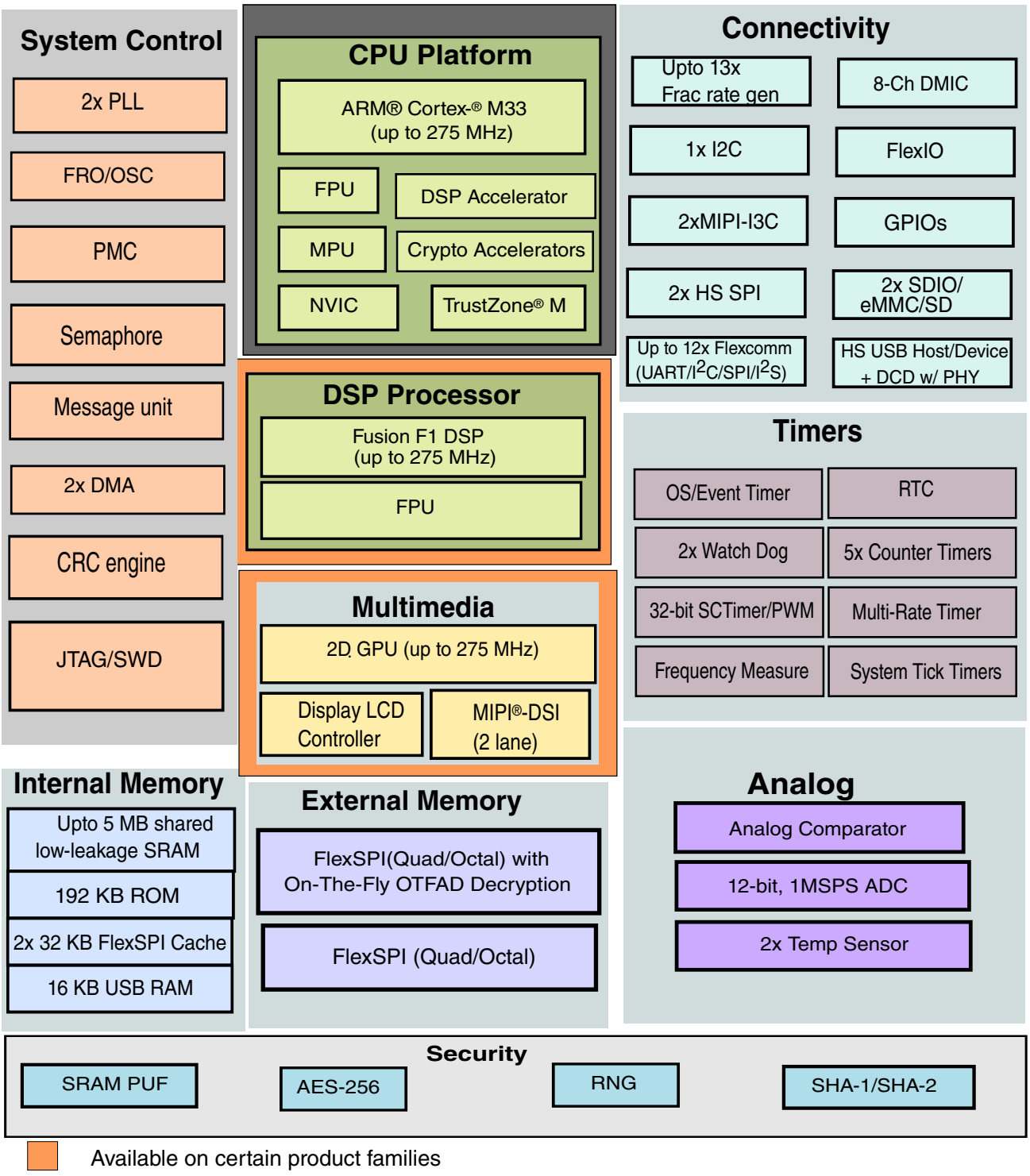


Figure 1. i.MX RT500 Block Diagram

The following table provides examples of orderable sample part numbers covered by this data sheet.

Orderable part number table

Orderable part number	Part number[1]	SRAM (MB)	DSP	Graphics	Security	USB	FlexComm's	Package
MIMXRT595SFFOC	MRT595SFFOC	5	Yes	Yes	SRAM PUF, AES256, HASH	HS	12	FOWLP249[2]
MIMXRT555SFFOC	MRT555SFFOC	5	No	Yes	SRAM PUF, AES256, HASH	HS	12	FOWLP249
MIMXRT533SFFOC	MRT533SFFOC	3	No	No	SRAM PUF, AES256, HASH	HS	12	FOWLP249
MIMXRT595SFFOCR	MRT595SFFOC	5	Yes	Yes	SRAM PUF, AES256, HASH	HS	12	FOWLP249
MIMXRT555SFFOCR	MRT555SFFOC	5	No	Yes	SRAM PUF, AES256, HASH	HS	12	FOWLP249
MIMXRT533SFFOCR	MRT533SFFOC	3	No	No	SRAM PUF, AES256, HASH	HS	12	FOWLP249
MIMXRT533SFAWCR	MRT533SFAWC	3	No	No	SRAM PUF, AES256, HASH	HS	9[3]	WLCSP141[4]
MIMXRT555SFAWCR	MRT555SFAWC	5	No	Yes	SRAM PUF, AES256, HASH	HS	9[3]	WLCSP141
MIMXRT595SFAWCR	MRT595SFAWC	5	Yes	Yes	SRAM PUF, AES256, HASH	HS	9[3]	WLCSP141

1. As marked on package
2. 249-pin Fan-out wafer-level package
3. FlexComm6 signals only include CTS/SDA and RTS/SCL and FlexComm12 only includes TXD/SDA and RXD/SCL
4. 141-pin wafer level chip scale package

Device revision number

Device Mask Set Number	SILICONREV_ID	JTAG_ID[CHIPREV]
2P43B	0x000B0002	0x2

Package markings for i.MX RT devices consist of 4 sets of identifiers as shown below.

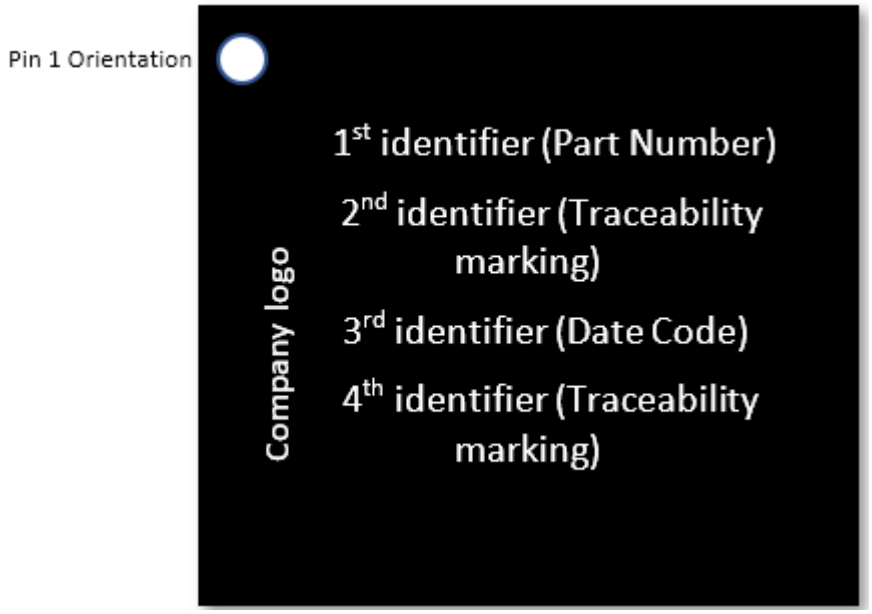


Figure 2. Package markings

- The 1st identifier defines the Part Number and is composed of 11 characters.
- The 2nd and 4th identifiers define the Traceability markings.
- The 3rd identifier defines the Date Code for the week of manufacture is a subset of the standard 5 character format.

The standard date code format is “xYYWW”:

- The leading digit represented by “x” can be ignored and “YYWW” indicate the Date Code.
- “YY" represents an encoding of the calendar year (for example, 19 corresponds to year 2019).
- “WW” represents an encoding of the work week within the calendar year (for example, 07 corresponds to work week 7).

Please provide this information to your local NXP representative for further details.

The following figure explains the part number for this device.

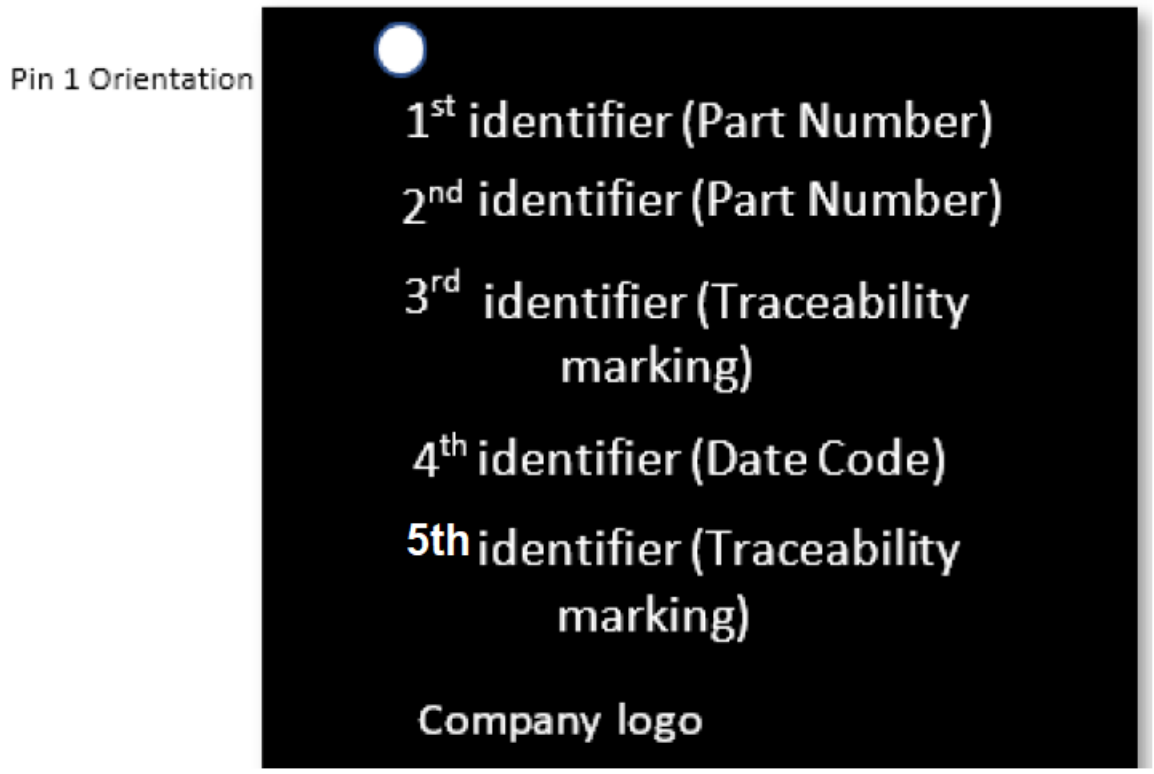


Figure 3. 141-pin package markings

- The 1st identifier defines the first portion of the Part Number and is composed of 8 characters.
- The 2nd identifier defines the last portion of the Part Number and is composed of 4 characters.
- The 3rd and 5th identifiers define the Traceability markings.
- The 4th identifier defines the Date Code for the week of manufacture is a subset of the standard 8 character format.

The standard date code format is “xxxxYYWW”:

- The leading digits represented by “x” can be ignored and “YYWW” indicate the Date Code.
- “YY" represents an encoding of the calendar year (for example, 19 corresponds to year 2019).
- “WW” represents an encoding of the work week within the calendar year (for example, 07 corresponds to work week 7).

Please provide this information to your local NXP representative for further details.

The following figure explains the part number for this device.

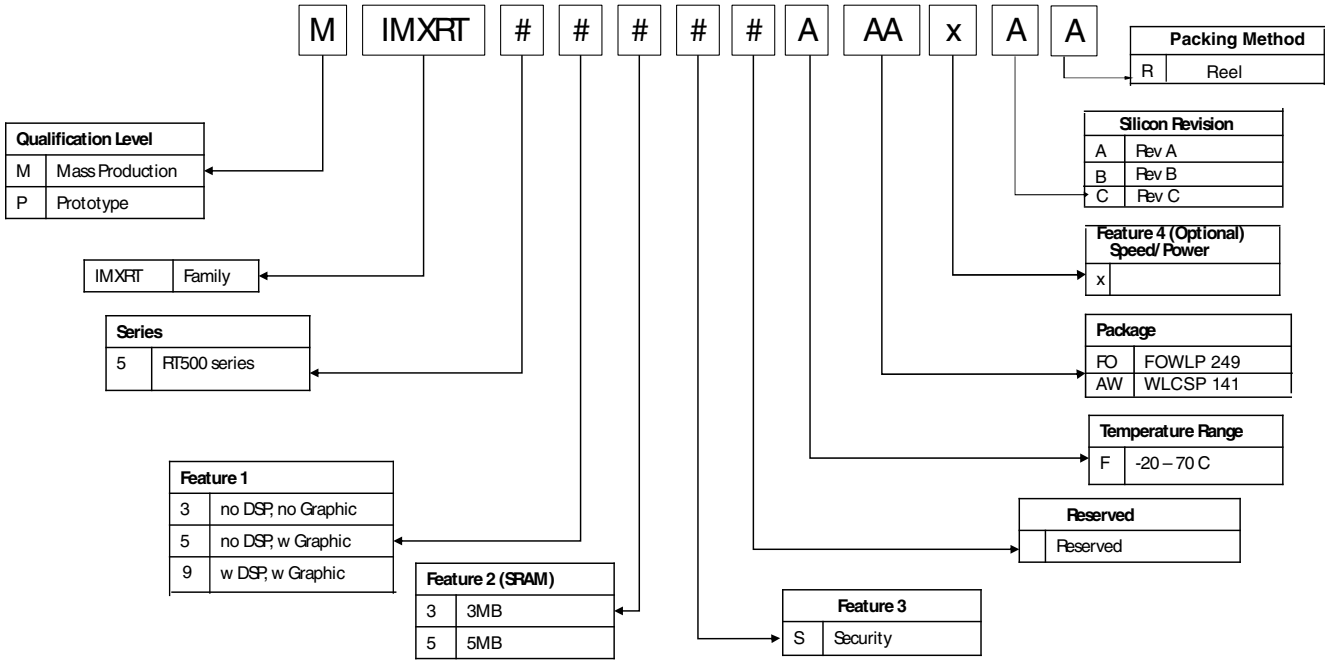


Figure 4. Part number diagram

Related Resources

Type	Description
Selector Guide	The Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.
Reference Manual	The *i.MX RT500 Low-Power Crossover MCU Reference Manual* contains a comprehensive description of the structure and function (operation) of a device.
Data Sheet	Refers to this document which includes electrical characteristics and signal connections.
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.

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1 Electrical characteristics

1.1 Chip-level conditions

This section provides the device-level electrical characteristics for the IC. See the following table for a quick reference to the individual tables and sections.

Table 1. i.MX RT500 chip-level conditions

For these charateristics	Topic appears
Absolute maximum voltage and current ratings	Absolute maximum voltage and current ratings
Thermal handling ratings	Thermal handling ratings
Moisture handling ratings	Moisture handling ratings
ESD handling ratings	ESD handling ratings
Thermal characteristics	Thermal characteristics
General operating conditions	General operating conditions
I/O parameters	I/O parameters
Power consumption operating behavior	Power consumption operating behavior

1.1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	—	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level (FOWLP)	—	3	—	1
MSL	Moisture sensitivity level (WLCSP)	—	1	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	500	V	2
I_{LAT}	Latch-up current at ambient temperature of 70 °C	-100	100	mA	3

1. Determined according to JS001, *Electrostatic Discharge (ESD) Sensitivity Testing, Human Body Model (HBM) - Component Level*.
2. Determined according to JEDEC Standard JS002, *Electrostatic Discharge (ESD) Sensitivity Testing, Charged Device Model (CDM) - Device Level*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1.2 Absolute maximum voltage and current ratings

Caution

Stress beyond those listed under the following table may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 2. Absolute maximum ratings1

Symbol	Parameter	Conditions	Notes	Min.	Max.	Unit
VDD_AO1V8	Supply 1.8 V supply for “always on” features	-	2	-0.3	1.98	V

Table continues on the next page...

Table 2. Absolute maximum ratings[1] (continued)

Symbol	Parameter	Conditions	Notes	Min.	Max.	Unit
VDD1V8	1.8 V supply voltage for on-chip analog functions other than the ADC and comparator.	-	2	-0.3	1.98	V
VDD1V8_1	1.8 V supply voltage for on-chip digital logic	-	2	-0.3	1.98	V
VDDCORE	1.1 V input supply for core logic	On-chip regulator not used. LDO_ENABLE[3] =0. Power supplied by an off-chip power management IC (PMIC).	2	-0.3	1.32	V
VDDIO_0/1/2/4	Supply voltage for GPIO pins	-	2	-0.3	1.98	V
VDDIO_3	Supply voltage for GPIO pins	-	2	-0.3	3.96	V
VDDA_ADC1V8	1.8 V analog supply voltage for ADC and comparator	-	2	-0.3	1.98	V
VDDA_BIAS	Bias voltage for ADC and comparator	-	2	-0.3	1.98	V
VREFP	ADC positive reference voltage	-	2	-0.3	1.98	V
USB1_VDD3V3	USB1 analog 3.3 V supply	-	2	-0.3	3.96	V
USB1_VBUS [4]	USB1_VBUS detection	-	-	-0.3	5.6	V
MIPI_DSI_VDD11	MIPI DSI 1.1 V PHY input core voltage supply	-	-	-0.3	1.32	V
MIPI_DSI_VDD18	MIPI DSI 1.8 V PHY IO input voltage supply	-	-	-0.3	1.98	V
MIPI_DSI_VDDA_CAP	MIPI DSI 1.1 V capacitor output voltage supply	-	-	-0.3	1.32	V

Table continues on the next page...

Table 2. Absolute maximum ratings[1] (continued)

Symbol	Parameter	Conditions	Notes	Min.	Max.	Unit
I_{DD}	supply current (FOWLP249)	per supply pin, 1.71 V ≤ V_{DD} < 1.89 V 1.71 V ≤ V_{DD} < 3.6 V	5	-	100	mA
	supply current (WCLSP141)	per supply pin, 1.71 V ≤ V_{DD} < 1.89 V 1.71 V ≤ V_{DD} < 3.6 V	5	-	100	mA
I_{SS}	ground current (FOWLP249)	per ground pin, 1.71 V ≤ V_{DD} < 1.89 V 1.71 V ≤ V_{DD} < 3.6 V	5	-	100	mA
	ground current (WLCSP141)	per ground pin, 1.71 V ≤ V_{DD} < 1.89 V 1.71 V ≤ V_{DD} < 3.6 V	5	-	100	mA
$P_{tot(pack)}$	total power dissipation (per package)	FOWLP 249, based on package heat transfer, not device power consumption	6	-	1.86	W
	total power dissipation (per package)	WLCSP141		-	1.42	W

1. In accordance with the Absolute Maximum Rating System (IEC 60134). The following applies to the limiting values:
   - This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
   - Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.
   - The limiting values are stress ratings only and operating the part at these values is not recommended and proper operation is not guaranteed. The conditions for functional operation are specified in Table 5.
2. Maximum/minimum voltage above the maximum operating voltage (see Table 5) and below ground should be avoided as proper operation cannot be guaranteed and could lead to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.
3. The WLCSP package does not support this signal and only supports an off-chip power management IC.
4. On WLCSP package, USB ISP mode is not supported. VBUS pin is not available on the WLCSP package. To detect VBUS connection, user can connect a GPIO pin to the USB connector's VBUS. When a rising edge occurs on the GPIO pin, software should set bit 10 (FORCE_VBUS) and bit 16 (DCON) in the DEVCMDSTAT register.
5. The peak current should not exceed the total supply current.
6. Determined in accordance to JEDEC JESD51-2A natural convection environment (still air).

1.3 Thermal specifications

1.3.1 Thermal operating requirements

Table 3. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_j	Die junction temperature	-20	105	°C	1
T_A	Ambient temperature	-20	70	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is: $T_J = T_A + R_{\Theta JA} \times$ chip power dissipation.

1.3.2 Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 4. Thermal resistance1

Symbol	Parameter	Conditions	Max/Min	Unit
249 FOWLP Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JESD51-9, 2s2p, still air	29.6	°C/W

Table continues on the next page...

Table 4. Thermal resistance[1] (continued)

Symbol	Parameter	Conditions	Max/Min	Unit
$R_{\Psi(JT)}$	thermal resistance from junction to package top	JESD51-9, 2s2p, still air	0.2	°C/W
141 WCLSP Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JESD51-9, 2s2p, still air	35.3	°C/W
$R_{\Psi(JT)}$	thermal resistance from junction to package top	JESD51-9, 2s2p, still air	0.1	°C/W

1. Determined in accordance to JEDEC JESD51-2A natural convection environment (still air). Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment

1.4 General operating conditions

Table 5. General operating conditions

Symbol	Parameter	Conditions	Min.	Typ.[1]	Max.	Unit
f_{clk}	CPU (Cortex-M33) clock frequency	-	-	-	275	MHz
	CPU (Cortex-M33) clock frequency	For USB high-speed device and host operations	90	-	275	MHz
		For OTP programming only	-	-	120	MHz
f_{clk}	DSP clock frequency	-	-	-	275	MHz
	GPU clock frequency	-	-	-	275	MHz
f_{otp_clk} ($f_{clk/OTP\_CLK\_DIV[DIV]}$)	OTP clock frequency	For OTP programming only	-	-	120	MHz
VDD_AO1V8	Supply 1.8 V supply for “always on” features.	-	1.71	-	1.89	V
VDD1V8	1.8 V supply voltage for on-chip analog functions other than the ADC and comparator	-	1.71	-	1.89	V
VDD1V8_1[2]	1.8 V supply voltage for on-	-	1.71	-	1.89	V

Table continues on the next page...

Table 5. General operating conditions (continued)

Symbol	Parameter	Conditions	Min.	Typ.[1]	Max.	Unit
	chip digital logic					
VDDCORE[3], [4], [5]	VDDCORE 1.1 V supply voltage required for Power-On	For initial power-on/ boot-up only	1.0	-	-	V
VDDCORE [3], [4], [5]	Core supply voltage required for Power-On	For initial power-on/ bootup only (High Speed clock - OTP setting - BOOT_CLK_SPEED)	1.13	-	-	V
VDDCORE [3], [4], [5], [6], [7]	Core supply voltage. On-chip regulator not used. LDO_ENABLE[8] =0. Power supplied by an off-chip power management IC (PMIC).	Retention mode	0.58	0.6	-	V
		Active Mode (M33/DSP/GPU Max Freq = 60 MHz, FBB)[9]	0.7	-	-	V
		Active Mode (M33/DSP/GPU Max Freq = 100 MHz, FBB)	0.8	-	-	V
		Active Mode (M33/DSP/GPU Max Freq = 192 MHz, FBB)	0.9	-	-	V
		Active Mode (M33/DSP/GPU Max Freq = 230 MHz[10], FBB)	1.0	-	-	V
		ctive Mode (M33/DSP/GPU Max Freq = 250 MHz[10], FBB)	1.02	-	-	V
		Active Mode (M33/DSP/GPU Max Freq = 275 MHz[10], FBB)	1.1	-	-	V
VDDIO_0/1/2/4[11]	supply voltage for GPIO rail	-	1.71	-	1.89	V
VDDIO_3	supply voltage for GPIO rail	-	1.71	-	3.6	V
VDDA_ADC1V8	1.8 V analog supply voltage for ADC and comparator	-	1.71	-	1.89	V
VDDA_BIAS[12]	Bias for ADC and comparator	-	1.71	-	1.89	V
VREFP	ADC positive reference voltage	-	1.71	-	1.89	V
USB1_VDD3V3	USB1 analog 3.3 V supply	-	3.0	-	3.6	V

Table continues on the next page...

Table 5. General operating conditions (continued)

Symbol	Parameter	Conditions	Min.	Typ.[1]	Max.	Unit
USB1_VBUS[13]	USB1_VBUS detection	-	4.0[14] or 3.0[15]	5.0	5.5	V
MIPI_DSI_VDD11	MIPI DSI 1.1V digital core input voltage supply	-	0.85[16]	-	1.155	V
MIPI_DSI_VDD18	MIPI DSI 1.8V PHY IO input voltage supply	-	1.71	-	1.89	V
MIPI_DSI_VDDA_CAP	MIPI DSI 1.1V digital core output voltage supply	-	-0.3	-	1.155	V

1. Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.
2. 1.8 V supply voltage for OTP during active mode. In deep-sleep mode, this pin can be powered off to conserve additional current (~20 uA). VDD1V8_1 must be stable before performing any OTP related functions.
3. When LDO_ENABLE is externally tied low, the user must boot at VDDCORE = 1.0 V or higher (Low power/Normal clock mode - OTP setting - BOOT_CLK_SPEED) or VDDCORE = 1.13 V (High Speed clock - OTP setting - BOOT_CLK_SPEED). Thereafter, the VDDCORE can be adjusted to the desired level.
4. When LDO_ENABLE is externally tied high, the on-chip regulator to the VDDCORE Core voltage in PMC is set to the default value 1.05 V (Low power/Normal clock mode - OTP setting - BOOT_CLK_SPEED) or 1.13 V (High Speed clock - OTP setting - BOOT_CLK_SPEED). Thereafter, the POWER_SetLdoVoltageForFreq API function can be used to internally configure the on-chip regulator voltage to the VDDCORE.
5. When performing any OTP read/write function, the VDDCORE voltage must be set to 1.0 V or higher when LDO_ENABLE is externally tied high or low.
6. The maximum frequency for the specified VDDCORE voltage is the frequency of the clock after the SYSCPUAHBCLKDIV, DSPCPUCLKDIV, and GPUCLKDIV clock dividers found in "RT500 clock diagram" of the i.MX RT500 Reference Manual. The VDDCORE voltage has to be set according to the chosen M33 CPU, DSP, GPU clock frequency. These limits apply to both the FRO and PLL as clock sources.
7. To further minimize power or energy consumption, AN13695: Dynamic Voltage Scaling using PVT Sensor on i.MX RT500 provides details for reducing VDDCORE voltage using the PVT Sensor.
8. The WLCSP package does not support this signal and only supports an off-chip power management IC.
9. GPU, FlexSPI, TRNG, and CTIMER are not supported on this voltage.
10. Although i.MX RT500 is targeted to operate up to 200 MHz for low power operation, it can operate up to 275 MHz; however, there will be an increase in current consumption.
11. It is strongly recommended that the default values for PADVRANGE[VDDIO_RANGE0/1/2/4] are changed to 01 to disable the VDDIO Detector in order to reduce current consumption
12. VDD_BIAS must be equal to maximum ADC input voltage or maximum comparator input voltage.
13. On WLCSP package, USB ISP mode is not supported. VBUS pin is not available on the WLCSP package. To detect VBUS connection, user can connect a GPIO pin to the USB connector's VBUS. When a rising edge occurs on the GPIO pin, software should set bit 10 (FORCE_VBUS) and bit 16 (DCON) in the DEVCMDSTAT register
14. The USB PHY provides two options for reporting VBUS valid back to the USB controller:
    - A programmable internal VBUS_VALID comparator (the default option), or
    - An alternate VBUS_VALID_3V detector that will report VBUS valid for voltages above 3 V

    USBPHY_USB1_VBUS_DETECTn[VBUSVALID_SEL] selects which option is used. If the VBUS_VALID comparator is used, USBPHY_USB1_VBUS_DETECTn[VBUSVALID_THRESH] determines the threshold voltage for a valid VBUS. The programmable range is 4.0V to 4.4V (default).
15. The USB PHY provides two options for reporting VBUS valid back to the USB controller:
    - A programmable internal VBUS_VALID comparator (the default option), or
    - An alternate VBUS_VALID_3V detector that will report VBUS valid for voltages above 3 V

USBPHY_USB1_VBUS_DETECTn[VBUSVALID_SEL] selects which option is used. If the VBUS_VALID_3V detector is used, the detector voltage is not programmable.

16. MIPI DSI 1.1V Digital core minimum voltage is 0.85 V for a limited temperature range of 0 to 70 C.

Table 6. VDDCORE minimum voltage when M33/DSP/GPU clock frequency = FRO96M[1]

VDDCORE Vmin (mV)	Minimum Temp (°C)
735	-20
715	0
706	15
700	>20

1. Data in this table is based on FRO trimmed at 96 MHz, main_clk sourced from FRO, FBB, and there are no other faster frequencies in the system.

1.5 Power supply for pins

The following table shows the GPIOs belonging to the specific VDDIO groups and VDD_AO1V8 domain.

VDDIO_0, 1, 2, and 4 supply pins can only be powered from 1.71 V to 1.89 V. The VDDIO_3 supply pin can be powered between 1.71V to 3.6V.

Table 7. Power supply for pins

Pin	GPIO pins
VDDIO_0	PIO0_0 to PIO0_13 (Fail Safe Pads) PIO1_11 to PIO1_15 (Fail Safe Pads) PIO1_18 to PIO1_29 (High Speed Pads[1]) PIO2_14 to PIO2_15 (Fail Safe Pads) PIO3_25 to PIO3_29 (Fail Safe Pads) PIO4_0 to PIO4_6 (Fail Safe Pads) PIO6_27 (Fail Safe Pad)
VDDIO_1	PIO0_14 to PIO0_19 (Fail Safe Pads) PIO0_21 to PIO0_25 (Fail Safe Pads) PIO0_28 to PIO0_31 (Fail Safe Pads) PIO1_0 (Fail Safe Pads) PIO1_3 to PIO1_7 (Fail Safe Pads) PIO1_9 to PIO1_10 (Fail Safe Pads)

Table continues on the next page...

Table 7. Power supply for pins (continued)

Pin	GPIO pins
	PIO2_24 to PIO2_31 (Fail Safe Pads)
	PIO3_1 to PIO3_3 (Fail Safe Pads)
	PIO4_11 to PIO4_17 (High Speed Pads[1])
	PIO4_18 (Fail Safe Pad)
	PIO5_4 and PIO5_8 (Fail Safe Pads)
	PIO5_15 to PIO5_18 (High Speed Pads[1])
	PMIC_I2C_SCL (Fail Safe Pad)
	PMIC_I2C_SDA (Fail Safe Pad)
VDDIO_2	PIO1_30 to PIO1_31 (High Speed Pads[1])
	PIO2_0 to PIO2_8 (High Speed Pads[1])
	PIO2_9 to PIO2_11 (Fail Safe Pads)
VDDIO_3	PIO4_20 to PIO4_31 (Fail Safe Pads)
	PIO5_0 to PIO5_3 (Fail Safe Pads)
VDDIO_4	PIO3_8 to PIO3_18 (High Speed Pads[1])
	PIO3_19 to PIO3_21 (Fail Safe Pads)
VDD_AO1V8	RESETN (Fail Safe Pad)
	LDO_ENABLE (Fail Safe Pad)
	PMIC_IRQ_N (Fail Safe Pad)
	PMIC_MODE0 and PMIC_MODE1 (Fail Safe Pads)

1. None of the HS pins can be floating. In active, sleep, or deep sleep, the HS pins should be managed via internal pull downs. In Deep Power Down, external pull downs should be used.

1.6 I/O parameters

1.6.1 I/O DC parameters

T_{amb} = -20 °C to +70 °C, unless otherwise specified. Values tested in production unless otherwise specified.

Table 8. I/O DC characteristics

Symbol	Parameter	Conditions	Notes	Min.	Typ.[1]	Max.	Unit
$\overline{\text{RESET}}$ pin, **LDO_ENABLE** pin, **PMIC_IRQ_N** pin, **PMIC_MODE**[2] pins							

Table continues on the next page...

Table 8. I/O DC characteristics (continued)

Symbol	Parameter	Conditions	Notes	Min.	Typ.[1]	Max.	Unit
V_{IH}	HIGH-level input voltage			0.7 x VDD_AO1V8	-	VDD_AO1V8 + 0.1	V
V_{IL}	LOW-level input voltage			-0.3	-	0.3 x VDD_AO1V8	V
V_{OH}	HIGH-level output voltage	I_{OH} = -2.9 mA; 1.71 V ≤ VDD_AO1V8 < 1.89 V		0.8 x VDD_AO1V8	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 2.9 mA; 1.71 V ≤ VDD_AO1V8 < 1.89 V		-	-	0.2 x VDD_AO1V8	V
V_{hys}	Input hysteresis voltage		3	0.06 x VDD_AO1V8	-	-	V
Fail-Safe GPIO pins and PMIC I2C pin input characteristics							
V_I	Input voltage	Fail-safe condition for Fail-Safe pins only VDDIO_0/1/4 = 0 V	4	0	-	1.89	V
		VDDIO_3 = 0 V		0	-	3.6	V
V_{IH}	High-level input voltage	1.71 V ≤ VDDIO < 1.89 V		0.75 x VDD1V8	-	VDDIO + 0.1	V
		3.0 V ≤ VDDIO ≤ 3.6 V		0.75 x VDD1V8	-	VDDIO + 0.1	V
V_{IL}	Low-level input voltage	1.71 V ≤ VDDIO < 1.89 V		-0.3	-	0.3 x VDD1V8	V
		3.0 V ≤ VDDIO ≤ 3.6 V		-0.3	-	0.3 x VDD1V8	V
V_{hys}	input hysteresis voltage	1.71 V ≤ VDDIO < 1.89 V	3	0.06 x VDD1V8	-	-	V
		3.0 V ≤ VDDIO ≤ 3.6 V	3	0.06 x VDD1V8	-	-	V
I_{IL}	Low-level input voltage	VI = 0 V; on-chip pull-up resistor disabled. 1.71 V ≤ VDDIO < 1.89 V	-	-1	-	1	V
		VI = 0 V; on-chip pull-up resistor disabled. 3.0 V ≤ VDDIO < 3.6 V	-	-1	-	1	V

Table continues on the next page...

Table 8. I/O DC characteristics (continued)

Symbol	Parameter	Conditions	Notes	Min.	Typ.[1]	Max.	Unit
I_{IH}	High-level input voltage	VI = VDDIO ; on-chip pull-down resistor disabled. 1.71 V ≤ VDDIO < 1.89 V	-	-1	0.5	1	V
		VI = VDDIO_x ; on-chip pull-down resistor disabled. 3.0 V ≤ VDDIO < 3.6 V	-	-1	0.5	1	V
I_{IN}	Input leakage current near V_{IL} threshold, Fail-Safe GPIO only	V_{IL} < VI < VDDIO	5	-	-	-	µA
		1.71 V ≤ VDDIO < 1.89 V		-	-2.5	-5.0	µA
		VDDIO = 3.0 V	-	-	-2.2	-4.4	µA
		VDDIO = 3.3 V	-	-	-2.0	-4.0	µA
		VDDIO = 3.6 V	-	-	-1.9	-3.8	µA
High-Speed GPIO pins, Input characteristics [4]							
V_{IH}	High-level input voltage	1.71 V ≤ VDDIO < 1.89 V		0.7 x VDDIO	-	VDDIO + 0.3	V
		3.0 V ≤ VDDIO ≤ 3.6 V		0.7 x VDDIO	-	VDDIO + 0.3	V
V_{IL}	Low-level input voltage	1.71 V ≤ VDDIO < 1.89 V		-0.3	-	0.3 x VDDIO	V
		3.0 V ≤ VDDIO ≤ 3.6 V		-0.3	-	0.3 x VDDIO	V
V_{hys}	input hysteresis voltage	1.71 V ≤ VDDIO < 1.89 V	3	0.06 x VDDIO	-	-	V
		3.0 V ≤ VDDIO ≤ 3.6 V	3	0.06 x VDDIO	-	-	V
I_{IL}	Low-level input voltage	VI = 0 V; on-chip pull-up resistor disabled. 1.71 V ≤ VDDIO < 1.89 V		-1	-	1	µA
		VI = 0 V; on-chip pull-up resistor disabled. 3.0 V ≤ VDDIO < 3.6 V		-1	-	1	µA
I_{IH}	High-level input voltage	VI = VDDIO ; on-chip pull-down resistor disabled.		-1	0.5	1	µA

Table continues on the next page...

Table 8. I/O DC characteristics (continued)

Symbol	Parameter	Conditions	Notes	Min.	Typ.[1]	Max.	Unit
		1.71 V ≤ VDDIO < 1.89 V					
		VI = VDDIO_x ; on-chip pull-down resistor disabled. 3.0 V ≤ VDDIO < 3.6 V		-1	0.5	1	µA
Fail-Safe and High-Speed GPIO pins and PMIC I2C pins, output characteristics							
V_{OH}	HIGH-level output voltage (Normal drive)	IOH = -2.9 mA; 1.71 V ≤ VDDIO < 1.89 V		0.8 x VDDIO	-	-	V
		IOH = -4 mA; 3.0 V ≤ VDDIO ≤ 3.6 V		0.8 x VDDIO	-	-	V
V_{OH}	HIGH-level output voltage (Full drive)	IOH = -5.8 mA; 1.71 V ≤ VDDIO < 1.89 V		0.8 x VDDIO	-	-	V
		IOH = -8 mA; 3.0 V ≤ VDDIO ≤ 3.6 V		0.8 x VDDIO	-	-	V
V_{OL}	LOW-level output voltage (Normal Drive)	IOL = 2.9 mA; 1.71 V ≤ VDDIO < 1.89 V		-	-	0.2 x VDDIO	V
		IOL = 4 mA; 3.0 V ≤ VDDIO ≤ 3.6 V		-	-	0.2 x VDDIO	V
	LOW-level output voltage (Full Drive)	IOL = 5.8 mA; 1.71 V ≤ VDDIO < 1.89 V		-	-	0.2 x VDDIO	V
		IOL = 8 mA; 3.0 V ≤ VDDIO ≤ 3.6 V		-	-	0.2 x VDDIO	V
Fail-Safe and High-Speed GPIO pins and PMIC I2C pins, weak input pull-up/pull-down characteristics							
I_{pd}	pull-down current	V_I = 1.8 V		34	-	180	µA
		V_I = 3.6 V	6	72	-	180	µA
I_{pu}	pull-up current	V_I = 0 V		-34	-	-180	µA
R_{pd}	pull-down resistance			20	-	50	kΩ
R_{pu}	pull-up resistance			20	-	50	kΩ

1. Typical ratings are not guaranteed. The values listed are at room temperature (25 C), nominal supply voltage.

2. PMIC mode pins are dedicated outputs; they are hard wired to normal drive, no input buffer, no pull ups or pull downs, and no slew rate control.
3. Guaranteed by design, not tested in production.
4. Fail-Safe pins are intended for VDDIO domains that are powered down. Fail-Safe pins do not have diodes to VDDIO. The fail-safe condition only exists when VDDIO = 0 V. High-Speed pins have diodes to VDDIO, so they are not fail-safe. The High-Speed pins (PIO1_18 to PIO1_29, PIO1_30 to PIO1_31, PIO2_0 to PIO2_8, PIO3_8 to PIO3_18, PIO4_11 to PIO4_17, and PIO5_15 to PIO5_18) share all VDDIO domains with Fail-Safe pins, except VDDIO_3.
5. The value of any series resistance on a Fail-Safe pin must be limited to ensure that the maximum VIL value can be satisfied when the pin is switched from high to low. Use Rmax = VIL / IIN to calculate the maximum allowed series resistance.
6. Based on characterization. Not tested in production.

1.7 Power consumption operating behavior

NOTE

- For the lowest power consumption, use the lowest SRAM partition number.
- To further minimize power or energy consumption in Active Mode (Table 9, Table 10, and Table 11,), AN13695: Dynamic Voltage Scaling using PVT Sensor on i.MX RT500 provides details for reducing VDDCORE voltage using the PVT Sensor.

T_{amb} = -20 °C to +70 °C, unless otherwise specified.

Table 9. Power consumption in active mode

Symbol	Parameter	Conditions	Notes	Min.	Typ.[1], [2], [3]	Max.	Unit
Cortex M33 in Active mode, DSP no clock[4]							
enhanced while (1) code[5]executed from SRAM partition 30[6]; Internal LDO disabled							
$I_{DDVDDCORE}$	VDDCORE supply current	HCLK = 12 MHz VDDCORE = 0.7 V	7	-	1.26	-	mA
		HCLK = 24 MHz VDDCORE = 0.7 V	7	-	2.15	-	mA
		HCLK = 48 MHz VDDCORE = 0.7 V	7	-	3.91	-	mA
		HCLK = 96 MHz VDDCORE = 0.8 V	7	-	8.63	-	mA
		HCLK = 192 MHz VDDCORE = 0.9 V	7	-	19.20	-	mA
		HCLK = 192 MHz VDDCORE = 1.0 V	7	-	21.86	-	mA
		HCLK = 192 MHz VDDCORE = 1.1 V	7	-	24.97	-	mA

1. Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). VDD_AO1V8 = VDD1V8 = VDDIO_0/1/2/3/4 = VDDA_ADC1V8 = 1.8 V. VDDA_BIAS = VREFP = 1.8 V. USB1_VDD3V3 = 3.3
2. Characterized through bench measurements using typical samples.
3. Compiler settings: IAR C/C++ Compiler for Arm ver 8.40.1. High, Speed, No Size Constraints. The optimization level is Low, Balanced.
4. Based on the power API library from the SDK software package available on nxp.com
5. The 'enhanced while(1)' loops through several LDR/STR instructions, but forces the core to fetch every instruction from the memory, so the current measurement is more realistic.
6. SRAM partition 30 represents the worst case partition.
7. FRO clock source, FBB enabled

T_{amb} = -20 °C to +70 °C, unless otherwise specified.

Table 10. Power consumption in active mode

Symbol	Parameter	Conditions		Min	Typ[1], [2], [3]	Max	Unit
Cortex M33 in Active mode, DSP no clock[4]							
CoreMark code executed from SRAM partition 30[5]							
$I_{DDVDDCORE}$	VDDCORE supply current	HCLK = 12 MHz VDDCORE = 0.7 V		-	1.25	-	mA
		HCLK = 24 MHz VDDCORE = 0.7 V		-	2.14	-	mA
		HCLK = 48 MHz VDDCORE = 0.7 V		-	3.80	-	mA
		HCLK = 96 MHz VDDCORE = 0.8 V		-	8.55	-	mA
		HCLK = 192 MHz VDDCORE = 0.9 V		-	19.06	-	mA
		HCLK = 192 MHz VDDCORE = 1.0 V		-	21.82	-	mA
		HCLK = 192 MHz VDDCORE = 1.1 V		-	24.93	-	mA

1. Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). VDD_AO1V8 = VDD1V8 = VDDIO_0/1/2/3/4 = VDDA_ADC1V8 = 1.8 V. VDDA_BIAS = VREFP = 1.8 V. USB1_VDD3V3 = 3.3 V
2. Characterized through bench measurements using typical samples.
3. Compiler settings: IAR C/C++ Compiler for Arm ver 8.40. High Speed, No Size constraints. The optimization level is Low, Balanced.
4. Based on the power API library from the SDK software package available on nxp.com
5. SRAM partition 30 represents the worst case partition.

T_{amb} = -20 °C to +70 °C, unless otherwise specified.

Table 11. Power consumption in active mode

Symbol	Parameter	Conditions	Notes	Min	Typ[1], [2], [3]	Max	Unit
FFT code executed from SRAM partition 30 and 31[4]; Internal LDO disabled							
DSP in Active mode, M33 in WFI[5]							

Table continues on the next page...

Table 11. Power consumption in active mode (continued)

Symbol	Parameter	Conditions	Notes	Min	Typ[1], [2], [3]	Max	Unit
$I_{DDVDDCORE}$	VDDCORE supply current	HCLK = 10 MHz VDDCORE = 0.7 V	6	-	1.43	-	mA
		HCLK = 40 MHz VDDCORE = 0.8 V	6		4.66		mA
		HCLK = 100 MHz VDDCORE = 0.8 V	6	-	10.02	-	mA
		HCLK = 150 MHz VDDCORE = 0.9 V	6	-	16.53	-	mA
		HCLK = 200 MHz VDDCORE = 0.9 V	6	-	21.48	-	mA

1. Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). VDD_AO1V8 = VDD1V8 = VDDIO_0/1/2/3/4 = VDDA_ADC1V8 = 1.8 V. VDDA_BIAS = VREFP = 1.8 V. USB1_VDD3V3 = 3.3 V
2. Characterized through bench measurements using typical samples.
3. Compiler settings: IAR C/C++ Compiler for Arm ver 8.40. High Speed, No Size constraints. The optimization level is Low, Balanced.
4. SRAM partitions 30 and 31 represent the worst case partitions. The Fusion F1 DSP requires DRAM and IRAM in different partitions. DSP_DRAM is in partition 30, DSP_IRAM is in partition 31.
5. Based on the power API library from the SDK software package available on nxp.com
6. PLL clock source, FBB enabled

Table 12. Power consumption in sleep mode

Symbol	Parameter	Conditions	Notes	Min.	Typ.	Max.	Unit
Cortex-M33 in Sleep mode, DSP no clock[1]							
$I_{DDVDDCORE}$	supply current	HCLK=12 MHz VDDCORE=0.7 V	2, 3, 4, 5	-	1.8	-	mA
		HCLK=12 MHz VDDCORE=1.0 V	2, 3, 4, 5	-	4.27	-	mA
		HCLK=24 MHz VDDCORE=1.0 V	2, 3, 4, 5	-	4.78	-	mA
		HCLK=48 MHz VDDCORE=1.0 V	2, 3, 4, 5	-	5.78	-	mA
		HCLK=96 MHz VDDCORE=1.0 V	2, 3, 4, 5	-	7.78	-	mA
		HCLK=192 MHz VDDCORE=0.9 V	2, 3, 4, 5	-	9.66	-	mA
		HCLK=192 MHz VDDCORE=1.0 V	2, 3, 4, 5	-	11.74	-	mA

1. 256 KB SRAM, internal LDO enabled
2. All peripheral clocks gated
3. PLL disabled

4. FRO used as clock source
5. IAR C/C++ Compiler for Arm ver 8.4.2.1.236

T_{amb} = -20 °C to +70 °C, unless otherwise specified.

Table 13. Power consumption in deep sleep mode

Symbol	Parameter	Conditions	Notes	Min	Typ[1], [2]	Max Before/ After[3]	Unit
I_{VDD1V8}	supply current	Deep-sleep mode; SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off	4	-	20	-	µA
$I_{VDDCORE}$	supply current	Deep-sleep mode; SRAM (32 KB) powered, Internal LDO disabled. Array On, Periphery Off T_{amb} = 25 °C	4	-	29	-	µA
		Deep-sleep mode; SRAM (32 KB) powered, Internal LDO disabled. Array On, Periphery Off T_{amb} = 70 °C	4	-	167		µA
$I_{VDDCORE}$	supply current	Deep-sleep mode; SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off T_{amb} = 25 °C	4	-	30	-	µA
		Deep-sleep mode; SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off T_{amb} = 70 °C	4	-	170	-	µA
$I_{VDDCORE}$	supply current	Deep-sleep mode; SRAM (5 MB) powered, Internal LDO disabled. Array On, Periphery Off T_{amb} = 25 °C	4	-	52	85/120[5]	µA
		Deep-sleep mode; SRAM (5 MB) powered, Internal LDO disabled. Array On, Periphery Off T_{amb} =70 °C	4	-	350	-	µA

1. Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). All power supplies = 1.8 V, except USB1_VDD3V3=3.3 V
2. Characterized through bench measurements using typical samples.
3. Tested in production
4. VDDCORE = 0.6 V, RBB Enabled
5. Before and After Max value based on Date Code 2225.

T_{amb} = -20 °C to +70 °C, unless otherwise specified.

Table 14. Power consumption in deep sleep mode

Symbol	Parameter	Conditions	Min	Typ[1], [2]	Max	Unit
I_{VDD_AO1V8}	supply current	Deep-sleep mode; SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off	-	0.60	-	µA
I_{VDDIO_0}	supply current	Deep-sleep mode; SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off	-	1.0	-	µA
I_{VDDIO_1}	supply current	Deep-sleep mode; SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off	-	0.8	-	µA
I_{VDDIO_2}	supply current	Deep-sleep mode; SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off	-	0.26	-	µA
I_{VDDIO_3}	supply current	Deep-sleep mode; SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off	-	0.6	-	µA
I_{VDDIO_4}	supply current	Deep-sleep mode; SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off	-	0.26	-	µA
I_{VDD1V8_1}	supply current	Deep-sleep mode; SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off	-	0.14	-	µA
I_{VREFP}	supply current	Deep-sleep mode; SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off	-	0.02	-	µA
I_{USB1_VDD3V3}	supply current	Deep-sleep mode; SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off	-	1.10	-	µA
$I_{MIPI\_DSI\_VDD18}$	supply current	Deep-sleep mode; SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off	-	0.12	-	µA
$I_{MIPI\_DSI\_VDD11}$	supply current	Deep-sleep mode; SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off		0.15	-	µA
$I_{VDDA\_ADC\_1V8}$	supply current	Deep-sleep mode; SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off	-	2	-	µA
I_{VDDA_BIAS}	supply current	Deep-sleep mode; SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off	-	30	-	nA

1. Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). All power supplies = 1.8 V, except USB1_VDD3V3=3.3 V
2. Characterized through bench measurements using typical samples.

T_{amb} = -20 °C to +70 °C, unless otherwise specified.

Table 15. Power consumption in deep power-down mode[1] and full deep power-down modes

Symbol	Parameter	Conditions	Min	Typ[2], [3]	Max	Unit
I_{VDD_AO1V8}	supply current	Full Deep power-down mode; Internal LDO disabled. RTC Off T_{amb}= *25 °C*	-	0.51	-	µA
		Full Deep power-down mode; Internal LDO disabled. RTC Off T_{amb}= *70 °C*	-	1.79	-	µA
I_{VDDIO_0}	supply curent	Deep power-down mode; Internal LDO disabled. RTC Off	-	2.4	-	µA
I_{VDDIO_1}	supply current	Deep power-down mode; Internal LDO disabled. RTC Off	-	1.68	-	µA
I_{VDDIO_2}	supply current	Deep power-down mode; Internal LDO disabled. RTC Off	-	0.45	-	µA
I_{VDDIO_3}	supply current	Deep power-down mode; Internal LDO disabled. RTC Off	-	0.37	-	µA
I_{VDDIO_4}	supply current	Deep power-down mode; Internal LDO disabled. RTC Off	-	0.44	-	µA
I_{VDD1V8}	supply current	Deep power-down mode; Internal LDO disabled. RTC Off	-	7.8	-	µA
I_{VDD1V8_1}	supply current	Deep power-down mode; Internal LDO disabled. RTC Off	-	0.14	-	µA
I_{VREFP}	supply current	Deep power-down mode; Internal LDO disabled. RTC Off	-	0.01	-	µA
I_{USB1_VDD3V3}	supply current	Deep power-down mode; Internal LDO disabled. RTC Off	-	1.1	-	µA
$I_{MIPI\_DSI\_VDD18}$	supply current	Deep power-down mode; Internal LDO disabled. RTC Off	-	0.1	-	µA
$I_{VDDA\_ADC\_1V8}$	supply current	Deep power-down mode; Internal LDO disabled. RTC Off	-	1	-	µA
I_{VDDA_BIAS}	supply current	Deep power-down mode; Internal LDO disabled. RTC Off	-	0.02	-	µA

1. Deep Power-down mode is not supported in the WLCSP package.
2. Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). All power supplies = 1.8 V, except USB1_VDD3V3=3.3V
3. Characterized through bench measurements using typical samples.

1.8 CoreMark data

Table 16. Coremark data

Parameters	Conditions	Notes	Typ.[1], [2], [3]	Unit
ARM Cortex-M33 in active mode				
CoreMark Score	CoreMark code executed from SRAM; HCLK = 12 MHz	4	3.85	(Iterations/s) / MHz
	HCLK = 24 MHz	4	3.85	(Iterations/s) / MHz
	HCLK = 48 MHz	4	3.85	(Iterations/s) / MHz
	HCLK = 96 MHz	5	3.85	(Iterations/s) / MHz
	HCLK = 192 MHz	5	3.85	(Iterations/s) / MHz

1. Characterized through bench measurements using typical samples.
2. Compiler settings: IAR C/C++ Compiler for Arm ver 8.22.2, optimization level 3, optimized for time on.
3. VDD_AO1V8 = VDD1V8 = VDDIO_0/1/2/3/4 = VDDA_ADC1V8 = VDDA_BIAS = VREFP = 1.8 V. USB1_VDD3V3 = 3.3 V
4. Clock source FRO. PLL disabled
5. Clock source external clock to XTALIN (bypass mode). PLL enabled.

2 System power and clocks

2.1 Power sequence

Following power-on sequence should be followed when using the internal LDO on the i.MX RT500:

1. VDD_AO1V8, VDD1V8, and VDD1V8_1 pins should be powered first. There is no power sequence requirement between powering the VDD_AO1V8 and VDD1V8 pins.
2. VDDA_ADC1V8, VDDA_BIAS, and VREFP can be powered concurrently with VDD_AO1V8 and VDD1V8 or later
3. VDDIO_x pins can be powered concurrently with VDD_AO1V8 and VDD1V8 if these pins are 1.8 V range or later if these pins are 3.3 V range. If the VDDIO_x is not powered concurrently with the VDD1V8, the delta voltage between VDDIO_x and VDD1V8 must be 1.89 V or less.

The VDDCORE pin will be supplied from the internal LDO and the LDO is powered from the VDD1V8. An external capacitor (4.7 uF) must be connected on the VDDCORE pin. USB1_VDD3V3 can be powered at any time, independent of the other supplies.

Following power-on sequence should be followed when using an external PMIC or external IC to drive the VDDCORE pin (internal LDO is disabled, see timing diagram below):

1. VDD_AO1V8, VDD1V8, and VDD1V8_1 pins should be powered first. There is no power sequence requirement between powering the VDD_AO1V8 and VDD1V8 pins.
2. VDDA_ADC1V8, VDDA_BIAS, and VREFP can be powered concurrently with VDD_AO1V8 and VDD1V8 or later.
3. VDDIO_x pins can be powered concurrently with VDD1V8 if these pins are 1.8 V range or later if these pins are 3.3 V range. If the VDDIO_x is not powered concurrently with the VDD1V8, the delta voltage between VDDIO_x and VDD1V8 must be 1.89 V or less.
4. Power up the VDDCORE. The external RESETN should be held low until VDDCORE is valid in the timing diagram.VDDCORE should not be ramped up until after all the other supplies have completed ramp up.

USB1_VDD3V3 can be powered at any time, independent of the other supplies.

Sequence of operations is handled internally so there is no specific timing requirement between the supplies. The time delays caused by any of the bypass capacitors will have no effect on the operation of the part. The internal POR detectors on VDD_AO1V8, VDD1V8 pins, and the Low Voltage Detector on VDDCORE pin, require a fall time of at least 10us (preliminary) to trigger. There is no restriction on the rise time, except for the sequencing defined above.

Table 17. Power-on characteristics

Symbol	Timing Parameter	Description	Min.	Max.	Unit
A	VDDIO_x valid to VDDCORE valid	The delay from when the IO pad voltages become valid to core voltage valid	10	-	µs
B	VDDCORE valid to De-assertion of RESETN	The delay from when the VDD core is valid to when the RESETN can be released	20	-	µs
AA	Mode pin valid	When the mode pins becomes valid. On power-on, the mode pins are reset to 00 and are controlled via a	-	2	µs

Table 17. Power-on characteristics

Symbol	Timing Parameter	Description	Min.	Max.	Unit
		POR circuit in the always-on domain. The timing is from when the VDD_AO1V8 is valid to when the mode pins are reset to 00.			

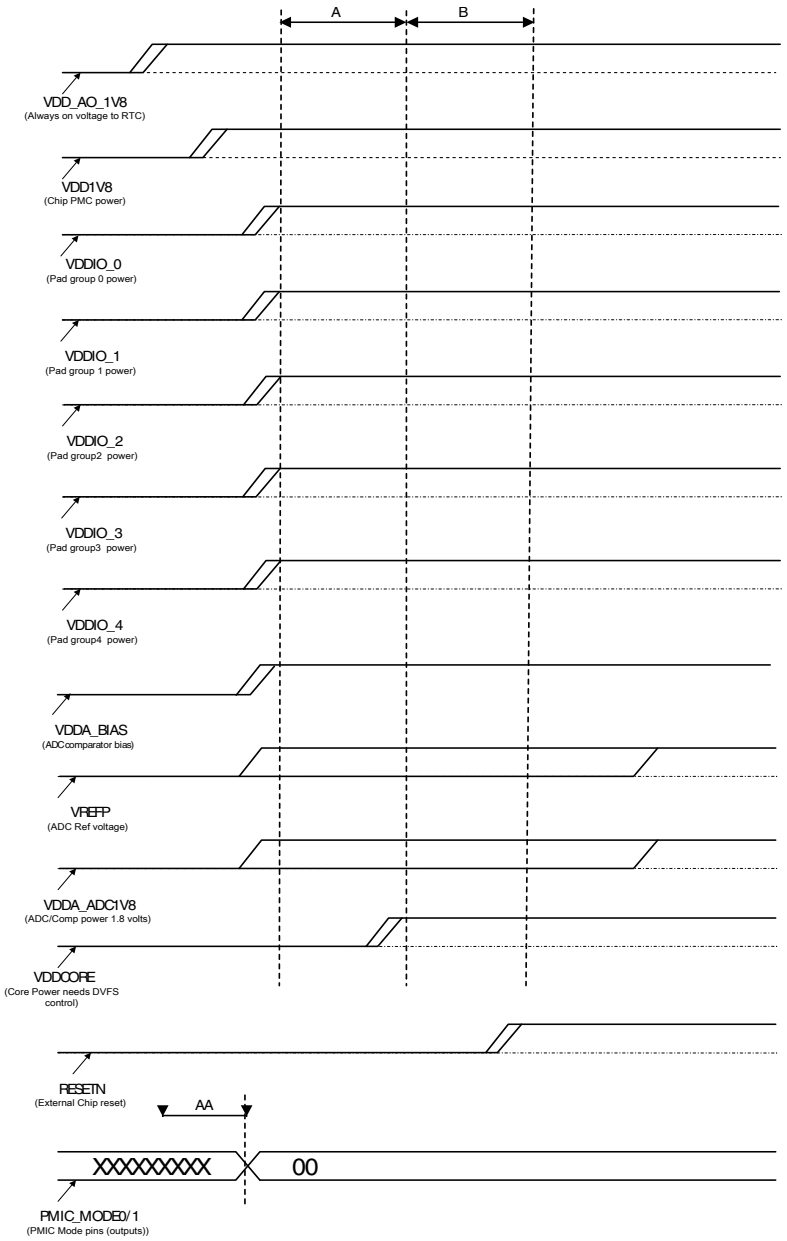


Figure 5. Power-up ramp

2.2 LVD operating requirements

Table 18. VDDCORE supply LVD operating requirments

Symbol	Description	Min.	Typ.	Max.	Unit
V_{LVD_POR}	Rising low-voltage detection on POR	1	-	-	V
V_{LVD_HYS}	Low-voltage detection hysteresis	-	20	-	mV
Rising low-voltage detect[1]					
V_{LVD_R0}	* Level 0 rising (LVDCORELVL=0)	717	-	763	mV
V_{LVD_R1}	* Level 1 rising (LVDCORELVL=1)	732	-	778	mV
V_{LVD_R2}	* Level 2 rising (LVDCORELVL=2)	747	-	793	mV
V_{LVD_R3}	* Level 3 rising (LVDCORELVL=3)	762	-	808	mV
V_{LVD_R4}	* Level 4 rising (LVDCORELVL=4)	776	-	824	mV
V_{LVD_R5}	* Level 5 rising (LVDCORELVL=5)	791	-	839	mV
V_{LVD_R6}	* Level 6 rising (LVDCORELVL=6)	806	-	854	mV
V_{LVD_R7}	* Level 7 rising (LVDCORELVL=7)	820	-	870	mV
V_{LVD_R8}	* Level 8 rising (LVDCORELVL=8)	835	-	885	mV
V_{LVD_R9}	* Level 9 rising (LVDCORELVL=9)	850	-	900	mV
V_{LVD_R10}	* Level 10 rising (LVDCORELVL=10)	864	-	916	mV
V_{LVD_R11}	* Level 11 rising (LVDCORELVL=11)	879	-	931	mV
V_{LVD_R12}	* Level 12 rising (LVDCORELVL=12)	894	-	946	mV
V_{LVD_R13}	* Level 13 rising (LVDCORELVL=13)	908	-	962	mV
V_{LVD_R14}	* Level 14 rising (LVDCORELVL=14)	923	-	977	mV
V_{LVD_R15}	* Level 15 rising (LVDCORELVL=15)	938	-	992	mV

Table continues on the next page...

Table 18. VDDCORE supply LVD operating requirments (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
Falling low-voltage detect[1]					
V_{LVD_F0}	* Level 0 falling (LVDCORELVL=0)	698	-	742	mV
V_{LVD_F1}	* Level 1 falling (LVDCORELVL=1)	713	-	757	mV
V_{LVD_F2}	* Level 2 falling (LVDCORELVL=2)	727	-	773	mV
V_{LVD_F3}	* Level 3 falling (LVDCORELVL=3)	742	-	788	mV
V_{LVD_F4}	* Level 4 falling (LVDCORELVL=4)	757	-	803	mV
V_{LVD_F5}	* Level 5 falling (LVDCORELVL=5)	771	-	819	mV
V_{LVD_F6}	* Level 6 falling (LVDCORELVL=6)	786	-	834	mV
V_{LVD_F7}	* Level 7 falling (LVDCORELVL=7)	801	-	849	mV
V_{LVD_F8}	* Level 8 falling (LVDCORELVL=8)	815	-	865	mV
V_{LVD_F9}	* Level 9 falling (LVDCORELVL=9)	830	-	880	mV
V_{LVD_F10}	* Level 10 falling (LVDCORELVL=10)	845	-	895	mV
V_{LVD_F11}	* Level 11 falling (LVDCORELVL=11)	859	-	911	mV
V_{LVD_F12}	* Level 12 falling (LVDCORELVL=12)	874	-	926	mV
V_{LVD_F13}	* Level 13 falling (LVDCORELVL=13)	889	-	941	mV
V_{LVD_F14}	* Level 14 falling (LVDCORELVL=14)	903	-	957	mV
V_{LVD_F15}	* Level 15 falling (LVDCORELVL=15)	918	-	972	mV

1. The Min. and Max. values include hysteresis, voltage reference and comparator variance.

2.3 Free-running oscillator FRO-250M specifications

Table 19. FRO-250M specifications[1]

Symbol	Characteristic	Min.	Typ.[2]	Max.	Unit
$f_{fro250m}$	FRO-250M frequency (nominal)		250		MHz
$\Delta f_{fro250m}$	• User trim close loop (Closed loop) using accurate clk src	—	—	±1	%
$t_{startup}$	Start-up time	—	58	—	µs
jit_{cyc}	Cycle to cycle jitter	—	90	—	ps
$I_{fro250m}$	Current consumption (VDDCORE)	—	68	—	µA
$I_{fro250m}$	Current consumption (VDD1V8)	—	171	—	µA
V_{min}	Minimum voltage	0.85	—	—	V

1. FBB is enabled. The logic in VDDCORE domain may require higher VDDCORE voltage to be clocked at 250 MHz. FRO divider options 2/4/8 can be used to reduce the FRO frequency to the VDDCORE logic. See General operating conditions for specific Max Freq vs VDDCORE limits.
2. Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

NOTE

Any divided versions of the FRO that are not being used anywhere should be turned off to save power.

2.4 Free-running oscillator FRO-192/96M specifications

Table 20. FRO-192M specifications[1]

Symbol	Characteristic	Min.	Typ.[2]	Max.	Unit
$f_{fro192m}$	FRO-192M frequency (nominal)		192		MHz
Δf_{fro96m}	Frequency deviation • 1T trim (Open loop)	—	—	±2.5[3]	%
	• User trim close loop (Closed loop) using accurate clk src	—	—	1	%
$t_{startup}$	Start-up time	—	75	—	µs
jit_{cyc}	Cycle to cycle jitter	—	105	—	ps
$I_{fro192m}$	Current consumption (VDDCORE)	—	45	—	µA
$I_{fro192m}$	Current consumption (VDD1V8)	—	150	—	µA
$t_{settling}$[4]	Frequency settling time for 1% accuracy	—	—	63	µs
$t_{settling}$[4]	Frequency settling time for 3% accuracy	—	—	28	µs
V_{min}	Minimum voltage	0.8	—	—	V

1. FBB is enabled. The logic in VDDCORE domain may require higher VDDCORE voltage to be clocked at 192 MHz. FRO divider options 2/4/8 can be used to reduce the FRO frequency to the VDDCORE logic. See General operating conditions for specific Max Freq vs VDDCORE limits.

2. Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.
3. Results may vary based on application board and SMT profile. NXP recommends customers perform application-level FRO trim to attain best FRO accuracy.
4. Based on characterization. Not tested in production.

NOTE

Any divided versions of the FRO that are not being used anywhere should be turned off to save power.

Table 21. FRO-96M specifications[1]

Symbol	Characteristic	Min.	Typ.[2]	Max.	Unit
f_{fro96m}	FRO-96M frequency (nominal)		96		MHz
Δf_{fro96m}	Frequency deviation • 1T trim (Open loop)	—	—	±2.5[3]	%
	• User trim close loop (Closed loop) using accurate clk src	—	—	1	%
$t_{startup}$	Start-up time	—	120	—	µs
jit_{cyc}	Cycle to cycle jitter	—	180	—	ps
I_{fro96m}	Current consumption (VDDCORE)	—	23	—	µA
I_{fro96m}	Current consumption (VDD1V8)	—	80	—	µA
$t_{settling}$[4]	Frequency settling time for 1% accuracy		—	42	µs
$t_{settling}$[4]	Frequency settling time for 3% accuracy		—	1	µs
V_{min}	Minimum voltage	0.7	—	—	V

1. FBB is enabled. The logic in VDDCORE domain may require higher VDDCORE voltage to be clocked at 96 MHz. FRO divider options 2/4/8 can be used to reduce the FRO frequency to the VDDCORE logic. See General operating conditions for specific Max Freq vs VDDCORE limits.
2. Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages
3. Results may vary based on application board and SMT profile. NXP recommends customers perform application-level FRO trim to attain best FRO accuracy.
4. Based on characterization. Not tested in production.

2.5 Main/System and Audio PLLs

Table 22. Main/system and audio PLL electrical parameters

Parameter	Min.	Typ.	Max.	Unit
Input reference frequency	5	—	26	MHz
PLL output frequency	80	—	572	MHz
Lock time	—	—	150	µs

Table continues on the next page...

Table 22. Main/system and audio PLL electrical parameters (continued)

Parameter	Min.	Typ.	Max.	Unit
Period jitter (p2p)	—	50	—	ps
PFD period jitter	—	100	—	ps
Duty cycle	45	—	55	%
V_{min}[1]	0.7	—	—	V

1. See General operating conditions for specific Max Freq vs VDDCORE limits.

2.6 Crystal oscillator

T_{amb} = -20 °C to +70 °C; 1.71 V ≤ V_{DD1V8} ≤ 1.89 V.[1]

Table 23. Crystal oscillator characteristics

Symbol	Parameter	Conditions	Min.	Typ.[2]	Max.	Unit
f_{range}	oscillator frequency range[3]		4	—	32	MHz
RF	Crystal feedback resistor4[4]	low-power mode	—	—	—	MΩ
		high-gain mode	—	1	—	MΩ
ESR	Equivalent series resistance		—	—	80	Ω
C_X	XTALIN load capacitance[5]	Crystal oscillator	—	—	-	pF
C_Y	XTALOUT load capacitance[5]	Crystal oscillator	—	—	—	pF
R_S	Series resistor[5]	Crystal oscillator	—	0	—	kΩ
V_{XTALIN}	XTALIN input voltage	External oscillator[6]	0	—	VDD18	V
V_{IH}	XTALIN input high voltage	External oscillator[6]	VDD1V8-0.5	—	VDD1V8	V
V_{IL}	XTALIN input low voltage	External oscillator[6]	VSS	—	0.5	V
t_{DC_XTALIN}	XTALIN input clock duty cycle	External oscillator[6]	40	50	60	%

1. Parameters are valid over operating temperature range unless otherwise specified.
2. Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.
3. Operating range of oscillator. Practical range is 5 MHz to 26 MHz, based on PLL requirements.
4. Feedback resistor only required for High Gain Mode (default). Select Low Power Mode by setting CLKCTL0_SYSOSCCTL0[LP_ENABLE] = 1.
5. See XTAL oscillator
6. Bypass mode uses an external square wave oscillator connected to XTALIN with XTALOUT floating. Set BYPASS_ENABLE in CLKCTL0_SYSOSCCTL0 to select the external clock input.

2.7 RTC oscillator

See RTC oscillator for connecting the RTC oscillator to an external clock source.

T_{amb} = -20 °C to +70 °C; 1.71 ≤ V_{DD_AO1V8} ≤ 1.89

Symbol	Parameter	Conditions	Min.	Typ.[1]	Max.	Unit
f_{RTC}	Input frequency	-	-	32.768	-	kHz
ESR	Equivalent series resistance	Crystal	-	50	100K	kΩ
C_L	Crystal load capacitance	Crystal	9	12.5	12.5	pF
C_{X1}	RTCXIN load capacitance[2]	Crystal		-		pF
C_{X2}	RTCXOUT load capacitance[2]	Crystal		-		pF
t_{start_xtal}	Crystal oscillator start-up time[2]	Crystal	-	250	-	ms
V_{pp_ext}	Peak-to-Peak square wave amplitude	External oscillator[3]	0.7	-	VDD_AO1V8	V
t_{dc_rtcxin}	RTCXIN input clock duty cycle	External oscillator[3]	40	50	60	%
t_{start_bypass}	Bypass oscillator start-up time	External oscillator[3]	-	1	-	ms

1. Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages
2. Proper PCB layout procedures must be followed to achieve specifications. See RTC oscillator
3. To bypass with an external source, apply an input square wave on RTCXIN and float RTCXOUT. VIH and VIL levels do not apply to this input.

2.8 External Clock Input (CLKIN) pin

T_{amb} = -20 °C to +70 °C; 1.71 ≤ VDDIO ≤ 1.89 V

Table 24. Dynamic characteristic: CLKIN

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
F_{CLKIN}	input frequency	-	-	-	50	MHz
V_{IH}	CLKIN input high voltage	external oscillator[1].	VDD1V8-0.5	-	VDD1V8	V

Table continues on the next page...

Table 24. Dynamic characteristic: CLKIN (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
V_{IL}	CLKIN input low voltage	external oscillator[1]	VSS	-	0.5	V

1. Connect an external square wave oscillator to the pin configured as the CLKIN input. Write CLKCTL0_SYSOSCBYPASS[SEL]=0b001 to select CLKIN as the external clock input.

2.9 External Master Clock (MCLK) pin

T_{amb} = -20 °C to +70 °C; 1.71 ≤ VDDIO ≤ 1.89 V

Table 25. Dynamic characteristic: MCLK

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
F_{MCLK}	input frequency	-	-	-	25	MHz
F_{MCLK}	output frequency	-	-	-	25	MHz

2.10 Internal low-power oscillator (1 MHz)

The LPOSC is trimmed to ±10% accuracy over the entire voltage and temperature range.

T_{amb} = -20 °C to +70 °C; 1.71 ≤ V_{DD} ≤ 1.89 V

Table 26. LPOSC characteristics

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$f_{osc\ (RC)}$	LPOSC clock frequency	-	0.9	1	1.1	MHz
$t_{startup}$	Start-up time	-	-	105	-	µs

1. Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

3 System modules

3.1 Reset timing parameters

The following figure shows the reset timing and Table 27 lists the timing parameters.

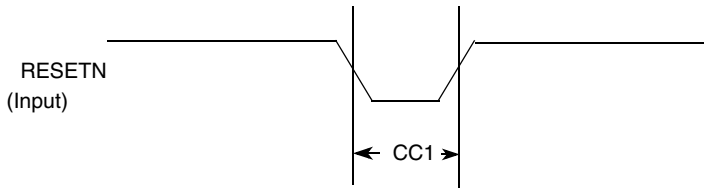


Figure 6. Reset timing diagram

Table 27. Reset timing parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of POR_B to be qualified as valid	40	-	ns

3.2 Serial Wire Debug (SWD) timing specifications

Table 28. SWD timing specifications

Symbol	Description	Min.	Max.	Unit
J1	SWD_CLK frequency of operation	0	25	MHz
J2	SWD_CLK cycle period	1000/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	37	ns
J12	SWD_CLK high to SWD_DIO high-Z	2	—	ns

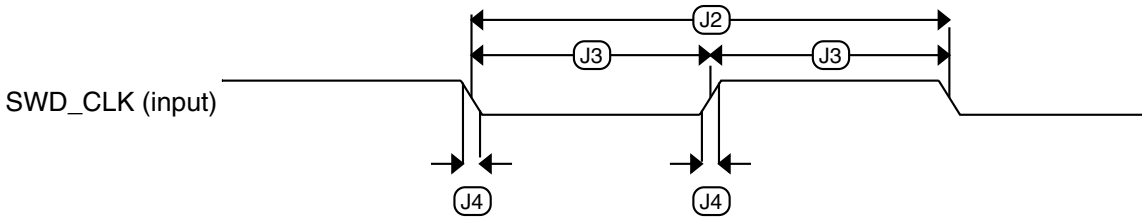


Figure 7. Serial wire clock input timing

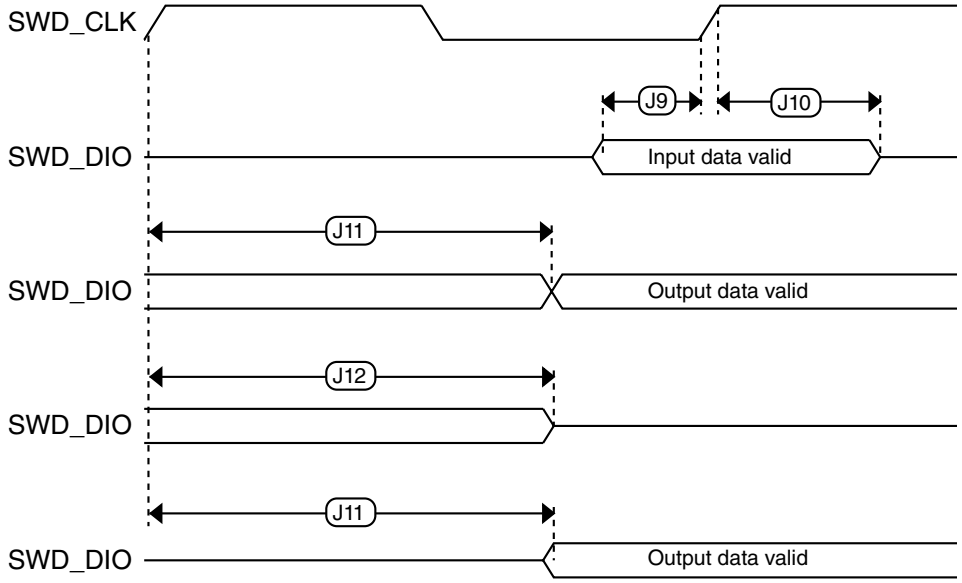


Figure 8. Serial wire data timing

3.3 JTAG timing specifications

Table 29. JTAG timing specifications

Symbol	Parameter	Min.[1]	Max.	Unit
J1	TCLK frequency of operation			
	• Boundary Scan	0	10	MHz
	• JTAG	0	25	MHz
J2	TCLK cycle period	1000/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG	20	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	5	—	ns
J7	TCLK low to boundary scan output data valid	—	28	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	10.5	—	ns
J10	TMS, TDI input data hold time after TCLK rise	2.5	—	ns
J11	TCLK low to TDO data valid	—	19	ns

Table continues on the next page...

Table 29. JTAG timing specifications (continued)

Symbol	Parameter	Min.[1]	Max.	Unit
J12	TCLK low to TDO high-Z	2	—	ns
J13	TRST (active-low) assert time	100	—	ns
J14	TRST (active-low) setup time (negation) to TCLK high	8	—	ns

1. For details about JTAG/Boundary Scan, see i.MX RT500 Reference Manual.

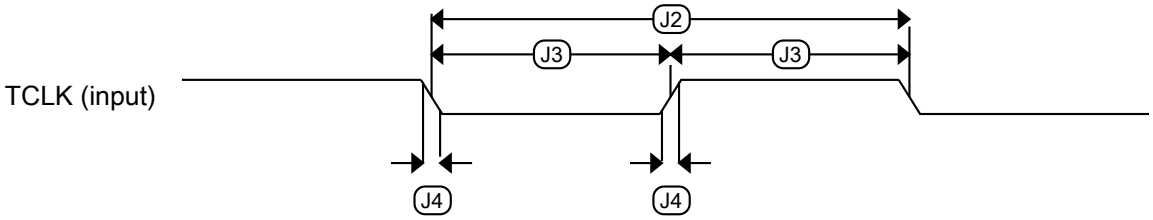


Figure 9. Test clock input timing

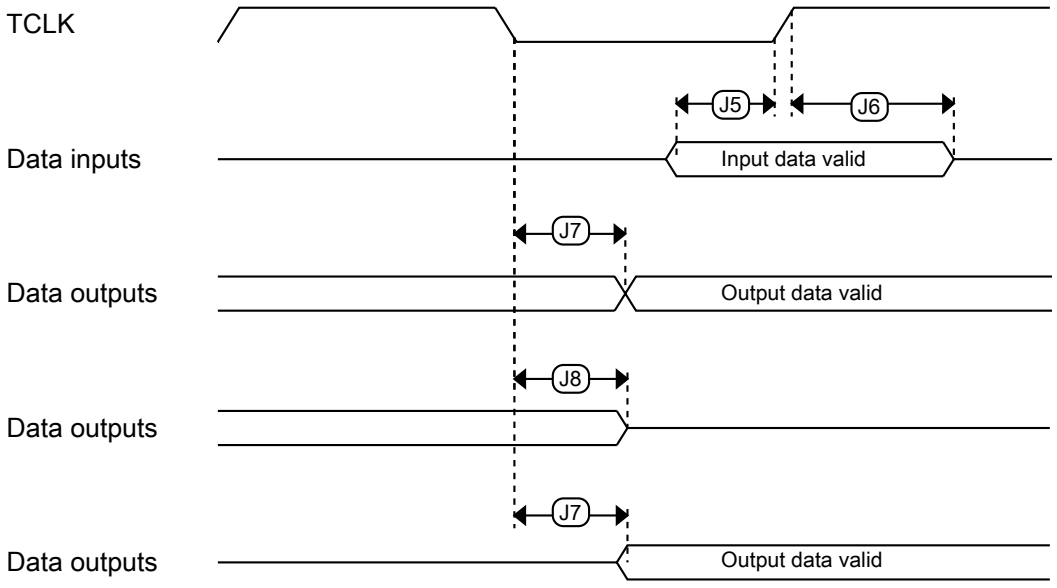


Figure 10. Boundary scan (JTAG) timing

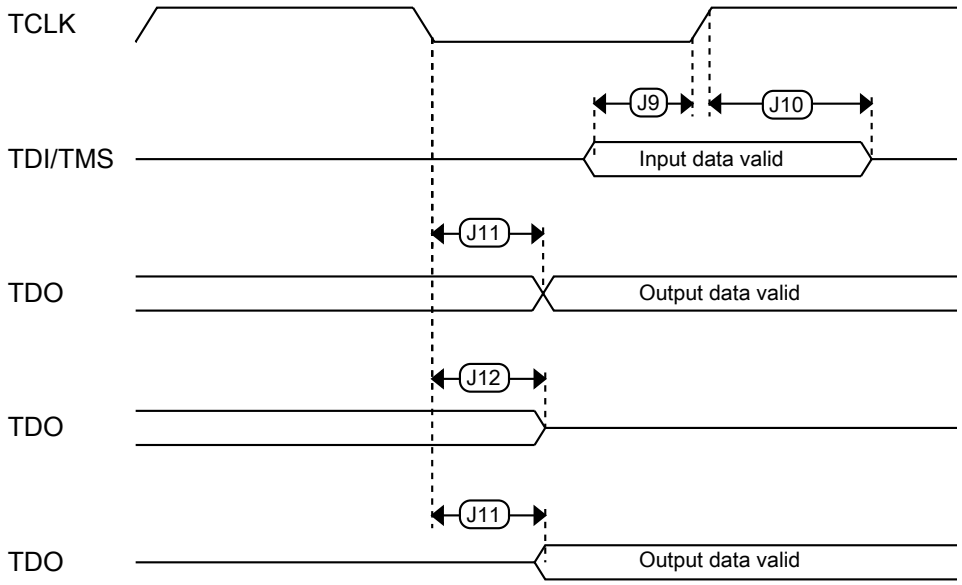


Figure 11. Test Access Port timing

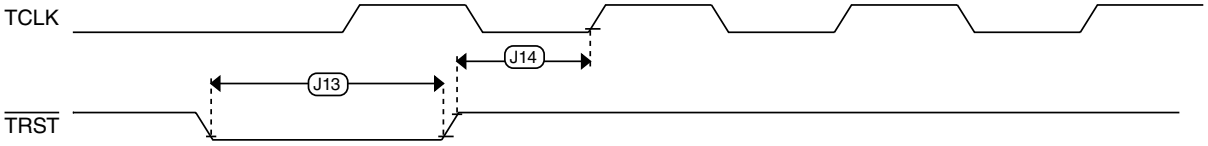


Figure 12. TRST (active-low) timing

3.4 Wake-up process

V_{DD} = 1.8 V;T_{amb} = 25 °C; using FRO as the system clock.

Table 30. Typical wake-up times from low power modes

Symbol	Parameter	Conditions	Notes	Min.	Typ.[1]	Max.	Unit
t_{wake}	wake-up time	from sleep mode, 200 MHz	2, 3	-	150	-	µs
t_{wake}	wake-up time	from deep-sleep mode, using RESETN.	2,3	-	120	-	µs

Table continues on the next page...

Table 30. Typical wake-up times from low power modes (continued)

Symbol	Parameter	Conditions	Notes	Min.	Typ.[1]	Max.	Unit
		from deep-sleep mode, using PMIC_IRQ_N.	2,3	-	120	-	µs
t_{wake}	wake-up time	from full deep power-down mode, using RESETN	4	-	8.64	-	ms
		from full deep power-down mode, using PMIC_IRQ_N	4	-	8.64	-	ms

1. Typical ratings are not guaranteed. The values listed are at room temperature (25 C), nominal supply voltages.
2. The wake-up time measured is the time between when a GPIO input pin is triggered to wake the device up from the low power modes and from when a GPIO output pin is set in the interrupt service routine (ISR) wake-up handler.
3. FRO disabled in Deep Sleep and re-enabled upon wake-up , all peripherals including the PLL are disabled. VDDCORE (Active 1V/ Deep Sleep 0.6V), 5 MB SRAM retained.
4. Wake up from deep power-down causes the part to go through entire reset process. The wake-up time measured is the time between when the Wake-Up pin is triggered to wake the device up and when a GPIO output pin is set in the reset handler.

4 External memory interfaces

4.1 FlexSPI Flash interface

Table 31. FlexSPI ipg_clk_sfck maximum frequency vs. VDDCORE1

FlexSPI frequency	Min.	Typ.	Max.	Unit
VDDCORE=0.8V	—	—	192	MHz
VDDCORE=0.9V	—	—	332	MHz
VDDCORE=1.0 V	—	—	360	MHz
VDDCORE=1.1V	—	—	400	MHz

1. Applies only to RX Clock Source = 3 with external DQS. SCLK maximum frequency in this mode is 200 MHz

Tamb = -20 C to +70 C, VDDIO_x = 1.71 V to 1.89V; CL = 5 pF balanced loading on all pins; Full Drive Mode on all pins, Input slew = 1 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge.

In FlexSPI DDR mode, serial root clock ipg_clk_sfck is twice the frequency of SCLK output clock to memory. ipg_clk_sfck and SCLK frequencies are the same SDR mode.

Table 32. Dynamic characteristics: FlexSPI flash interface[1]

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SDR mode						
f_{clk}	clock frequency	Transmit	—	—	200	MHz
		RX clock source = 0	—	—	60	MHz
		RX clock source = 1	—	—	116	MHz
		RX clock source = 3	—	—	200	MHz
t_{DS}	data set-up time	RX clock source = 0 (internal dummy read strobe and loopbacked internally)	6	—	—	ns
		RX clock source = 1 (internal dummy read strobe and loopbacked from DQS pad)	1	—	—	ns
		source = 3 (external DQS, Flash provides read strobe)	0	—	0.6	ns
t_{DH}	data hold time	RX clock source = 0 (internal dummy read strobe and loopbacked internally)	1	—	—	ns
		RX clock source = 1 (internal dummy read strobe and loopbacked from DQS pad)	0	—	—	ns
		source = 3 (external DQS, Flash provides read strobe)	0	—	—	ns
$t_{V(Q)}$	data output valid time		0	—	3	ns
DDR Mode (with and without DQS)						
f_{clk}	clock frequency	Transmit	—	—	200	MHz
		RX clock source = 0	—	—	30	MHz
		RX clock source = 1	—	—	58	MHz
		RX clock source = 3, with external DQS.	—	—	200	MHz
t_{DS}	data set-up time	RX clock source = 0 (internal dummy read strobe and loopbacked internally)	6	—	—	ns

Table continues on the next page...

Table 32. Dynamic characteristics: FlexSPI flash interface1 (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
		RX clock source = 1 (internal dummy read strobe and loopbacked from DQS pad)	1	—	—	ns
		source = 3 (external DQS, Flash provides read strobe)	0	—	0.6	ns
t_{DH}	data hold time	RX clock source = 0 (internal dummy read strobe and loopbacked internally)	1	—	—	ns
		RX clock source = 1 (internal dummy read strobe and loopbacked from DQS pad)	0	—	—	ns
		source = 3 (external DQS, Flash provides read strobe)	0	—	—	ns
$t_{V(Q)}$	data output valid time		0	—	—	ns

1. Based on simulation; not tested in production.

Following are the FlexSPI timing diagrams for SDR and DDR input and output timing modes.

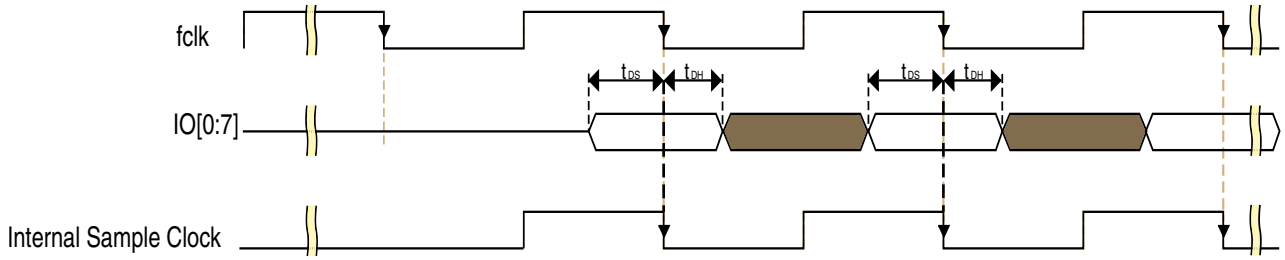


Figure 13. SDR mode (input timing, mode 0 and 1)

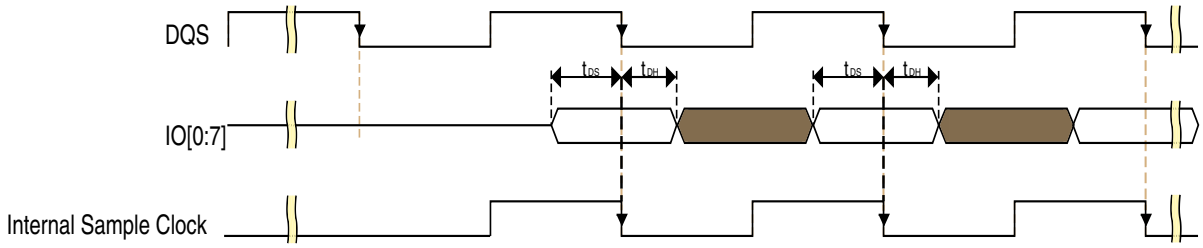


Figure 14. SDR mode (input timing, mode 3)

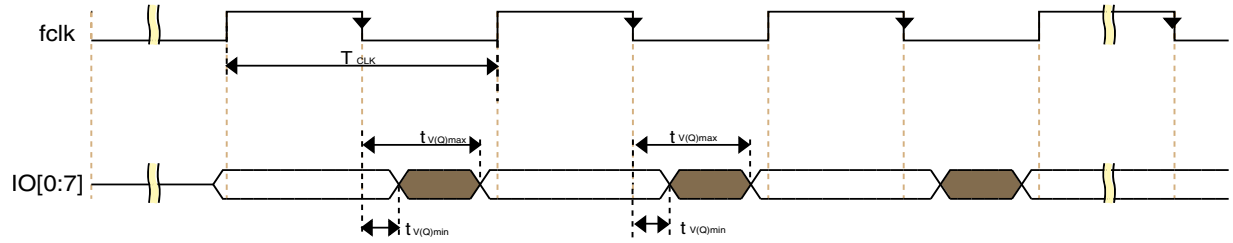


Figure 15. SDR mode (output timing, mode 0 and 1)

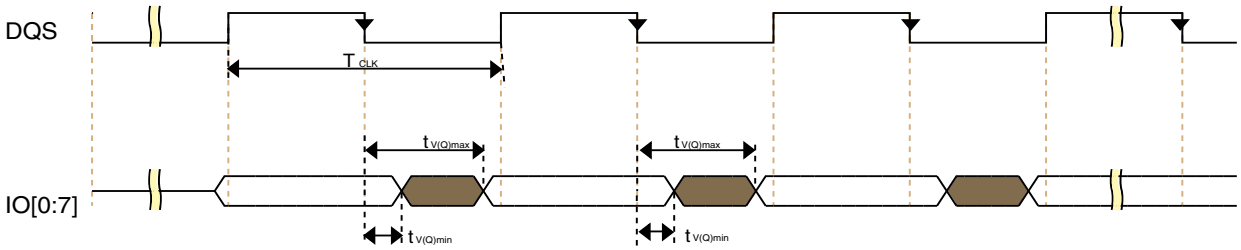


Figure 16. SDR mode (output timing, mode 3)

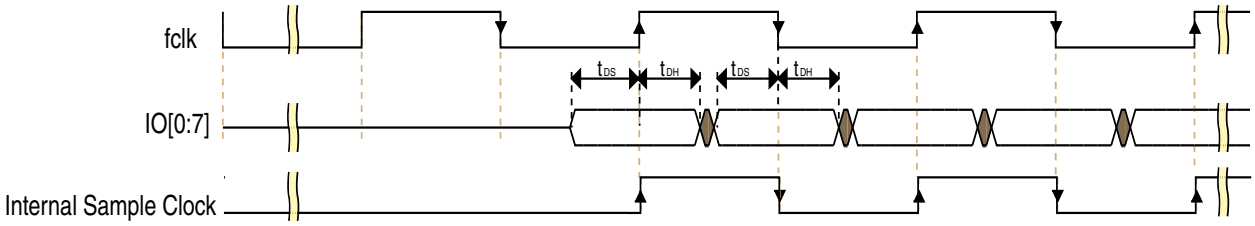


Figure 17. DDR mode (input timing, mode 0 and 1)

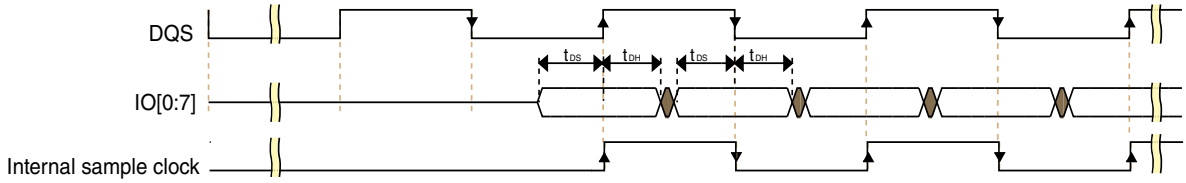


Figure 18. DDR mode (input timing, mode 3)

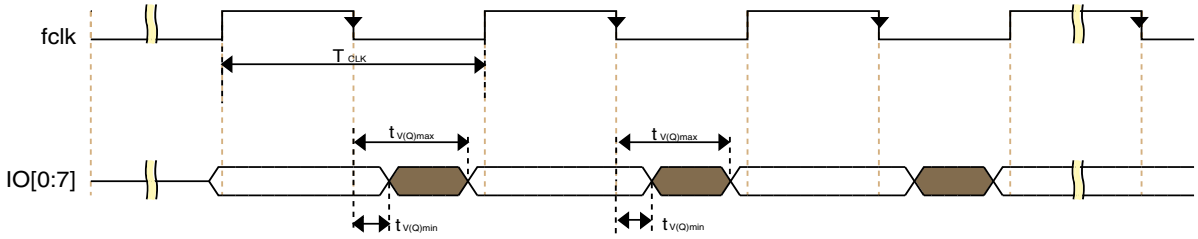


Figure 19. DDR mode (output timing, mode 0 and 1)

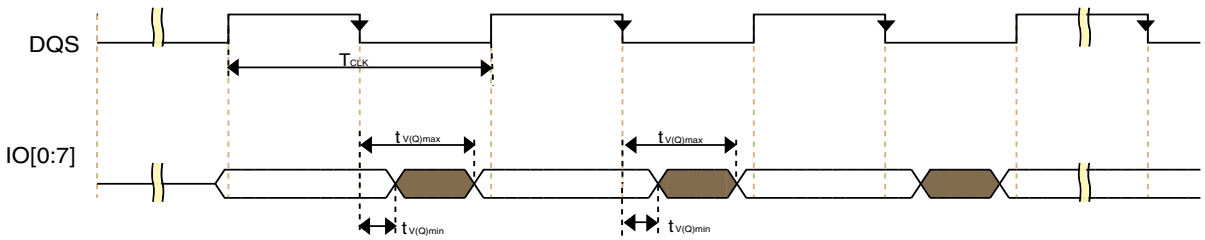


Figure 20. DDR mode (output timing, mode 3)

5 Display and graphics

5.1 LCDIF

T_{amb} = -20 °C to 70 °C; V_{DD} = 1.8 V; C_L = 30 pF. Simulated values.

Table 33. LCDIF characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{clk}	clock frequency	on pin LCD_DCLK	-	-	60	MHz
$t_{v(Q)}$	data output valid time	on all LCD output pins	0.3	-	4.5	ns

5.2 MIPI DSI timing

The i.MX RT500 conforms to the MIPI D-PHY electrical specifications MIPI DSI Version 1.01 and D-PHY specification Rev. 1.0 (and also DPI version 2.0, DBI version 2.0, DSC version 1.0a at protocol layer) for MIPI display port x2 lanes.

5.3 Flexible IO controller (FlexIO)

Table 34. FlexIO timing specifications

Symbol	Description	Min	Typ.	Max.	Unit	Notes
t_{ODS}	Output delay skew between any two FlexIO_Dx pins configured as outputs that toggle on same internal clock cycle	0	—	1.957	ns	1
t_{IDS}	Input delay skew between any two FlexIO_Dx pins configured as inputs that are sampled on the same internal clock cycle	0	—	1.403	ns	1

1. Assumes pins muxed on same VDD_IO domain with same load

6 Analog characteristics

6.1 12-bit ADC characteristics

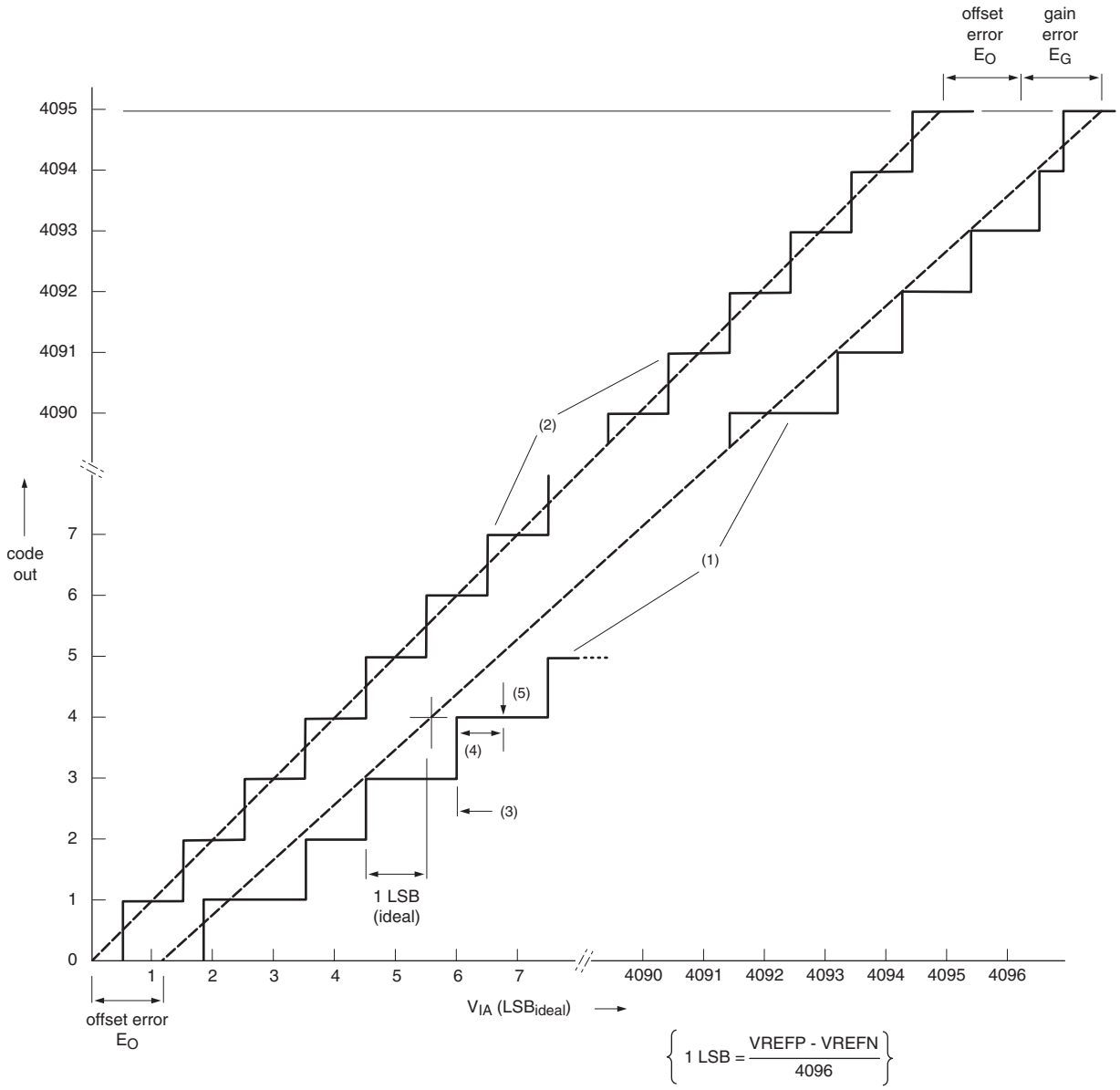
T_{amb} = -20 °C to +70 °C; VDDA_ADC1V8 = VDDA_BIAS = VREFP = 1.8 V; V_{SSA} = VREFN = GND. ADC calibrated at T_{amb} = 25 °C.

Table 35. 12-bit ADC static characteristics

Symbol	Parameter	Conditions	Notes	Min	Typ[1]	Max	Unit
VADIN	analog input voltage		See Figure 22	VREFN	-	VREFP	V
$f_{clk(ADC)}$	ADC clock frequency				-	60	MHz
f_s	sampling frequency			-	-	1	Msamples/s
$C_{samples}$	Sample cycles			3.5	-	131.5	
$C_{compare}$	Fixed compare cycles			-	17.5	-	cycles
$C_{conversion}$	Conversion cycles			$C_{conversion} = C_{samples} + C_{compare}$			cycles
CADIN	Analog input capacitance		[2], See Figure 22	-	4.5	-	pF
RADIN	Input resistance		See Figure 22	-	500	-	Ω
RAS	Analog source resistance		3	-	-	5	kΩ
E_D	differential linearity error		4, 5	-	<±1	-	LSB
$E_{I(adj)}$	integral non-linearity	$f_{clk(ADC)}$ = 22 MHz Sample Time select (STS bit in CMDH register) = 0	4, 6	-	<±1.1	-	LSB
E_O	offset error		4, 7	-	±0.01	±0.02	%FSV
E_G	Gain error		4, 8	-	-0.16	-0.56	%FSV

1. Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.
2. CADIN represents the external capacitance on the analog input channel for sampling speeds of 1.0 Msamples/s. No parasitic capacitances included.

3. This resistance is external to the MCU. To achieve the best results, the analog source resistance must be kept as low possible. The results in this data sheet were derived from a system that had less than 15 Ω analog source resistance. See Figure 1
4. Based on characterization; not tested in production.
5. The differential linearity error (ED) is the difference between the actual step width and the ideal step width. See Figure 1.
6. The integral non-linearity ($E_{I(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 1.
7. The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 1.
8. The gain error (EG) is the difference between the straight-line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 1.



(1) Example of an actual transfer curve.
(2) The ideal transfer curve.
(3) Differential linearity error (E_D).
(4) Integral non-linearity ($E_{I(adj)}$).
(5) Center of a step of the actual transfer curve.

Figure 21. 12-bit ADC characteristics

6.1.1 ADC input impedance

The following figure shows the ADC input impedance for this device.

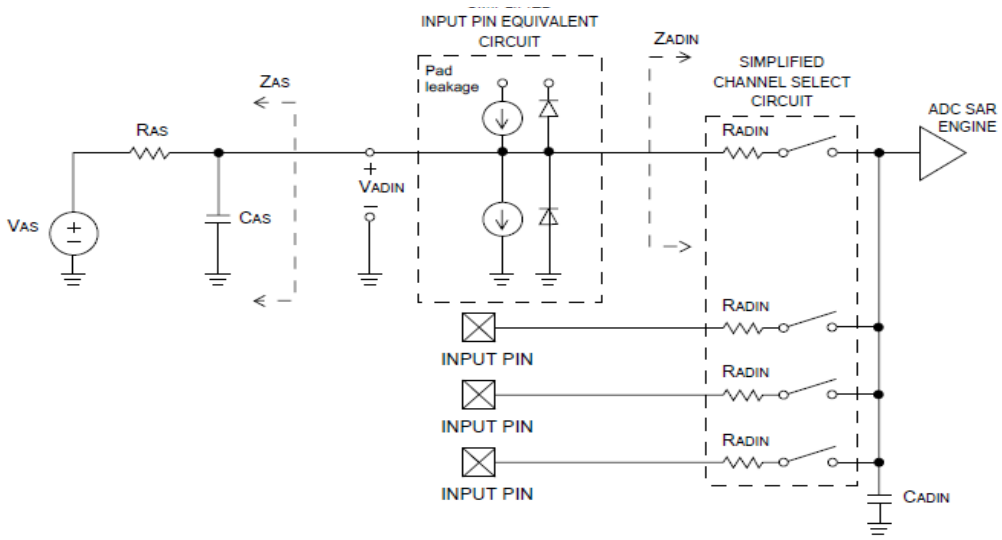


Figure 22. ADC input impedance

6.2 ADC temperature sensor

Table 36. Temperature sensor static and dynamic characteristics (VDDA_BIAS = 1.8 V, All other supplies = 1.8 V)

Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Unit
DT_{sen}	sensor temperature accuracy	T_{amb} = -20 °C to 70 °C	1	-	2.1	2.77	°C

1. Absolute temperature accuracy. Based on characterization. Not tested in production

Table 37. Temperature sensor Linear-Least-Square (LLS) fit parameters (VDDA_BIAS = 1.8 V, All other supplies = 1.8 V)

Fit parameter	Conditions	Notes	Min	Typ	Max	Unit
LLS slope	T_{amb} = -20 °C to 70 °C	1, 2	-	-1.5738	-	mV/°C
LLS intercept at 0° C	Tamb = -20 °C to 70 °C	1, 2	-	809.55	-	mV
LLS intercept at 25 °C	Tamb = -20 °C to 70 °C	1, 2	-	770.4	-	mV

1. Based on characterization, Not tested in production.
2. Equation: Temp = 25 - ((Vtemp -Vtemp25)/m) Where: VTEMP is the voltage of the temperature sensor channel at the ambient temperature VTEMP is the voltage of the temperature sensor channel at 25°C and VDD = 1.8 V m is the voltage versus temperature slope in V/°C.

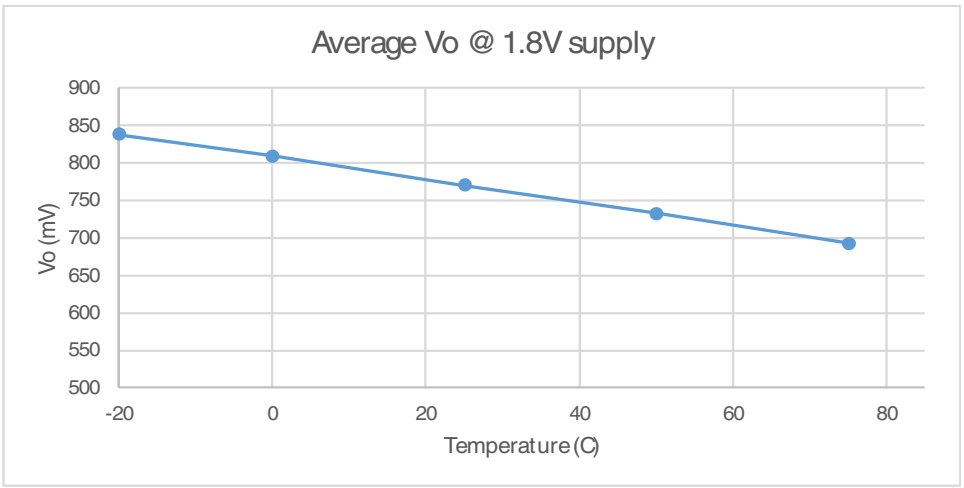


Fig 29. Average Vo @ 1.8V supply

Figure 23. Average Vo @ 1.8V supply

6.3 Comparator characteristics

T_{amb} = -20 C to +70 C; V_{DD} = 1.8 V.

Table 38. Comparator characteristics

Symbol	Parameter	Conditions	Notes	Min.	Typ.[1]	Max.	Unit
Static characteristics							
Voffset	offset voltage	V_{IC} = 0.1 V; V_{DD} = 1.8 V		—	6	—	mV
		V_{IC} = 0.9 V; V_{DD} = 1.8 V		—	7	—	mV
		V_{IC} = 1.7 V; V_{DD} = 1.8 V		—	9	—	mV
Dynamic characteristics							
t_{PD}	propagation delay	HIGH to LOW; V_{DD} = 1.8 V; T_{amb} = 25 °C V_{IC} = 0.1 V; 100 mV overdrive input	2	—	2	—	µs
		V_{IC} = 0.1 V; rail-to-rail input		—	915	—	ns
		V_{IC} = 0.9 V; 100 mV overdrive input	2	—	525	—	ns
		V_{IC} = 0.9 V; rail-to-rail input		—	600	—	ns

Table continues on the next page...

Table 38. Comparator characteristics (continued)

Symbol	Parameter	Conditions	Notes	Min.	Typ.[1]	Max.	Unit
		V_{IC} = 1.7 V; 100 mV overdrive input	2	—	500	—	ns
		V_{IC} = 1.7 V; rail-to-rail input		—	350	—	ns
t_{PD}	propagation delay	HIGH to LOW; V_{DD} = 1.8 V; T_{amb} = 25 °C V_{IC} = 0.1 V; 100 mV overdrive input	2	—	270	—	ns
		V_{IC} = 0.1 V; rail-to-rail input		—	310	—	ns
		V_{IC} = 0.9 V; 100 mV overdrive input	2	—	340	—	ns
		V_{IC} = 0.9 V; rail-to-rail input		—	210	—	ns
		V_{IC} = 1.7 V; 100 mV overdrive input	2	—	150	—	ns
		V_{IC} = 1.7 V; rail-to-rail input		—	125	—	ns
t_{PD}	propagation delay	LOW to HIGH; VV_{DD} = 1.8 V; T_{amb} = 25 °C, V_{IC} = 0.1 V; 100 mV overdrive input		—	5.8	—	µs
		V_{IC} = 0.1 V; rail-to-rail input		—	470	—	ns
		V_{IC} = 0.9 V; 100 mV overdrive input	2	—	750	—	ns
		V_{IC} = 0.9 V; rail-to-rail input		—	600	—	ns
		V_{IC} = 1.7 V; 100 mV overdrive input	2	—	5.5	—	µs
		V_{IC} = 1.7 V; rail-to-rail input		—	1.25	—	µs
t_{PD}	propagation delay	LOW to HIGH; VV_{DD} = 1.8 V; T_{amb} = 25 °C, V_{IC} = 0.1 V; 100 mV overdrive input		—	105	—	ns
		V_{IC} = 0.1 V; rail-to-rail input		—	115	—	ns
		V_{IC} = 0.9 V; 100 mV overdrive input	2	—	110	—	ns
		V_{IC} = 0.9 V; rail-to-rail input		—	120	—	ns
		V_{IC} = 1.7 V; 100 mV overdrive input	2	—	110	—	ns

Table continues on the next page...

Table 38. Comparator characteristics (continued)

Symbol	Parameter	Conditions	Notes	Min.	Typ.[1]	Max.	Unit
		V_{IC} = 1.7 V; rail-to-rail input		—	120	—	ns
V_{hys}	hysteresis voltage[3]	HYSTCRT[1:0] = 01	—	—	13		mV
		HYSTCRT[1:0] = 10		—	27	—	mV
		HYSTCRT[1:0] = 11		—	35	—	mV

1. Characterized on typical samples, not tested in production
2. 100 mV overdrive corresponds to a square wave from 50 mV below the reference (VIC) to 50 mV above the reference.
3. Input hysteresis is relative to the reference input channel and is software programmable.

7 Communication interfaces

7.1 USART interface

Excluding delays introduced by external device and PCB, the maximum supported bit rate for USART master synchronous mode is 20 Mbit/s, and the maximum supported bit rate for USART slave synchronous mode is 20.0 Mbit/s.

The actual USART bit rate depends on the delays introduced by the external trace, the external device, system clock (HCLK), and capacitive loading.

T_{amb} = -20 °C to 70 °C; V_{DD} = 1.71 V to 1.89 V; C_L = 20 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge.

Table 39. USART interface characteristics1

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
USART master (in synchronous mode)						
$t_{su(D)}$	data input set-up time	-	0.087	-	-	ns
$t_{h(D)}$	data input hold time	-	0.03	-	-	ns
$t_{v(Q)}$	data output valid time	-	14.058	-	16.412	ns
USART slave (in synchronous mode)						
$t_{su(D)}$	data input set-up time	-	0.087	-	-	ns
$t_{h(D)}$	data input hold time	-	0.03	-	-	ns
$t_{v(Q)}$	data output valid time	-	0	-	3.684	ns

1. Based on simulation; not tested in production

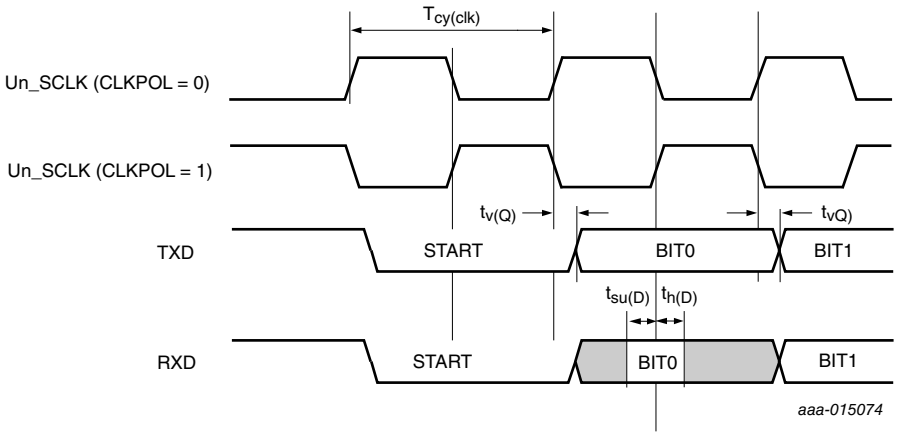


Figure 24. USART timing

7.2 I²C-bus

T_{amb} = -20 °C to +70 °C; 1.71 V ≤ V_{DD} ≤ 1.89 V.[1]

Table 40. I²C-bus pins[1]

Symbol	Parameter	Notes	Conditions	Min.	Max.	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus	0	1	MHz
t_f	fall time	2, 3, 4, 5	Both SDA and SCL signals Standard-mode	-	300	ns
			Fast-mode	20x(VDD/3.6V)	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock	6	Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock	6	Standard-mode	4	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time	7, 2, 8	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time	9, 10	Standard-mode	4.7	-	ns

Table continues on the next page...

1. Parameters are valid over operating temperature range unless otherwise specified. See the I2C-bus specification UM10204 for details.

Table 40. I²C-bus pins1 (continued)

Symbol	Parameter	Notes	Conditions	Min.	Max.	Unit
			Fast-mode	0.6	-	ns
			Fast-mode Plus	0.26	-	ns

1. Guaranteed by design. Not tested in production.
2. A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the VIH(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. Cb = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall times are allowed.
4. The maximum tf for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage tf is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
5. In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
6. The MSTTIME register allows programming of certain times for the clock (SCL) high and low times. Please see i.MX RT500 Low-Power Crossover MCU Reference Manual for further details.
7. $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.
8. The maximum $t_{HD;DAT}$ could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.
9. $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.
10. A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr(max) + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

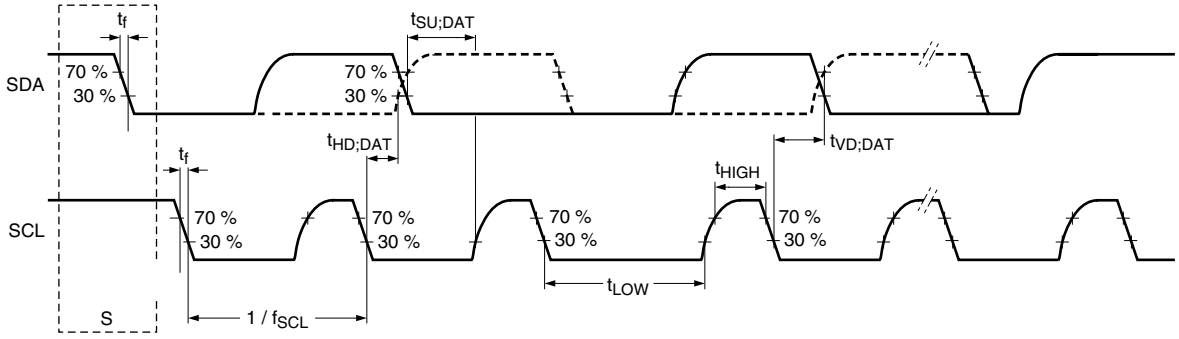


Figure 25. I²C bus pins clock timing

7.3 I²S-bus interface

T_{amb} = -20 °C to 70 °C; V_{DD} = 1.71 V to 1.89 V; C_L = 30 pF balanced loading on all pins; Input slew = 1.0 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge.

Table 41. I²S-bus interface pins[1], [2]

Symbol	Parameter	Conditions	Notes	Min.	Typ.[3]	Max.	Unit
Common to master and slave							
t_{WH}	pulse width HIGH	on pins I2Sx_TX_SCK and I2Sx_RX_SCK[4]					
				45%	-	55%	TCLK Period
t_{WL}	pulse width LOW	on pins I2Sx_TX_SCK and I2Sx_RX_SCK[4]					
				45%	-	55%	TCLK Period
Master							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	5				
				6.798	-	17.505	ns
		on pin I2Sx_WS					
				5	-	16.055	ns
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	5	1.3	-	-	ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	5	2.9	-	-	ns
Slave							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	5	13.8		23.6	ns
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	5	4.7	-	-	ns
		on pin I2Sx_WS		0.9	-	-	ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	5	0	-	-	ns
		on pin I2Sx_WS		0	-	-	ns

1. Based on simulation; not tested in production.
2. The Flexcomm Interface function clock frequency should not be above 100 MHz. See the data rates section in the I2S chapter in the i.MX RT500 Low-Power Crossover MCU Reference Manual (IMXRT500RM) to calculate clock and sample rates.
3. Typical ratings are not guaranteed.
4. Based on simulation. Not tested in production.
5. Clock Divider register (DIV) = 0x0.

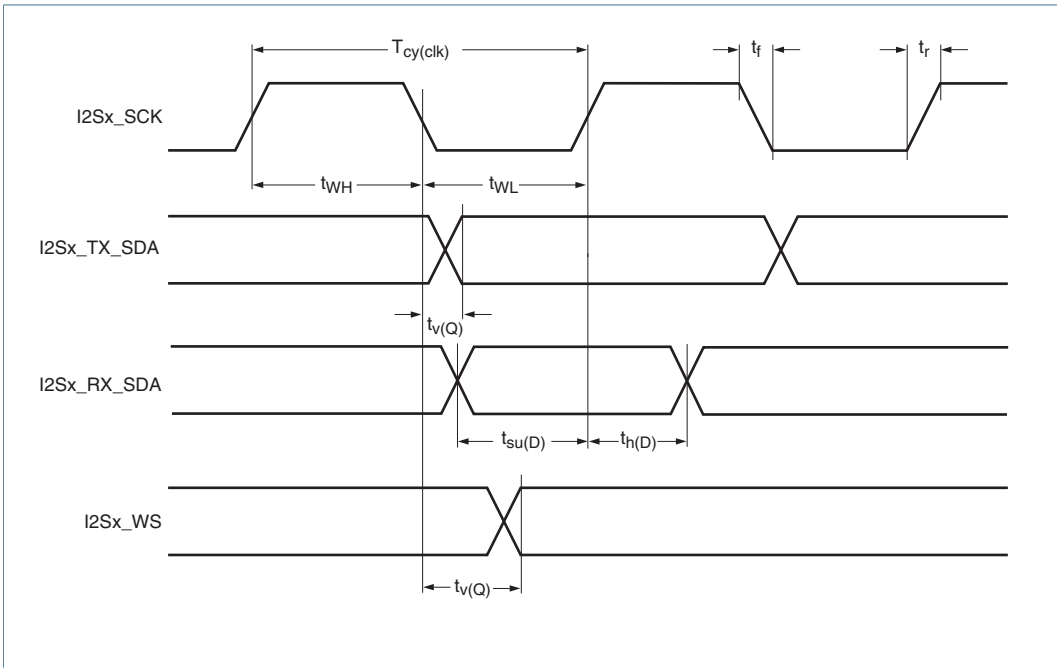


Figure 26. I²S-bus timing (master)

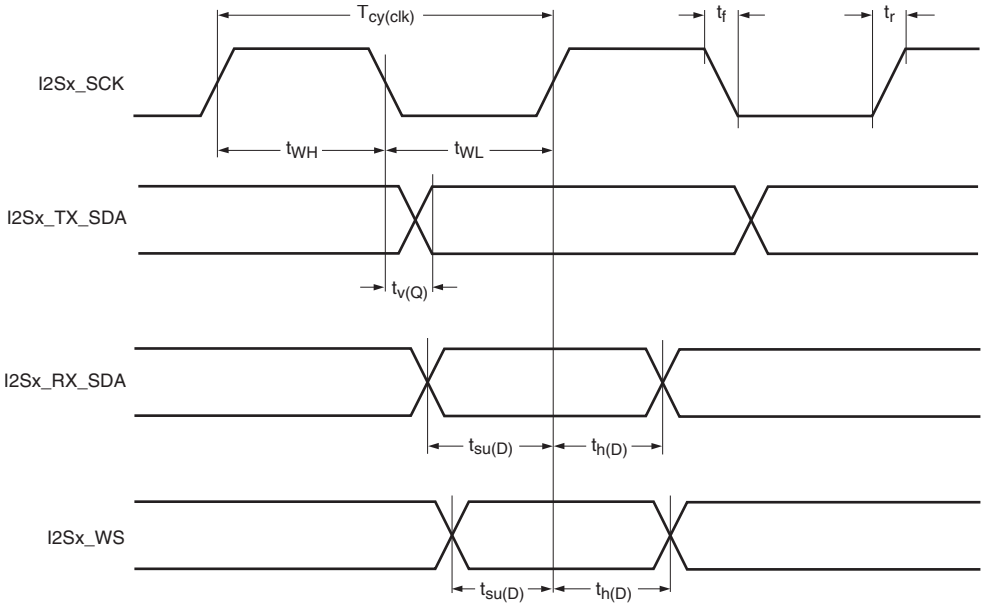


Figure 27. I²S-bus timing (slave)

7.4 SPI interfaces (Flexcomm interfaces 0-8, 10-12)

The actual SPI bit rate depends on the delays introduced by the external trace, the external device, system clock (HCLK), and capacitive loading.

Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI master mode (transmit/receive) is 25 Mbit/s and the maximum supported bit rate for SPI slave mode (transmit/receive) is 25 Mbit/s.

T_{amb} = -20 °C to 70 °C; 1.71 V ≤ V_{DD}≤ 1.89 V; C_L = 10 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = standard mode for all pins;. Parameters sampled at the 50 % level of the rising or falling edge.

Table 42. SPI interfaces[1]

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
SPI master							
t_{DS}	data set-up time	-		5.0	-	-	ns
t_{DH}	data hold time	-		0	-	-	ns
$t_{v(Q)}$	data output valid time	-		0	-	13.0	ns
SPI slave							
t_{DS}	data set-up time	-		5.0	-	-	ns
t_{DH}	data hold time	-		0	-	-	ns
$t_{v(Q)}$	data output valid time	-		0	-	13	ns

1. Based on simulation; not tested in production

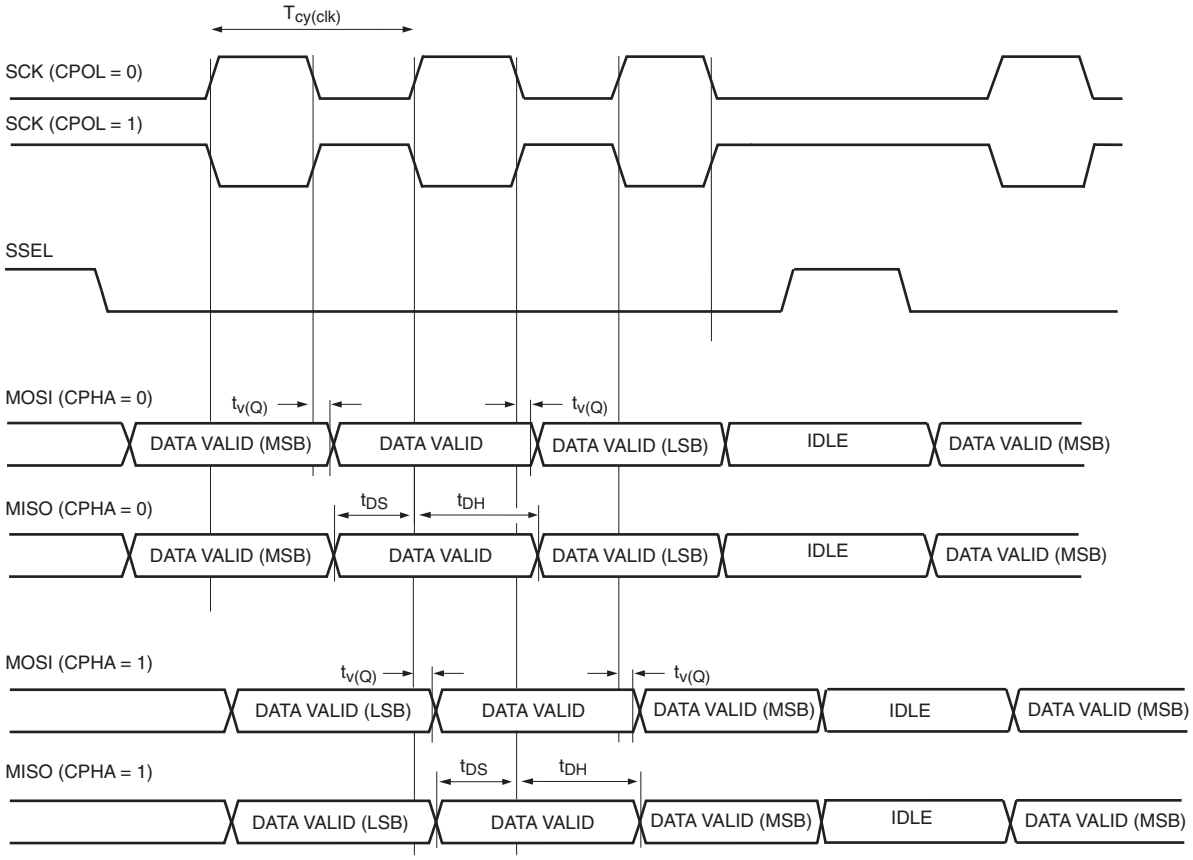


Figure 28. SPI master timing

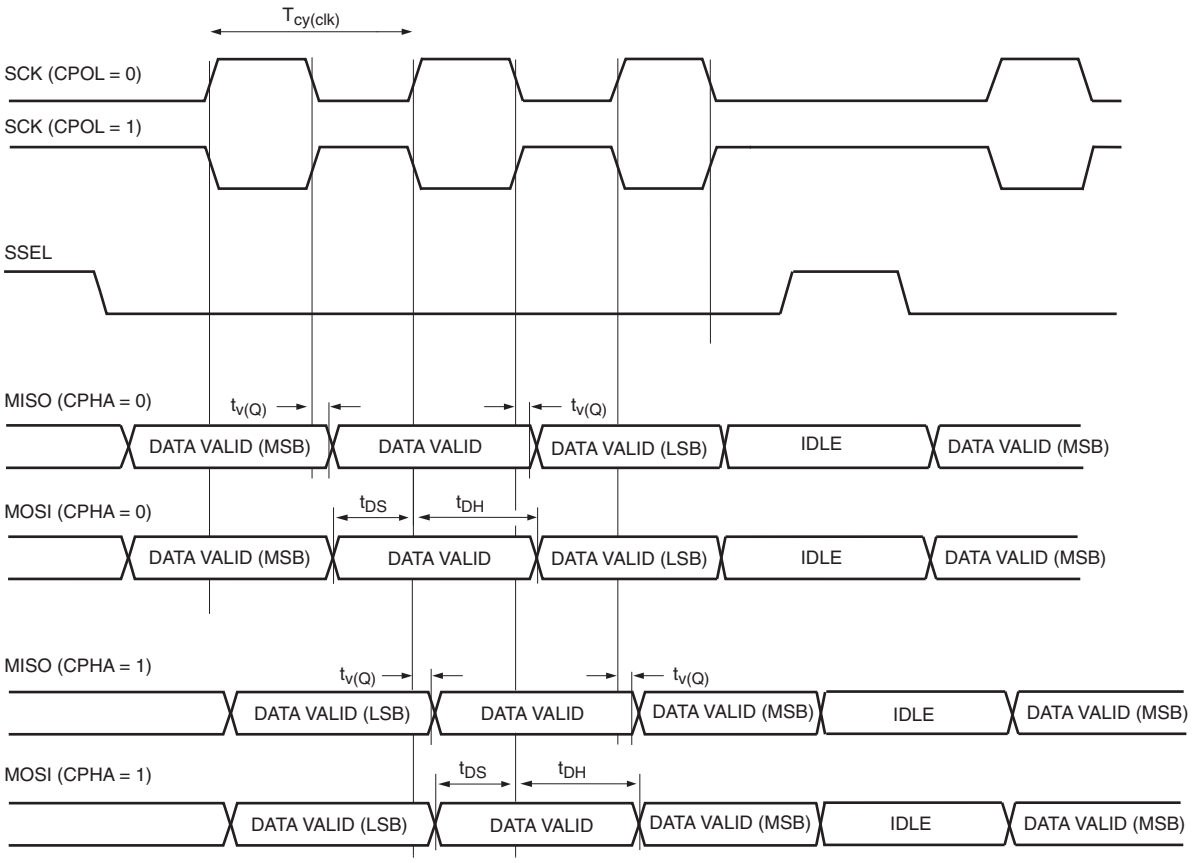


Figure 29. SPI slave timing

7.5 High-Speed SPI interface (Flexcomm interfaces 14 and 16)

The actual SPI bit rate depends on the delays introduced by the external trace, the external device, system clock (HCLK), and capacitive loading.

Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI master mode (transmit/receive) is 50 Mbit/s.

Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI slave mode (receive) is 50 Mbit/s and for SPI slave mode (transmit) is 35 Mbit/s.

T_{amb} = -20 °C to 70 °C; 1.71 V ≤ V_{DD}≤ 1.89 V; C_L = 10 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = standard mode for all pins;. Parameters sampled at the 50 % level of the rising or falling edge.

Table 43. High-Speed SPI interfaces[1]

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
SPI master							
t_{DS}	data set-up time	-		4.0	-	-	ns
t_{DH}	data hold time	-		0	-	-	ns
$t_{v(Q)}$	data output valid time	-		0	-	6.0	ns
SPI slave							
t_{DS}	data set-up time	-		3.0	-	-	ns
t_{DH}	data hold time	-		0	-	-	ns
$t_{v(Q)}$	data output valid time	-		0	-	10.0	ns

1. Based on simulation; not tested in production

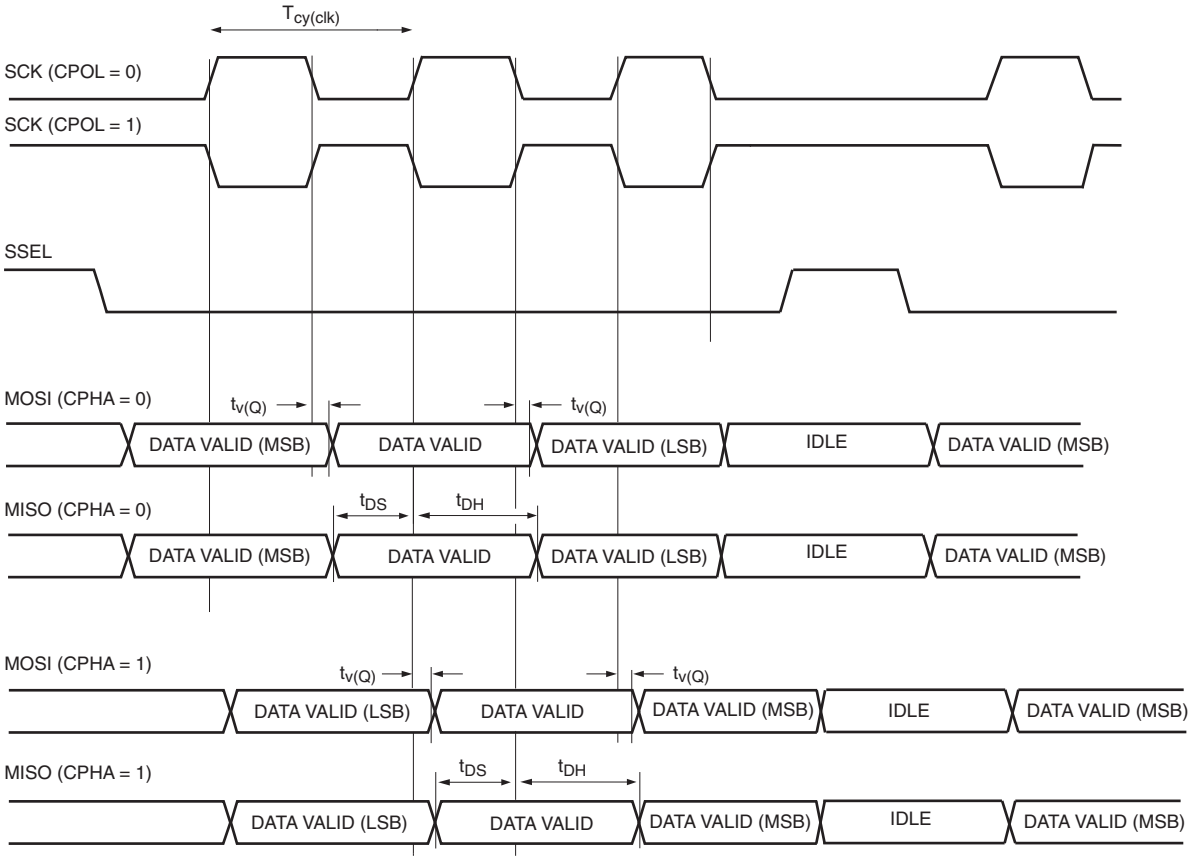


Figure 30. SPI master timing

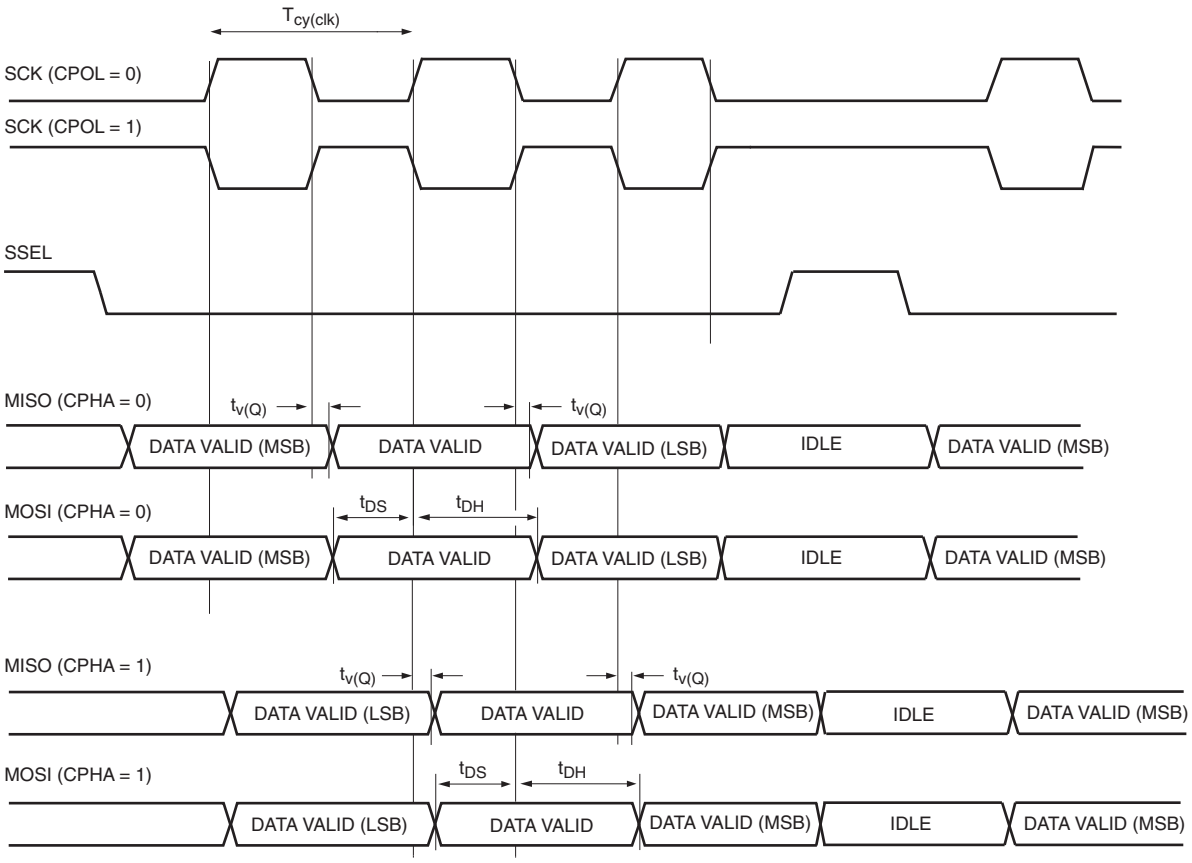


Figure 31. SPI slave timing

7.6 SD/MMC and SDIO

T_{amb} = -20 °C to +70 °C, V_{DD} = 1.71 V to 1.89 V; VDDCORE = 1.13 V; CL = 10 pF. DLL_CTRL = 0x200, Full Drive Mode on all pins, Input slew = 1 ns, SLEW setting = standard mode for all pins;. Parameters sampled at the 50 % level of the rising or falling edge. Based on simulation, not tested in production.

Table 44. SD/MMC and SDIO characteristics (Default Speed (DS), High Speed (HS) SDR-12 and SDR-25)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode. DS/ SDR-12 (12.5 MB/s)	-	-	12.5	MHz
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode, HS/ SDR-25 (25 MB/s)	-	-	25	MHz

Table continues on the next page...

Table 44. SD/MMC and SDIO characteristics (Default Speed (DS), High Speed (HS) SDR-12 and SDR-25) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{su(D)}$	data input set-up time	on pins SD_DATn as inputs	7.5	-	-	ns
		on pins SD_CMD as inputs	7.5	-	-	ns
$t_{h(D)}$	data input hold time	on pins SD_DATn as inputs	1.0	-	-	ns
		on pins SD_CMD as inputs	1.0	-	-	ns
$t_{v(Q)}$	data output valid time	on pins SD_DATn as outputs	-	-	7.5	ns
		on pins SD_CMD as outputs	-	-	7.5	ns

T_{amb} = -20 °C to +70 °C, V_{DD} = 1.71 V to 1.89 V; VDDCORE = 1.13 V; CL = 10 pF. DLL_CTRL = 0x200, Full Drive Mode on all pins, Input slew = 1 ns, SLEW setting = standard mode for all pins;. Parameters sampled at the 50 % level of the rising or falling edge. Based on simulation, not tested in production.

Table 45. SD/MMC and SDIO characteristics ((SDR-50, SDR-104, HS-200 (MMC))

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode, SDR-50 (50 MB/s)	-	-	100	MHz
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode, SDR-104 (104 MB/s)	-	-	208	MHz
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode, HS-200 (MMC) (200 MB/s)	-	-	200	MHz
$t_{su(D)}$	data input set-up time	on pins SD_DATn as inputs	7.5	-	-	ns
		on pins SD_CMD as inputs	7.5	-	-	ns

Table continues on the next page...

Table 45. SD/MMC and SDIO characteristics ((SDR-50, SDR-104, HS-200 (MMC)) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{h(D)}$	data input hold time	on pins SD_DATn as inputs	0	-	-	ns
		on pins SD_CMD as inputs	0	-	-	ns
$t_{v(Q)}$	data output valid time	on pins SD_DATn as outputs	0	-	7.5	ns
		on pins SD_CMD as outputs	0	-	7.5	ns

T_{amb} = -20 °C to +70 °C, V_{DD} = 1.71 V to 1.89 V; VDDCORE = 1.13 V; CL = 10 pF. DLL_CTRL = 0x200, Full Drive Mode on all pins, Input slew = 1 ns, SLEW setting = standard mode for all pins;. Parameters sampled at the 50 % level of the rising or falling edge. Based on simulation, not tested in production. HS-400 supported on SD port 0 only.

Table 46. SD/MMC and SDIO characteristics ((DDR-50, HS DDR (MMC))

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode, DDR-50 (50 MB/s)	-	-	50	MHz
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode, HS-DDR (104 MB/s)			52	MHz
$t_{su(D)}$	data input set-up time	on pins SD_DATn as inputs	4.8	-	-	ns
		on pins SD_CMD as inputs	4.8	-	-	ns
$t_{h(D)}$	data input hold time	on pins SD_DATn as inputs	0	-	-	ns
		on pins SD_CMD as inputs	0	-	-	ns
$t_{v(Q)}$	data output valid time	on pins SD_DATn as outputs	0	-	5.0	ns
		on pins SD_CMD as outputs	0	-	5.0	ns

T_{amb} = -20 °C to +70 °C, V_{DD} = 1.71 V to 1.89 V; VDDCORE = 1.13 V; CL = 10 pF. DLL_CTRL = 0x200, Full Drive Mode on all pins, Input slew = 1 ns, SLEW setting = standard mode for all pins;. Parameters sampled at the 50 % level of the rising or falling edge. Based on simulation, not tested in production. HS-400 supported on SD port 0 only.

Table 47. SD/MMC and SDIO characteristics (HS-400(MMC))

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode, HS-400 (400 MB/s)	-	-	200	MHz
$t_{su(D)}$	data input set-up time	on pins SD_DATn as inputs	0.5	-	-	ns
		on pins SD_CMD as inputs	0.5	-	-	ns
$t_{h(D)}$	data input hold time	on pins SD_DATn as inputs	0	-	-	ns
		on pins SD_CMD as inputs	0	-	-	ns
$t_{v(Q)}$	data output valid time	on pins SD_DATn as outputs	0	-	1.0	ns
		on pins SD_CMD as outputs	0	-	1.0	ns

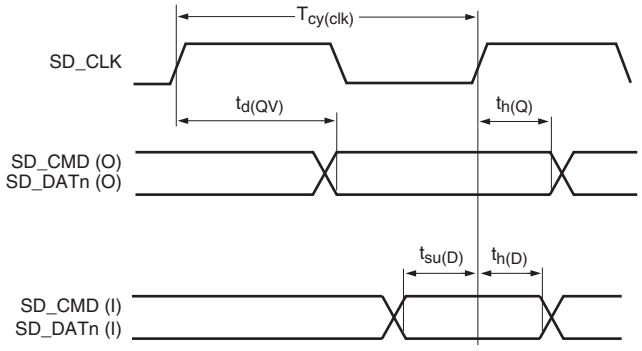


Figure 32. SD/MMC and SDIO timing

7.7 DMIC subsystem

T_{amb} = -20 °C to 70 °C; V_{DD} = 1.71 V to 1.89 V; C_L = 20 pF balanced loading on all pins; Input slew = 1 ns, SLEW set to standard mode for all pins; Bypass bit = 0; Parameters sampled at the 50% level of the rising or falling edge.

Table 48. Dynamic characteristics[1]

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{DS}	data set-up time	-	13	-	-	ns
t_{DH}	data hold time	-	0	-	-	ns

1. Based on simulated values.

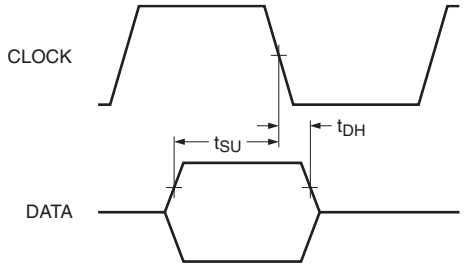


Figure 33. DMIC timing diagram

7.8 USB interface characteristics

This section describes the USB1 port High Speed/Full Speed (HS/FS) transceiver. The USB HS/FS meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 Specification.

7.9 USB DCD electrical specifications

Table 49. USB DCD electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DP_SRC}, V_{DM_SRC}	USB_DP and USB_DM source voltages (up to 250 µA)	0.5	—	0.7	V
V_{LGC}	Threshold voltage for logic high	0.8	—	2.0	V
I_{DP_SRC}	USB_DP source current	7	10	13	µA
I_{DM_SINK}, I_{DP_SINK}	USB_DM and USB_DP sink currents	50	100	150	µA
R_{DM_DWN}	D- pulldown resistance for data pin contact detect	14.25	—	24.8	kΩ
V_{DAT_REF}	Data detect voltage	0.25	0.33	0.4	V

7.10 USB High Speed Transceiver and PHY specifications

This section describes the High Speed USB PHY parameters. The high speed PHY is capable of full speed signaling as well.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 Specification with the amendments below.

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010

USB1_VBUS[2] pin is a detector function which is 5v tolerant and complies with the above specifications without needing any external voltage division components.

7.11 Improved Inter-Integrated Circuit Interface (MIPI-I3C) specifications

Unless otherwise specified, MIPI-I3C specifications are timed to/from the V_{IH} and/or V_{IL} signal points.

2. On WLCSP package, USB ISP mode is not supported. VBUS pin is not available on the WLCSP package. To detect VBUS connection, user can connect a GPIO pin to the USB connector's VBUS. When a rising edge occurs on the GPIO pin, software should set bit 10 (FORCE_VBUS) and bit 16 (DCON) in the DEVCMDSTAT register

Table 50. MIPI-I3C specifications when communicating with legacy I^2C devices[1]

Symbol	Characteristic	400 kHz/Fast mode		1 MHz/ Fast+ mode		Unit
		Min.	Max.	Min.	Max.	
f_{SCL}	SCL Clock Frequency	0	0.4	0	1	MHz
t_{SU_STA}	Set-up time for a repeated START condition	600	—	260	—	ns
t_{HD}; STA	Hold time (repeated) START condition	600	—	260	—	ns
t_{LOW}	LOW period of the SCL clock	1300	—	500	—	ns
t_{HIGH}	HIGH period of the SCL clock	600	—	260	—	ns
t_{SU_DAT}	Data set-up time	100	—	50	—	ns
t_{HD_DAT}	Data hold time for I_2C bus devices	0	—	0	—	ns
t_f	Fall time of SDA and SCL signals	20*(Vdd/5.5 v)	300	20*(Vdd/5.5 v)	120	ns
t_r	Rise time of SDA and SCL signals	20	300	—	120	ns
t_{SU_STO}	Set-up time for STOP condition	600	—	260	—	ns
t_{BUF}	Bus free time between STOP and START condition	1.3	—	0.5	—	µs
t_{SPIKE}	Pulse width of spikes that must be suppressed by the input filter. Input buffer is enabled in boundary scan mode	0	50	0	50	ns

1. Based on simulation, not tested in production.

Table 51. MIPI-I3C open drain mode specifications[1]

Symbol	Characteristic	Min.	Max.	Unit	Notes
t_{LOW_OD}	LOW period of the SCL clock	200	—	ns	
t_{HIGH}	HIGH period of the SCL clock (Mixed Bus)	—	41	ns	
t_{HIGH}	HIGH period of the SCL clock (Pure Bus)	24	—	ns	
t_{fDA_OD}	Fall time of SDA signal	—	12	ns	
t_{SU_OD}	Data set-up time during open drain mode	3	—	ns	
t_{CAS}	Clock after START (S) Condition • ENTAS0 • ENTAS1 • ENTAS2 • ENTAS3	 38.4 n 38.4 n 38.4 n 38.4 n	 1 µ 100 µ 2 m 50 m	 s s s s	
t_{CBP}	Clock before STOP (P) condition	t_{CAS}(min)/2	—	ns	
$t_{MMOverlap}$	Current master to secondary master overlap time during handoff	$t_{DIG\_OD\_L}$	—	ns	
t_{AVAL}	Bus available condition	1	—	µs	
t_{IDLE}	Bus idle condition	200	—	µs	
t_{MMLock}	1	t_{AVAL}	—	µs	

1. Based on simulation, not tested in production.

Table 52. MIPI-I3C push-pull specifications for SDR and HDR-DDR modes[1]

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
f_{SCL}	SCL Clock Frequency	0.01	12.5	13	MHz	
t_{LOW}	LOW period of the SCL clock	24	—	—	ns	
t_{DIG_L}		32	—	—	ns	
t_{HIGH_MIXED}	HIGH period of the SCL clock for a mixed bus	24	—	—	ns	
$t_{DIG\_H\_MIXED}$		32	—	45	ns	2
t_{HIGH}	HIGH period of the SCL clock	24	—	—	ns	
t_{DIG_H}		32	—	—	ns	3
t_{SCO}	Clock in to data out for a slave	—	—	12	ns	
t_{CR}	SCL clock rise time	—	—	150e06 * 1 / fSCL (capped at 60)	ns	
t_{CF}	SCL clock fall time	—	—	150e06 * 1 / fSCL (capped at 60)	ns	
t_{HD_PP}	SDA signal data hold • Master mode • Slave mode	tCR+3 and tCF+3 0	— —	— —	ns	
t_{SU_PP}	SDA signal setup	3	—	—	ns	
t_{CASr}	Clock after repeated START (Sr)	t_{CAS} (min)/2	—	—	ns	
t_{CBSr}	Clock before repeated START (Sr)	t_{CAS} (min)/2	—	—	ns	
C_b	Capacitive load per bus line	—	—	50	pF	

1. Based on simulation, not tested in production.
2. When communicating with an I3C Device on a mixed Bus, the $t_{DIG\_H\_MIXED}$ period must be constrained in order to make sure that I^2C devices do not interpret I3C signaling as valid I^2C signaling.
3. When communication with an I3C Device on a mixed Bus, the t_{DIG_H} period must be constrained in order to make sure that I2C devices do not interpret I3C signaling as valid I2C signaling.

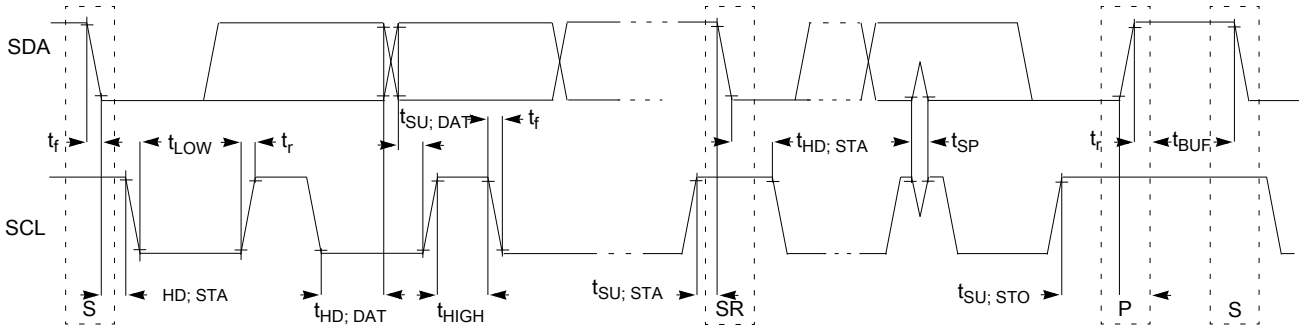


Figure 34. Timing definition for devices on the I^2C bus

8 Timer modules

8.1 SCTimer/PWM output timing

T_{amb} = -20 °C to 70 °C; 1.71 V ≤ V_{DD}≤ 1.89 V C_L = 20 pF. Simulated skew (over process, voltage, and temperature) of any two SCT fixed-pin output signals; sampled at the 50% level of the rising or falling edge; values guaranteed by design.

Table 53. SCTimer/PWM output dynamic characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{sk(o)}$	output skew time	-	0	-	2.8	ns

9 Architectural overview

The Arm Cortex-M33 includes two AHB-Lite buses: the code bus and the system bus.

The i.MX RT500 uses a multi-layer AHB matrix to connect the Arm Cortex-M33 buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals that are on different slave ports of the matrix to be accessed simultaneously by different bus masters.

9.1 Detailed block diagram

The following figure shows the detailed block diagram for i. MX RT500

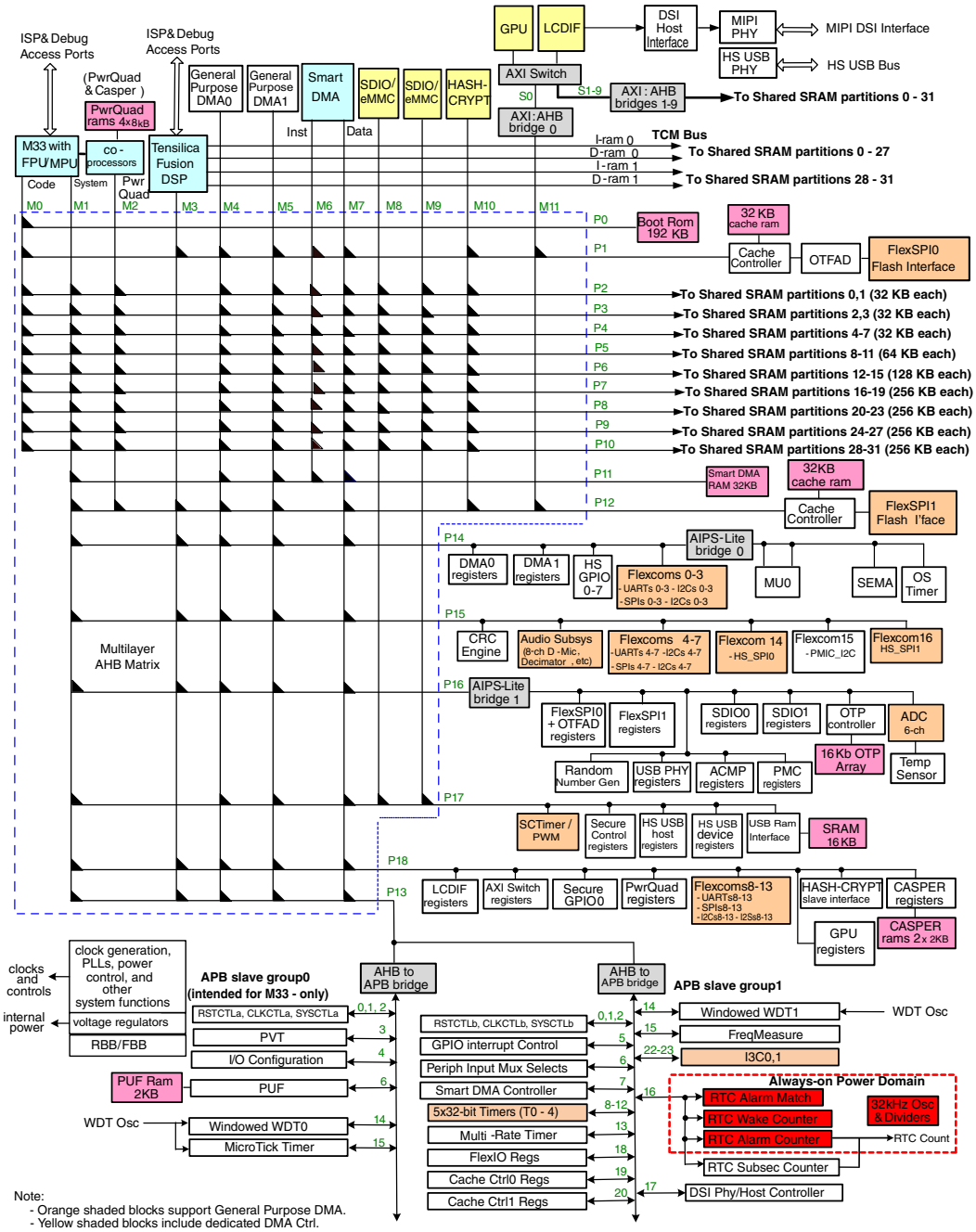


Figure 35. i.MX RT500 detailed block diagram

9.2 Shared system SRAM

The entire system TCM SRAM space (accessed in single cycle) of up to 5 MB is divided into up to 32 separate partitions, which are accessible to both CPUs, both DMA engines, and all other AHB bus masters. The Fusion CPU TCMI (Instruction) &

TCMD (Data) interfaces and the Graphics (GPU/LCD) subsystem each access the RAM via separate, dedicated 64-bit interfaces. All other masters, including the Cortex-M33 processor and the DMA engines, access RAM via the main 32-bit AHB bus. All of these accesses are single-cycle with the exception of the GPU/LCD. Hardware interface modules arbitrate access to each RAM partition between the main AHB bus, the graphics AHB bus and the Fusion Tightly-Coupled-Memory buses.

Under software control, each of the 32 individual SRAM partitions can be used exclusively as code or as data, dedicated either CPU, or shared among the various masters. Each partition can be independently placed in a low-power retention mode or powered off entirely.

9.3 RT500 modules list

The i.MX RT500 contains a variety of digital and analog modules. The following table describes briefly about these modules.

Table 54. i.MX RT500 modules list

Block Name	Block Mnemonic	Subsystem	Brief description
Arm core modules			
ARM Cortex M33 processor	MCU	Core module	The Arm Cortex-M33 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption. The Arm Cortex-M33 offers many new features, including a Thumb-2 instruction set, low interrupt latency, hardware multiply and divide, interruptable/continuable multiple load and store instructions, automatic state save and restore for interrupts, tightly integrated interrupt controller with wake-up interrupt controller, and multiple core buses capable of simultaneous accesses. M33 includes ARM's TrustZone M for enhanced security as well as a co-processor interface. This interface is used on this device to provide hardware acceleration for DSP functions (Powerquad co-processor) and Security/ cryptography operations (CASPER co-processor). A 3-stage pipeline is employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its

Table continues on the next page...

Table 54. i.MX RT500 modules list (continued)

Block Name	Block Mnemonic	Subsystem	Brief description
			successor is being decoded, and a third instruction is being fetched from memory.
Arm Cortex-M33 integrated Floating Point Unit (FPU)	FPU	Core modules	The FPU fully supports single-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations. It also provides conversions between fixed-point and floating-point data formats, and floating-point constant instructions. The FPU provides floating-point computation functionality that is compliant with the ANSI/IEEE Std 754-2008, IEEE Standard for Binary Floating-Point Arithmetic, referred to as the IEEE 754 standard.
Cadence Xtensa Fusion F1 Digital Signal Processor	DSP	Core modules	The Cadence Xtensa Fusion F1 Audio DSP is a digital signal processor designed for low-energy, high-performance IoT/ wearable applications running at frequencies of up to 275 MHz. It has a single-precision Hardware Floating Point Unit. It also features a Serial Wire Debug module (shared with Cortex-M33 Control Domain CPU).
Memory Protection Unit	MPU	Core module	The Cortex-M33 includes a Memory Protection Unit (MPU) which can be used to improve the reliability of an embedded system by protecting critical data within the user application. The MPU allows separating processing tasks by disallowing access to each other's data, disabling access to memory regions, allowing memory regions to be defined as read-only and detecting unexpected memory accesses that could potentially break the system. The MPU separates the memory into distinct regions and implements protection by preventing disallowed accesses. The MPU supports up to eight regions each of which can be divided into eight subregions. Accesses to memory locations that are not defined in the MPU regions, or not permitted by the region setting, will cause the Memory Management Fault exception to take place.
Nested Vectored Interrupt Controller (NVIC) for Cortex-M33	NVIC	Core modules	The NVIC is an integral part of the Cortex-M33. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

Table continues on the next page...

Table 54. i.MX RT500 modules list (continued)

Block Name	Block Mnemonic	Subsystem	Brief description
System Tick timer (SysTick)	SysTick	Core modules	The Arm Cortex-M33 includes a system tick timer (SysTick) that is intended to generate a dedicated SYSTICK exception. The clock source for the SysTick can be the FRO or the Cortex-M33 core clock.
Memories			
On-Chip static RAM	SRAM	Memories	The i.MX RT500 supports up to 5 MB SRAM with separate bus master access for higher throughput and individual power control for low-power operation.
On-chip ROM	ROM	Memories	The 192 KB on-chip ROM contains the boot loader and the following Application Programming Interfaces (API): • In-Application Programming (IAP) and In-System Programming (ISP). • ROM-based USB drivers (HID, CDC, MSC). Supports flash updates via USB. • Supports booting from valid Octal/ Quad SPI, eMMC, USB, USART, SPI, and I2C. • Legacy, Single, and Dual image boot. • OTP API for programming OTP memory. • Random Number Generator (RNG) API.
One-Time Programmable memory	OTP	Memories	The i.MX RT500 contains up to 16 kbits one-time-programmable memory used for part configuration, key storage (as an alternative to PUF) and other uses.
Clock sources			
192 MHz Free Running Oscillator (FRO)	FRO	System control	The 192 MHz FRO oscillator provides a high-frequency clock source that can be used without the need for a high-power PLL for many applications. This oscillator is factory trimmed to ±1% accuracy but can optionally be tuned to ±0.1% accuracy using an accurate, known reference clock such as the crystal oscillator. The 192 MHz FRO, or a divided version of it, may be used as the main system clock and for many other purposes.
1 MHz Low Power Oscillator	LPO	System Control	The 1 MHz oscillator provides an ultra low-power, low-frequency clock source that can be used to clock a variety of functions including the Watchdog Timer (WWDT) and the OS/EVENT Timer. It can

Table continues on the next page...

Table 54. i.MX RT500 modules list (continued)

Block Name	Block Mnemonic	Subsystem	Brief description
			also be used as the main system clock for low-power operation. On Reset, the device boots using this 1 MHz oscillator. The 1 MHz Low Power oscillator is accurate to ±10% over temperature.
Crystal Oscillator	-	System Control	The main crystal oscillator on the i.MX RT500 can be used with crystal frequencies from 4 MHz to 26 MHz. The crystal oscillator may be used to drive a PLL to achieve higher clock rates.
32 KHz Crystal Oscillator	-	System Control	The 32KHz oscillator resides in the "always-on" domain and is used to drive the Real Time Clock. It is also available for use for a variety of other purposes including low-power UART operation or as the main system clock for very low frequency operation
System Control (PLLs)			
System PLL (PLL0)	PLL0	System Control	The system PLL accepts an input clock frequency in the range of 4 MHz to 26 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). Generates four independent outputs (PFD0-3).
Audio PLL (PLL1)	PLL1	System Control	The audio PLL accepts an input clock frequency in the range of 4 MHz to 26 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The PLL can be enabled or disabled by software.
I/O Muxing			
General Purpose I/O (GPIO)	GPIO	Pin Muxing	The i.MX RT500 provides up to six GPIO ports with a total of up to 136 GPIO pins. Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The current level of a port pin can be read back no matter what peripheral is selected for that pin. It can optionally contribute to one of two GPIO group interrupts, with selection of polarity, level or edge detection.
Pin Interrupt and Pattern Match (PINT)	-	I/O Mux	The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC. The pattern match engine can

Table continues on the next page...

Table 54. i.MX RT500 modules list (continued)

Block Name	Block Mnemonic	Subsystem	Brief description
			optionally be used in conjunction with software to create complex state machines based on pin inputs. Any digital pin, independent of the function selected through the switch matrix can be configured through the SYSCON block as an input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are located on the I/O+ bus for fast single-cycle access.
Communication peripherals			
High-speed USB Host/ Device interface (USB1)	USB1	Communication interfaces	The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The device controller enables 480 Mbit/s data exchange with a USB host controller. It consists of a register interface, serial interface engine, endpoint buffer memory. The bus supports hot plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.
Flex SPI Controller (FlexSPI)	FlexSPI	Communication interfaces	Two FlexSPI Interface modules, supporting Octal and Quad SPI memory devices are provided. The first FlexSPI instance is primarily intended for code execution from off-chip SPI flash memory. The second instance is primarily intended to access data from RAMs like HyperRAM or pSRAM (particularly for graphics). The second instance is accessible by the DSP processor as well as the M33. Target will be for both interfaces to support up to 200 MHz DDR/SDR The FlexSPI interfaces support HyperFlash, HyperRAM and Xccela memory types, among others. The first FlexSPI interface (FlexSPI0) supports execute-in-place and on-the-fly decryption using the latest OTFAD module. It also provides a mechanism to shift a designated range of addresses to a different region of off-chip memory to support dual-image boot. Both FlexSPI Interfaces include a 32 KB cache with an CACHE64 AHB-cache controller. Additional logic is provided at the CACHE64 interface to enable different

Table continues on the next page...

Table 54. i.MX RT500 modules list (continued)

Block Name	Block Mnemonic	Subsystem	Brief description
			caching policies for different address regions. These policies include: • Write-back • Write-through • Non-cached .
SD/eMMC interfaces	uSDHC	Communication interfaces	Two uSDHC SDIO/MMC card interfaces are provided. One instance of this interface (SDIO0) supports the eMMC 5.0 standard including HS400 DDR mode. The other instance supports 100 MHz SDR, 50 MHz DDR.
Flexcomm Interface	FlexComm	Communication interfaces	Following are the features of FlexComm: • USART with asynchronous operation or synchronous master or slave operation. • SPI master or slave, with up to 4 slave selects. • I2C, including separate master, slave, and monitor functions. • Two I2S functions using Flexcomm Interface 6 and Flexcomm Interface 7. • Data for USART, SPI, and I2S traffic uses the Flexcomm Interface FIFO. The I2C function does not use the FIFO.
I3C interface	I3C	Communication interface	Two I3C master/slave interfaces are provided, both of which support DDR.
		Counter/Timer modules	
General-purpose 32-bit timers/external event counter	-	Counter/Timers	The i.MX RT500 includes five general-purpose 32-bit timer/counters. The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.
SCTimer/PWM	SCT/PWM	Counters/Timers	The SCTimer/PWM allows a wide variety of timing, counting, output modulation, and input capture operations. The inputs and outputs of the SCTimer/PWM are shared with the capture and match inputs/outputs of the 32-bit general-purpose counter/timers. The SCTimer/PWM can

Table continues on the next page...

Table 54. i.MX RT500 modules list (continued)

Block Name	Block Mnemonic	Subsystem	Brief description
			be configured as two 16-bit counters or a unified 32-bit counter. In the two-counter case, in addition to the counter value the following operational elements are independent for each half: • State variable • Limit, halt, stop, and start conditions. • Values of Match/Capture registers, plus reload or capture control values. In the two-counter case, the following operational elements are global to the SCTimer/PWM, but the last three can use match conditions from either counter: • Clock selection • Inputs • Events • Outputs • Interrupts
Windowed Watchdog Timer (WWDT)	WWDT	Timers	The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window. A separate Watchdog Timer is provided for each of the two CPUs.
Real Time Clock Timer	RTC Timer	Timers	The RTC timer is a 32-bit timer which counts down from a preset value to zero. At zero, the preset value is reloaded and the counter continues. The RTC timer uses the 32.768 kHz clock input to create a 1 Hz or 1 kHz clock.
Multi-Rate Timer	MRT	Timers	The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.
OS/Event Timer	-	Timers	An OS/EVENT Timer module provides a common timebase between the two CPUs for event synchronization and timestamping. The OS/EVENT Timer is comprised of a shared, free-running counter readable by each CPU and individual match and capture registers for each CPU. The shared and local counters in this module are implemented using Gray code. This will enable them to be read asynchronously by the processing domains. The main counter in the OS/

Table continues on the next page...

Table 54. i.MX RT500 modules list (continued)

Block Name	Block Mnemonic	Subsystem	Brief description
			EVENT Timer module begins counting immediately following power-up and continues counting through any subsequent system resets (except those caused by a new POR).
Micro-Tick Timer	MTR	Timers	A 32-bit MicroTick timer that runs from the 1 MHz low-power oscillator. This timer can wake up the device from reduced power modes up to deep-sleep, with extremely low power consumption. The MicroTick timer has an added timestamp feature in the form of 4 capture registers.
Graphics Peripherals			
2D Graphics Processing Unit (GPU)	GPU2D	Graphics	A 2D graphics engine is provided. The GPU is used to generate graphics data for display by the LCD Display Controller.
MIPI DSI Controller with on-chip PHY	MIPI-DSI	Graphics	LCD Display Controller, with on-chip MIPI DSI Phy provides transfer rates up to 895.1 Mbps to support 1024x480 displays with 24-bit color at 60 frames per second. A parallel DBI interface is also provided (alternative to the serial PHY).
Flexio	FlexIO	Graphics/Multimedia	The Flexio module under "Others" category can be used to interface to an LCD with a parallel interface.
Other Digital Peripherals			
DMA Controller	DMA	Other	The DMA controller allows peripheral-to memory, memory-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional DMA transfers for a single source and destination. Two identical DMA controllers are provided on i.MX RT500. The user may elect to dedicate one of these to the Cortex M-33 CPU and the other for use by the DSP CPU and/or one may be used as a secure DMA the other non-secure.
DMIC Subsystem	DMIC	Other	DMIC subsystem includes: • Pulse-Density Modulation (PDM) data input for left and/or right channels on 1 or 2 buses. • Flexible decimation. • 16 entry FIFO for each channel. • DC blocking or unaltered DC bias can be selected. • Data can be transferred using DMA from deep-sleep mode without waking up the CPU, then

Table continues on the next page...

Table 54. i.MX RT500 modules list (continued)

Block Name	Block Mnemonic	Subsystem	Brief description
			automatically returning to deep-sleep mode. • Data can be streamed directly to I2S on Flexcomm Interface 7.
Smart DMA Engine	Smart DMA Controller	Other	Smart DMA Controller with dedicated 32 KB code RAM
Flexible Input/Output	FlexIO	Others	The Flexible Input/Output (FlexIO) module is capable of supporting a wide range of protocols including, but not limited to: UART, I2C, SPI, I2S, camera interface, display interface, PWM waveform generation, and so on
Cyclic Redundancy Check(CRC) engine	CRC	Other	The Cyclic Redundancy Check (CRC) generator with programmable polynomial settings supports several CRC standards commonly used. To save system power and bus bandwidth, the CRC engine supports DMA transfers.
Analog Peripherals			
12-bit Analog to Digital Converter	ADC	Analog	The ADC supports a resolution of 12-bit and fast conversion rates of up to 1 Msamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources. Possible trigger sources are the SCTimer/PWM, external pins, and the Arm TXEV interrupt.
Temperature Sensor	-	Analog	The temperature sensor transducer uses an intrinsic pn-junction diode reference and outputs a CTAT voltage (Complement To Absolute Temperature). The output voltage varies inversely with device temperature with an absolute accuracy of better than ±5 °C over the full temperature range (-20 °C to +70 °C). The temperature sensor is only approximately linear with a slight curvature. The output voltage is measured over different ranges of temperatures and fit with linear-least-square lines. After power-up, the temperature sensor output must be allowed to settle to its stable value before it can be used as an accurate ADC input. For an accurate measurement of the temperature sensor by the ADC, the ADC must be configured in single-channel burst mode. The last value of a nine-conversion (or more) burst provides an accurate result.
Analog Comparator	CMP	Analog	The Comparator (CMP) module provides a circuit for comparing two analog input

Table continues on the next page...

Table 54. i.MX RT500 modules list (continued)

Block Name	Block Mnemonic	Subsystem	Brief description
			voltages. The comparator circuit is designed to operate across the full range of the supply voltage (rail to rail operation).
Security			
Security Subsystem	-	Security	Comprises of: • Trust Zone M • AES256 Decryption Engine. • SHA-1, SHA-2 HASH Engine. • Physical Unclonable Function (PUF) Key Generation • CASPAR security Cortex-M33 co-processor • OTP memory • Random number generator (RNG) • On-the-Fly Decryption on FlexSPI interface .
On-The-Fly AES Decryption	OTFAD	Security	The On-The-Fly AES Decryption (OTFAD) module provides an advanced hardware implementation that minimizes any incremental cycles of latency introduced by the decryption in the overall external memory access time. The OTFAD engine also includes complete hardware support for a standard AES key unwrap mechanism to decrypt a key BLOB data instruction containing the parameters needed for up to 4 unique AES contexts.
True Random Number Generator	TRNG	Security	The True Random Number Generator (TRNG) module is used to generate high quality, cryptographically secure, random data. The TRNG module is capable of generating its own entropy using an integrated ring oscillator.

10 Application information

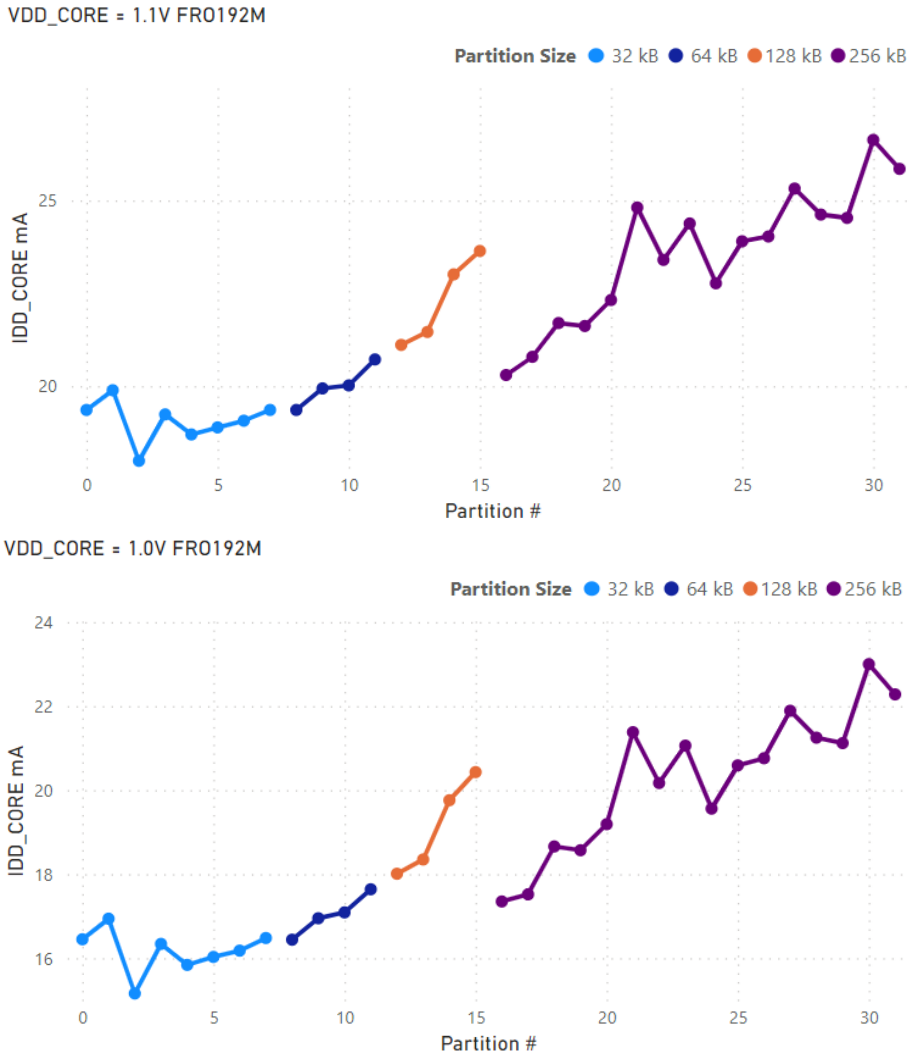
10.1 Current consumption vs. memory partitions

The following figure shows the current consumption vs memory partitions:

M33 active, running enhanced-while(1) code in different partitions.

Typical silicon, VDDCore=1.1V, Temperature=25℃, FBB, HCLK=192MHz (FRO).

All memories array/periphery ON (PDRUNCFG2/3) and only one partition clocked (AHB_SRAM_ACCESS_DISABLE register).



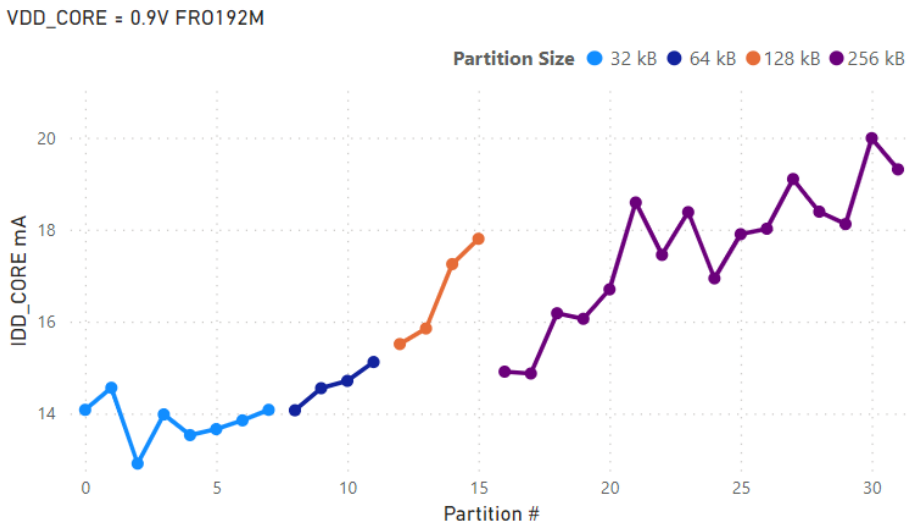


Figure 36. Current consumption vs. memory partitions

10.2 Standard I/O pin configuration

Each port pin (PIOm_n), PMIC_I2C_SCL and PMIC_I2C_SDA has one IOPCTL register assigned to control the characteristics of the pin. This chip has two types of GPIO pads: Fail Safe pads, which can handle input voltages up to 3.6 V when the VDDIO supply is 0V (not powered); and High Speed pads, which are used on higher speed ports and cannot handle input voltages greater than VDDIO at any time.

The IO pins associated with power domains VDDIO_0/1/2/4 can only support input voltages up to 1.8V when powered. IO pins in the VDDIO_3 power domain can support input voltages up to 3.6V (when VDDIO_3 is 3.6V).

The IOPCTL registers control the following GPIO pad properties: pull-up/-down resistors, input buffer enable, output slew rate, output drive strength, analog multiplexor enable, pseudo open-drain output enable, and input invert enable.

For the High Speed pads, the IOPCTL registers don't control the following GPIO pad properties: output slew rate and analog mulitplexer enable.

	IOPCTL Register Functions							
Pad Type	**IIENA**	**ODENA**	**AMENA**	**FULLDRIVE**	**SLEWRATE**	**IBENA**	**PUPDSEL**	**PUPDENA**
Fail Safe	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
High Speed	Yes	Yes	No	Yes	No	Yes	Yes	Yes

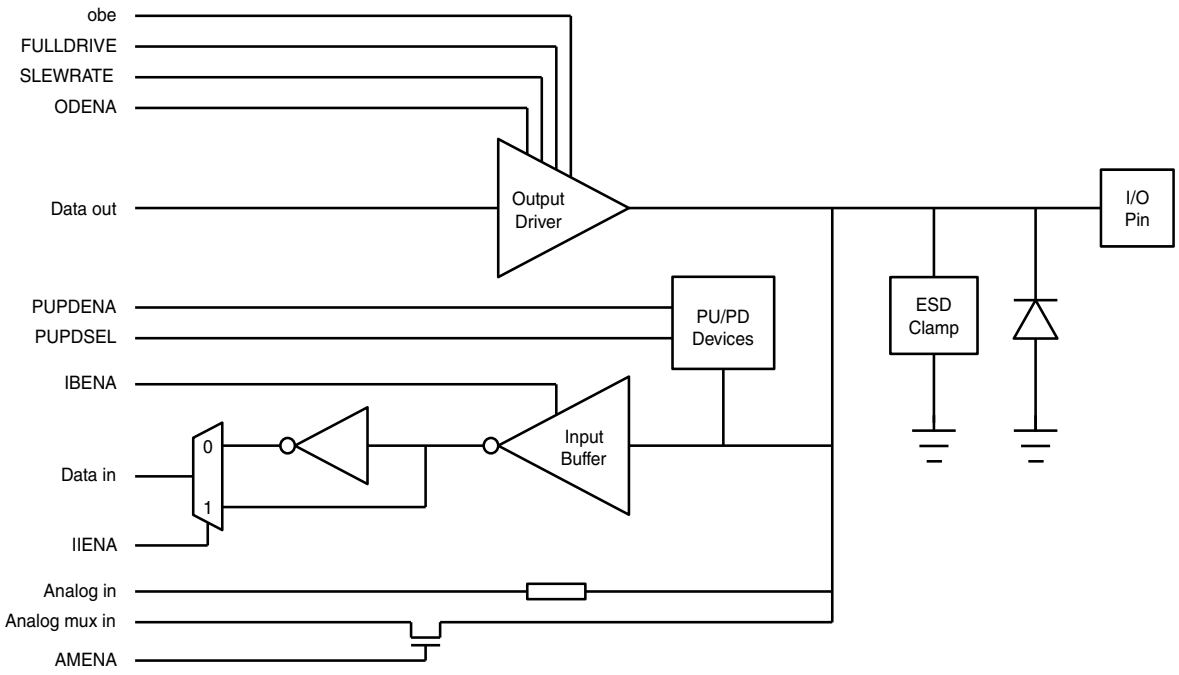


Figure 37. Simplified Fail Safe pin configuration

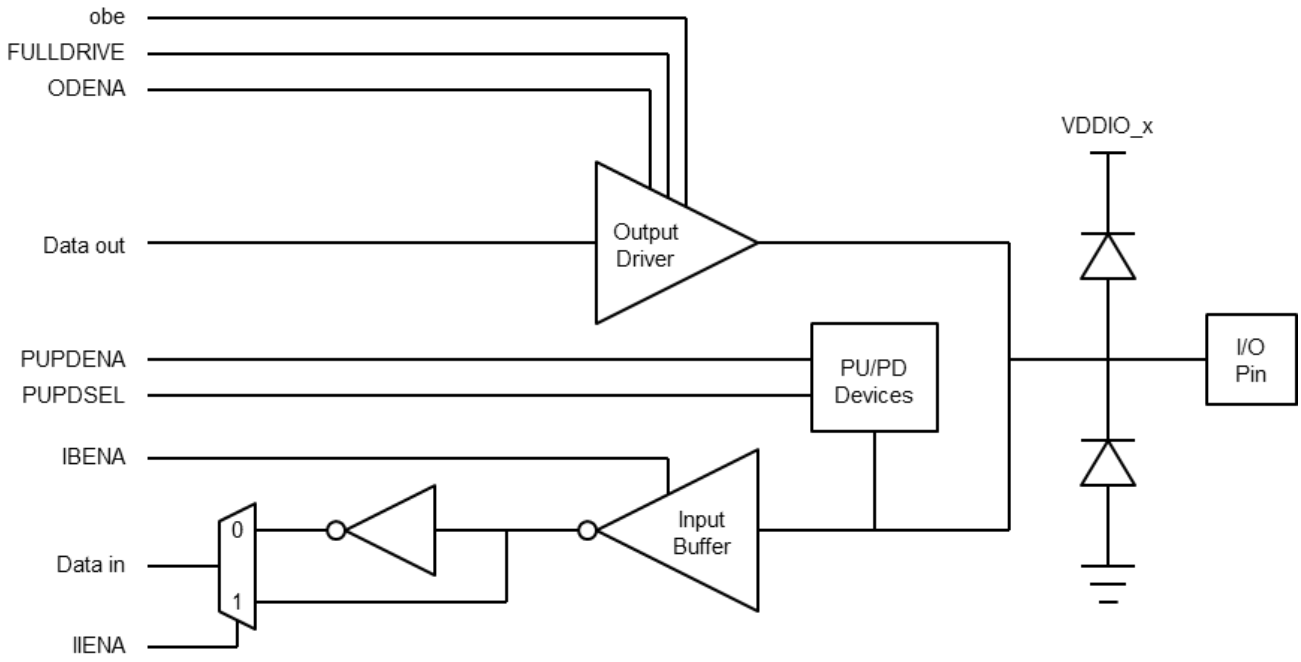


Figure 38. Simplified High Speed pin configuration

10.3 RTC oscillator

In the RTC oscillator circuit, only the crystal (XTAL) needs to be connected externally on RTCXIN and RTCXOUT. Load capacitances C_{X1} and C_{X2} can be applied externally or internally using the RTC_OSC_loadcap settings in the RTC_CTRL register. See the following figure and parameters in RTC oscillator.

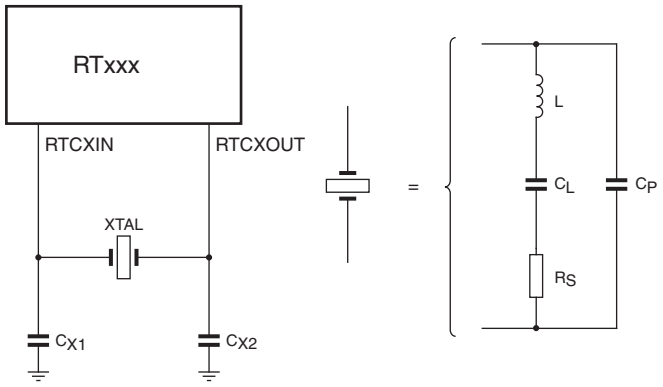


Figure 39. RTC oscillator components

For best frequency accuracy, the load capacitors need to be tuned in the application using the following guidance. After selecting the crystal, the approximate load capacitor C_{X1} and C_{X2} values can be generally determined by the following expression:

$C_{X1} = C_{X2} = 2C_L - C_{Pad} - 2C_{STRAY}$

Where:

C_L - Crystal load capacitance (from crystal specification)

C_{Pad} - Pad capacitance of the RTCXIN and RTCXOUT pins (~3 pF, for each pad).

C_{STRAY} – stray capacitance between RTCXIN and RTCXOUT pins.

For example:

$C_L = 9$ pF

$C_{X1} = C_{X2} = 2C_L - C_{Pad} - 2C_{STRAY}$

$C_{X1} = C_{X2} = 2*9 - 3 - 0 = 15$ pF

Although C_{STRAY} can be ignored in first-pass calculations, the actual board layout and placement of external components influence the optimal values of external load capacitors. Therefore, it is recommended to fine tune the values of load capacitors on

actual hardware board to get the accurate clock frequency. For fine tuning, output the RTC Clock to the CLKOUT pin and optimize the values of load capacitors for minimum frequency deviation.

To bypass the RTC crystal oscillator with an external CMOS crystal oscillator, connect the external oscillator to the RTCXIN pin and float RTCXOUT.

10.3.1 RTC Printed Circuit Board (PCB) design guidelines

- Place the crystal (and external load capacitors, if necessary) on the PCB as close as possible to the oscillator pins on the same layer as the chip.
- Keep trace lengths as short as possible.
- The layer beneath the crystal should be a ground plane for load capacitor connection, as well as field control.
- Do not place any signal traces near the crystal traces.

10.4 XTAL oscillator

In the XTAL oscillator circuit, the crystal (XTAL), feedback resistor (high gain mode only), and the load capacitances C_X and C_Y need to be connected externally on XTALIN and XTALOUT. See the figure below and parameters in Crystal oscillator.

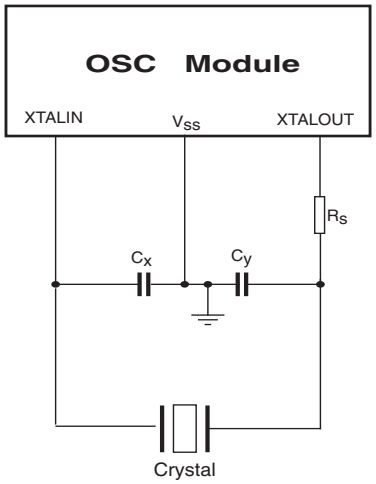


Figure 40. XTAL oscillator connection - Low-Power Mode

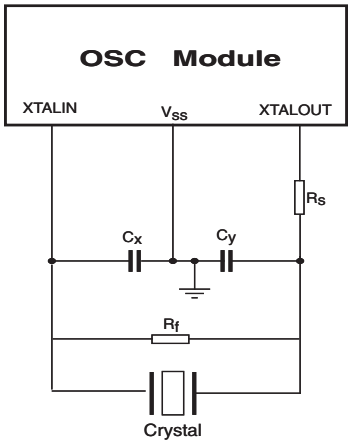


Figure 41. XTAL oscillator connection - High Gain Mode

For best frequency accuracy, the load capacitors need to be tuned in the application using the following guidance. After selecting the crystal, the approximate load capacitor C_X and C_Y values can be generally determined by the following expression:

$C_x = C_y = 2C_L - C_{Pad} - 2C_{STRAY}$

Where:

C_L - Crystal load capacitance

C_{Pad} - Pad capacitance of the XTALIN and XTALOUT pins (~3 pF, for each pad).

C_{STRAY} − stray capacitance between XTALIN and XTALOUT pins.

For example:

$C_L = 9$ pF

$C_x = C_y = 2C_L - C_{Pad} - 2C_{STRAY}$

$C_x = C_y = 2*9 - 3 - 0 = 15$ pF

Although C_{STRAY} can be ignored in first-pass calculations, the actual board layout and placement of external components influence the optimal values of external load capacitors. Therefore, it is recommended to fine tune the values of external load capacitors on actual hardware board to get the accurate clock frequency. For fine tuning, measure the clock on the CLKOUT pin and optimize the values of external load capacitors for minimum frequency deviation.

To bypass the crystal oscillator with an external CMOS crystal oscillator, connect the external oscillator to the XTALIN pin and float XTALOUT. Set the BYPASS_ENABLE bit in CLKCTL0_SYSOSCCTL0.

For oscillator high gain mode, a larger voltage swing is used at the crystal pin. This gives a higher noise immunity within the oscillator and less edge-to-edge jitter of the internal clock. If high gain mode is not required, power used by the crystal oscillator can be reduced by using low power mode.

NOTE

High gain mode requires a 1 megaohm feedback resistor (RF) to be inserted.

10.4.1 XTAL Printed Circuit Board (PCB) design guidelines

- Connect the crystal, feedback resistor (high gain mode only), and load capacitors on the PCB as close as possible to the oscillator pins on the same layer as the chip.
- Keep trace lengths as short as possible.
- The layer beneath the crystal should be a ground plane for load capacitor connection, as well as field control.
- Do not place any signal traces near the crystal traces.

10.4.2 Temperature compensated crystal oscillator (TCXO)

A clipped sine-wave temperature compensated crystal oscillator can be used as the input clock to the main oscillator. Connect the TCXO output to the XTALIN pin and float the XTALOUT pin. Do not use a series (AC coupling) capacitor between the TCXO output and XTALIN, as the low power oscillator has an internal coupling capacitor. Configure the oscillator to use the low power mode by setting LP_ENABLE in CLKCTL0_SYSOSCCTL0. (Leave BYPASS_ENABLE cleared). See the following figure.

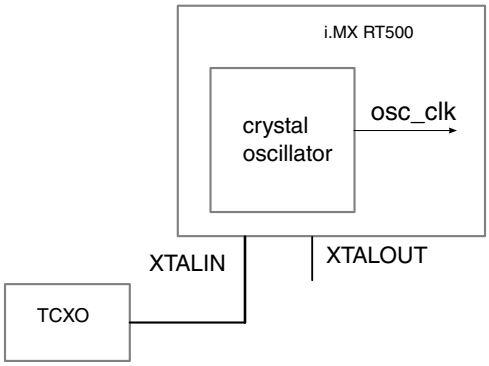


Figure 42. Temperature compensated crystal oscillator

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{Main}	Oscillator frequency range[1]	-	4	-	32	MHz
V_{XTALIN}	XTALIN input voltage	TCXO[2]	0	-	VDD1V8	V
V_{pp_tcxo}	Peak-to-Peak TCXO amplitude	TCXO	0.7[3]	-	VDD1V8	V

1. Operating range of oscillator. Practical range is 5 MHz to 26 MHz, based on PLL requirements.
2. TCXO supply should be same as VDD1V8.
3. TCXO output minimum Vpp should be greater than this value. Do not insert a DC-cut capacitor.

10.5 Suggested USB interface solutions

The USB device can be connected to the USB as self-powered device (see Figure 43) or bus-powered device (see Figure 44).

On the i.MX RT500, the USB_VBUS[3] pin is 5 V tolerant pin regardless of whether USB1_VDD3V3 or VDD pins are present or not.

3. On WLCSP package, USB ISP mode is not supported. VBUS pin is not available on the WLCSP package. To detect VBUS connection, user can connect a GPIO pin to the USB connector's VBUS. When a rising edge occurs on the GPIO pin, software should set bit 10 (FORCE_VBUS) and bit 16 (DCON) in the DEVCMDSTAT register

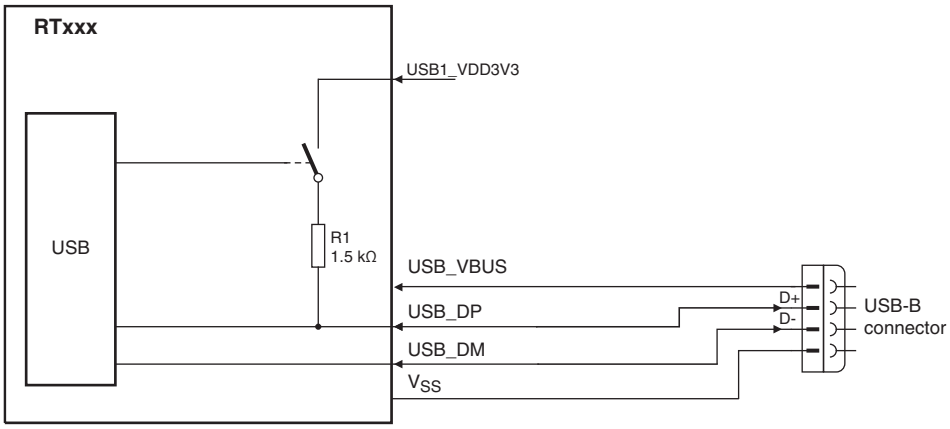


Figure 43. USB interface on a self-powered device where USB_VBUS = 5 V

The internal pull-up (1.5 kΩ) can be enabled by setting the DCON bit in the DEVCMDSTAT register to prevent the USB from timing out when there is a significant delay between power-up and handling USB traffic. External circuitry is not required.

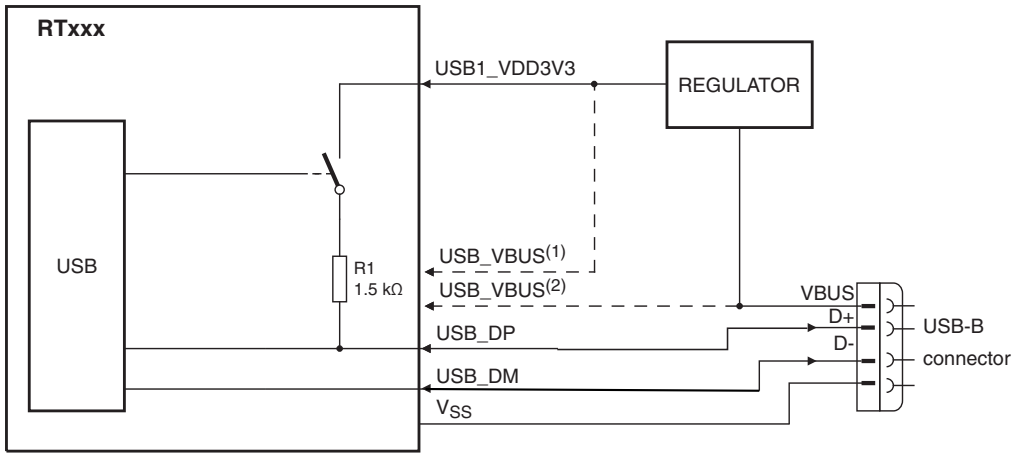


Figure 44. USB interface on a bus-powered device

In the figure above, two options exist for connecting VBUS to the USB_VBUS pin:

1. Connect the regulator output to USB_VBUS. In this case, the USB_VBUS signal is HIGH whenever the part is powered.

2. Connect the VBUS signal directly from the connector to the USB_VBUS pin. In this case, 5 V are applied to the USB_VBUS pin while the regulator is ramping up to to supply USB1_VDD3V3

10.6 Boundary scan method

The RESET pin selects between the JTAG boundary scan (RESET = LOW) and the Arm SWD debug (RESET = HIGH). The Arm SWD debug port is disabled while the RT5xx is in reset. The JTAG boundary scan pins are selected by hardware when the part is in boundary scan mode.

To perform boundary scan testing, follow these steps:

1. Power up the part with the RESET pin pulled LOW externally.
2. Wait for at least 4.4 ms.
3. Perform boundary scan operations.
4. Once the boundary scan operations are completed, assert the TRST pin to enable the SWD debug mode, and release the RESET pin (pull HIGH).

NOTE

The JTAG interface cannot be used for debug purposes.

10.6.1 VDDA_BIAS Power Supply Connection

Since all analog pins are in the 1.8 V VDDIO domains, VDDA_BIAS must be connected to a 1.8 V supply.

11 Abbreviations

Table 55. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
API	Application Programming Interface
DMA	Direct Memory Access
FRO oscillator	Internal Free-Running Oscillator, tuned to the factory specified frequency
GPIO	General Purpose Input/Output

Table continues on the next page...

Table 55. Abbreviations (continued)

Acronym	Description
FRO	Free Running Oscillator
LSB	Least Significant Bit
MCU	MicroController Unit
PDM	Pulse Density Modulation
PLL	Phase-Locked Loop
SPI	Serial Peripheral Interface
TCP/IP	Transmission Control Protocol/Internet Protocol
TTL	Transistor-Transistor Logic
USART	Universal Asynchronous Receiver/Transmitter

12 Pinouts

12.1 Signal multiplexing and pinouts

The table below shows the pin functions available on each pin, and for each package. These functions are selectable using IOPCTL control registers.

Some functions, such as ADC or comparator inputs, are available only on specific pins when digital functions are disabled on those pins. By default, the GPIO functionality, Func 0, is always selected with the exception of PIO2_25 and PIO2_26, which have Func 1 (SWD) selected, at reset. This allows debug to operate through reset.

Most pins have all pull-ups, pull-downs, and inputs turned off at reset. This prevents power loss through pins prior to software configuration. Due to special pin functions, some pins have a different reset configuration: If the Boot ROM OTP is configured to use the ISP Select pins at boot, then these pins PIO1_15, PIO3_28, and PIO3_29 have pull-ups enabled by ROM; otherwise these pull-ups are not enabled at boot. The SWD pins PIO2_25 and PIO2_26 have the input buffers enabled at reset.

The state of pins PIO1_15, PIO3_28, and PIO3_29 at Reset determine the boot source for the part (if configured in the Boot ROM OTP) or if the ISP handler is invoked.

The JTAG functions TRST, TCK, TMS, TDI, and TDO, are selected on pins PIO0_7 to PIO0_11 by hardware when the part is in boundary scan mode.

12.2 i.MXRT500 Pinouts: 249 FOWLP package

Part Num (249FOWLP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
F14	PIO0_0	PIO0_0	PIO0_0	FC0_SCK			CTIMER0_MAT0	I2S_BRIDGE_CLK_IN	GPIO_INT_BMAT		SEC_PIO0_0	
G16	PIO0_1	PIO0_1	PIO0_1	FC0_TXD_SCL_MISO_WS			CTIMER0_MAT1	I2S_BRIDGE_WS_IN			SEC_PIO0_1	
H16	PIO0_2	PIO0_2	PIO0_2	FC0_RXD_SDA_MOSI_DATA			CTIMER0_MAT2	I2S_BRIDGE_DATA_IN			SEC_PIO0_2	
H15	PIO0_3	PIO0_3	PIO0_3	FC0_CTS_SDA_SSEL0			CTIMER0_MAT3	FC1_SSEL2			SEC_PIO0_3	
H14	PIO0_4	PIO0_4	PIO0_4	FC0_RTS_SCL_SSEL1			CTIMER_INP0	FC1_SSEL3		CMP0_OUT	SEC_PIO0_4	
F16	PIO0_5 / ADC0_0	PIO0_5	PIO0_5	FC0_SSEL2	SCT0_GPI0	SCT0_OUT0	CTIMER_INP1				SEC_PIO0_5	
F17	PIO0_6 / ADC0_8	PIO0_6	PIO0_6	FC0_SSEL3	SCT0_GPI1	SCT0_OUT1	CTIMER0_MAT0				SEC_PIO0_6	
J15	PIO0_7 / TRST	PIO0_7	PIO0_7	FC1_SCK	SCT0_GPI4	SCT0_OUT4	CTIMER1_MAT0	I2S_BRIDGE_CLK_OUT			SEC_PIO0_7	
H12	PIO0_8 / TCK	PIO0_8	PIO0_8	FC1_TXD_SCL_MISO_WS	SCT0_GPI5	SCT0_OUT5	CTIMER1_MAT1	I2S_BRIDGE_WS_OUT			SEC_PIO0_8	
H17	PIO0_9 / TMS	PIO0_9	PIO0_9	FC1_RXD_SDA_MOSI_DATA	SCT0_GPI6	SCT0_OUT6	CTIMER1_MAT2	I2S_BRIDGE_DATA_OUT			SEC_PIO0_9	
K16	PIO0_10 / TDI	PIO0_10	PIO0_10	FC1_CTS_SDA_SSEL0	SCT0_GPI7	SCT0_OUT7	CTIMER1_MAT3	FC0_SSEL2			SEC_PIO0_10	
K15	PIO0_11 / TDO	PIO0_11	PIO0_11	FC1_RTS_SCL_SSEL1	SCT0_GPI0	SCT0_OUT8	CTIMER_INP2	FC0_SSEL3			SEC_PIO0_11	

Table continues on the next page...

Part Num (249FOWLP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
E14	PIO0_12 / ADC0_1	PIO0_12	PIO0_12	FC1_SSEL2	SCT0_GPI2	SCT0_OUT2	CTIMER_INP3				SEC_PIO0_12	
F15	PIO0_13 / ADC0_9	PIO0_13	PIO0_13	FC1_SSEL3	SCT0_GPI3	SCT0_OUT3	CTIMER0_MAT1				SEC_PIO0_13	
B12	PIO0_14	PIO0_14	PIO0_14	FC2_SCK	SCT0_GPI0	SCT0_OUT0	CTIMER2_MAT0	I2S_BRIDGE_CLK_IN			SEC_PIO0_14	
B15	PIO0_15	PIO0_15	PIO0_15	FC2_TXD_SCL_MISO_WS	SCT0_GPI1	SCT0_OUT1	CTIMER2_MAT1	I2S_BRIDGE_WS_IN			SEC_PIO0_15	
A16	PIO0_16	PIO0_16	PIO0_16	FC2_RXD_SDA_MOSI_DATA	SCT0_GPI2	SCT0_OUT2	CTIMER2_MAT2	I2S_BRIDGE_DATA_IN			SEC_PIO0_16	
B17	PIO0_17	PIO0_17	PIO0_17	FC2_CTS_SDA_SSEL0	SCT0_GPI3	SCT0_OUT3	CTIMER2_MAT3	FC5_SSEL2			SEC_PIO0_17	
B16	PIO0_18	PIO0_18	PIO0_18	FC2_RTS_SCL_SSEL1	SCT0_GPI6	SCT0_OUT6	CTIMER_INP4	FC5_SSEL3			SEC_PIO0_18	
F13	PIO0_19 / ADC0_2	PIO0_19	PIO0_19	FC2_SSEL2	SCT0_GPI4	SCT0_OUT4	CTIMER_INP5	UTICK_CAP0			SEC_PIO0_19	
A14	PIO0_21	PIO0_21	PIO0_21	FC3_SCK	SCT0_GPI5	SCT0_OUT5	CTIMER3_MAT0	CTIMER_INP11	TRACECLK		SEC_PIO0_21	
B14	PIO0_22	PIO0_22	PIO0_22	FC3_TXD_SCL_MISO_WS	SCT0_GPI6	SCT0_OUT6	CTIMER3_MAT1	CTIMER_INP7	TRACEDATA[0]		SEC_PIO0_22	
C13	PIO0_23	PIO0_23	PIO0_23	FC3_RXD_SDA_MOSI_DATA	SCT0_GPI7	SCT0_OUT8	CTIMER3_MAT2	CTIMER0_MAT3	TRACEDATA[1]		SEC_PIO0_23	
D13	PIO0_24	PIO0_24	PIO0_24	FC3_CTS_SDA_SSEL0	SCT0_GPI2	SCT0_OUT9	CTIMER3_MAT3	FC2_SSEL2	TRACEDATA[2]	CLKOUT	SEC_PIO0_24	

Table continues on the next page...

Part Num (249FOWLP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
C12	PIO0_25	PIO0_25	PIO0_25	FC3_RTS_SCL_SSEL1		FREQME_GPIO_CLK	CTIMER_INP6	FC2_SSEL3	TRACEDATA[3]	CLKIN	SEC_PIO0_25	
A12	PIO0_28	PIO0_28	PIO0_28	FC4_SCK			CTIMER4_MAT0	I2S_BRIDGE_CLK_OUT			SEC_PIO0_28	
B11	PIO0_29	PIO0_29	PIO0_29	FC4_TXD_SCL_MISO_WS			CTIMER4_MAT1	I2S_BRIDGE_WS_OUT			SEC_PIO0_29	
D14	PIO0_30	PIO0_30	PIO0_30	FC4_RXD_SDA_MOSI_DATA			CTIMER4_MAT2	I2S_BRIDGE_DATA_OUT			SEC_PIO0_30	
D12	PIO0_31	PIO0_31	PIO0_31	FC4_CTS_SDA_SSEL0	SCT0_GPI0	SCT0_OUT6	CTIMER4_MAT3	FC3_SSEL2			SEC_PIO0_31	
A10	PIO1_0	PIO1_0	PIO1_0	FC4_RTS_SCL_SSEL1	SCT0_GPI1	SCT0_OUT7	CTIMER_INP8	FC3_SSEL3				
K2	PIO1_3	PIO1_3	PIO1_3	FC5_SCK					HS_SPI1_SCK			
K1	PIO1_4	PIO1_4	PIO1_4	FC5_TXD_SCL_MISO_WS					HS_SPI1_MISO			
L2	PIO1_5	PIO1_5	PIO1_5	FC5_RXD_SDA_MOSI_DATA					HS_SPI1_MOSI			
N4	PIO1_6	PIO1_6	PIO1_6	FC5_CTS_SDA_SSEL0	SCT0_GPI4	SCT0_OUT4		FC4_SSEL2	HS_SPI1_SSELN0			
M1	PIO1_7	PIO1_7	PIO1_7	FC5_RTS_SCL_SSEL1	SCT0_GPI5	SCT0_OUT5	CTIMER_INP9	FC4_SSEL3	HS_SPI1_SSELN1			
M5	PIO1_10	PIO1_10	PIO1_10	MCLK		FREQME_GPIO_CLK	CTIMER_INP10			CLKOUT		

Table continues on the next page...

Part Num (249FOWLP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
K13	PIO1_11	PIO1_11	PIO1_11	HS_SPI0_SCK			CTIMER2_MAT0					
K14	PIO1_12	PIO1_12	PIO1_12	HS_SPI0_MISO			CTIMER2_MAT1					
K17	PIO1_13	PIO1_13	PIO1_13	HS_SPI0_MOSI			CTIMER2_MAT2					
L16	PIO1_14	PIO1_14	PIO1_14	HS_SPI0_SSELN0			CTIMER2_MAT3					
M16	PIO1_15 / ISP0	PIO1_15	PIO1_15	HS_SPI0_SSELN1			CTIMER3_MAT0					
T17	PIO1_18	PIO1_18	PIO1_18	FLEXSPI0_SCLK	SCT0_GPI0		CTIMER3_MAT3					
U16	PIO1_19	PIO1_19	PIO1_19	FLEXSPI0_SS0_N	SCT0_OUT0		CTIMER4_MAT0			CLKOUT		
T15	PIO1_20	PIO1_20	PIO1_20	FLEXSPI0_DATA0	SCT0_GPI1		CTIMER4_MAT1					
T14	PIO1_21	PIO1_21	PIO1_21	FLEXSPI0_DATA1	SCT0_OUT1		CTIMER4_MAT2					
R13	PIO1_22	PIO1_22	PIO1_22	FLEXSPI0_DATA2	SCT0_GPI2		CTIMER4_MAT3					
R12	PIO1_23	PIO1_23	PIO1_23	FLEXSPI0_DATA3	SCT0_OUT2		CTIMER_INP8					
N12	PIO1_24	PIO1_24	PIO1_24	FLEXSPI0_DATA4	SCT0_GPI3							
R14	PIO1_25	PIO1_25	PIO1_25	FLEXSPI0_DATA5	SCT0_OUT3							
P14	PIO1_26	PIO1_26	PIO1_26	FLEXSPI0_DATA6	SCT0_GPI4							
P13	PIO1_27	PIO1_27	PIO1_27	FLEXSPI0_DATA7	SCT0_OUT4							
U14	PIO1_28	PIO1_28	PIO1_28	FLEXSPI0_DQS	SCT0_GPI5							

Table continues on the next page...

Part Num (249FOWLP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
U12	PIO1_29	PIO1_29	PIO1_29	FLEXSPI0_SS1_N	SCT0_OUT5	UTICK_CAP2	CTIMER_INP13	FLEXSPI0_SCLK_N				
R5	PIO1_30	PIO1_30	PIO1_30	SD0_CLK	SCT0_GPI0							
R6	PIO1_31	PIO1_31	PIO1_31	SD0_CMD	SCT0_GPI1							
U4	PIO2_0	PIO2_0	PIO2_0	SD0_D[0]	SCT0_GPI2							SmartDMA_PIO0
T4	PIO2_1	PIO2_1	PIO2_1	SD0_D[1]	SCT0_GPI3							SmartDMA_PIO1
T7	PIO2_2	PIO2_2	PIO2_2	SD0_D[2]	SCT0_OUT0							SmartDMA_PIO2
U6	PIO2_3	PIO2_3	PIO2_3	SD0_D[3]	SCT0_OUT1							SmartDMA_PIO3
P6	PIO2_4	PIO2_4	PIO2_4	SD0_WR_PRT	SCT0_OUT2			SD0_DS				SmartDMA_PIO4
P5	PIO2_5	PIO2_5	PIO2_5	SD0_D[4]	SCT0_OUT3			FC8_SCK				SmartDMA_PIO5
R4	PIO2_6	PIO2_6	PIO2_6	SD0_D[5]	SCT0_GPI4		CTIMER1_MAT0	FC8_TXD_SCL_MISO_WS				SmartDMA_PIO6
P4	PIO2_7	PIO2_7	PIO2_7	SD0_D[6]	SCT0_GPI5		CTIMER1_MAT1	FC8_RXD_SDA_MOSI_DATA				SmartDMA_PIO7
T6	PIO2_8	PIO2_8	PIO2_8	SD0_D[7]	SCT0_OUT4		CTIMER1_MAT2	FC8_CTS_SDA_SSEL0				SmartDMA_PIO8
T3	PIO2_9	PIO2_9	PIO2_9	SD0_CARD_DET_N	SCT0_OUT5		CTIMER1_MAT3	FC8_CTS_SDA_SSEL1				SmartDMA_PIO9
N5	PIO2_10	PIO2_10	PIO2_10	SD0_RESET_N	SCT0_GPI6		CTIMER2_MAT0	FC8_SSEL2				SmartDMA_PIO10

Table continues on the next page...

Part Num (249FOWLP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
R2	PIO2_11	PIO2_11	PIO2_11	SD0_VOLT	SCT0_GPI7		CTIMER2_MAT1	FC8_SSEL3				SmartDMA_PIO11
E15	PIO2_14 / CMP0_A	PIO2_14	PIO2_14		SCT0_OUT8		CTIMER_INP1			32KHZ_CLKOUT		SmartDMA_PIO14
D17	PIO2_15 / CMP0_D	PIO2_15	PIO2_15		SCT0_OUT9					CLKIN		SmartDMA_PIO15
N3	PIO2_24	PIO2_24	PIO2_24	SWO					GPIO_INT_BMAT			SmartDMA_PIO24
M2	PIO2_25	PIO2_25	PIO2_25	SWCLK								SmartDMA_PIO25
M4	PIO2_26	PIO2_26	PIO2_26	SWDIO								SmartDMA_PIO26
M3	PIO2_27	PIO2_27	PIO2_27	USB1_OVERCURRENTN								SmartDMA_PIO27
P1	PIO2_28	PIO2_28	PIO2_28	USB1_PORTPWRN								SmartDMA_PIO28
B10	PIO2_29	PIO2_29	PIO2_29	I3C0_SCL	SCT0_OUT0			CLKOUT				SmartDMA_PIO029
D10	PIO2_30	PIO2_30	PIO2_30	I3C0_SDA	SCT0_OUT3			CLKIN		CMP0_OUT		SmartDMA_PIO30
C14	PIO2_31 / CMP0_B	PIO2_31	PIO2_31	I3C0_PUR	SCT0_OUT7	UTICK_CAP3	CTIMER_INP15	SWO				SmartDMA_PIO31
T2	USB1_VBUS	USB1_VBUS										
K5	USB1_VDD3V3	USB1_VDD3V3										
T1	USB1_DM	USB1_DM										
U2	USB1_DP	USB1_DP										
E4	PMIC_MODE1	PMIC_MODE1										

Table continues on the next page...

Part Num (249FOWLP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
D3	PMIC_MODE0	PMIC_MODE0										
K6	PMIC_I2C_SDA	PMIC_I2C_SDA										
K4	PMIC_I2C_SCL	PMIC_I2C_SCL										
D5	PMIC_IRQ_N	PMIC_IRQ_N										
C5	LDO_ENABLE	LDO_ENABLE										
B4	XTALIN	XTALIN										
A4	XTALOUT	XTALOUT										
A2	RTCXIN	RTCXIN										
B3	RTCXOUT	RTCXOUT										
C4	RESETN	RESETN										
F12	VREFP	VREFP										
G12	VREFN	VREFN										
D16	PIO3_1	PIO3_1	PIO3_1	PDM_CLK23	PDM_DATA23			FC0_TXD_SCL_MISO_WS	I3C1_SCL			
C16	PIO3_2	PIO3_2	PIO3_2	PDM_CLK45	PDM_DATA45			FC0_RXD_SDA_MOSI_DATA	I3C1_SDA			
D15	PIO3_3	PIO3_3	PIO3_3	PDM_CLK67	PDM_DATA67	LCD_D23		FC0_CTS_SDA_SSEL0	I3C1_PUR	CMP0_OUT		
A8	PIO3_8	PIO3_8	PIO3_8	SD1_CLK	LCD_D9		CTIMER0_MAT0		FC10_SCK			
B8	PIO3_9	PIO3_9	PIO3_9	SD1_CMD	LCD_D10		CTIMER0_MAT1		FC10_TXD_SCL_MISO			

Table continues on the next page...

Part Num (249FOWLP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
C8	PIO3_10	PIO3_10	PIO3_10	SD1_D[0]	LCD_D11		CTIMER0_MAT2		FC10_RXD_SDA_MOSI			
C10	PIO3_11	PIO3_11	PIO3_11	SD1_D[1]	LCD_D12		CTIMER0_MAT3		FC10_CTS_SDA_SSELN0			
A6	PIO3_12	PIO3_12	PIO3_12	SD1_D[2]	LCD_D13		CTIMER_INP0		FC10_RTS_SCL_SSELN1			
B7	PIO3_13	PIO3_13	PIO3_13	SD1_D[3]	LCD_D14		CTIMER_INP1		FC10_SSELN2			
D9	PIO3_14	PIO3_14	PIO3_14	SD1_WR_PRT	LCD_D15		CTIMER3_MAT0	SD1_DS	FC10_SSELN3			
E10	PIO3_15	PIO3_15	PIO3_15	SD1_D[4]	LCD_D16		CTIMER3_MAT1	FC5_SCK				
C9	PIO3_16	PIO3_16	PIO3_16	SD1_D[5]	LCD_D17		CTIMER3_MAT2	FC5_TXD_SCL_MISO_WS				
D8	PIO3_17	PIO3_17	PIO3_17	SD1_D[6]	LCD_D18		CTIMER3_MAT3	FC5_RXD_SDA_MOSI_DATA				
B6	PIO3_18	PIO3_18	PIO3_18	SD1_D[7]	LCD_D19		CTIMER4_MAT0	FC5_CTS_SDA_SSEL0				
C6	PIO3_19	PIO3_19	PIO3_19	SD1_CARD_DET_N	LCD_D20		CTIMER4_MAT1	MCLK				
D6	PIO3_20	PIO3_20	PIO3_20	SD1_RESET_N	LCD_D21		CTIMER4_MAT2					
E5	PIO3_21	PIO3_21	PIO3_21	SD1_VOLT	LCD_D22		CTIMER4_MAT3		GPIO_INT_BMAT			
R16	PIO3_25	PIO3_25	PIO3_25	FC6_SCK								

Table continues on the next page...

Part Num (249FOW LP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
T16	PIO3_26	PIO3_26	PIO3_26	FC6_TXD_SCL_MISO_WS								
N14	PIO3_27	PIO3_27	PIO3_27	FC6_RXD_SDA_MOSI_DATA								
N13	PIO3_28 / ISP1	PIO3_28	PIO3_28	FC6_CTS_SDA_SSEL0								
M13	PIO3_29 / ISP2	PIO3_29	PIO3_29	FC6_RTS_SCL_SSEL1								
N15	PIO4_0	PIO4_0	PIO4_0	FC7_SCK			FREQME_GPIO_CLK			CLKOUT		
M15	PIO4_1	PIO4_1	PIO4_1	FC7_TXD_SCL_MISO_WS						CLKIN		
M17	PIO4_2	PIO4_2	PIO4_2	FC7_RXD_SDA_MOSI_DATA								
M14	PIO4_3	PIO4_3	PIO4_3	FC7_CTS_SDA_SSEL0								
P17	PIO4_4	PIO4_4	PIO4_4	FC7_RTS_SCL_SSEL1				FC1_SCK				
P16	PIO4_5	PIO4_5	PIO4_5	FC7_SSEL2				FC1_TXD_SCL_MISO_WS				
P15	PIO4_6	PIO4_6	PIO4_6	FC7_SSEL3				FC1_RXD_SDA_MOSI_DATA				
D2	MIPI_DSI_CLKP	MIPI_DSI_CLKP										

Table continues on the next page...

Part Num (249FOWLP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
D1	MIPI_DSI_CLKN	MIPI_DSI_CLKN										
B1	MIPI_DSI_D0P	MIPI_DSI_D0P										
C2	MIPI_DSI_D0N	MIPI_DSI_D0N										
E3	MIPI_DSI_D1P	MIPI_DSI_D1P										
F3	MIPI_DSI_D1N	MIPI_DSI_D1N										
J8	MIPI_DSI_VDD11	MIPI_DSI_VD11										
F8	MIPI_DSI_VDD18	MIPI_DSI_VDD18										
F5	MIPI_DSI_VDDA_CAP	MIPI_DSI_VDDA_CAP										
F4	MIPI_DSI_VSS	MIPI_DSI_VSS										
H2	PIO4_11	PIO4_11	PIO4_11	FC2_SCK	FLEXSPI1_SCLK		SD1_CLK					
H1	PIO4_12	PIO4_12	PIO4_12	FC2_TXD_SCL_MISO_WS	FLEXSPI1_DATA0		SD1_CMD					
G2	PIO4_13	PIO4_13	PIO4_13	FC2_RXD_SDA_MOSI_DATA	FLEXSPI1_DATA1		SD1_D[0]					
F1	PIO4_14	PIO4_14	PIO4_14	FC2_CTS_SDA_SSEL0	FLEXSPI1_DATA2		SD1_D[1]					
K3	PIO4_15	PIO4_15	PIO4_15	FC2_RTS_SCL_SSEL1	FLEXSPI1_DATA3		SD1_D[2]					

Table continues on the next page...

Part Num (249FOWLP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
H3	PIO4_16	PIO4_16	PIO4_16	FC2_SSEL2	FLEXSPI1_DQS		SD1_D[3]					
F2	PIO4_17	PIO4_17	PIO4_17	FC2_SSEL3	FLEXSPI1_SS1_N	FLEXSPI1_SCLK_N	SD1_WR_PRT					
E13	PIO4_18 / ADC0_6	PIO4_18	PIO4_18		FLEXSPI1_SS0_N		SD1_D[4]					
R8	PIO4_20	PIO4_20	PIO4_20	DBI_CSX			SD1_D[6]		FC11_SCK		FLEXIO_D0	
P10	PIO4_21	PIO4_21	PIO4_21	DBI_DCX			SD1_D[7]		FC11_TXD_SCL_MISO		FLEXIO_D1	
U10	PIO4_22	PIO4_22	PIO4_22				SD1_CARD_DET_N		FC11_RXD_SDA_MOSI		FLEXIO_D2	
T8	PIO4_23	PIO4_23	PIO4_23	DBI_RWDX	LCD_ENABLE		SD1_RESET_N		FC11_CTS_SDA_SSELN0	TRACECLK	FLEXIO_D3	
T10	PIO4_24	PIO4_24	PIO4_24	DBI_WRX	LCD_DTCLK		SD1_VOLT		FC11_RTS_SCL_SSELN1	TRACEDATA[0]	FLEXIO_D4	
T11	PIO4_25	PIO4_25	PIO4_25	DBI_E	LCD_HSYNC				FC11_SSELN2	TRACEDATA[1]	FLEXIO_D5	
T12	PIO4_26	PIO4_26	PIO4_26	LCD_VSYNC					FC11_SSELN3	TRACEDATA[2]	FLEXIO_D6	
P9	PIO4_27	PIO4_27	PIO4_27	LCD_D0	DBI_D0					TRACEDATA[3]	FLEXIO_D7	
U8	PIO4_28	PIO4_28	PIO4_28	LCD_D1	DBI_D1						FLEXIO_D8	
P8	PIO4_29	PIO4_29	PIO4_29	LCD_D2	DBI_D2				FC12_SCK		FLEXIO_D9	
N8	PIO4_30	PIO4_30	PIO4_30	LCD_D3	DBI_D3				FC12_TXD_SCL_MISO		FLEXIO_D10	

Table continues on the next page...

Part Num (249FOWLP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
N10	PIO4_31	PIO4_31	PIO4_31	LCD_D4	DBI_D4				FC12_RXD_SDA_MOSI		FLEXIO_D11	
P12	PIO5_0	PIO5_0	PIO5_0	LCD_D5	DBI_D5				FC12_CTS_SDA_SSELN0		FLEXIO_D12	
M9	PIO5_1	PIO5_1	PIO5_1	LCD_D6	DBI_D6				FC12_RTS_SCL_SSELN1		FLEXIO_D13	
R9	PIO5_2	PIO5_2	PIO5_2	LCD_D7	DBI_D7				FC12_SSELN2	LOW_FREQ_CLKOUT	FLEXIO_D14	
R10	PIO5_3	PIO5_3	PIO5_3	LCD_D8	DBI_D8				FC12_SSELN3	LOW_FREQ_CLKOUT_N	FLEXIO_D15	
P2	PIO5_4	PIO5_4	PIO5_4	LCD_D9	DBI_D9		PDM_CLK01					
P3	PIO5_8	PIO5_8	PIO5_8	LCD_D13	DBI_D13		PDM_DATA01					
H5	PIO5_15	PIO5_15	PIO5_15	LCD_D20	FLEXSPI1_DATA4		FC4_CTS_SDA_SSEL0					
H4	PIO5_16	PIO5_16	PIO5_16	LCD_D21	FLEXSPI1_DATA5		FC4_RTS_SCL_SSEL1					
J3	PIO5_17	PIO5_17	PIO5_17	LCD_D22	FLEXSPI1_DATA6		FC4_SSEL2					
J4	PIO5_18	PIO5_18	PIO5_18	LCD_D23	FLEXSPI1_DATA7		FC4_SSEL3					
J12, J13,K12, M10,M12	VDDIO_0											

Table continues on the next page...

Part Num (249FOWLP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
E9, F10,F11, F9,J5 J6	VDDIO_1											
N6, P7	VDDIO_2											
M8 N9	VDDIO_3											
F6, F7	VDDIO_4											
G9, H10,H8, H9,J10, J11,J9, K10,K8, K9, L9	VDDCORE											
D4, B2	VDD_AO1V8											
H13	VDDA_ADC1V8											
E12	VDDA_BIAS											
D11, D7	VSSA											
A1, A17, C3, C7, C11, C15, E7, E11, G3, G4, G5, G7, G8, G10, G11, G13, G14, G15, H11, K7, K11, L3, L4, L5, L6, L7, L8, L10, L11, L12, L13, L14, L15,	VSS											

Table continues on the next page...

Part Num (249FOWLP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
M7, M11, N7, N11, P11, R3, R7, R11, R15, U1, U17												
G6, M6, H7, J7, J14, H6, E6	VDD1V8											
E8	VDD1V8_1											

12.3 i.MX RT500 Pinouts: 141 CSP package

Part Num (141WLCSP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
J1	PIO0_0	PIO0_0	PIO0_0	FC0_SCK			CTIMER0_MAT0	I2S_BRIDGE_CLK_IN	GPIO_INT_BMAT			
G3	PIO0_1	PIO0_1	PIO0_1	FC0_TXD_SCL_MISO_WS			CTIMER0_MAT1	I2S_BRIDGE_WS_IN				
F1	PIO0_10 / TDI	PIO0_10	PIO0_10	FC1_CTS_SDA_SSEL0	SCT0_GPI7	SCT0_OUT7	CTIMER1_MAT3	FC0_SSEL2				
E3	PIO0_11 / TDO	PIO0_11	PIO0_11	FC1_RTS_SCL_SSEL1	SCT0_GPI0	SCT0_OUT8	CTIMER_INP2	FC0_SSEL3				
G5	PIO0_12 / ADC0_1	PIO0_12	PIO0_12	FC1_SSEL2	SCT0_GPI2	SCT0_OUT2	CTIMER_INP3					
J2	PIO0_13 / ADC0_9	PIO0_13	PIO0_13	FC1_SSEL3	SCT0_GPI3	SCT0_OUT3	CTIMER0_MAT1					
K6	PIO0_14	PIO0_14	PIO0_14	FC2_SCK	SCT0_GPI0	SCT0_OUT0	CTIMER2_MAT0	I2S_BRIDGE_CLK_IN				
K4	PIO0_15	PIO0_15	PIO0_15	FC2_TXD_SCL_MISO_WS	SCT0_GPI1	SCT0_OUT1	CTIMER2_MAT1	I2S_BRIDGE_WS_IN				
M3	PIO0_16	PIO0_16	PIO0_16	FC2_RXD_SDA_MOSI_DATA	SCT0_GPI2	SCT0_OUT2	CTIMER2_MAT2	I2S_BRIDGE_DATA_IN				
M2	PIO0_17	PIO0_17	PIO0_17	FC2_CTS_SDA_SSEL0	SCT0_GPI3	SCT0_OUT3	CTIMER2_MAT3	FC5_SSEL2				
J4	PIO0_18	PIO0_18	PIO0_18	FC2_RTS_SCL_SSEL1	SCT0_GPI6	SCT0_OUT6	CTIMER_INP4	FC5_SSEL3				
H4	PIO0_19 / ADC0_2	PIO0_19	PIO0_19	FC2_SSEL2	SCT0_GPI4	SCT0_OUT4	CTIMER_INP5	UTICK_CAP0				

Table continues on the next page...

Part Num (141WLCSP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
H2	PIO0_2	PIO0_2	PIO0_2	FC0_RXD_SDA_MOSI_DATA			CTIMER0_MAT2	I2S_BRIDGE_DATA_IN				
M4	PIO0_21	PIO0_21	PIO0_21	FC3_SCK	SCT0_GPI5	SCT0_OUT5	CTIMER3_MAT0	CTIMER_INP11	TRACECLK			
J5	PIO0_22	PIO0_22	PIO0_22	FC3_TXD_SCL_MISO_WS	SCT0_GPI6	SCT0_OUT6	CTIMER3_MAT1	CTIMER_INP7	TRACEDATA[0]			
L5	PIO0_23	PIO0_23	PIO0_23	FC3_RXD_SDA_MOSI_DATA	SCT0_GPI7	SCT0_OUT8	CTIMER3_MAT2	CTIMER0_MAT3	TRACEDATA[1]			
L4	PIO0_24	PIO0_24	PIO0_24	FC3_CTS_SDA_SSEL0	SCT0_GPI2	SCT0_OUT9	CTIMER3_MAT3	FC2_SSEL2	TRACEDATA[2]	CLKOUT		
H6	PIO0_25	PIO0_25	PIO0_25	FC3_RTS_SCL_SSEL1		FREQME_GPIO_CLK	CTIMER_INP6	FC2_SSEL3	TRACEDATA[3]	CLKIN		
M6	PIO0_28	PIO0_28	PIO0_28	FC4_SCK			CTIMER4_MAT0	I2S_BRIDGE_CLK_OUT				
J7	PIO0_29	PIO0_29	PIO0_29	FC4_TXD_SCL_MISO_WS			CTIMER4_MAT1	I2S_BRIDGE_WS_OUT				
G2	PIO0_3	PIO0_3	PIO0_3	FC0_CTS_SDA_SSEL0			CTIMER0_MAT3	FC1_SSEL2				
L3	PIO0_30	PIO0_30	PIO0_30	FC4_RXD_SDA_MOSI_DATA			CTIMER4_MAT2	I2S_BRIDGE_DATA_OUT				
J6	PIO0_31	PIO0_31	PIO0_31	FC4_CTS_SDA_SSEL0	SCT0_GPI0	SCT0_OUT6	CTIMER4_MAT3	FC3_SSEL2				
F4	PIO0_4	PIO0_4	PIO0_4	FC0_RTS_SCL_SSEL1			CTIMER_INP0	FC1_SSEL3		CMP0_OUT		

Table continues on the next page...

Part Num (141WLCSP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
H3	PIO0_5 / ADC0_0	PIO0_5	PIO0_5	FC0_SSEL2	SCT0_GPI0	SCT0_OUT0	CTIMER_INP1					
K1	PIO0_6 / ADC0_8	PIO0_6	PIO0_6	FC0_SSEL3	SCT0_GPI1	SCT0_OUT1	CTIMER0_MAT0					
E4	PIO0_7 / TRST	PIO0_7	PIO0_7	FC1_SCK	SCT0_GPI4	SCT0_OUT4	CTIMER1_MAT0	I2S_BRIDGE_CLK_OUT				
G1	PIO0_8 / TCK	PIO0_8	PIO0_8	FC1_TXD_SCL_MISO_WS	SCT0_GPI5	SCT0_OUT5	CTIMER1_MAT1	I2S_BRIDGE_WS_OUT				
F3	PIO0_9 / TMS	PIO0_9	PIO0_9	FC1_RXD_SDA_MOSI_DATA	SCT0_GPI6	SCT0_OUT6	CTIMER1_MAT2	I2S_BRIDGE_DATA_OUT				
L7	PIO1_0	PIO1_0	PIO1_0	FC4_RTS_SCL_SSEL1	SCT0_GPI1	SCT0_OUT7	CTIMER_INP8	FC3_SSEL3				
D3	PIO1_11	PIO1_11	PIO1_11	HS_SPI0_SCK			CTIMER2_MAT0					
E2	PIO1_12	PIO1_12	PIO1_12	HS_SPI0_MISO			CTIMER2_MAT1					
D2	PIO1_13	PIO1_13	PIO1_13	HS_SPI0_MOSI			CTIMER2_MAT2					
C2	PIO1_14	PIO1_14	PIO1_14	HS_SPI0_SSELN0			CTIMER2_MAT3					
D1	PIO1_15 / ISP0	PIO1_15	PIO1_15	HS_SPI0_SSELN1			CTIMER3_MAT0					
A5	PIO1_18	PIO1_18	PIO1_18	FLEXSPI0_SCLK	SCT0_GPI0		CTIMER3_MAT3					
D4	PIO1_19	PIO1_19	PIO1_19	FLEXSPI0_SS0_N	SCT0_OUT0		CTIMER4_MAT0			CLKOUT		
B5	PIO1_20	PIO1_20	PIO1_20	FLEXSPI0_DATA0	SCT0_GPI1		CTIMER4_MAT1					

Table continues on the next page...

Part Num (141WLCSP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
C5	PIO1_21	PIO1_21	PIO1_21	FLEXSPI0_DATA1	SCT0_OUT1		CTIMER4_MAT2					
D5	PIO1_22	PIO1_22	PIO1_22	FLEXSPI0_DATA2	SCT0_GPI2		CTIMER4_MAT3					
C6	PIO1_23	PIO1_23	PIO1_23	FLEXSPI0_DATA3	SCT0_OUT2		CTIMER_INP8					
A6	PIO1_28	PIO1_28	PIO1_28	FLEXSPI0_DQS	SCT0_GPI5							
F11	PIO1_3	PIO1_3	PIO1_3	FC5_SCK					HS_SPI1_SCK			
F12	PIO1_4	PIO1_4	PIO1_4	FC5_TXD_SCL_MISO_WS					HS_SPI1_MISO			
E12	PIO1_5	PIO1_5	PIO1_5	FC5_RXD_SDA_MOSI_DATA					HS_SPI1_MOSI			
E9	PIO1_6	PIO1_6	PIO1_6	FC5_CTS_SDA_SSEL0	SCT0_GPI4	SCT0_OUT4		FC4_SSEL2	HS_SPI1_SSELN0			
F9	PIO1_7	PIO1_7	PIO1_7	FC5_RTS_SCL_SSEL1	SCT0_GPI5	SCT0_OUT5	CTIMER_INP9	FC4_SSEL3	HS_SPI1_SSELN1			
L2	PIO1_9 / ADC0_12 / CMP1_B	PIO1_9	PIO1_9	FC5_SSEL3	SCT0_GPI7	UTICK_CAP1	CTIMER1_MAT3		HS_SPI1_SSELN3			
K2	PIO2_14 / CMP0_A	PIO2_14	PIO2_14		SCT0_OUT8		CTIMER_INP1			32KHZ_CLKOUT		SmartDMA_PIO14
L1	PIO2_15 / CMP0_D	PIO2_15	PIO2_15		SCT0_OUT9					CLKIN		SmartDMA_PIO15
E8	PIO2_24	PIO2_24	PIO2_24	SWO					GPIO_INT_BMAT			SmartDMA_PIO24
F10	PIO2_25	PIO2_25	PIO2_25	SWCLK								SmartDMA_PIO25

Table continues on the next page...

Part Num (141WLCSP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
E11	PIO2_26	PIO2_26	PIO2_26	SWDIO								SmartDMA_PIO26
E10	PIO2_27	PIO2_27	PIO2_27	USB1_OVERCURRENTN								SmartDMA_PIO27
M7	PIO2_29	PIO2_29	PIO2_29	I3C0_SCL	SCT0_OUT0			CLKOUT				SmartDMA_PIO29
K7	PIO2_30	PIO2_30	PIO2_30	I3C0_SDA	SCT0_OUT3			CLKIN		CMP0_OUT		SmartDMA_PIO30
K5	PIO2_31 / CMP0_B	PIO2_31	PIO2_31	I3C0_PUR	SCT0_OUT7	UTICK_CAP3	CTIMER_INP15	SWO				SmartDMA_PIO31
A4	PIO3_28 / ISP1	PIO3_28	PIO3_28	FC6_CTS_SDA_SSEL0								
B4	PIO3_29 / ISP2	PIO3_29	PIO3_29	FC6_RTS_SCL_SSEL1								
B8	PIO4_20	PIO4_20	PIO4_20	DBI_CSX					FC11_SCK		FLEXIO_D0	
B7	PIO4_21	PIO4_21	PIO4_21	DBI_DCX					FC11_TXD_SCL_MISO		FLEXIO_D1	
A8	PIO4_22	PIO4_22	PIO4_22						FC11_RXD_SDA_MOSI		FLEXIO_D2	
E7	PIO4_23	PIO4_23	PIO4_23	DBI_RWDX	LCD_ENABLE				FC11_CTS_SDA_SSELN0	TRACECLK	FLEXIO_D3	
C7	PIO4_24	PIO4_24	PIO4_24	DBI_WRX	LCD_DTCLK				FC11_RTS_SCL_SSELN1	TRACEDATA[0]	FLEXIO_D4	
D7	PIO4_25	PIO4_25	PIO4_25	DBI_E	LCD_HSYNC				FC11_SSELN2	TRACEDATA[1]	FLEXIO_D5	

Table continues on the next page...

Part Num (141WLCSP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
D6	PIO4_26	PIO4_26	PIO4_26	LCD_VSYNC					FC11_SSELN3	TRACEDATA[2]	FLEXIO_D6	
C8	PIO4_27	PIO4_27	PIO4_27	LCD_D0	DBI_D0					TRACEDATA[3]	FLEXIO_D7	
B10	PIO4_28	PIO4_28	PIO4_28	LCD_D1	DBI_D1						FLEXIO_D8	
D8	PIO4_29	PIO4_29	PIO4_29	LCD_D2	DBI_D2				FC12_SCK		FLEXIO_D9	
C9	PIO4_30	PIO4_30	PIO4_30	LCD_D3	DBI_D3				FC12_TXD_SCL_MISO		FLEXIO_D10	
B9	PIO4_31	PIO4_31	PIO4_31	LCD_D4	DBI_D4				FC12_RXD_SDA_MOSI		FLEXIO_D11	
D9	PIO5_4	PIO5_4	PIO5_4	LCD_D9	DBI_D9		PDM_CLK01					
C11	PIO5_8	PIO5_8	PIO5_8	LCD_D13	DBI_D13		PDM_DATA01					
C4	PIO6_27	PIO6_27	PIO6_27	MCLK								
J12	MIPI_DSI_CLKN	MIPI_DSI_CLKN										
H11	MIPI_DSI_CLKP	MIPI_DSI_CLKP										
H9	MIPI_DSI_D0N	MIPI_DSI_D0N										
H8	MIPI_DSI_D0P	MIPI_DSI_D0P										
H12	MIPI_DSI_VDD11											
G10	MIPI_DSI_VDD18											

Table continues on the next page...

Part Num (141WLCSP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
K12	MIPI_DSI_VDDA_CAP											
J11	MIPI_DSI_VSS											
K9	PMIC_IRQ_N	PMIC_IRQ_N										
K10	PMIC_MODE0	PMIC_MODE0										
J9	PMIC_MODE1	PMIC_MODE1										
L11	RESETN	RESETN										
J10	RTCXIN	RTCXIN										
K11	RTCXOUT	RTCXOUT										
B11	USB1_DM	USB1_DM										
B12	USB1_DP	USB1_DP										
D10	USB1_VDD3V3	USB1_VDD3V3										
K3	VREFN/VSSA	VREFN										
J3	VREFP/VDDA_ADC1V8/VDDA_BIAS	VREFP										
L9	XTALIN	XTALIN										
K8	XTALOUT	XTALOUT										
A3, B1, B6, E1, F2, G4	VDDIO_0											
D11, G6, H5, L6, M5	VDDIO_1											

Table continues on the next page...

Part Num (141WLCSP)	Pin Name	DEFAULT	Func 0	Func 1	Func 2	Func 3	Func 4	Func 5	Func 6	Func 7	Func 8	Func 15
NC	VDDIO_2											
E5	VDDIO_3											
NC	VDDIO_4											
A10, B2, C1, C3, C10, C12, E6, F6, G7, G12, M8	VDDCORE											
A11, L12, M11, F5, L8	VDD1V8											
L10	VDD_AO1V8											
M10	VDD1V8_1											
J8	VSSA											
A1, A2, A12, B3, F7, F8, G8, G11, H1, H7, G9, H10, M1, M9, M12	VSS											

12.4 249-pin FOWLP and 141-pin WLCSP ballmaps

The following figure shows the 249 FOWLP ballmap for this device.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	VSS	RTCXIN		XTALOUT		PIO3_12		PIO3_8		PIO1_0		PIO0_28		PIO0_21		PIO0_16	VSS
B	MIPI_DSI_D0P	VDD_AO1V8	RTCXOUT	XTALIN		PIO3_18	PIO3_13	PIO3_9		PIO2_29	PIO0_29	PIO0_14		PIO0_22	PIO0_15	PIO0_18	PIO0_17
C		MIPI_DSI_D0N	VSS	RESETN	LDO_ENABLE	PIO3_19	VSS	PIO3_10	PIO3_16	PIO3_11	VSS	PIO0_25	PIO0_23	PIO2_31	VSS	PIO3_2	
D	MIPI_DSI_CLKN	MIPI_DSI_CLKP	PMIC_MODE0	VDD_AO1V8	PMIC_IRQ_N	PIO3_20	VSSA	PIO3_17	PIO3_14	PIO2_30	VSSA	PIO0_31	PIO0_24	PIO0_30	PIO3_3	PIO3_1	PIO2_15
E			MIPI_DSI_D1P	PMIC_MODE1	PIO3_21	VDD1V8	VSS	VDD1V8_1	VDDIO_1	PIO3_15	VSS	VDDA_BIAS	PIO4_18	PIO0_12	PIO2_14		
F	PIO4_14	PIO4_17	MIPI_DSI_D1N	MIPI_DSI_VSS	MIPI_DSI_VDDA_CAP	VDDIO_4	VDDIO_4	MIPI_DSI_VDDA18	VDDIO_1	VDDIO_1	VDDIO_1	VREFP	PIO0_19	PIO0_0	PIO0_13	PIO0_5	PIO0_6
G		PIO4_13	VSS	VSS	VSS	VDD1V8	VSS	VSS	VDDCORE	VSS	VSS	VREFN	VSS	VSS	VSS	PIO0_1	
H	PIO4_12	PIO4_11	PIO4_16	PIO5_16	PIO5_15	VDD1V8	VDD1V8	VDDCORE	VDDCORE	VDDCORE	VSS	PIO0_8	VDDA_ADC1V8	PIO0_4	PIO0_3	PIO0_2	PIO0_9
J			PIO5_17	PIO5_18	VDDIO_1	VDDIO_1	VDD1V8	MIPI_DSI_VDD11	VDDCORE	VDDCORE	VDDCORE	VDDIO_0	VDDIO_0	VDD1V8	PIO0_7		
K	PIO1_4	PIO1_3	PIO4_15	PMIC_I2C_SCL	USB1_VDD3V3	PMIC_I2C_SDA	VSS	VDDCORE	VDDCORE	VDDCORE	VSS	VDDIO_0	PIO1_11	PIO1_12	PIO0_11	PIO0_10	PIO1_13
L		PIO1_5	VSS	VSS	VSS	VSS	VSS	VSS	VDDCORE	VSS	VSS	VSS	VSS	VSS	VSS	PIO1_14	
M	PIO1_7	PIO2_25	PIO2_27	PIO2_26	PIO1_10	VDD1V8	VSS	VDDIO_3	PIO5_1	VDDIO_0	VSS	VDDIO_0	PIO3_29	PIO4_3	PIO4_1	PIO1_15	PIO4_2
N			PIO2_24	PIO1_6	PIO2_10	VDDIO_2	VSS	PIO4_30	VDDIO_3	PIO4_31	VSS	PIO1_24	PIO3_28	PIO3_27	PIO4_0		
P	PIO2_28	PIO5_4	PIO5_8	PIO2_7	PIO2_5	PIO2_4	VDDIO_2	PIO4_29	PIO4_27	PIO4_21	VSS	PIO5_0	PIO1_27	PIO1_26	PIO4_6	PIO4_5	PIO4_4
R		PIO2_11	VSS	PIO2_6	PIO1_30	PIO1_31	VSS	PIO4_20	PIO5_2	PIO5_3	VSS	PIO1_23	PIO1_22	PIO1_25	VSS	PIO3_25	
T	USB1_DM	USB1_VBUS	PIO2_9	PIO2_1		PIO2_8	PIO2_2	PIO4_23		PIO4_24	PIO4_25	PIO4_26		PIO1_21	PIO1_20	PIO3_26	PIO1_18
U	VSS	USB1_DP		PIO2_0		PIO2_3		PIO4_28		PIO4_22		PIO1_29		PIO1_28		PIO1_19	VSS

Figure 45. i.MX RT500 249-pin FOWLP ballmap

The following figure shows the 141-pin WLCSP ballmap for this device.

	1	2	3	4	5	6	7	8	9	10	11	12
M	VSS	PIO0_17	PIO0_16	PIO0_21	VDDIO_1	PIO0_28	PIO2_29	VDDCORE	VSS	VDD1V8_1	VDD1V8	VSS
L	PIO2_15	PIO1_9	PIO0_30	PIO0_24	PIO0_23	VDDIO_1	PIO1_0	VDD1V8	XTALOUT	VDD_AO1V8	RESETN	VDD1V8
K	PIO0_6	PIO2_14	VSSA	PIO0_15	PIO2_31	PIO0_14	PIO2_30	XTALOUT	PMIC_IRQ	PMIC_MODE0	RTCXOUT	MIPI_DSI_VDDA_CAP
J	PIO0_0	PIO0_13	VDDA_ADC1V8	PIO0_18	PIO0_22	PIO0_31	PIO0_29	VSSA	PMIC_MODE1	RTCXIN	MIPI_DSI_VSS	MIPI_DSI_CLKN
H	VSS	PIO0_2	PIO0_5	PIO0_19	VDDIO_1	PIO0_25	VSS	MIPI_DSI_D0P	MIPI_DSI_D0N	VSS	MIPI_DSI_CLKP	MIPI_DSI_VDD11
G	PIO0_8	PIO0_3	PIO0_1	VDDIO_0	PIO0_12	VDDIO_1	VDDCORE	VSS	VSS	MIPI_DSI_VDD18	VSS	VDDCORE
F	PIO0_10	VDDIO_0	PIO0_9	PIO0_4	VDD1V8	VDDCORE	VSS	VSS	PIO1_7	PIO2_25	PIO1_3	PIO1_4
E	VDDIO_0	PIO1_12	PIO0_11	PIO0_7	VDDIO_3	VDDCORE	PIO4_23	PIO2_24	PIO1_6	PIO2_27	PIO2_26	PIO1_5
D	PIO1_15	PIO1_13	PIO1_11	PIO1_19	PIO1_22	PIO4_26	PIO4_25	PIO4_29	PIO5_4	USB1_VDD3V3	VDDIO_1	
C	VDDCORE	PIO1_14	VDDCORE	PIO6_27	PIO1_21	PIO1_23	PIO4_24	PIO4_27	PIO4_30	VDDCORE	PIO5_8	VDDCORE
B	VDDIO_0	VDDCORE	VSS	PIO3_29	PIO1_20	VDDIO_0	PIO4_21	PIO4_20	PIO4_31	PIO4_28	USB1_DM	USB1_DP
A	VSS	VSS	VDDIO_0	PIO3_28	PIO1_18	PIO1_28		PIO4_22		VDDCORE	VDD1V8	VSS

Figure 46. i.MX RT500 141-pin CSP ballmap

12.5 Termination of unused pins

The following table shows how to terminate pins on functions that are not used in the application. Unused Fail Safe GPIO pins can be left unconnected. High Speed GPIO pins must not float, whether they are used or not. Other unused pins may require biasing with a resistor or directly to a power rail.

By default, unused pins with GPIO functions are tri-stated with the input buffer disabled.

All power pins in the domains listed below must be connected to the recommended voltage.

Function	Pin Name	Default state[1]	Recommended termination of unused pins
GPIO	All PIOn pins (Fail Safe)	Z	Leave unconnected.
GPIO	All PIOn pins (High Speed)	Z	Deep power-down mode - 10 kΩ resistor to ground.
GPIO	All PIOn pins (High Speed)	Z	Enable internal pull-down or use external resistor to ground in all other power modes.
PMIC Control	PMIC_I2C_SCL/SDA	Z	Leave unconnected. [2]
PMIC Control	PMIC_IRQ_N	I, Z	10 kΩ resistor to VDD_AO1V8.
PMIC Control	PMIC_MODEn	O	Leave unconnected.
Control	LDO_ENABLE	I	10 kΩ resistor to ground.
Control	RESETN	I	100 kΩ resistor to VDD_AO1V8.
Oscillator	RTCXIN	I	Connect to ground.
Oscillator	RTCXOUT	-	Leave unconnected.
Oscillator	XTALIN	I	Connect to ground.
Oscillator	XTALOUT	-	Leave unconnected.
USB1	USB1_DM/DP	-	Leave unconnected.
USB1	USB1_VBUS[3]	-	Leave unconnected.
USB1	USB1_VDD3V3	-	Leave unconnected.
MIPI_DSI	MIPI_DSI_VDD11	-	10 kΩ resistor to ground.
MIPI_DSI	MIPI_DSI_VDD18	-	10 kΩ resistor to ground.
MIPI_DSI	MIPI_DSI_VDDA_CAP	-	Leave unconnected.
MIPI_DSI	MIPI_DSI_VSS	-	Connect to ground.
MIPI_DSI	MIPI_DSI_D0N/D0P	-	Leave unconnected.
MIPI_DSI	MIPI_DSI_D1N/D1P	-	Leave unconnected.

Table continues on the next page...

Function	Pin Name	Default state[1]	Recommended termination of unused pins
MIPI_DSI	MIPI_DSI_CLKP	-	Leave unconnected.
MIPI_DSI	MIPI_DSI_CLKN	-	Leave unconnected.
Analog	VREFP	-	Connect to VDDA_ADC1V8.
Analog	VREFN	-	Connect to ground.
Power	VDDCORE	-	Connect to 1.0V power.
Power	VDD1V8	-	Connect to 1.8V power.
Power	VDD_1V8_1	-	Connect to 1.8V power during active. Can be powered off during deep sleep mode to reduce current consumption by approximately 22 uA.
Power	VDD_AO1V8	-	Connect to 1.8V power.
Power	VDDIO_n		Connect to 1.8V power.
Power	VDDA_ADC1V8	-	Connect to 1.8V power.
Power	VDDA_BIAS	-	Connect to 1.8V power.
Power	VSSA	-	Connect to ground.
Power	VSS	-	Connect to ground.

1. Z = high impedance; I = Input; O = Output
2. For the WLCSP package, in addition to managing the externally bonded High Speed pins on the package, the following unbonded High Speed pins need to be configured via software with internal pull-down resistors: PIO1_24 - 27, PIO1_29, PIO4_11 - 17, PIO5_15 - 18.
3. On WLCSP package, USB ISP mode is not supported. VBUS pin is not available on the WLCSP package. To detect VBUS connection, user can connect a GPIO pin to the USB connector's VBUS. When a rising edge occurs on the GPIO pin, software should set bit 10 (FORCE_VBUS) and bit 16 (DCON) in the DEVCMDSTAT register.

12.6 Pin states in different power modes

Table 56. Pin states in different power modes

Pin	Active	Sleep	Deep-sleep	Deep power-down[1]
All PIOn pins	As configured in IOPCTL[2]. Default is Z (input, pull-up, and pull-down disabled), except for a few pins where the pull-up and input are enabled.			Floating

1. Deep Power-down mode is not supported in the WLCSP package.
2. Default and programmed pin states are retained in sleep and deep-sleep.

12.7 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
249-pin FOWLP	98ASA01357D
141-pin WLCSP	98ASA01653D

13 Revision history

Table 57. Revision history

Rev. No.	Date	Substantial changes
0	02/2021	Initial public release
1	09/2022	• Updated the Features list within Front Matter Content . • Updated core frequency to be 275 MHz, throughout the document. • Updated this table. • Updated Figure 1 • Added a note to USB1_VBUS signal, throughout the document. • Updated the section Power consumption operating behavior • Updated Table 20 and Table 21. • Updated Table 2 and Table 5. • Updated the section I^2S-bus interface • Updated Table 35 • Updated the section Wake-up process. • Updated the section Power supply for pins and moved it before the I/O DC parameters section.. • Updated the section I/O DC parameters • Added Table 31 • Updated the section CoreMark data • Updated the section Power sequence. • Added the section LVD operating requirements. • Updated Table 21. • Updated Table 31. • Updated the section Crystal oscillator , RTC oscillator, and

Table continues on the next page...

Table 57. Revision history

Rev. No.	Date	Substantial changes

		Internal low-power oscillator (1 MHz) .
		• Updated the section Improved Inter-Integrated Circuit Interface (MIPI-I3C) specifications.
		• Updated the section External Clock Input (CLKIN) pin.
		• Updated the section Main/System and Audio PLLs
		• Updated ADC temperature sensor.
		• Updated VDD in Comparator characteristics.
		• Updated the FlexComm instance in the title of High-Speed SPI interface (Flexcomm interfaces 14 and 16)
		• Updated operating voltage range for DMIC subsystem.
		• Changed USB0 to USB1 in USB High Speed Transceiver and PHY specifications.
		• Updated Figure 35.
		• Updated module descriptions of GPU2D, PLL0, LPO, and PLL1 in RT500 modules list.
		• Updated the section Standard I/O pin configuration.
		• Updated graphs in the section Application information
		• Updated the following sections:
		  • RTC Printed Circuit Board (PCB) design guidelines
		  • XTAL oscillator
		  • XTAL Printed Circuit Board (PCB) design guidelines
		  • Temperature compensated crystal oscillator (TCXO)
		  • Signal multiplexing and pinouts
		  • Added FC12_SCK to PIO4_29 pin in i.MXRT500 Pinouts: 249 FOWLP package and removed all SD1 pins from i.MX RT500 Pinouts: 141 CSP package
		  • Updated the section Termination of unused pins
		  • Pin states in different power modes.
		  • Added the sections Main/System and Audio PLLs, Boundary scan method,

Table continues on the next page...

Table 57. Revision history (continued)

Rev. No.	Date	Substantial changes
		and External Master Clock (MCLK) pin
2	05/2023	• Added the section Free-running oscillator FRO-250M specifications. • Updated the section General operating conditions for FRO250M specifications. • Updated Table 20.

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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