



## K51 Sub-Family

Supports: MK51DX256CLL7,  
MK51DX128CMC7, MK51DX256CMC7

### Features

- Operating Characteristics
  - Voltage range: 1.71 to 3.6 V
  - Flash write voltage range: 1.71 to 3.6 V
  - Temperature range (ambient): -40 to 85°C
- Clocks
  - 3 to 32 MHz crystal oscillator
  - 32 kHz crystal oscillator
  - Multi-purpose clock generator
- System peripherals
  - Multiple low-power modes to provide power optimization based on application requirements
  - 16-channel DMA controller, supporting up to 63 request sources
  - External watchdog monitor
  - Software watchdog
  - Low-leakage wakeup unit
- Security and integrity modules
  - Hardware CRC module to support fast cyclic redundancy checks
  - 128-bit unique identification (ID) number per chip
- Human-machine interface
  - Segment LCD controller supporting up to 36 frontplanes and 8 backplanes, or 40 frontplanes and 4 backplanes, depending on the package size
  - Low-power hardware touch sensor interface (TSI)
  - General-purpose input/output

## K51P100M72SF1



- Analog modules
  - Two 16-bit SAR ADCs
  - Programmable gain amplifier (PGA) (up to x64) integrated into each ADC
  - 12-bit DAC
  - Two operational amplifiers
  - One transimpedance amplifier
  - Three analog comparators (CMP) containing a 6-bit DAC and programmable reference input
  - Voltage reference
- Timers
  - Programmable delay block
  - Eight-channel motor control/general purpose/PWM timer
  - Two 2-channel quadrature decoder/general purpose timers
  - Periodic interrupt timers
  - 16-bit low-power timer
  - Carrier modulator transmitter
  - Real-time clock
- Communication interfaces
  - USB full-/low-speed On-the-Go controller with on-chip transceiver
  - Two SPI modules
  - Two I2C modules
  - Five UART modules
  - I2S module

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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# 1 Ordering parts

## 1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to [www.freescale.com](http://www.freescale.com) and perform a part number search for the following device numbers: PK51 and MK51.

# 2 Part identification

## 2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

## 2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	<ul style="list-style-type: none"> <li>M = Fully qualified, general market flow</li> <li>P = Prequalification</li> </ul>
K##	Kinetis family	<ul style="list-style-type: none"> <li>K51</li> </ul>
A	Key attribute	<ul style="list-style-type: none"> <li>D = Cortex-M4 w/ DSP</li> <li>F = Cortex-M4 w/ DSP and FPU</li> </ul>
M	Flash memory type	<ul style="list-style-type: none"> <li>N = Program flash only</li> <li>X = Program flash and FlexMemory</li> </ul>

*Table continues on the next page...*

Field	Description	Values
FFF	Program flash memory size	<ul style="list-style-type: none"> <li>• 32 = 32 KB</li> <li>• 64 = 64 KB</li> <li>• 128 = 128 KB</li> <li>• 256 = 256 KB</li> <li>• 512 = 512 KB</li> <li>• 1M0 = 1 MB</li> </ul>
R	Silicon revision	<ul style="list-style-type: none"> <li>• Z = Initial</li> <li>• (Blank) = Main</li> <li>• A = Revision after main</li> </ul>
T	Temperature range (°C)	<ul style="list-style-type: none"> <li>• V = -40 to 105</li> <li>• C = -40 to 85</li> </ul>
PP	Package identifier	<ul style="list-style-type: none"> <li>• FM = 32 QFN (5 mm x 5 mm)</li> <li>• FT = 48 QFN (7 mm x 7 mm)</li> <li>• LF = 48 LQFP (7 mm x 7 mm)</li> <li>• LH = 64 LQFP (10 mm x 10 mm)</li> <li>• MP = 64 MAPBGA (5 mm x 5 mm)</li> <li>• LK = 80 LQFP (12 mm x 12 mm)</li> <li>• LL = 100 LQFP (14 mm x 14 mm)</li> <li>• MC = 121 MAPBGA (8 mm x 8 mm)</li> <li>• LQ = 144 LQFP (20 mm x 20 mm)</li> <li>• MD = 144 MAPBGA (13 mm x 13 mm)</li> <li>• MJ = 256 MAPBGA (17 mm x 17 mm)</li> </ul>
CC	Maximum CPU frequency (MHz)	<ul style="list-style-type: none"> <li>• 5 = 50 MHz</li> <li>• 7 = 72 MHz</li> <li>• 10 = 100 MHz</li> <li>• 12 = 120 MHz</li> <li>• 15 = 150 MHz</li> </ul>
N	Packaging type	<ul style="list-style-type: none"> <li>• R = Tape and reel</li> <li>• (Blank) = Trays</li> </ul>

## 2.4 Example

This is an example part number:

MK51DN512ZVMD10

## 3 Terminology and guidelines

### 3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

### 3.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

Symbol	Description	Min.	Max.	Unit
$V_{DD}$	1.0 V core supply voltage	0.9	1.1	V

## 3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

### 3.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

Symbol	Description	Min.	Max.	Unit
$I_{WP}$	Digital I/O weak pullup/pulldown current	10	130	$\mu A$

## 3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

### 3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
$C_{IN\_D}$	Input capacitance: digital pins	—	7	pF

### 3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

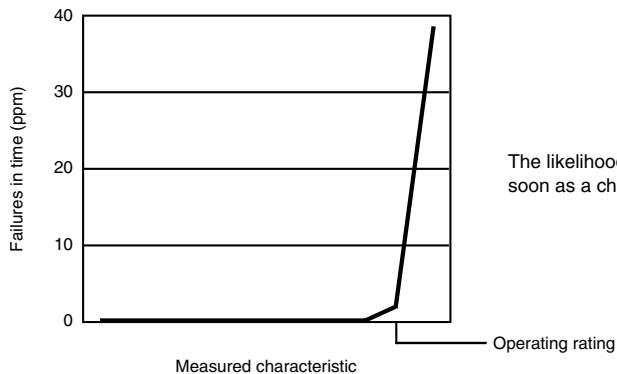
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

#### 3.4.1 Example

This is an example of an operating rating:

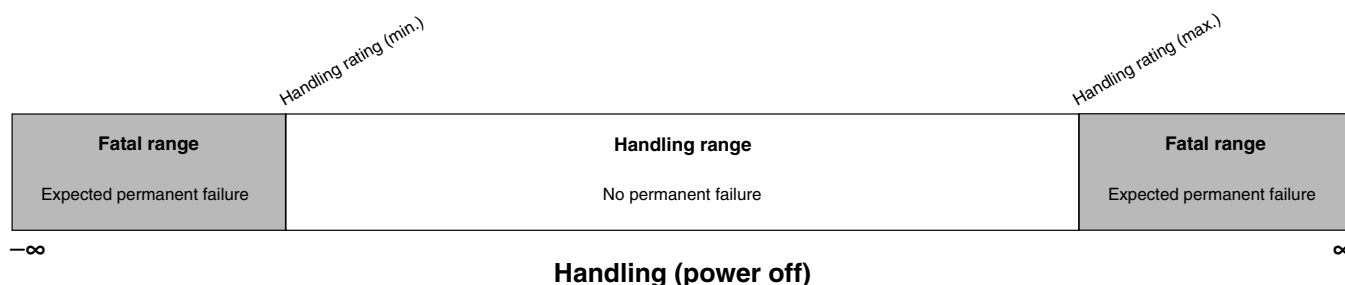
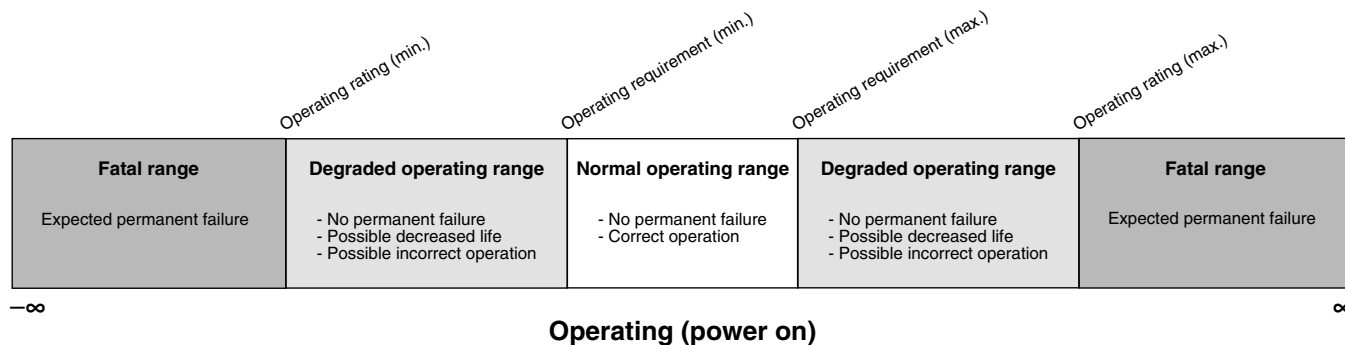
Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	1.0 V core supply voltage	-0.3	1.2	V

### 3.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

### 3.6 Relationship between ratings and operating requirements



### 3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip’s ratings.
- During normal operation, don’t exceed any of the chip’s operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

### 3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.



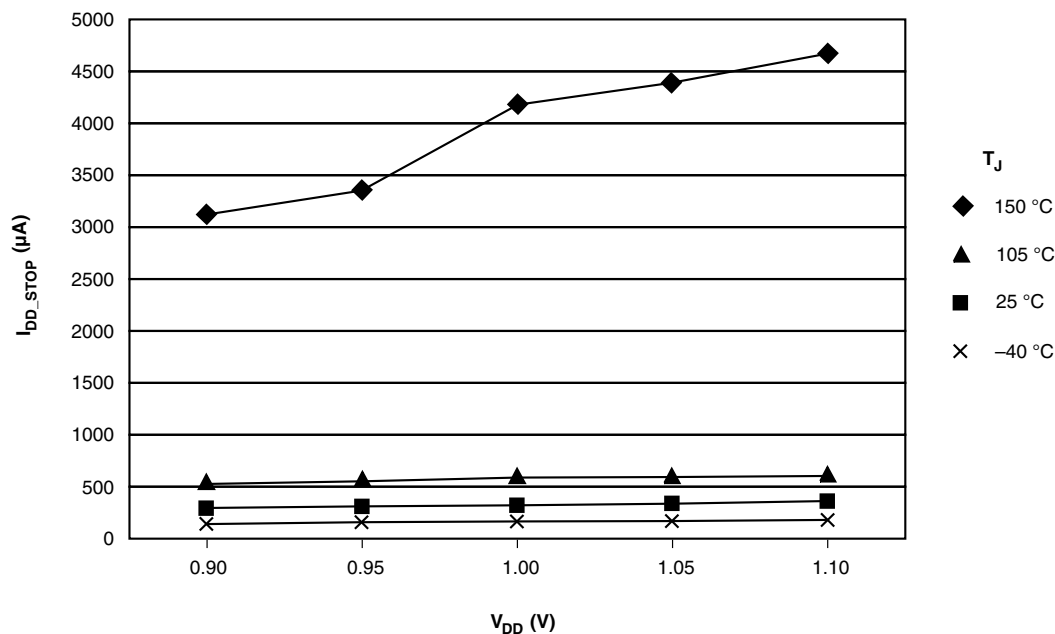
### 3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
$I_{WP}$	Digital I/O weak pullup/pulldown current	10	70	130	$\mu\text{A}$

### 3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



## 3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
$T_A$	Ambient temperature	25	$^{\circ}\text{C}$
$V_{DD}$	3.3 V supply voltage	3.3	V

## 4 Ratings

### 4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T <sub>STG</sub>	Storage temperature	-55	150	°C	1
T <sub>SDR</sub>	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

### 4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

### 4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>HBM</sub>	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V <sub>CDM</sub>	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I <sub>LAT</sub>	Latch-up current at ambient temperature of 105°C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

### 4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	Digital supply voltage	-0.3	3.8	V

Table continues on the next page...

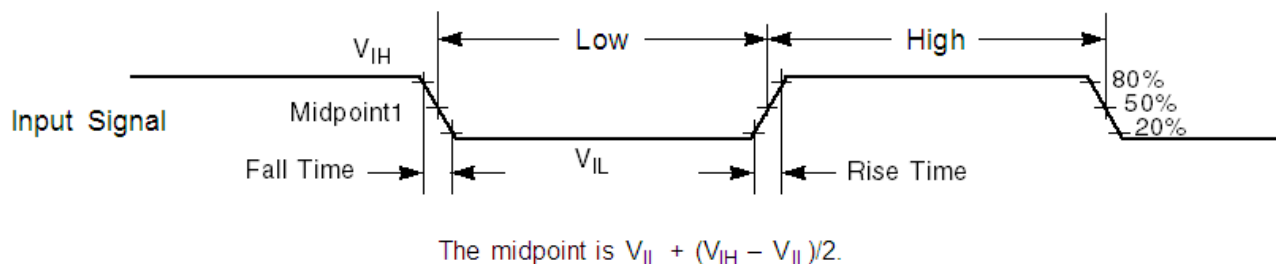
Symbol	Description	Min.	Max.	Unit
$I_{DD}$	Digital supply current	—	185	mA
$V_{DIO}$	Digital input voltage (except $\overline{RESET}$ , EXTAL, and XTAL)	-0.3	5.5	V
$V_{AIO}$	Analog <sup>1</sup> , $\overline{RESET}$ , EXTAL, and XTAL input voltage	-0.3	$V_{DD} + 0.3$	V
$I_D$	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
$V_{DDA}$	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V
$V_{USB\_DP}$	USB_DP input voltage	-0.3	3.63	V
$V_{USB\_DM}$	USB_DM input voltage	-0.3	3.63	V
VREGIN	USB regulator input	-0.3	6.0	V
$V_{BAT}$	RTC battery supply voltage	-0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

## 5 General

### 5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



**Figure 1. Input signal measurement reference**

All digital I/O switching characteristics assume:

1. output pins
  - have  $C_L=30\text{pF}$  loads,
  - are configured for fast slew rate ( $\text{PORTx\_PCRn[SRE]}=0$ ), and
  - are configured for high drive strength ( $\text{PORTx\_PCRn[DSE]}=1$ )
2. input pins
  - have their passive filter disabled ( $\text{PORTx\_PCRn[PFE]}=0$ )

### 5.2 Nonswitching electrical specifications

## 5.2.1 Voltage and current operating requirements

**Table 1. Voltage and current operating requirements**

Symbol	Description	Min.	Max.	Unit	Notes
$V_{DD}$	Supply voltage	1.71	3.6	V	
$V_{DDA}$	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	$V_{DD}$ -to- $V_{DDA}$ differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	$V_{SS}$ -to- $V_{SSA}$ differential voltage	-0.1	0.1	V	
$V_{BAT}$	RTC battery supply voltage	1.71	3.6	V	
$V_{IH}$	Input high voltage <ul style="list-style-type: none"> <li><math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math></li> <li><math>1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math></li> </ul>	$0.7 \times V_{DD}$ $0.75 \times V_{DD}$	— —	V V	
$V_{IL}$	Input low voltage <ul style="list-style-type: none"> <li><math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math></li> <li><math>1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math></li> </ul>	— —	$0.35 \times V_{DD}$ $0.3 \times V_{DD}$	V V	
$V_{HYS}$	Input hysteresis	$0.06 \times V_{DD}$	—	V	
$I_{CDIO}$	Digital pin negative DC injection current — single pin <ul style="list-style-type: none"> <li><math>V_{IN} &lt; V_{SS}-0.3\text{V}</math></li> </ul>	-5	—	mA	1
$I_{CAIO}$	Analog <sup>2</sup> , EXTAL, and XTAL pin DC injection current — single pin <ul style="list-style-type: none"> <li><math>V_{IN} &lt; V_{SS}-0.3\text{V}</math> (Negative current injection)</li> <li><math>V_{IN} &gt; V_{DD}+0.3\text{V}</math> (Positive current injection)</li> </ul>	-5 —	— +5	mA	3
$I_{Ccont}$	Contiguous pin DC injection current — regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins <ul style="list-style-type: none"> <li>Negative current injection</li> <li>Positive current injection</li> </ul>	-25 —	— +25	mA	
$V_{RAM}$	$V_{DD}$ voltage required to retain RAM	1.2	—	V	
$V_{RFVBAT}$	$V_{BAT}$ voltage required to retain the VBAT register file	$V_{POR\_VBAT}$	—	V	

- All 5 V tolerant digital I/O pins are internally clamped to  $V_{SS}$  through a ESD protection diode. There is no diode connection to  $V_{DD}$ . If  $V_{IN}$  greater than  $V_{DIO\_MIN}$  ( $=V_{SS}-0.3\text{V}$ ) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as  $R=(V_{DIO\_MIN}-V_{IN})/|I_{IC}|$ .
- Analog pins are defined as pins that do not have an associated general purpose I/O port function.
- All analog pins are internally clamped to  $V_{SS}$  and  $V_{DD}$  through ESD protection diodes. If  $V_{IN}$  is greater than  $V_{AIO\_MIN}$  ( $=V_{SS}-0.3\text{V}$ ) and  $V_{IN}$  is less than  $V_{AIO\_MAX}$  ( $=V_{DD}+0.3\text{V}$ ) is observed, then there is no need to provide current limiting resistors at the pads. If these limits cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as  $R=(V_{AIO\_MIN}-V_{IN})/|I_{IC}|$ . The positive injection current limiting resistor is calculated as  $R=(V_{IN}-V_{AIO\_MAX})/|I_{IC}|$ . Select the larger of these two calculated resistances.

## 5.2.2 LVD and POR operating requirements

**Table 2. V<sub>DD</sub> supply LVD and POR operating requirements**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>POR</sub>	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V <sub>LVDH</sub>	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
V <sub>LVW1H</sub>	Low-voltage warning thresholds — high range					1
	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V <sub>LVW2H</sub>	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V <sub>LVW3H</sub>	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V <sub>LVW4H</sub>	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V <sub>HYSH</sub>	Low-voltage inhibit reset/recover hysteresis — high range	—	±80	—	mV	
V <sub>LVDL</sub>	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
V <sub>LVW1L</sub>	Low-voltage warning thresholds — low range					1
	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V <sub>LVW2L</sub>	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V <sub>LVW3L</sub>	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V <sub>LVW4L</sub>	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V <sub>HYSL</sub>	Low-voltage inhibit reset/recover hysteresis — low range	—	±60	—	mV	
V <sub>BG</sub>	Bandgap voltage reference	0.97	1.00	1.03	V	
t <sub>LPO</sub>	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

1. Rising thresholds are falling threshold + hysteresis voltage

**Table 3. VBAT power operating requirements**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>POR_VBAT</sub>	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

### 5.2.3 Voltage and current operating behaviors

**Table 4. Voltage and current operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes	
V <sub>OH</sub>	Output high voltage — high drive strength					
	• 2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, I <sub>OH</sub> = -9mA	V <sub>DD</sub> - 0.5	—	V		
	• 1.71 V ≤ V <sub>DD</sub> ≤ 2.7 V, I <sub>OH</sub> = -3mA	V <sub>DD</sub> - 0.5	—	V		
	Output high voltage — low drive strength					
I <sub>OHT</sub>	Output high current total for all ports	—	100	mA		
	V <sub>OL</sub>	Output low voltage — high drive strength				
		• 2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, I <sub>OL</sub> = 9mA	—	0.5	V	
	• 1.71 V ≤ V <sub>DD</sub> ≤ 2.7 V, I <sub>OL</sub> = 3mA	—	0.5	V		
Output low voltage — low drive strength						
I <sub>OLT</sub>	• 2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, I <sub>OL</sub> = 2mA	—	0.5	V		
	• 1.71 V ≤ V <sub>DD</sub> ≤ 2.7 V, I <sub>OL</sub> = 0.6mA	—	0.5	V		
I <sub>IN</sub>	Input leakage current (per pin) for full temperature range except TRI0_DM, TRI0_DP, TRI1_DM, TRI1_DP	—	1	μA	1	
I <sub>IN</sub>	Input leakage current (per pin) at 25°C except TRI0_DM, TRI0_DP, TRI1_DM, TRI1_DP	—	0.025	μA	1	
I <sub>ILKG_A</sub>	Input leakage current (per pin) for TRI0_DM, TRI0_DP, TRI1_DM, TRI1_DP	—	5	nA	1	
I <sub>OZ</sub>	Hi-Z (off-state) leakage current (per pin)	—	1	μA		
R <sub>PU</sub>	Internal pullup resistors	20	50	kΩ	2	
R <sub>PD</sub>	Internal pulldown resistors	20	50	kΩ	3	

1. Measured at V<sub>DD</sub>=3.6V
2. Measured at V<sub>DD</sub> supply voltage = V<sub>DD</sub> min and V<sub>input</sub> = V<sub>SS</sub>
3. Measured at V<sub>DD</sub> supply voltage = V<sub>DD</sub> min and V<sub>input</sub> = V<sub>DD</sub>

### 5.2.4 Power mode transition operating behaviors

All specifications except t<sub>POR</sub>, and V<sub>L</sub>L<sub>S</sub>x→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 72 MHz
- Bus clock = 36 MHz
- Flash clock = 24 MHz

**Table 5. Power mode transition operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes
$t_{POR}$	After a POR event, amount of time from the point $V_{DD}$ reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	300	$\mu s$	1
	• VLLS1 → RUN	—	112	$\mu s$	
	• VLLS2 → RUN	—	74	$\mu s$	
	• VLLS3 → RUN	—	73	$\mu s$	
	• LLS → RUN	—	5.9	$\mu s$	
	• VLPS → RUN	—	5.8	$\mu s$	
	• STOP → RUN	—	4.2	$\mu s$	

1. Normal boot (FTFL\_OPT[LPBOOT]=1)

## 5.2.5 Power consumption operating behaviors

**Table 6. Power consumption operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$I_{DDA}$	Analog supply current	—	—	See note	mA	1
$I_{DD\_RUN}$	Run mode current — all peripheral clocks disabled, code executing from flash					2
	• @ 1.8V	—	21.5	25	mA	
	• @ 3.0V	—	21.5	30	mA	
$I_{DD\_RUN}$	Run mode current — all peripheral clocks enabled, code executing from flash					3, 4
	• @ 1.8V	—	31	34	mA	
	• @ 3.0V					
	• @ 25°C	—	31	34	mA	
	• @ 125°C	—	32	39	mA	
$I_{DD\_WAIT}$	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	12.5	—	mA	2
$I_{DD\_WAIT}$	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	7.2	—	mA	5
$I_{DD\_VLPR}$	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	0.996	—	mA	6
$I_{DD\_VLPR}$	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.46	—	mA	7

Table continues on the next page...

**Table 6. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>DD_VLPW</sub>	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	0.61	—	mA	8
I <sub>DD_STOP</sub>	Stop mode current at 3.0 V					
	• @ -40 to 25°C	—	0.35	0.567	mA	
	• @ 70°C	—	0.384	0.793	mA	
	• @ 105°C	—	0.628	1.2	mA	
I <sub>DD_VLPS</sub>	Very-low-power stop mode current at 3.0 V					
	• @ -40 to 25°C	—	5.9	32.7	μA	
	• @ 70°C	—	26.1	59.8	μA	
	• @ 105°C	—	98.1	188	μA	
I <sub>DD_LLS</sub>	Low leakage stop mode current at 3.0 V					9
	• @ -40 to 25°C	—	2.6	8.6	μA	
	• @ 70°C	—	10.3	29.1	μA	
	• @ 105°C	—	42.5	92.5	μA	
I <sub>DD_VLLS3</sub>	Very low-leakage stop mode 3 current at 3.0 V					9
	• @ -40 to 25°C	—	1.9	5.8	μA	
	• @ 70°C	—	6.9	12.1	μA	
	• @ 105°C	—	28.1	41.9	μA	
I <sub>DD_VLLS2</sub>	Very low-leakage stop mode 2 current at 3.0 V					
	• @ -40 to 25°C	—	1.59	5.5	μA	
	• @ 70°C	—	4.3	9.5	μA	
	• @ 105°C	—	17.5	34	μA	
I <sub>DD_VLLS1</sub>	Very low-leakage stop mode 1 current at 3.0 V					
	• @ -40 to 25°C	—	1.47	5.4	μA	
	• @ 70°C	—	2.97	8.1	μA	
	• @ 105°C	—	12.41	32	μA	
I <sub>DD_VBAT</sub>	Average current with RTC and 32kHz disabled at 3.0 V					
	• @ -40 to 25°C	—	0.19	0.22	μA	
	• @ 70°C	—	0.49	0.64	μA	
	• @ 105°C	—	2.2	3.2	μA	

Table continues on the next page...



**Table 6. Power consumption operating behaviors (continued)**

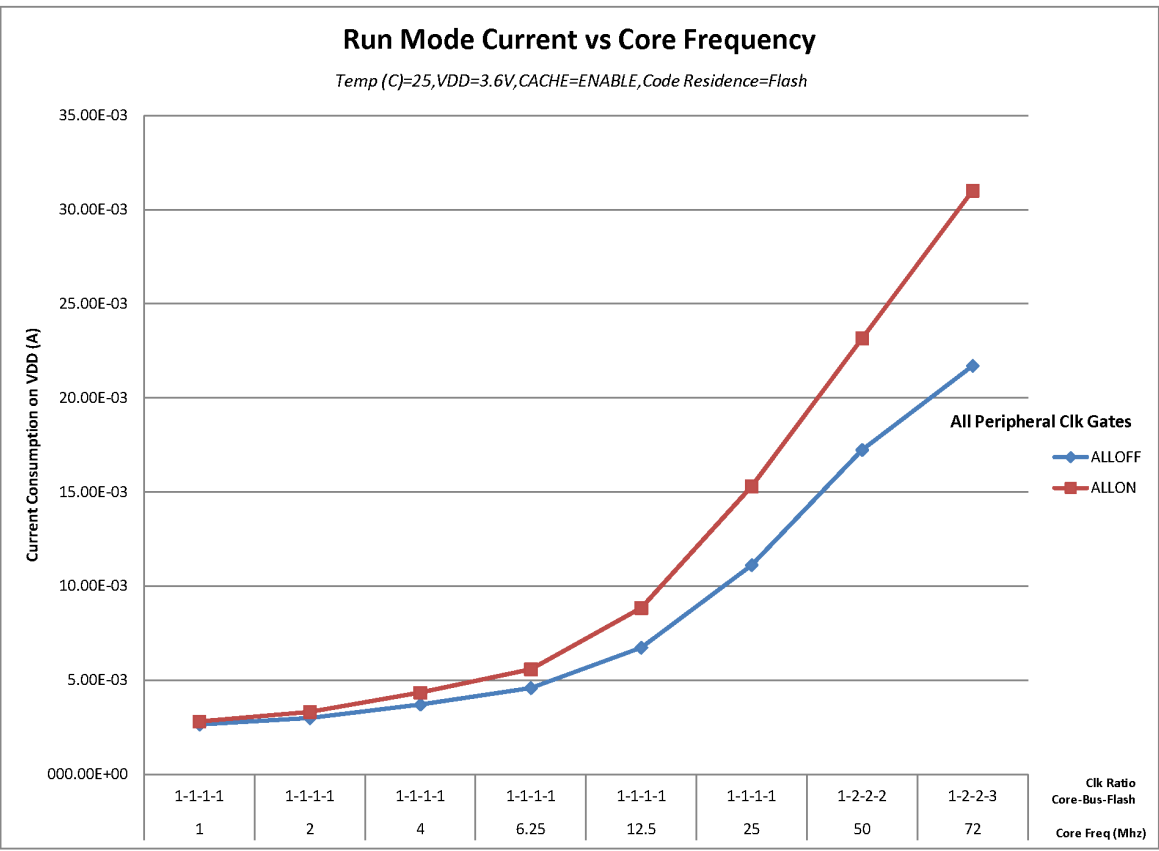
Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>DD_VBAT</sub>	Average current when CPU is not accessing RTC registers					10
	• @ 1.8V					
	• @ -40 to 25°C	—	0.57	0.67	μA	
	• @ 70°C	—	0.90	1.2	μA	
	• @ 105°C	—	2.4	3.5	μA	
	• @ 3.0V					
	• @ -40 to 25°C	—	0.67	0.94	μA	
	• @ 70°C	—	1.0	1.4	μA	
	• @ 105°C	—	2.7	3.9	μA	

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 72MHz core and system clock, 36MHz bus clock, and 24MHz flash clock. MCG configured for FEE mode. All peripheral clocks disabled.
3. 72MHz core and system clock, 36MHz bus clock, and 24MHz flash clock. MCG configured for FEE mode. All peripheral clocks enabled.
4. Max values are measured with CPU executing DSP instructions.
5. 25MHz core, system, bus and flash clock. MCG configured for FEI mode.
6. 4 MHz core and system clock, 4 MHz and bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
7. 4 MHz core and system clock, 4 MHz and bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
8. 4 MHz core and system clock, 4 MHz and bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
9. Data reflects devices with 128 KB of RAM. For devices with 64 KB of RAM, power consumption is reduced by 2 μA.
10. Includes 32kHz oscillator current and RTC operation.

### 5.2.5.1 Diagram: Typical I<sub>DD\_RUN</sub> operating behavior

The following data was measured under these conditions:

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at greater than 50 MHz frequencies.
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL



**Figure 2. Run mode supply current vs. core frequency**

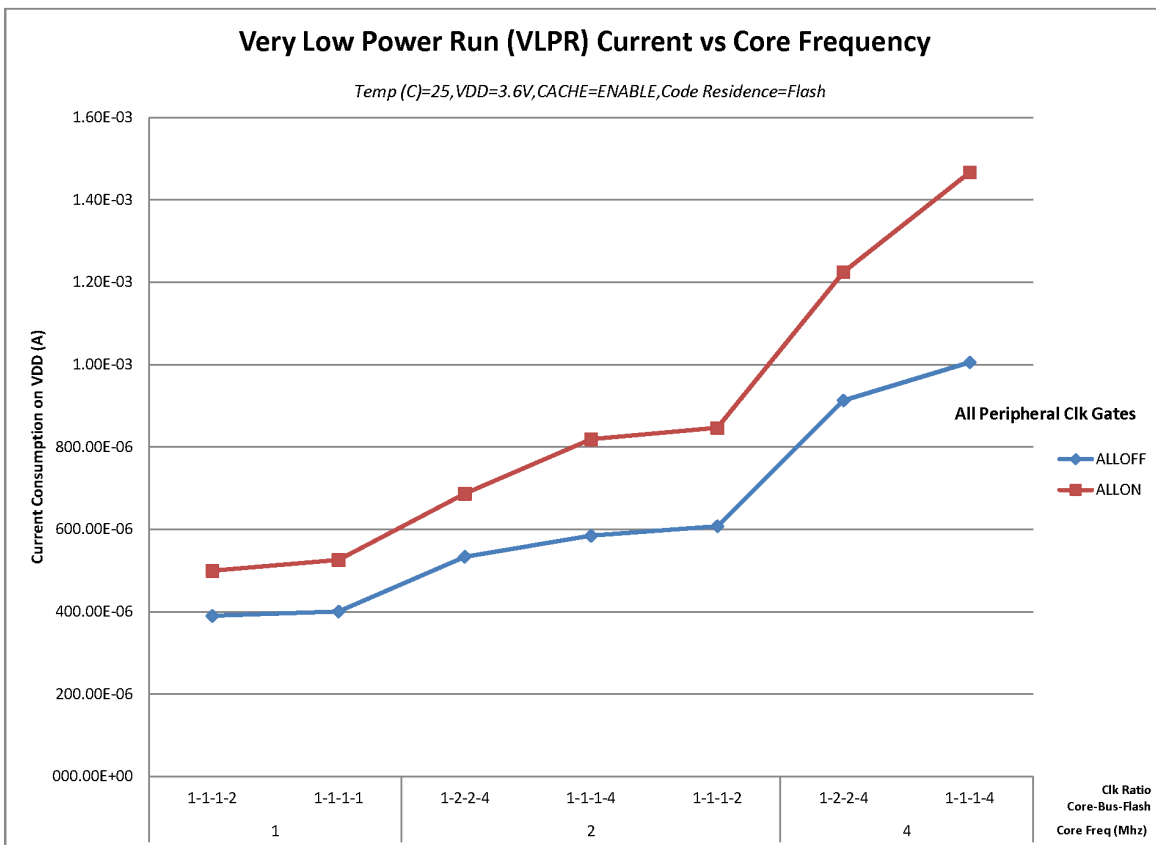


Figure 3. VLPR mode supply current vs. core frequency

### 5.2.6 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to [www.freescale.com](http://www.freescale.com).
2. Perform a keyword search for “EMC design.”

### 5.2.7 Capacitance attributes

Table 7. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C <sub>IN_A</sub>	Input capacitance: analog pins	—	7	pF
C <sub>IN_D</sub>	Input capacitance: digital pins	—	7	pF

## 5.3 Switching specifications

### 5.3.1 Device clock specifications

**Table 8. Device clock specifications**

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f <sub>SYS</sub>	System and core clock	—	72	MHz	
f <sub>SYS_USB</sub>	System and core clock when Full Speed USB in operation	20	—	MHz	
f <sub>BUS</sub>	Bus clock	—	50	MHz	
f <sub>FLASH</sub>	Flash clock	—	25	MHz	
f <sub>LPTMR</sub>	LPTMR clock	—	25	MHz	
VLPR mode <sup>1</sup>					
f <sub>SYS</sub>	System and core clock	—	4	MHz	
f <sub>BUS</sub>	Bus clock	—	4	MHz	
f <sub>FLASH</sub>	Flash clock	—	0.5	MHz	
f <sub>ERCLK</sub>	External reference clock	—	16	MHz	
f <sub>LPTMR_pin</sub>	LPTMR clock	—	25	MHz	
f <sub>LPTMR_ERCLK</sub>	LPTMR external reference clock	—	16	MHz	
f <sub>FlexCAN_ERCLK</sub>	FlexCAN external reference clock	—	8	MHz	
f <sub>I2S_MCLK</sub>	I2S master clock	—	12.5	MHz	
f <sub>I2S_BCLK</sub>	I2S bit clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

### 5.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, CMT, and I<sup>2</sup>C signals.

**Table 9. General switching specifications**

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	3

*Table continues on the next page...*

**Table 9. General switching specifications (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	16	—	ns	3
	External reset pulse width (digital glitch filter disabled)	100	—	ns	3
	Mode select (EZP_CS) hold time after reset deassertion	2	—	Bus clock cycles	
	Port rise and fall time (high drive strength) <ul style="list-style-type: none"> <li>• Slew disabled                             <ul style="list-style-type: none"> <li>• <math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li>• <math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> <li>• Slew enabled                             <ul style="list-style-type: none"> <li>• <math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li>• <math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> </ul>	— — — —	12 6 36 24	ns ns ns ns	4
	Port rise and fall time (low drive strength) <ul style="list-style-type: none"> <li>• Slew disabled                             <ul style="list-style-type: none"> <li>• <math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li>• <math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> <li>• Slew enabled                             <ul style="list-style-type: none"> <li>• <math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li>• <math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> </ul>	— — — —	12 6 36 24	ns ns ns ns	5

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75pF load
5. 15pF load

## 5.4 Thermal specifications

### 5.4.1 Thermal operating requirements

**Table 10. Thermal operating requirements**

Symbol	Description	Min.	Max.	Unit
$T_J$	Die junction temperature	-40	125	°C
$T_A$	Ambient temperature	-40	85	°C

## 5.4.2 Thermal attributes

Board type	Symbol	Description	121 MAPBGA	100 LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	74	52	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	42	40	°C/W	1, 3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	62	42	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	38	34	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	23	25	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	19	12	°C/W	5
—	$\Psi_{JT}$	Thermal characterization parameter, junction to package top outside center (natural convection)	4	2	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. For the LQFP, the board meets the JESD51-3 specification. For the MAPBGA, the board meets the JESD51-9 specification.
3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuits Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal. For the LQFP, the board meets the JESD51-7 specification.
4. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.

5. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
6. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

## 6 Peripheral operating requirements and behaviors

### 6.1 Core modules

#### 6.1.1 Debug trace timing specifications

Table 11. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
$T_{cyc}$	Clock period	Frequency dependent		MHz
$T_{wl}$	Low pulse width	2	—	ns
$T_{wh}$	High pulse width	2	—	ns
$T_r$	Clock and data rise time	—	3	ns
$T_f$	Clock and data fall time	—	3	ns
$T_s$	Data setup	3	—	ns
$T_h$	Data hold	2	—	ns

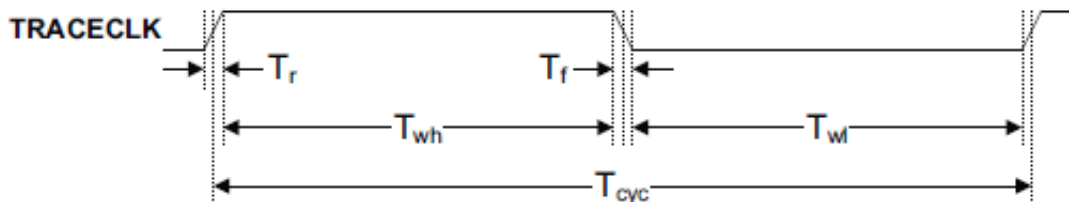


Figure 4. TRACE\_CLKOUT specifications

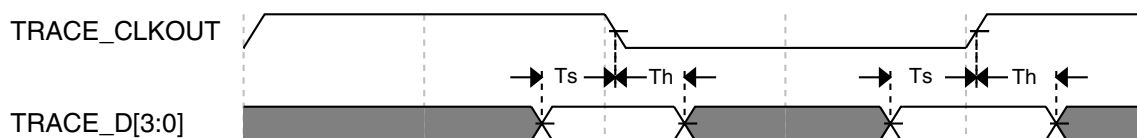


Figure 5. Trace data specifications

## 6.1.2 JTAG electricals

**Table 12. JTAG limited voltage range electricals**

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation <ul style="list-style-type: none"> <li>• Boundary Scan</li> <li>• JTAG and CJTAG</li> <li>• Serial Wire Debug</li> </ul>	0 0 0	10 25 50	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width <ul style="list-style-type: none"> <li>• Boundary Scan</li> <li>• JTAG and CJTAG</li> <li>• Serial Wire Debug</li> </ul>	50 20 10	— — —	ns ns ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	17	ns
J12	TCLK low to TDO high-Z	—	17	ns
J13	TRST assert time	100	—	ns
J14	TRST setup time (negation) to TCLK high	8	—	ns

**Table 13. JTAG full voltage range electricals**

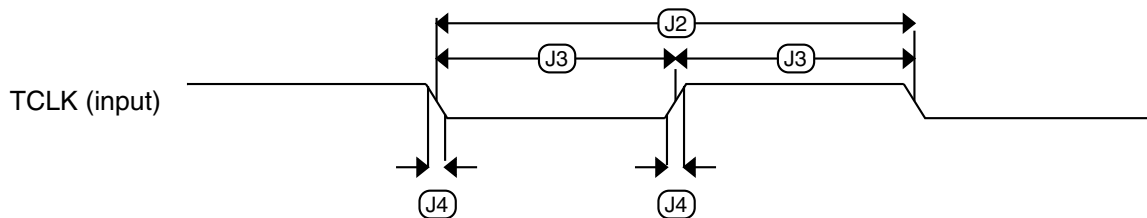
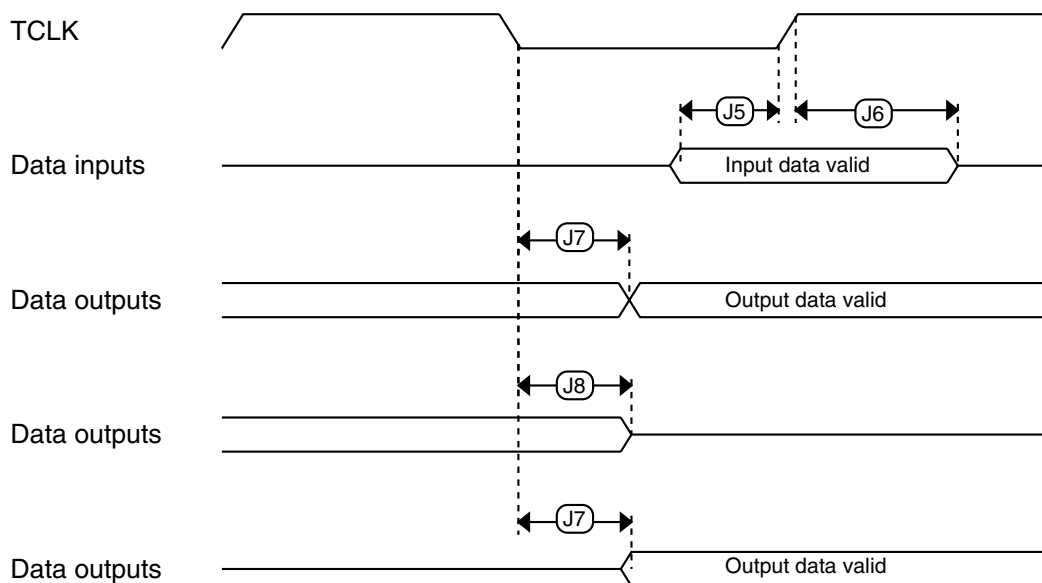
Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation <ul style="list-style-type: none"> <li>• Boundary Scan</li> <li>• JTAG and CJTAG</li> <li>• Serial Wire Debug</li> </ul>	0 0 0	10 20 40	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width <ul style="list-style-type: none"> <li>• Boundary Scan</li> <li>• JTAG and CJTAG</li> <li>• Serial Wire Debug</li> </ul>	50 25 12.5	— — —	ns ns ns
J4	TCLK rise and fall times	—	3	ns

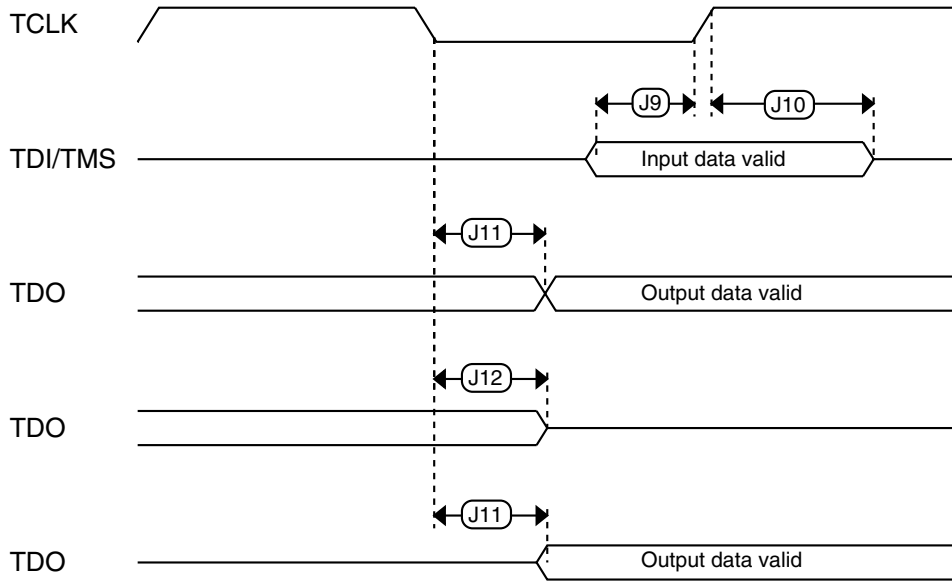
Table continues on the next page...



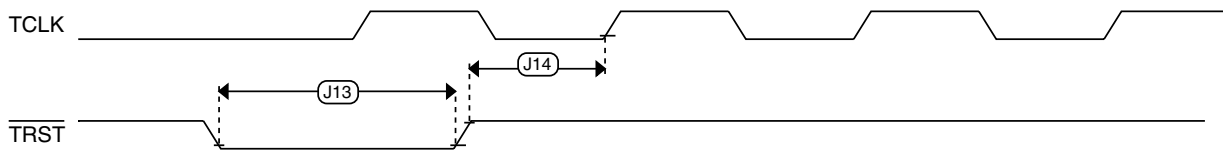
**Table 13. JTAG full voltage range electricals (continued)**

Symbol	Description	Min.	Max.	Unit
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	—	22.1	ns
J12	TCLK low to TDO high-Z	—	22.1	ns
J13	TRST assert time	100	—	ns
J14	TRST setup time (negation) to TCLK high	8	—	ns


**Figure 6. Test clock input timing**

**Figure 7. Boundary scan (JTAG) timing**



**Figure 8. Test Access Port timing**



**Figure 9.  $\overline{\text{TRST}}$  timing**

## 6.2 System modules

There are no specifications necessary for the device's system modules.

## 6.3 Clock modules

### 6.3.1 MCG specifications

**Table 14. MCG specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes	
$f_{ints\_ft}$	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz		
$f_{ints\_t}$	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz		
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	$\pm 0.3$	$\pm 0.6$	% $f_{dco}$	1	
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only	—	$\pm 0.2$	$\pm 0.5$	% $f_{dco}$	1	
$\Delta f_{dco\_t}$	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	+0.5/-0.7	—	% $f_{dco}$	1	
$\Delta f_{dco\_t}$	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—	$\pm 0.3$	$\pm 0.3$	% $f_{dco}$	1	
$f_{intf\_ft}$	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C	—	4	—	MHz		
$f_{intf\_t}$	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	—	5	MHz		
$f_{loc\_low}$	Loss of external clock minimum frequency — RANGE = 00	$(3/5) \times f_{ints\_t}$	—	—	kHz		
$f_{loc\_high}$	Loss of external clock minimum frequency — RANGE = 01, 10, or 11	$(16/5) \times f_{ints\_t}$	—	—	kHz		
FLL							
$f_{fill\_ref}$	FLL reference frequency range	31.25	—	39.0625	kHz		
$f_{dco}$	DCO output frequency range	Low range (DRS=00) $640 \times f_{fill\_ref}$	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) $1280 \times f_{fill\_ref}$	40	41.94	50	MHz	
		Mid-high range (DRS=10) $1920 \times f_{fill\_ref}$	60	62.91	75	MHz	
		High range (DRS=11) $2560 \times f_{fill\_ref}$	80	83.89	100	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS=00) $732 \times f_{fill\_ref}$	—	23.99	—	MHz	4, 5
		Mid range (DRS=01) $1464 \times f_{fill\_ref}$	—	47.97	—	MHz	
		Mid-high range (DRS=10) $2197 \times f_{fill\_ref}$	—	71.99	—	MHz	
		High range (DRS=11) $2929 \times f_{fill\_ref}$	—	95.98	—	MHz	

Table continues on the next page...

**Table 14. MCG specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$J_{cyc\_fll}$	FLL period jitter <ul style="list-style-type: none"> <li><math>f_{VCO} = 48</math> MHz</li> <li><math>f_{VCO} = 98</math> MHz</li> </ul>	—	180	—	ps	
		—	150	—		
$t_{fll\_acquire}$	FLL target frequency acquisition time	—	—	1	ms	6
PLL						
$f_{vco}$	VCO operating frequency	48.0	—	100	MHz	
$I_{pll}$	PLL operating current <ul style="list-style-type: none"> <li>PLL @ 96 MHz (<math>f_{osc\_hi\_1} = 8</math> MHz, <math>f_{pll\_ref} = 2</math> MHz, VDIV multiplier = 48)</li> </ul>	—	1060	—	$\mu$ A	7
		—	600	—	$\mu$ A	7
$f_{pll\_ref}$	PLL reference frequency range	2.0	—	4.0	MHz	
$J_{cyc\_pll}$	PLL period jitter (RMS) <ul style="list-style-type: none"> <li><math>f_{vco} = 48</math> MHz</li> <li><math>f_{vco} = 100</math> MHz</li> </ul>	—	120	—	ps	8
		—	50	—	ps	
$J_{acc\_pll}$	PLL accumulated jitter over 1 $\mu$ s (RMS) <ul style="list-style-type: none"> <li><math>f_{vco} = 48</math> MHz</li> <li><math>f_{vco} = 100</math> MHz</li> </ul>	—	1350	—	ps	8
		—	600	—	ps	
$D_{lock}$	Lock entry frequency tolerance	$\pm 1.49$	—	$\pm 2.98$	%	
$D_{unl}$	Lock exit frequency tolerance	$\pm 4.47$	—	$\pm 5.97$	%	
$t_{pll\_lock}$	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll\_ref})$	s	9

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation ( $\Delta f_{dco\_t}$ ) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
9. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

### 6.3.2 Oscillator electrical specifications

This section provides the electrical characteristics of the module.

### 6.3.2.1 Oscillator DC electrical specifications

**Table 15. Oscillator DC electrical specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{DD}$	Supply voltage	1.71	—	3.6	V	
$I_{DDOSC}$	Supply current — low-power mode (HGO=0) <ul style="list-style-type: none"> <li>• 32 kHz</li> <li>• 4 MHz</li> <li>• 8 MHz (RANGE=01)</li> <li>• 16 MHz</li> <li>• 24 MHz</li> <li>• 32 MHz</li> </ul>	—	500	—	nA	1
		—	200	—	$\mu$ A	
		—	300	—	$\mu$ A	
		—	950	—	$\mu$ A	
		—	1.2	—	mA	
		—	1.5	—	mA	
$I_{DDOSC}$	Supply current — high gain mode (HGO=1) <ul style="list-style-type: none"> <li>• 32 kHz</li> <li>• 4 MHz</li> <li>• 8 MHz (RANGE=01)</li> <li>• 16 MHz</li> <li>• 24 MHz</li> <li>• 32 MHz</li> </ul>	—	25	—	$\mu$ A	1
		—	400	—	$\mu$ A	
		—	500	—	$\mu$ A	
		—	2.5	—	mA	
		—	3	—	mA	
		—	4	—	mA	
$C_x$	EXTAL load capacitance	—	—	—		2, 3
$C_y$	XTAL load capacitance	—	—	—		2, 3
$R_F$	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	M $\Omega$	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	M $\Omega$	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	M $\Omega$	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	M $\Omega$	
$R_S$	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	k $\Omega$	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	k $\Omega$	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	k $\Omega$	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	k $\Omega$	

Table continues on the next page...

**Table 15. Oscillator DC electrical specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{pp}^5$	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	$V_{DD}$	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	$V_{DD}$	—	V	

1.  $V_{DD}=3.3$  V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3.  $C_x, C_y$  can be provided by using either the integrated capacitors or by using external components.
4. When low power mode is selected,  $R_F$  is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

### 6.3.2.2 Oscillator frequency specifications

**Table 16. Oscillator frequency specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{osc\_lo}$	Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
$f_{ec\_extal}$	Input clock frequency (external clock mode)	—	—	50	MHz	1, 2
$t_{dc\_extal}$	Input clock duty cycle (external clock mode)	40	50	60	%	
$t_{cst}$	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.

- Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG\_S register being set.

### NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

## 6.3.3 32 kHz Oscillator Electrical Characteristics

This section describes the module electrical characteristics.

### 6.3.3.1 32 kHz oscillator DC electrical specifications

Table 17. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
$V_{BAT}$	Supply voltage	1.71	—	3.6	V
$R_F$	Internal feedback resistor	—	100	—	$M\Omega$
$C_{para}$	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
$V_{pp}$ <sup>1</sup>	Peak-to-peak amplitude of oscillation	—	0.6	—	V

- When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

### 6.3.3.2 32kHz oscillator frequency specifications

Table 18. 32kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{osc\_lo}$	Oscillator crystal	—	32.768	—	kHz	
$t_{start}$	Crystal start-up time	—	1000	—	ms	1
$V_{ec\_extal32}$	Externally provided input clock amplitude	700	—	$V_{BAT}$	mV	2, 3

- Proper PC board layout procedures must be followed to achieve specifications.
- This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
- The parameter specified is a peak-to-peak value and  $V_{IH}$  and  $V_{IL}$  specifications do not apply. The voltage of the applied clock must be within the range of  $V_{SS}$  to  $V_{BAT}$ .

## 6.4 Memories and memory interfaces

### 6.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

### 6.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

**Table 19. NVM program/erase timing specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hvp\text{gm}4}$	Longword Program high-voltage time	—	7.5	18	$\mu\text{s}$	
$t_{h\text{versscr}}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{h\text{versblk}32\text{k}}$	Erase Block high-voltage time for 32 KB	—	52	452	ms	1
$t_{h\text{versblk}256\text{k}}$	Erase Block high-voltage time for 256 KB	—	104	904	ms	1

1. Maximum time based on expectations at cycling end-of-life.

### 6.4.1.2 Flash timing specifications — commands

**Table 20. Flash command timing specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1\text{blk}32\text{k}}$	Read 1s Block execution time					
	<ul style="list-style-type: none"> <li>32 KB data flash</li> </ul>	—	—	0.5	ms	
$t_{rd1\text{blk}256\text{k}}$	<ul style="list-style-type: none"> <li>256 KB program flash</li> </ul>	—	—	1.7	ms	
$t_{rd1\text{sec}1\text{k}}$	Read 1s Section execution time (data flash sector)	—	—	60	$\mu\text{s}$	1
$t_{rd1\text{sec}2\text{k}}$	Read 1s Section execution time (program flash sector)	—	—	60	$\mu\text{s}$	1
$t_{pgm\text{chk}}$	Program Check execution time	—	—	45	$\mu\text{s}$	1
$t_{rd\text{rsrc}}$	Read Resource execution time	—	—	30	$\mu\text{s}$	1
$t_{pgm4}$	Program Longword execution time	—	65	145	$\mu\text{s}$	
$t_{ers\text{blk}32\text{k}}$	Erase Flash Block execution time					2
	<ul style="list-style-type: none"> <li>32 KB data flash</li> </ul>	—	55	465	ms	
$t_{ers\text{blk}256\text{k}}$	<ul style="list-style-type: none"> <li>256 KB program flash</li> </ul>	—	122	985	ms	
$t_{ers\text{scr}}$	Erase Flash Sector execution time	—	14	114	ms	2
$t_{pgm\text{sec}512\text{p}}$	Program Section execution time					
	<ul style="list-style-type: none"> <li>512 B program flash</li> </ul>	—	2.4	—	ms	
$t_{pgm\text{sec}512\text{d}}$	<ul style="list-style-type: none"> <li>512 B data flash</li> </ul>	—	4.7	—	ms	
$t_{pgm\text{sec}1\text{kp}}$	<ul style="list-style-type: none"> <li>1 KB program flash</li> </ul>	—	4.7	—	ms	
$t_{pgm\text{sec}1\text{kd}}$	<ul style="list-style-type: none"> <li>1 KB data flash</li> </ul>	—	9.3	—	ms	
$t_{rd1\text{all}}$	Read 1s All Blocks execution time	—	—	1.8	ms	
$t_{rd\text{once}}$	Read Once execution time	—	—	25	$\mu\text{s}$	1
$t_{pgm\text{once}}$	Program Once execution time	—	65	—	$\mu\text{s}$	
$t_{ers\text{all}}$	Erase All Blocks execution time	—	175	1500	ms	2

Table continues on the next page...



**Table 20. Flash command timing specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{\text{vfykey}}$	Verify Backdoor Access Key execution time	—	—	30	$\mu\text{s}$	1
$t_{\text{swapx01}}$	Swap Control execution time	—	200	—	$\mu\text{s}$	
$t_{\text{swapx02}}$	• control code 0x02	—	70	150	$\mu\text{s}$	
$t_{\text{swapx04}}$	• control code 0x04	—	70	150	$\mu\text{s}$	
$t_{\text{swapx08}}$	• control code 0x08	—	—	30	$\mu\text{s}$	
$t_{\text{pgmpart32k}}$	Program Partition for EEPROM execution time	—	70	—	ms	
$t_{\text{setramff}}$	Set FlexRAM Function execution time:	—	50	—	$\mu\text{s}$	
$t_{\text{setram8k}}$	• Control Code 0xFF	—	0.3	0.5	ms	
$t_{\text{setram32k}}$	• 8 KB EEPROM backup	—	0.7	1.0	ms	
	• 32 KB EEPROM backup	—				
Byte-write to FlexRAM for EEPROM operation						
$t_{\text{eewr8bers}}$	Byte-write to erased FlexRAM location execution time	—	175	260	$\mu\text{s}$	3
$t_{\text{eewr8b8k}}$	Byte-write to FlexRAM execution time:	—	340	1700	$\mu\text{s}$	
$t_{\text{eewr8b16k}}$	• 8 KB EEPROM backup	—	385	1800	$\mu\text{s}$	
$t_{\text{eewr8b32k}}$	• 16 KB EEPROM backup	—	475	2000	$\mu\text{s}$	
	• 32 KB EEPROM backup	—				
Word-write to FlexRAM for EEPROM operation						
$t_{\text{eewr16bers}}$	Word-write to erased FlexRAM location execution time	—	175	260	$\mu\text{s}$	
$t_{\text{eewr16b8k}}$	Word-write to FlexRAM execution time:	—	340	1700	$\mu\text{s}$	
$t_{\text{eewr16b16k}}$	• 8 KB EEPROM backup	—	385	1800	$\mu\text{s}$	
$t_{\text{eewr16b32k}}$	• 16 KB EEPROM backup	—	475	2000	$\mu\text{s}$	
	• 32 KB EEPROM backup	—				
Longword-write to FlexRAM for EEPROM operation						
$t_{\text{eewr32bers}}$	Longword-write to erased FlexRAM location execution time	—	360	540	$\mu\text{s}$	
$t_{\text{eewr32b8k}}$	Longword-write to FlexRAM execution time:	—	545	1950	$\mu\text{s}$	
$t_{\text{eewr32b16k}}$	• 8 KB EEPROM backup	—	630	2050	$\mu\text{s}$	
$t_{\text{eewr32b32k}}$	• 16 KB EEPROM backup	—	810	2250	$\mu\text{s}$	
	• 32 KB EEPROM backup	—				

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

### 6.4.1.3 Flash high voltage current behaviors

Table 21. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I <sub>DD_PGM</sub>	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I <sub>DD_ERS</sub>	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

### 6.4.1.4 Reliability specifications

Table 22. NVM reliability specifications

Symbol	Description	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
Program Flash						
t <sub>nvmretp10k</sub>	Data retention after up to 10 K cycles	5	50	—	years	
t <sub>nvmretp1k</sub>	Data retention after up to 1 K cycles	20	100	—	years	
n <sub>nvmcycp</sub>	Cycling endurance	10 K	50 K	—	cycles	2
Data Flash						
t <sub>nvmretd10k</sub>	Data retention after up to 10 K cycles	5	50	—	years	
t <sub>nvmretd1k</sub>	Data retention after up to 1 K cycles	20	100	—	years	
n <sub>nvmcygd</sub>	Cycling endurance	10 K	50 K	—	cycles	2
FlexRAM as EEPROM						
t <sub>nvmretee100</sub>	Data retention up to 100% of write endurance	5	50	—	years	
t <sub>nvmretee10</sub>	Data retention up to 10% of write endurance	20	100	—	years	
n <sub>nvmwree16</sub>	Write endurance					3
n <sub>nvmwree128</sub>	• EEPROM backup to FlexRAM ratio = 16	35 K	175 K	—	writes	
n <sub>nvmwree512</sub>	• EEPROM backup to FlexRAM ratio = 128	315 K	1.6 M	—	writes	
n <sub>nvmwree4k</sub>	• EEPROM backup to FlexRAM ratio = 512	1.27 M	6.4 M	—	writes	
n <sub>nvmwree4k</sub>	• EEPROM backup to FlexRAM ratio = 4096	10 M	50 M	—	writes	
n <sub>nvmwree8k</sub>	• EEPROM backup to FlexRAM ratio = 8192	20 M	100 M	—	writes	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40°C ≤ T<sub>j</sub> ≤ 125°C.
3. Write endurance represents the number of writes to each FlexRAM location at -40°C ≤ T<sub>j</sub> ≤ 125°C influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup per subsystem. Minimum and typical values assume all byte-writes to FlexRAM.

### 6.4.1.5 Write endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

The bytes not assigned to data flash via the FlexNVM partition code are used by the flash memory module to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

$$\text{Writes\_subsystem} = \frac{\text{EEPROM} - 2 \times \text{EESPLIT} \times \text{EESIZE}}{\text{EESPLIT} \times \text{EESIZE}} \times \text{Write\_efficiency} \times n_{\text{nvmcyed}}$$

where

- Writes\_subsystem — minimum number of writes to each FlexRAM location for subsystem (each subsystem can have different endurance)
- EEPROM — allocated FlexNVM for each EEPROM subsystem based on DEPART; entered with the Program Partition command
- EESPLIT — FlexRAM split factor for subsystem; entered with the Program Partition command
- EESIZE — allocated FlexRAM based on DEPART; entered with the Program Partition command
- Write\_efficiency —
  - 0.25 for 8-bit writes to FlexRAM
  - 0.50 for 16-bit or 32-bit writes to FlexRAM
- $n_{\text{nvmcyed}}$  — data flash cycling endurance (the following graph assumes 10,000 cycles)

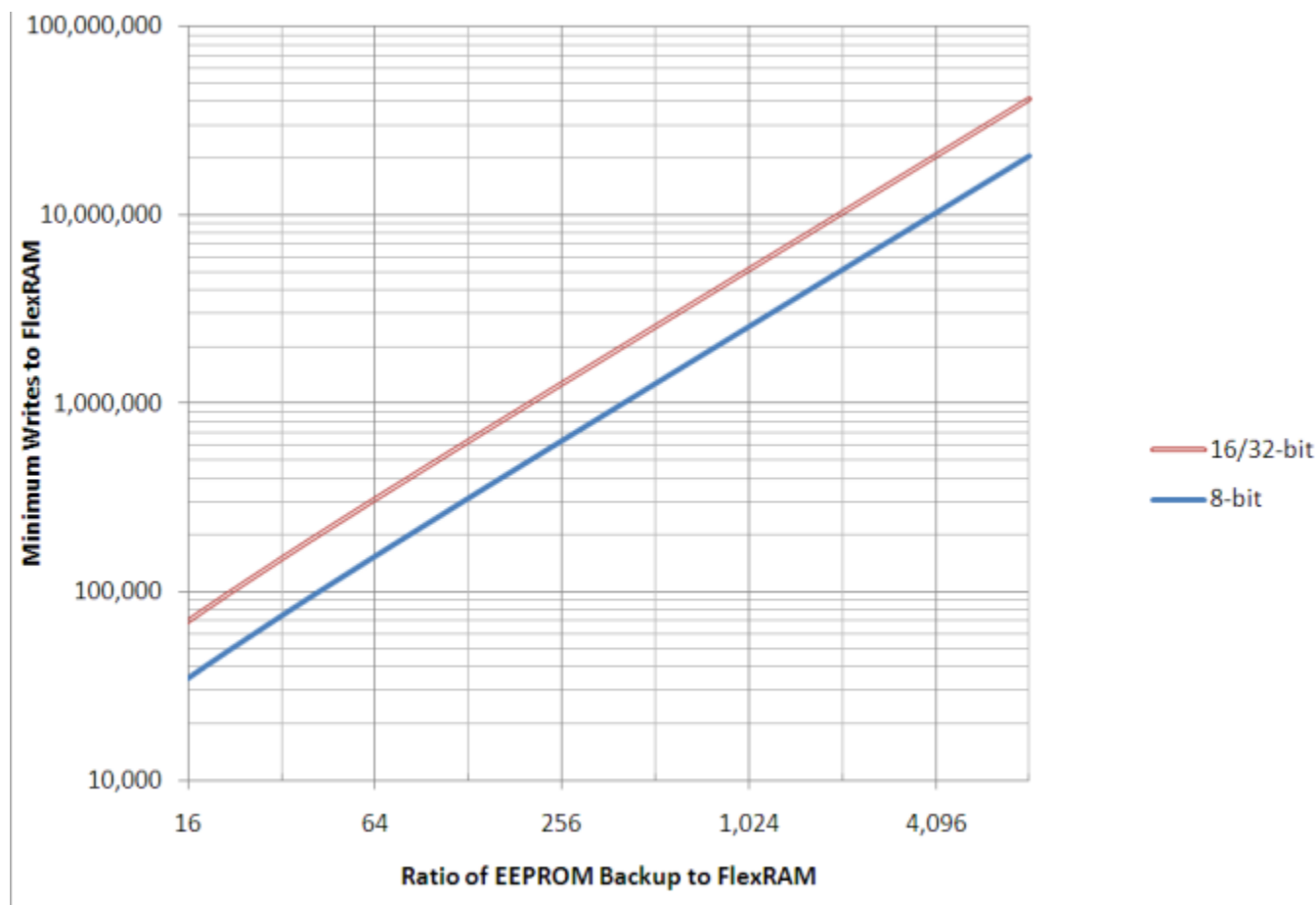


Figure 10. EEPROM backup writes to FlexRAM

## 6.4.2 EzPort Switching Specifications

Table 23. EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)	—	$f_{SYS}/2$	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	$f_{SYS}/8$	MHz
EP2	EZP_CS negation to next EZP_CS assertion	$2 \times t_{EZP\_CK}$	—	ns
EP3	EZP_CS input valid to EZP_CK high (setup)	5	—	ns
EP4	EZP_CK high to EZP_CS input invalid (hold)	5	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	2	—	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	—	ns
EP7	EZP_CK low to EZP_Q output valid	—	16	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	EZP_CS negation to EZP_Q tri-state	—	12	ns

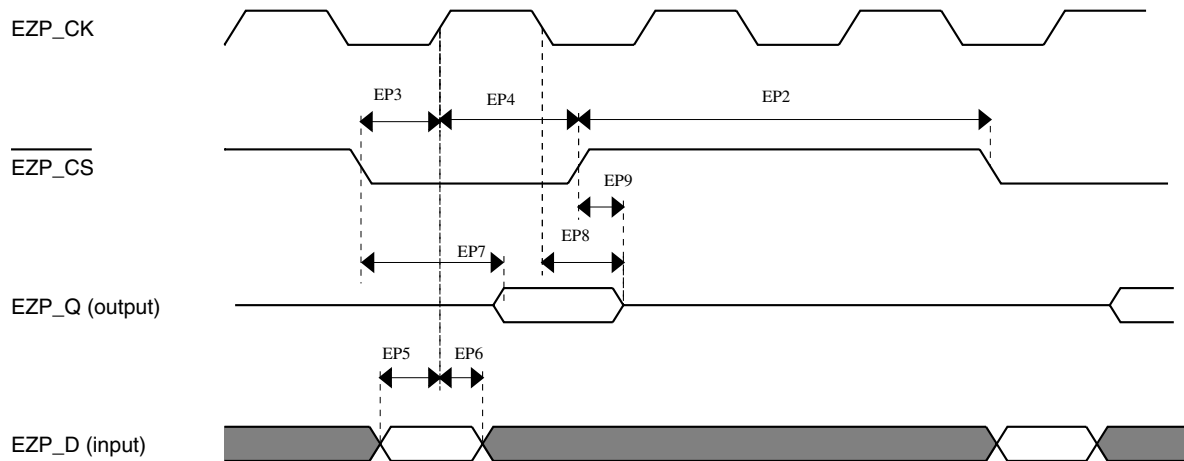


Figure 11. EzPort Timing Diagram

## 6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

## 6.6 Analog

### 6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in [Table 24](#) and [Table 25](#) are achievable on the differential pins ADCx\_DP0, ADCx\_DM0.

The ADCx\_DP2 and ADCx\_DM2 ADC inputs are connected to the PGA outputs and are not direct device pins. Accuracy specifications for these pins are defined in [Table 26](#) and [Table 27](#).

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

### 6.6.1.1 16-bit ADC operating conditions

**Table 24. 16-bit ADC operating conditions**

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
$V_{DDA}$	Supply voltage	Absolute	1.71	—	3.6	V	
$\Delta V_{DDA}$	Supply voltage	Delta to $V_{DD}$ ( $V_{DD} - V_{DDA}$ )	-100	0	+100	mV	2
$\Delta V_{SSA}$	Ground voltage	Delta to $V_{SS}$ ( $V_{SS} - V_{SSA}$ )	-100	0	+100	mV	2
$V_{REFH}$	ADC reference voltage high		1.13	$V_{DDA}$	$V_{DDA}$	V	
$V_{REFL}$	ADC reference voltage low		$V_{SSA}$	$V_{SSA}$	$V_{SSA}$	V	
$V_{ADIN}$	Input voltage	<ul style="list-style-type: none"> <li>16-bit differential mode</li> <li>All other modes</li> </ul>	VREFL	—	31/32 * VREFH	V	
$C_{ADIN}$	Input capacitance	<ul style="list-style-type: none"> <li>16-bit mode</li> <li>8-/10-/12-bit modes</li> </ul>	—	8	10	pF	
$R_{ADIN}$	Input resistance		—	2	5	k $\Omega$	
$R_{AS}$	Analog source resistance	13-/12-bit modes $f_{ADCK} < 4$ MHz	—	—	5	k $\Omega$	3
$f_{ADCK}$	ADC conversion clock frequency	$\leq$ 13-bit mode	1.0	—	18.0	MHz	4
$f_{ADCK}$	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	4
$C_{rate}$	ADC conversion rate	$\leq$ 13 bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	5
$C_{rate}$	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	5

1. Typical values assume  $V_{DDA} = 3.0$  V, Temp = 25 °C,  $f_{ADCK} = 1.0$  MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. The analog source resistance must be kept as low as possible to achieve the best results. The results in this data sheet were derived from a system which has < 8  $\Omega$  analog source resistance. The  $R_{AS}/C_{AS}$  time constant should be kept to < 1ns.
4. To use the maximum ADC conversion clock frequency, the ADHSC bit must be set and the ADLPC bit must be clear.
5. For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#)

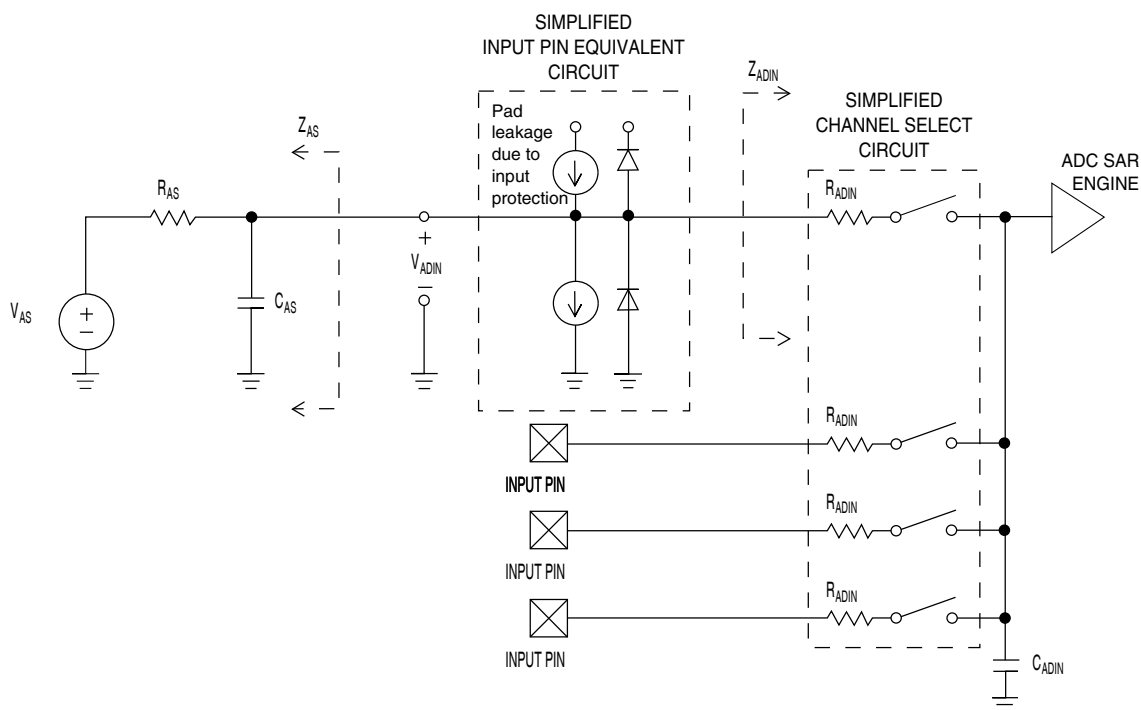


Figure 12. ADC input impedance equivalency diagram

### 6.6.1.2 16-bit ADC electrical characteristics

 Table 25. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ )

Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
$I_{DDA\_ADC}$	Supply current		0.215	—	1.7	mA	3
$f_{ADACK}$	ADC asynchronous clock source	<ul style="list-style-type: none"> <li>ADLPC = 1, ADHSC = 0</li> <li>ADLPC = 1, ADHSC = 1</li> <li>ADLPC = 0, ADHSC = 0</li> <li>ADLPC = 0, ADHSC = 1</li> </ul>	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	$t_{ADACK} = 1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	<ul style="list-style-type: none"> <li>12-bit modes</li> <li>&lt;12-bit modes</li> </ul>	— —	$\pm 4$ $\pm 1.4$	$\pm 6.8$ $\pm 2.1$	LSB <sup>4</sup>	5
DNL	Differential non-linearity	<ul style="list-style-type: none"> <li>12-bit modes</li> <li>&lt;12-bit modes</li> </ul>	— —	$\pm 0.7$ $\pm 0.2$	-1.1 to +1.9 -0.3 to 0.5	LSB <sup>4</sup>	5
INL	Integral non-linearity	<ul style="list-style-type: none"> <li>12-bit modes</li> <li>&lt;12-bit modes</li> </ul>	— —	$\pm 1.0$ $\pm 0.5$	-2.7 to +1.9 -0.7 to +0.5	LSB <sup>4</sup>	5
$E_{FS}$	Full-scale error	<ul style="list-style-type: none"> <li>12-bit modes</li> <li>&lt;12-bit modes</li> </ul>	— —	-4 -1.4	-5.4 -1.8	LSB <sup>4</sup>	$V_{ADIN} = V_{DDA}$ 5

Table continues on the next page...

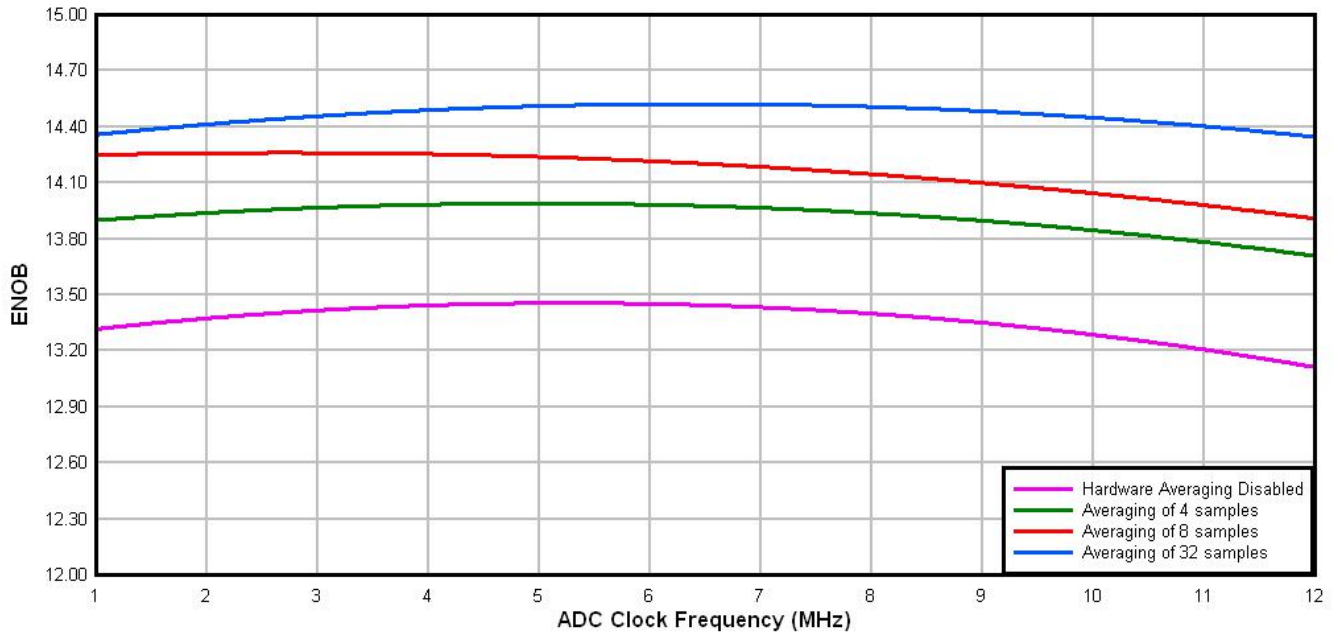
**Table 25. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)**

Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
$E_Q$	Quantization error	<ul style="list-style-type: none"> <li>16-bit modes</li> <li>≤13-bit modes</li> </ul>	—	-1 to 0	—	LSB <sup>4</sup>	
ENOB	Effective number of bits	16-bit differential mode <ul style="list-style-type: none"> <li>Avg = 32</li> <li>Avg = 4</li> </ul> 16-bit single-ended mode <ul style="list-style-type: none"> <li>Avg = 32</li> <li>Avg = 4</li> </ul>	12.8 11.9	14.5 13.8	— —	bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit differential mode <ul style="list-style-type: none"> <li>Avg = 32</li> </ul> 16-bit single-ended mode <ul style="list-style-type: none"> <li>Avg = 32</li> </ul>	—	-94	—	dB	7
SFDR	Spurious free dynamic range	16-bit differential mode <ul style="list-style-type: none"> <li>Avg = 32</li> </ul> 16-bit single-ended mode <ul style="list-style-type: none"> <li>Avg = 32</li> </ul>	82	95	—	dB	7
$E_{IL}$	Input leakage error		$I_{In} \times R_{AS}$			mV	$I_{In}$ = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	—	1.715	—	mV/°C	
$V_{TEMP25}$	Temp sensor voltage	25 °C	—	719	—	mV	

- All accuracy numbers assume the ADC is calibrated with  $V_{REFH} = V_{DDA}$
- Typical values assume  $V_{DDA} = 3.0$  V, Temp = 25°C,  $f_{ADCK} = 2.0$  MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- The ADC supply current depends on the ADC conversion clock speed, conversion rate and the ADLPC bit (low power). For lowest power operation the ADLPC bit must be set, the HSC bit must be clear with 1 MHz ADC conversion clock speed.
- 1 LSB =  $(V_{REFH} - V_{REFL})/2^N$
- ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
- Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
- Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.

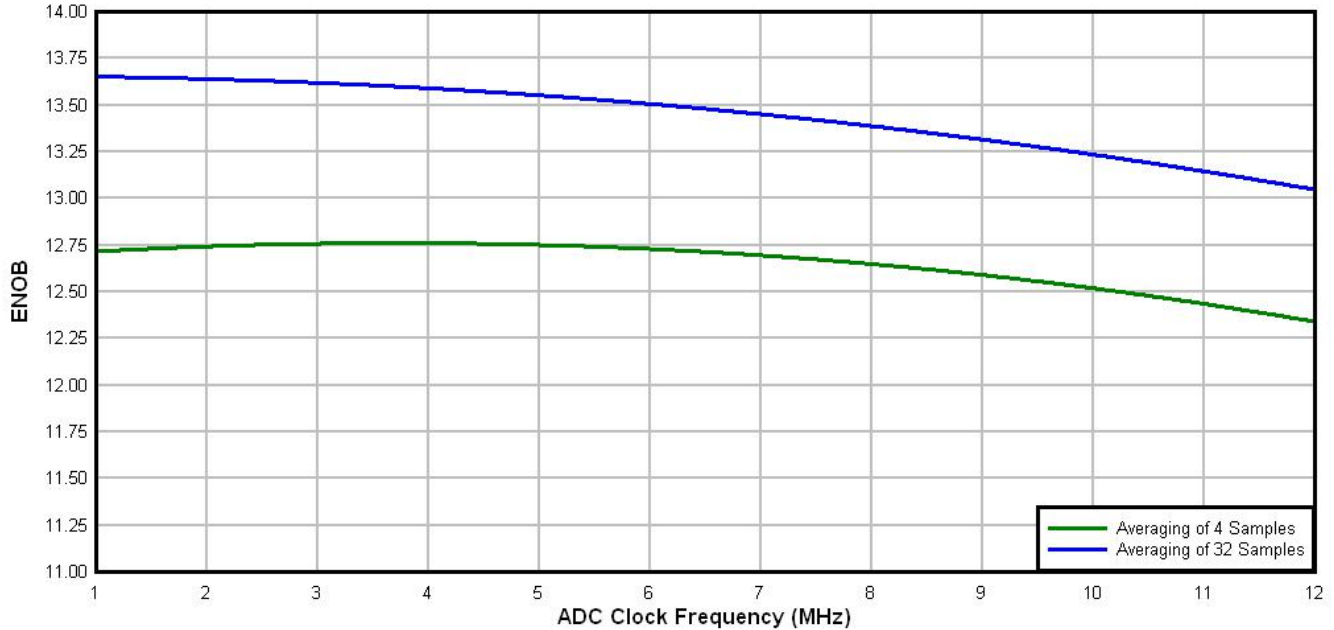


**Typical ADC 16-bit Differential ENOB vs ADC Clock**  
**100Hz, 90% FS Sine Input**



**Figure 13. Typical ENOB vs. ADC\_CLK for 16-bit differential mode**

**Typical ADC 16-bit Single-Ended ENOB vs ADC Clock**  
**100Hz, 90% FS Sine Input**



**Figure 14. Typical ENOB vs. ADC\_CLK for 16-bit single-ended mode**

### 6.6.1.3 16-bit ADC with PGA operating conditions

**Table 26. 16-bit ADC with PGA operating conditions**

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
V <sub>DDA</sub>	Supply voltage	Absolute	1.71	—	3.6	V	
V <sub>REFPGA</sub>	PGA ref voltage		VREF_OUT	VREF_OUT	VREF_OUT	V	2, 3
V <sub>ADIN</sub>	Input voltage		V <sub>SSA</sub>	—	V <sub>DDA</sub>	V	
V <sub>CM</sub>	Input Common Mode range		V <sub>SSA</sub>	—	V <sub>DDA</sub>	V	
R <sub>PGAD</sub>	Differential input impedance	Gain = 1, 2, 4, 8 Gain = 16, 32 Gain = 64	—	128 64 32	—	kΩ	IN+ to IN- <sup>4</sup>
R <sub>AS</sub>	Analog source resistance		—	100	—	Ω	5
T <sub>S</sub>	ADC sampling time		1.25	—	—	μs	6
C <sub>rate</sub>	ADC conversion rate	≤ 13 bit modes No ADC hardware averaging Continuous conversions enabled Peripheral clock = 50 MHz	18.484	—	450	Ksps	7
		16 bit modes No ADC hardware averaging Continuous conversions enabled Peripheral clock = 50 MHz	37.037	—	250	Ksps	8

1. Typical values assume V<sub>DDA</sub> = 3.0 V, Temp = 25°C, f<sub>ADCK</sub> = 6 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. ADC must be configured to use the internal voltage reference (VREF\_OUT)
3. PGA reference is internally connected to the VREF\_OUT pin. If the user wishes to drive VREF\_OUT with a voltage other than the output of the VREF module, the VREF module must be disabled.
4. For single ended configurations the input impedance of the driven input is R<sub>PGAD</sub>/2
5. The analog source resistance (R<sub>AS</sub>), external to MCU, should be kept as minimum as possible. Increased R<sub>AS</sub> causes drop in PGA gain without affecting other performances. This is not dependent on ADC clock frequency.
6. The minimum sampling time is dependent on input signal frequency and ADC mode of operation. A minimum of 1.25μs time should be allowed for F<sub>in</sub>=4 kHz at 16-bit differential mode. Recommended ADC setting is: ADLSMP=1, ADLSTS=2 at 8 MHz ADC clock.
7. ADC clock = 18 MHz, ADLSMP = 1, ADLST = 00, ADHSC = 1
8. ADC clock = 12 MHz, ADLSMP = 1, ADLST = 01, ADHSC = 1

### 6.6.1.4 16-bit ADC with PGA characteristics with Chop enabled (ADC\_PGA[PGACHPb] =0)

**Table 27. 16-bit ADC with PGA characteristics**

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
I <sub>DDA_PGA</sub>	Supply current	Low power (ADC_PGA[PGALPb]=0)	—	420	644	μA	2
I <sub>DC_PGA</sub>	Input DC current		$\frac{2}{R_{PGAD}} \left( \frac{V_{REFPGA} \times 0.583}{\text{Gain} + 1} - V_{CM} \right)$			A	3
		Gain =1, V <sub>REFPGA</sub> =1.2V, V <sub>CM</sub> =0.5V	—	1.54	—	μA	
		Gain =64, V <sub>REFPGA</sub> =1.2V, V <sub>CM</sub> =0.1V	—	0.57	—	μA	
G	Gain <sup>4</sup>	• PGAG=0	0.95	1	1.05		R <sub>AS</sub> < 100Ω
		• PGAG=1	1.9	2	2.1		
		• PGAG=2	3.8	4	4.2		
		• PGAG=3	7.6	8	8.4		
		• PGAG=4	15.2	16	16.6		
		• PGAG=5	30.0	31.6	33.2		
		• PGAG=6	58.8	63.3	67.8		
BW	Input signal bandwidth	• 16-bit modes	—	—	4	kHz	
		• < 16-bit modes	—	—	40	kHz	
PSRR	Power supply rejection ratio	Gain=1	—	-84	—	dB	V <sub>DDA</sub> = 3V ±100mV, f <sub>VDDA</sub> = 50Hz, 60Hz
CMRR	Common mode rejection ratio	• Gain=1	—	-84	—	dB	V <sub>CM</sub> = 500mVpp, f <sub>VCM</sub> = 50Hz, 100Hz
		• Gain=64	—	-85	—	dB	
V <sub>OFS</sub>	Input offset voltage		—	0.2	—	mV	Output offset = V <sub>OFS</sub> *(Gain+1)
T <sub>GSW</sub>	Gain switching settling time		—	—	10	μs	5
dG/dT	Gain drift over full temperature range	• Gain=1	—	6	10	ppm/°C	
		• Gain=64	—	31	42	ppm/°C	
dG/dV <sub>DDA</sub>	Gain drift over supply voltage	• Gain=1	—	0.07	0.21	%/V	V <sub>DDA</sub> from 1.71 to 3.6V
		• Gain=64	—	0.14	0.31	%/V	
E <sub>IL</sub>	Input leakage error	All modes	I <sub>In</sub> × R <sub>AS</sub>			mV	I <sub>In</sub> = leakage current  (refer to the MCU's voltage and current operating ratings)

Table continues on the next page...

**Table 27. 16-bit ADC with PGA characteristics (continued)**

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
V <sub>PP,DIFF</sub>	Maximum differential input signal swing		$\left( \frac{(\min(V_X, V_{DDA} - V_X) - 0.2) \times 4}{\text{Gain}} \right)$ where V <sub>X</sub> = V <sub>REFPGA</sub> × 0.583			V	6
SNR	Signal-to-noise ratio	<ul style="list-style-type: none"> <li>Gain=1</li> <li>Gain=64</li> </ul>	80	90	—	dB	16-bit differential mode, Average=32
			52	66	—	dB	
THD	Total harmonic distortion	<ul style="list-style-type: none"> <li>Gain=1</li> <li>Gain=64</li> </ul>	85	100	—	dB	16-bit differential mode, Average=32, f <sub>in</sub> =100Hz
			49	95	—	dB	
SFDR	Spurious free dynamic range	<ul style="list-style-type: none"> <li>Gain=1</li> <li>Gain=64</li> </ul>	85	105	—	dB	16-bit differential mode, Average=32, f <sub>in</sub> =100Hz
			53	88	—	dB	
ENOB	Effective number of bits	<ul style="list-style-type: none"> <li>Gain=1, Average=4</li> <li>Gain=64, Average=4</li> <li>Gain=1, Average=32</li> <li>Gain=2, Average=32</li> <li>Gain=4, Average=32</li> <li>Gain=8, Average=32</li> <li>Gain=16, Average=32</li> <li>Gain=32, Average=32</li> <li>Gain=64, Average=32</li> </ul>	11.6	13.4	—	bits	16-bit differential mode, f <sub>in</sub> =100Hz
			7.2	9.6	—	bits	
			12.8	14.5	—	bits	
			11.0	14.3	—	bits	
			7.9	13.8	—	bits	
			7.3	13.1	—	bits	
			6.8	12.5	—	bits	
			6.8	11.5	—	bits	
			7.5	10.6	—	bits	
SINAD	Signal-to-noise plus distortion ratio	See ENOB	6.02 × ENOB + 1.76			dB	

1. Typical values assume V<sub>DDA</sub> = 3.0V, Temp = 25°C, f<sub>ADCK</sub> = 6MHz unless otherwise stated.
2. This current is a PGA module adder, in addition to ADC conversion currents.
3. Between IN+ and IN-. The PGA draws a DC current from the input terminals. The magnitude of the DC current is a strong function of input common mode voltage (V<sub>CM</sub>) and the PGA gain.
4. Gain = 2<sup>PGAG</sup>
5. After changing the PGA gain setting, a minimum of 2 ADC+PGA conversions should be ignored.
6. Limit the input signal swing so that the PGA does not saturate during operation. Input signal swing is dependent on the PGA reference voltage and gain setting.

## 6.6.2 CMP and 6-bit DAC electrical specifications

**Table 28. Comparator and 6-bit DAC electrical specifications**

Symbol	Description	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Supply voltage	1.71	—	3.6	V

Table continues on the next page...

**Table 28. Comparator and 6-bit DAC electrical specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit
$I_{DDHS}$	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	$\mu\text{A}$
$I_{DDL5}$	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	$\mu\text{A}$
$V_{AIN}$	Analog input voltage	$V_{SS} - 0.3$	—	$V_{DD}$	V
$V_{AIO}$	Analog input offset voltage	—	—	20	mV
$V_H$	Analog comparator hysteresis <sup>1</sup> <ul style="list-style-type: none"> <li>• CR0[HYSTCTR] = 00</li> <li>• CR0[HYSTCTR] = 01</li> <li>• CR0[HYSTCTR] = 10</li> <li>• CR0[HYSTCTR] = 11</li> </ul>	—	5	—	mV
		—	10	—	mV
		—	20	—	mV
		—	30	—	mV
$V_{CMPOH}$	Output high	$V_{DD} - 0.5$	—	—	V
$V_{CMPOI}$	Output low	—	—	0.5	V
$t_{DHS}$	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
$t_{DLS}$	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay <sup>2</sup>	—	—	40	$\mu\text{s}$
$I_{DAC6b}$	6-bit DAC current adder (enabled)	—	7	—	$\mu\text{A}$
INL	6-bit DAC integral non-linearity	-0.5	—	0.5	LSB <sup>3</sup>
DNL	6-bit DAC differential non-linearity	-0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to  $V_{DD}-0.6\text{V}$ .
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3.  $1 \text{ LSB} = V_{\text{reference}}/64$

Peripheral operating requirements and behaviors

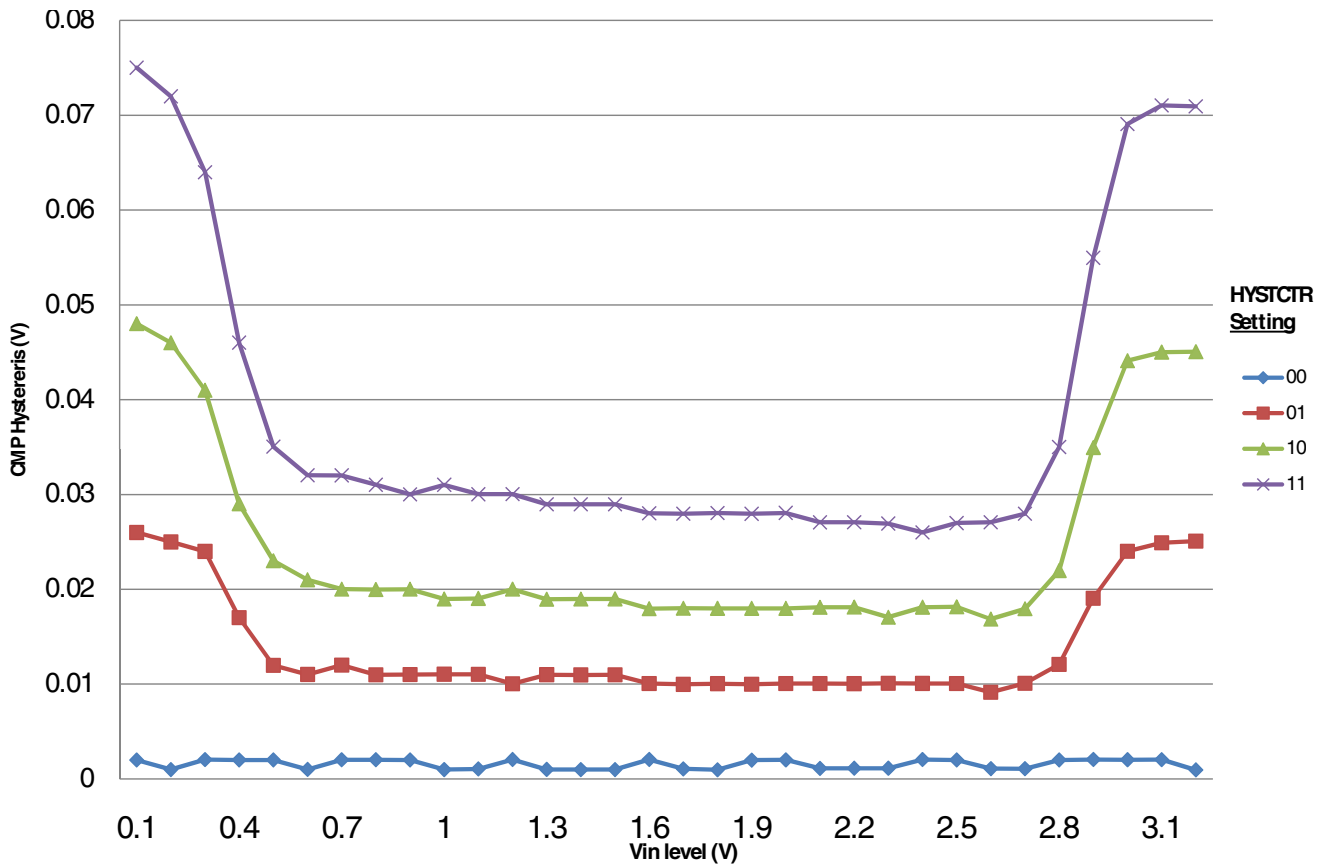


Figure 15. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=0)

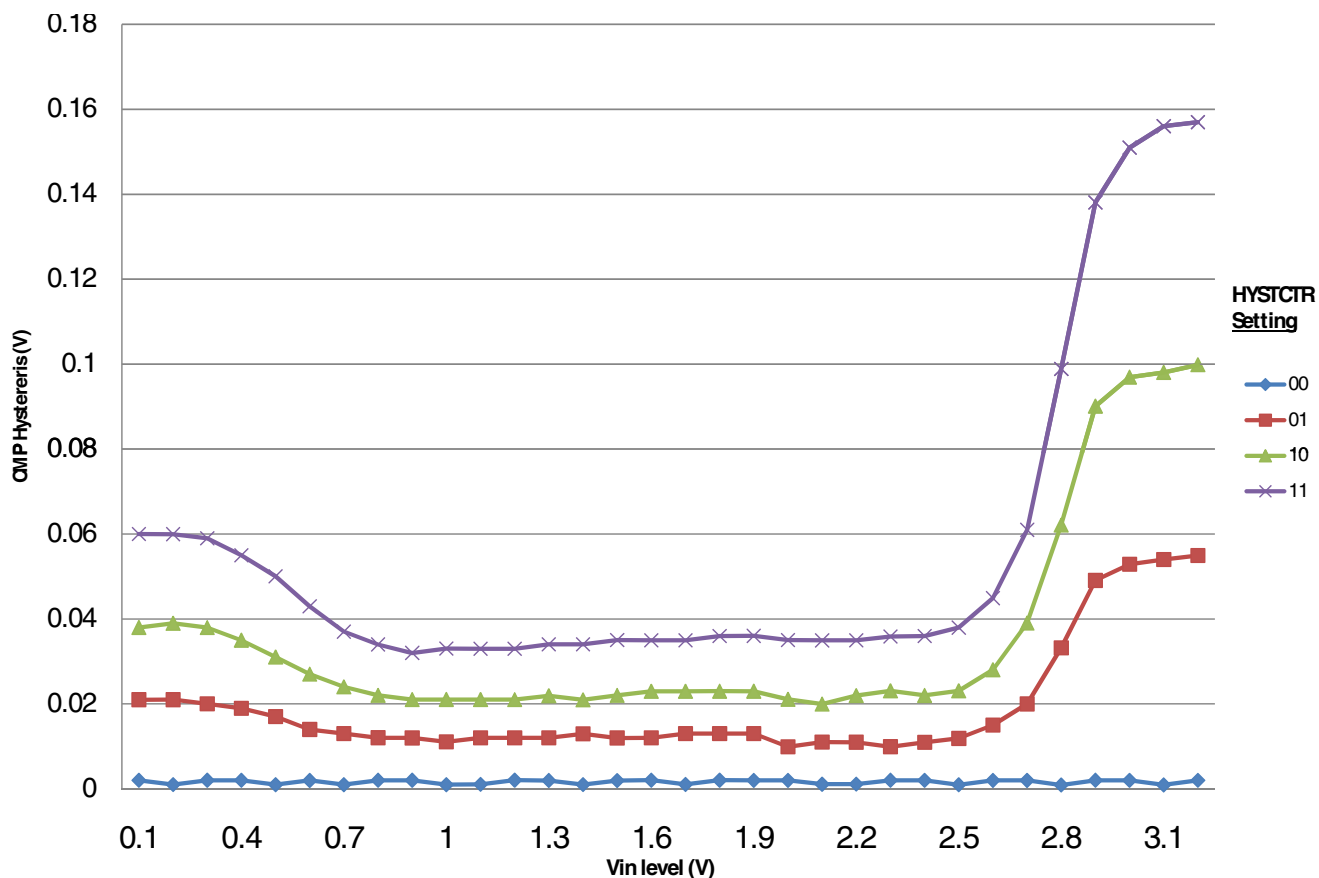


Figure 16. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=1)

## 6.6.3 12-bit DAC electrical characteristics

### 6.6.3.1 12-bit DAC operating requirements

Table 29. 12-bit DAC operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
$V_{DDA}$	Supply voltage	1.71	3.6	V	
$V_{DACR}$	Reference voltage	1.13	3.6	V	1
$T_A$	Temperature	Operating temperature range of the device		°C	
$C_L$	Output load capacitance	—	100	pF	2
$I_L$	Output load current	—	1	mA	

1. The DAC reference can be selected to be  $V_{DDA}$  or the voltage output of the VREF module (VREF\_OUT)
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

### 6.6.3.2 12-bit DAC operating behaviors

**Table 30. 12-bit DAC operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$I_{DDA\_DACLP}$	Supply current — low-power mode	—	—	150	$\mu\text{A}$	
$I_{DDA\_DACHP}$	Supply current — high-speed mode	—	—	700	$\mu\text{A}$	
$t_{DACLP}$	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	$\mu\text{s}$	1
$t_{DACHP}$	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	$\mu\text{s}$	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	$\mu\text{s}$	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	$V_{DACR} - 100$	—	$V_{DACR}$	mV	
INL	Integral non-linearity error — high speed mode	—	—	$\pm 8$	LSB	2
DNL	Differential non-linearity error — $V_{DACR} > 2\text{ V}$	—	—	$\pm 1$	LSB	3
DNL	Differential non-linearity error — $V_{DACR} = V_{REF\_OUT}$	—	—	$\pm 1$	LSB	4
$V_{OFFSET}$	Offset error	—	$\pm 0.4$	$\pm 0.8$	%FSR	5
$E_G$	Gain error	—	$\pm 0.1$	$\pm 0.6$	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} \geq 2.4\text{ V}$	60	—	90	dB	
$T_{CO}$	Temperature coefficient offset voltage	—	3.7	—	$\mu\text{V}/\text{C}$	6
$T_{GE}$	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
$R_{op}$	Output resistance load = 3 k $\Omega$	—	—	250	$\Omega$	
SR	Slew rate -80h → F7Fh → 80h <ul style="list-style-type: none"> <li>• High power (<math>SP_{HP}</math>)</li> <li>• Low power (<math>SP_{LP}</math>)</li> </ul>	1.2 0.05	1.7 0.12	— —	V/ $\mu\text{s}$	
CT	Channel to channel cross talk	—	—	-80	dB	
BW	3dB bandwidth <ul style="list-style-type: none"> <li>• High power (<math>SP_{HP}</math>)</li> <li>• Low power (<math>SP_{LP}</math>)</li> </ul>	550 40	— —	— —	kHz	

- Settling within  $\pm 1$  LSB
- The INL is measured for 0 + 100 mV to  $V_{DACR} - 100$  mV
- The DNL is measured for 0 + 100 mV to  $V_{DACR} - 100$  mV
- The DNL is measured for 0 + 100 mV to  $V_{DACR} - 100$  mV with  $V_{DDA} > 2.4\text{ V}$
- Calculated by a best fit curve from  $V_{SS} + 100$  mV to  $V_{DACR} - 100$  mV
- $V_{DDA} = 3.0\text{ V}$ , reference select set for  $V_{DDA}$  ( $DACX\_CO:DACRFS = 1$ ), high power mode ( $DACX\_CO:LPEN = 0$ ), DAC set to 0x800, temperature range is across the full range of the device



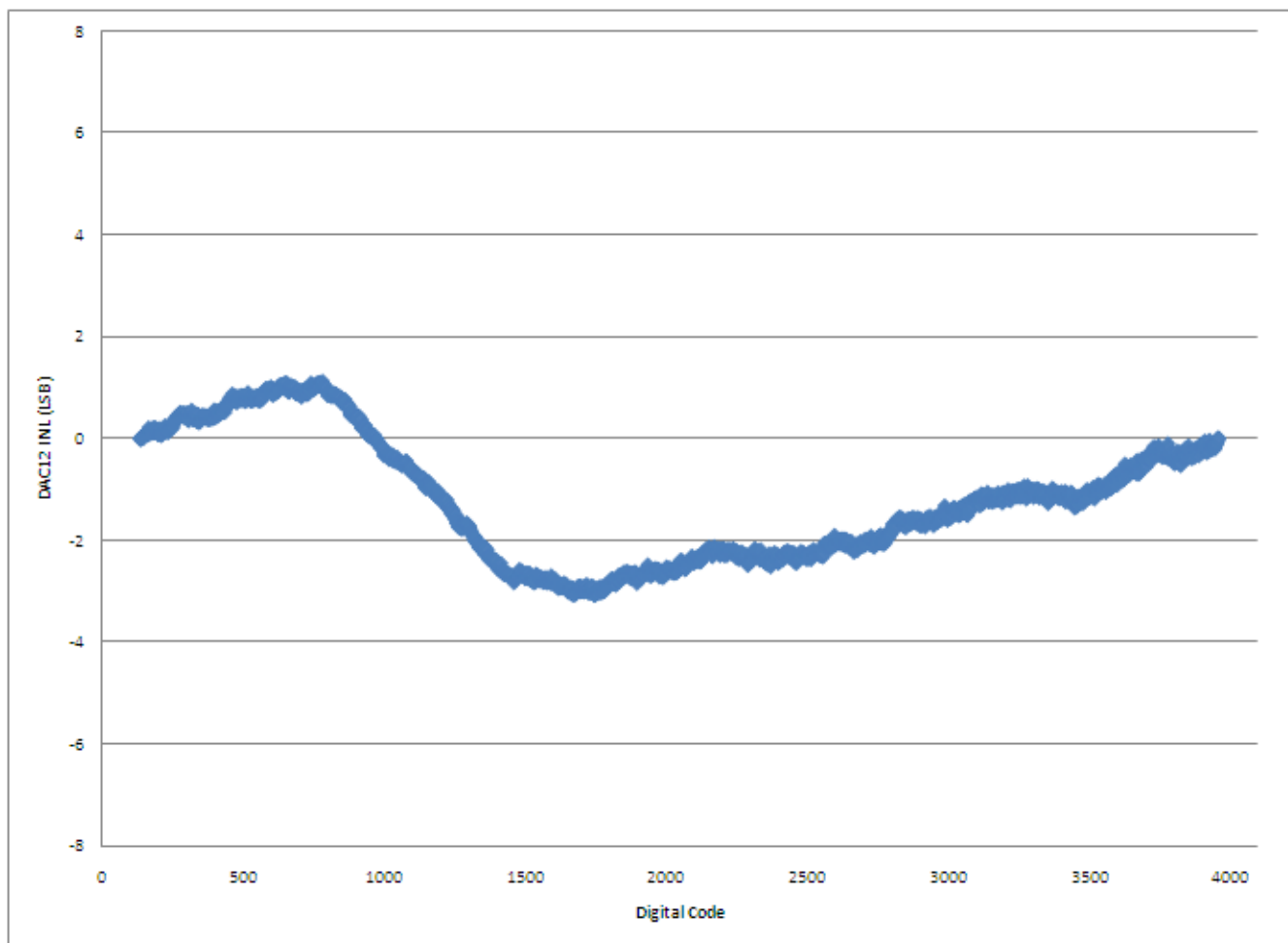


Figure 17. Typical INL error vs. digital code

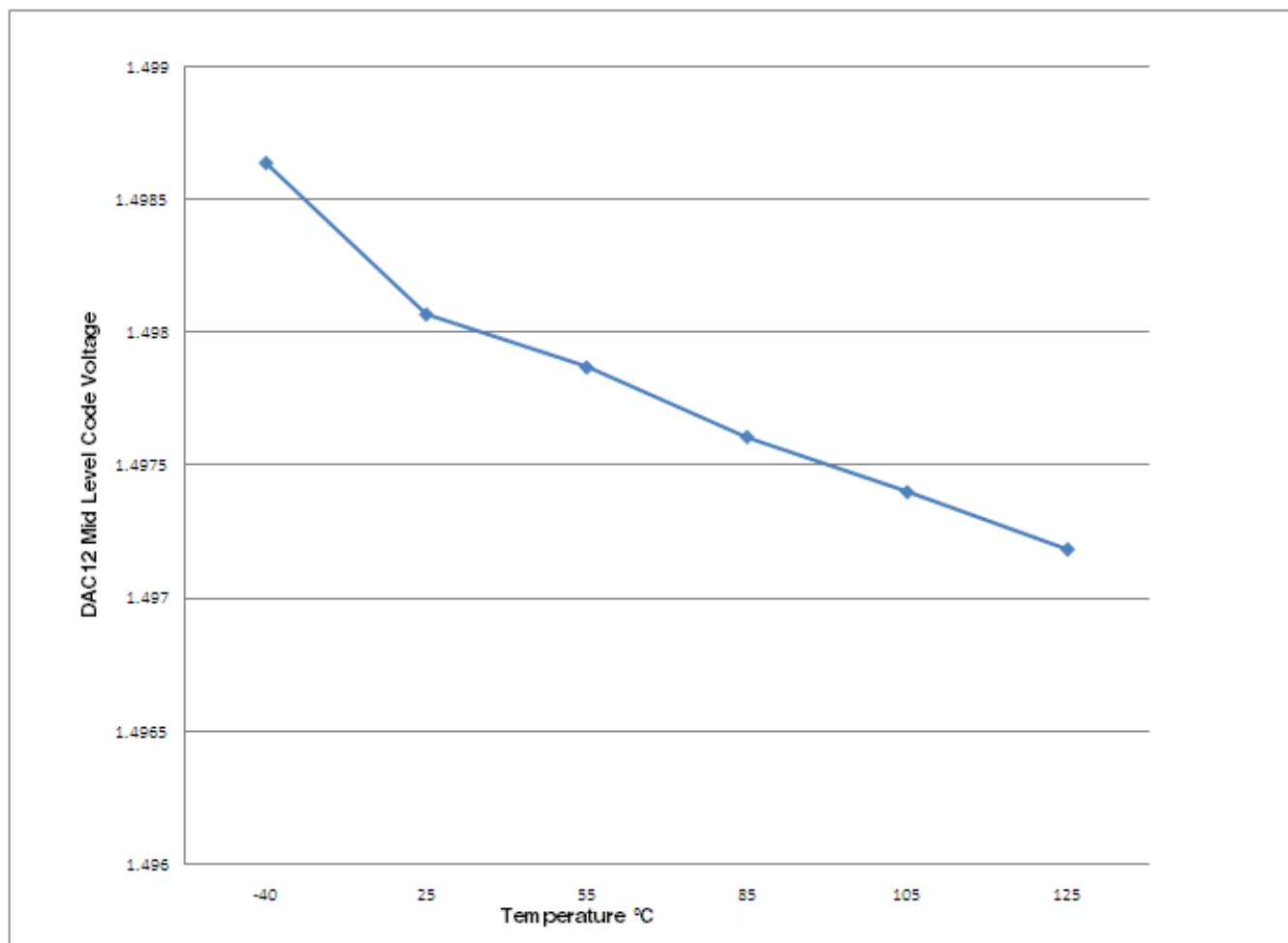


Figure 18. Offset at half scale vs. temperature

## 6.6.4 Op-amp electrical specifications

Table 31. Op-amp electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Operating voltage	1.71	—	3.6	V
I <sub>SUPPLY</sub>	Supply current (I <sub>OUT</sub> =0mA, CL=0), low-power mode	—	106	125	μA
I <sub>SUPPLY</sub>	Supply current (I <sub>OUT</sub> =0mA, CL=0), high-speed mode	—	545	630	μA
V <sub>OS</sub>	Input offset voltage	—	±3	±10	mV
α <sub>VOS</sub>	Input offset voltage temperature coefficient	—	10	—	μV/C
I <sub>OS</sub>	Typical input offset current across the following temp range (0–50°C)	—	±500	—	pA
I <sub>OS</sub>	Typical input offset current across the following temp range (-40–105°C)	—	4	—	nA

Table continues on the next page...

**Table 31. Op-amp electrical specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit
$I_{BIAS}$	Typical input bias current across the following temp range (0–50°C)	—	±500	—	pA
$I_{BIAS}$	Typical input bias current across the following temp range (-40–105°C)	—	±4	—	nA
$V_{CML}$	Input common mode voltage low	0	—	—	V
$V_{CMH}$	Input common mode voltage high	—	—	VDD	V
$R_{IN}$	Input resistance	—	500	—	MΩ
$C_{IN}$	Input capacitance	—	17 <sup>1</sup>	—	pF
$ X_{IN} $	AC input impedance ( $f_{IN}=100kHz$ )	—	50	—	MΩ
CMRR	Input common mode rejection ratio	60	—	—	dB
PSRR	Power supply rejection ratio	60	—	—	dB
SR	Slew rate ( $\Delta V_{IN}=500mV$ ), low-power mode	0.1	—	—	V/μs
SR	Slew rate ( $\Delta V_{IN}=500mV$ ), high-speed mode	1.5	4	—	V/μs
GBW	Unity gain bandwidth, low-power mode	0.15	—	—	MHz
GBW	Unity gain bandwidth, high-speed mode	1	—	—	MHz
$A_V$	DC open-loop voltage gain	80	90	—	dB
CL(max)	Load capacitance driving capability	—	100	—	pF
$R_{OUT}$	Output resistance @ 100 kHz, high speed mode	—	1500	—	Ω
$V_{OUT}$	Output voltage range	0.12	—	VDD - 0.12	V
$I_{OUT}$	Output load current	—	±0.5	—	mA
GM	Gain margin	—	20	—	dB
PM	Phase margin	45	56	—	deg
$T_{settle}$	Settling time <sup>2</sup> (Buffer mode, low-power mode) ( $T_o < 0.1\%$ , $V_{in}=1.65V$ )	—	5.7	—	μs
$T_{settle}$	Settling time <sup>2</sup> (Buffer mode, high-speed mode) ( $T_o < 0.1\%$ , $V_{in}=1.65V$ )	—	3.0	—	μs
$V_n$	Voltage noise density (noise floor) 1kHz	—	350	—	nV/√Hz
$V_n$	Voltage noise density (noise floor) 10kHz	—	90	—	nV/√Hz

1. The input capacitance is dependant on the package type used.
2. Settling time is measured from the time the Op-amp is enabled until the output settles to within 0.1% of final value. This time includes Op-amp startup time, output slew, and settle time.

## 6.6.5 Transimpedance amplifier electrical specifications — full range

**Table 32. TRIAMP full range operating requirements**

Symbol	Description	Min.	Max.	Unit	Notes
$V_{DDA}$	Supply voltage	1.71	3.6	V	
$V_{IN}$	Input voltage range	-0.1	$V_{DDA}-1.4$	V	
$C_L$	Output load capacitance	—	100	pf	

**Table 33. TRIAMP full range operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>SUPPLY</sub>	Supply current (I <sub>OUT</sub> =0mA, CL=0) — Low-power mode	—	60	80	μA	
I <sub>SUPPLY</sub>	Supply current (I <sub>OUT</sub> =0mA, CL=0) — High-speed mode	—	280	450	μA	
V <sub>OS</sub>	Input offset voltage	—	±3	±5	mV	
α <sub>VOS</sub>	Input offset voltage temperature coefficient	—	4.8	—	μV/C	
I <sub>OS</sub>	Input offset current	—	±0.3	±5	nA	
I <sub>BIAS</sub>	Input bias current	—	±0.3	±5	nA	
R <sub>IN</sub>	Input resistance	500	—	—	MΩ	
C <sub>IN</sub>	Input capacitance	—	17	—	pF	
R <sub>OUT</sub>	Output AC impedance	—	—	1500	Ω	@ 100kHz, High speed mode
X <sub>IN</sub>	AC input impedance (f <sub>IN</sub> =100kHz)	—	159	—	kΩ	
CMRR	Input common mode rejection ratio	60	—	—	dB	
PSRR	Power supply rejection ratio	60	—	—	dB	
SR	Slew rate (ΔV <sub>IN</sub> =100mV) — Low-power mode	0.1	—	—	V/μs	
SR	Slew rate (ΔV <sub>IN</sub> =100mV) — High speed mode	1	—	—	V/μs	
GBW	Unity gain bandwidth — Low-power mode 50pF	0.15	—	—	MHz	
GBW	Unity gain bandwidth — High speed mode 50pF	1	—	—	MHz	
A <sub>V</sub>	DC open-loop voltage gain	80	—	—	dB	
V <sub>OUT</sub>	Output voltage range	0.15	—	V <sub>DD</sub> -0.15	V	
I <sub>OUT</sub>	Output load current	—	±0.5	—	mA	
GM	Gain margin	—	20	—	dB	
PM	Phase margin	50	60	—	deg	
V <sub>n</sub>	Voltage noise density (noise floor) 1kHz	—	280	—	nV/√Hz	
V <sub>n</sub>	Voltage noise density (noise floor) 10kHz	—	100	—	nV/√Hz	

### 6.6.6 Transimpedance amplifier electrical specifications — limited range

**Table 34. TRIAMP limited range operating requirements**

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>DDA</sub>	Supply voltage	2.4	3.3	V	
V <sub>IN</sub>	Input voltage range	0.1	V <sub>DDA</sub> -1.4	V	
T <sub>A</sub>	Temperature	0	50	C	
C <sub>L</sub>	Output load capacitance	—	100	pf	

**Table 35. TRIAMP limited range operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{OS}$	Input offset voltage	—	$\pm 3$	$\pm 5$	mV	
$\alpha_{VOS}$	Input offset voltage temperature coefficient	—	4.8	—	$\mu V/C$	
$I_{OS}$	Input offset current	—	$\pm 300$	$\pm 600$	pA	
$I_{BIAS}$	Input bias current	—	$\pm 300$	$\pm 600$	pA	
$R_{OUT}$	Output AC impedance	—	—	1500	$\Omega$	@ 100kHz, High speed mode
$ X_{IN} $	AC input impedance ( $f_{IN}=100kHz$ )	—	159	—	$k\Omega$	
CMRR	Input common mode rejection ratio	—	70	—	dB	
PSRR	Power supply rejection ratio	—	70	—	dB	
SR	Slew rate ( $\Delta V_{IN}=500mV$ ) — Low-power mode	0.1	—	—	$V/\mu s$	
SR	Slew rate ( $\Delta V_{IN}=500mV$ ) — High speed mode	1.5	3.5	—	$V/\mu s$	
GBW	Unity gain bandwidth — Low-power mode 50pF	0.15	—	—	MHz	
GBW	Unity gain bandwidth — High speed mode 50pF	1	—	—	MHz	
$A_V$	DC open-loop voltage gain	80	—	—	dB	
GM	Gain margin	—	20	—	dB	
PM	Phase margin	60	69	—	deg	

## 6.6.7 Voltage reference electrical specifications

**Table 36. VREF full-range operating requirements**

Symbol	Description	Min.	Max.	Unit	Notes
$V_{DDA}$	Supply voltage	1.71	3.6	V	
$T_A$	Temperature	Operating temperature range of the device		$^{\circ}C$	
$C_L$	Output load capacitance	100		nF	1, 2

- $C_L$  must be connected to VREF\_OUT if the VREF\_OUT functionality is being used for either an internal or external reference.
- The load capacitance should not exceed +/-25% of the nominal specified  $C_L$  value over the operating temperature range of the device.

**Table 37. VREF full-range operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{out}$	Voltage reference output with factory trim at nominal $V_{DDA}$ and temperature=25C	1.1915	1.195	1.1977	V	
$V_{out}$	Voltage reference output — factory trim	1.1584	—	1.2376	V	
$V_{out}$	Voltage reference output — user trim	1.193	—	1.197	V	
$V_{step}$	Voltage reference trim step	—	0.5	—	mV	

Table continues on the next page...

**Table 37. VREF full-range operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{tdrift}$	Temperature drift ( $V_{max} - V_{min}$ across the full temperature range)	—	—	80	mV	
$I_{bg}$	Bandgap only current	—	—	80	$\mu$ A	1
$I_{lp}$	Low-power buffer current	—	—	360	$\mu$ A	1
$I_{hp}$	High-power buffer current	—	—	1	mA	1
$\Delta V_{LOAD}$	Load regulation • current = $\pm 1.0$ mA	—	200	—	$\mu$ V	1, 2
$T_{stup}$	Buffer startup time	—	—	100	$\mu$ s	
$V_{vdift}$	Voltage drift ( $V_{max} - V_{min}$ across the full voltage range)	—	2	—	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF\_OUT voltage with no load vs. voltage with defined load

**Table 38. VREF limited-range operating requirements**

Symbol	Description	Min.	Max.	Unit	Notes
$T_A$	Temperature	0	50	$^{\circ}$ C	

**Table 39. VREF limited-range operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes
$V_{out}$	Voltage reference output with factory trim	1.173	1.225	V	

## 6.7 Timers

See [General switching specifications](#).

## 6.8 Communication interfaces

### 6.8.1 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit <http://www.usb.org>.

## 6.8.2 USB DCD electrical specifications

Table 40. USB DCD electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V <sub>DP_SRC</sub>	USB_DP source voltage (up to 250 $\mu$ A)	0.5	—	0.7	V
V <sub>LGC</sub>	Threshold voltage for logic high	0.8	—	2.0	V
I <sub>DP_SRC</sub>	USB_DP source current	7	10	13	$\mu$ A
I <sub>DM_SINK</sub>	USB_DM sink current	50	100	150	$\mu$ A
R <sub>DM_DWN</sub>	D- pulldown resistance for data pin contact detect	14.25	—	24.8	k $\Omega$
V <sub>DAT_REF</sub>	Data detect voltage	0.25	0.33	0.4	V

## 6.8.3 USB VREG electrical specifications

Table 41. USB VREG electrical specifications

Symbol	Description	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
V <sub>REGIN</sub>	Input supply voltage	2.7	—	5.5	V	
I <sub>DDon</sub>	Quiescent current — Run mode, load current equal zero, input supply (V <sub>REGIN</sub> ) > 3.6 V	—	120	186	$\mu$ A	
I <sub>DDstby</sub>	Quiescent current — Standby mode, load current equal zero	—	1.1	10	$\mu$ A	
I <sub>DDoff</sub>	Quiescent current — Shutdown mode <ul style="list-style-type: none"> <li>V<sub>REGIN</sub> = 5.0 V and temperature=25C</li> <li>Across operating voltage and temperature</li> </ul>	—	650	—	nA	
		—	—	4	$\mu$ A	
I <sub>LOADrun</sub>	Maximum load current — Run mode	—	—	120	mA	
I <sub>LOADstby</sub>	Maximum load current — Standby mode	—	—	1	mA	
V <sub>Reg33out</sub>	Regulator output voltage — Input supply (V <sub>REGIN</sub> ) > 3.6 V <ul style="list-style-type: none"> <li>Run mode</li> <li>Standby mode</li> </ul>	3	3.3	3.6	V	
		2.1	2.8	3.6	V	
V <sub>Reg33out</sub>	Regulator output voltage — Input supply (V <sub>REGIN</sub> ) < 3.6 V, pass-through mode	2.1	—	3.6	V	2
C <sub>OUT</sub>	External output capacitor	1.76	2.2	8.16	$\mu$ F	
ESR	External output capacitor equivalent series resistance	1	—	100	m $\Omega$	
I <sub>LIM</sub>	Short circuit current	—	290	—	mA	

1. Typical values assume V<sub>REGIN</sub> = 5.0 V, Temp = 25 °C unless otherwise stated.

2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I<sub>Load</sub>.

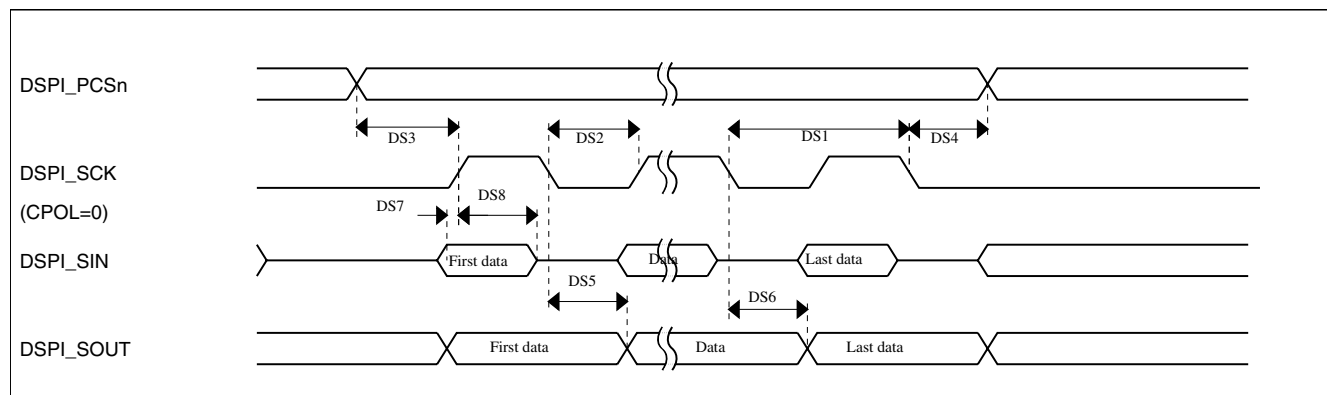
### 6.8.4 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

**Table 42. Master mode DSPI timing (limited voltage range)**

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	25	MHz	
DS1	DSPI_SCK output cycle time	$2 \times t_{BUS}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	$(t_{BUS} \times 2) - 2$	—	ns	1
DS4	DSPI_SCK to DSPI_PCSn invalid delay	$(t_{BUS} \times 2) - 2$	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	15	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx\_CTARn[PSSCK] and SPIx\_CTARn[CSSCK].
2. The delay is programmable in SPIx\_CTARn[PASC] and SPIx\_CTARn[ASC].



**Figure 19. DSPI classic SPI timing — master mode**

**Table 43. Slave mode DSPI timing (limited voltage range)**

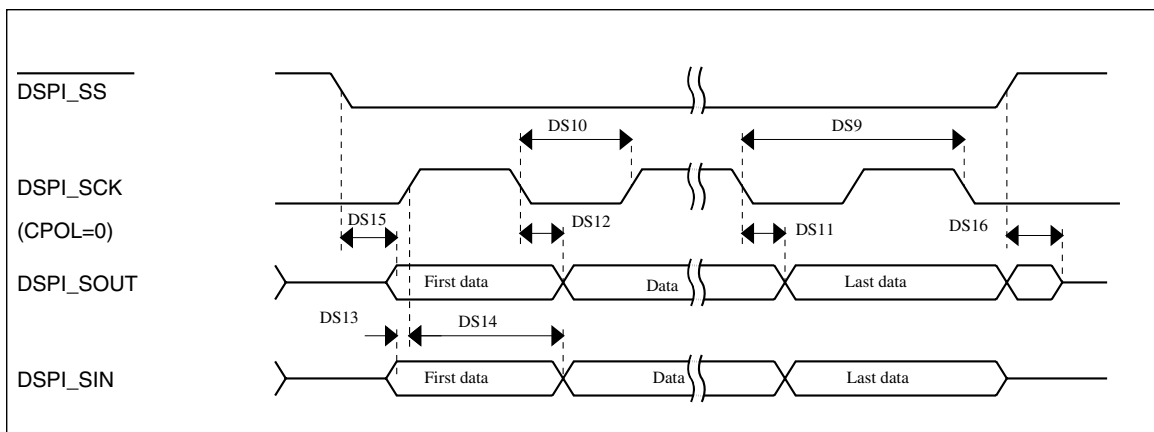
Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	$4 \times t_{BUS}$	—	ns

Table continues on the next page...



**Table 43. Slave mode DSPI timing (limited voltage range) (continued)**

Num	Description	Min.	Max.	Unit
DS10	DSPI_SCK input high/low time	$(t_{SCK/2}) - 2$	$(t_{SCK/2}) + 2$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	10	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	14	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	14	ns


**Figure 20. DSPI classic SPI timing — slave mode**

### 6.8.5 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

**Table 44. Master mode DSPI timing (full voltage range)**

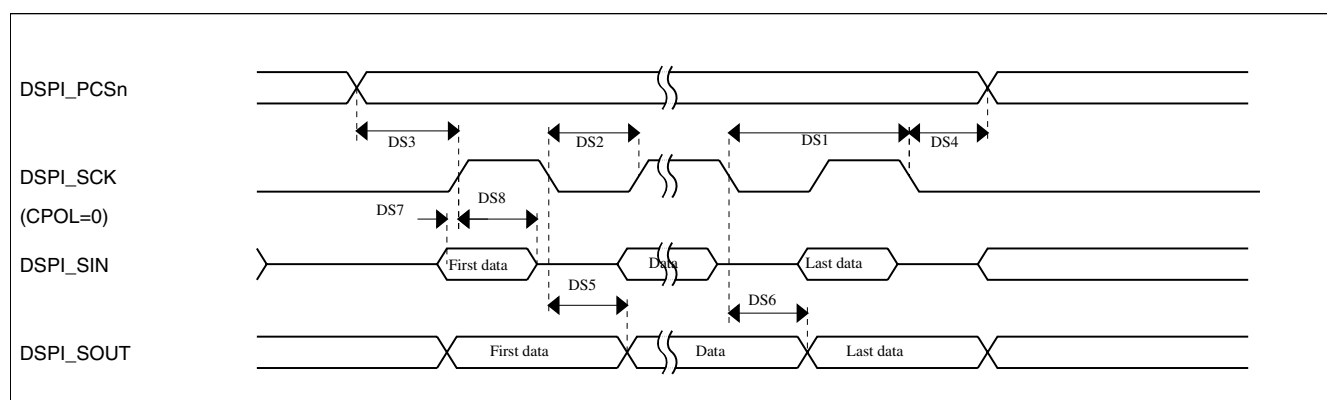
Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	12.5	MHz	
DS1	DSPI_SCK output cycle time	$4 \times t_{BUS}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{SCK/2}) - 4$	$(t_{SCK/2}) + 4$	ns	
DS3	DSPI_PCS <sub>n</sub> valid to DSPI_SCK delay	$(t_{BUS} \times 2) - 4$	—	ns	2

Table continues on the next page...

**Table 44. Master mode DSPI timing (full voltage range) (continued)**

Num	Description	Min.	Max.	Unit	Notes
DS4	DSPI_SCK to DSPI_PCSn invalid delay	$(t_{BUS} \times 2) - 4$	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-4.5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	20.5	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx\_CTARn[PSSCK] and SPIx\_CTARn[CSSCK].
3. The delay is programmable in SPIx\_CTARn[PASC] and SPIx\_CTARn[ASC].



**Figure 21. DSPI classic SPI timing — master mode**

**Table 45. Slave mode DSPI timing (full voltage range)**

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	6.25	MHz
DS9	DSPI_SCK input cycle time	$8 \times t_{BUS}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 4$	$(t_{SCK}/2) + 4$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	19	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	19	ns

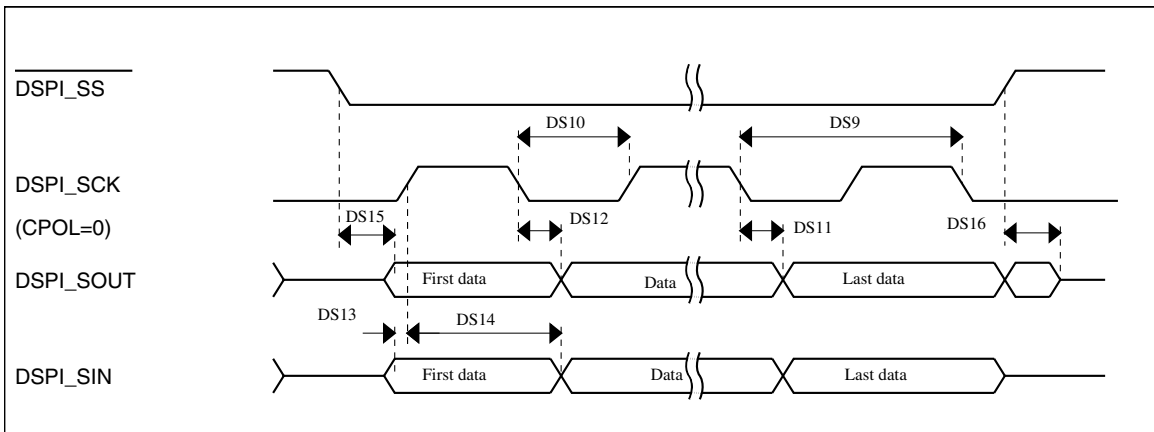


Figure 22. DSPI classic SPI timing — slave mode

### 6.8.6 I<sup>2</sup>C switching specifications

See [General switching specifications](#).

### 6.8.7 UART switching specifications

See [General switching specifications](#).

### 6.8.8 I2S/SAI Switching Specifications

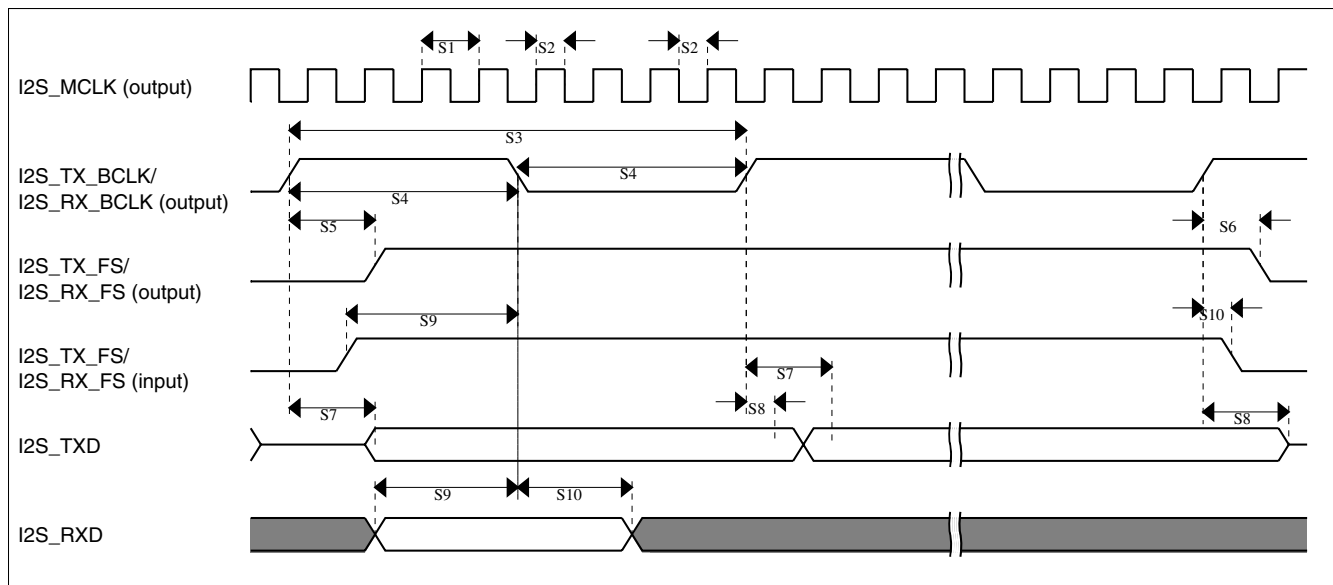
This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

#### 6.8.8.1 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

**Table 46. I2S/SAI master mode timing in Normal Run, Wait and Stop modes (full voltage range)**

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	-1.0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	20.5	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns



**Figure 23. I2S/SAI timing — master modes**

**Table 47. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (full voltage range)**

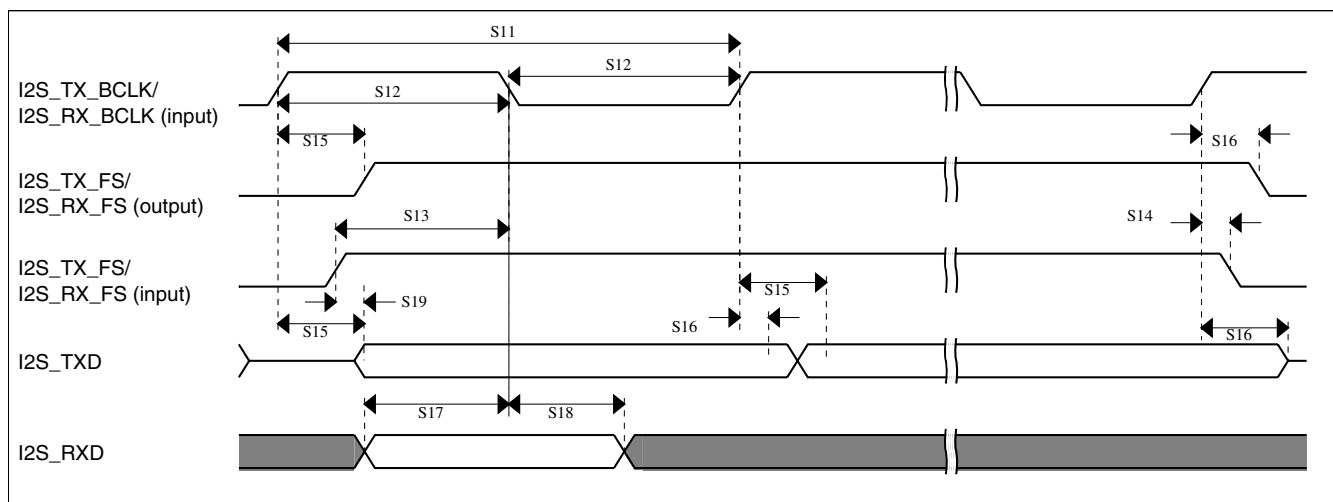
Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period

Table continues on the next page...

**Table 47. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (full voltage range) (continued)**

Num.	Characteristic	Min.	Max.	Unit
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	5.8	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	5.8	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid <sup>1</sup>	—	25	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear


**Figure 24. I2S/SAI timing — slave modes**

### 6.8.8.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

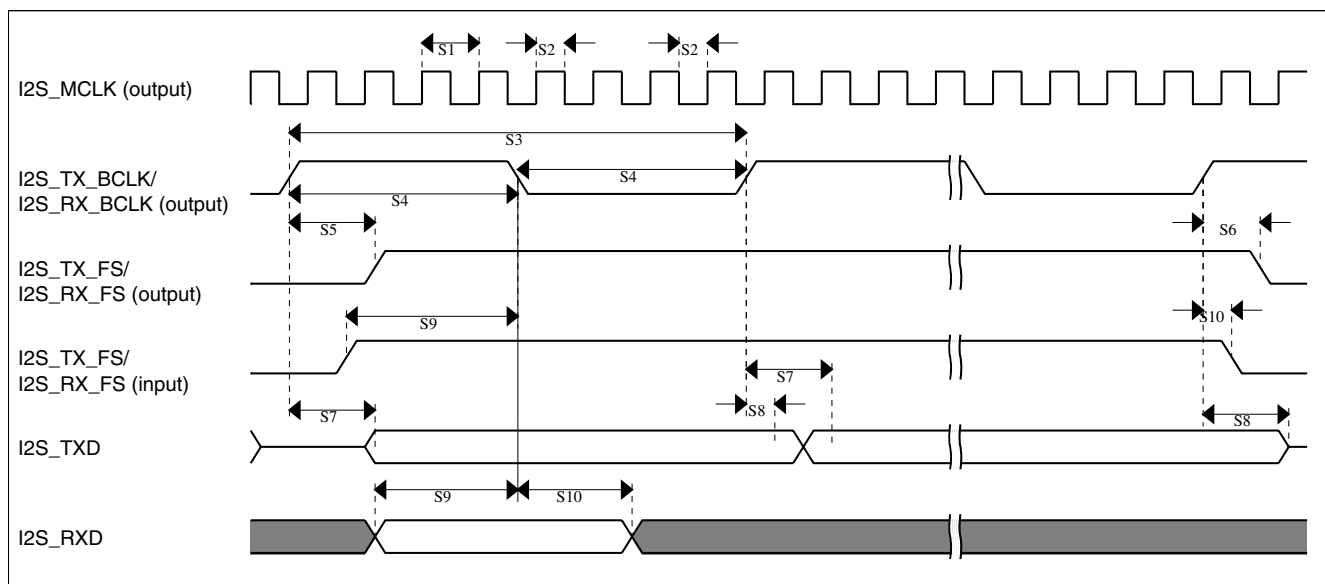
**Table 48. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)**

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period

Table continues on the next page...

**Table 48. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)**

Num.	Characteristic	Min.	Max.	Unit
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	53	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns



**Figure 25. I2S/SAI timing — master modes**

**Table 49. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)**

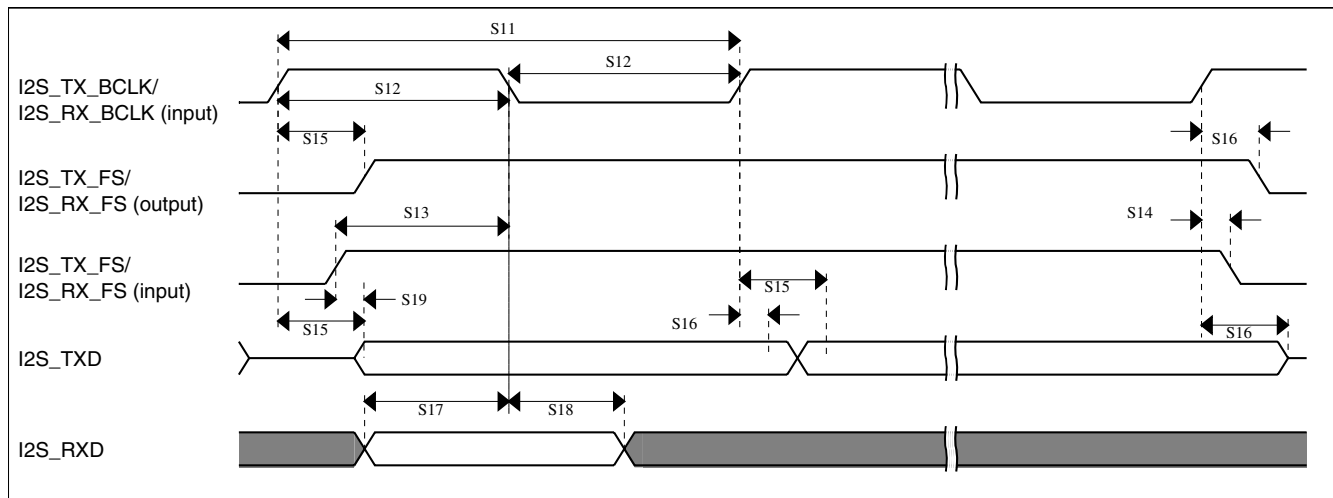
Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	7.6	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	67	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns

Table continues on the next page...

**Table 49. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)**

Num.	Characteristic	Min.	Max.	Unit
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	6.5	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid <sup>1</sup>	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear


**Figure 26. I2S/SAI timing — slave modes**

## 6.9 Human-machine interfaces (HMI)

### 6.9.1 TSI electrical specifications

**Table 50. TSI electrical specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{DDTSI}$	Operating voltage	1.71	—	3.6	V	
$C_{ELE}$	Target electrode capacitance range	1	20	500	pF	1
$f_{REFmax}$	Reference oscillator frequency	—	8	15	MHz	2, 3
$f_{ELEmax}$	Electrode oscillator frequency	—	1	1.8	MHz	2, 4
$C_{REF}$	Internal reference capacitor	—	1	—	pF	
$V_{DELTA}$	Oscillator delta voltage	—	500	—	mV	2, 5
$I_{REF}$	Reference oscillator current source base current <ul style="list-style-type: none"> <li>• 2 <math>\mu</math>A setting (REFCHRG = 0)</li> <li>• 32 <math>\mu</math>A setting (REFCHRG = 15)</li> </ul>	—	2	3	$\mu$ A	2, 6

Table continues on the next page...

**Table 50. TSI electrical specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>ELE</sub>	Electrode oscillator current source base current <ul style="list-style-type: none"> <li>• 2 μA setting (EXTCHRG = 0)</li> <li>• 32 μA setting (EXTCHRG = 15)</li> </ul>	—	2	3	μA	2, 7
Pres5	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	8
Pres20	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	9
Pres100	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	10
MaxSens	Maximum sensitivity	0.008	1.46	—	fF/count	11
Res	Resolution	—	—	16	bits	
T <sub>Con20</sub>	Response time @ 20 pF	8	15	25	μs	12
I <sub>TSI_RUN</sub>	Current added in run mode	—	55	—	μA	
I <sub>TSI_LP</sub>	Low power mode current adder	—	1.3	2.5	μA	13

1. The TSI module is functional with capacitance values outside this range. However, optimal performance is not guaranteed.
2. Fixed external capacitance of 20 pF.
3. REFCHRG = 2, EXTCHRG=0.
4. REFCHRG = 0, EXTCHRG = 10.
5. V<sub>DD</sub> = 3.0 V.
6. The programmable current source value is generated by multiplying the SCANC[REFCHRG] value and the base current.
7. The programmable current source value is generated by multiplying the SCANC[EXTCHRG] value and the base current.
8. Measured with a 5 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 8; I<sub>ext</sub> = 16.
9. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 2; I<sub>ext</sub> = 16.
10. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 16, NSCN = 3; I<sub>ext</sub> = 16.
11. Sensitivity defines the minimum capacitance change when a single count from the TSI module changes. Sensitivity depends on the configuration used. The documented values are provided as examples calculated for a specific configuration of operating conditions using the following equation:  $(C_{ref} * I_{ext}) / (I_{ref} * PS * NSCN)$   
 The typical value is calculated with the following configuration:  
 I<sub>ext</sub> = 6 μA (EXTCHRG = 2), PS = 128, NSCN = 2, I<sub>ref</sub> = 16 μA (REFCHRG = 7), C<sub>ref</sub> = 1.0 pF  
 The minimum value is calculated with the following configuration:  
 I<sub>ext</sub> = 2 μA (EXTCHRG = 0), PS = 128, NSCN = 32, I<sub>ref</sub> = 32 μA (REFCHRG = 15), C<sub>ref</sub> = 0.5 pF  
 The highest possible sensitivity is the minimum value because it represents the smallest possible capacitance that can be measured by a single count.
12. Time to do one complete measurement of the electrode. Sensitivity resolution of 0.0133 pF, PS = 0, NSCN = 0, 1 electrode, EXTCHRG = 7.
13. REFCHRG=0, EXTCHRG=4, PS=7, NSCN=0F, LPSCNITV=F, LPO is selected (1 kHz), and fixed external capacitance of 20 pF. Data is captured with an average of 7 periods window.

## 6.9.2 LCD electrical characteristics

**Table 51. LCD electricals**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f <sub>Frame</sub>	LCD frame frequency	28	30	58	Hz	
C <sub>LCD</sub>	LCD charge pump capacitance — nominal value	—	100	—	nF	1
C <sub>BYLCD</sub>	LCD bypass capacitance — nominal value	—	100	—	nF	1
C <sub>Glass</sub>	LCD glass capacitance	—	2000	8000	pF	2

Table continues on the next page...



**Table 51. LCD electricals (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{IREG}$	$V_{IREG}$					3
$\Delta_{RTRIM}$	$V_{IREG}$ TRIM resolution	—	—	3.0	% $V_{IREG}$	
—	$V_{IREG}$ ripple					
$I_{VIREG}$	$V_{IREG}$ current adder — $RVEN = 1$	—	1	—	$\mu A$	4
$I_{RBIAS}$	RBIAS current adder <ul style="list-style-type: none"> <li>LADJ = 10 or 11 — High load (LCD glass capacitance <math>\leq 8000</math> pF)</li> <li>LADJ = 00 or 01 — Low load (LCD glass capacitance <math>\leq 2000</math> pF)</li> </ul>	—	10	—	$\mu A$	
		—	1	—	$\mu A$	
$R_{RBIAS}$	RBIAS resistor values <ul style="list-style-type: none"> <li>LADJ = 10 or 11 — High load (LCD glass capacitance <math>\leq 8000</math> pF)</li> <li>LADJ = 00 or 01 — Low load (LCD glass capacitance <math>\leq 2000</math> pF)</li> </ul>	—	0.28	—	$M\Omega$	
		—	2.98	—	$M\Omega$	
VLL2	VLL2 voltage					
VLL3	VLL3 voltage					

1. The actual value used could vary with tolerance.
2. For highest glass capacitance values, LCD\_GCR[LADJ] should be configured as specified in the LCD Controller chapter within the device's reference manual.
3.  $V_{IREG}$  maximum should never be externally driven to any level other than  $V_{DD} - 0.15$  V
4. 2000 pF load LCD, 32 Hz frame frequency

## 7 Dimensions

### 7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to [www.freescale.com](http://www.freescale.com) and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
100-pin LQFP	98ASS23308W
121-pin MAPBGA	98ASA00344D

## 8 Pinout

### 8.1 K51 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

121 MAP BGA	100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
E4	1	PTE0	ADC1_SE4a	ADC1_SE4a	PTE0	SPI1_PCS1	UART1_TX			I2C1_SDA	RTC_CLKOUT	
E3	2	PTE1/ LLWU_P0	ADC1_SE5a	ADC1_SE5a	PTE1/ LLWU_P0	SPI1_SOUT	UART1_RX			I2C1_SCL	SPI1_SIN	
E2	3	PTE2/ LLWU_P1	ADC1_SE6a	ADC1_SE6a	PTE2/ LLWU_P1	SPI1_SCK	UART1_CTS_ b					
F4	4	PTE3	ADC1_SE7a	ADC1_SE7a	PTE3	SPI1_SIN	UART1_RTS_ b				SPI1_SOUT	
E7	—	VDD	VDD	VDD								
F7	—	VSS	VSS	VSS								
H7	5	PTE4/ LLWU_P2	DISABLED		PTE4/ LLWU_P2	SPI1_PCS0	UART3_TX					
G4	6	PTE5	DISABLED		PTE5	SPI1_PCS2	UART3_RX					
E6	7	VDD	VDD	VDD								
G7	8	VSS	VSS	VSS								
L6	—	VSS	VSS	VSS								
F1	9	USB0_DP	USB0_DP	USB0_DP								
F2	10	USB0_DM	USB0_DM	USB0_DM								
G1	11	VOOUT33	VOOUT33	VOOUT33								
G2	12	VREGIN	VREGIN	VREGIN								
H1	13	ADC0_DP1/ OP0_DP0	ADC0_DP1/ OP0_DP0	ADC0_DP1/ OP0_DP0								
H2	14	ADC0_DM1/ OP0_DM0	ADC0_DM1/ OP0_DM0	ADC0_DM1/ OP0_DM0								
J1	15	ADC1_DP1/ OP1_DP0/ OP1_DM1	ADC1_DP1/ OP1_DP0/ OP1_DM1	ADC1_DP1/ OP1_DP0/ OP1_DM1								
J2	16	ADC1_DM1/ OP1_DM0	ADC1_DM1/ OP1_DM0	ADC1_DM1/ OP1_DM0								
K1	17	PGA0_DP/ ADC0_DPO/ ADC1_DP3	PGA0_DP/ ADC0_DPO/ ADC1_DP3	PGA0_DP/ ADC0_DPO/ ADC1_DP3								
K2	18	PGA0_DM/ ADC0_DM0/ ADC1_DM3	PGA0_DM/ ADC0_DM0/ ADC1_DM3	PGA0_DM/ ADC0_DM0/ ADC1_DM3								

121 MAP BGA	100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
L1	19	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3								
L2	20	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3								
F5	21	VDDA	VDDA	VDDA								
G5	22	VREFH	VREFH	VREFH								
G6	23	VREFL	VREFL	VREFL								
F6	24	VSSA	VSSA	VSSA								
J3	25	ADC1_SE16/ OP1_OUT/ CMP2_IN2/ ADC0_SE22/ OP0_DP2/ OP1_DP2	ADC1_SE16/ OP1_OUT/ CMP2_IN2/ ADC0_SE22/ OP0_DP2/ OP1_DP2	ADC1_SE16/ OP1_OUT/ CMP2_IN2/ ADC0_SE22/ OP0_DP2/ OP1_DP2								
H3	26	ADC0_SE16/ OP0_OUT/ CMP1_IN2/ ADC0_SE21/ OP0_DP1/ OP1_DP1	ADC0_SE16/ OP0_OUT/ CMP1_IN2/ ADC0_SE21/ OP0_DP1/ OP1_DP1	ADC0_SE16/ OP0_OUT/ CMP1_IN2/ ADC0_SE21/ OP0_DP1/ OP1_DP1								
L3	27	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18								
K3	28	TRIO_OUT/ OP1_DM2	TRIO_OUT/ OP1_DM2	TRIO_OUT/ OP1_DM2								
H4	29	TRIO_DM	TRIO_DM	TRIO_DM								
J4	30	TRIO_DP	TRIO_DP	TRIO_DP								
H5	31	NC	NC	NC								
J5	32	NC	NC	NC								
H6	33	CMP2_IN5/ ADC1_SE22	CMP2_IN5/ ADC1_SE22	CMP2_IN5/ ADC1_SE22								
K5	34	DAC0_OUT/ CMP1_IN3/ ADC0_SE23/ OP0_DP4/ OP1_DP4	DAC0_OUT/ CMP1_IN3/ ADC0_SE23/ OP0_DP4/ OP1_DP4	DAC0_OUT/ CMP1_IN3/ ADC0_SE23/ OP0_DP4/ OP1_DP4								
K4	35	CMP0_IN4/ CMP2_IN3/ ADC1_SE23/ OP0_DP5/ OP1_DP5	CMP0_IN4/ CMP2_IN3/ ADC1_SE23/ OP0_DP5/ OP1_DP5	CMP0_IN4/ CMP2_IN3/ ADC1_SE23/ OP0_DP5/ OP1_DP5								
L7	—	RTC_ WAKEUP_B	RTC_ WAKEUP_B	RTC_ WAKEUP_B								
L4	36	XTAL32	XTAL32	XTAL32								
L5	37	EXTAL32	EXTAL32	EXTAL32								

**Pinout**

121 MAP BGA	100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
K6	38	VBAT	VBAT	VBAT								
J6	39	PTA0	JTAG_TCLK/ SWD_CLK/ EZP_CLK	TSIO_CH1	PTA0	UART0_CTS_ b/ UART0_COL_ b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
H8	40	PTA1	JTAG_TDI/ EZP_DI	TSIO_CH2	PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
J7	41	PTA2	JTAG_TDO/ TRACE_SWO/ EZP_DO	TSIO_CH3	PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
H9	42	PTA3	JTAG_TMS/ SWD_DIO	TSIO_CH4	PTA3	UART0_RTS_ b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
J8	43	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b	TSIO_CH5	PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
E5	—	VDD	VDD	VDD								
G3	—	VSS	VSS	VSS								
K8	44	PTA12	CMP2_IN0	CMP2_IN0	PTA12		FTM1_CH0			I2S0_TXD0	FTM1_QD_ PHA	
L8	45	PTA13/ LLWU_P4	CMP2_IN1	CMP2_IN1	PTA13/ LLWU_P4		FTM1_CH1			I2S0_TX_FS	FTM1_QD_ PHB	
K9	46	PTA14	DISABLED		PTA14	SPI0_PCS0	UART0_TX			I2S0_RX_ BCLK	I2S0_TXD1	
L9	47	PTA15	DISABLED		PTA15	SPI0_SCK	UART0_RX			I2S0_RXD0		
L10	48	VDD	VDD	VDD								
K10	49	VSS	VSS	VSS								
L11	50	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0				
K11	51	PTA19	XTAL0	XTAL0	PTA19		FTM1_FLT0	FTM_CLKIN1		LPTMR0_ ALT1		
J11	52	RESET_b	RESET_b	RESET_b								
G11	53	PTB0/ LLWU_P5	LCD_P0/ ADC0_SE8/ ADC1_SE8/ TSIO_CH0	LCD_P0/ ADC0_SE8/ ADC1_SE8/ TSIO_CH0	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_ PHA	LCD_P0	
G10	54	PTB1	LCD_P1/ ADC0_SE9/ ADC1_SE9/ TSIO_CH6	LCD_P1/ ADC0_SE9/ ADC1_SE9/ TSIO_CH6	PTB1	I2C0_SDA	FTM1_CH1			FTM1_QD_ PHB	LCD_P1	
G9	55	PTB2	LCD_P2/ ADC0_SE12/ TSIO_CH7	LCD_P2/ ADC0_SE12/ TSIO_CH7	PTB2	I2C0_SCL	UART0_RTS_ b			FTM0_FLT3	LCD_P2	
G8	56	PTB3	LCD_P3/ ADC0_SE13/ TSIO_CH8	LCD_P3/ ADC0_SE13/ TSIO_CH8	PTB3	I2C0_SDA	UART0_CTS_ b/ UART0_COL_ b			FTM0_FLT0	LCD_P3	
E11	57	PTB7	LCD_P7/ ADC1_SE13	LCD_P7/ ADC1_SE13	PTB7						LCD_P7	
D11	58	PTB8	LCD_P8	LCD_P8	PTB8		UART3_RTS_ b				LCD_P8	

121 MAP BGA	100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
E10	59	PTB9	LCD_P9	LCD_P9	PTB9	SPI1_PCS1	UART3_CTS_b				LCD_P9	
D10	60	PTB10	LCD_P10/ ADC1_SE14	LCD_P10/ ADC1_SE14	PTB10	SPI1_PCS0	UART3_RX			FTM0_FLT1	LCD_P10	
C10	61	PTB11	LCD_P11/ ADC1_SE15	LCD_P11/ ADC1_SE15	PTB11	SPI1_SCK	UART3_TX			FTM0_FLT2	LCD_P11	
B10	62	PTB16	LCD_P12/ TSIO_CH9	LCD_P12/ TSIO_CH9	PTB16	SPI1_SOUT	UART0_RX			EWM_IN	LCD_P12	
E9	63	PTB17	LCD_P13/ TSIO_CH10	LCD_P13/ TSIO_CH10	PTB17	SPI1_SIN	UART0_TX			EWM_OUT_b	LCD_P13	
D9	64	PTB18	LCD_P14/ TSIO_CH11	LCD_P14/ TSIO_CH11	PTB18		FTM2_CH0	I2S0_TX_BCLK		FTM2_QD_PHA	LCD_P14	
C9	65	PTB19	LCD_P15/ TSIO_CH12	LCD_P15/ TSIO_CH12	PTB19		FTM2_CH1	I2S0_TX_FS		FTM2_QD_PHB	LCD_P15	
F10	66	PTB20	LCD_P16	LCD_P16	PTB20					CMP0_OUT	LCD_P16	
F9	67	PTB21	LCD_P17	LCD_P17	PTB21					CMP1_OUT	LCD_P17	
F8	68	PTB22	LCD_P18	LCD_P18	PTB22					CMP2_OUT	LCD_P18	
E8	69	PTB23	LCD_P19	LCD_P19	PTB23		SPI0_PCS5				LCD_P19	
B9	70	PTC0	LCD_P20/ ADC0_SE14/ TSIO_CH13	LCD_P20/ ADC0_SE14/ TSIO_CH13	PTC0	SPI0_PCS4	PDB0_EXTRG			I2S0_TXD1	LCD_P20	
D8	71	PTC1/ LLWU_P6	LCD_P21/ ADC0_SE15/ TSIO_CH14	LCD_P21/ ADC0_SE15/ TSIO_CH14	PTC1/ LLWU_P6	SPI0_PCS3	UART1_RTS_b	FTM0_CH0		I2S0_TXD0	LCD_P21	
C8	72	PTC2	LCD_P22/ ADC0_SE4b/ CMP1_IN0/ TSIO_CH15	LCD_P22/ ADC0_SE4b/ CMP1_IN0/ TSIO_CH15	PTC2	SPI0_PCS2	UART1_CTS_b	FTM0_CH1		I2S0_TX_FS	LCD_P22	
B8	73	PTC3/ LLWU_P7	LCD_P23/ CMP1_IN1	LCD_P23/ CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	I2S0_TX_BCLK	LCD_P23	
—	74	VSS	VSS	VSS								
A11	75	VLL3	VLL3	VLL3								
A10	76	VLL2	VLL2	VLL2								
A9	77	VLL1	VLL1	VLL1								
B11	78	VCAP2	VCAP2	VCAP2								
C11	79	VCAP1	VCAP1	VCAP1								
A8	80	PTC4/ LLWU_P8	LCD_P24	LCD_P24	PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3		CMP1_OUT	LCD_P24	
D7	81	PTC5/ LLWU_P9	LCD_P25	LCD_P25	PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ALT2	I2S0_RXD0		CMP0_OUT	LCD_P25	
C7	82	PTC6/ LLWU_P10	LCD_P26/ CMP0_IN0	LCD_P26/ CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_EXTRG	I2S0_RX_BCLK		I2S0_MCLK	LCD_P26	
B7	83	PTC7	LCD_P27/ CMP0_IN1	LCD_P27/ CMP0_IN1	PTC7	SPI0_SIN	USB_SOF_OUT	I2S0_RX_FS			LCD_P27	

**Pinout**

121 MAP BGA	100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
A7	84	PTC8	LCD_P28/ ADC1_SE4b/ CMP0_IN2	LCD_P28/ ADC1_SE4b/ CMP0_IN2	PTC8			I2S0_MCLK			LCD_P28	
D6	85	PTC9	LCD_P29/ ADC1_SE5b/ CMP0_IN3	LCD_P29/ ADC1_SE5b/ CMP0_IN3	PTC9			I2S0_RX_ BCLK		FTM2_FLT0	LCD_P29	
C6	86	PTC10	LCD_P30/ ADC1_SE6b	LCD_P30/ ADC1_SE6b	PTC10	I2C1_SCL		I2S0_RX_FS			LCD_P30	
C5	87	PTC11/ LLWU_P11	LCD_P31/ ADC1_SE7b	LCD_P31/ ADC1_SE7b	PTC11/ LLWU_P11	I2C1_SDA		I2S0_RXD1			LCD_P31	
B6	—	PTC12	LCD_P32	LCD_P32	PTC12		UART4_RTS_ b				LCD_P32	
A6	—	PTC13	LCD_P33	LCD_P33	PTC13		UART4_CTS_ b				LCD_P33	
A5	—	PTC14	LCD_P34	LCD_P34	PTC14		UART4_RX				LCD_P34	
—	88	VSS	VSS	VSS								
—	89	VDD	VDD	VDD								
D5	90	PTC16	LCD_P36	LCD_P36	PTC16		UART3_RX				LCD_P36	
C4	91	PTC17	LCD_P37	LCD_P37	PTC17		UART3_TX				LCD_P37	
B4	92	PTC18	LCD_P38	LCD_P38	PTC18		UART3_RTS_ b				LCD_P38	
A4	—	PTC19	LCD_P39	LCD_P39	PTC19		UART3_CTS_ b				LCD_P39	
D4	93	PTD0/ LLWU_P12	LCD_P40	LCD_P40	PTD0/ LLWU_P12	SPI0_PCS0	UART2_RTS_ b				LCD_P40	
D3	94	PTD1	LCD_P41/ ADC0_SE5b	LCD_P41/ ADC0_SE5b	PTD1	SPI0_SCK	UART2_CTS_ b				LCD_P41	
C3	95	PTD2/ LLWU_P13	LCD_P42	LCD_P42	PTD2/ LLWU_P13	SPI0_SOUT	UART2_RX				LCD_P42	
B3	96	PTD3	LCD_P43	LCD_P43	PTD3	SPI0_SIN	UART2_TX				LCD_P43	
A3	97	PTD4/ LLWU_P14	LCD_P44	LCD_P44	PTD4/ LLWU_P14	SPI0_PCS1	UART0_RTS_ b	FTM0_CH4		EWM_IN	LCD_P44	
A2	98	PTD5	LCD_P45/ ADC0_SE6b	LCD_P45/ ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_ b/ UART0_COL_ b	FTM0_CH5		EWM_OUT_b	LCD_P45	
B2	99	PTD6/ LLWU_P15	LCD_P46/ ADC0_SE7b	LCD_P46/ ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6		FTM0_FLT0	LCD_P46	
A1	100	PTD7	LCD_P47	LCD_P47	PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1	LCD_P47	
F3	—	NC	NC	NC								
K7	—	NC	NC	NC								
J9	—	NC	NC	NC								
J10	—	NC	NC	NC								
H10	—	NC	NC	NC								
H11	—	NC	NC	NC								
F11	—	NC	NC	NC								

121 MAP BGA	100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
B5	—	NC	NC	NC								
B1	—	NC	NC	NC								
C2	—	NC	NC	NC								
C1	—	NC	NC	NC								
D2	—	NC	NC	NC								
D1	—	NC	NC	NC								
E1	—	NC	NC	NC								

## 8.2 K51 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

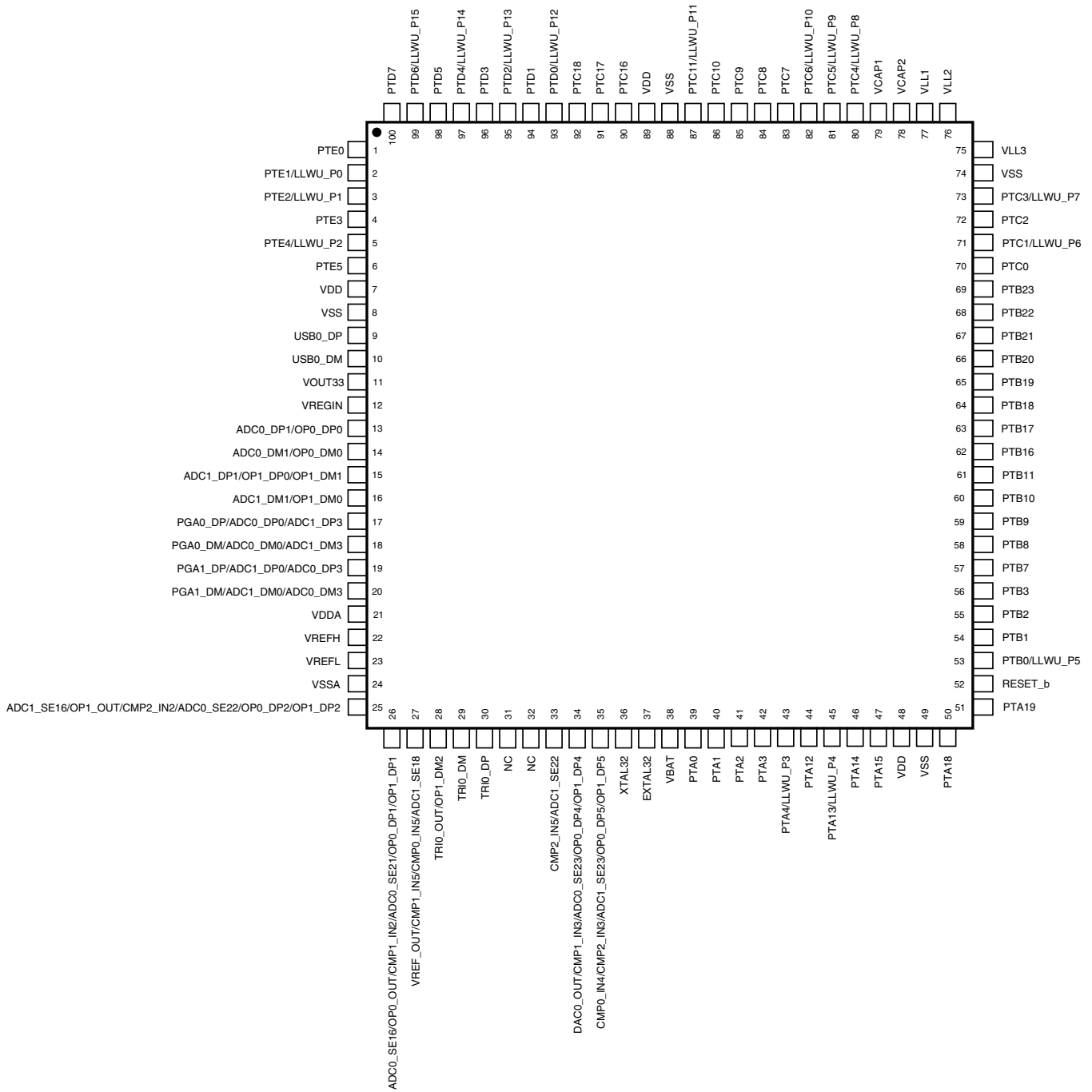


Figure 27. K51 100 LQFP Pinout Diagram



	1	2	3	4	5	6	7	8	9	10	11	
A	PTD7	PTD5	PTD4/ LLWU_P14	PTC19	PTC14	PTC13	PTC8	PTC4/ LLWU_P8	VLL1	VLL2	VLL3	A
B	NC	PTD6/ LLWU_P15	PTD3	PTC18	NC	PTC12	PTC7	PTC3/ LLWU_P7	PTC0	PTB16	VCAP2	B
C	NC	NC	PTD2/ LLWU_P13	PTC17	PTC11/ LLWU_P11	PTC10	PTC6/ LLWU_P10	PTC2	PTB19	PTB11	VCAP1	C
D	NC	NC	PTD1	PTD0/ LLWU_P12	PTC16	PTC9	PTC5/ LLWU_P9	PTC1/ LLWU_P6	PTB18	PTB10	PTB8	D
E	NC	PTE2/ LLWU_P1	PTE1/ LLWU_P0	PTE0	VDD	VDD	VDD	PTB23	PTB17	PTB9	PTB7	E
F	USB0_DP	USB0_DM	NC	PTE3	VDDA	VSSA	VSS	PTB22	PTB21	PTB20	NC	F
G	VOUT33	VREGIN	VSS	PTE5	VREFH	VREFL	VSS	PTB3	PTB2	PTB1	PTB0/ LLWU_P5	G
H	ADC0_DP1/ OP0_DP0	ADC0_DM1/ OP0_DM0	ADC0_SE16/ OP0_OUT1/ ADC0_SE21/ OP0_DP1/ OP1_DP1	TRIO_DM	NC	CMP2_IN5/ ADC1_SE22	PTE4/ LLWU_P2	PTA1	PTA3	NC	NC	H
J	ADC1_DP1/ OP1_DP0/ OP1_DM1	ADC1_DM1/ OP1_DM0	ADC1_SE16/ OP1_OUT1/ CMP2_IN2/ ADC0_SE22/ OP0_DP2/ OP1_DP2	TRIO_DP	NC	PTA0	PTA2	PTA4/ LLWU_P3	NC	NC	RESET_b	J
K	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DM/ ADC0_DM0/ ADC1_DM3	TRIO_OUT/ OP1_DM2	CMP0_IN4/ ADC1_SE23/ OP0_DP5/ OP1_DP5	DAC0_OUT/ CMP1_IN3/ ADC0_SE23/ OP0_DP4/ OP1_DP4	VBAT	NC	PTA12	PTA14	VSS	PTA19	K
L	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DM/ ADC1_DM0/ ADC0_DM3	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	XTAL32	EXTAL32	VSS	RTC WAKEUP_B	PTA13/ LLWU_P4	PTA15	VDD	PTA18	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 28. K51 121 MAPBGA Pinout Diagram

## 9 Revision History

The following table provides a revision history for this document.

**Table 52. Revision History**

Rev. No.	Date	Substantial Changes
1	3/2012	Initial public release

Table continues on the next page...

**Table 52. Revision History (continued)**

Rev. No.	Date	Substantial Changes
2	4/2012	<ul style="list-style-type: none"> <li>• Replaced TBDs throughout.</li> <li>• Updated "Power consumption operating behaviors" table.</li> <li>• Updated "ADC electrical specifications" section.</li> <li>• Updated "VREF full-range operating behaviors" table.</li> <li>• Updated "I2S/SAI Switching Specifications" section.</li> <li>• Updated "TSI electrical specifications" table.</li> </ul>
3	11/2012	<ul style="list-style-type: none"> <li>• Updated orderable part numbers.</li> <li>• Updated the maximum input voltage (<math>V_{ADIN}</math>) specification in the "16-bit ADC operating conditions" section.</li> <li>• Updated the maximum <math>I_{DDstby}</math> specification in the "USB VREG electrical specifications" section.</li> </ul>