DC to 45GHz Broadband MMIC Low-Noise Amplifier

Features

- Integrated PLFX technology:
  - Allows use of less-expensive coil
- Very low power dissipation:
  - 4.5V, 85mA (383mW)
  - High drain efficiency (40dBm/W)
- Excellent 18-40GHz performance:
  - 11 ± 0.25dB gain, 15.5dBm Psat
  - 4dB noise figure
- Broadband 45GHz performance:
  - 11 ± 1.75dB gain, 14.5dBm Psat
- >30dB dynamic gain control
- Integrated temperature-referenced power detector output
- 100% DC, RF, and visually tested
- Size: 1640x920um (64.6x36.2mil)
- ECCN 3A001.b.2.d

Description

The MMA030AA is a seven stage traveling wave amplifier. The amplifier features Microsemi PLFX (Passive Low Frequency eXtension) circuitry designed to reduce the integration cost of the amplifier. PLFX isolates the amplifier from bias inductor resonances, allowing use of a less-expensive coil.

Application

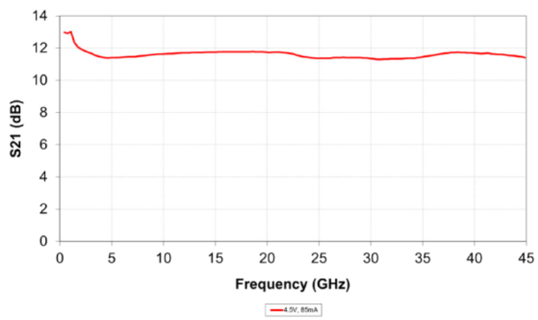
The MMA030AA Broadband MMIC Low-Noise Amplifier with PLFX is designed for high efficiency and low-noise broadband applications in RF and microwave communications, test equipment and military systems. By using specific external components, the bandwidth of operation can be extended below 40MHz.

Key Characteristics: Vdd=4.5V, Idd=85mA, Zo=50Ω
Specifications pertain to wafer measurements with RF probes and DC bias cards @ 25°C

		18 - 40GHz			1.5 - 40GHz			0.04 - 45GHz		
Parameter	**Description**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
S21 (dB)	Small Signal Gain	9.5	11	-	9.5	11	-	9.5	11	-
Flatness (±dB)	Gain Flatness	-	0.25	0.75	-	0.5	1.25	-	1.25	1.75
S11 (dB)	Input Match	-	-12	-10	-	-12	-10	-	-12	-10
S22 (dB)	Output Match	-	-14	-11	-	-13	-10	-	-11	-8
S12 (dB)	Reverse Isolation	-	-18	-15	-	-18	-15	-	-17	-15
P1dB (dBm)	1dB Compressed Output Power	11.5	13	-	11.5	13	-	10	11.5	-
Psat (dBm)	Saturated Output Power	14	15.5	-	14	15.5	-	13	14.5	-
NF (dB)	Noise Figure	-	4	-	-	4.5	-	-	4.5	-
RF_{det} (mV/mW)	RF Detector Sensitivity	-	0.5	-	-	0.5	-	-	0.5	-

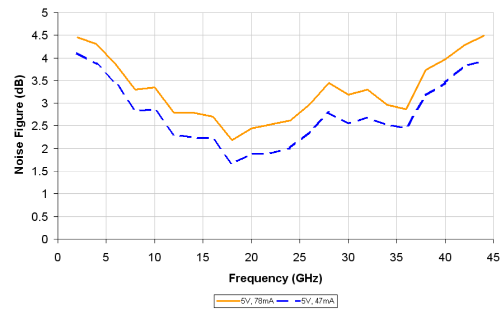
Supplemental Specifications

S21



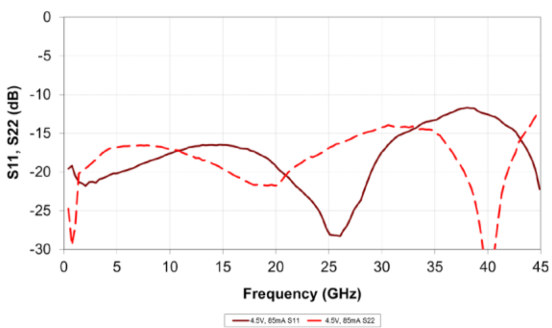
Typical IC performance measured on-wafer

Noise Figure



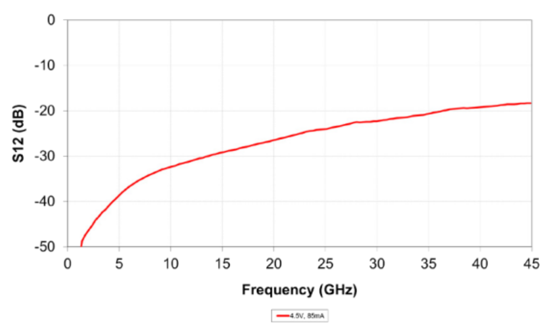
Typical IC performance with package de-embedded

S11, S22



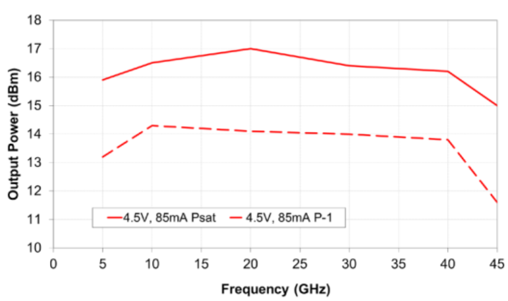
Typical IC performance measured on-wafer

S12



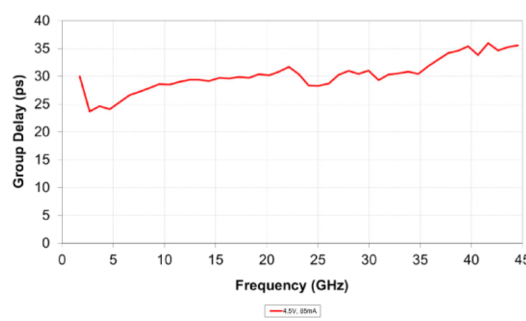
Typical IC performance measured on-wafer

Output Power



Typical IC performance measured on-wafer

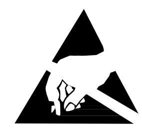
Group Delay



Typical IC performance measured on-wafer

Table 1: Supplemental Specifications

Parameter	Description	Min	Typ	Max
Vdd	Drain Bias Voltage	3V	4.5V	7.5V
Idd	Drain Bias Current	-	85mA	120mA
Vg1	1st Gate Bias Voltage	-4V	-	+0.5V
Vg2	2nd Gate Bias Voltage	Vdd - Vg2 < 7V	N/C	+4V
P_{in}	Input Power (CW)	-	-	20dBm
P_{dc}	Power Dissipation	-	0.383W	-
T_{ch}	Channel Temperature	-	-	150˚C
Θ_{ch}	Thermal Resistance (T_{case}=85˚C)	-	22˚ C/W	-



Caution, ESD
Sensitive Device

DC Bias:
The MMA030AA features a patented on-chip passive bias circuit called ‘PLFX’. This circuit isolates the amplifier from bias coil resonances above 14GHz, allowing the use of less expensive coils; traditional biasing requires bias coils with self-resonances outside the operating range of the amplifier.

The device is biased by applying a positive voltage to the drain (Vdd), then setting the drain current (Idd) using a negative voltage on the gate (Vg1). The nominal bias is Vdd=4.5V, Idd=85mA.

Improved performance can be achieved with gate bias adjustment; use the drain termination bypass to alter the output voltage (detected at drain voltage sense).

Gain Control:
Dynamic gain control is available when operating the amplifier in the linear gain region. Negative voltage applied to the second gate (Vg2) reduces amplifier gain.

RF Power Detection:
RF output power can be calculated from the difference between the RF detector voltage and the DC detector voltage, minus a DC offset. Please consult the application note available on the Microsemi website.

Low-Frequency Use:
The MMA030AA has been designed so that the bandwidth can be extended to low frequencies. The low end corner frequency of the device is primarily determined by the external biasing and AC coupling circuitry.

Matching:
The amplifier incorporates on- chip termination resistors on the RF input and output. These resistors are RF grounded through on-chip capacitors, which are small and become open circuits at frequencies below 1GHz.

A pair of gate and drain termination bypass pads are provided for connecting external capacitors required for the low frequency extension network. These capacitors should be 10x the value of the DC blocking capacitors.

DC Blocks:
The amplifier is DC coupled to the RF input and output pads; DC voltage on these pads must be isolated from external circuitry.

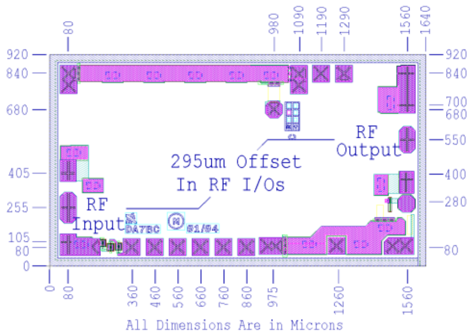
For operation above 2GHz, a series DC-blocking capacitor with minimum value of 20pF is recommended; operation above 40MHz requires a minimum of 120pF.

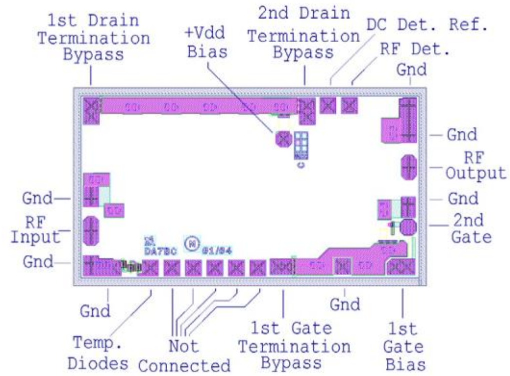
Bias Inductor:
DC bias applied to the drain (Vdd) must be decoupled with an off-chip RF choke inductor. The amount of bias inductance will determine the low frequency operating point. Inductive biasing can also be applied to the chip through the RF output.

For many applications above 2GHz, a bondwire from the Vdd pad will suffice as the biasing inductor.

Die size, pad locations, and pad descriptions

Chip size: 1640x920um (64.6x36.2mil)
Chip size tolerance: ±5um (0.2mil)
Chip thickness: 100 ±10um (4 ±0.4mil)
Pad dimensions: 80x80um (3.1x3.1mil)





Pick-up and Chip Handling:

This MMIC has exposed air bridges on the top surface. Do not pick up chip with vacuum on the die center; handle from edges or with a custom collet.

Thermal Heat Sinking:

To avoid damage and for optimum performance, you must observe the maximum channel temperature and ensure adequate heat sinking.

ESD Handling and Bonding:

This MMIC is ESD sensitive; preventive measures should be taken during handling, die attach, and bonding.

Epoxy die attach is recommended. Please review our application note MM-APP-0001 handling and die attach recommendations, on our website for more handling, die attach and bonding information.