

MMA041PP5 Datasheet

DC–25 GHz GaAs MMIC Distributed Low-Noise Amplifier



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Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

Revision 2.0 is the second publication of this document released December 2018.

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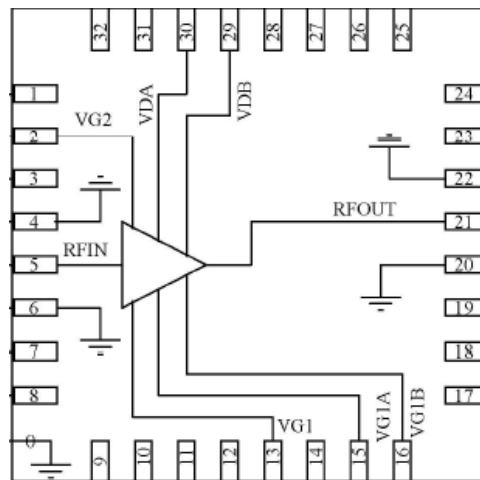
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2 Product Overview

MMA041PP5 is a gallium arsenide (GaAs) monolithic microwave integrated circuit (MMIC) pseudomorphic high-electron-mobility transistor (pHEMT) distributed low noise amplifier in a leadless 5 mm × 5 mm surface-mount package that operates between DC and 25 GHz. It is ideal for test instrumentation, wideband military and space applications. The amplifier provides a flat gain of 17 dB, 2.5 dB noise figure, and 21 dBm of output power at 1 dBm gain compression while requiring only 150 mA from a 7 V supply. Output IP3 is typically 35 dBm. The MMA041PP5 amplifier features RF I/Os that are internally matched to 50 Ω. It is also available in die form as the MMA041AA.

The following image shows the primary functional blocks of the MMA041PP5 device.

Figure 1 Functional Block Diagram



2.1 Applications

The MMA041PP5 device is designed for the following applications:

- Test and measurement instrumentation
- Military and space
- Wideband microwave radios
- Microwave and millimeter-wave communication systems

2.2 Key Features

The following are key features of the MMA041PP5 device:

- Frequency range: DC to 25 GHz
- High gain: 18 dB
- High output IP3: 35 dBm
- Low noise figure: 2.5 dB at 10 GHz
- Supply voltage: 7 V at 150 mA
- 50 Ω matched I/O
- 32-lead 5 mm × 5 mm × 1.2 mm plastic QFN package

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The following table shows the absolute maximum ratings at 25 °C unless otherwise specified.

Table 1 Absolute Maximum Ratings

Parameter	Rating
Storage temperature	–65 to 150 °C
Operating temperature	–55 to 85 °C
Drain bias voltage, (V_{DD})	8 V
First gate bias voltage, (V_{G1})	–2 to 0.5 V
Second gate bias voltage, (V_{G2})	$V_{DD} \pm 20\%$
V_D current (I_{DD})	300 mA
RF input power	19 dBm
DC power dissipation ($T = 85$ °C)	2.4 W
Channel temperature	150 °C
Thermal impedance	18 °C/W

3.2 Typical Electrical Performance

The following table lists the specified electrical performance of the MMA041PP5 device at 25 °C, where VDD is 7 V, IDD is 150 mA, and VGG is –0.4 V.

Table 2 Specified Electrical Performance

Parameter	Frequency Range	Min	Typ	Max	Units
Operational frequency range					
Gain	DC-6 GHz	17	18		dB
	6 GHz-12 GHz	16	17.5		dB
	12 GHz-20 GHz	15	17		dB
Gain flatness	4 GHz-12 GHz		± 0.5		dB
	12 GHz-20 GHz		± 0.5		dB
Noise figure @5V 150mA	DC-6 GHz		2.7		dB
	6 GHz-12 GHz		2		dB
	12 GHz-20 GHz		2.5		dB
Input return loss	DC-6 GHz		15		dB
	6 GHz-12 GHz		18		dB
	12 GHz-20 GHz		13		dB
Output return loss	DC-6 GHz		13		dB
	6 GHz-12 GHz		18		dB
	12 GHz-20 GHz		16		dB
P1dB	DC-6 GHz		21		dBm
	6 GHz-12 GHz	21	22		dBm
	12 GHz-20 GHz	17	19		dBm
Psat	DC-6 GHz		24		dBm
	6 GHz-12 GHz		24		dBm
	12 GHz-20 GHz		21		dBm
OIP3	DC-6 GHz		35		dBm
	6 GHz-12 GHz		36		dBm
	12 GHz-20 GHz		34		dBm
V _{DD} (drain voltage supply)			7		V
I _{DD} (drain current)			150		mA
V _{GG} (gate voltage supply)		-1.0	-0.4	0	V

3.3 Typical Performance Curves

The following graphs show the typical performance curves of the MMA041PP5 device at 25 °C, unless otherwise indicated.

Figure 2 Gain vs. Temperature ($V_{DD} = 7V$, $I_{DD} = 150mA$)

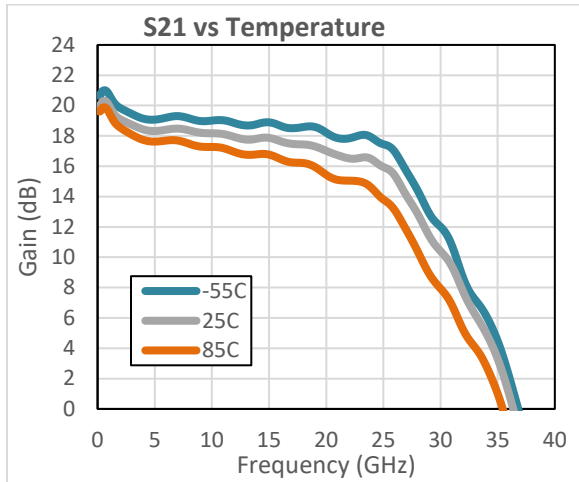


Figure 4 Gain vs I_{DD} ($V_{DD} = 7V$, $T = 25^{\circ}C$)

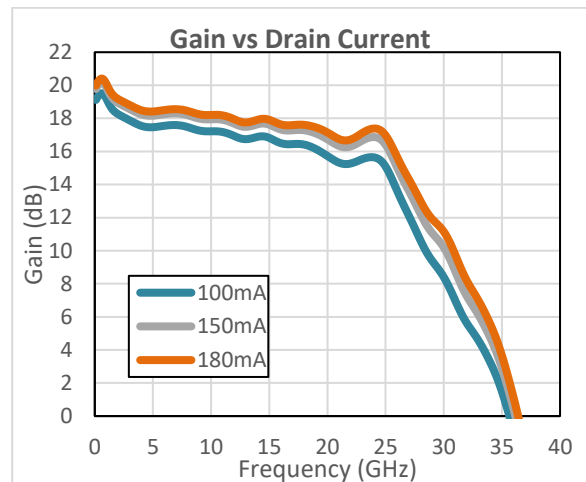


Figure 3 Gain vs V_{DD} ($I_{DD} = 150mA$, $T = 25^{\circ}C$)

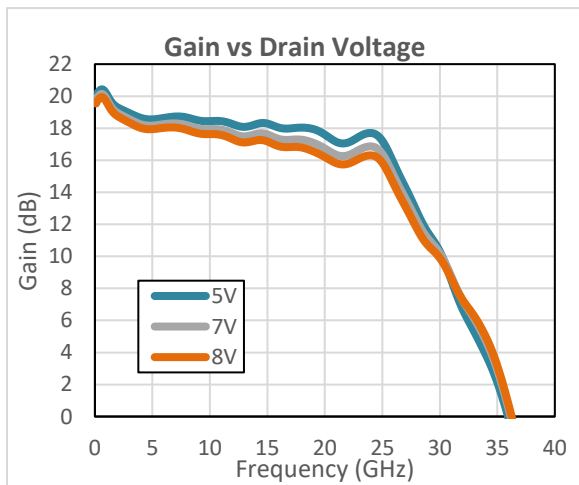


Figure 5 S_{11} vs Temperature ($V_{DD} = 7V$, $I_{DD} = 150mA$)

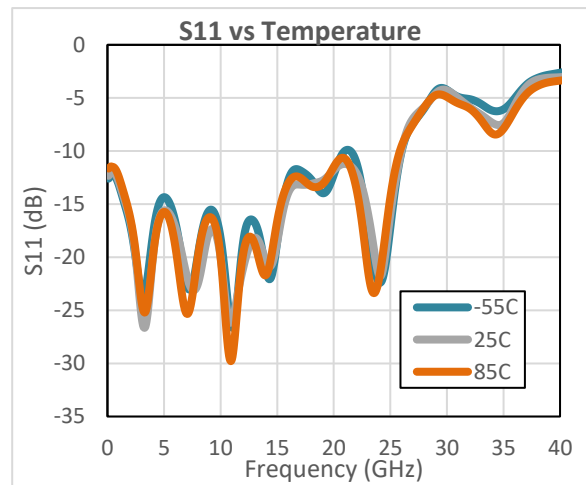


Figure 6 S_{22} vs Temperature ($V_{DD} = 7V$, $I_{DD} = 150mA$)

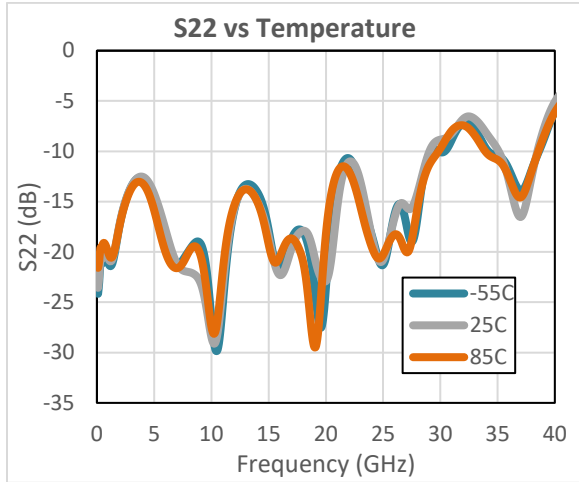


Figure 9 Noise Figure vs Drain Current ($V_{DD} = 7V$, $T = 25^\circ C$)

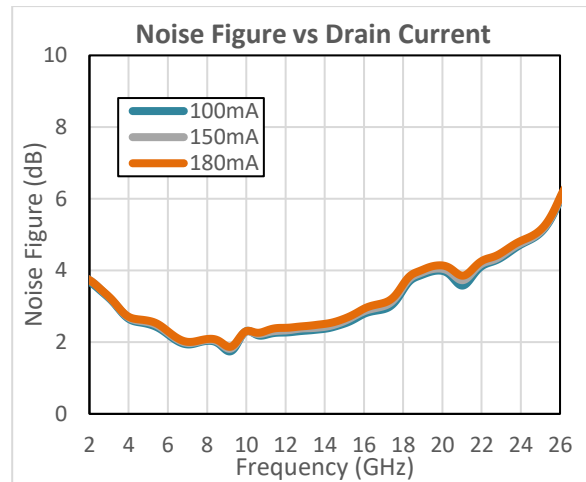


Figure 7 Noise Figure vs. Temperature ($V_{DD} = 7V$, $I_{DD} = 150mA$)

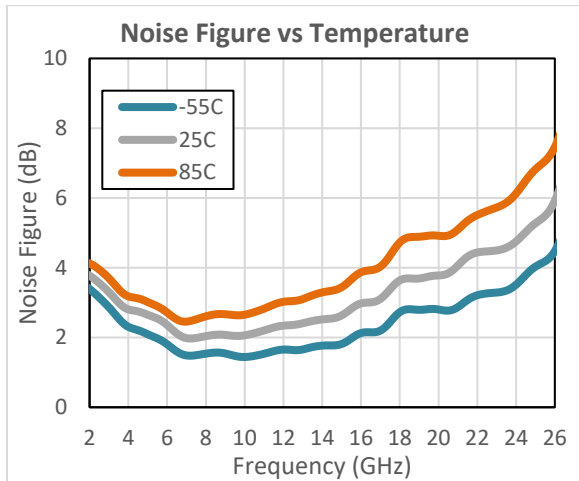


Figure 10 P1dB vs V_{DD} ($I_{DD} = 150mA$, $T = 25^\circ C$)

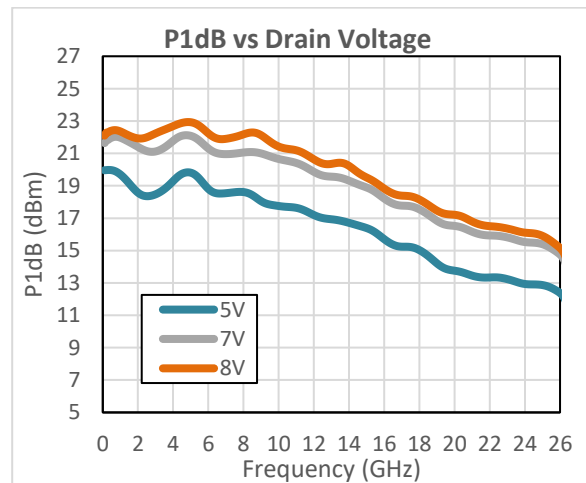


Figure 8 NF vs Drain Voltage ($I_{DD} = 150mA$, $T = 25^\circ C$)

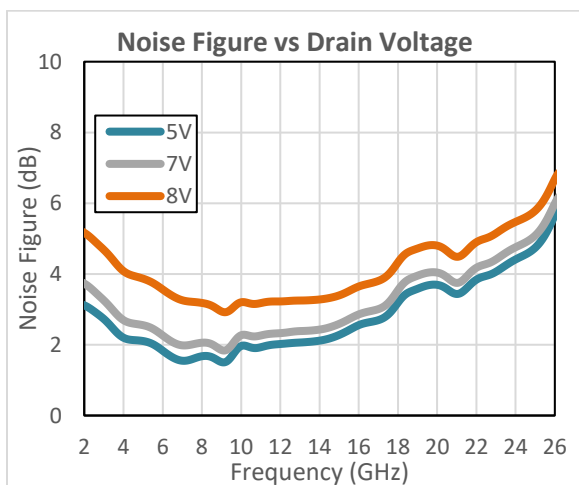


Figure 11 P1dB vs. Temperature ($V_{DD} = 7V$, $I_{DD} = 150mA$)

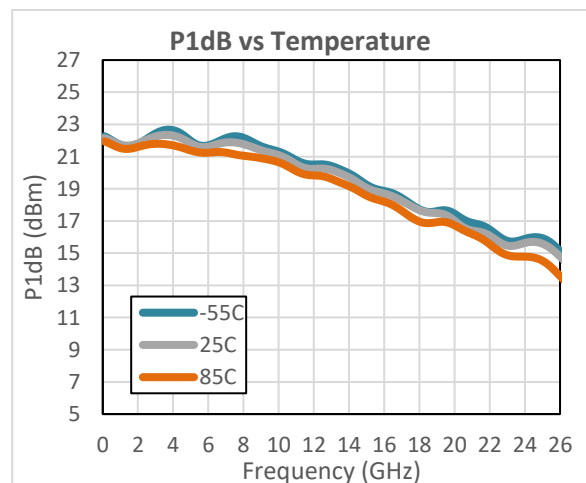


Figure 12 P3dB vs V_{DD} (I_{DD} = 150mA, T = 25°C)

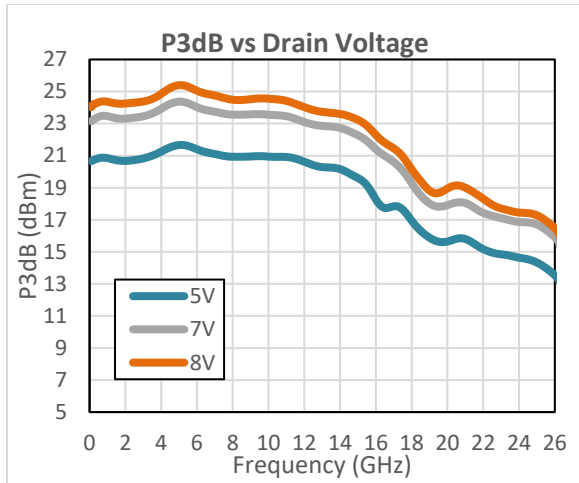


Figure 15 OIP3 vs V_{DD} (I_{DD} = 150mA, T = 25°C, P_{out} = 5dBm)

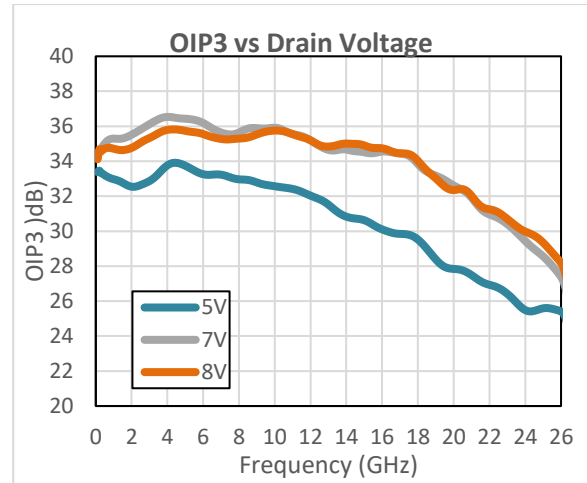


Figure 13 P3dB vs. Temperature (V_{DD} = 7V, I_{DD} = 150mA)

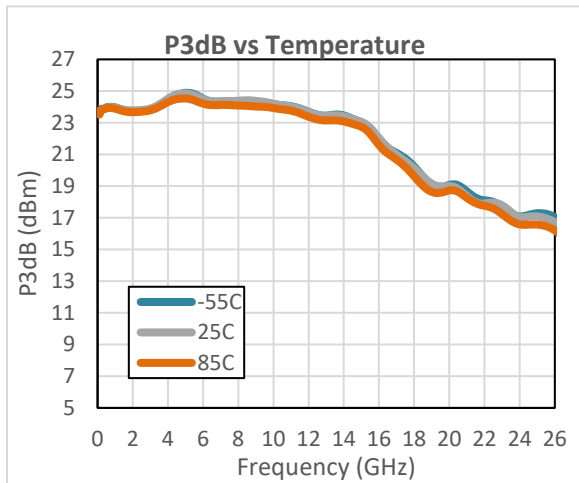


Figure 16 OIP3 vs. Current (V_{DD} = 7V, T = 25°C, P_{out} = 5dBm)

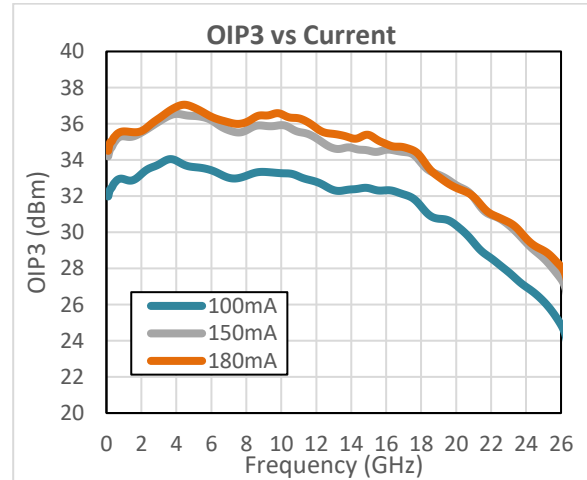
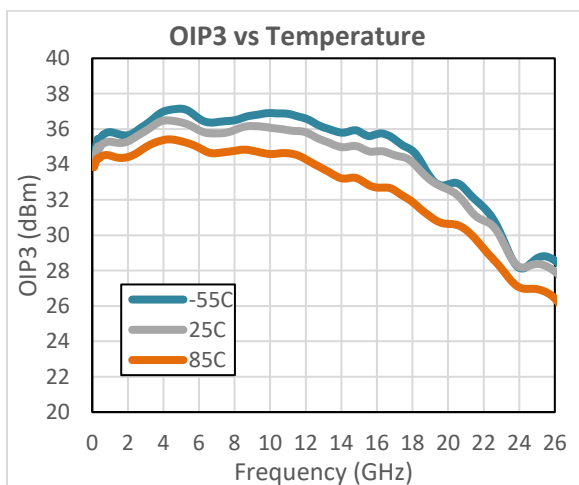


Figure 14 OIP3 vs. Temp (V_{DD} = 7V, I_{DD} = 150mA, P_{out} = 5dBm)



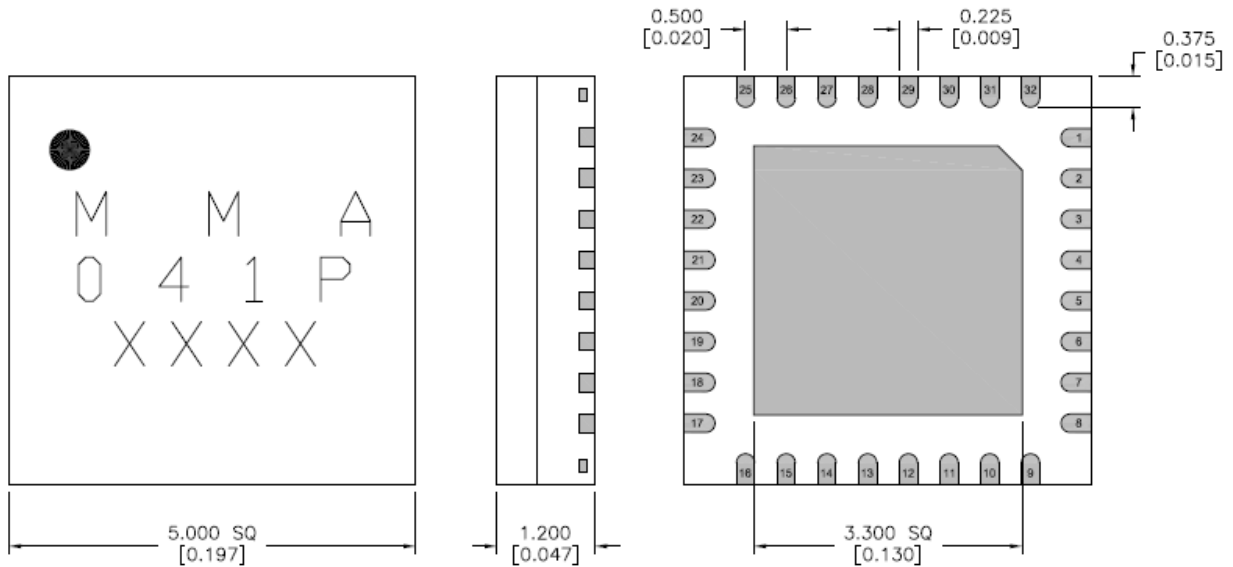
4 Package Specification

This section details the package specifications of the MMA041PP5 device.

4.1 Package Outline Drawing

The following illustration shows the package outline of the MMA041PP5 device. Dimensions are in millimeters [inches].

Figure 15 Outline Package



4.2 Packaging Information

The following table shows the chip outline of the MMA041PP5 device. For additional packaging information, contact your Microsemi sales representative.

Table 3 Packaging Information

Part Number	Package Body Material	Lead Finish
MMA041PP5	Low-stress injection molded plastic	Ni/Pd/Au

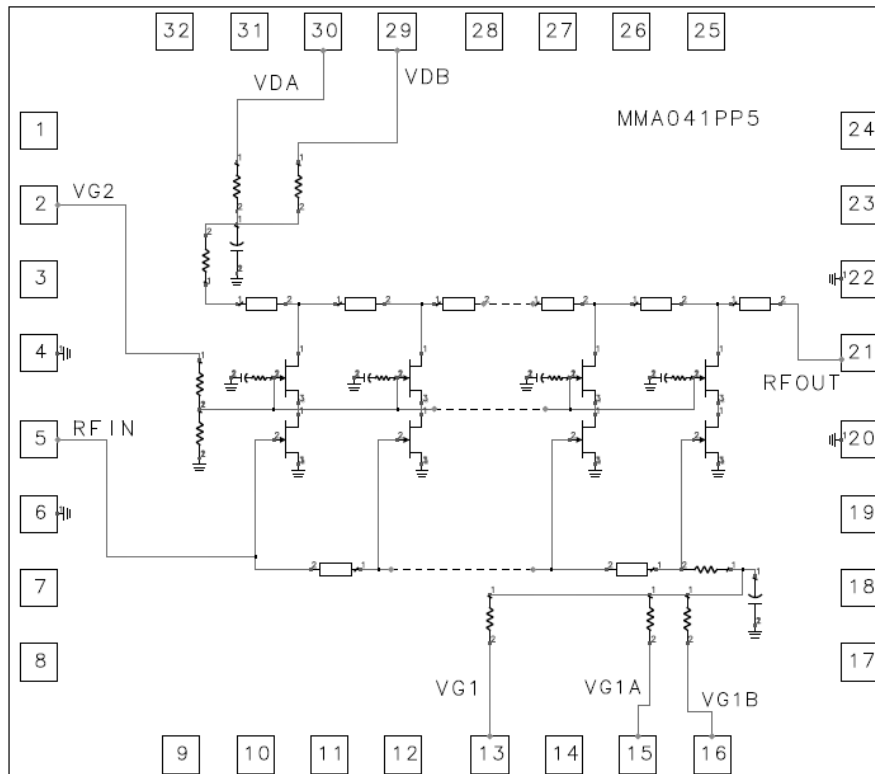
4.3 Pin Descriptions

The following table describes the pins of the MMA041PP5 device.

Table 4 Pin Description

Pin Number	Pin Name	Description
2	V _{G2}	DC couple to V _{DA} externally for nominal operation.
5	RF _{IN}	This pin is matched to 50 Ω. (Optional V _{G1} can be biased on this line.)
13	V _{G1}	First gate bias. Adjust to achieve required I _{DD} .
15, 16	V _{G1A} , V _{G1B}	Low-frequency termination. Connect bypass capacitors per application circuit below. (no bias necessary)
21	RF _{OUT} +V _{DD}	This pin is matched to 50 Ω and is used to bias V _{DD} .
29, 30	V _{DB} , V _{DA}	Low-frequency termination. Connect bypass capacitors per application circuit below. (no bias necessary)
4, 6, 20, 22	GND	Ground paddle must be connected to RF/DC ground.
Backside Paddle	RF/DC GND	RF/DC ground.
1, 3, 7, 8, 9, 10, 11, 12, 14, 17, 18, 19, 23, 24, 25, 26, 27, 28, 31, 32	N/C	These pins are not connected internally. All data was measured with these pins connected to RF/DC ground externally.

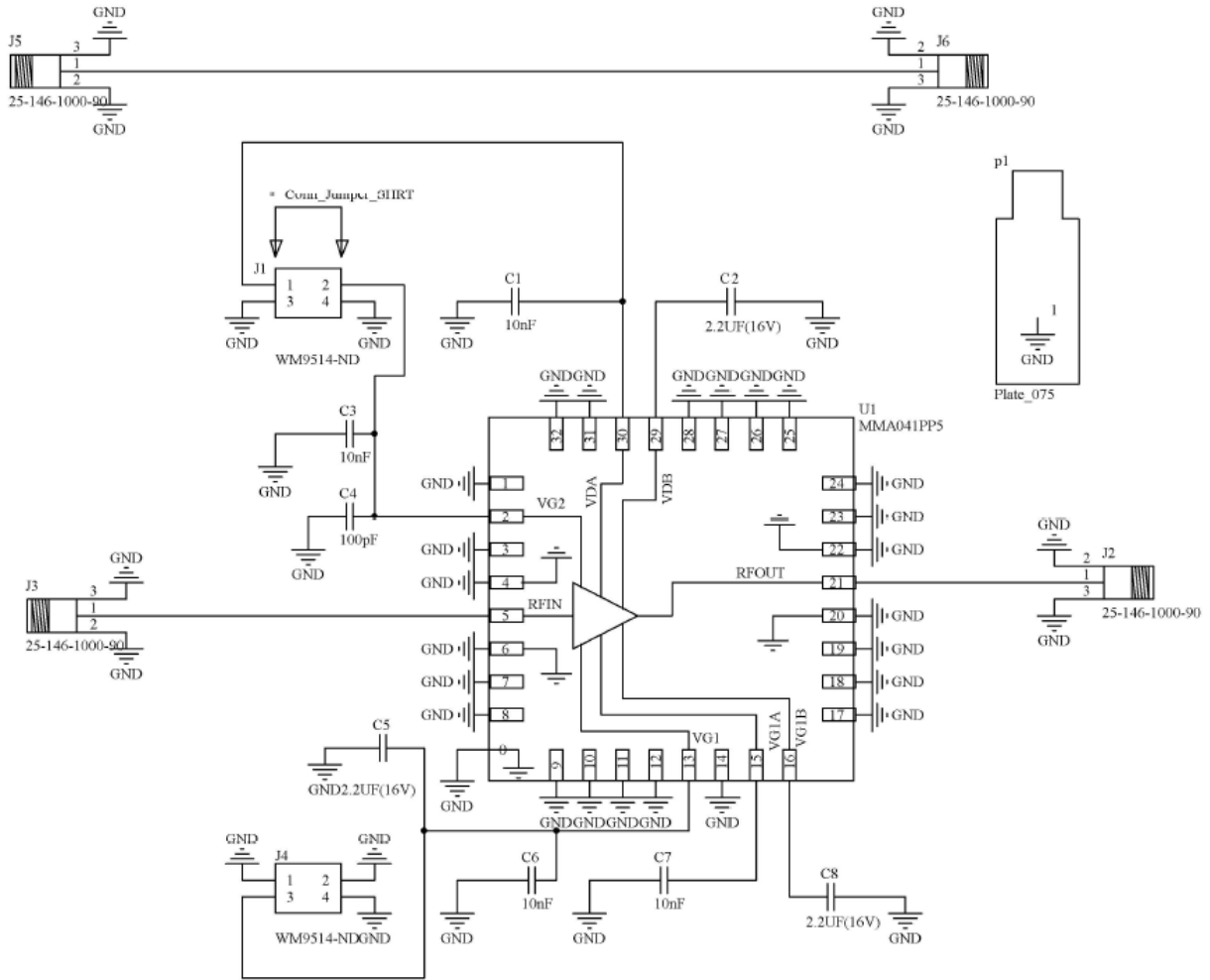
Figure 17 Functional Block Diagram



4.4 Application Circuit

The following illustration shows the application circuit of the MMA041PP5 device.

Figure 18 Application Circuit



5 Handling Recommendations

Gallium arsenide integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Microsemi application note [AN01 GaAs MMIC Handling and Die Attach Recommendations](#).

6 Evaluation Board Information

The following image shows the evaluation board of the MMA041PP5 device.

Figure 19 Evaluation Board

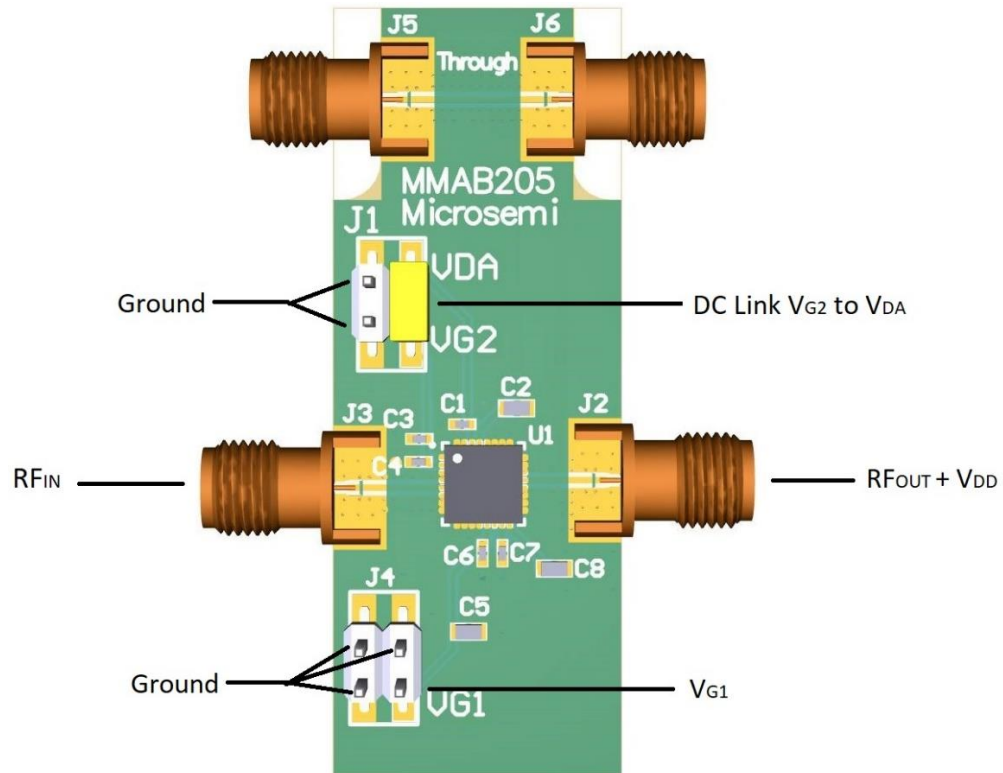


Table 5 Bias Sequence

Bias Sequence	
1)	Set the gate voltage VG1 to -1V
2)	Set drain voltage VDD to 7V
3)	Adjust the gate voltage until the drain current is 150mA

The following table shows the list of materials for the evaluation PCB MMA041PP5E.

Table 6 List of Materials for Evaluation PCB MMA041PP5e

Item	Description
C1, C3, C6, C7	CAP 10 nF 50 V –20% to +80% 0402
C2, C5, C8	2.2 μ F 16 V ceramic capacitor X5R 0603
C4	CAP 100 pF 50 V \pm 10% 0402
J1, J4	Header, 2-pin, dual row
J2, J3, J5, J6	CONN 2.9 mm female PCB edge mount .012 pin