

MMA053PP5 Datasheet

DC–10 GHz 1 W GaAs MMIC pHEMT Distributed Power Amplifier



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Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 is the first publication of this document.

Contents

Revision History.....	3
1.1 Revision 1.0.....	3
2 Product Overview	7
The following figure is a functional block diagram for the MMA053PP5 device.....	7
2.1 Applications	7
2.2 Key Features.....	7
3 Electrical Specifications.....	8
3.1 Absolute Maximum Ratings	8
3.2 Typical Electrical Performance	9
3.3 Typical Performance Curves.....	10
4 Package Specification	13
4.1 Package Outline Drawing	13
4.2 Packaging Information	13
4.3 Pin Descriptions	14
4.4 Application Circuit.....	16
5 Handling Recommendations.....	17
6 Evaluation Board Information.....	18

List of Figures

Figure 1 Functional Block Diagram	7
Figure 2 Gain vs V_{DD} ($I_{DD} = 420\text{mA}$, $T = 25\text{ }^\circ\text{C}$)	10
Figure 3 Gain vs I_{DD} ($V_{DD} = 10\text{ V}$, $T = 25\text{ }^\circ\text{C}$)	10
Figure 4 Gain vs Temperature ($V_{DD} = 10\text{ V}$, $I_{DD} = 420\text{mA}$)	10
Figure 5 S_{11} vs Temperature ($V_{DD} = 10\text{ V}$, $I_{DD} = 420\text{mA}$)	10
Figure 6 S_{22} vs Temperature ($V_{DD} = 10\text{ V}$, $I_{DD} = 420\text{mA}$)	11
Figure 7 Noise Figure vs Temperature ($V_{DD}=10\text{ V}$, $I_{DD}=420\text{mA}$)	11
Figure 8 Noise Figure vs I_{DD} ($I_{DD} = 420\text{mA}$, $T = 25\text{ }^\circ\text{C}$)	11
Figure 9 P1dB vs Temperature ($V_{DD} = 10\text{ V}$, $I_{DD} = 420\text{mA}$)	11
Figure 10 P1dB vs V_{DD} ($I_{DD} = 420\text{mA}$, $T = 25\text{ }^\circ\text{C}$)	11
Figure 11 P3dB vs Temperature ($V_{DD} = 10\text{ V}$, $I_{DD} = 420\text{mA}$)	11
Figure 12 P3dB vs V_{DD} ($I_{DD} = 420\text{mA}$, $T = 25\text{ }^\circ\text{C}$)	12
Figure 13 OIP3 vs Temperature ($V_{DD} = 10\text{ V}$, $I_{DD} = 420\text{mA}$, Output Power = 10dBm)	12
Figure 14 OIP3 vs I_{DD} ($V_{DD} = 10\text{ V}$, $T = 25\text{ }^\circ\text{C}$)	12
Figure 15 IM3 vs Output Power ($V_{DD} = 10\text{ V}$, $I_{DD} = 420\text{mA}$, $T = 25\text{ }^\circ\text{C}$)	12
Figure 16 Second Harmonic vs Output Power ($V_{DD} = 10\text{ V}$, $I_{DD} = 420\text{mA}$, $T = 25\text{ }^\circ\text{C}$)	12
Figure 17 Functional Schematic	15
Figure 18 Application Circuit	16
Figure 19 Evaluation Board	18



List of Tables

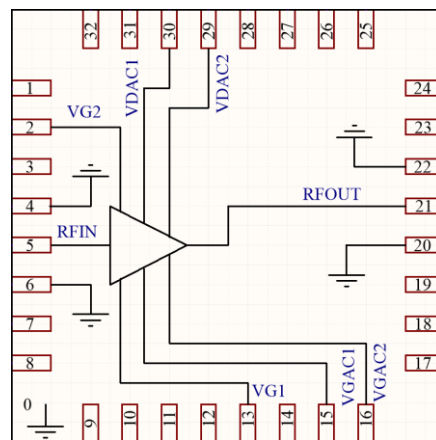
Table 1 Absolute Maximum Ratings	8
Table 2 Specified Electrical Performance	9
Table 3 Packaging Information	13
Table 4 Pin Description	14
Table 5 List of Materials for Evaluation PCB MMA053PP5E	18
Table 6 Bias Sequence	18

2 Product Overview

MMA053PP5 is a gallium arsenide (GaAs) monolithic microwave integrated circuit (MMIC) pHEMT distributed power amplifier that operates between DC and 10 GHz. The plastic packaged amplifier provides 17 dB of gain, 43 dBm output IP3, and 32 dBm of output power at 3 dB compression. Gain flatness over the 100 MHz to 10 GHz frequency range varies by only ± 1 dB, making the MMA053PP5 ideal for EW, ECM, radar, and test equipment applications. The MMA053PP5 amplifier features compact plastic SMT package size and I/Os that are internally matched to $50\ \Omega$, which is ideal for any surface mount technology (SMT) assembly equipment.

The following figure is a functional block diagram for the MMA053PP5 device.

Figure 1 Functional Block Diagram



2.1 Applications

The MMA053PP5 device is designed for the following applications:

- Military and Space
- Test instrumentation
- Telecom infrastructure
- Microwave radio and VSAT
- Microwave communications

2.2 Key Features

The following are key features of the MMA053PP5 device:

- Frequency range: DC to 10 GHz
- Gain: 17 dB
- NF: 2.8 @ 6GHz
- High P3dB output power: 32 dBm
- High OIP3: 43 dBm
- Bias VDD = 10 V/ 420 mA
- $50\ \Omega$ matched I/O
- Package size: 5mm x 5mm, 32L plastic QFN

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The following table shows the absolute maximum ratings at 25 °C unless otherwise specified. Exceeding one or any of the maximum ratings potentially could cause damage or latent defects to the device.

Table 1 Absolute Maximum Ratings

Parameter	Rating
Storage temperature	–65 to 150 °C
Operating temperature	–55 to 85 °C
Drain bias voltage, (V_{DD})	12 V
Drain bias current, (I_{DD})	500 mA
First gate bias voltage, (V_{G1})	0 V
RF input power	18 dBm
DC power dissipation ($T = 85$ °C)	6 W
Junction Channel temperature	150 °C
Thermal impedance	14 C/W

3.2 Typical Electrical Performance

The following table lists the specified electrical performance of the MMA053PP5 device at 25 °C, where V_{DD} is 10 V, I_{DD} is 420mA, and V_{GG} is –0.7 V.

Table 2 Specified Electrical Performance

Parameter	Frequency Range	Min	Typ	Max	Units
Operational frequency range		DC		10	GHz
Gain	DC-6 GHz	16	17		dB
	6-10 GHz	15	16.5		dB
Noise figure	DC-6 GHz		4		dB
	6-10 GHz		2.8	3.5	dB
Input return loss	DC-6 GHz		23	20	dB
	6-10 GHz		14	12	dB
Output return loss	DC-6 GHz		16	14	dB
	6-10 GHz		14	12	dB
P _{1dB} @ 11V, 420mA	DC-6 GHz	27	29		dBm
	6-10 GHz	26.5	29		dBm
P _{3dB} @ 11V, 420mA	DC-6 GHz	31	33		dBm
	6-10 GHz	30.5	32		dBm
OIP ₃	DC-6 GHz	42	44		dBm
	6-10 GHz	41	43		dBm
V _{DD} (drain voltage supply)			10		V
I _{DD} (drain current)			420		mA
V _{GG} (gate voltage supply)			-0.7		V

3.3 Typical Performance Curves

The following graphs show the typical performance curves of the MMA053PP5 device at 25 °C, unless otherwise indicated. These measurements were taken on the evaluation board.

Figure 2 Gain vs V_{DD} ($I_{DD} = 420\text{mA}$, $T = 25\text{ }^\circ\text{C}$)

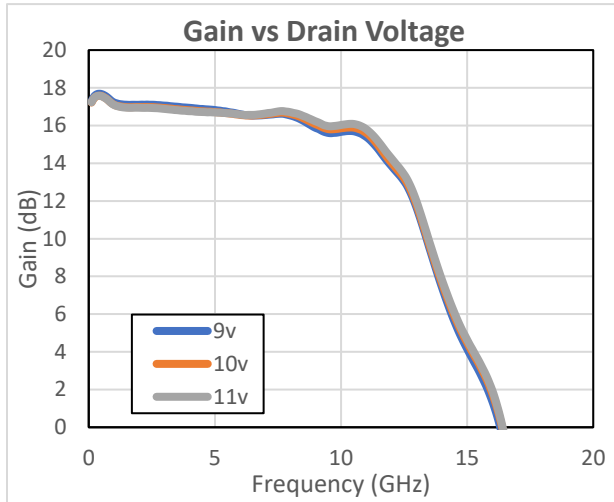


Figure 4 Gain vs Temperature ($V_{DD} = 10\text{ V}$, $I_{DD} = 420\text{mA}$)

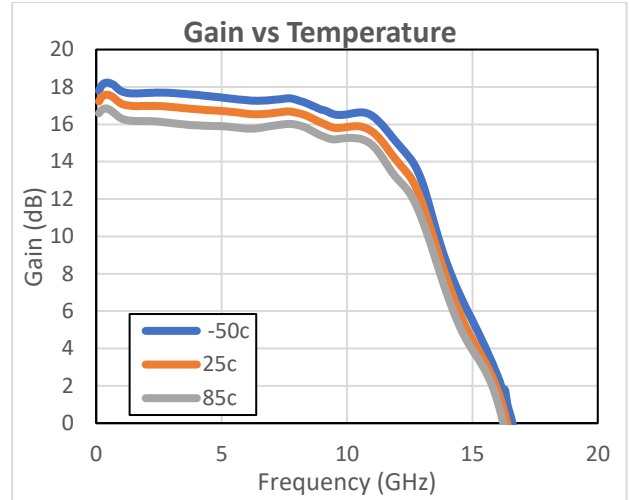


Figure 3 Gain vs I_{DD} ($V_{DD} = 10\text{ V}$, $T = 25\text{ }^\circ\text{C}$)

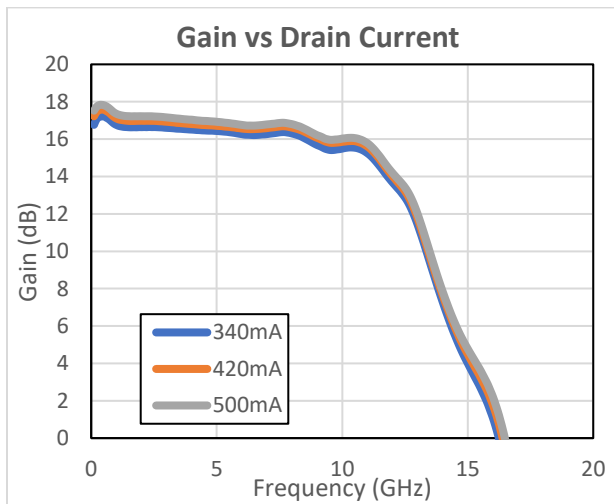


Figure 5 S_{11} vs Temperature ($V_{DD} = 10\text{ V}$, $I_{DD} = 420\text{mA}$)

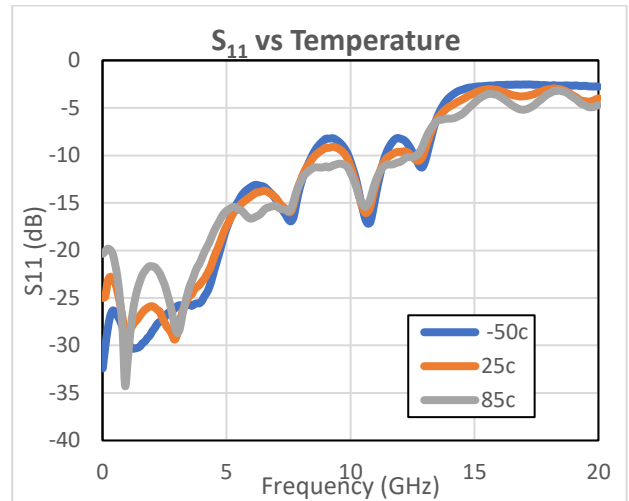


Figure 6 S_{22} vs Temperature ($V_{DD} = 10\text{ V}$, $I_{DD} = 420\text{mA}$)

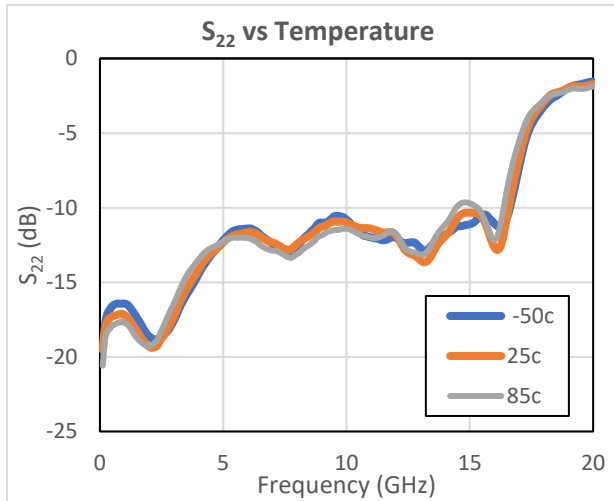


Figure 9 P1dB vs Temperature ($V_{DD} = 10\text{ V}$, $I_{DD} = 420\text{mA}$)

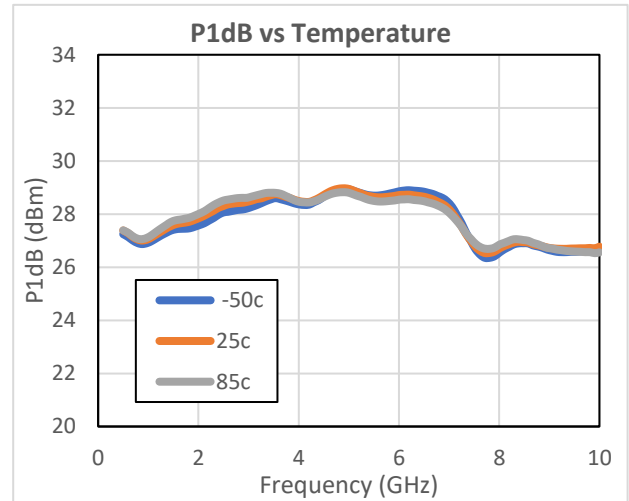


Figure 7 Noise Figure vs Temperature ($V_{DD}=10\text{ V}$, $I_{DD}=420\text{mA}$)

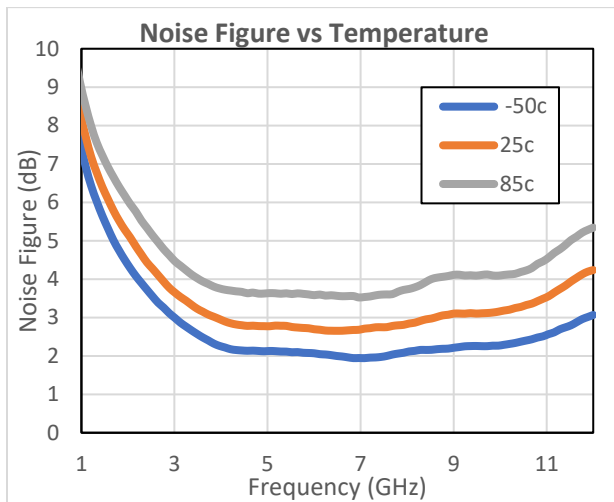


Figure 10 P1dB vs V_{DD} ($I_{DD} = 420\text{mA}$, $T = 25\text{ }^\circ\text{C}$)

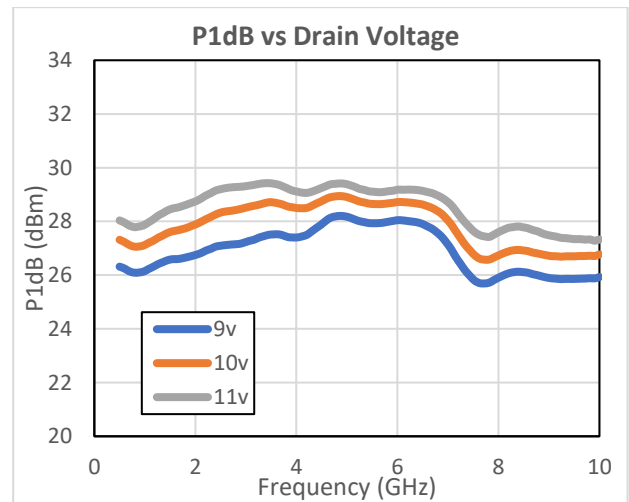


Figure 8 Noise Figure vs I_{DD} ($I_{DD} = 420\text{mA}$, $T = 25\text{ }^\circ\text{C}$)

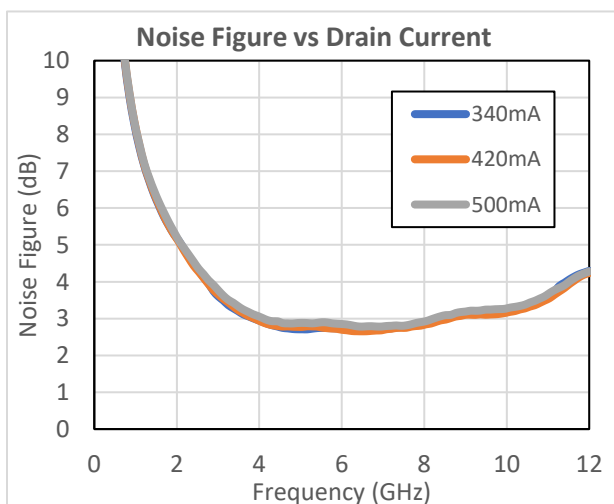


Figure 11 P3dB vs Temperature ($V_{DD} = 10\text{ V}$, $I_{DD} = 420\text{mA}$)

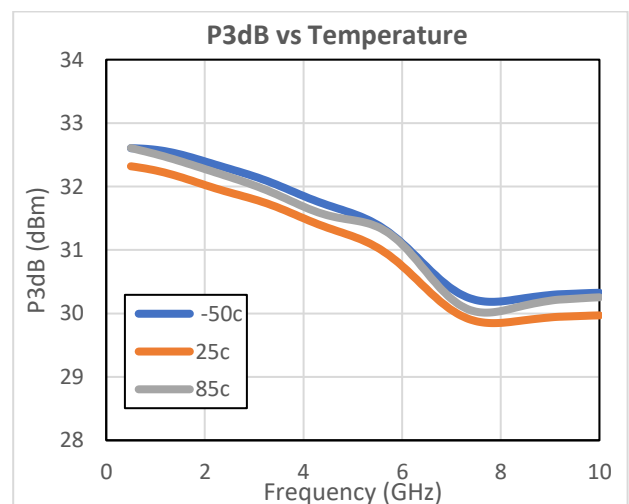


Figure 12 P3dB vs V_{DD} (I_{DD} = 420mA, T = 25 °C)

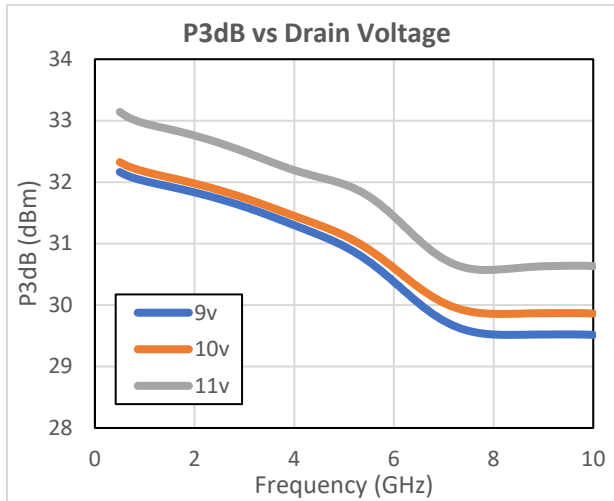


Figure 14 OIP3 vs I_{DD} (V_{DD} = 10 V, T = 25 °C)

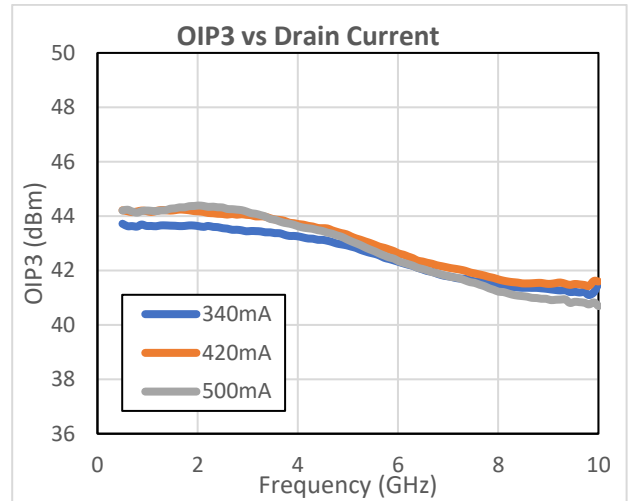


Figure 13 OIP3 vs Temperature (V_{DD} = 10 V, I_{DD} = 420mA, Output Power = 10dBm)

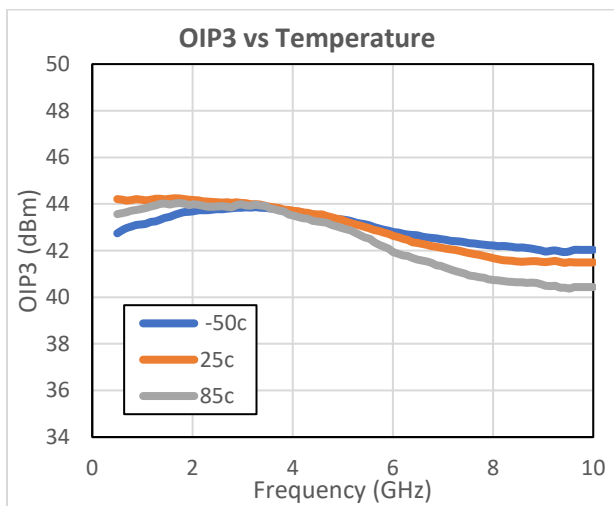


Figure 15 IM3 vs Output Power (V_{DD} = 10 V, I_{DD} = 420mA, T = 25 °C)

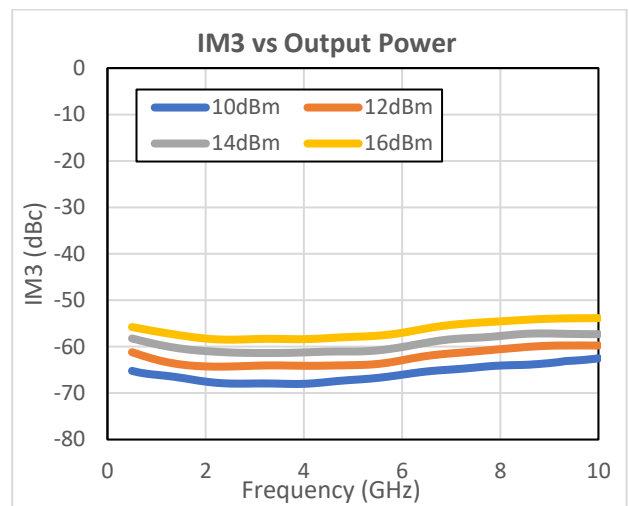
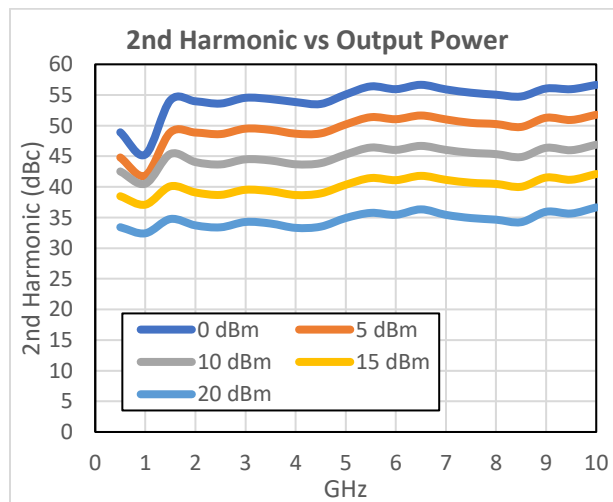


Figure 16 Second Harmonic vs Output Power (V_{DD} = 10 V, I_{DD} = 420mA, T = 25 °C)



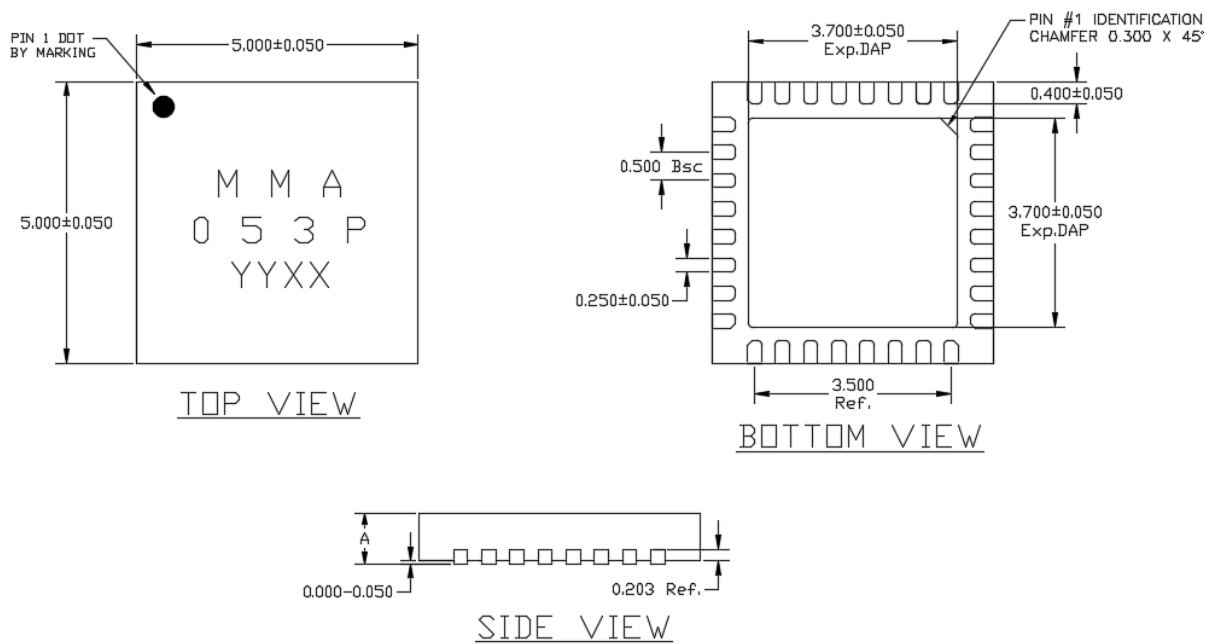
4 Package Specification

This section details the package specifications of the MMA053PP5 device.

4.1 Package Outline Drawing

The following illustration shows the package outline of the MMA053PP5 device. Dimensions are in millimeters.

Figure 15 Outline Package



4.2 Packaging Information

Table 3 Packaging Information

Part Number	Package Body Material	Lead Finish
MMA053PP5	RoHS - Compliance Low-stress injection molded plastic	Matte Sn

4.3 Pin Descriptions

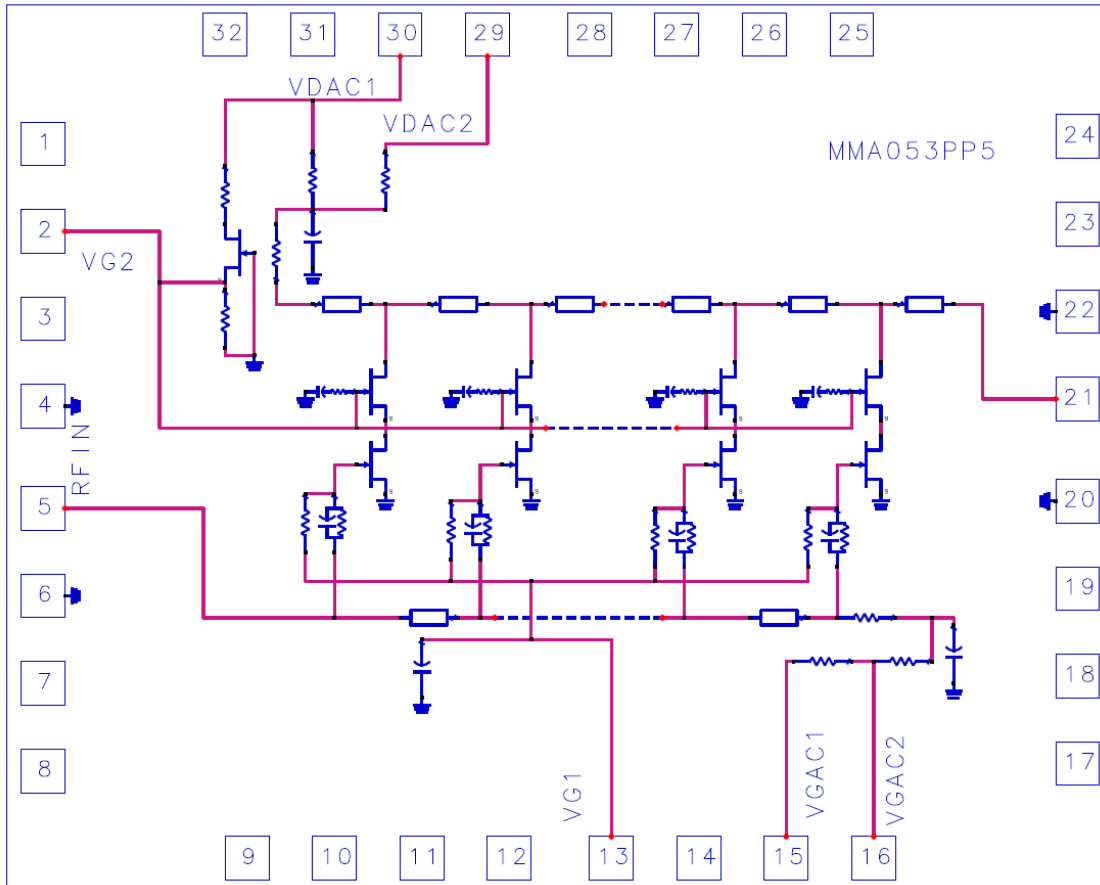
The following table describes the pins of the MMA053PP5 device.

Table 4 Pin Description

Pin Number	Pin Name	Description
2	V_{G2}	Low-frequency termination. Connect bypass capacitors per application circuit below.
5	RF_{IN}	Pin 5 on the layout and is matched to 50 Ω , and DC coupled to gate 1.
13	V_{G1}	First gate Bias. Adjust to achieve required I_{DD} .
15, 16	V_{G1A} , V_{G1B}	Low-frequency termination. Connect bypass capacitors per application circuit below.
21	$RF_{OUT}+V_{DD}$	Pin 21 is matched to 50 Ω , and DC coupled to V_{DD} . Bias V_{DD} through a bias tee.
29, 30	V_{DB} , V_{DA}	DC linked V_{DD} internally. External bypass capacitors are required to extend RF match and gain flatness below 2 GHz.
4, 6, 20, 22	GND	Ground paddle. connect to RF/DC ground.
Backside Paddle	RF/DC GND	RF/DC ground.
1, 3, 7, 8, 9, 10, 11, 12, 14, 17, 18, 19, 23, 24, 25, 26, 27, 28, 31, 32	N/C	Connect to ground.

The following image shows the functional schematic of the MMA053PP5 device.

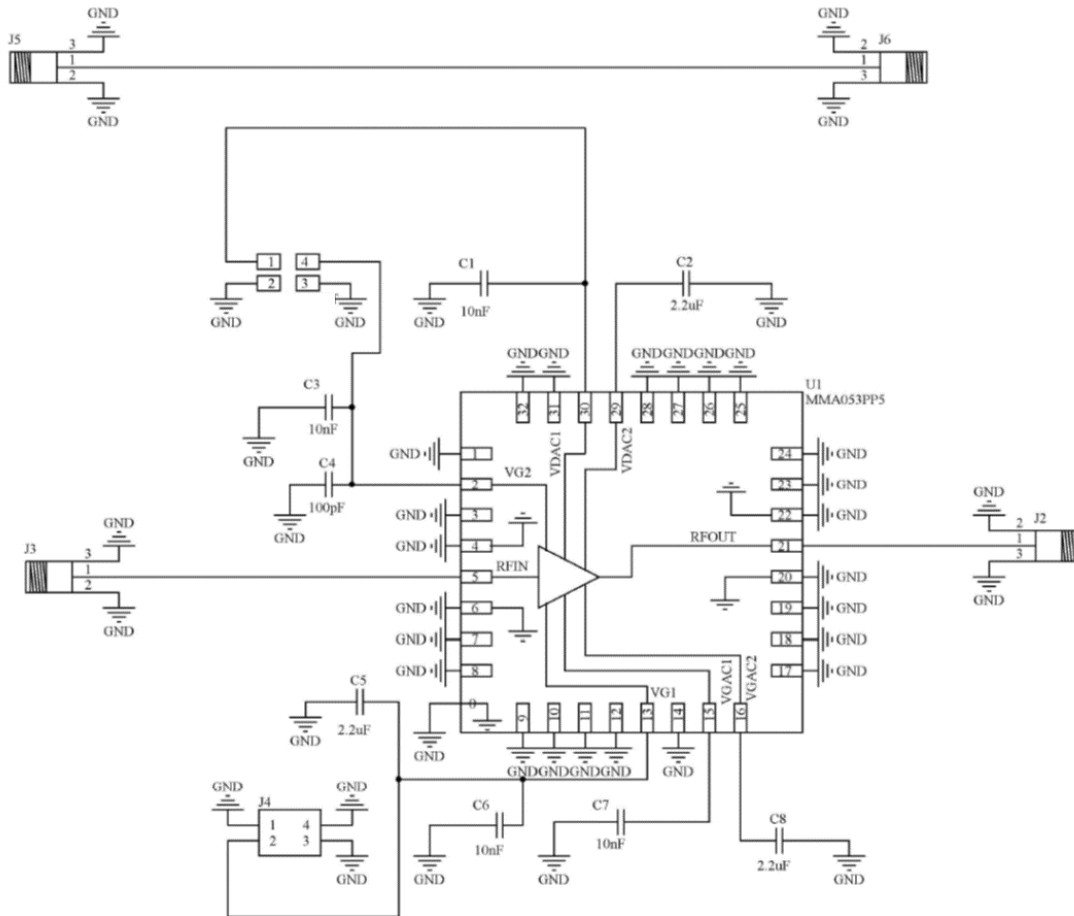
Figure 17 Functional Schematic



4.4 Application Circuit

The following illustration shows the application circuit of the MMA053PP5E device. Note that there is no internal DC blocking capacitor on the input or the output, and a bias tee must be used on pin 21 for biasing V_{DD} .

Figure 18 Application Circuit



5 Handling Recommendations

Gallium arsenide integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Microsemi application note [AN01 GaAs MMIC Handling and Die Attach Recommendations](#).

6 Evaluation Board Information

The following image shows the evaluation board of the MMA053PP5E device.

Figure 19 Evaluation Board

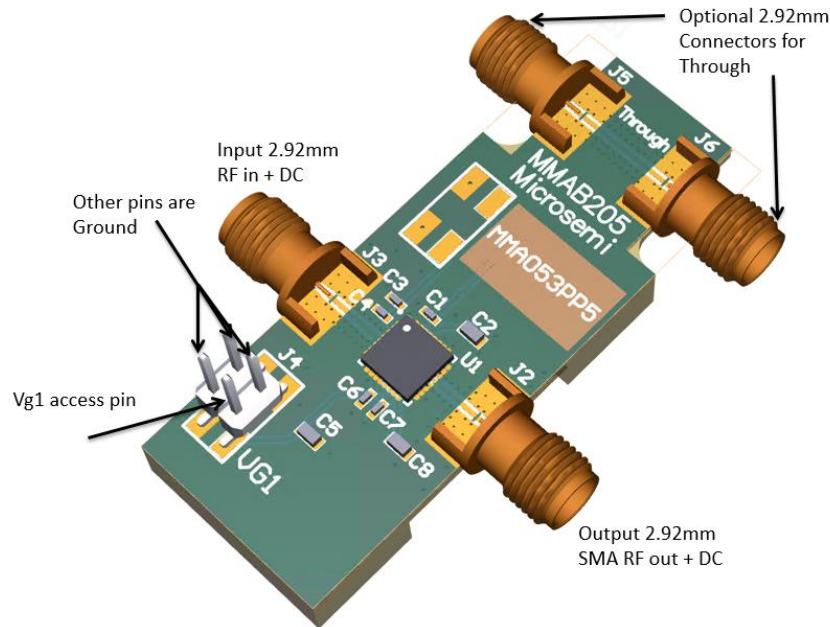


Table 5 List of Materials for Evaluation PCB MMA053PP5E

Item	Description
C1, C3, C6, C7	CAP 10 nF 50 V –20% to +80% 0402
C2, C5, C8	2.2 μ F 16 V ceramic capacitor X5R 0603
C4	CAP 100 pF 50 V \pm 10% 0402
J4	Header, 2-pin, dual row
J2, J3, J5, J6	CONN 2.92 mm female PCB edge mount .012 pin

Table 6 Bias Sequence

Bias Sequence	
1)	Set the gate voltage VG1 to -1V
2)	Set drain voltage VDD to 10V
3)	Adjust the gate voltage until the drain current is 420mA