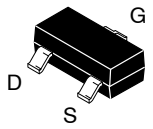
N-Channel General Purpose Amplifier

MMBF5457

This device is a low level audio amplifier and switching transistors, and can be used for analog switching applications. Sourced from Process 55.



NOTE: Source & Drain are interchangeable

SOT−23
CASE 318−08

ABSOLUTE MAXIMUM RATINGS* (T_A = 25°C unless otherwise noted)

Symbol	Rating	Value	Unit
V_{DG}	Drain−Gate Voltage	25	V
V_{GS}	Gate−Source Voltage	−25	V
I_{GF}	Forward Gate Current	10	mA
T_J, T_{stg}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*These rating are limiting values above which the serviceability of any semiconductor device may be impaired.

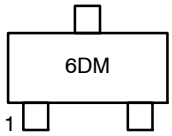
1. These rating are based on a maximum junction temperature of 150°C.
2. These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

THERMAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Characteristic	Max *MMBF5457	Unit
P_D	Total Device Dissipation Derate above 25°C	350 2.8	mW mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	−	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	556	°C/W

*Device mounted on FR−4 PCB 1.6” x 1.6” x 0.06”.

MARKING DIAGRAM



6D = Device Code
M = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
MMBF5457	SOT−23 (Pb−Free, Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
$V_{(BR)GSS}$	Gate−Source Breakdown Voltage	I_G = 10 μA, V_{DS} = 0	−25	–	–	V
I_{GSS}	Gate Reverse Current	V_{GS} = −15 V, V_{DS} = 0 V_{GS} = −15 V, V_{DS} = 0, T_A = 100°C	– –	– –	−1.0 −200	nA nA
$V_{GS(off)}$	Gate−Source Cutoff Voltage	V_{DS} = 15 V, I_D = 10 nA	−0.5	–	−6.0	V
V_{GS}	Gate−Source Voltage	V_{DS} = 15 V, I_D = 100 μA	–	−2.5	–	V
ON CHARACTERISTICS						
I_{DSS}	Zero−Gate Voltage Drain Current (Note 3)	V_{DS} = 15 V, V_{GS} = 0	1.0	3.0	5.0	mA
SMALL SIGNAL CHARACTERISTICS						
g_{fs}	Forward Transfer Conductance (Note 3)	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 kHz	1000	–	5000	μmhos
g_{os}	Output Conductance (Note 3)	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 kHz	–	10	50	μmhos
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 MHz	–	4.5	7.0	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 MHz	–	1.5	3.0	pF
NF	Noise Figure	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 kHz, R_G = 1.0 MΩ, BW = 1.0 Hz	–	–	3.0	dB

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 ms, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

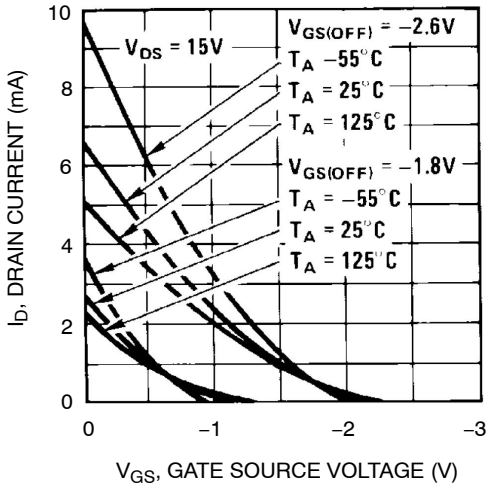


Figure 1. Transfer Characteristics

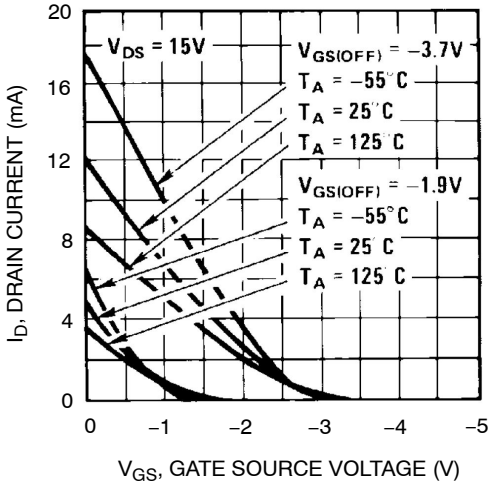


Figure 2. Transfer Characteristics

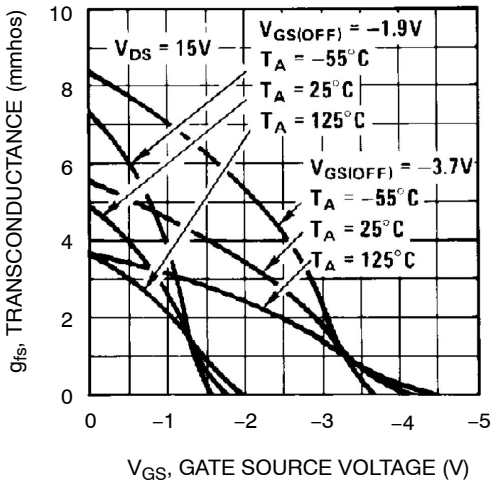


Figure 3. Transfer Characteristics

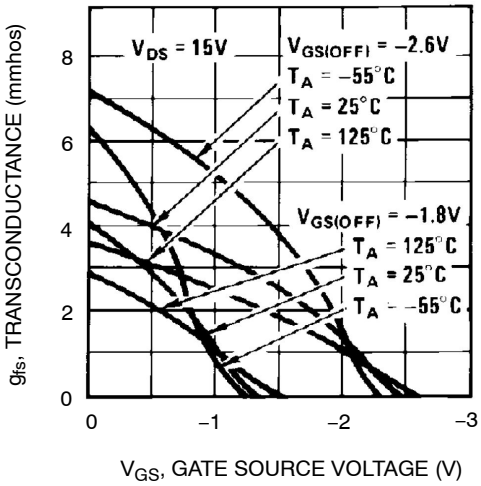


Figure 4. Transfer Characteristics

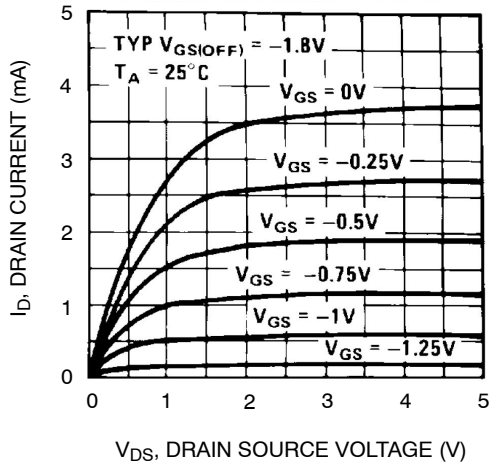


Figure 5. Common Drain−Source

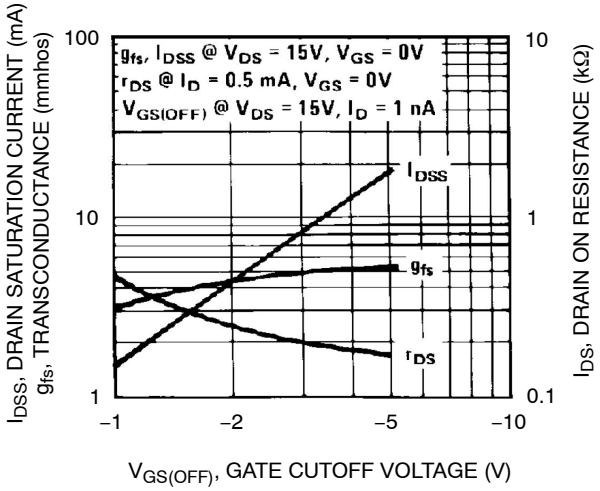


Figure 6. Parameter Interaction

TYPICAL CHARACTERISTICS (CONTINUED)

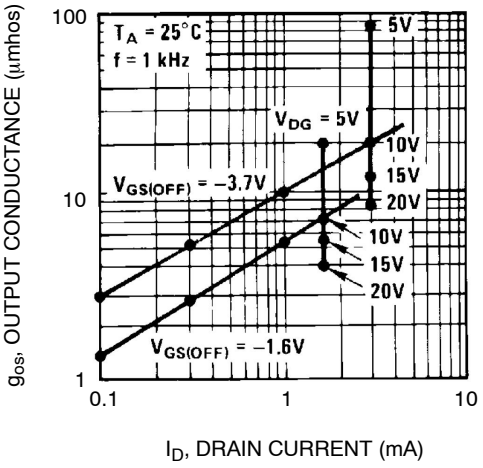


Figure 7. Output Conductance vs. Drain Current

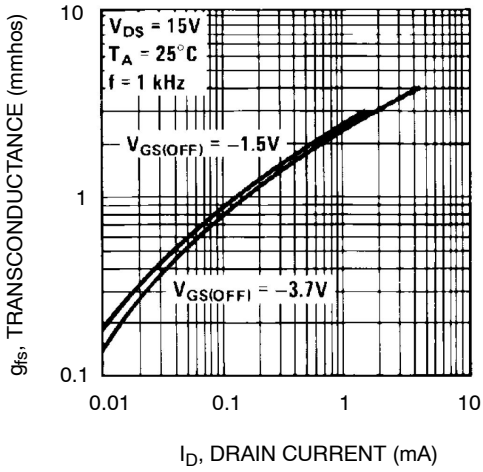


Figure 8. Transconductance vs. Drain Current

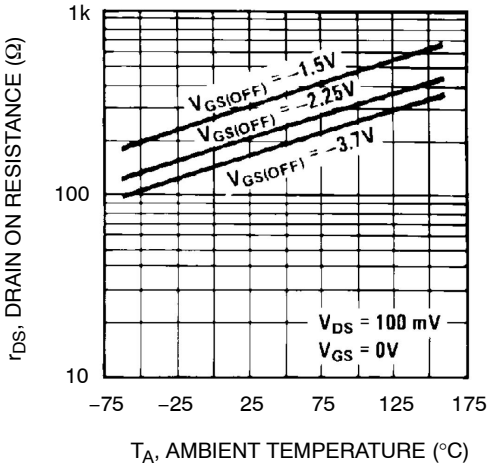


Figure 9. Channel Resistance vs. Temperature

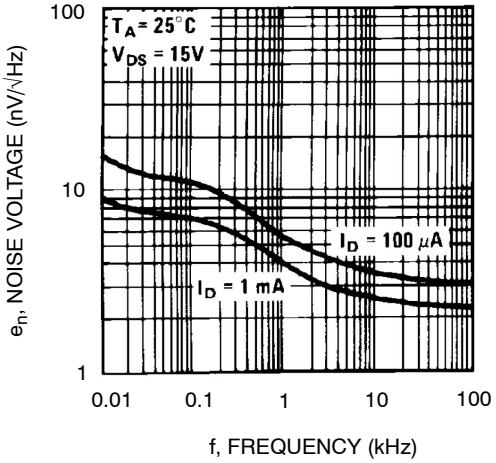


Figure 10. Noise Voltage vs. Frequency

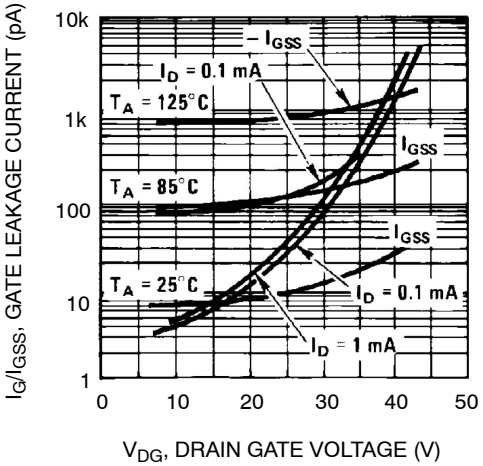


Figure 11. Leakage Current vs. Voltage

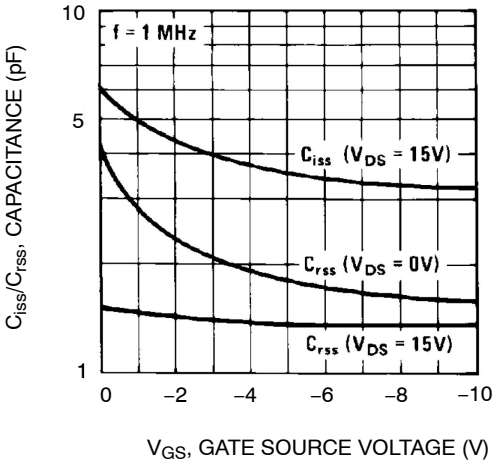


Figure 12. Capacitance vs. Voltage

TYPICAL CHARACTERISTICS (CONTINUED)

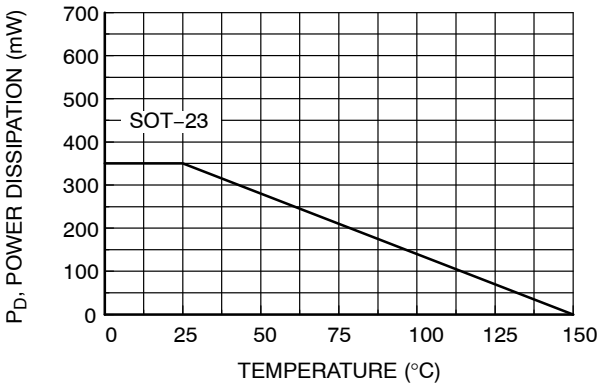
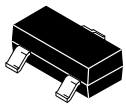


Figure 13. Power Dissipation vs. Ambient Temperature

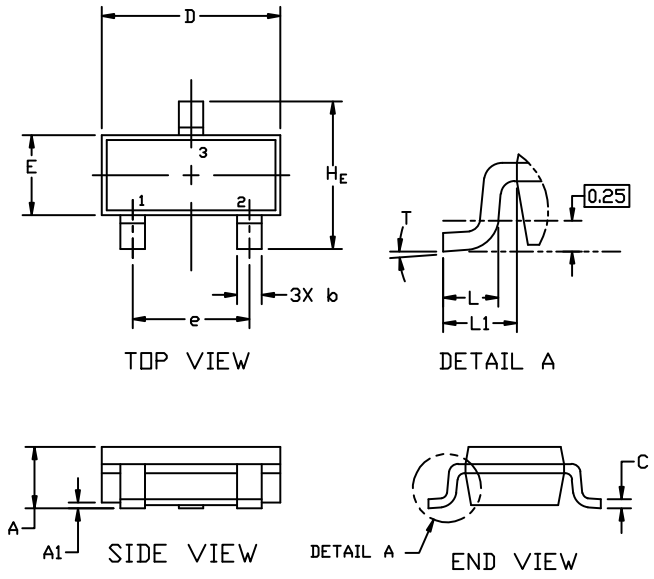
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 4:1

SOT−23 (TO−236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

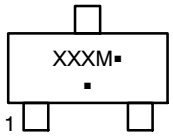


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

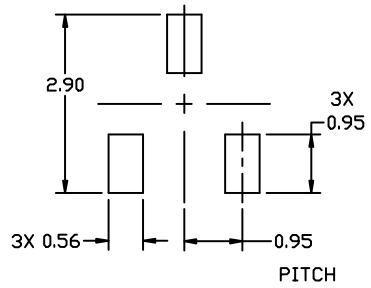
	MILLIMETERS			INCHES		
DIM	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H_E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42226B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOT−23 (TO−236)**		**PAGE 1 OF 2**

SOT−23 (TO−236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE