MP2328C

High-Efficiency, 28V, 2A, 450kHz, Synchronous Step-Down Converter with PG, SS, and Forced CCM

DESCRIPTION

The MP2328C is a fully integrated, high-frequency, synchronous, rectified, step-down switch-mode converter with internal power MOSFETs. It offers a very compact solution to achieve 2A of continuous output current (I_{OUT}) across a wide input voltage (V_{IN}) range, with excellent load and line regulation. The MP2328C offers synchronous mode operation for high efficiency across the wide I_{OUT} load range.

Constant-on-time (COT) control provides very fast transient response and easy loop design, as well as tight output regulation.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

The MP2328C requires a minimal number of readily available, standard external components. It is available in a space-saving SOT583 package.

FEATURES

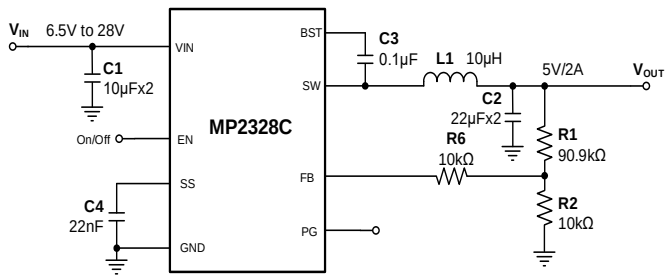
- Wide 4.5V to 28V Operating Input Voltage (V_{IN}) Range
- Wide 0.5V to 16V Output Voltage (V_{OUT}) Range
- ±1.5% Internal Reference Accuracy Over-Temperature (OT)
- 130mΩ/60mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- >92% Efficiency for 24V to 5V/2A Condition
- Fast Load Transient Response
- 450kHz Switching Frequency (f_{SW})
- t_{ON} Extension to Improve Dropout
- Configurable Soft-Start Time (t_{SS})
- Forced Continuous Conduction Mode (FCCM)
- Power Good (PG) Indication
- Over-Current Protection (OCP) with Hiccup Mode
- Thermal Shutdown Protection
- Available in a SOT583 Package

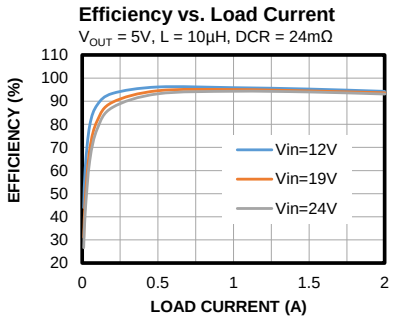
MPL Optimized Performance with MPS Inductor MPL-AL6060 Series

APPLICATIONS

- Game Consoles
- Multi-Function Printers
- Power Meters
- Flat-Panel Televisions and Monitors
- General-Purpose Power Supplies

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2328CGTL	SOT583	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP2328CGTL-Z).

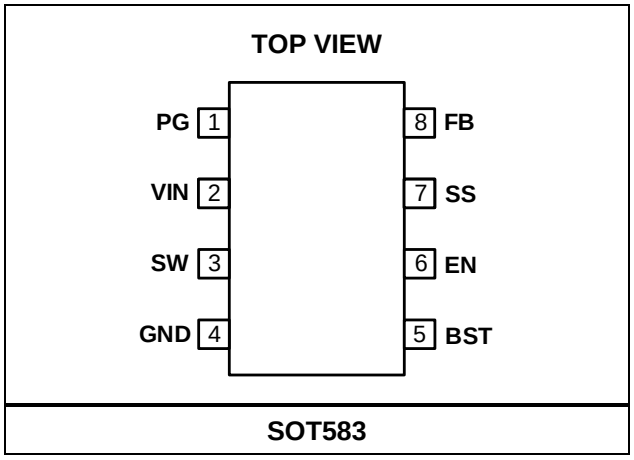
TOP MARKING

BRNY

LLL

BRN: Product code of MP2328CGTL
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	PG	**Power good output.** This pin is an open-drain output. When the IC is disabled, PG is pulled low. PG can be pulled up to other DC source. Note that if PG is pulled up to an external voltage, then it does not de-assert (logic low) when the input power is off. It is recommended to pull PG up to the output voltage (V_{OUT}) so that PG can de-assert (logic low) when the input power is off.
2	VIN	**Supply voltage.** The MP2328C operates from a 4.5V to 28V input rail. Place a capacitor on VIN to decouple the input rail. Connect VIN using a wide PCB trace.
3	SW	**Switch output.** Connect SW using a wide PCB trace.
4	GND	**System ground.** Reference ground of the regulated V_{OUT}. GND requires careful consideration when designing the PCB layout. Connect GND with copper traces and vias.
5	BST	**Bootstrap.** Connect a capacitor between the SW and BST pins to form a floating supply across the high-side MOSFET (HS-FET) driver. It is typically recommended to use a 0.1µF bootstrap capacitor.
6	EN	**Enable pin**. EN is a digital input that turns the buck regulator on and off. When the power supply of the control circuit is ready, pull EN high to turn the buck regulator on. Pull EN low to turn the regulator off. Connect EN to VIN through a voltage resistor divider for automatic start-up. The EN voltage should not exceed 6V.
7	SS	**Soft start.** Connect an external capacitor to SS to configure the soft-start time (t_{SS}) for the switch-mode regulator.
8	FB	**Feedback.** Connect FB to the tap of an external resistor divider from the output to GND to set V_{OUT}.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to +30V
V_{SW}.....
-0.3V (-5V for <10ns) to +30V (32V for <10ns)
V_{BST} ..... V_{SW} + 5.5V
All other pins .....-0.3V to +6V
PG pin current..... 5mA (2)
Continuous power dissipation (T_A = 25°C) (3)
.....2.27W (4)
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2000V
Charged device model (CDM) ..... ±750V

Recommended Operating Conditions (5)

Supply voltage (V_{IN}) .....4.5V to 28V
Output voltage (V_{OUT}).....
..... 0.5V to 0.95 x V_{IN} or 16V max
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

SOT583
EVL2328C-TL-00A (4) .....55 ..... 21°C/W
JESD51-7 (6) .....130 ..... 60°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) When the PG pin is pulled up to power source, the current should be limited below the maximum value.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can generate excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Measured on the EVL2328C-TL-00A, 2-layer PCB (63.5mmx63.5mm).
5) The device is not guaranteed to function outside of its operating conditions.
6) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, the over-temperature (OT) limit is derived by characterization, unless otherwise noted. (7)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
V_{IN} under-voltage lockout (UVLO) threshold	$V_{IN\_UVLO\_R}$	V_{IN} rising, V_{EN} = 2V	3.66	3.96	4.25	V
V_{IN} UVLO hysteresis	$V_{IN\_UVLO\_HYS}$			330		mV
Shutdown supply current	I_{SD}	V_{EN} = 0V		2	10	µA
Quiescent supply current	I_Q	V_{EN} = 2V, V_{FB} = 0.55V		560	700	µA
Enable Control						
EN rising threshold	$V_{EN-RISE}$		1.1	1.2	1.3	V
EN hysteresis	V_{EN-HYS}			120		mV
EN input current	I_{EN}	V_{EN} = 2V		2	10	µA
Power MOSFET						
High-side MOSFET (HS-FET) on resistance	HS_{RDS-ON}	V_{BST-SW} = 5V		130		mΩ
Low-side MOSFET (LS-FET) on resistance	LS_{RDS-ON}			60		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V			1	µA
Current Limit						
Low-side (LS) switching valley current limit	$I_{LIMIT-LS-OC}$		1.9	2.75	3.6	A
Negative current limit	I_{NEG}	V_{OUT} = 5V, L = 1.5µH		-1.6		A
Frequency						
Oscillator frequency	f_{SW}	V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 1.5A	350	450	550	kHz
Minimum on time (8)	t_{ON-MIN}			50		ns
Minimum off time (8)	$t_{OFF-MIN}$			160		ns
Feedback Control						
Feedback (FB) voltage	V_{REF}	T_J = 25°C	495	500	505	mV
		T_J = -40°C to +125°C	492.5	500	507.5	mV
FB current	I_{FB}	V_{FB} = 0.5V		10	50	nA
Soft-start current	I_{SS}		5.5	7.5	9.5	µA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, the over-temperature (OT) limit is derived by characterization, unless otherwise noted. (7)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Good (PG) Indication						
PG lower trip rising threshold	$PG_{LOWER-R}$	PG from low to high	85	90	95	% of V_{REF}
PG lower trip falling threshold	$PG_{LOWER-F}$	PG from high to low	79	84	89	% of V_{REF}
PG upper trip rising threshold	$PG_{UPPER-R}$	PG from high to low	107	112	117	% of V_{REF}
PG upper trip falling threshold	$PG_{UPPER-F}$	PG from low to high	101	106	111	% of V_{REF}
PG rising delay	PG_{TD-R}			12		µs
PG falling delay	PG_{TD-F}			20		µs
PG sink current capability	V_{PG}	Sink 4mA			0.4	V
PG leakage current	I_{PG-LKG}	V_{IN} = 12V, V_{EN} = 2V, V_{FB} = 0.52V, V_{PG} = 5V		2	10	µA
Protection						
FB under-voltage (UV) threshold	$FBUV_{VTH}$		40	50	60	% of V_{REF}
Hiccup protection duty cycle (8)	D_{HICCUP}			25		%
Thermal shutdown	T_{SD}			150		°C
Thermal shutdown hysteresis	T_{SD_HYS}			20		°C

Notes:

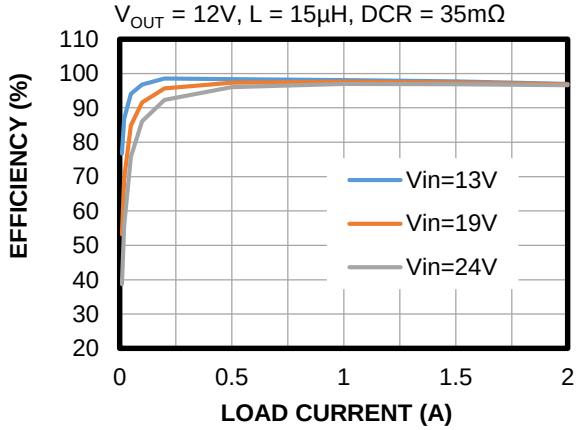
7) Not tested in production. Derived by over-temperature correlation.
8) Derived by sample characterization. Not tested in production.

TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 10µH, T_A = 25°C, unless otherwise noted.

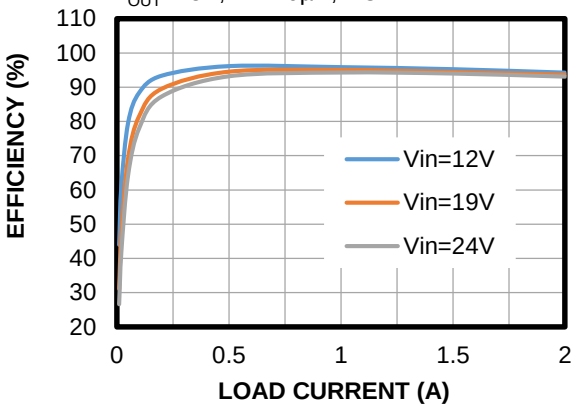
Efficiency vs. Load Current

V_{OUT} = 12V, L = 15µH, DCR = 35mΩ



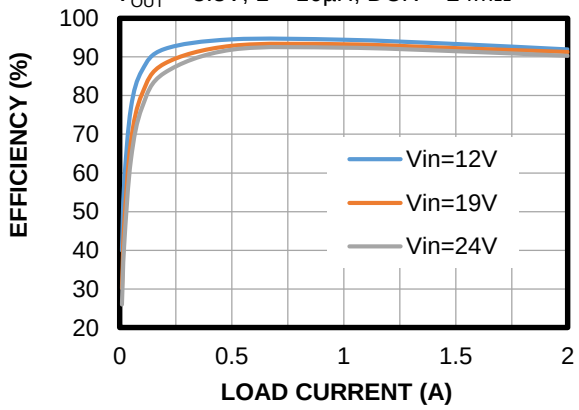
Efficiency vs. Load Current

V_{OUT} = 5V, L = 10µH, DCR = 24mΩ



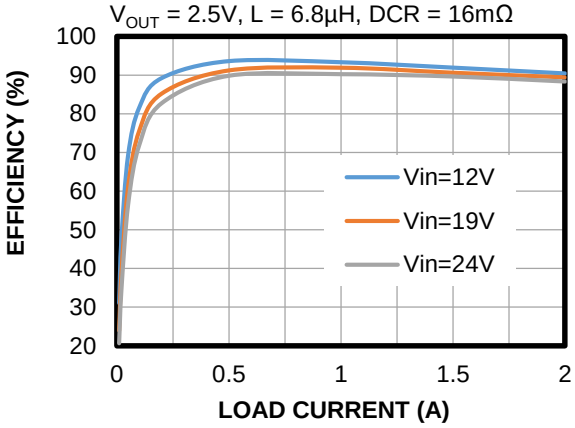
Efficiency vs. Load Current

V_{OUT} = 3.3V, L = 10µH, DCR = 24mΩ



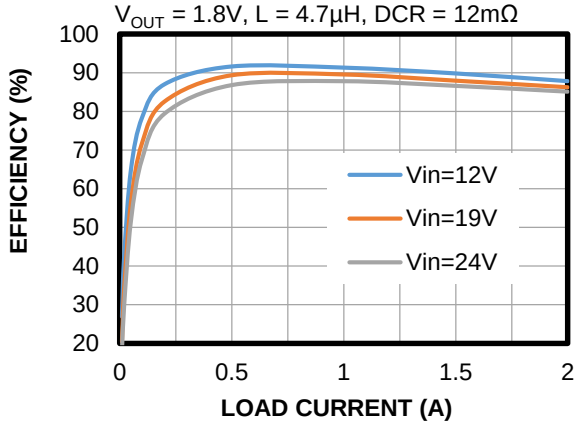
Efficiency vs. Load Current

V_{OUT} = 2.5V, L = 6.8µH, DCR = 16mΩ



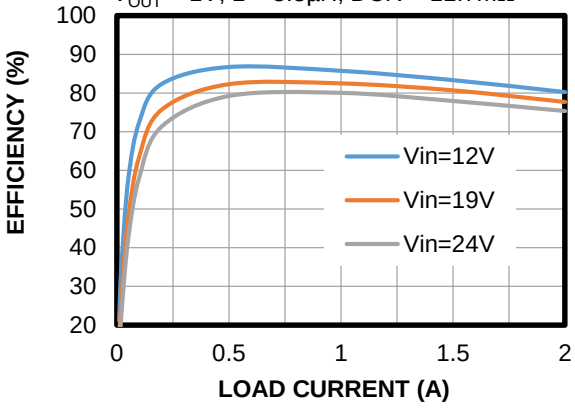
Efficiency vs. Load Current

V_{OUT} = 1.8V, L = 4.7µH, DCR = 12mΩ



Efficiency vs. Load Current

V_{OUT} = 1V, L = 3.3µH, DCR = 11.7mΩ

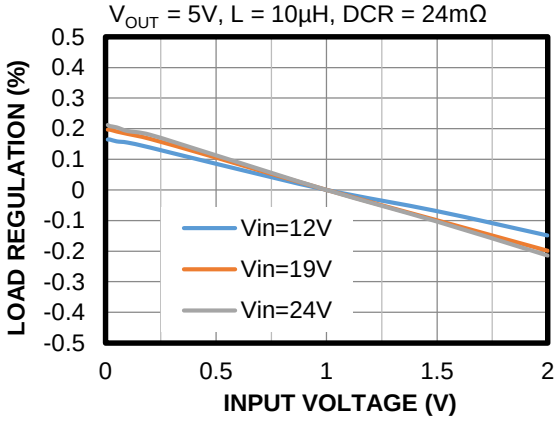


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 10µH, T_A = 25°C, unless otherwise noted.

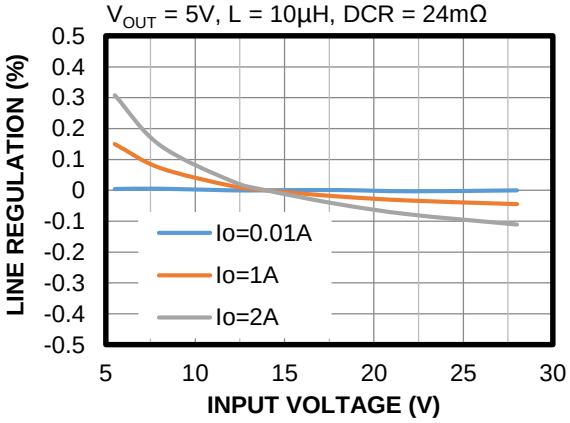
Load Regulation

V_{OUT} = 5V, L = 10µH, DCR = 24mΩ

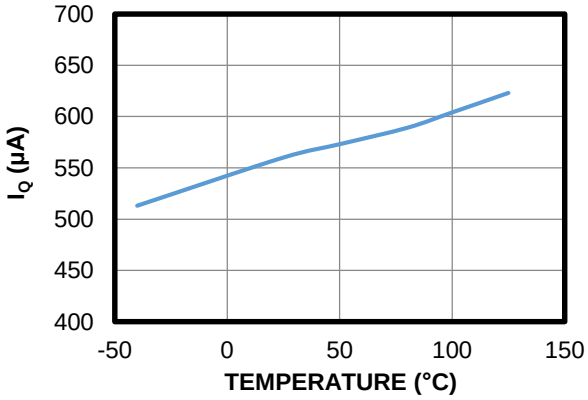


Line Regulation

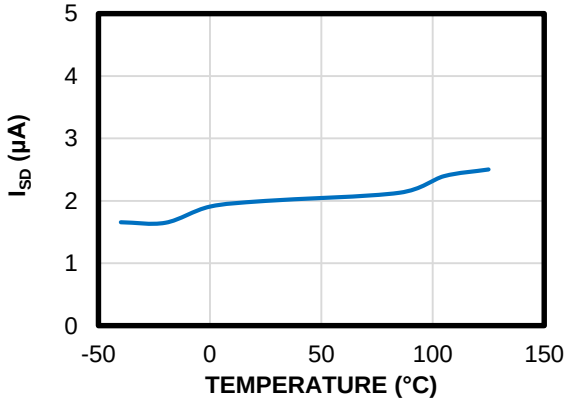
V_{OUT} = 5V, L = 10µH, DCR = 24mΩ



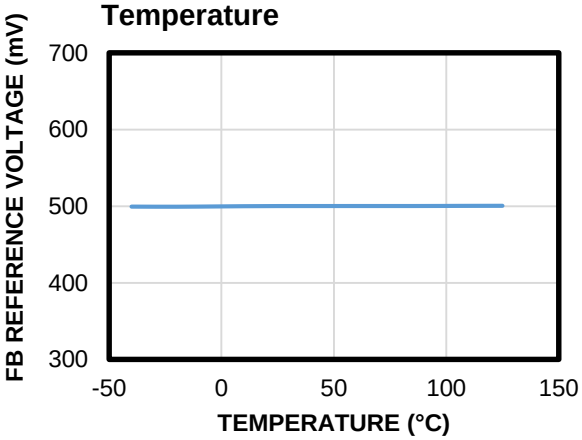
Quiescent Supply Current vs. Temperature



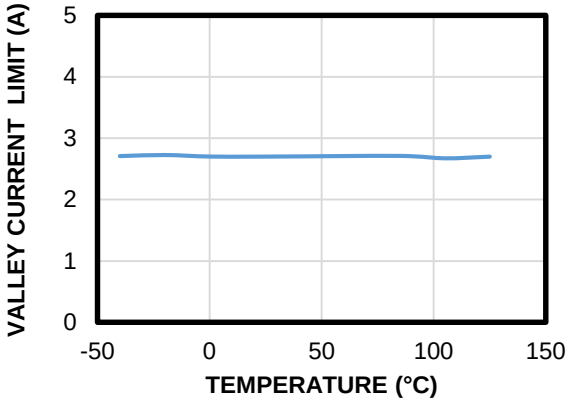
Shutdown Supply Current vs. Temperature



FB Reference Voltage vs. Temperature



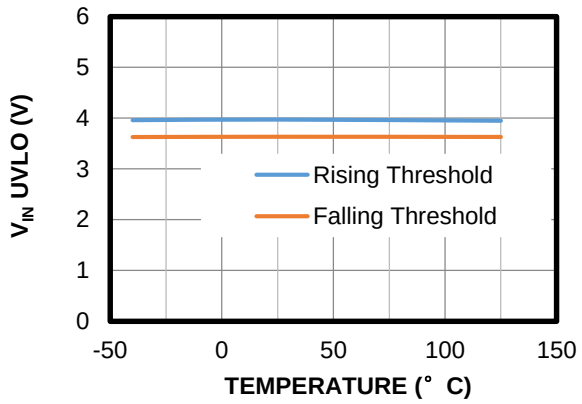
Valley Current Limit vs. Temperature



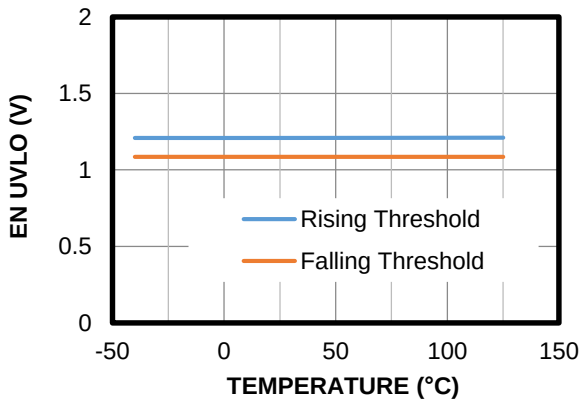
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 10µH, T_A = 25°C, unless otherwise noted.

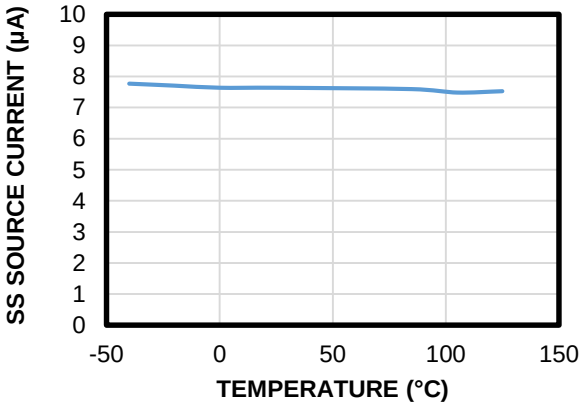
V_{IN} UVLO vs. Temperature



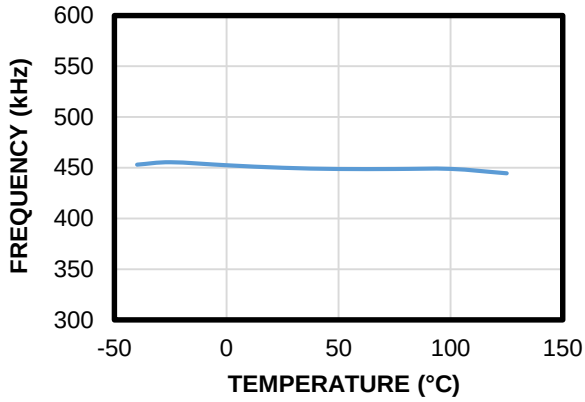
EN UVLO vs. Temperature



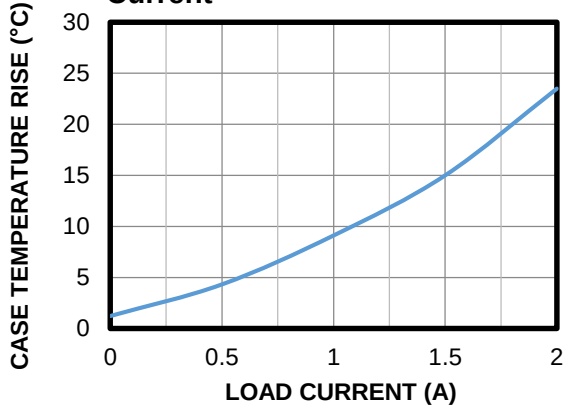
Soft-Start Source Current vs. Temperature



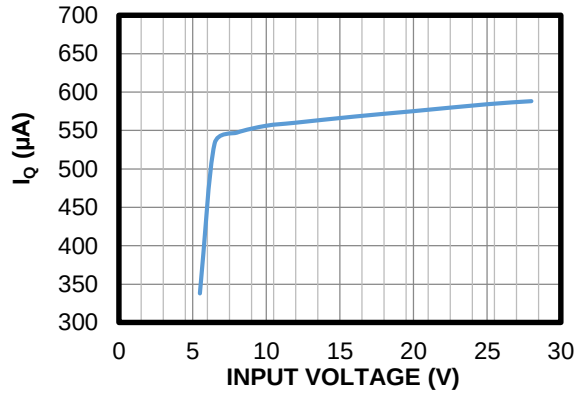
Frequency vs. Temperature



Case Temperature Rise vs. Load Current



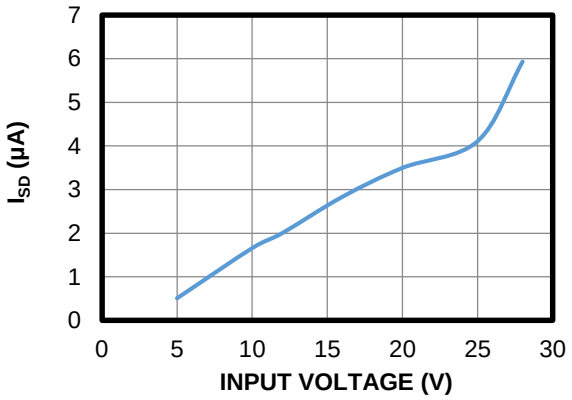
Quiescent Supply Current vs. Input Voltage



TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 10µH, T_A = 25°C, unless otherwise noted.

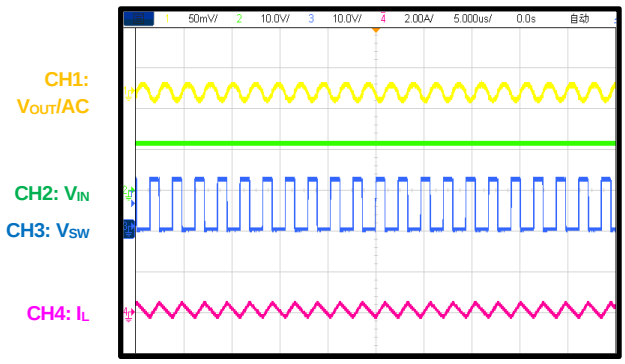
Shutdown Supply Current vs. Input Voltage



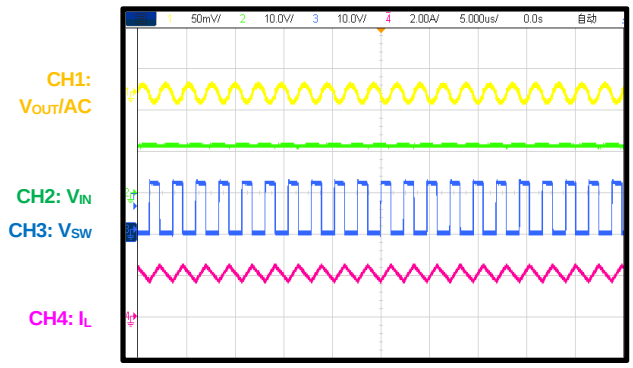
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 10µH, T_A = 25°C, unless otherwise noted.

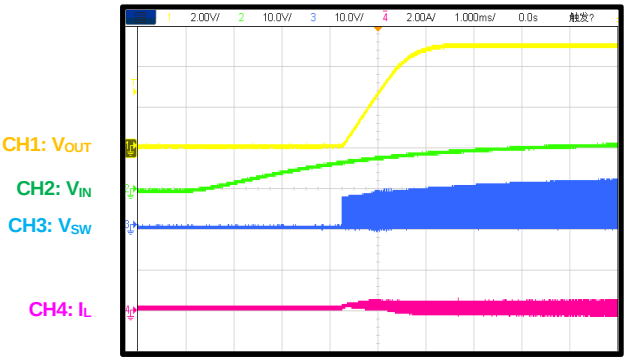
Steady State
I_{OUT} = 0A



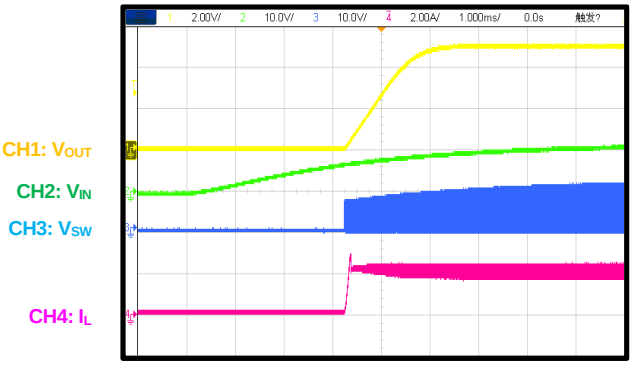
Steady State
I_{OUT} = 2A



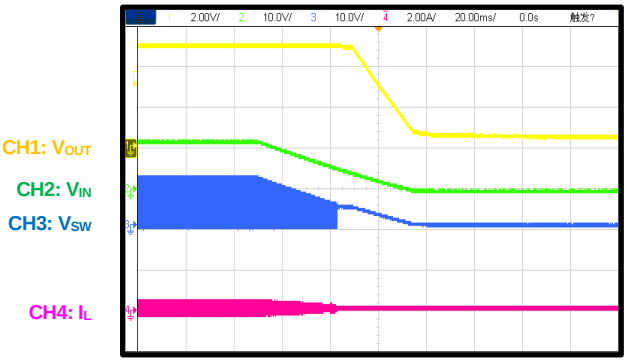
Input Power Start-Up
I_{OUT} = 0A



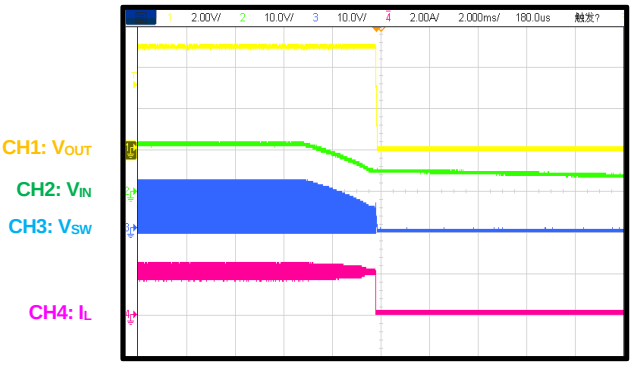
Input Power Start-Up
I_{OUT} = 2A



Input Power Shutdown
I_{OUT} = 0A



Input Power Shutdown
I_{OUT} = 2A

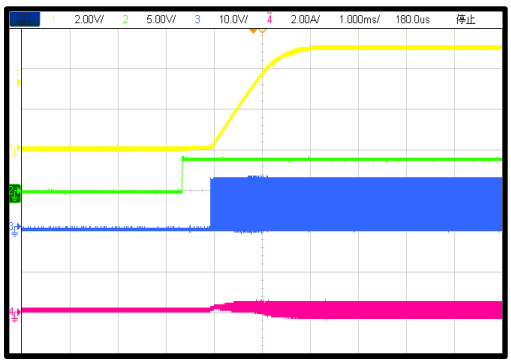


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 10µH, T_A = 25°C, unless otherwise noted.

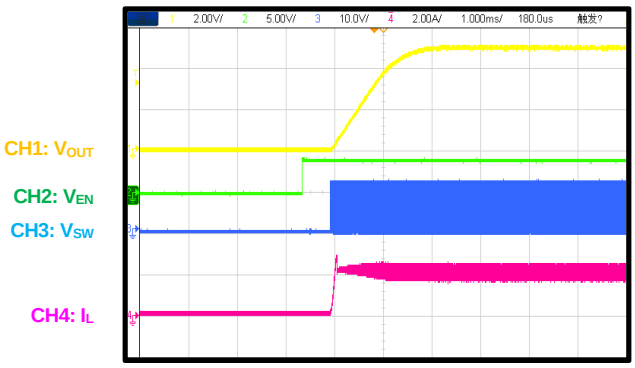
Start-Up through EN

I_{OUT} = 0A



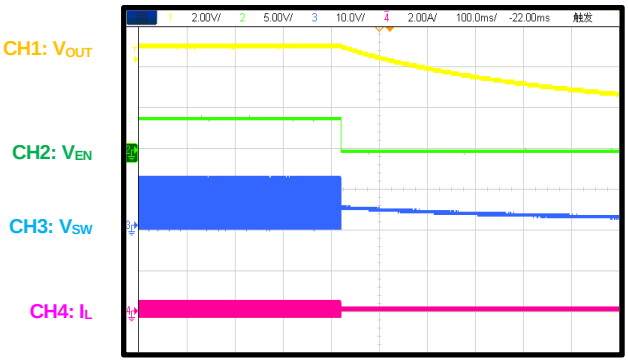
Start-Up through EN

I_{OUT} = 2A



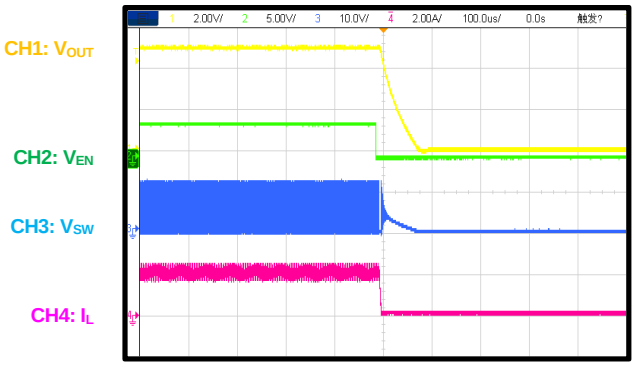
Shutdown through EN

I_{OUT} = 0A



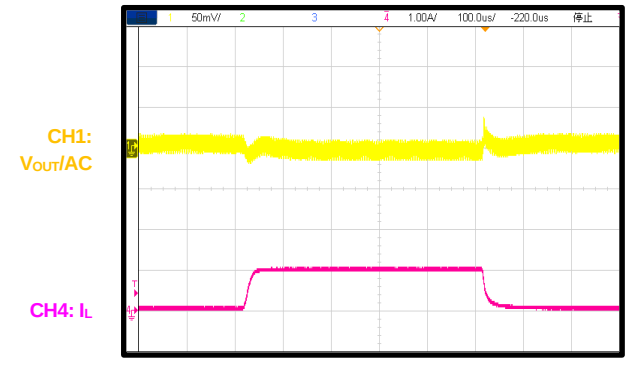
Shutdown through EN

I_{OUT} = 2A



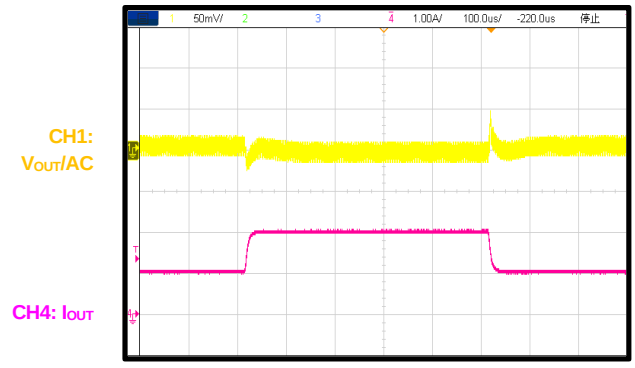
Load Transient

I_{OUT} = 0A to 1A



Load Transient

I_{OUT} = 1A to 2A

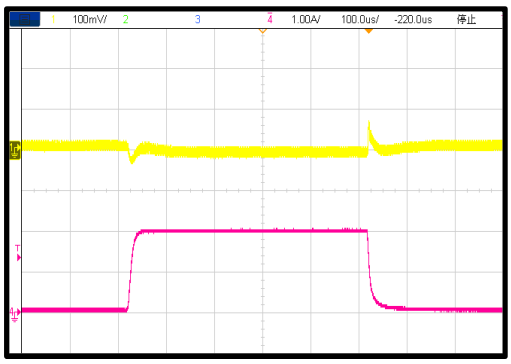


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 10µH, T_A = 25°C, unless otherwise noted.

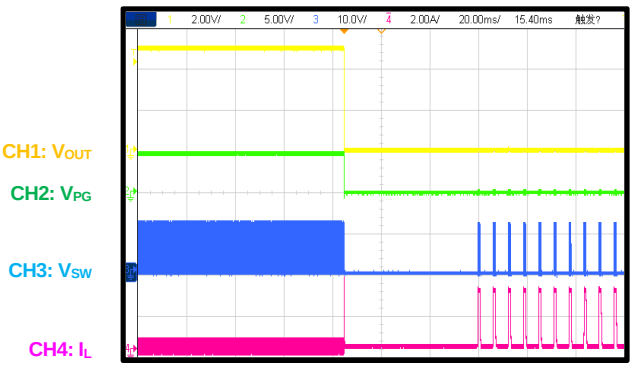
Load Transient

I_{OUT} = 0A to 2A



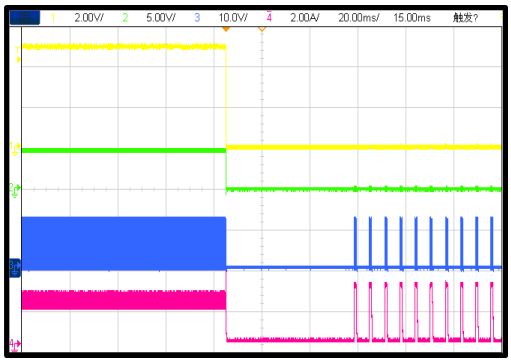
SCP Entry

I_{OUT} = 0A



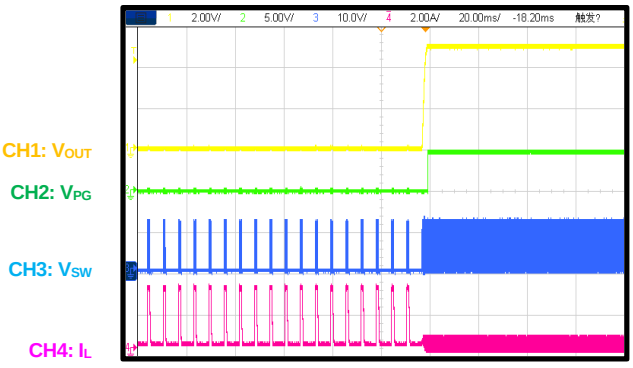
SCP Entry

I_{OUT} = 2A



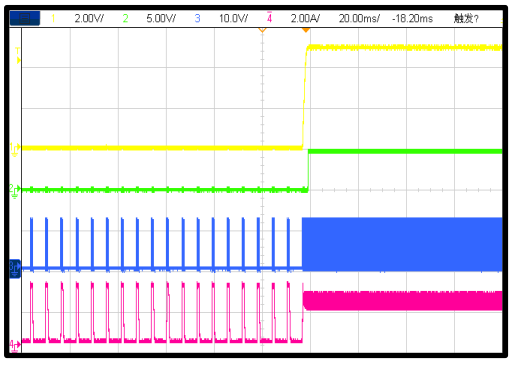
SCP Recovery

I_{OUT} = 0A



SCP Recovery

I_{OUT} = 2A



FUNCTIONAL BLOCK DIAGRAM

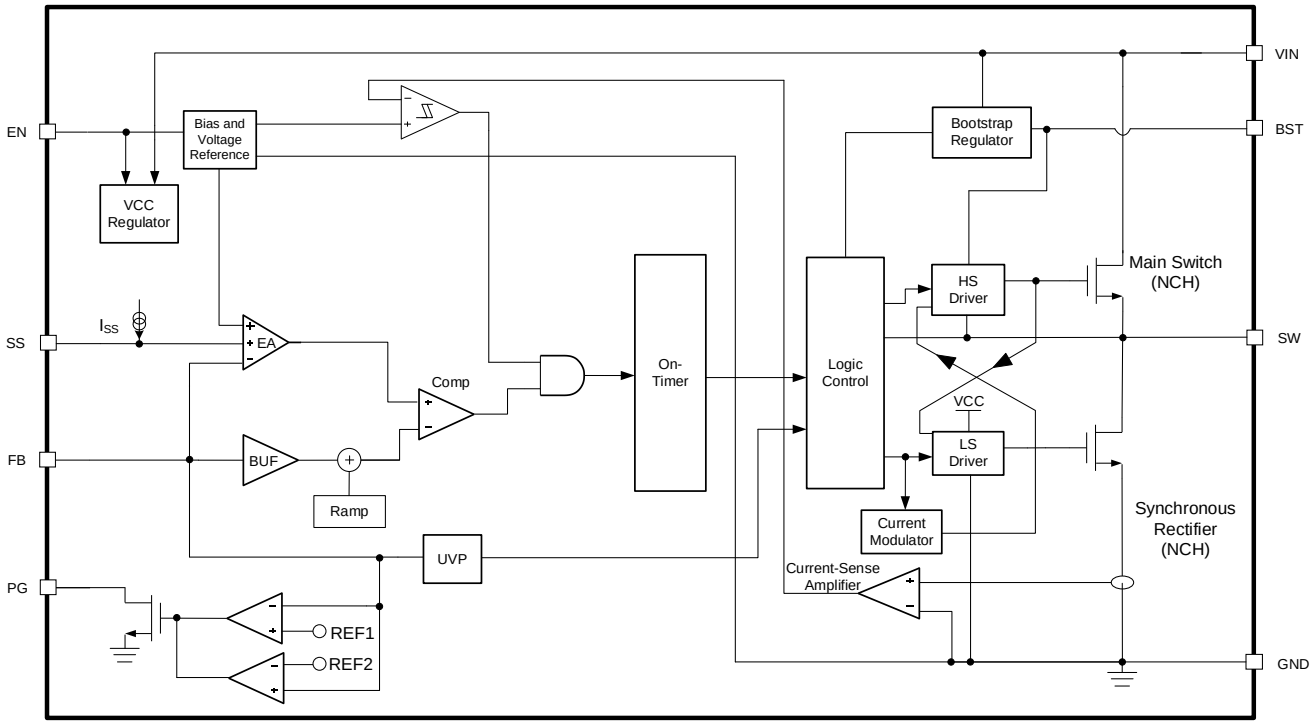


Figure 1: Functional Block Diagram

OPERATION

Pulse-Width Modulation (PWM) Operation

The MP2328C is a fully integrated, synchronous, rectified, step-down switch-mode converter. Constant-on-time (COT) control is employed to provide fast transient response and ease loop stabilization.

At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on when the FB voltage (V_{FB}) drops below the reference voltage (V_{REF}). The HS-FET turns on for a fixed interval, determined by the one-shot on timer. The on-timer is determined by both the output voltage (V_{OUT}) and input voltage (V_{IN}) to keep the switching frequency (f_{SW}) fairly constant across the V_{IN} range. After the on period finishes, the HS-FET turns off until the next period begins. By repeating this operation, the converter regulates V_{OUT}.

The low-side MOSFET (LS-FET) turns on when the HS-FET is off to minimize conduction loss. If both the HS-FET and LS-FET turn on at the same time, a dead short occurs between the input and GND. This is called shoot-through. To prevent shoot-through, a dead time (DT) is generated internally between the HS-FET off time and LS-FET on time, and vice versa.

The MP2328C works in forced continuous conduction mode (FCCM) to achieve smaller output ripple, better load regulation, and improved transient response in full load range.

Enable (EN) Control

The enable (EN) pin can enable or disable the entire chip. Pull EN high to turn the regulator on; pull it low to turn the regulator off.

For automatic start-up, EN can be pulled up to V_{IN} through a voltage resistor divider. There is an internal 1MΩ resistor from EN to GND. To calculate the automatic start-up voltage (V_{IN_START}), determine the values of the pull-up resistor (R_{UP}, from VIN to EN) and pull-down resistor (R_{DOWN}, from EN to GND) using Equation (2):

$$V_{IN\_START} = 1.3 \times \frac{R_{UP} + R_{DOWN}//1000k\Omega}{R_{DOWN}//1000k\Omega} \quad (1)$$

For example, if R_{UP} = 191kΩ and R_{DOWN} = 49.9kΩ, set $V_{IN\text{-}START}$ to 6.5V.

To avoid damaging the internal circuit, the EN voltage must not exceed 6V.

Under-Voltage Lockout (UVLO)

V_{IN} under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO rising threshold is about 3.96V, and its falling threshold is about 3.63V typically.

Soft Start (SS)

The MP2328C employs a soft start (SS) mechanism to ensure smooth output ramping during start-up.

When the part starts, an internal current source (typically 7.5μA) charges up the SS capacitor (C_{SS}) to generate a soft-start voltage (V_{SS}).

When V_{SS} is below V_{REF}, V_{SS} overrides V_{REF}. The error amplifier (EA) uses V_{SS} as the reference, and V_{OUT} ramps up smoothly. Once V_{SS} exceeds V_{REF}, the EA uses V_{REF} as the reference. At this point, soft start finishes and the device enters steady state operation.

C_{SS} can be determined using Equation (2):

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}} \quad (2)$$

Over-Current Protection (OCP)

The MP2328C has a valley current limit. While the LS-FET is on, the inductor current is monitored. When the sensed inductor current (I_L) reaches the valley current limit, the LS limit comparator (see Figure 1 on page 13) turns over and the device enters over-current protection (OCP) mode. The HS-FET does not turn on again until the valley current limit disappears. Meanwhile, V_{OUT} drops until V_{FB} falls below the FB under-voltage (UV) threshold. Once a UV condition is triggered, the MP2328C enters hiccup mode (after SS) to periodically restart the part.

During OCP, the device tries to recover from the over-current (OC) fault with hiccup mode. In hiccup mode, the chip disables the output power stage, discharges the soft-start capacitor, and then automatically tries to soft start again. If the OC condition remains after SS ends, then the device repeats this operation cycle until the OC

conditions disappear, and the output rises back to the regulation level.

Power Good (PG)

The power good (PG) pin indicates whether V_{OUT} is in the normal range compared to the internal V_{REF}. It is an open-drain output that requires an external pull-up supply. During start-up, the PG output is pulled low, which indicates to the system to remain off and keep the load on the output to a minimum. This helps reduce inrush current at start-up.

When V_{OUT} is between 90% and 112% of the internal V_{REF} and SS is finished, the PG signal is pulled high. If V_{OUT} is below 84% after SS finishes, the PG signal stays low.

When V_{OUT} exceeds 112% of the internal V_{REF}, PG switches low. The PG signal is pulled high once V_{OUT} drops below 106% of the internal reference voltage.

The PG output is pulled low when EN UVLO, OCP, or over-temperature protection (OTP) is triggered.

If PG is pulled up to an external voltage, then PG does not de-assert (logic low) when V_{IN} drops below 0.8V. If PG is pulled up to V_{OUT}, then PG de-asserts (logic low) when V_{IN} drops below 0.8V.

On Time (t_{ON}) Extension

To improve dropout, the MP2328C is designed to extend its on time (t_{ON}) when the duty cycle exceeds 92%. When the HS-FET on time is extended, the frequency drops. The typical minimum frequency is 250kHz. The frequency cannot drop below 250kHz.

Pre-Biased Start-Up

The MP2328C is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the bootstrap (BST) voltage (V_{BST}) is refreshed and charged. The voltage on the soft-start capacitor is also charged. If V_{BST} exceeds its rising threshold voltage and V_{SS} exceeds the sensed output feedback voltage at the FB pin, the part starts switching normally.

Floating Driver and Bootstrap Charging

An external BST capacitor (C_{BST}) powers the floating power MOSFET driver. This floating driver has its own UVLO protection, with a 2.62V rising threshold and a 130mV hysteresis. V_{IN} regulates the C_{BST} voltage internally through D1, M1, C3, L1, and C2 (see Figure 2). If (V_{IN} - V_{SW}) exceeds 5V, then U2 regulates M1 to maintain a 5V V_{BST} across C3.

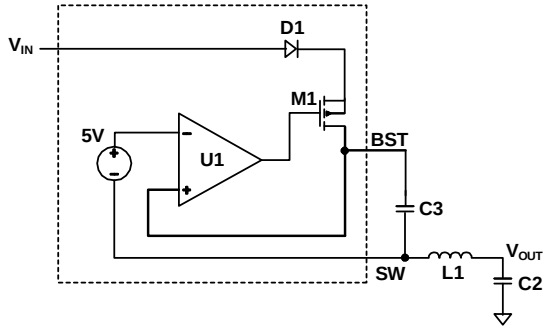


Figure 2: Internal Bootstrap Charger

Start-Up and Shutdown

If both V_{IN} and EN exceed their respective thresholds, the chip starts up. The reference block starts first, generating stable V_{REF} and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuits.

Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. The shutdown procedure begins by blocking the signaling path to avoid any fault triggering. Then the internal supply rail is pulled down.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled again and resumes normal operation.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets V_{OUT}. First, choose a value for R2. R2 should be chosen reasonably, as a small R2 value results in considerable quiescent current loss, while a large R2 value makes the FB noise sensitive. It is recommended to set R2 to be between 5kΩ and 50kΩ for a good balance between system stability and no-load loss. R1 can then be calculated using Equation (3):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (3)$$

Figure 3 shows the feedback circuit. R_T is an optional resistor for feedback compensation.

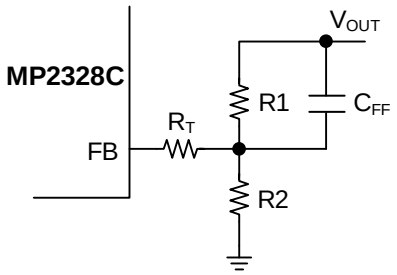


Figure 3: Feedback Network

Table 1 lists the recommended parameters for common output voltages.

Table 1: Parameter Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R_T (kΩ)	C_{FF} (pF)	L (µH)
1	51	51	10	82	3.3
1.8	51	19.6	10	470	4.7
2.5	51	12.7	10	470	6.8
3.3	51	9.09	10	470	10
5	90.9	10	10	300	10
12	255	11	10	82	15

Selecting the Inductor

The inductor supplies constant current to the output load while being driven by the switched V_{IN}. A larger-value inductor results in less ripple current and a lower output ripple voltage; however, it also has a larger physical footprint, higher series resistance, and lower saturation current. The inductance can be calculated using Equation (4):

$$L = \frac{V_{OUT}}{f_{sw} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum peak inductor current. The peak inductor current can be calculated using Equation (5):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times f_{sw} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 2 lists our power inductor recommendations. Select a part number based on the relevant design requirements.

Table 2: Power Inductor Selection

Part Number	Inductance	Manufacturer
MPL-AL	2.2µH to 15µH	MPS
MPL-AL-6050-3R3	3.3µH	MPS
MPL-AL-6060-4R7	4.7µH	MPS
MPL-AL6060-6R8	6.8µH	MPS
MPL-AL6060-100	10µH	MPS
MPL-AL6060-150	15µH	MPS

Visit MonolithicPower.com under Products > Inductors for more information.

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. Ceramic capacitors are recommended for the best performance, and should be placed as close to the VIN pin as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable amid temperature fluctuations.

The capacitors must also have a ripple current rating exceeding the maximum input ripple current of the converter. The input ripple current (I_{CIN}) can be estimated using Equation (6):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (6)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be estimated using Equation (7):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (7)$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half of the maximum load current.

The input capacitance determines the input voltage ripple (ΔV_{IN}) of the converter. If there is a ΔV_{IN} requirement in the system, choose the input capacitor that meets the relevant specifications.

ΔV_{IN} can be estimated using Equation (8):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{sw} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

Under worst-case conditions where V_{IN} = 2 x V_{OUT}, ΔV_{IN} can be estimated using Equation (9):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{sw} \times C_{IN}} \quad (9)$$

Selecting the Output Capacitor

The output capacitor (C_{OUT}) is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple (ΔV_{OUT}) can be estimated using Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{sw} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (10)$$

With ceramic capacitors, the capacitance dominates the impedance at f_{SW}, and causes the majority of ΔV_{OUT}. For simplification, ΔV_{OUT} can be estimated using Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

ΔV_{OUT} caused by the ESR is very small. With POSCAP capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated using Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (12)$$

Besides considering the output ripple, choosing a larger-value C_{OUT} improves load transient response, but the maximum C_{OUT} limit should also be considered in design applications. If C_{OUT} is too high, V_{OUT} cannot reach the design value during the soft-start time and fails to regulate. The maximum C_{OUT} value (C_{O_MAX}) can be limited using Equation (13):

$$C_{O\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times t_{SS} / V_{OUT} \quad (13)$$

Where I_{LIM_AVG} is the average start-up current during SS, and t_{SS} is the soft-start time.

Design Example

Table 3 is a design example following the application guidelines for the specifications below.

Table 3: Design Example

V_{IN}	V_{OUT}	I_{OUT}
6.5V to 28V	5V	2A

For the detailed application schematic, see Figure 9 on page 20. For the typical performance and circuit waveforms, see the Typical Performance Characteristics section on page 10. For more device applications, refer to the related evaluation board datasheet.

PCB Layout Guidelines

Proper layout of the switching power supplies is important for proper function. Poor layout design can result in poor line or load regulation and stability issues. For the best results, refer to Figure 4 and follow the guidelines below:

1. Place the high-current paths (GND, VIN, and SW) as close to the device as possible with short, direct, and wide traces.
2. Place the input capacitor as close to VIN and GND as possible (it is recommended to be within 1mm).
3. Place the external feedback resistors next to FB.
4. Keep the switching node (SW) short, and route it away from the feedback network.

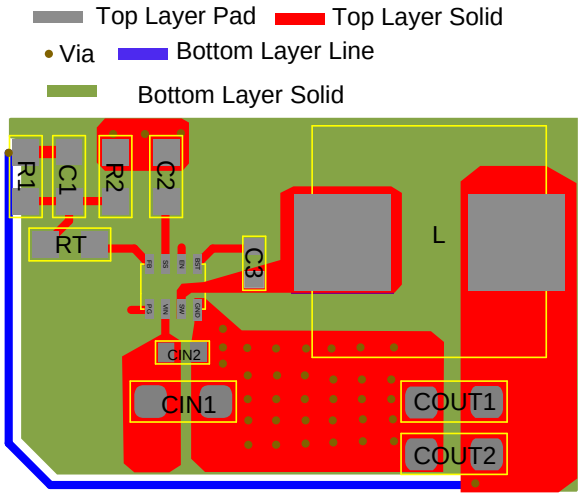


Figure 4: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

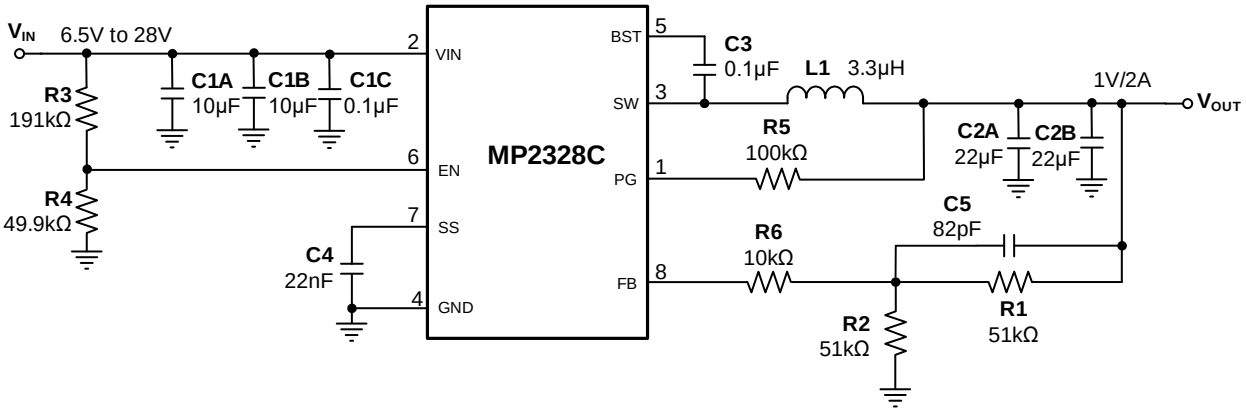


Figure 5: Typical Application Circuit (V_{IN} = 6.5V to 28V, V_{OUT} = 1V, I_{OUT} = 2A)

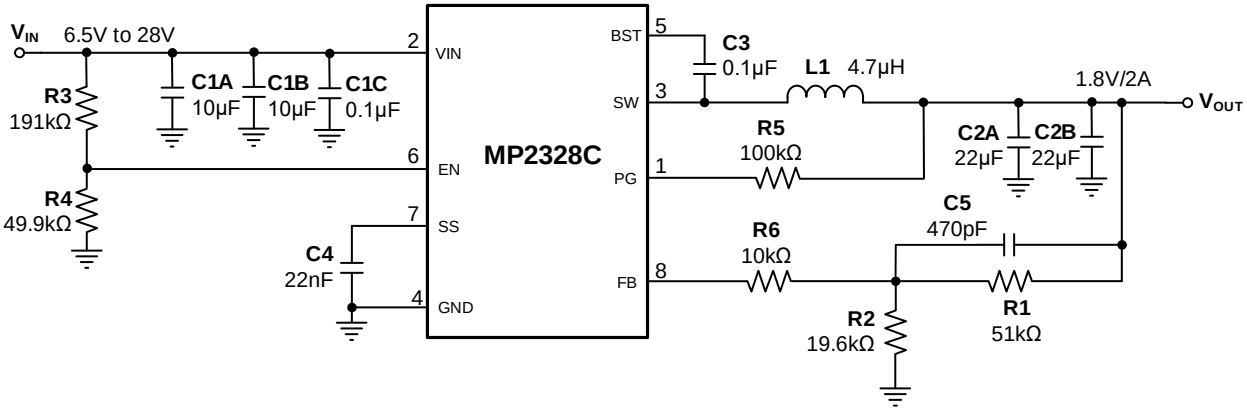


Figure 6: Typical Application Circuit (V_{IN} = 6.5V to 28V, V_{OUT} = 1.8V, I_{OUT} = 2A)

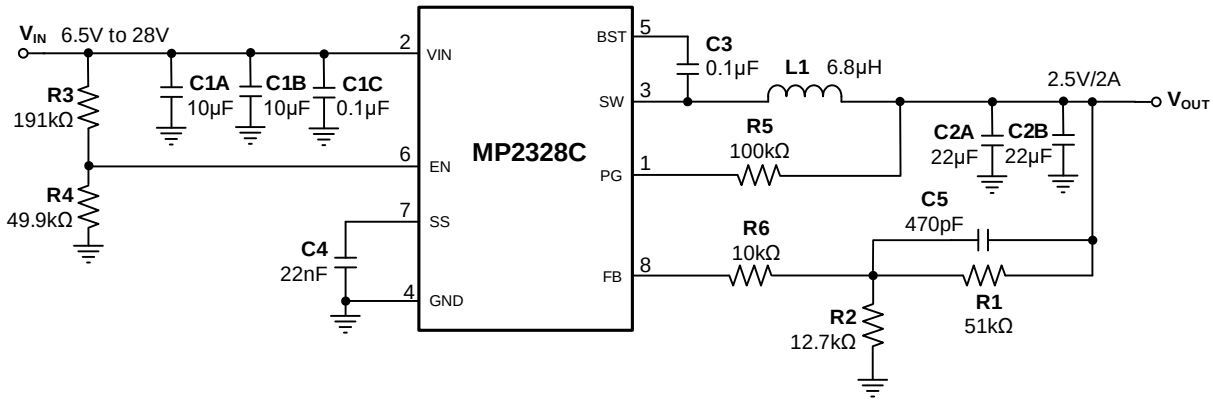


Figure 7: Typical Application Circuit (V_{IN} = 6.5V to 28V, V_{OUT} = 2.5V, I_{OUT} = 2A)

TYPICAL APPLICATION CIRCUITS *(continued)*

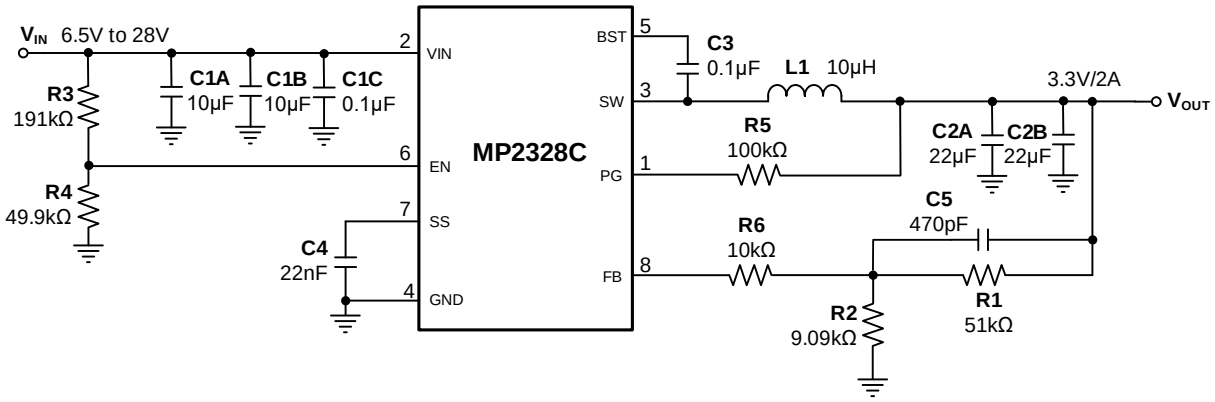


Figure 8: Typical Application Circuit (V_{IN} = 6.5V to 28V, V_{OUT} = 3.3V, I_{OUT} = 2A)

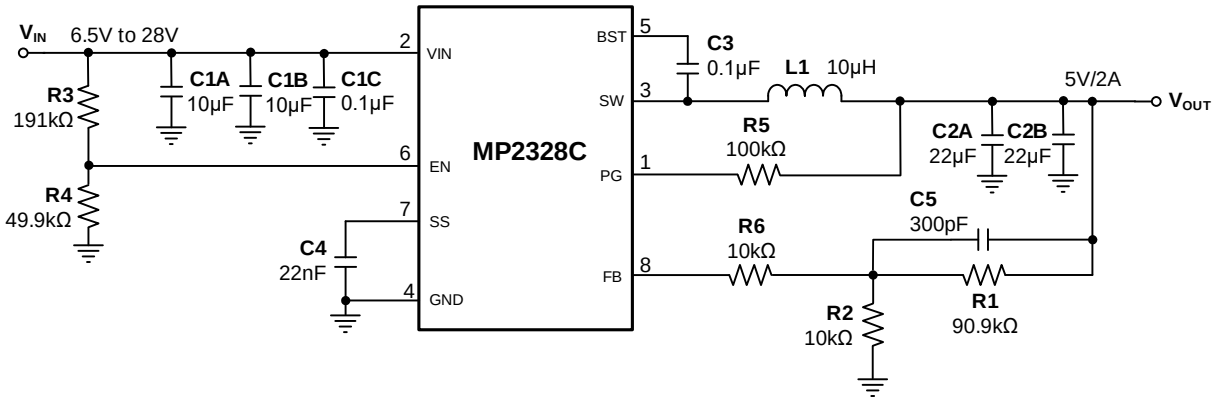


Figure 9: Typical Application Circuit (V_{IN} = 6.5V to 28V, V_{OUT} = 5V, I_{OUT} = 2A)

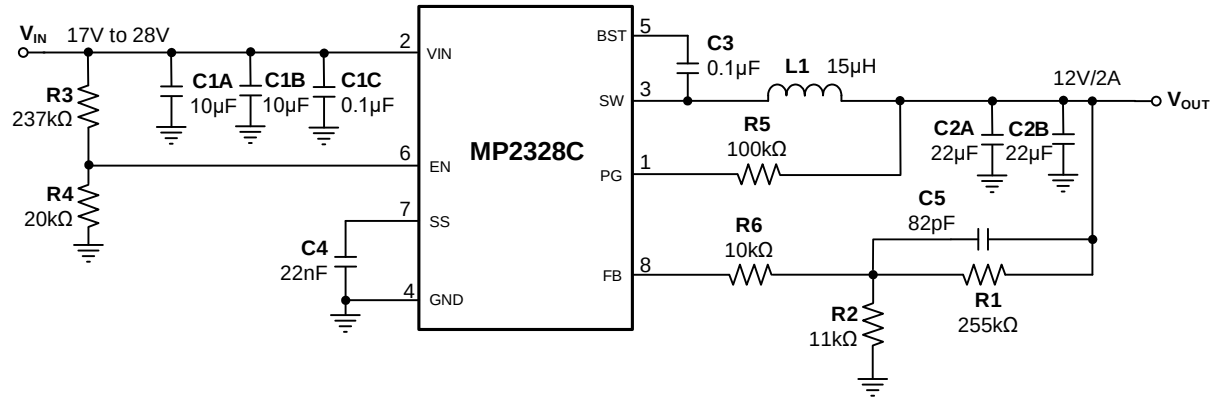
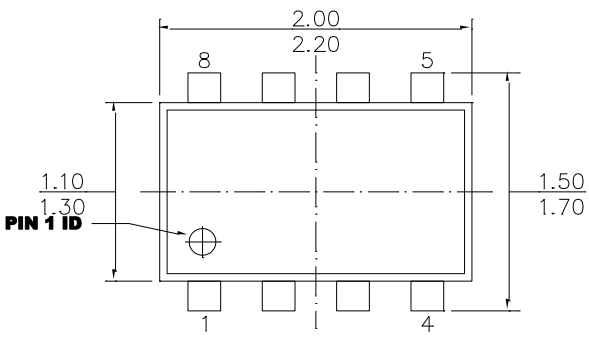


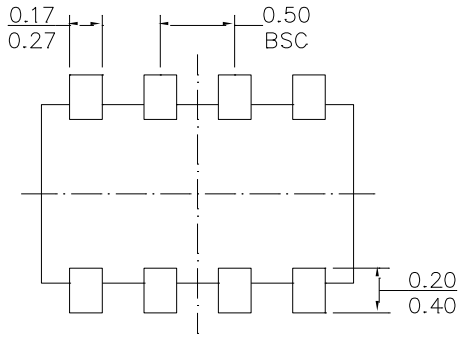
Figure 10: Typical Application Circuit (V_{IN} = 17V to 28V, V_{OUT} = 12V, I_{OUT} = 2A)

PACKAGE INFORMATION

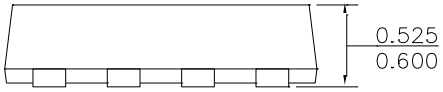
SOT583



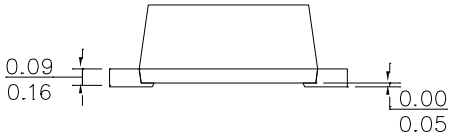
TOP VIEW



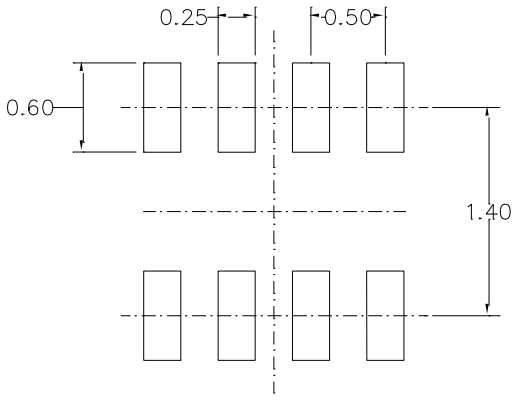
BOTTOM VIEW



FRONT VIEW



SIDE VIEW

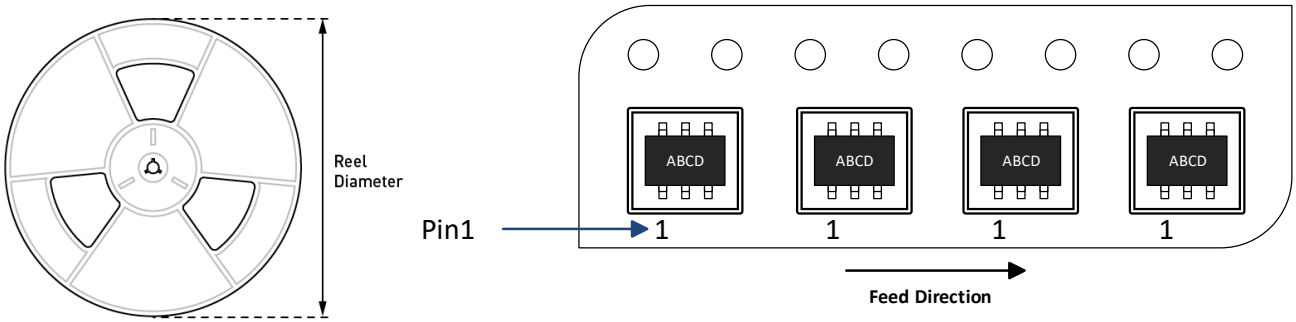


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
3) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity /Reel	Quantity/ Tube	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2328CGTL-Z	SOT583	5000	N/A	N/A	7in	8mm	4mm