MP4432

36V, 2.2A, Low Quiescent Current, Synchronous, Step-Down Converter

DESCRIPTION

The MP4432 is a synchronous, step-down, switching regulator with programmable frequency (350kHz to 2.5MHz) and integrated, internal, high-side and low-side power MOSFETs. The MP4432 provides up to 2.2A of highly efficient output current with current mode control for fast loop response.

The wide 3.3V to 36V input range accommodates a variety of step-down applications in automotive input environments. The MP4432 is ideal for battery-powered applications due to its extremely low quiescent current.

The MP4432 employs advanced asynchronous mode (AAM) to achieve high efficiency in light-load condition by scaling down the switching frequency to reduce switching and gate driving losses.

Standard features include soft start, external clock synchronization, enable control, and power good indication. High-duty cycle and low dropout mode are provided for automotive cold-crank.

Over-current protection (OCP) with valley-current detection is employed to prevent the inductor current from running away. Hiccup mode reduces the average current greatly in short-circuit condition. Thermal shutdown provides reliable and fault-tolerant operation.

The MP4432 is available in a QFN-16 (3mmx4mm) package.

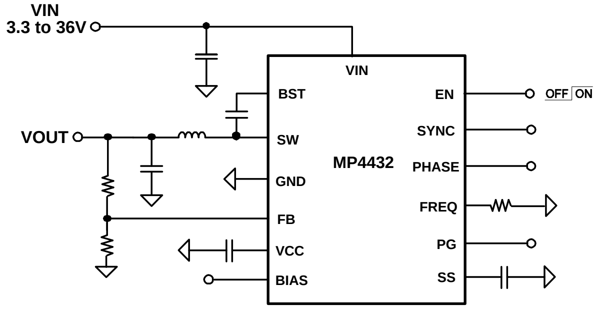
FEATURES

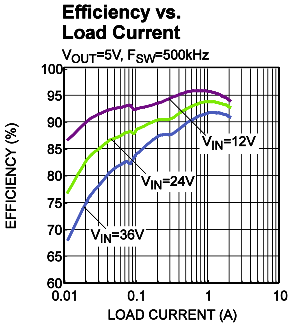
- Wide 3.3V to 36V Operating Input Range
- 2.2A Continuous Output Current
- 1μA Low Shutdown Mode Current
- 10μA Sleep Mode Quiescent Current
- Internal 90mΩ High-Side and 40mΩ Low-Side MOSFETs
- 350kHz to 2.5MHz Programmable Switching Frequency
- Fixed Output Options: 3.3V, 3.8V, 5V
- Synchronize to External Clock, Selectable In-Phase or 180° Out-of-Phase
- Power Good Indicator
- Programmable Soft-Start Time
- 80ns Minimum On Time
- Selectable Forced CCM or AAM
- Low Dropout Mode
- Over-Current Protection (OCP) with Valley-Current Detection and Hiccup
- Available in a QFN-16 (3mmx4mm) Package

APPLICATIONS

- Automotive Systems
- Industrial Power Systems

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP4432GL	QFN-16 (3mmx4mm)	*See Below*

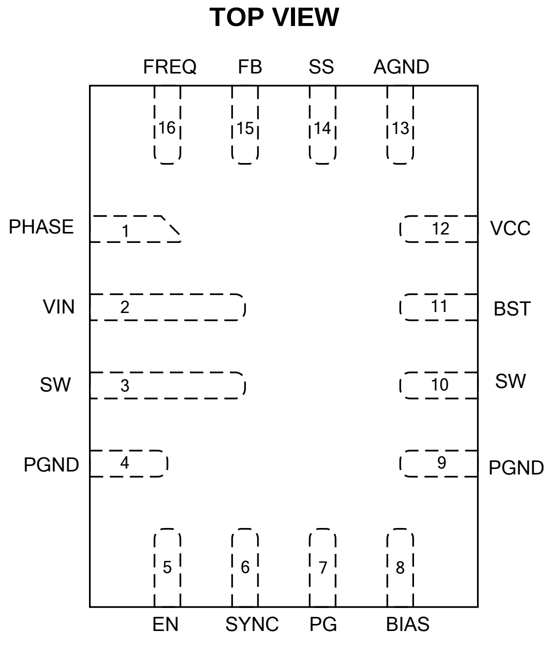
* For Tape & Reel, add suffix –Z (e.g. MP4432GL–Z)

TOP MARKING

MPYW
4432
LLL

MP: MPS prefix
Y: Year code
W: Week code
4432: First four digits of the part number
LLL: Lot number

PACKAGE REFERENCE



QFN-16 (3mmx4mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (VIN)	-0.3V to 40V
Switch voltage (V_{SW})	-0.3V to VIN + 0.3V
BST voltage (V_{BST})	V_{SW} + 6.5V
EN voltage (V_{EN})	-0.3V to 40V
BIAS voltage (V_{BIAS})	-0.3V to 20V
All other pins	-0.3V to 6V
Continuous power dissipation (T_A = +25°C) **(2)**	
QFN-16 (3mmx4mm)	2.6W
Junction temperature	150°C
Lead temperature	260°C
Storage temperature	-65°C to 150°C

Recommended Operating Conditions

Supply voltage (VIN)	3.3V to 36V
Operating junction temp (T_J)	-40°C to +125°C

Thermal Resistance (3)	θ_{JA}	θ_{JC}	
QFN-16 (3mmx4mm)	48	11	°C/W

NOTES:

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VIN = 12V, V_{EN} = 2V, T_J = -40°C to +125°C (4), unless otherwise noted. Typical values are at T_J = +25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VIN quiescent current	I_Q	V_{FB} = 0.85V, no load, no switching, T_J = +25°C		10	18	μA
		V_{FB} = 0.85V, no load, no switching		10	25	
VIN shutdown current	I_{SHDN}	V_{EN} = 0V		1	5	μA
VIN under-voltage lockout threshold rising	$INUV_{RISING}$		2.4	2.8	3.2	V
VIN under-voltage lockout threshold hysteresis	$INUV_{HYS}$			150		mV
Feedback reference voltage	V_{REF}		784	800	816	mV
		T_J = 25°C	792	800	808	mV
Switching frequency	F_{SW}	R_{FREQ} = 180kΩ or from sync clock	400	475	550	kHz
		R_{FREQ} = 82kΩ or from sync clock	850	1000	1150	kHz
		R_{FREQ} = 27kΩ or from sync clock	2250	2500	2750	kHz
Minimum on time (5)	T_{ON_MIN}			80		ns
Sync input low voltage	V_{SYNC_LOW}				0.4	V
Sync input high voltage	V_{SYNC_HIGH}		1.8			V
Current limit	I_{LIMIT_HS}	Duty cycle = 40%	4.1	5.2	6.7	A
Low-side valley current limit	I_{LIMIT_LS}	V_{OUT} = 3.3V, L = 4.7μH	2.5	3.8	5.1	A
ZCD current	I_{ZCD}			0.1		A
Reverse current limit	$I_{LIMIT\_REVERSE}$			3		A
Switch leakage current	I_{SW_LKG}			0.01	1	μA
HS switch on resistance	R_{ON_HS}	V_{BST} - V_{SW} = 5V		90	155	mΩ
LS switch on resistance	R_{ON_LS}			40	75	mΩ
Soft-start current	I_{SS}	V_{SS} = 0.8V	5	10	15	μA
EN rising threshold	V_{EN_RISING}		0.9	1.05	1.2	V
EN threshold hysteresis	V_{EN_HYS}			120		mV
PG rising threshold (V_{FB}/V_{REF})	PG_{RISING}	V_{FB} rising	85	90	95	%
		V_{FB} falling	105	110	115	
PG falling threshold (V_{FB}/V_{REF})	$PG_{FALLING}$	V_{FB} falling	79	84	89	%
		V_{FB} rising	113.5	118.5	123.5	%
PG deglitch timer	$T_{PG\_DEGLITCH}$	PG from low to high		30		μs
		PG from high to low		50		μs
PG output voltage low	V_{PG_LOW}	I_{SINK} = 2mA		0.2	0.4	V
VCC regulator	V_{CC}			5		V
VCC load regulation		I_{CC} = 5mA			3	%
Thermal shutdown (5)	T_{SD}			170		°C
Thermal shutdown hysteresis (5)	T_{SD_HYS}			20		°C

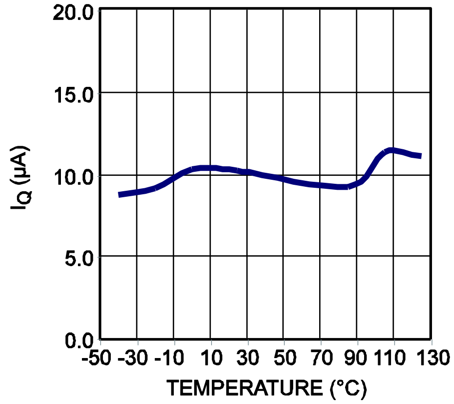
NOTE:

4) Not tested in production and guaranteed by over-temperature correlation.
5) Not tested in production. Guaranteed by design and characterization.

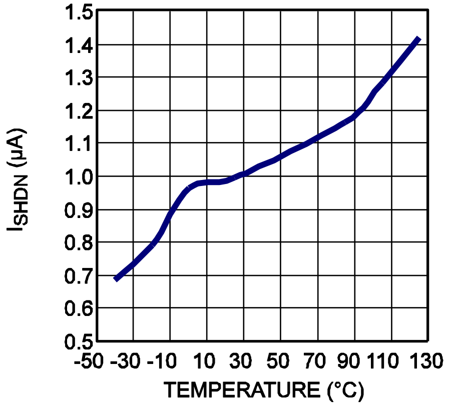
TYPICAL CHARACTERISTICS

VIN = 12V, T_J = -40°C to +125°C, unless otherwise noted.

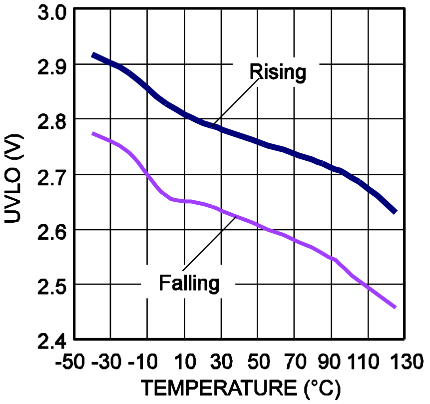
Quiescent Current vs. Temperature



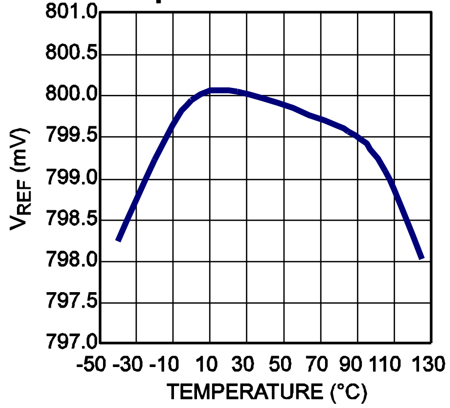
Shutdown Current vs. Temperature



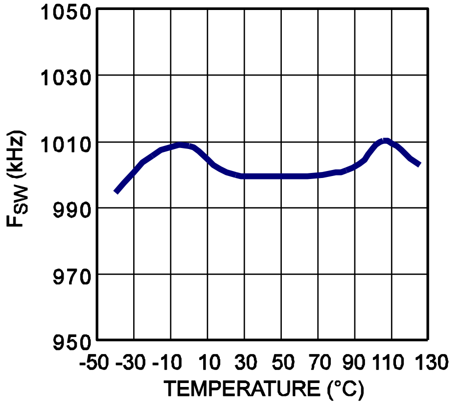
VIN UVLO Threshold vs. Temperature



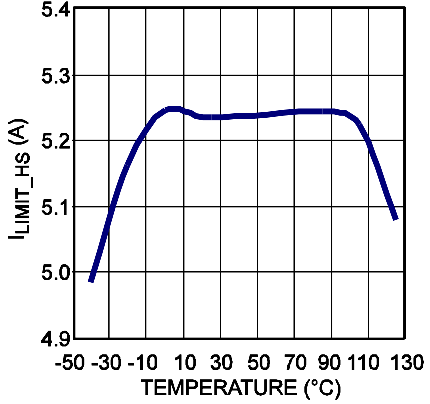
Feedback Reference vs. Temperature



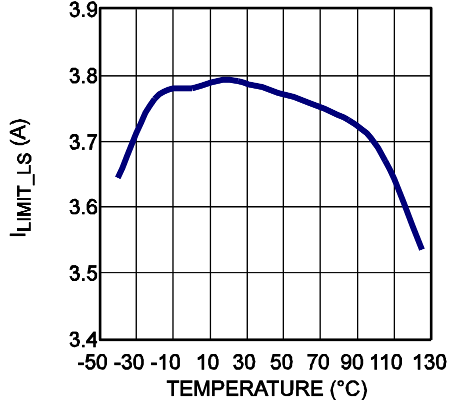
Switching Frequency vs. Temperature



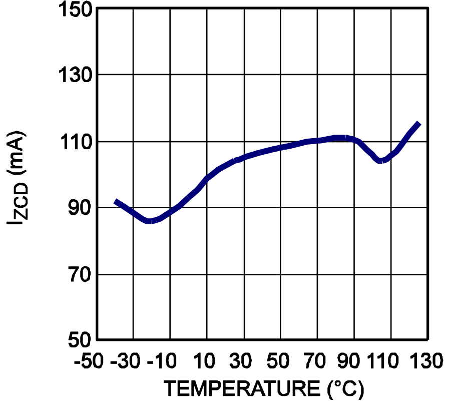
Current Limit vs. Temperature



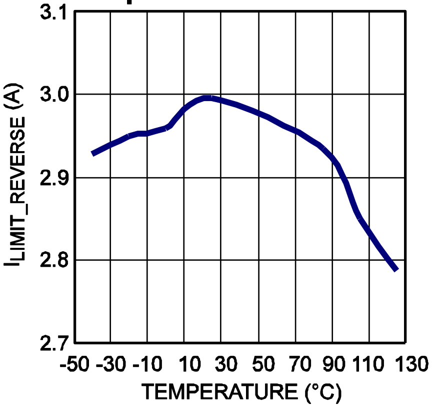
Valley Current Limit vs. Temperature



ZCD Current vs. Temperature



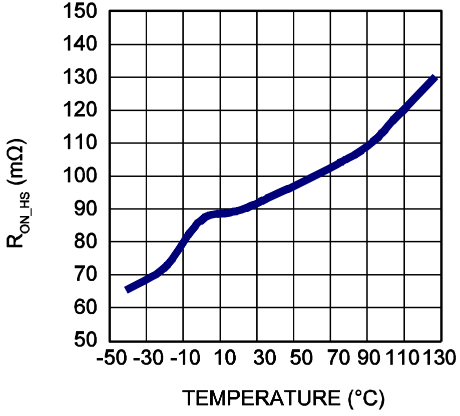
Reverse Current Limit vs. Temperature



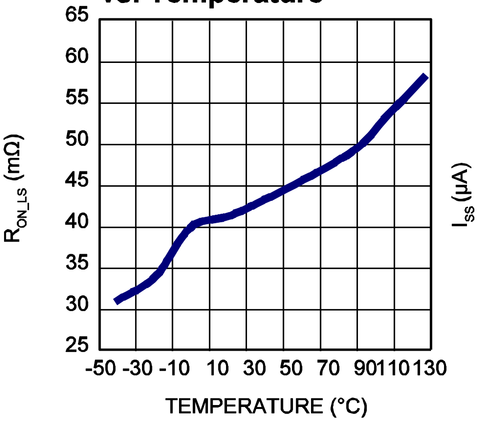
TYPICAL CHARACTERISTICS *(continued)*

VIN = 12V, T_J = -40°C to +125°C, unless otherwise noted.

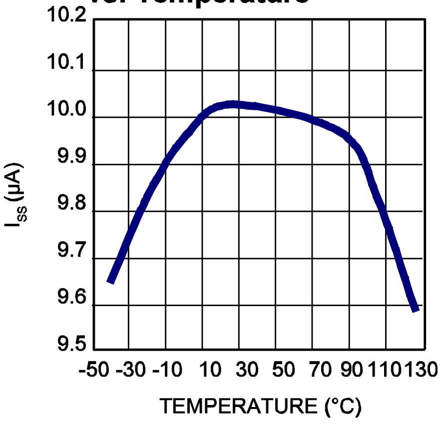
HS-FET On Resistance vs. Temperature



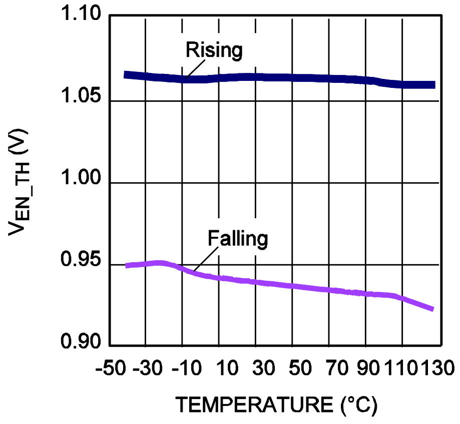
LS-FET On Resistance vs. Temperature



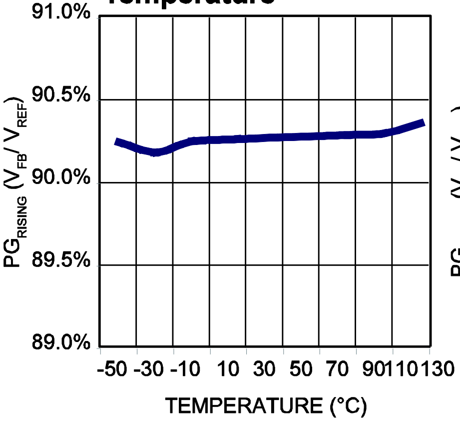
Soft-Start Current vs. Temperature



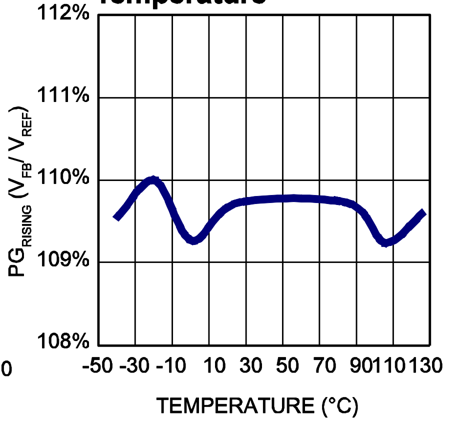
EN Threshold vs. Temperature



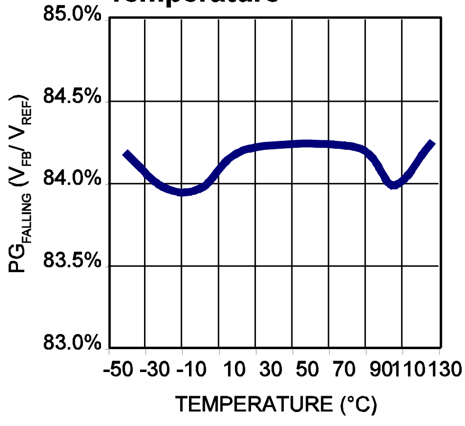
PG Rising Threshold (V_{FB} Rising) vs. Temperature



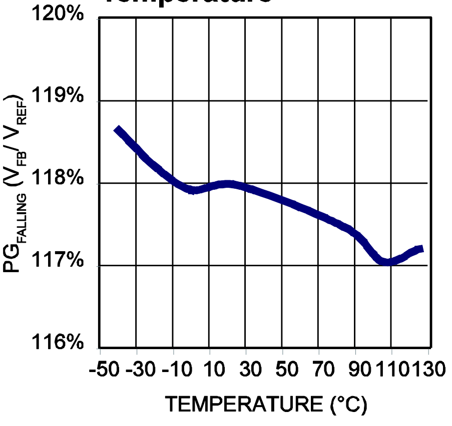
PG Rising Threshold (V_{FB} Falling) vs. Temperature



PG Falling Threshold (V_{FB} Falling) vs. Temperature

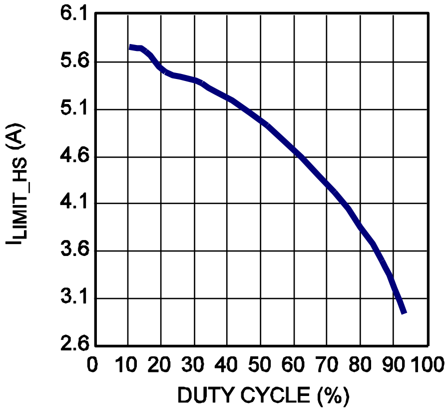


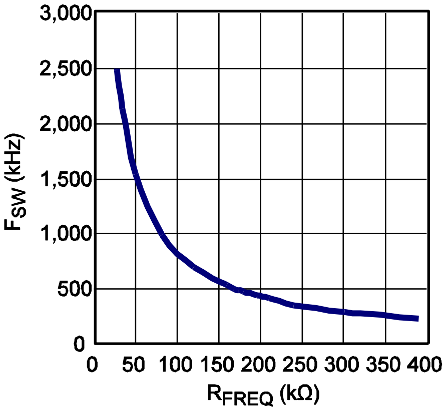
PG Falling Thershold (V_{FB} Rising) vs. Temperature

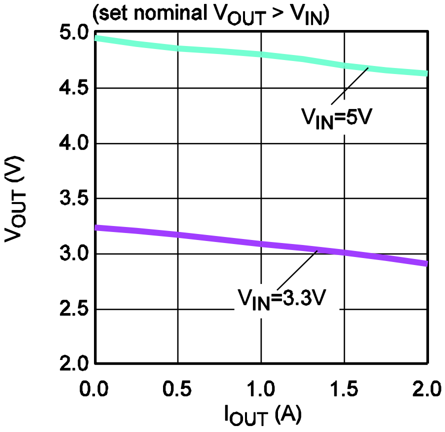


TYPICAL PERFORMANCE CHARACTERISTICS

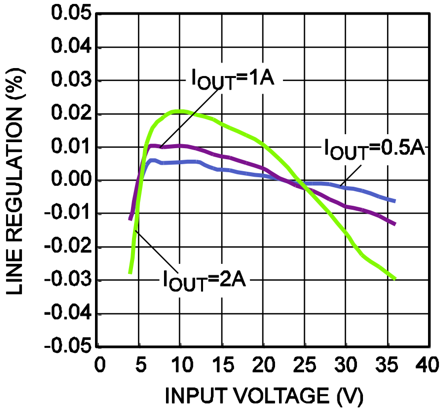
VIN = 12V, V_{OUT} = 3.3V, L = 10µH, F_{SW} = 500kHz, AAM, T_A = +25°C, unless otherwise noted.

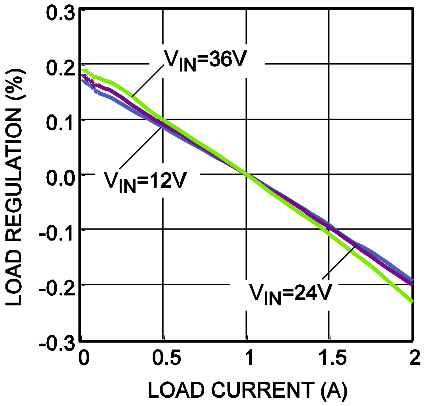

Current Limit vs. Duty Cycle


F_{SW} vs. R_{FREQ}


Output Voltage vs. Load Current

Dropout Performance
(set nominal V_{OUT} > V_{IN})

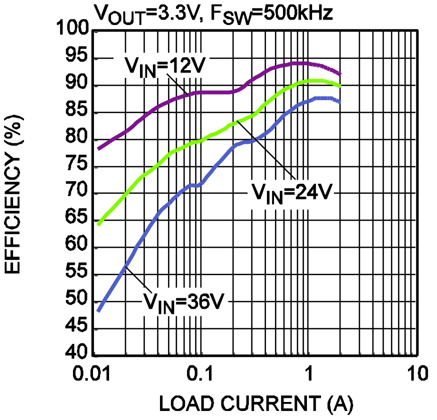

Line Regulation


Load Regulation

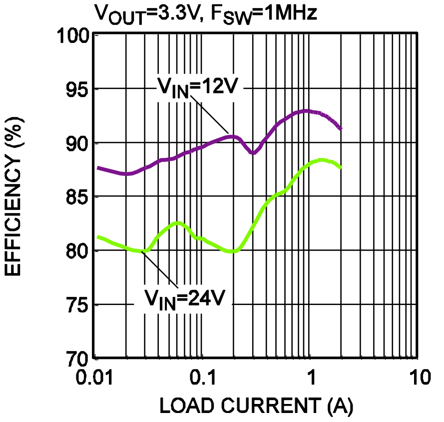
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 3.3V, L = 10µH, F_{SW} = 500kHz, AAM, T_A = +25°C, unless otherwise noted.

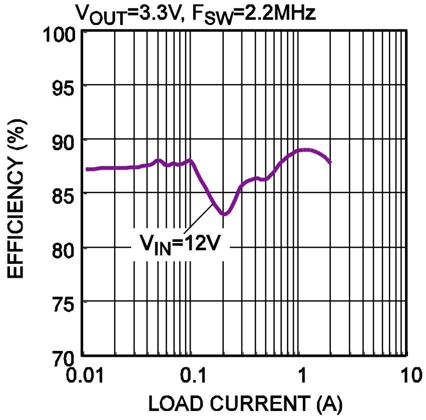
Efficiency vs. Load Current



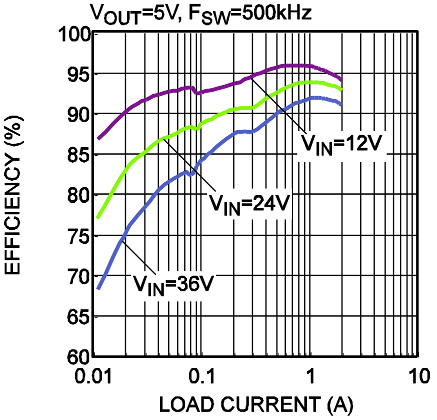
Efficiency vs. Load Current



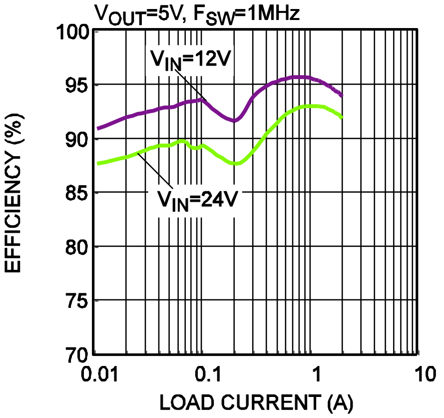
Efficiency vs. Load Current



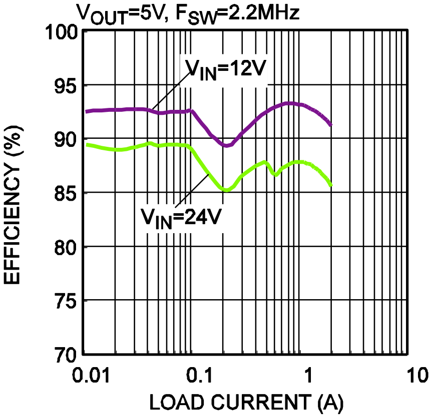
Efficiency vs. Load Current



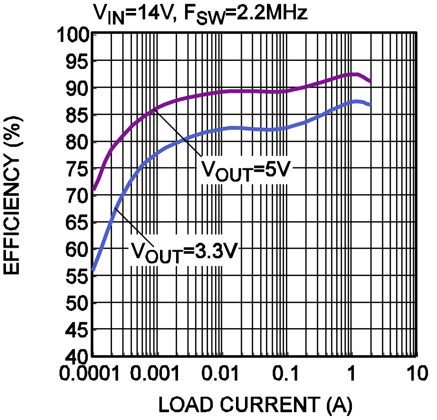
Efficiency vs. Load Current



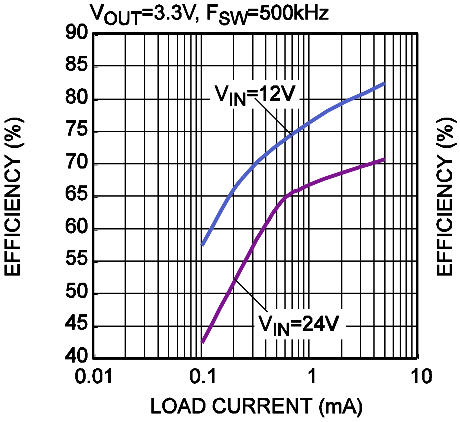
Efficiency vs. Load Current



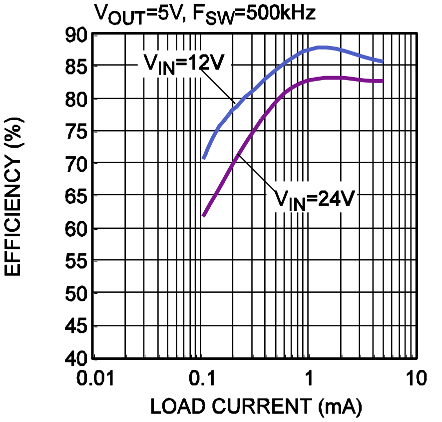
Efficiency vs. Load Current



Efficiency vs. Load Current (Extreme Light Load)



Efficiency vs. Load Current (Extreme Light Load)

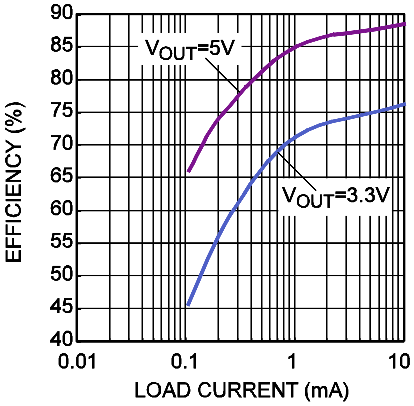


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 3.3V, L = 10µH, F_{SW} = 500kHz, AAM, T_A = +25°C, unless otherwise noted.

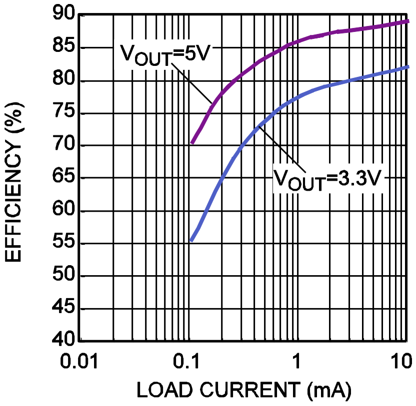
Efficiency vs. Load Current (Extreme Light Load)

V_{IN}=14V, F_{SW}=400kHz



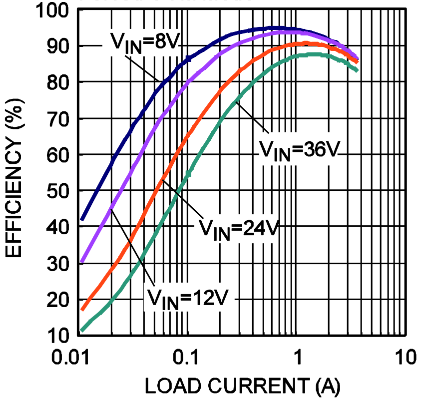
Efficiency vs. Load Current (Extreme Light Load)

V_{IN}=14V, F_{SW}=2.2MHz



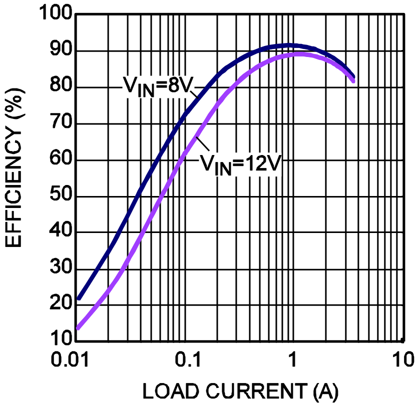
Efficiency vs. Load Current

V_{OUT}=3.3V, F_{SW}=500kHz,
Forced CCM Mode



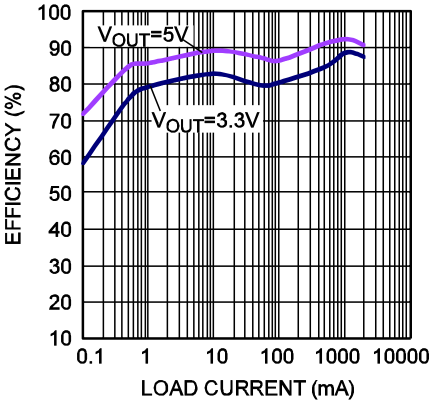
Efficiency vs. Load Current

V_{OUT}=3.3V, F_{SW}=2.2MHz,
Forced CCM Mode



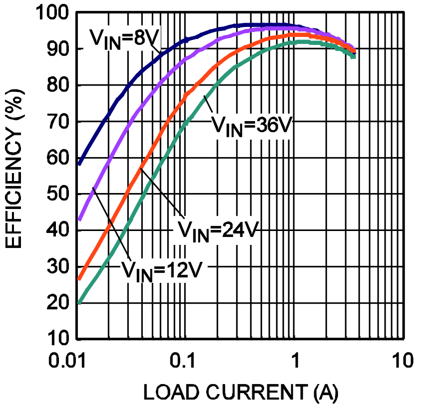
Efficiency vs. Load Current

V_{IN}=12V, F_{SW}=2.2MHz, L=2.2µH



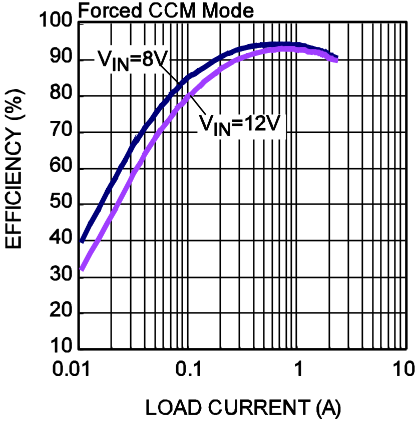
Efficiency vs. Load Current

V_{OUT}=5V, F_{SW}=500kHz,
Forced CCM Mode



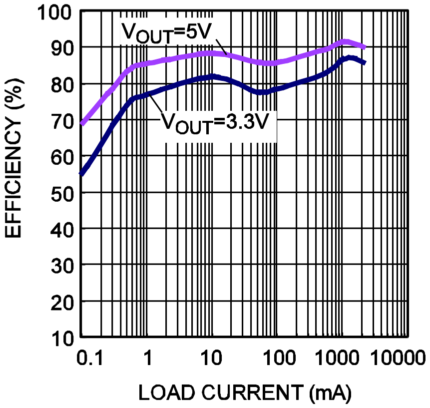
Efficiency vs. Load Current

V_{OUT}=5V, F_{SW}=2.2MHz,
Forced CCM Mode



Efficiency vs. Load Current

V_{IN}=14V, F_{SW}=2.2MHz, L=2.2µH

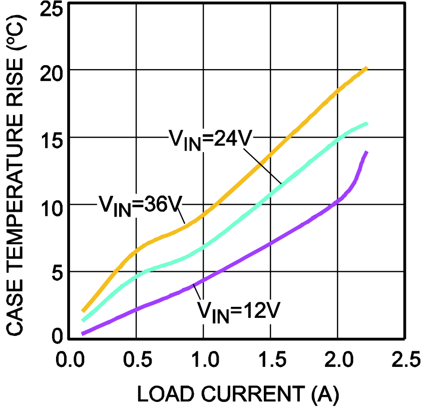


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 3.3V, L = 10µH, F_{SW} = 500kHz, AAM, T_A = +25°C, unless otherwise noted.

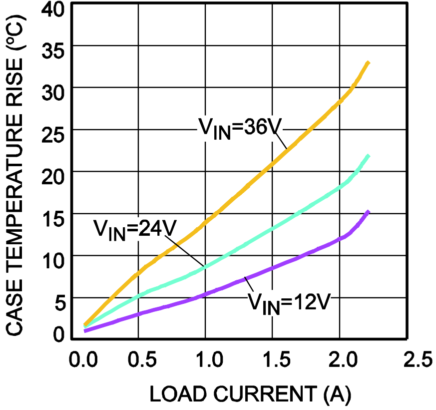
Case Temperature Rise vs. Load Current

V_{OUT}=3.3V, F_{SW}=500kHz



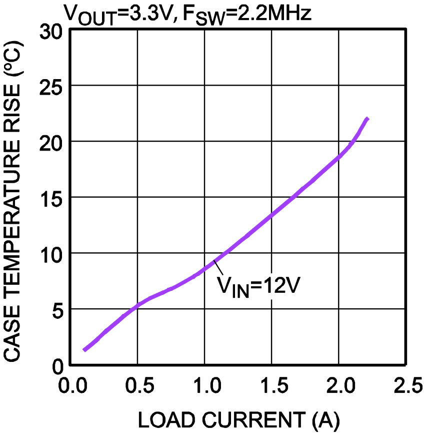
Case Temperature Rise vs. Load Current

V_{OUT}=3.3V, F_{SW}=1MHz



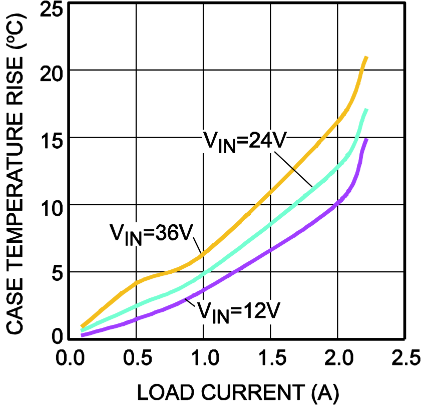
Case Temperature Rise vs. Load Current

V_{OUT}=3.3V, F_{SW}=2.2MHz



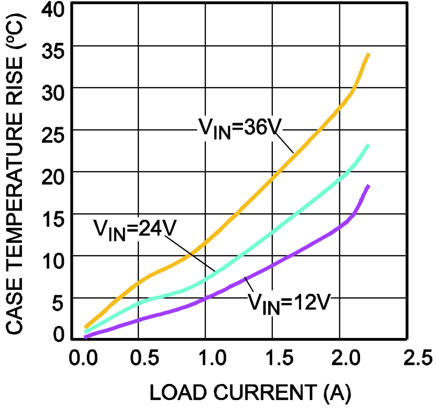
Case Temperature Rise vs. Load Current

V_{OUT}=5V, F_{SW}=500kHz



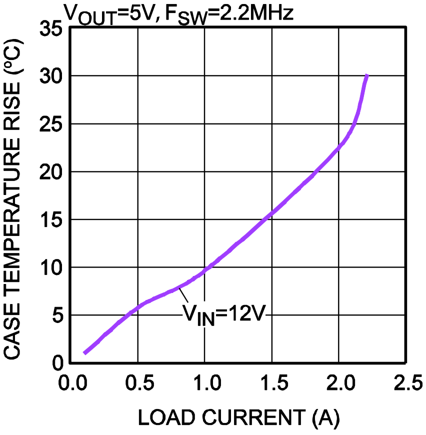
Case Temperature Rise vs. Load Current

V_{OUT}=5V, F_{SW}=1MHz



Case Temperature Rise vs. Load Current

V_{OUT}=5V, F_{SW}=2.2MHz

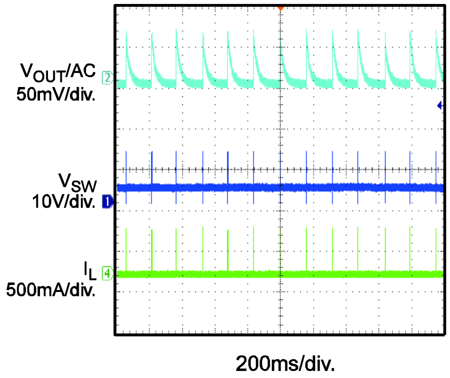


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 3.3V, L = 10µH, F_{SW} = 500kHz, AAM, T_A = +25°C, unless otherwise noted.

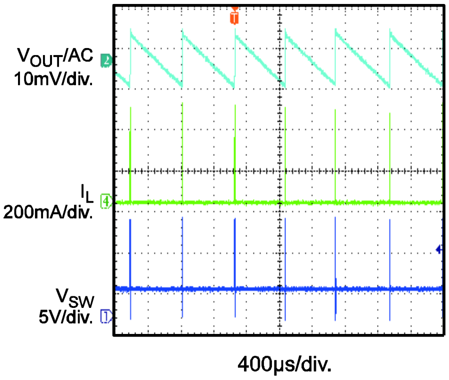
Steady State

I_{OUT}=0A, AAM mode



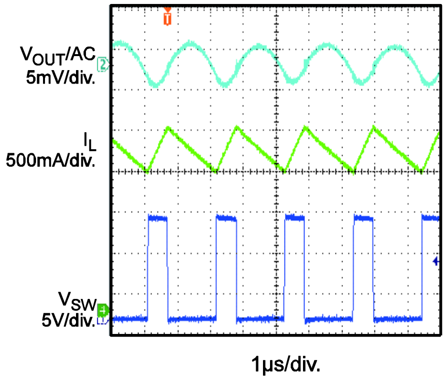
Steady State

I_{OUT}=1mA, AAM mode



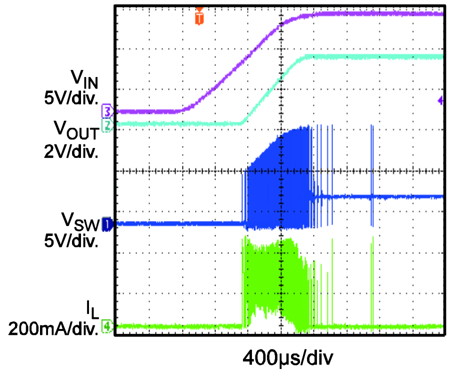
Steady State

I_{OUT}=2A



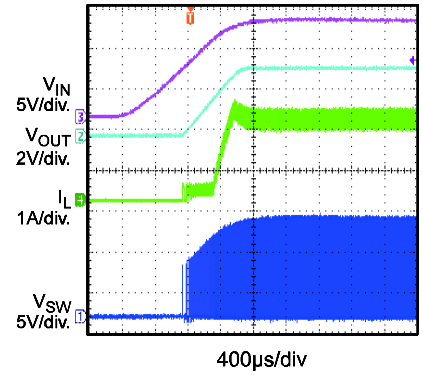
Start-Up through VIN

I_{OUT}=0A



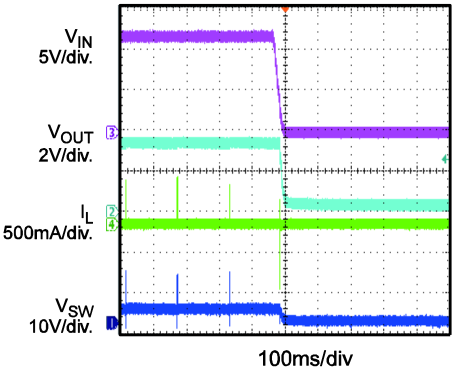
Start-Up through VIN

I_{OUT}=2A



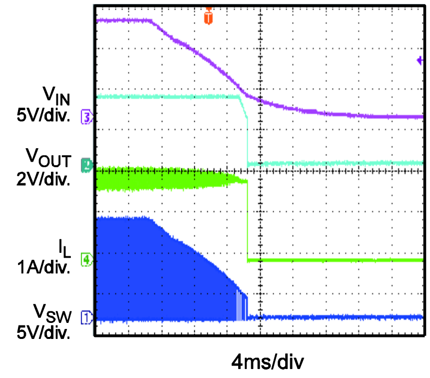
Shutdown through VIN

I_{OUT}=0A



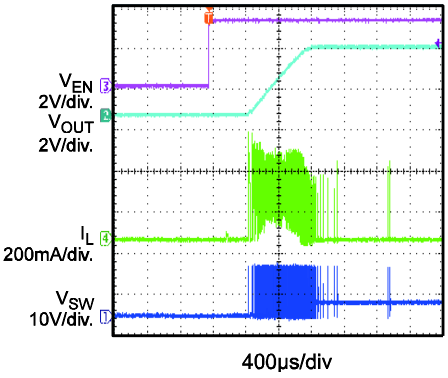
Shutdown through VIN

I_{OUT}=2A



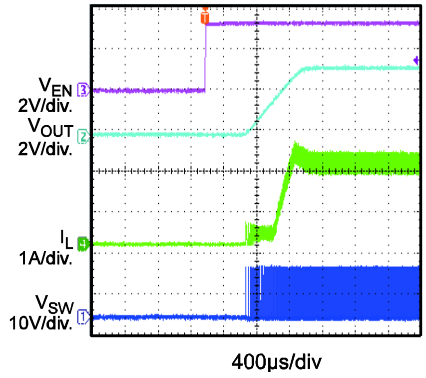
Start-Up through EN

I_{OUT}=0A



Start-Up through EN

I_{OUT}=2A

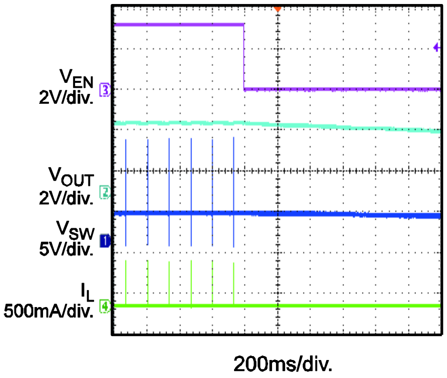


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 3.3V, L = 10µH, F_{SW} = 500kHz, AAM, T_A = +25°C, unless otherwise noted.

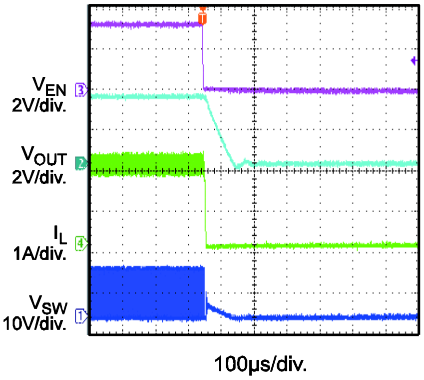
Shutdown through EN

I_{OUT}=0A



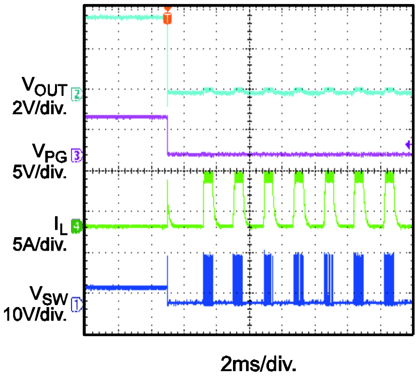
Shutdown through EN

I_{OUT}=2A



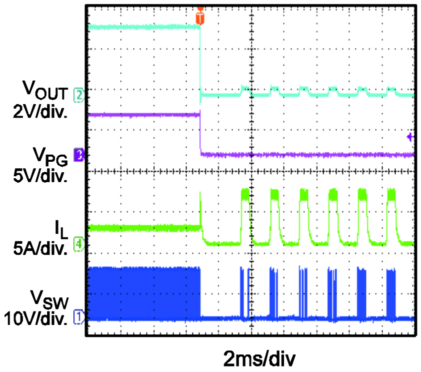
SCP Entry

I_{OUT}=0A to short circuit

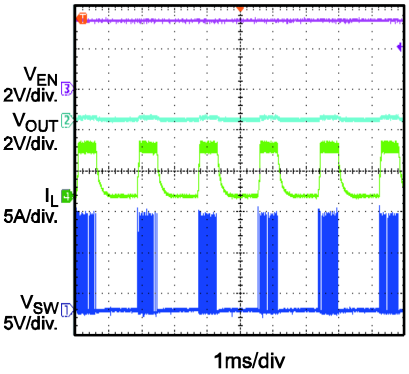


SCP Entry

I_{OUT}=2A to short circuit

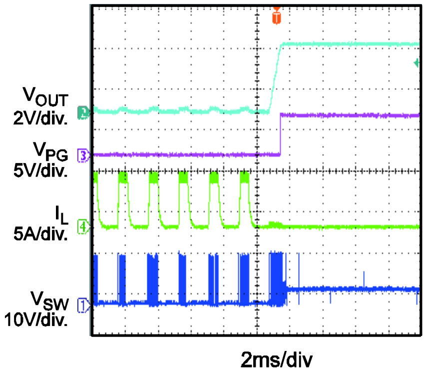


SCP Steady State



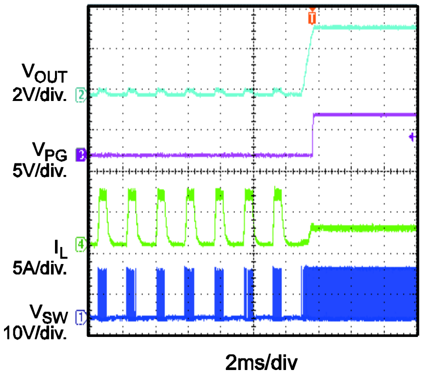
SCP Recovery

short circuit to I_{OUT}=0A



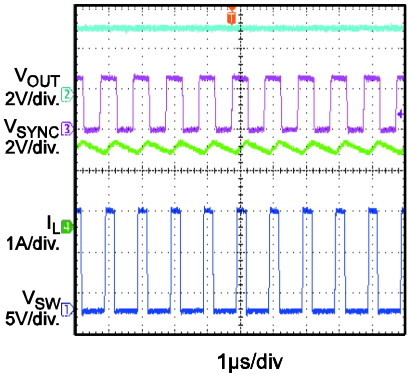
SCP Recovery

short circuit to I_{OUT}=2A



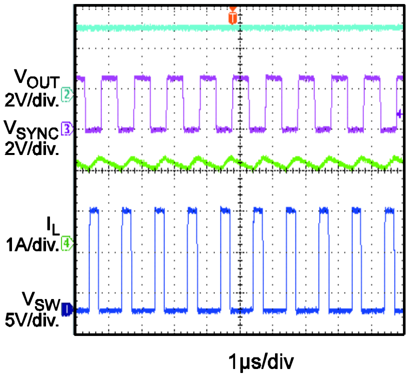
SYNC Operation (In-Phase)

drive PHASE high, I_{OUT}=2A



SYNC Operation (180° Out-of-Phase)

drive PHASE low, I_{OUT}=2A

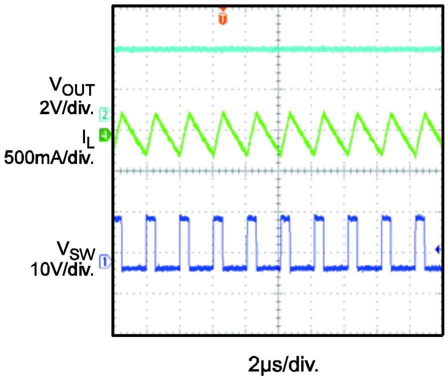


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 3.3V, L = 10μH, F_{SW} = 500kHz, AAM, T_A = +25°C, unless otherwise noted.

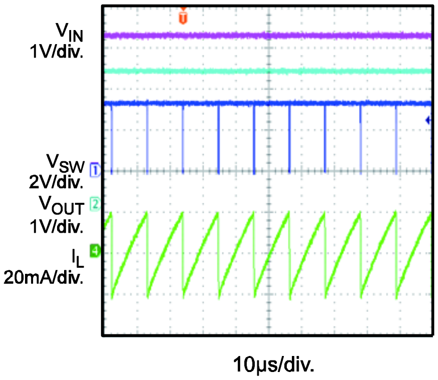
Forced CCM Operation

I_{OUT}=0A, forced CCM mode



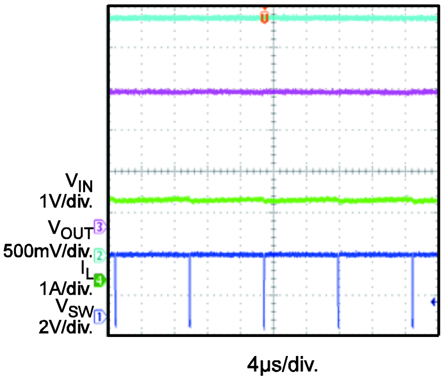
Dropout Operation

V_{IN}=3.3V, V_{OUT} set to3.3V, I_{OUT}=0A



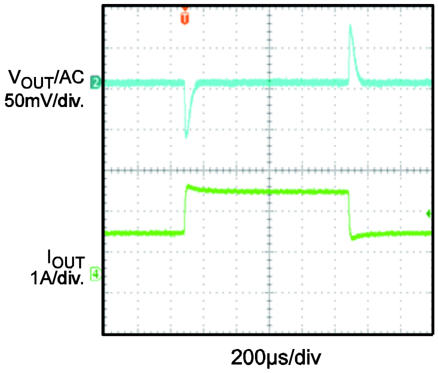
Dropout Operation

V_{IN}=3.3V, V_{OUT} set to3.3V, I_{OUT}=2A



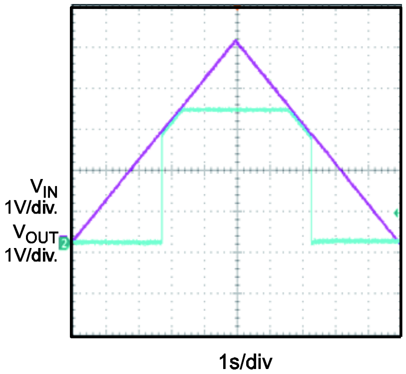
Load Transient

IOUT=1A<->2A, 1.6A/μs



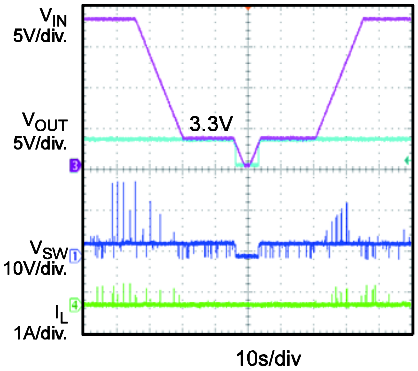
VIN Ramp Up and Down

I_{OUT}=0.1A



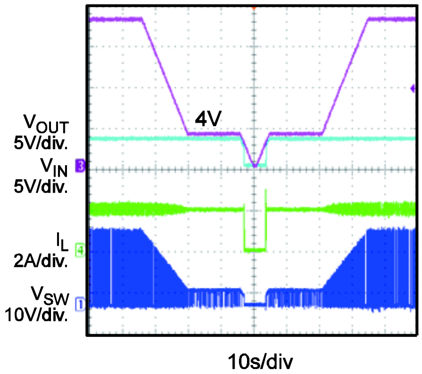
VIN Ramp Down and Up

I_{OUT}=1mA



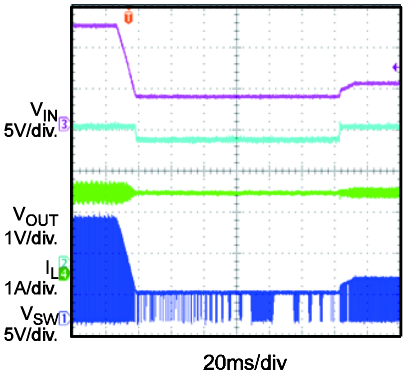
VIN Ramp Down and Up

I_{OUT}=2A



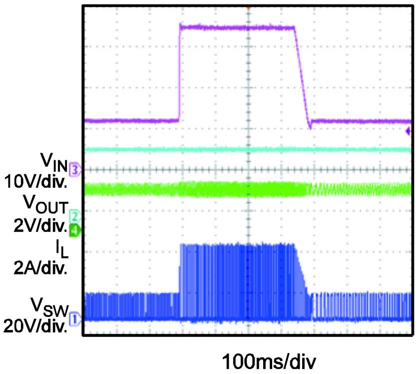
Cold Crank

V_{IN}=12V->3.3V->5V, I_{OUT}=2A



Load Dump

V_{IN}=12V<->36V, I_{OUT}=2A

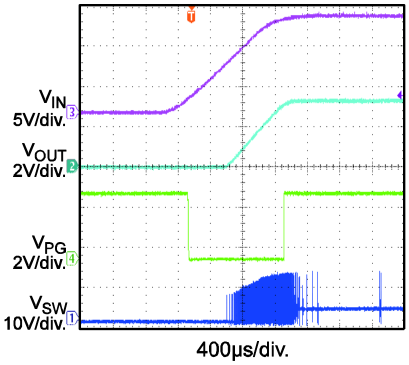


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 3.3V, L = 10µH, F_{SW} = 500kHz, AAM, T_A = +25°C, unless otherwise noted.

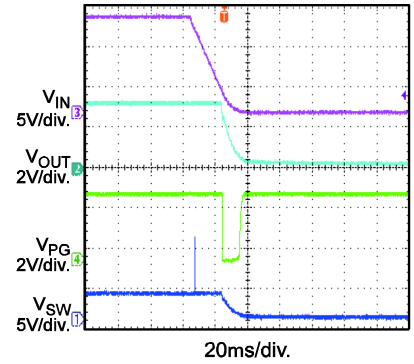
PG in Start-Up through VIN

I_{OUT} = 0A, PG is Pulled to 3.3V through 100k Resistor



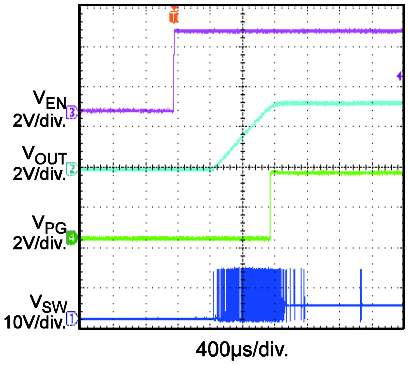
PG in Shutdown through VIN

I_{OUT} = 0A, PG is Pulled to 3.3V through 100k Resistor



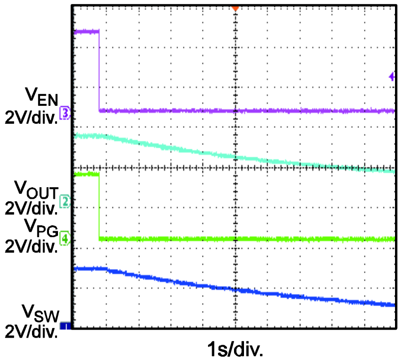
PG in Start-Up through EN

I_{OUT} = 0A, PG is Pulled to 3.3V through 100k Resistor



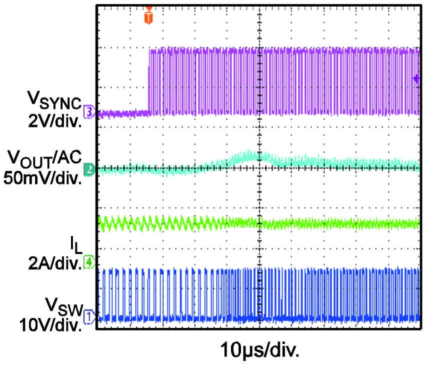
PG in Shutdown through EN

I_{OUT} = 0A, PG is Pulled to 3.3V through 100k Resistor



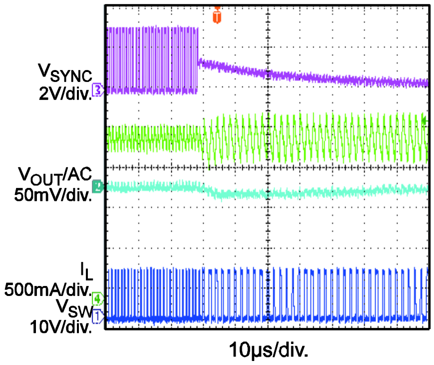
Sync In Transient

I_{OUT} = 2A, SYNC = 1MHz



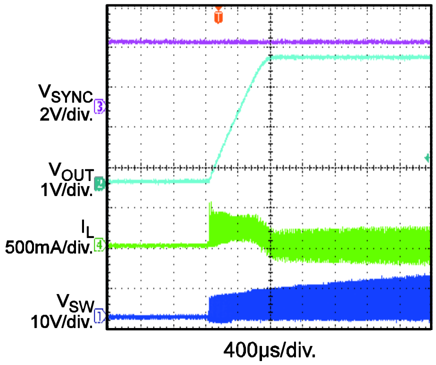
Sync Out Transient

I_{OUT} = 2A, SYNC = 1MHz



Forced CCM Entry

I_{OUT} = 0A, Pull Sync High before Startup



PIN FUNCTIONS

Pin #	Name	Description
1	PHASE	**Selectable in-phase or 180° out-of-phase of SYNC input.** Drive PHASE high to be in-phase; drive PHASE low to be 180° out-of-phase.
2	VIN	**Input supply.** VIN supplies power to all of the internal control circuitries and the power switch connected to SW. Place a decoupling capacitor to ground close to VIN to minimize switching spikes.
3, 10	SW	**Switch node.** SW is the output of the internal power switch.
4, 9	PGND	**Power ground.** PGND is the reference ground of the power device. PGND requires careful consideration during PCB layout. For best results, connect PGND with copper pours and vias.
5	EN	**Enable.** Pull EN below the specified threshold to shut down the chip. Pull EN above the specified threshold to enable the chip.
6	SYNC	**Synchronize.** Apply a 350kHz to 2.5MHz clock signal to SYNC to synchronize the internal oscillator frequency to the external clock. The external clock should be at least 250kHz larger than the R_{FREQ} set frequency. SYNC can also be used to select forced CCM or AAM. Drive SYNC high before the chip starts up to choose forced CCM; drive SYNC low or leave SYNC floating to choose AAM.
7	PG	**Power good indicator.** The output of PG is an open drain. PG goes high if the output voltage is within ±10% of the nominal voltage.
8	BIAS	**External power supply for the internal regulator.** Connecting BIAS to an external power supply ($5V \le V_{BIAS} \le 18V$) reduces power dissipation and increases efficiency. Float BIAS or connect BIAS to ground if it is not being used.
11	BST	**Bootstrap.** BST is the positive power supply for the high-side MOSFET driver connected to SW. Connect a bypass capacitor between BST and SW.
12	VCC	**Internal bias supply.** VCC supplies power to the internal control circuit and gate drivers. A ≥1µF decoupling capacitor to ground is required close to VCC.
13	AGND	**Analog ground.** AGND is the reference ground of the logic circuit.
14	SS	**Soft-start input.** Place an external capacitor from SS to AGND to set the soft-start period. The MP4432 sources 10µA from SS to the soft-start capacitor at start-up. As the SS voltage rises, the feedback threshold voltage increases to limit inrush current during start-up.
15	FB	**Feedback input.** Connect FB to the tap of an external resistor divider from the output to AGND to set the output voltage. The feedback threshold voltage is 0.8V. Place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces.
16	FREQ	**Switching frequency program.** Connect a resistor from FREQ to ground to set the switching frequency.

BLOCK DIAGRAM

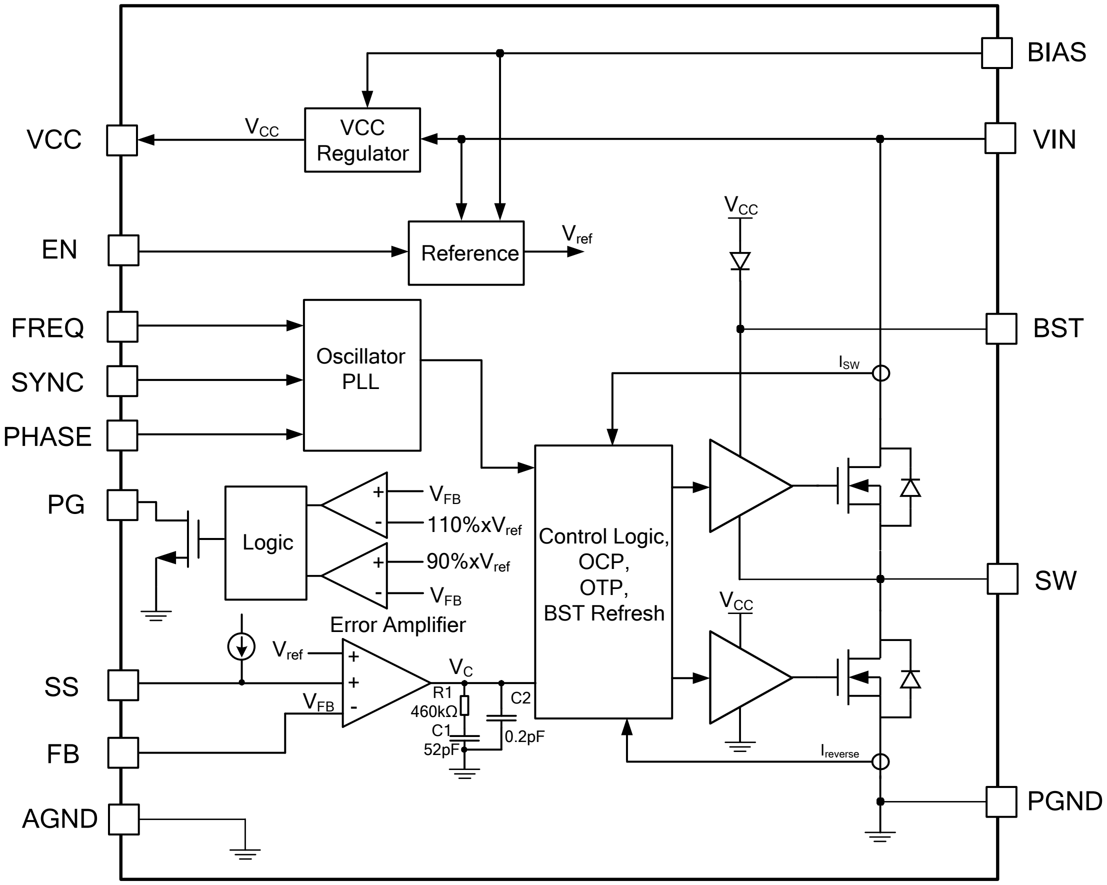


Figure 1: Functional Block Diagram

TIMING SEQUENCE

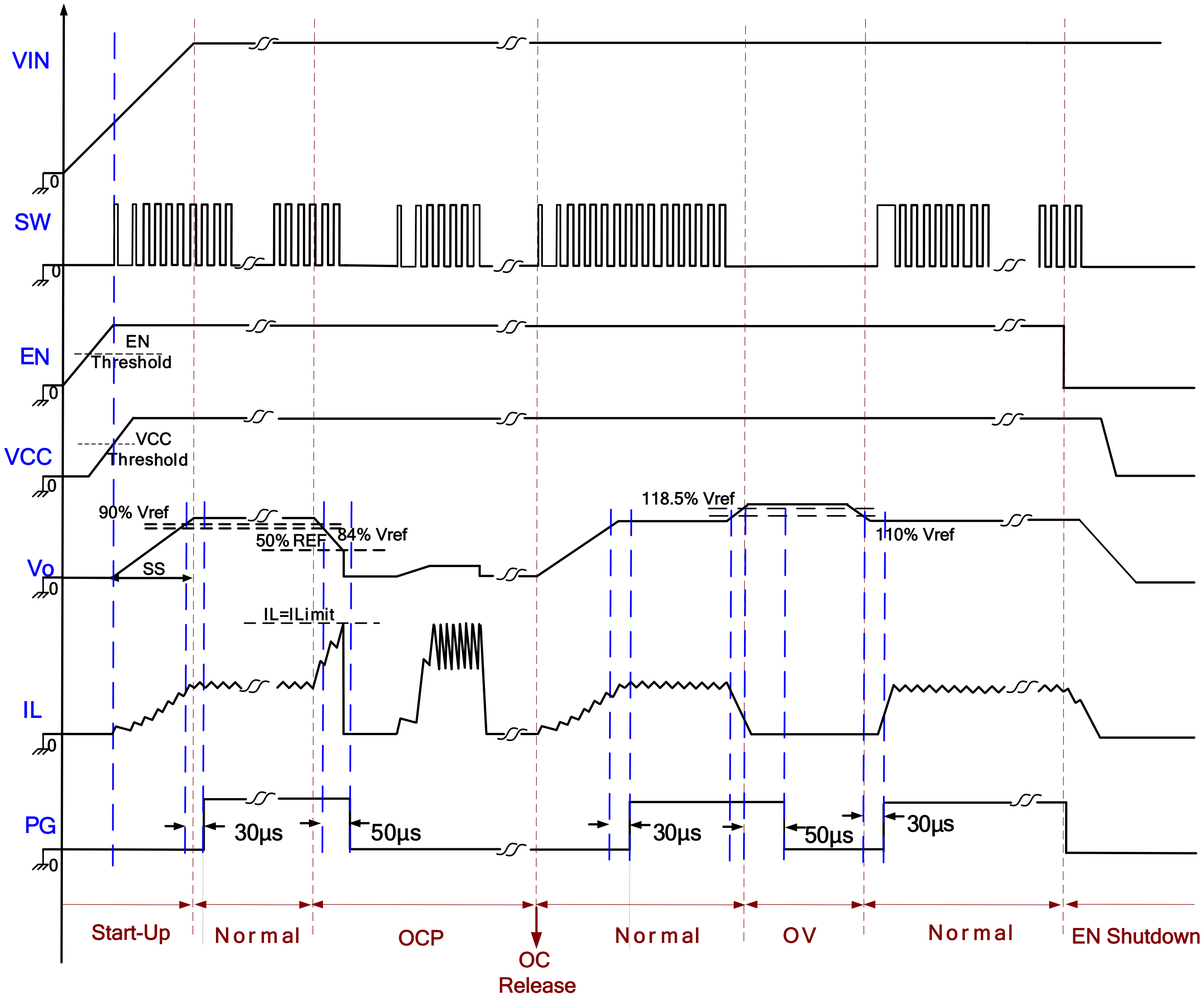


Figure 2: Timing Sequence

OPERATION

The MP4432 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with integrated, internal, high-side and low-side power MOSFETs. The MP4432 offers a very compact solution that achieves 2.2A of continuous output current with excellent load and line regulation over a wide 3.3V to 36V input supply range. The MP4432 features switching frequency programmable from 350kHz to 2.5MHz, external soft start, power good indication, and precision current limit. Its very low operational quiescent current makes it suitable for battery-powered applications.

Pulse Width Modulation (PWM) Control

At moderate-to-high output current, the MP4432 operates in a fixed-frequency, peak-current-control mode to regulate the output voltage. An internal clock initiates a PWM cycle. At the rising edge of the clock, the high-side power MOSFET (HS-FET) is turned on, and the inductor current rises linearly to provide energy to the load. The HS-FET remains on until its current reaches the value set by the COMP voltage (V_{COMP}), which is the output of the internal error amplifier. If the current in the HS-FET does not reach V_{COMP} in one PWM period, the HS-FET remains on, saving a turn-off operation. When the HS-FET is off, it remains off until the next clock cycle begins. The low-side MOSFET (LS-FET) turns on immediately while the inductor current flows through it. To avoid a shoot-through, dead time is inserted to prevent the HS-FET and LS-FET from turning on at the same time. For each turn on and turn off in a switching cycle, the HS-FET remains on and off with a minimum on and off time limit.

Forced CCM and AAM

The MP4432 has selectable forced continuous conduction mode (CCM) and advanced asynchronous mode (AAM) (see Figure 3). Drive SYNC above its specified threshold before the chip starts up to force the device into CCM with a fixed frequency, regardless of the output load current. Once the device is in CCM, SYNC can be pulled low again or driven with an external clock if needed. The advantage of CCM is a controllable frequency and smaller output ripple, but it also has low efficiency at light load.

Drive SYNC below its specified threshold or leave SYNC floating before the chip starts up to enable AAM power-save mode. The MP4432 first enters non-synchronous operation for as long as the inductor current approaches zero at light load. If the load is further decreased or is at no load, making V_{COMP} below the internally set AAM value (V_{AAM}), the MP4432 enters sleep mode, consuming very low quiescent current to further improve light-load efficiency.

In sleep mode, the internal clock is blocked first, and the MP4432 skips some pulses. Since the FB voltage (V_{FB}) is lower than the internal 0.8V reference (V_{REF}), V_{COMP} ramps up until it crosses over V_{AAM}. Then the internal clock is reset, and the crossover time is taken as the benchmark of the next clock. This control scheme helps achieve high efficiency by scaling down the frequency to reduce switching and gate driver losses during light-load or no-load conditions.

When the output current increases from light load condition, V_{COMP} becomes larger, and the switching frequency increases. If the DC value of V_{COMP} exceeds V_{AAM}, the operation mode resumes discontinuous conduction mode (DCM) or CCM, which have a constant switching frequency.

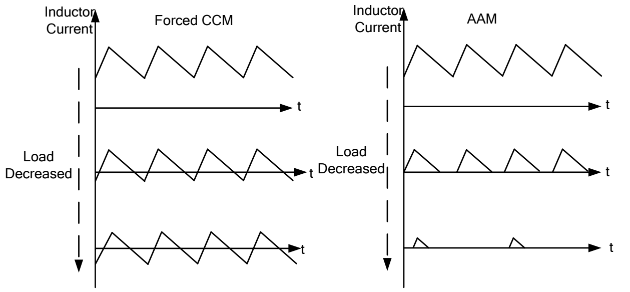


Figure 3: Forced CCM and AAM

Error Amplifier (EA)

The error amplifier compares V_{FB} with V_{REF} and outputs a current proportional to the difference between the two. This output current then charges or discharges the internal compensation network to form V_{COMP}, which controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

Internal Regulator and BIAS

Most of the internal circuitry is powered by the 5V internal regulator. This regulator takes VIN and operates in the full VIN range. When VIN exceeds 5V, the output of the regulator is in full regulation. When VIN falls below 5V, the output decreases following VIN. A decoupling ceramic capacitor is needed close to VCC.

For better thermal performance, connect BIAS to an external power supply between 5V to 18V. The BIAS supply overrides VIN to power the internal regulator. Using the BIAS supply allows VCC to be derived from a high-efficiency external source, such as V_{OUT}. Float BIAS or connect BIAS to ground if it is not being used.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 2.8V with a 150mV hysteresis.

Enable Control (EN)

EN is a digital control pin that turns the regulator on and off. When EN is pulled below its threshold voltage, the chip is put into the lowest shutdown current mode. Pulling EN above its threshold voltage turns on the part. Do not float EN.

Power Good Indicator (PG)

The MP4432 has a power good (PG) indication. PG is the open drain of a MOSFET and should be connected to VCC or another voltage source through a resistor (e.g.: 100kΩ). In the presence of an input voltage, the MOSFET turns on so that PG is pulled low before SS is ready. When the regulator output is within ±10% of its nominal output, the PG output is pulled high after a delay (typically 30µs). When the output voltage moves outside this range with a hysteresis, the PG output is pulled low with a 50µs delay to indicate a failure output status.

Programmable Frequency

The oscillating frequency of the MP4432 can be programmed either by an external frequency resistor (R_{FREQ}) or by a logic level synchronization clock.

The frequency resistor should be placed between FREQ and ground as close to the device as possible. The value of R_{FREQ} can be estimated with Equation (1):

$$R_{FREQ}(k\Omega) = \frac{170000}{f_s^{\,1.11}(kHz)} \qquad (1)$$

The calculated resistance may need fine tuning with a bench test. Do not float FREQ even if an external SYNC clock is added.

SYNC and PHASE

The internal oscillator frequency can also be synchronized to an external clock ranging from 350kHz to 2.5MHz through SYNC. The external clock should be at least 250kHz larger than the R_{FREQ} set frequency. Ensure that the high amplitude of the SYNC clock is higher than 1.8V and the low amplitude is lower than 0.4V. There is no pulse width requirement, but there is always a parasitic capacitance of the pad, so if the pulse width is too short, a clear rising and falling edge may not be seen due to the parasitic capacitance. A pulse longer than 100ns is recommended in application.

PHASE is used when two or more MP4432 devices are in parallel with the same SYNC clock. Pulling PHASE high forces the device to operate in-phase of the SYNC clock. Pulling PHASE low forces the device to be 180° out-of-phase of the SYNC clock. By setting different voltages of PHASE, two devices can operate in 180° out-of-phase to reduce the total input current ripple, so a smaller input bypass capacitor can be used (see Figure 4). The PHASE rising threshold is about 2.5V with a 400mV hysteresis.

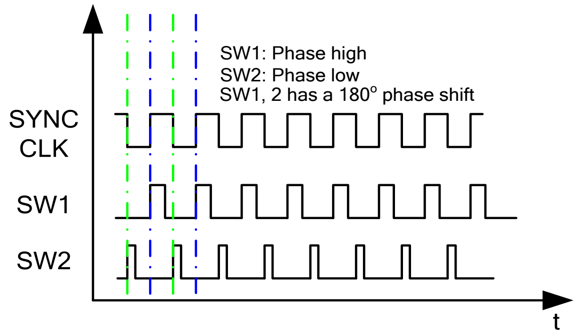


Figure 4: In-Phase and 180° Out-of-Phase

Soft Start (SS)

Soft start (SS) is implemented to prevent the converter output voltage from overshooting during start-up.

When the chip starts up, an internal current source begins charging the external soft-start capacitor. When the soft-start voltage (V_{SS}) is lower than the internal reference (V_{REF}), V_{SS} overrides V_{REF}, so the error amplifier uses V_{SS} as the reference. When V_{SS} is higher than V_{REF}, the error amplifier uses V_{REF} as the reference.

The soft-start time (t_{SS}) set by the external SS capacitor can be calculated with Equation (2):

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)} \tag{2}$$

Where C_{SS} is the external SS capacitor, V_{REF} = 0.8V, and I_{SS} is the internal 10μA SS charge current.

SS can be used for tracking and sequencing.

Pre-Bias Start-Up

At start-up, if V_{FB} is higher than V_{SS} (the output has a pre-bias voltage), neither the HS-FET or LS-FET turn on until V_{SS} is higher than V_{FB}.

Over-Current Protection (OCP) and Hiccup

The MP4432 has cycle-by-cycle peak current limit protection with valley-current detection and hiccup mode.

The power MOSFET current is sensed accurately via a current sense MOSFET. The current is then fed to the high-speed current comparator for current-mode control purposes. During the HS-FET on-state, if the sensed current exceeds the peak current limit value set by the COMP high-clamp voltage, the HS-FET turns off immediately. Then the LS-FET turns on to discharge the energy, and the inductor current decreases. The HS-FET remains off unless the inductor valley current is lower than a certain current threshold (the valley current limit), even though the internal clock pulses high.

If the inductor current does not drop below the valley current limit when the internal clock pulses high, the HS-FET misses the clock, and the switching frequency decreases to half the nominal value. Both the peak and valley current limits keep the inductor current from running away during an overload or short-circuit condition.

When the output is shorted to ground, causing the output voltage to drop below 55% of its nominal output, meanwhile the peak current limit is kicked, the device will consider this an output dead short and trigger hiccup mode immediately to periodically restart the part.

In hiccup mode, the MP4432 disables its output power stage and slowly discharges the soft-start capacitor. The MP4432 restarts with a full soft start when the soft-start capacitor is fully discharged. If the short-circuit condition still remains after the soft-start ends, the device repeats this operation until the fault is removed and the output returns to the regulation level. This protection mode reduces the average short circuit current greatly to alleviate thermal issues and protect the regulator.

Floating Driver and Bootstrap Charging

A 0.1μF to 1μF external bootstrap capacitor powers the floating power MOSFET driver. The floating driver has its own UVLO protection with a rising threshold of 2.5V and a hysteresis of 200mV.

The bootstrap capacitor voltage is charged to ~5V from VCC through a PMOS pass transistor when the LS-FET is on.

At high duty cycle operation or sleep-mode condition, the time period available to the bootstrap charging is less, so the bootstrap capacitor may not be charged sufficiently. In case the external circuit does not have sufficient voltage or time to charge the bootstrap capacitor, extra external circuitry can be used to ensure that the bootstrap voltage is in the normal operation region.

BST Refresh

To improve drop out, the MP4432 is designed to operate at close to 100% duty cycle for as long as the BST to SW voltage is greater than 2.5V. When the voltage from BST to SW drops below 2.5V, the HS-FET is turned off using a UVLO circuit, which forces the LS-FET on to refresh the charge on the BST capacitor.

Since the supply current sourced from the BST capacitor is low, the HS-FET can remain on for more switching cycles than are required to refresh the capacitor, thus making the effective duty cycle of the switching regulator high.

The effective duty cycle during dropout of the regulator is influenced mainly by the voltage drops across the HS-FET, LS-FET, inductor resistance, and printed circuit board resistance.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from running away thermally. When the silicon die temperature exceeds its upper threshold, the power MOSFETs shut down. When the temperature drops below its lower threshold, the chip is enabled again.

Start-Up and Shutdown

If both VIN and EN exceed their appropriate thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the rest of the circuitries.

While the internal supply rail is up, an internal timer holds the power MOSFET off for about 50µs to blank the start-up glitches. When the soft-start block is enabled, it first holds its SS output low to ensure that the rest of the circuitries are ready, and then slowly ramps up.

Three events can shut down the chip: VIN low, EN low, and thermal shutdown. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

APPLICATION INFORMATION

Setting the Output Voltage

An external resistor divider connected to FB sets the output voltage (see Figure 5).

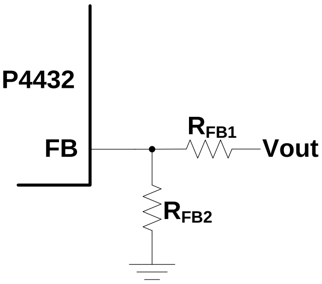


Figure 5: Feedback Network

Choose R_{FB1} to be around 40kΩ. R_{FB2} can then be calculated with Equation (3):

$$R_{FB2} = \frac{R_{FB1}}{\frac{V_{OUT}}{0.8V} - 1} \quad (3)$$

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)
3.3	41.2 (1%)	13 (1%)
5	68.1 (1%)	13 (1%)

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, use a 4.7µF to 10µF capacitor. It is strongly recommended to use another lower-value capacitor (e.g.: 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and GND as possible.

Since C_{IN} absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (4):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (4)$$

The worst-case condition occurs at VIN = $2V_{OUT}$, shown in Equation (5):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g.: 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated with Equation (6):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \cdot (1 - \frac{V_{OUT}}{V_{IN}}) \cdot (R_{ESR} + \frac{1}{8f_{SW} \times C_{OUT}}) \quad (7)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple.

For simplification, the output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}{}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (9)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP4432 can be optimized for a wide range of capacitance and ESR values.

Selecting the Inductor

A 1µH to 10µH inductor with a DC current rating at least 25% higher than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a low DC resistance. A larger value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductor value is to allow the inductor ripple current to be approximately 30% of the maximum load current. The inductance value can then be calculated with Equation (10):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_{L}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (11):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

VIN UVLO Setting

The MP4432 has an internal, fixed, under-voltage lockout (UVLO) threshold. The rising threshold is 2.8V, while the falling threshold is about 2.65V. For applications requiring a higher UVLO point, an external resistor divider between VIN and EN can be used to achieve a higher equivalent UVLO threshold (see Figure 6).

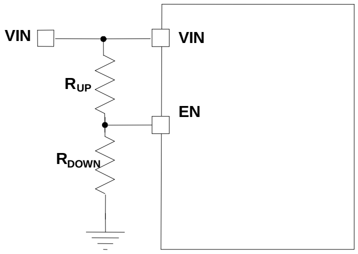


Figure 6: Adjustable UVLO Using EN Divider

The UVLO threshold can be calculated with Equation (12) and Equation (13):

$$INUV_{RISING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN\_RISING} \quad (12)$$

$$INUV_{FALLING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN\_FALLING} \quad (13)$$

Where V_{EN_RISING} = 1.05V, and $V_{EN\_FALLING}$ = 0.93V.

External BST Diode

An external BST diode can enhance the efficiency of the regulator when the duty cycle is high. A power supply between 2.5V and 5V can be used to power the external bootstrap diode. VCC or V_{OUT} is recommended for this power supply in the circuit (see Figure 7).

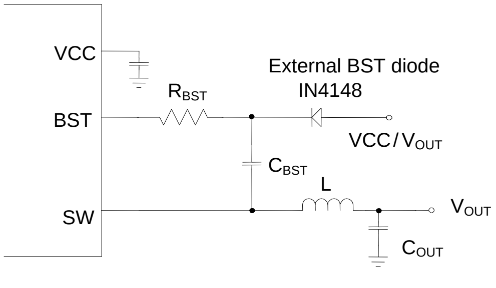


Figure 7: Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the recommended BST capacitor value is 0.1µF to 1µF.

A resistor in series with the BST capacitor (R_{BST}) can reduce the SW rising rate and voltage spikes. This helps enhance EMI performance and reduce voltage stress at a high VIN. A higher resistance is better for SW spike reduction but compromises efficiency. For a tradeoff between EMI and efficiency, a ≤20Ω R_{BST} is recommended.

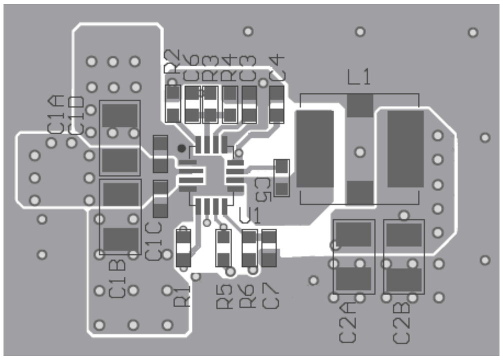
PCB Layout Guidelines (6)

Efficient PCB layout, especially of the input capacitor placement, is critical for stable operation. For best results, refer to Figure 8 and follow the guidelines below. A four-layer layout is strongly recommended to achieve better thermal performance.

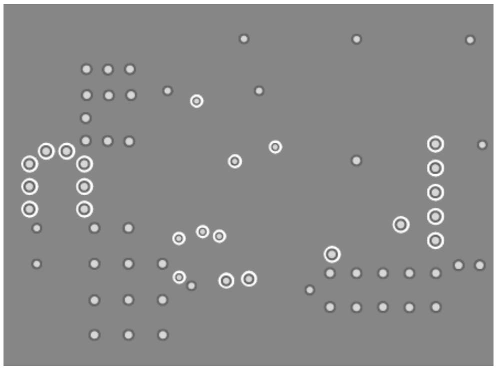
1. Place symmetric input capacitors as close to VIN and GND as possible.
2. Use a large ground plane to connect directly to PGND. If the bottom layer is a ground plane, add vias near PGND.
3. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
4. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to minimize high frequency noise.
5. Keep the connection of the input capacitor and IN as short and wide as possible.
6. Place the VCC capacitor as close to VCC and GND as possible.
7. Route SW and BST away from sensitive analog areas, such as FB.
8. Place the feedback resistors close to the chip to ensure that the trace connecting to FB is as short as possible.
9. Use multiple vias to connect the power planes to the internal layers.

NOTE:

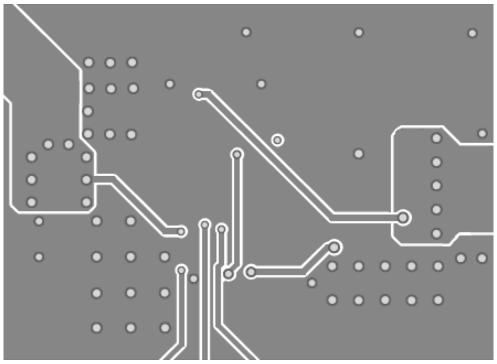
6) The recommended PCB layout is based on Figure 9.



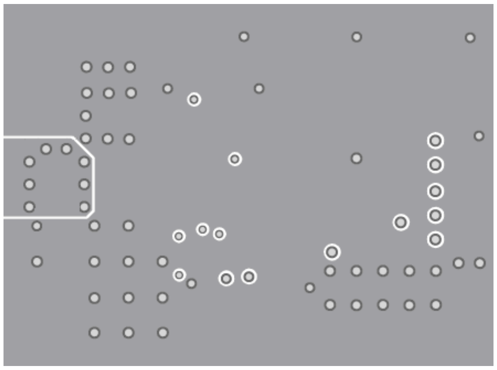
Top Layer



Inner Layer 1



Inner Layer 2



Bottom Layer

Figure 8: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

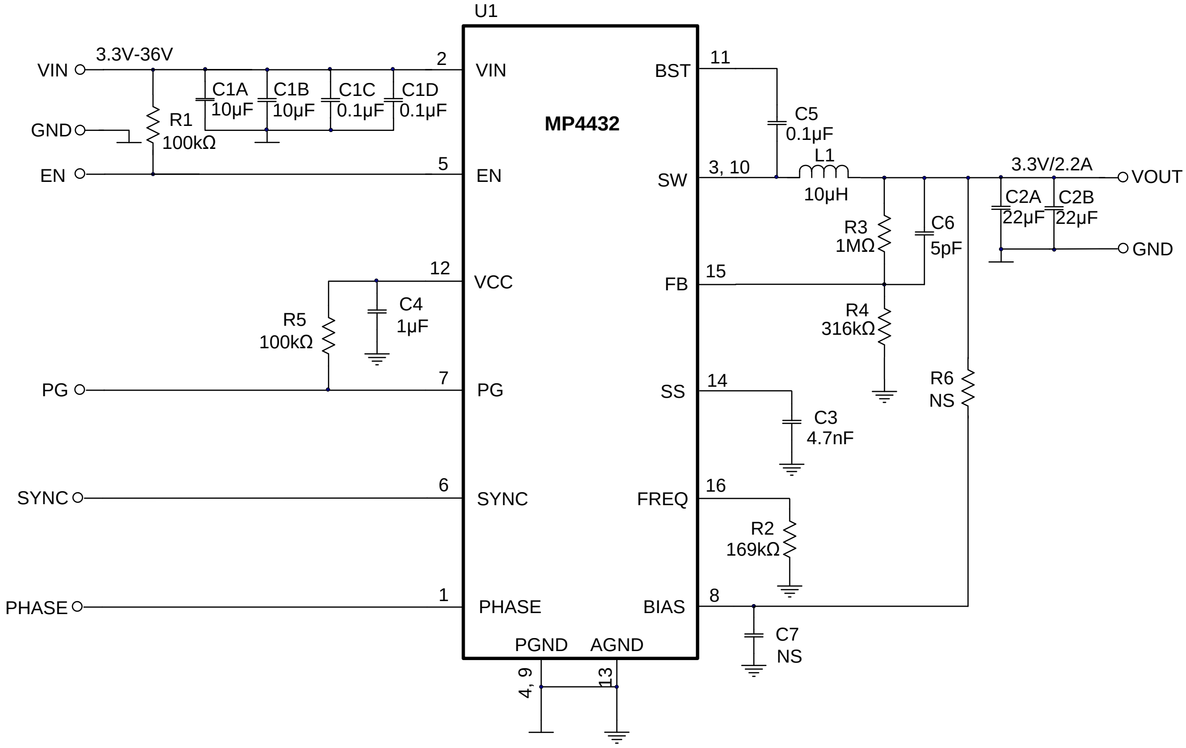


Figure 9: V_{OUT} = 3.3V, F_{SW} = 500kHz

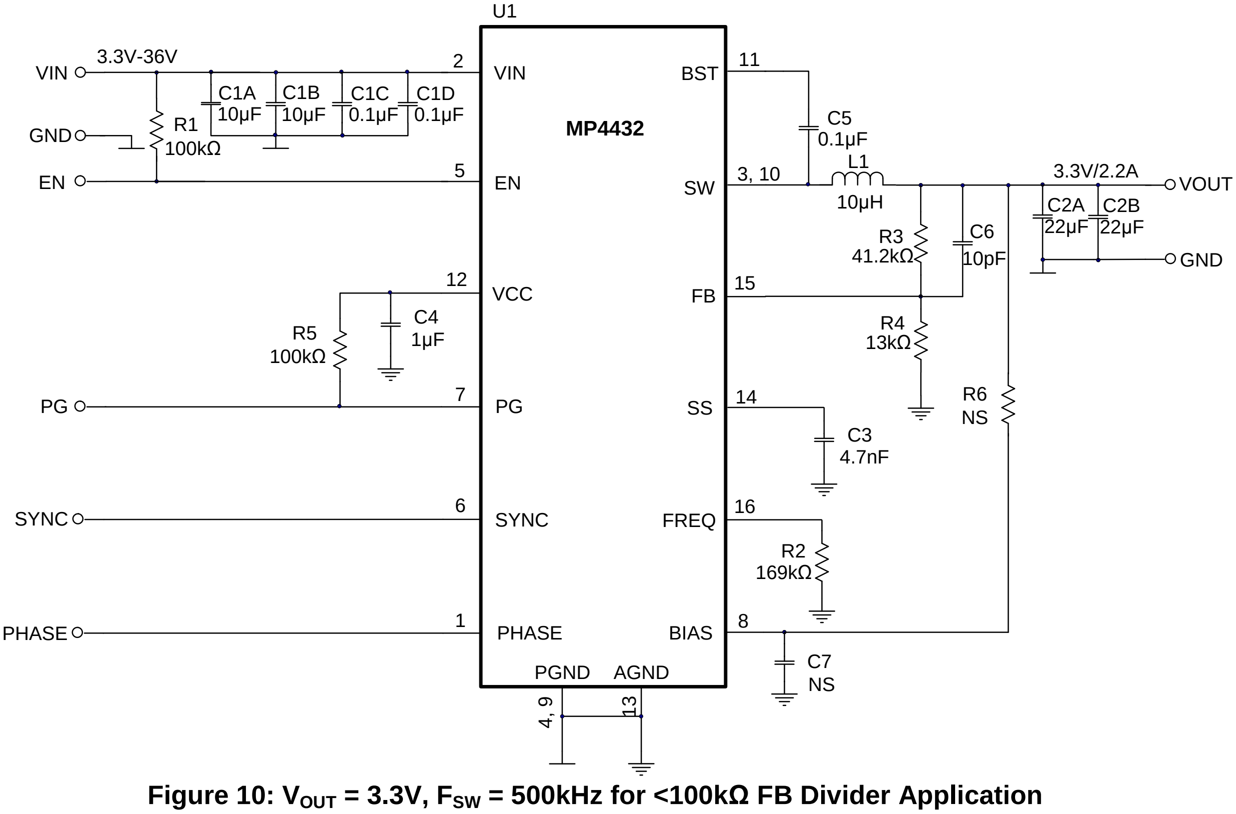


Figure 10: V_{OUT} = 3.3V, F_{SW} = 500kHz for <100kΩ FB Divider Application

TYPICAL APPLICATION CIRCUITS *(continued)*

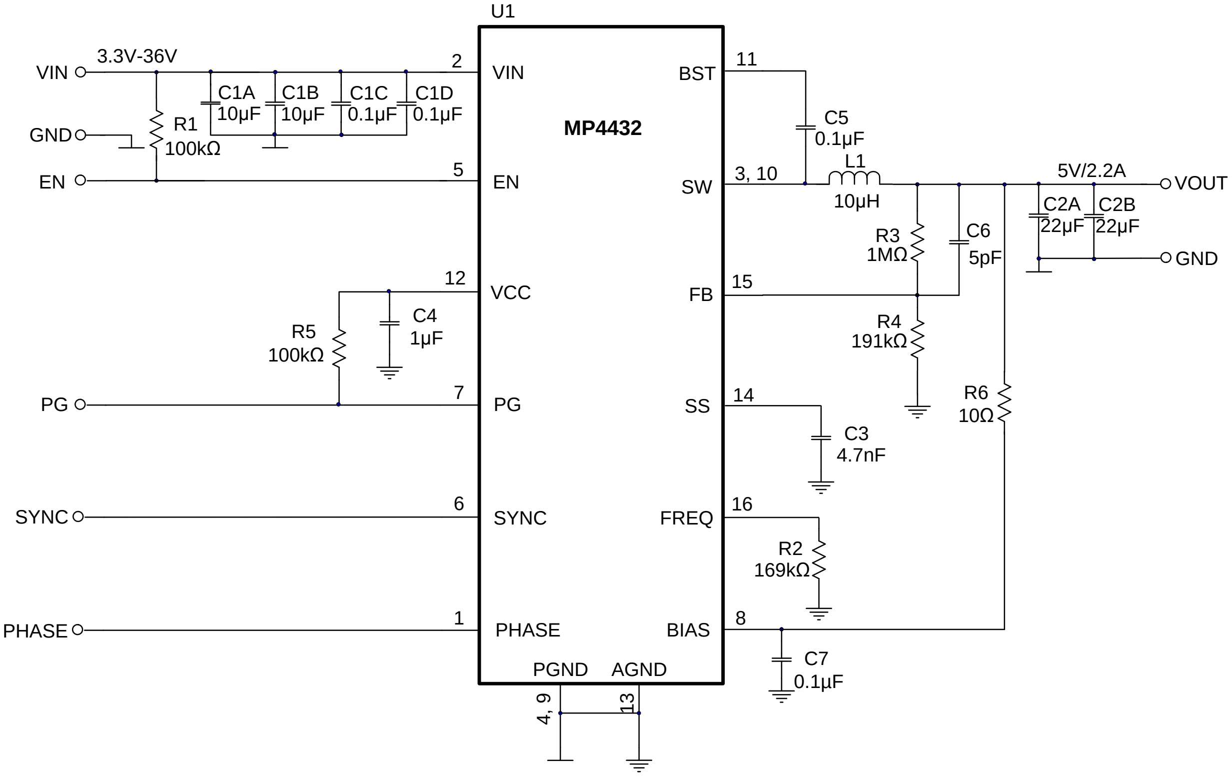


Figure 11: V_{OUT} = 5V, F_{SW} = 500kHz

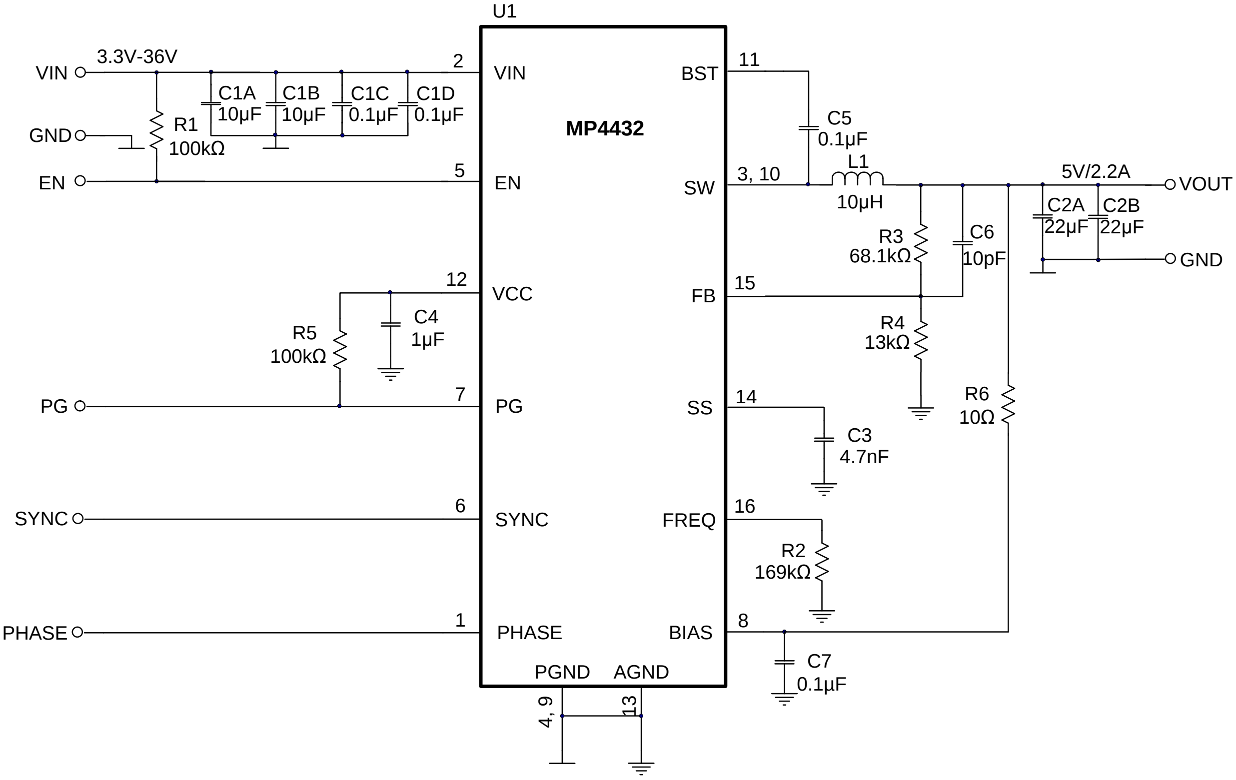


Figure 12: V_{OUT} = 5V, F_{SW} = 500kHz for <100kΩ FB Divider Application

TYPICAL APPLICATION CIRCUITS *(continued)*

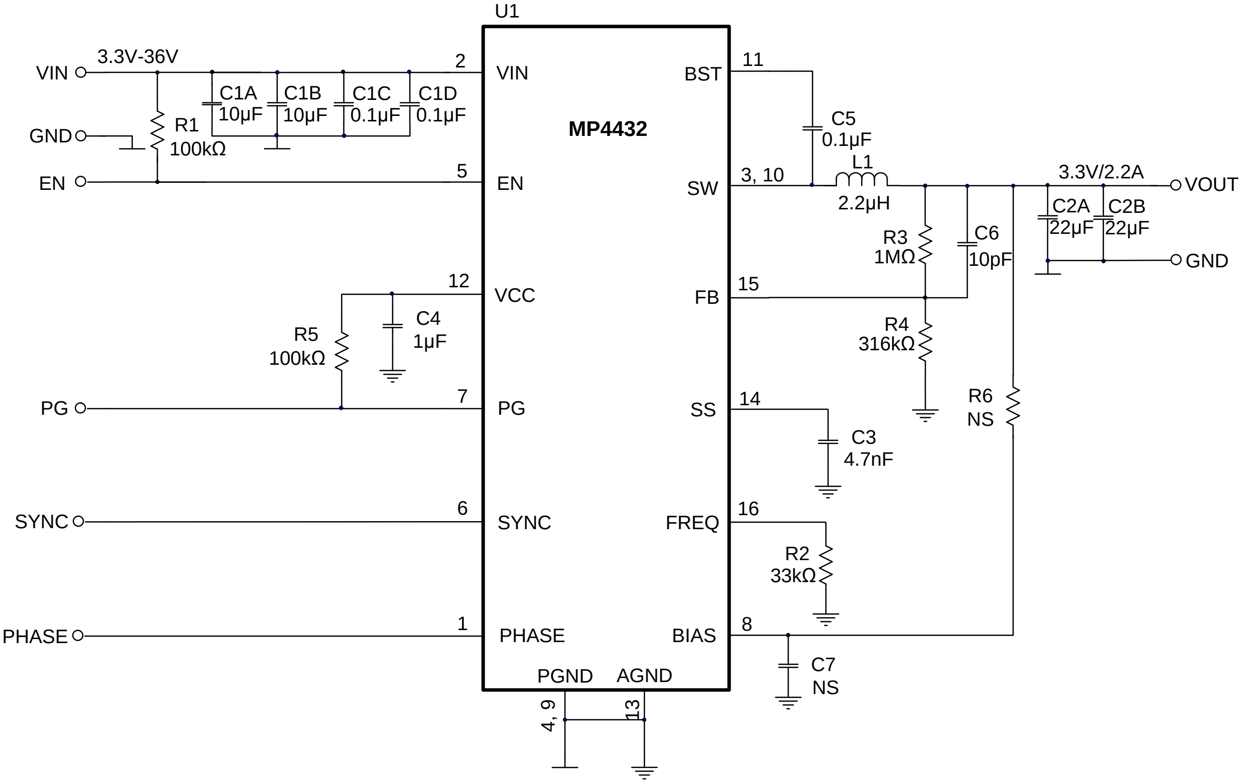


Figure 13: V_{OUT} = 3.3V, F_{SW} = 2.2MHz

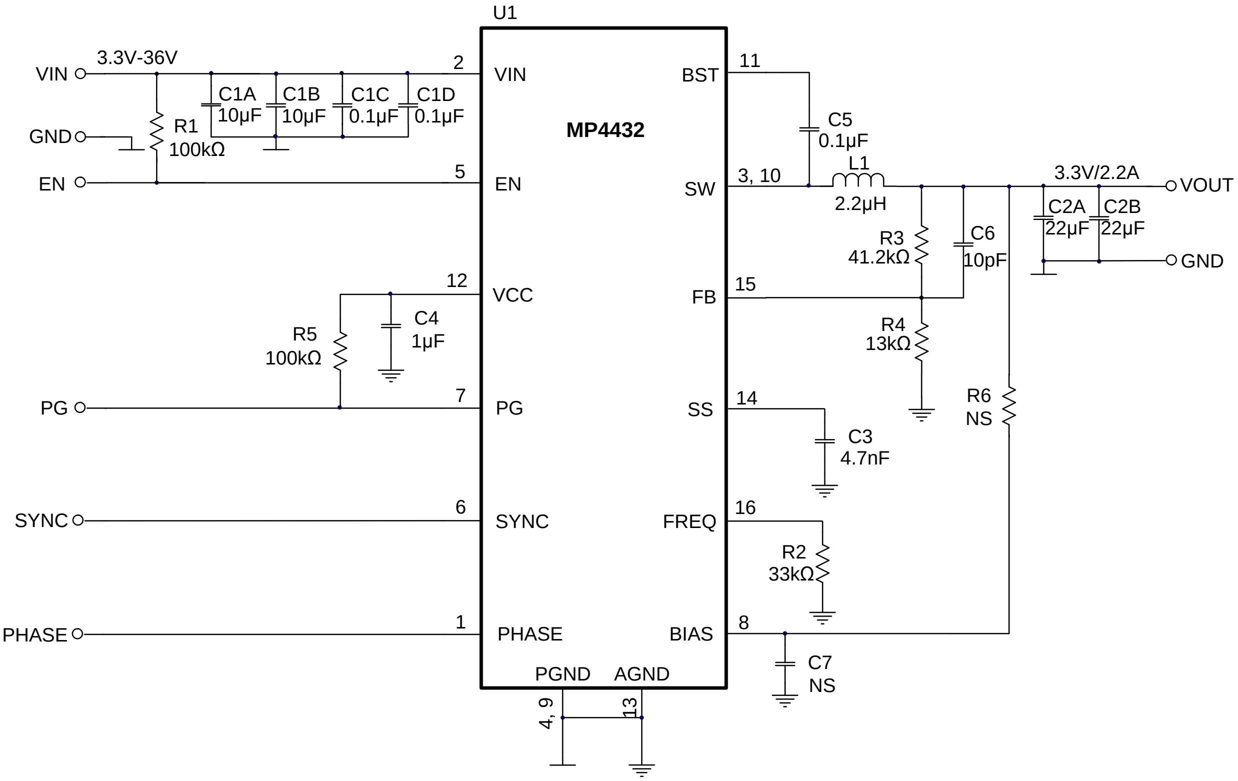


Figure 14: V_{OUT} = 3.3V, F_{SW} = 2.2MHz for <100kΩ FB Divider Application

TYPICAL APPLICATION CIRCUITS *(continued)*

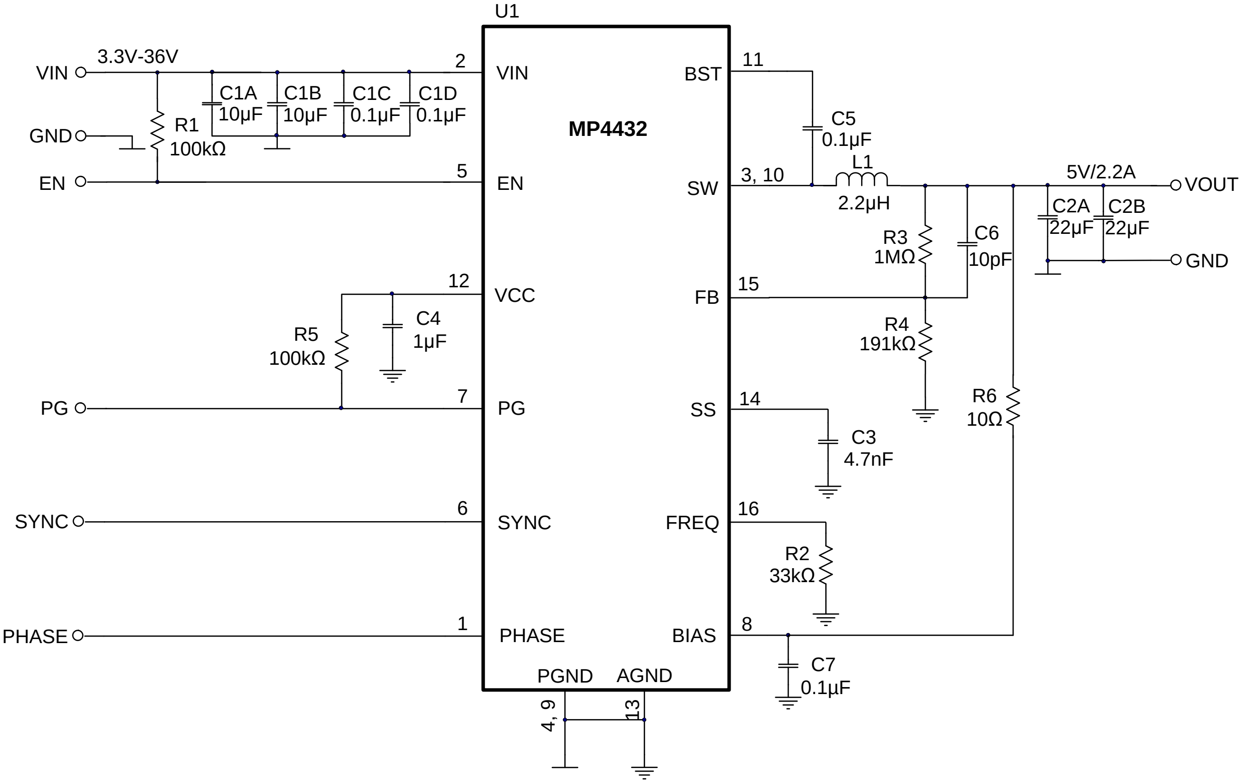


Figure 15: V_{OUT} = 5V, F_{SW} = 2.2MHz

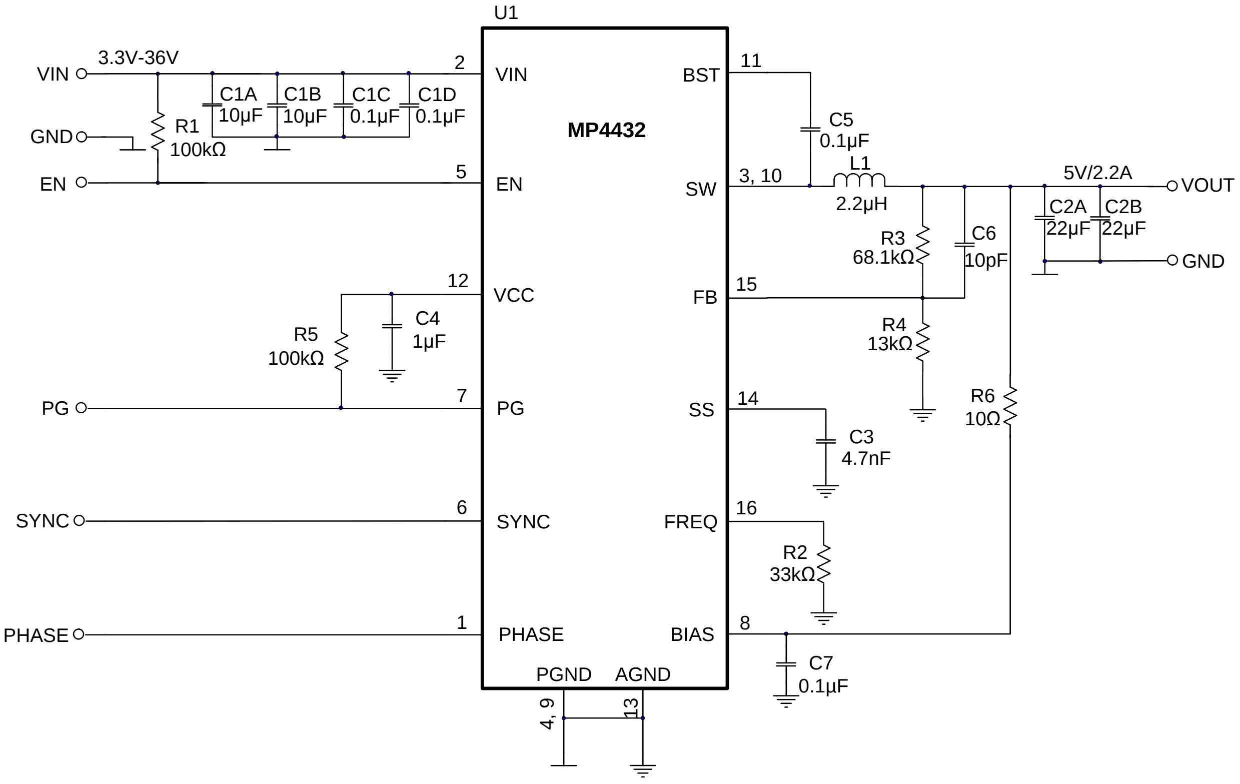


Figure 14: V_{OUT} = 5V, F_{SW} = 2.2MHz for <100kΩ FB Divider Application