# MP4816

## 16-Channel, High-Voltage Analog Switch

The Future of Analog IC Technology

## DESCRIPTION

The MP4816 is a 16-channel, high-voltage, single-pole, single-throw, SPST, analog switch designed for medical ultrasound imaging applications. The MP4816 is designed to multiplex transmit and receive voltages to and from multiple piezoelectric transducers (PZT).

The output switches are controlled by a 16-bit serial shift register followed by a 16-bit data latch. A data out pin ($D_{OUT}$) is provided to allow for multiple devices to be cascaded together. This helps minimize the number of input/output (I/O) control lines. A logic high in the data latch turns on the corresponding analog switch. A logic low turns off the corresponding analog switch.

The MP4816 does not require any high-voltage supplies. Only two low-voltage supplies are required (3.3V and 10V). The analog switch can block or pass analog voltages up to ±90V with peak currents of up to ±2.0A.

The MP4816 is available in a TQFP-48 (7mmx7mm) package.

## FEATURES

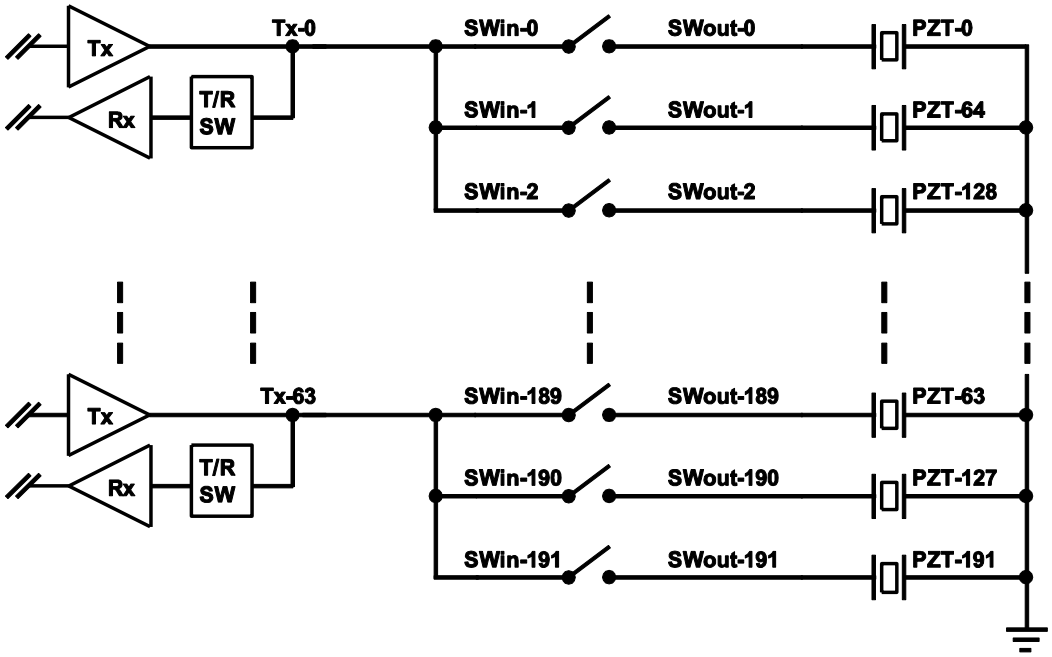
- No High-Voltage Supplies Required
- 16 Channels
- Up to ±90V Analog Signals
- 12.5Ω Typical Switch Resistance
- ±2.0A Typical Switch Peak Current
- Off-Isolation of -66dB at 5.0MHz
- 80MHz Clock Frequency
- Available in a TQFP-48 (7mmx7mm) Package

## APPLICATIONS

- Medical Ultrasound Imaging
- Non-Destructive Testing (NDT)



## TYPICAL APPLICATION



## ORDERING INFORMATION

| Part Number | Package | Top Marking |
|---|---|---|
| MP4816GFP | TQFP-48 (7mmx7mm) | *See Below* |

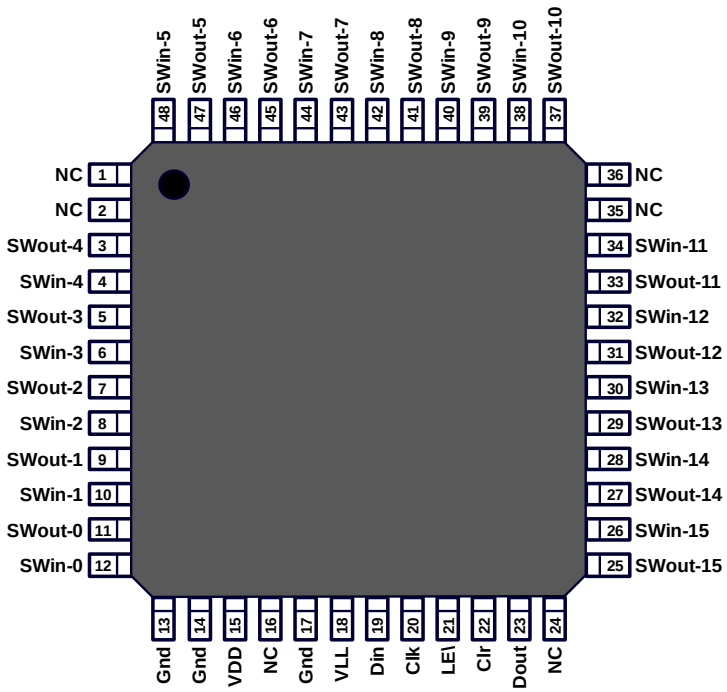
## TOP MARKING

MPSYYWW
MP4816
LLLLLLLLL

MPS: MPS prefix
YY: year code
WW: week code
MP4816: part number
LLLLLLLLL: lot number

## PACKAGE REFERENCE

**TOP VIEW**




**TQFP-48 (7mmx7mm)**

## ABSOLUTE MAXIMUM RATINGS (1)

Logic supply ($V_{LL}$).....-0.5V to +6.6V
Translator supply ($V_{DD}$) .....-0.5V to +11V
Analog signal range (pulsed voltage) ($V_{SIG}$).....
.....0V to ±105V
Junction temperature .....150°C
Lead temperature .....260°C
Continuous power dissipation ($T_A$ = 25°C) (2)
..... 1.47W
HBM; SWoutx: Class 1B, SWinx: Class 1C: Other pins: Class 2 (JEDEC Standard) CDM: All pins: Class C3 (JEDEC Standard)
Storage temperature..... -55°C to 150°C

## *Recommended Operating Conditions* (3)

Logic supply voltage ($V_{LL}$).....2.7V to 5.5V
Translator supply voltage ($V_{DD}$) ..... 9V to 10V
Analog signal range ($V_{SIG}$) ..... 0 to ±90V
Junction temperature ($T_J$) .....-25°C to +125°C

| ***Thermal Resistance*** (4) | $\theta_{JA}$ | $\theta_{JC}$ |
|---|---|---|
| TQFP-48 (7mmx7mm) | 68 | 15 | °C/W |

**NOTES:**

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX)-$T_A$)/$\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, resulting in permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

## DC ELECTRICAL CHARACTERISTICS

**$V_{DD}$ = 10V, $V_{LL}$ = 5.0V, unless otherwise noted. (5)**

| Parameter | Sym | Conditions | $T_J$ = 0°C | | $T_J$ = 25°C | | | $T_J$ = 70°C | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| Analog signal range | $V_{SIG}$ | Applied to SWin pin | 0 | ±90 | 0 | | ±90 | 0 | ±90 | V |
| On resistance | $R_{ON}$ | $I_{SIG}$ = ±5.0mA, SWout = 0V. See test circuit 1. | | 16 | | 12.5 | 19 | | 24 | Ω |
| | | $I_{SIG}$ = ±200mA, SWout = 0V. See test circuit 1. | | 16 | | 12.5 | 19 | | 24 | |
| Small signal on resistance matching | $\Delta R_{ON}$ | $I_{SIG}$ = ±5.0mA, SWout = 0V | | | | 5.0 | | | | % |
| Large signal on resistance (6) | $R_{ONL}$ | $I_{SIG}$ = ±1.0A, $t_{PW}$ ≤ 500ns, duty cycle ≤ 1.0%, SWout = 0V. See test circuit 2. | | | | 13 | | | | Ω |
| Switch output peak current (6) | $I_{SWPK}$ | $t_{PW}$ < 100ns, duty cycle < 0.1% | | | | ±2.0 | | | | A |
| Switch off DC offset | $V_{DC-OFF}$ | 36kΩ to ground. See test circuit 3. | | ±75 | | | ±75 | | ±75 | mV |
| Switch on DC offset | $V_{DC-ON}$ | 36kΩ to ground. See test circuit 3. | | ±75 | | | ±75 | | ±75 | mV |
| $V_{LL}$ quiescent current | $I_{LLQ}$ | All logic inputs are static | | 50 | | | 50 | | 50 | µA |
| $V_{DD}$ quiescent current | $I_{DDQ}$ | All switches on or off, SWin = SWout = ground | | 60 | | | 60 | | 60 | µA |
| $V_{LL}$ average dynamic current | $I_{LL}$ | $f_{CLK}$ = 40MHz, $D_{IN}$ = 20MHz, LE\ = H, Clr = H | | | | 2.2 | 6 | | | mA |
| | | $f_{CLK}$ = 80MHz, $D_{IN}$ = 40MHz, LE\ = H, Clr = H (6) | | | | 4.3 | | | | |
| $V_{DD}$ average dynamic current | $I_{DD}$ | All output switches are turning on and off at 50kHz. $D_{IN}$ = H, Clr = 50kHz. | | | | 2.3 | 4 | | | mA |
| Input voltage logic low | $V_{IL}$ | | 0 | 0.2$V_{LL}$ | 0 | | 0.2$V_{LL}$ | 0 | 0.2$V_{LL}$ | V |
| Input voltage logic high | $V_{IH}$ | | 0.8$V_{LL}$ | $V_{LL}$ | 0.8$V_{LL}$ | | $V_{LL}$ | 0.8$V_{LL}$ | $V_{LL}$ | V |
| Input current logic low | $I_{IL}$ | | -1.0 | | -1.0 | | | -1.0 | | µA |
| Input current logic high | $I_{IH}$ | | | 1.0 | | | 1.0 | | 1.0 | µA |
| Data out logic low voltage | $V_{OL}$ | Isink = 10mA | | 1.0 | | | 1.0 | | 1.0 | V |
| Data out logic high voltage | $V_{OH}$ | Isource = 10mA | $V_{LL}$-1.0 | | $V_{LL}$-1.0 | | | $V_{LL}$-1.0 | | V |
| Logic input capacitance | $C_{IN}$ | | | 10 | | | 10 | | 10 | pF |

**NOTES:**

5) Production test is at 25°C only. 0°C and 70°C limits are guaranteed by design and characterization.

6) Parameters are not tested in mass production, only guaranteed by design or bench characterization.

## AC ELECTRICAL CHARACTERISTICS

**$V_{DD}$ = 10V, $V_{LL}$ = 5.0V, unless otherwise noted. (5)**

| Parameter | Sym | Conditions | | $T_J$ = 0°C | | $T_J$ = 25°C | | | $T_J$ = 70°C | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Typ | Max | Min | Max | |
| Clock frequency (6) | $f_{CLK}$ | 50% duty cycle | $V_{LL}$ = 3.3V | 0 | 40 | 0 | | 40 | 0 | 40 | MHz |
| | | | $V_{LL}$ = 5.0V | 0 | 80 | 0 | | 80 | 0 | 80 | |
| Clock rise time (6) | $t_r$ | | | | 50 | | | 50 | | 50 | ns |
| Clock fall time (6) | $t_f$ | | | | 50 | | | 50 | | 50 | ns |
| Set-up time from data to rising edge of clock (6) | $t_{SU}$ | | | 3.0 | | 3.0 | | | 3.0 | | ns |
| Hold time from rising edge of clock to data (6) | $t_H$ | | | 3.0 | | 3.0 | | | 3.0 | | ns |
| Set-up time before LE\ rises (6) | $t_{SD}$ | | | 6.0 | | 6.0 | | | 6.0 | | ns |
| LE\ pulse width (6) | $t_{WLE\ bar}$ | | | 6.0 | | 6.0 | | | 6.0 | | ns |
| Clear pulse width (6) | $t_{WCLR}$ | | | 6.0 | | 6.0 | | | 6.0 | | ns |
| Data propagation delay time from rising edge of clock (6) | $t_{DOLH}$, $t_{DOHL}$ | 20pF on $D_{OUT}$ to ground | | 4.0 | 8.0 | 4.0 | 6.0 | 8.0 | 4.0 | 8.0 | ns |
| Output switch turn on time | $T_{ON}$ | SWin = 2.0V, SWout = 50Ω to ground. See test circuit 4. | | | 2.0 | | | 2.0 | | 2.0 | µs |
| Output switch turn off time | $T_{OFF}$ | | | | 2.0 | | | 2.0 | | 2.0 | µs |
| Analog signal slew rate (6) | dv/dt | | | | 20 | | | 20 | | 20 | V/ns |
| Off isolation (6) | $K_O$ | freq = 5.0MHz, Rload = 50Ω. See test circuit 5. | | | | | -66 | | | | dB |
| Switch crosstalk (6) | $K_{CR}$ | freq = 5.0MHz, Rload = 50Ω. See test circuit 6. | | | | | -60 | | | | dB |
| Switch off capacitance (6) | $C_{SWin-OFF}$ | | | | | | 10 | | | | pF |
| Switch on capacitance (6) | $C_{SW-ON}$ | | | | | | 13 | | | | pF |
| Positive output voltage spike (6) | $+V_{SPK}$ | SWin = 1kΩ to ground, SWout = 50Ω to ground. See test circuit 7. | | | | | 16 | | | | mV |
| Negative output voltage spike(6) | $-V_{SPK}$ | | | | | | -14 | | | | mV |
| Output charge injection (6) | $Q_{INJ}$ | Cload = 1000pF. See test circuit 8. | | | | | 18 | | | | pC |

**NOTES:**

5) Production test is at 25°C only. 0°C and 70°C limits are guaranteed by design and characterization.
6) Parameters are not tested in mass production, only guaranteed by design or bench characterization.

## PIN FUNCTIONS

| Package Pin # | Name | Description |
|---|---|---|
| 1, 2, 16, 24, 35, 36 | NC | **No internal connections.** |
| 3 | SWout-4 | **Analog switch output 4.** Connect SWout-4 to the piezoelectric transducer. |
| 4 | SWin-4 | **Analog switch input 4.** Connect SWin-4 to the high-voltage pulser/transmitter. |
| 5 | SWout-3 | **Analog switch output 3.** Connect SWout-3 to the piezoelectric transducer. |
| 6 | SWin-3 | **Analog switch input 3.** Connect SWin-3 to the high-voltage pulser/transmitter. |
| 7 | SWout-2 | **Analog switch output 2.** Connect SWout-2 to the piezoelectric transducer. |
| 8 | SWin-2 | **Analog switch input 2.** Connect SWin-2 to the high-voltage pulser/transmitter. |
| 9 | SWout-1 | **Analog switch output 1.** Connect SWout-1 to the piezoelectric transducer. |
| 10 | SWin-1 | **Analog switch input 1.** Connect SWin-1 to the high-voltage pulser/transmitter. |
| 11 | SWout-0 | **Analog switch output 0.** Connect SWout-0 to the piezoelectric transducer. |
| 12 | SWin-0 | **Analog switch input 0.** Connect SWin-0 to the high-voltage pulser/transmitter. |
| 13, 14, 17 | Gnd | **Device ground.** |
| 15 | $V_{DD}$ | **Translators supply voltage.** $V_{DD}$ has a 9 - 10V operating range. |
| 18 | $V_{LL}$ | **Logic supply voltage.** $V_{LL}$ has a 2.7 - 5.5V operating range. |
| 19 | $D_{IN}$ | **Logic input.** $D_{IN}$ is the data input for the 16-bit serial shift register. |
| 20 | Clk | **Logic input.** Clk is the clock input for the 16-bit serial shift register. Data is loaded into Clk during the rising edge of the clock. |
| 21 | LE\ | **Logic input.** LE\ is the latch enable bar for the 16-bit latch. Logic low on LE\ transfers data from the shift registers to the latches. Logic high on LE\ holds the data in the latches. Refer to the logic truth table on page 8. |
| 22 | Clr | **Logic input.** Clr is the clear input for the 16-bit latch. Logic high on Clr clears the data in the latches by setting them all to 0. Data in the shift register remains unchanged. Refer to the logic truth table on page 8. |
| 23 | $D_{OUT}$ | **Logic output.** $D_{OUT}$ is the data output for the 16-bit serial shift register. |
| 25 | SWout-15 | **Analog switch output 15.** Connect SWout-15 to the piezoelectric transducer. |
| 26 | SWin-15 | **Analog switch input 15.** Connect SWin-15 to the high-voltage pulser/transmitter. |
| 27 | SWout-14 | **Analog switch output 14.** Connect SWout-14 to the piezoelectric transducer. |
| 28 | SWin-14 | **Analog switch input 14.** Connect SWin-14 to the high-voltage pulser/transmitter. |
| 29 | SWout-13 | **Analog switch output 13.** Connect SWout-13 to the piezoelectric transducer. |
| 30 | SWin-13 | **Analog switch input 13.** Connect SWin-13 to the high-voltage pulser/transmitter. |

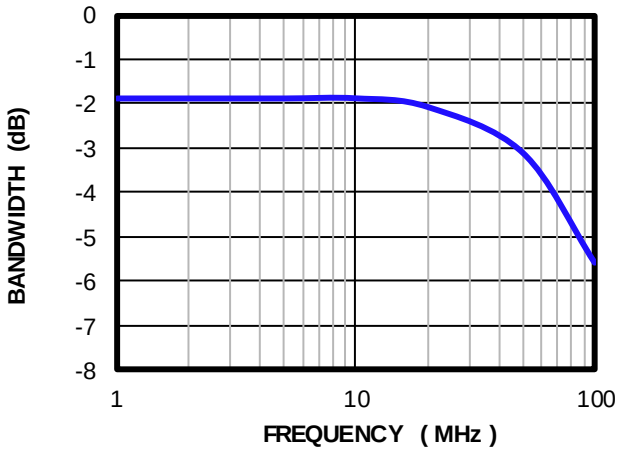
## PIN FUNCTIONS *(continued)*

| Package Pin # | Name | Description |
|---|---|---|
| 31 | SWout-12 | **Analog switch output 12.** Connect SWout-12 to the piezoelectric transducer. |
| 32 | SWin-12 | **Analog switch input 12.** Connect SWin-12 to the high-voltage pulser/transmitter. |
| 33 | SWout-11 | **Analog switch output 11.** Connect SWout-11 to the piezoelectric transducer. |
| 34 | SWin-11 | **Analog switch input 11.** Connect SWin-11 to the high-voltage pulser/transmitter. |
| 37 | SWout-10 | **Analog switch output 10.** Connect SWout-10 to the piezoelectric transducer. |
| 38 | SWin-10 | **Analog switch input 10.** Connect SWin-10 to the high-voltage pulser/transmitter. |
| 39 | SWout-9 | **Analog switch output 9.** Connect SWout-9 to the piezoelectric transducer. |
| 40 | SWin-9 | **Analog switch input 9.** Connect SWin-9 to the high-voltage pulser/transmitter. |
| 41 | SWout-8 | **Analog switch output 8.** Connect SWout-8 to the piezoelectric transducer. |
| 42 | SWin-8 | **Analog switch input 8.** Connect SWin-8 to the high-voltage pulser/transmitter. |
| 43 | SWout-7 | **Analog switch output 7.** Connect SWout-7 to the piezoelectric transducer. |
| 44 | SWin-7 | **Analog switch input 7.** Connect SWin-7 to the high-voltage pulser/transmitter. |
| 45 | SWout-6 | **Analog switch output 6.** Connect SWout-6 to the piezoelectric transducer. |
| 46 | SWin-6 | **Analog switch input 6.** Connect SWin-6 to the high-voltage pulser/transmitter. |
| 47 | SWout-5 | **Analog switch output 5.** Connect SWout-5 to the piezoelectric transducer. |
| 48 | SWin-5 | **Analog switch input 5.** Connect SWin-5 to the high-voltage pulser/transmitter. |

## TYPICAL PERFORMANCE CHARACTERISTICS

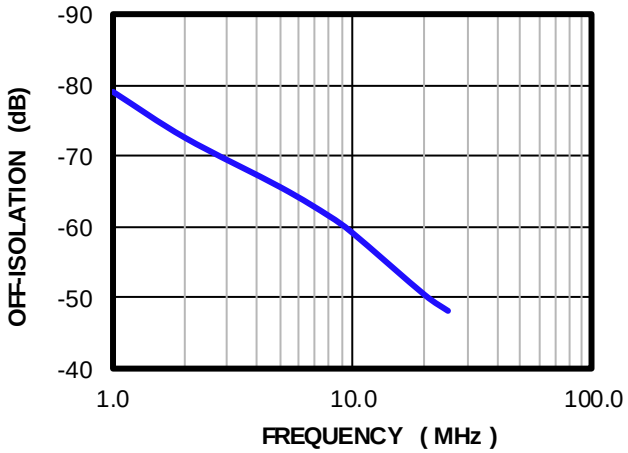
### Bandwidth vs. Frequency

$R_{LOAD}$ = 50Ω



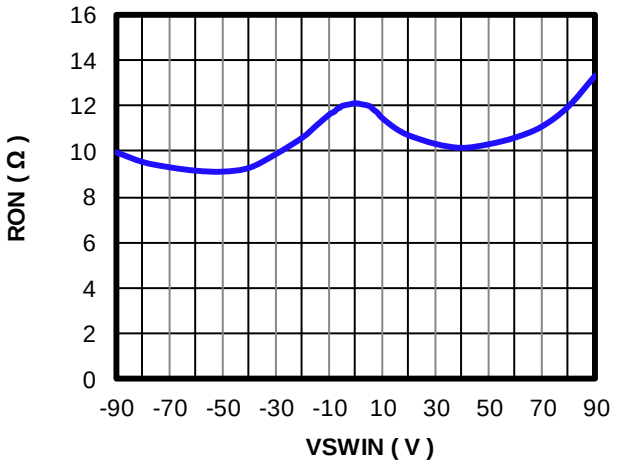

### Off-Isolation vs. Frequency

$R_{LOAD}$ = 50Ω



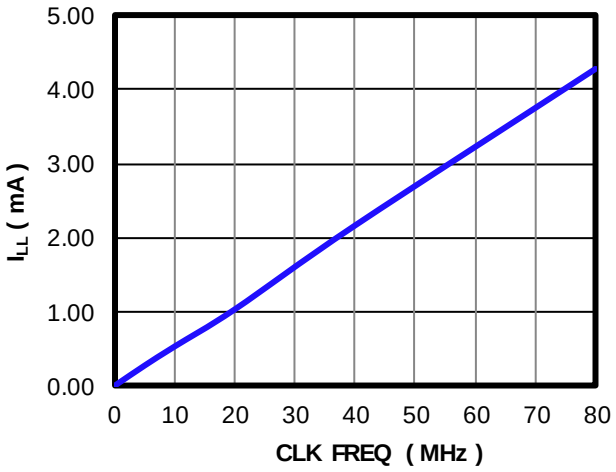

### Switch Resistance vs. Switch Input Voltage

$R_{LOAD}$ = 50Ω



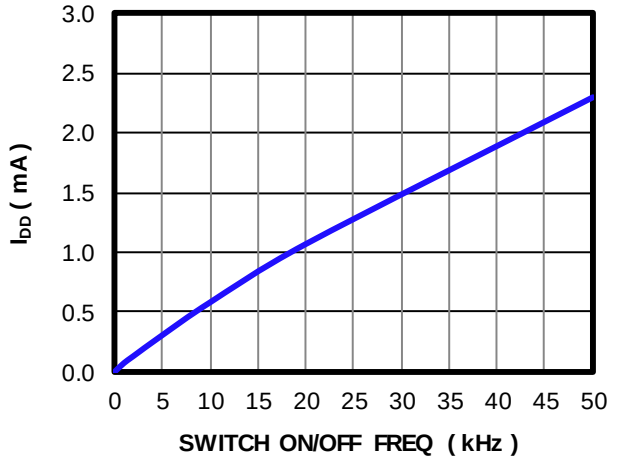

### $I_{LL}$ vs. Clock Frequency

$V_{LL}$ = 5.0V, $V_{DD}$ = 10V



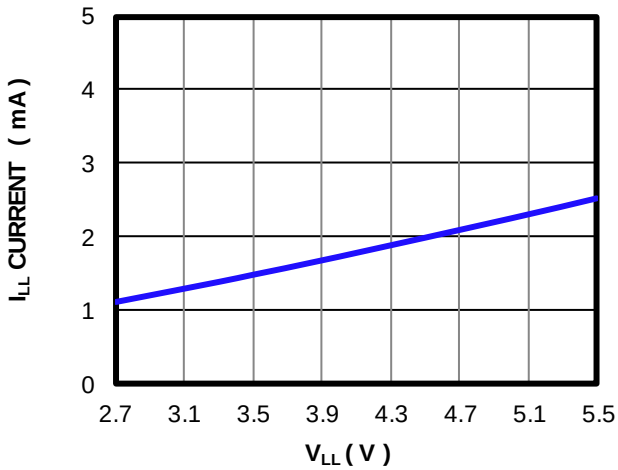

### $I_{DD}$ Vs. Switch On/Off Frequency

$V_{LL}$ = 5.0V, $V_{DD}$ = 10V, all 16 channels switching

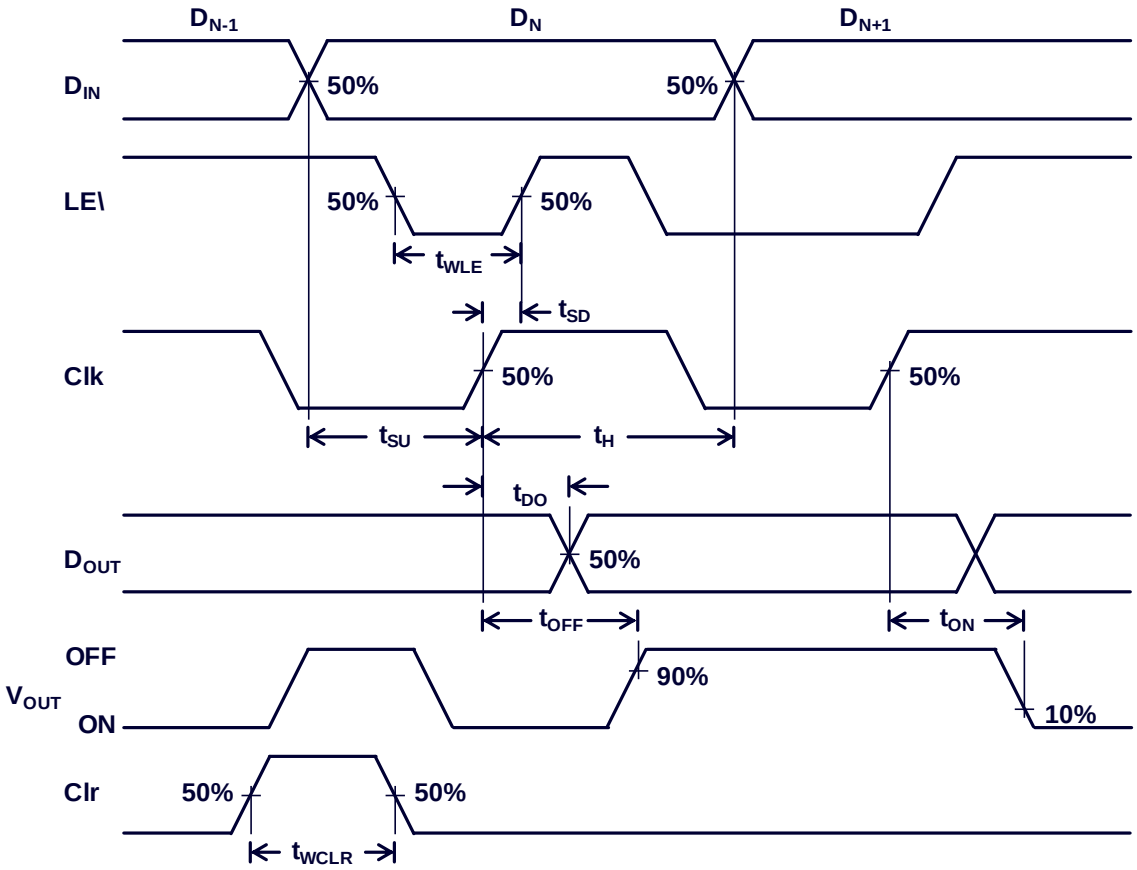



### $I_{LL}$ Current vs. $V_{LL}$ Voltage

Clk = 40MHz, $D_{IN}$ = 20MHz



## TIMING DIAGRAM



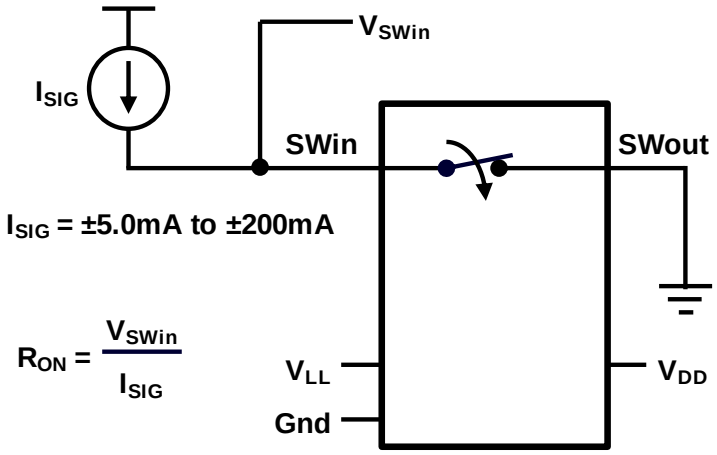

## LOGIC TRUTH TABLE

| Logic Input | | | | | | | Switch State | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| D0 | D1 | D2 | _ _ _ | D15 | LE bar | Clr | SW0 | SW1 | SW2 | _ _ _ | SW15 |
| L | - | - | | - | L | L | Off | - | - | | - |
| H | - | - | | - | L | L | On | - | - | | - |
| - | L | - | | - | L | L | - | Off | - | | - |
| - | H | - | | - | L | L | - | On | - | | - |
| - | - | L | | - | L | L | - | - | Off | | - |
| - | - | H | | - | L | L | - | - | On | | - |
| ⋮ | ⋮ | ⋮ | | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | | ⋮ |
| - | - | - | | L | L | L | - | - | - | | Off |
| - | - | - | | H | L | L | - | - | - | | On |
| x | x | x | | x | H | L | Holds previous state | | | | |
| x | x | x | | x | x | H | All switches off | | | | |

L = logic level low
H = logic level high
x = value does not matter

## TEST CIRCUITS

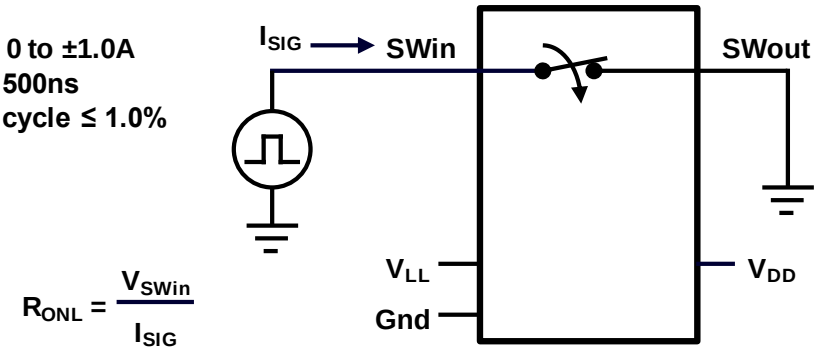
### Test Circuit 1




**Ron**

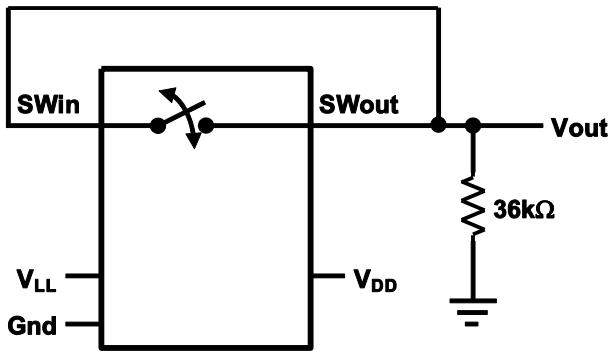
### Test Circuit 2

$I_{SIG}$ = 0 to ±1.0A
$t_{PW}$ ≤ 500ns
Duty cycle ≤ 1.0%




**Large Signal Ron**

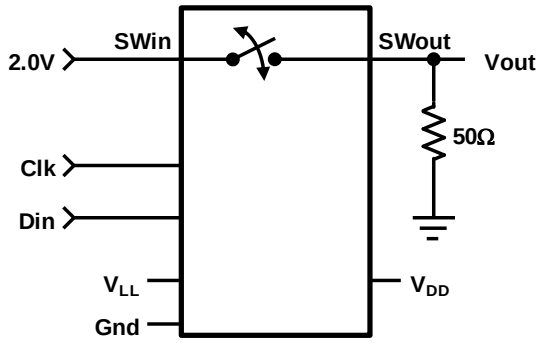
### Test Circuit 3

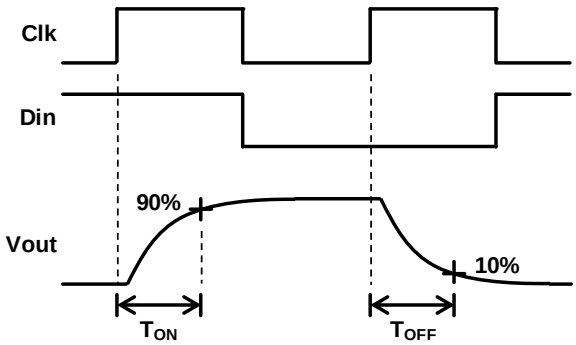



**Switch On/Off DC Offset**

## TEST CIRCUITS *(continued)*

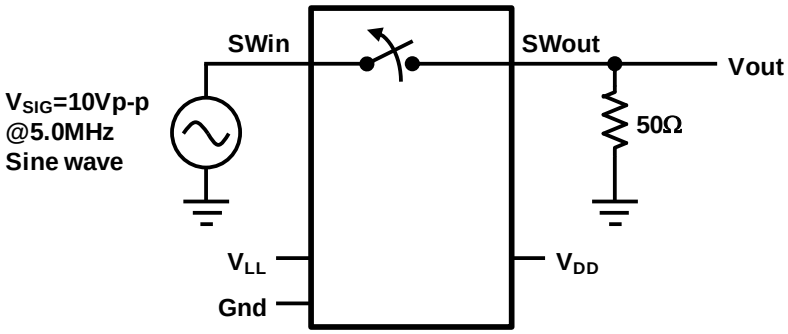
### Test Circuit 4




$T_{ON}$ / $T_{OFF}$

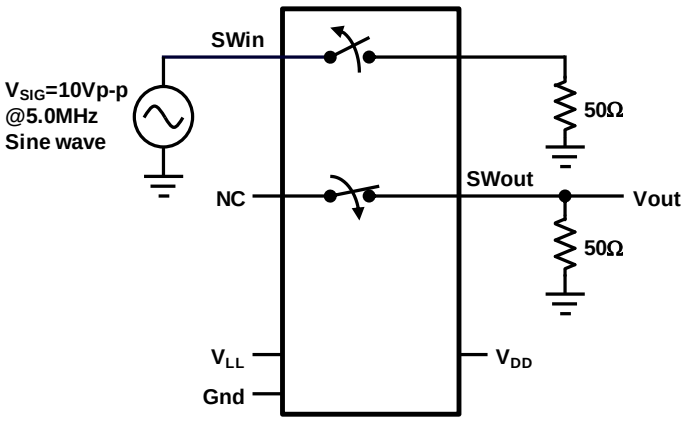
### Test Circuit 5




$$K_O = 20Log \left| \frac{Vout}{V_{SIG}} \right|$$

**Switch Off-Isolation**

### Test Circuit 6

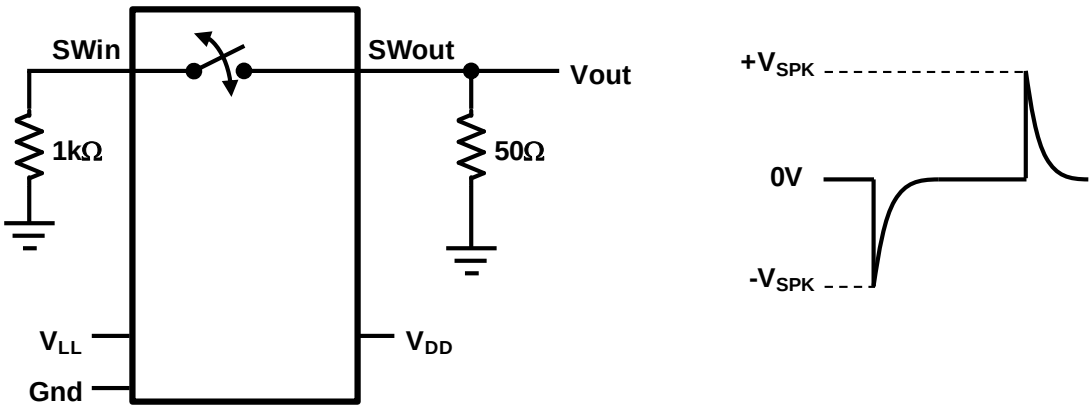



$$K_{CR} = 20Log \left| \frac{Vout}{V_{SIG}} \right|$$

**Switch Crosstalk**

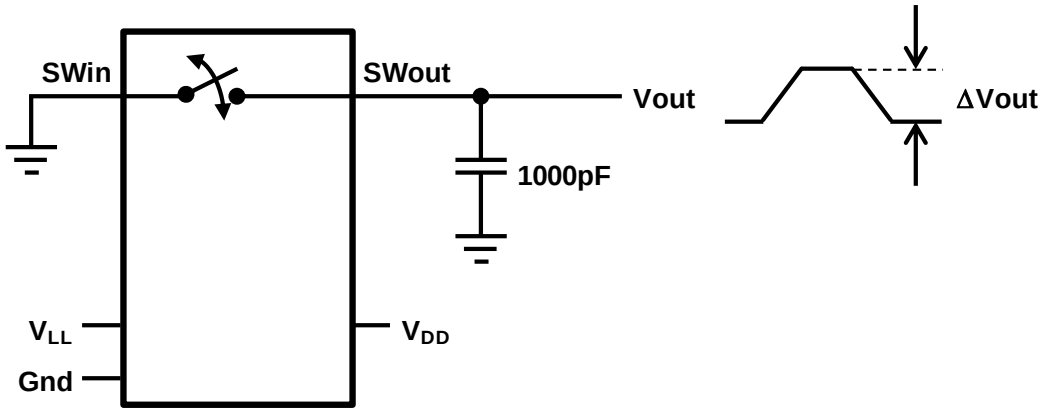
## TEST CIRCUITS *(continued)*

**Test Circuit 7**




### Output Voltage Spike

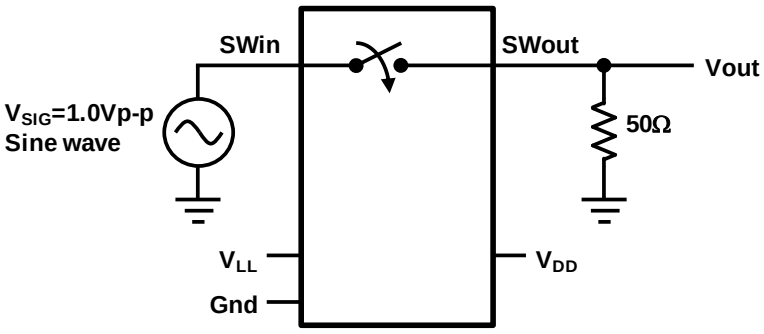
**Test Circuit 8**




$Q_{INJ}$ = 1000pF x ΔVout

### Charge Injection

**Test Circuit 9**




### Small Signal Bandwidth

## BLOCK DIAGRAM

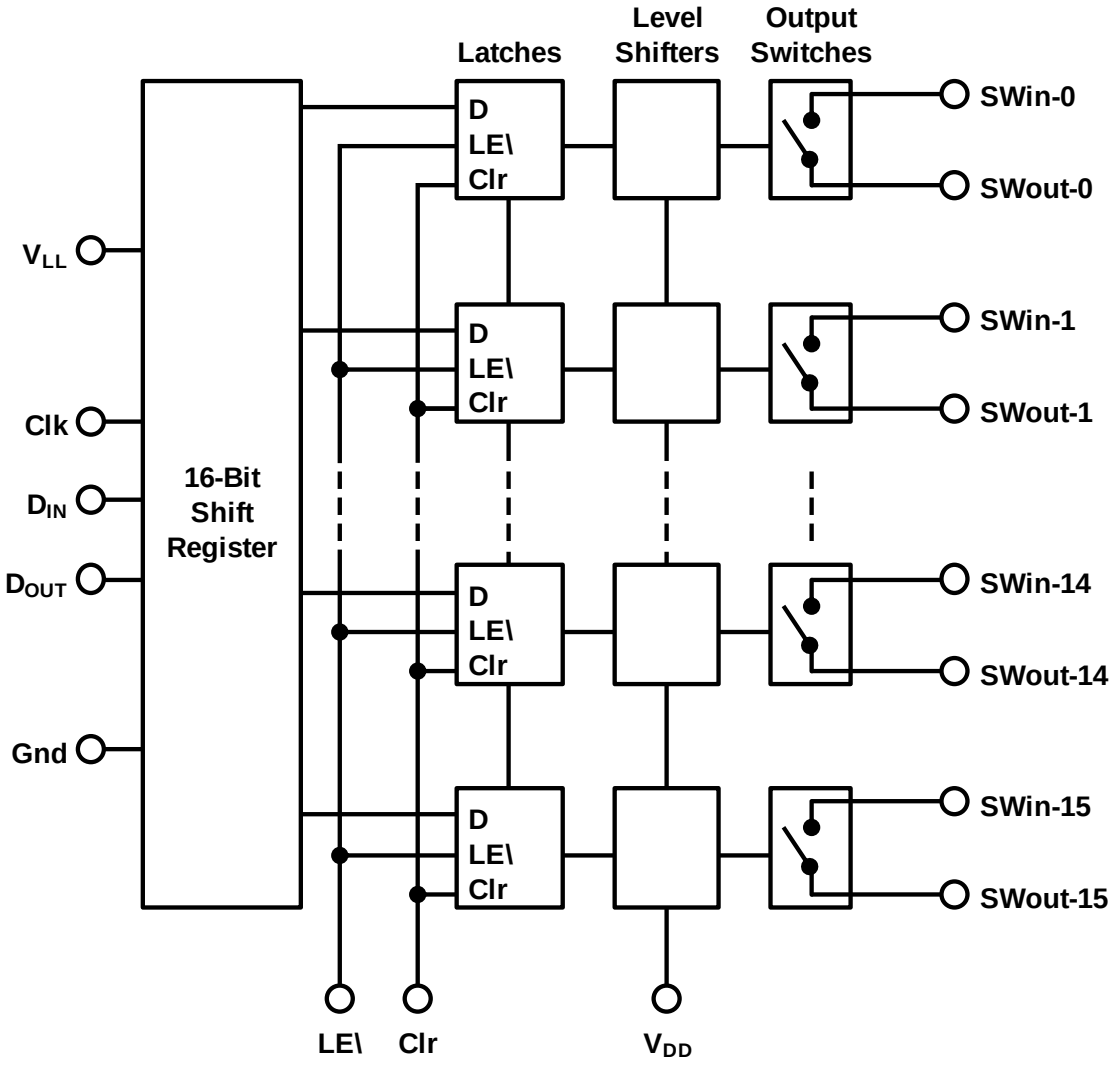



**Figure 1: Functional Block Diagram**

## APPLICATION INFORMATION

The MP4816 is a 16-channel, high-voltage, single-pole, single-throw, SPST, analog switch designed for medical ultrasound imaging and non-destructive testing (NDT) applications. The MP4816 is designed to multiplex high transmit voltages to selected piezoelectric transducers and multiplex small analog echo signals to selected receivers.

The output switches are controlled by a 16-bit serial shift register followed by a 16-bit data latch. A data out pin ($D_{OUT}$) allows for multiple devices to be cascaded together. This helps minimize the number of input/output (I/O) control lines. A logic high in the data latch turns on the corresponding analog switch. A logic low turns off the corresponding analog switch.

The MP4816 has a unique, patented design that does not require any high-voltage negative or positive supplies. This eliminates:

- the need to generate high-voltage positive and negative supplies.
- the need for high-voltage bypass capacitors next to each device.
- safety concerns on high-voltage buses.
- power-up/-down fault conditions concerns.

### Analog Switch

The analog switches have a typical switch resistance of 12.5Ω. In the on state, the device can pass transmit voltages up to ±90V with peak currents of up to ±2.0A. In the off state, the device can block voltages up to ±90V.

Each switch has a dedicated input and output pin (SWin and Swout). The transmit voltages must be connected to the SWin pins. The PZT load must be connected to the SWout pins. The SWin and SWout pins are not interchangeable.

Typical high-voltage transmission waves are short bursts of high-voltage pulses. The burst consists of single or multiple cycles of 1 - 15MHz pulses starting and ending at 0V (see Figure 2).

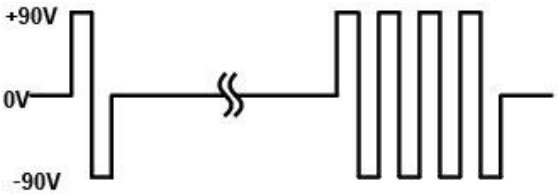



**Figure 2: Typical Tx High-Voltage Burst**

The SWin input must be close to ground before sending the high-voltage pulses. This allows the internal circuitry to drive the output switches properly.

Transmit voltages greater than ±5V must have frequencies higher than 500kHz. When receiving the echo signals where the voltages are less than ±0.5V, there is no restriction. The switch can pass low-voltage DC signals.

### Logic Interface

The MP4816 is controlled by a 16-bit serial shift register followed by a 16-bit latch. Data is loaded into the shift register during the rising edge of the clock. No data is transferred during the falling edge. Data is shifted into register 0 and is shifted out from register 15.

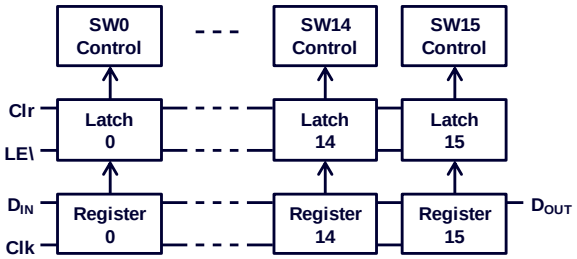



**Figure 3: Logic Interface Details**

Figure 3 shows the logic interface details. In the first clock cycle, the first data bit enters into shift register 0. After 15 more clocked cycles, the first bit is in register 15.

When the latch enable bar (LE\) is low, the data in the shift registers are transferred into the 16-bit latch. When LE\ is high, the data in the latches are held. With LE\ high, new data can be shifted into the 16-bit serial shift register without affecting the data in the 16-bit latch. The output switch state follows the data in the 16-bit latch. The Clr pin clears the data in the 16-bit latch only. Clr will not affect the data in the 16-bit serial shift register.

## APPLICATION DIAGRAM

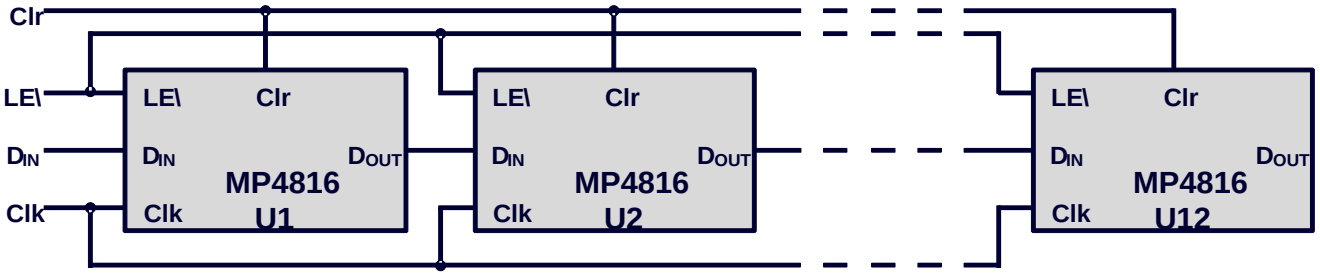



**Figure 4: Daisy-Chaining 12 MP4816 Devices with a Single Data Input Line**

The maximum clock frequency for the MP4816 is 80MHz. The front-end logic control is designed to minimize the number of I/O control lines. A system requiring 192 channels needs 192 ÷ 16 = 12 devices. Figure 4 shows 12 MP4816 devices in a single daisy-chain configuration. With an 80MHz clock, all 192 channels can be updated in 2.4µs. Only four control lines are required: clock, data in, latch enable bar, and clear. For systems requiring a faster update, multiple data in lines can be used (see Figure 5).

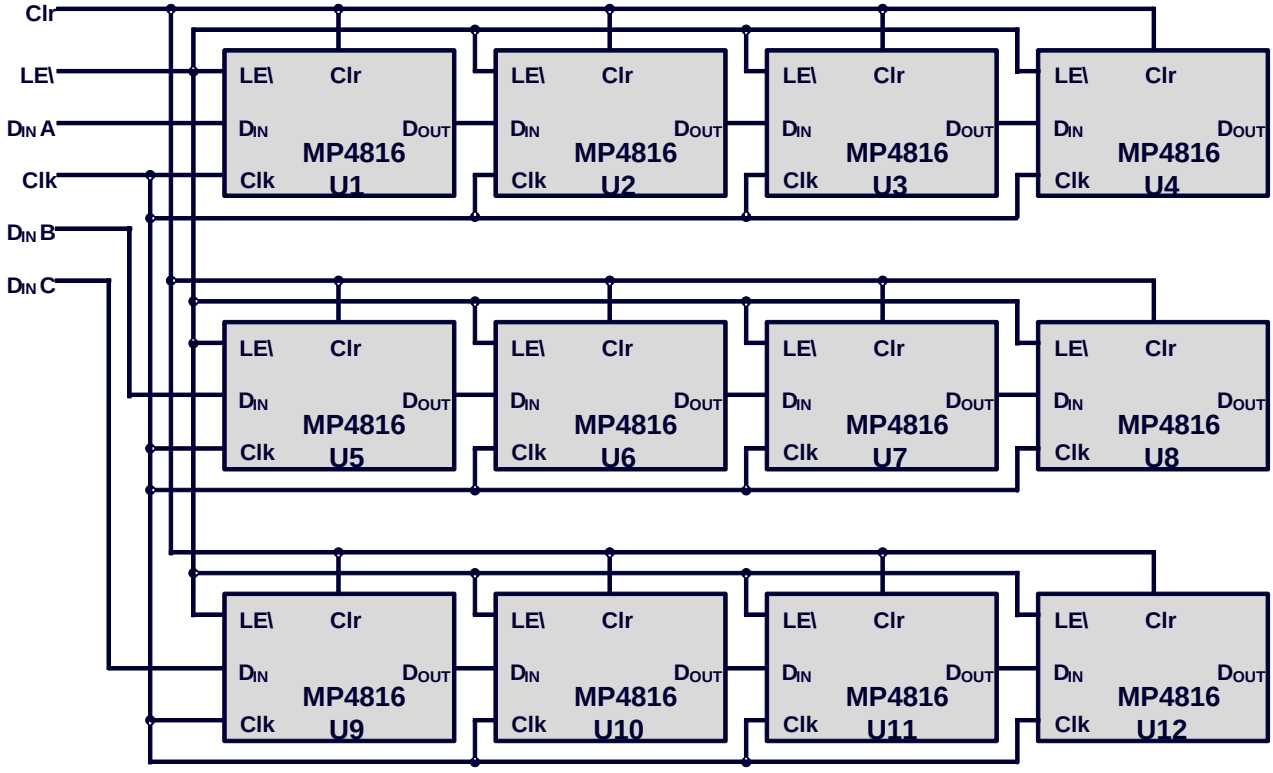



**Figure 5: Daisy-Chaining MP4816 Devices with Multiple Data Input Lines**

Figure 5 is a 192-channel system incorporating three data input lines ($D_{INA}$, $D_{INB}$, $D_{INC}$). Each data input line addresses four MP4816 devices daisy-chained together. There are now six control lines. With an 80MHz clock, all 192 channels can be updated in 800ns.

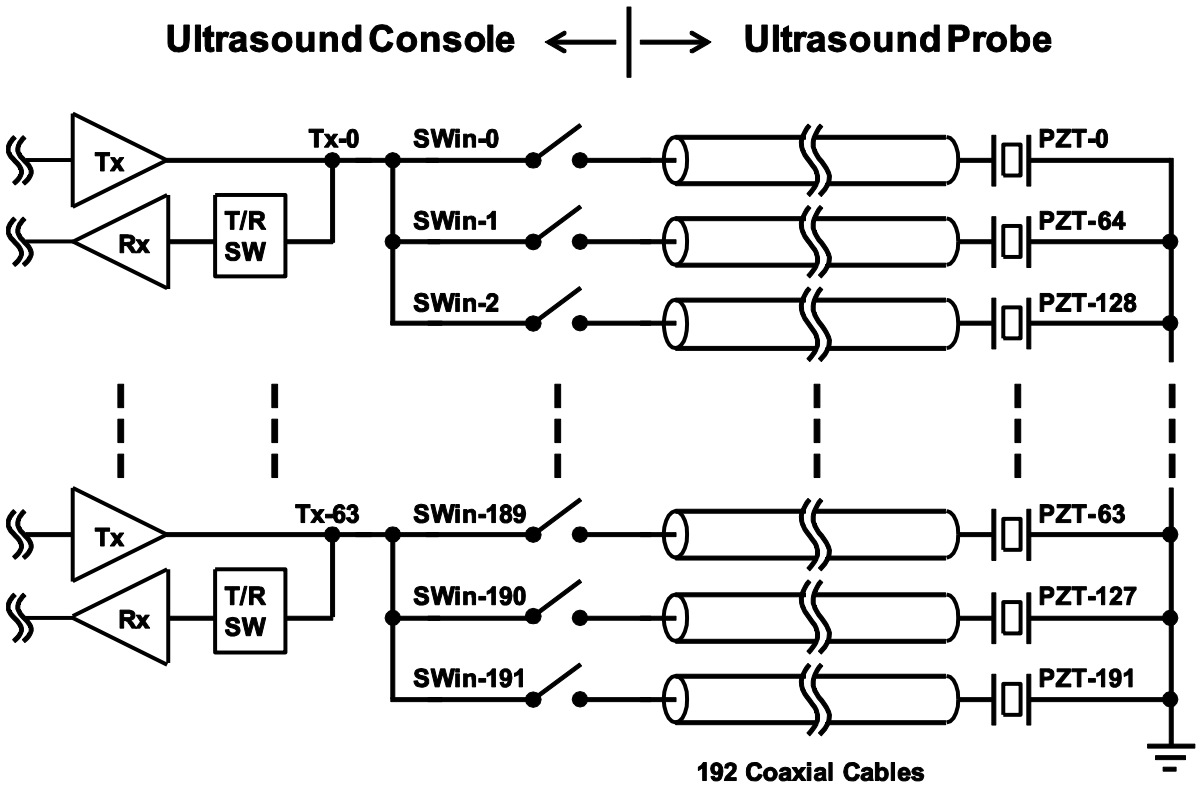



**Figure 6: MP4816 in the Console**

Figure 6 shows where the MP4816 analog switches reside in an ultrasound system. A 1:3 multiplexing configuration is shown as an example. Multiplexing configurations can range from 1:2 to 1:8 or higher. The 1:8 or higher ratios can have slower image frame rates and/or lower-quality images, which are generally used in the lower-end, lower-cost ultrasound market. The MP4816 can be used in any ratio.

The main advantage of using the MP4816 is that it reduces the number of transmitter and receiver circuitries. As shown in Figure 6, without any analog switches, the ultrasound console requires 192 transmitters and receivers to drive an ultrasound probe with 192 PZT elements. With analog switches, only 64 transmitters and receivers are needed. This reduction saves board space, power, and cost, since the transmitter and receiver circuitry can be quite complex. These benefits are especially important for portable ultrasound systems where space, battery life, and weight are all premiums.

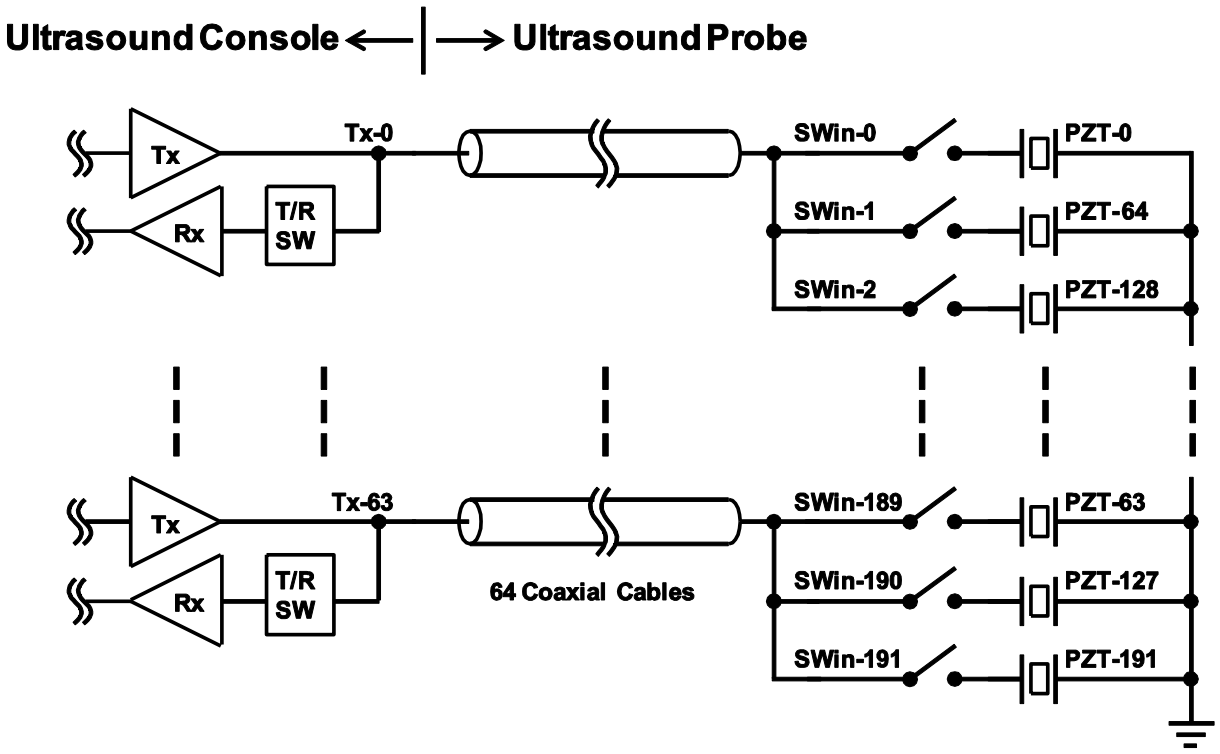


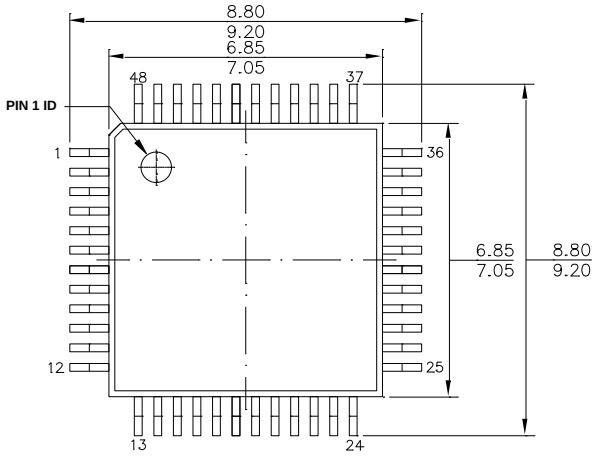

**Figure 7: MP4816 inside the Ultrasound Probe Head**

Figure 7 shows the advantages of putting analog switches inside the probe head, which may be referred to as an active probe. Generally, the probe head is severely space-limited and thermally limited. The housing is waterproof since it must be submersed in alcohol for sterilization. By employing analog switches inside the probe head, the number of coaxial cables can be reduced. Instead of 192 coaxial cables, only 64 coaxial cables are needed for the PZT plus 10 or fewer additional coaxial cables for the supply lines and logic interface.

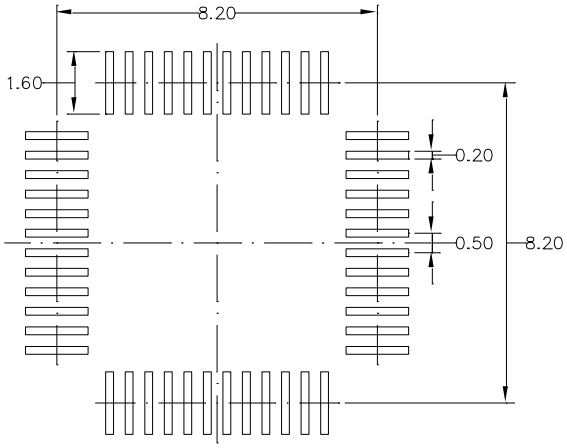
The reduction of coaxial cables required significantly reduces cost for the probe head. The coaxial cable is by far the most expensive item. Aside from the material cost, the labor to connect the coaxial cables is also quite costly. An added user benefit is that the probe head becomes more maneuverable. The sonographer experiences less fatigue using an active probe. Since the MP4816 does not need any high-voltage supplies, safety concerns about running high-voltage DC lines on the coaxial cables are eliminated, and the minimal power dissipation design eliminates the concern of thermal constraints inside the probe head, and the higher clock speed helps reduce the number of data lines.

# PACKAGE INFORMATION

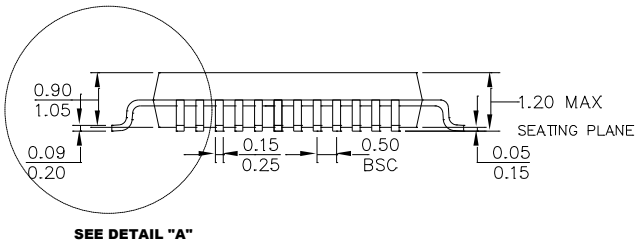
## TQFP-48 (7mmx7mm)



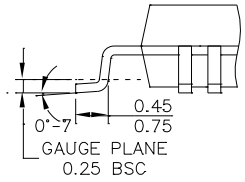

**TOP VIEW**




**RECOMMENDED LAND PATTERN**




**SIDE VIEW**




**DETAIL "A"**

**NOTE:**

**1) ALL DIMENSIONS ARE IN MILLIMETERS.**
**2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.**
**3) PACKAGE WITDH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.**
**4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.**
**5) JEDEC REFERENCE IS MO-143.**
**6) DRAWING IS NOT TO SCALE.**