The Future of Analog IC Technology®

MP5000

12V, 5A Programmable Current Limit Switch

DESCRIPTION

The MP5000 is a protection device designed to protect circuitry on the output (source) from transients on input (V_{CC}). It also protects V_{CC} from undesired shorts and transients coming from the source.

At start up, inrush current is limited by limiting the slew rate at the source. The slew rate is controlled by a small capacitor at the dv/dt pin. The dv/dt pin has an internal circuit that allows the customer to float this pin (no connect) and still receive 1.1ms ramp time at the source.

The max load at the output (source) is current limited. This is accomplished by utilizing a sense FET topology. The magnitude of the current limit is controlled by an external resistor from the I-Limit pin to the Source pin.

An internal charge pump drives the gate of the power device, allowing a very low on-resistance DMOS power FET of just 44mΩ.

The source is protected from the V_{CC} input being too low or too high. Under Voltage Lockout (UVLO) assures that V_{CC} is above the minimum operating threshold, before the power device is turned on. If V_{CC} goes above the high output threshold, the source voltage will be limited.

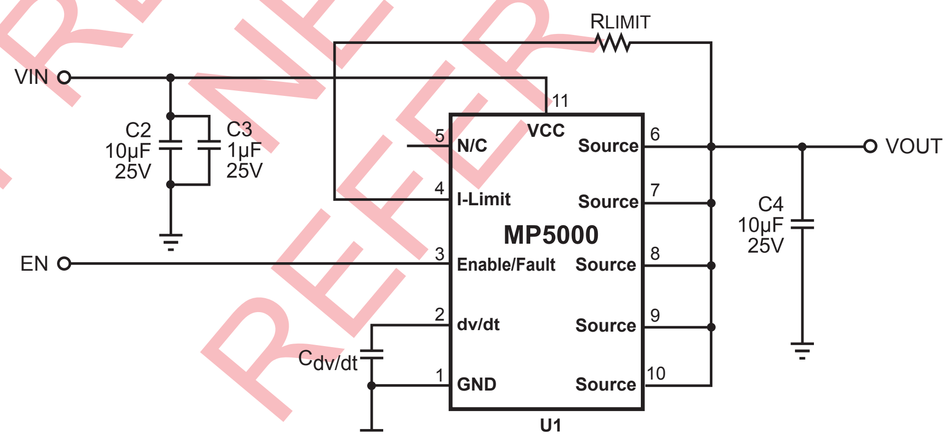
FEATURES

- Integrated 44mΩ Power FET
- Enable/Fault Pin
- Adjustable Slew Rate for Output Voltage
- Adjustable Current Limit: 1-5A
- Thermal Protection
- Over Voltage Limit

APPLICATIONS

- Hot Swap
- PC Cards
- Laptops

TYPICAL APPLICATION

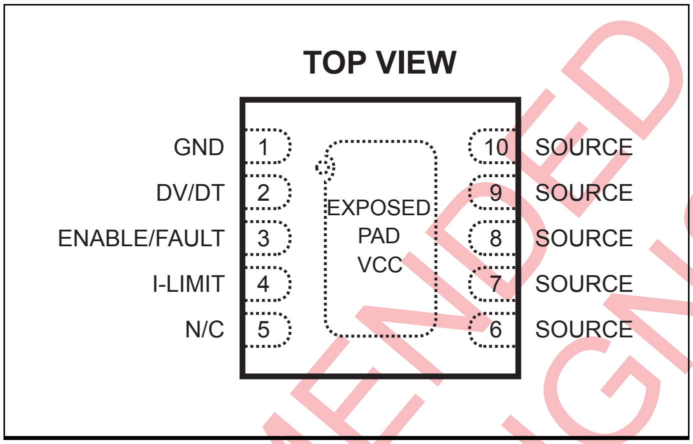


ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP5000DQ	QFN10 (3 x3mm)	V6	-40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP5000DQ–Z);
For RoHS Compliant Packaging, add suffix –LF (e.g. MP5000DQ–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

V_{CC}, SOURCE, I-LIMIT .... -0.3V to 22V
dv/dt, ENABLE/FAULT..................... -0.3V to 6V
Storage Temperature............... -65°C to +155°C
Continuous Power Dissipation (T_A = +25°C) (2)
....2.5W
Operating Junction Temperature. -40°C to 150°C
Input Voltage Operating Range........ 10V to 18V
Input Voltage Transient (100mS) .... V_{IN}=25V

***Thermal Resistance* (3)**	θ_{JA}	θ_{JC}	
QFN10	50	12 ...	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7 4-layer board.

ELECTRICAL CHARACTERISTICS

V_{CC} = 12V, R_{LIMIT}=22Ω, Capacitive Load = 100µF, T_A=25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Power FET						
Delay Time	t_{DLY}	Enabling of chip to I_D=100mA with a 1A resistive load		0.15		ms
ON Resistance (4)	R_{DSon}	T_J=25°C		44	82	mΩ
		T_J=80°C		95		
Off State Output Voltage	V_{OFF}	V_{CC}=18Vdc, V_{ENABLE}=0Vdc, R_L= 500Ω			120	mV
Continuous Current	I_D	0.5 in² pad,		4.2		A
		Minimum Copper, T_A=80°C		2.3		
Thermal Latch						
Shutdown Temperature	T_{SD}			175		°C
Under/Over Voltage Protection						
Output Clamping Voltage	V_{CLAMP}	Overvoltage Protection V_{CC}=17V	13.8	15	16.2	V
Under Voltage Lockout	V_{UVLO}	Turn on, Voltage going high	7.7	8.5	9.3	V
Under Voltage Lockout (UVLO) Hysteresis	V_{HYST}			0.80		V
Current Limit						
Hold Current (4)	I_{LIM-SS}	R_{LIM}=22Ω	2.4	3.7	5.0	A
Trip Current	I_{LIM-OL}	R_{LIM}=22Ω,		5.0		A
dv/dt Circuit						
Rise Time	T_r	Float dv/dt pin, Note 5	0.64	1.1	2.1	ms
Enable/Fault						
Low Level Input Voltage	V_{IL}	Output Disabled			0.5	V
Intermediate Level Input Voltage	$V_{I(INT)}$	Thermal Fault, Output Disabled	0.82	1.4	1.95	V
High Level Input Voltage	V_{IH}	Output Enabled	2.5			V
High State Maximum Voltage	$V_{I(MAX)}$			4.8		V
Low Level Input Current (Sink)	I_{IL}	V_{ENABLE}=0V		-28	-50	µA
Maximum Fanout for Fault Signal		Total number of chips that can be connected for simultaneous shutdown			3	Units
Maximum Voltage on Enable/Fault Pin	V_{MAX}	Note 6			VCC	V
Total Device						
Bias Current	I_{BIAS}	Device Operational		1.5	2.0	mA
		Thermal Shutdown		0.4		
Minimum Operating Voltage for UVLO	V_{MIN}	Enable<0.5V			5	V

Notes:

4) Guaranteed by design.
5) Measured from 10% to 90%.
6) Maximum Input Voltage on Enable pin to be ≤ 6.0V if Vcc ≥ 6.0V, Maximum Input Voltage on Enable pin to be Vcc if Vcc ≤ 6.0V.

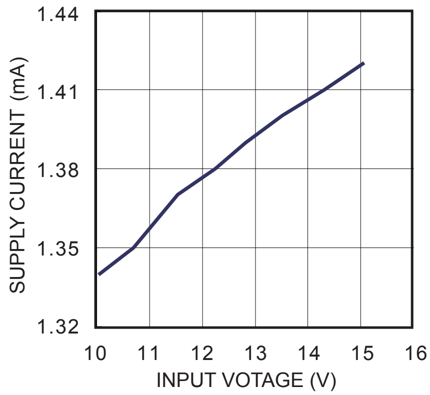
PIN FUNCTIONS

Pin #	Name	Description
1	GND	Negative Input Voltage to the Device. This is used as the internal reference for the IC.
2	dv/dt	The internal dv/dt circuit controls the slew rate of the output voltage at turn on. It has an internal capacitor that allows it to ramp up over the period of 1.1ms. An external capacitor can be added to this pin to increase the ramp time. If an additional time delay is not required, this pin should be left open.
3	Enable/Fault	The Enable/Fault pin is a tri-state, bi-directional interface. It can be used to enable the output of the device by floating the pin, or disable the chip by pulling it to ground (using an open drain or open collector device). If a thermal fault occurs, the voltage on this pin will go to an intermediate state to signal a monitoring circuit that the device is in thermal shutdown. See text: "ENABLE/FAULT PIN".
4	I-Limit	A resistor between this pin and the Source pin sets the overload and short circuit current limit levels.
5	N/C	DO NOT CONNECT. Pin must be left floating.
6-10	SOURCE	This pin is the source of the internal power FET and the output terminal of the IC.
11	V_{CC} (Exposed Pad)	Positive input voltage to the device (exposed pad).

TYPICAL PERFORMANCE CHARACTERISTICS

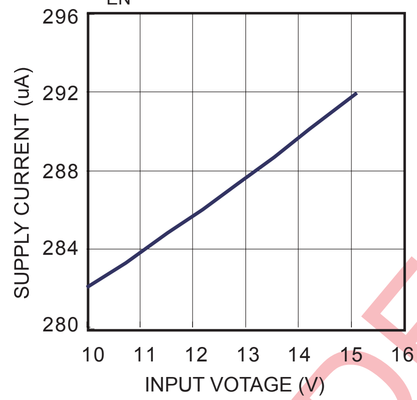
Supply Current, Output Enabled vs. Input Voltage

V_{EN}=3.3V, no load



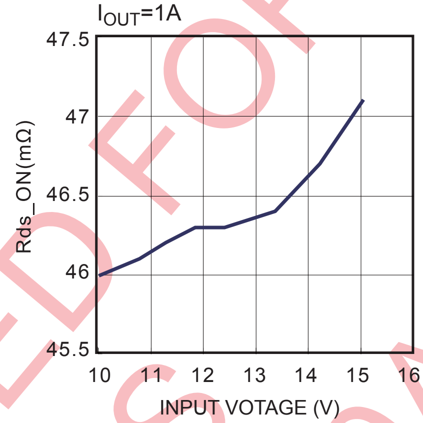
Supply Current, Output Disabled vs. Input Voltage

V_{EN}=0V

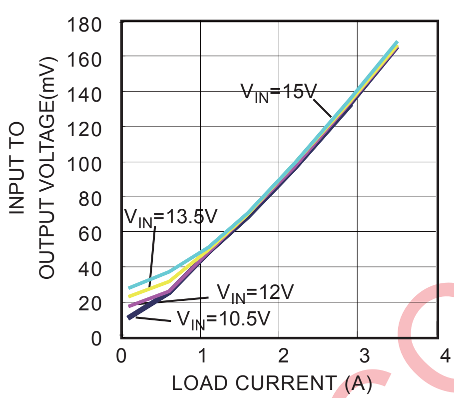


Static Drain-Source On-State Resistance vs. Input Voltage

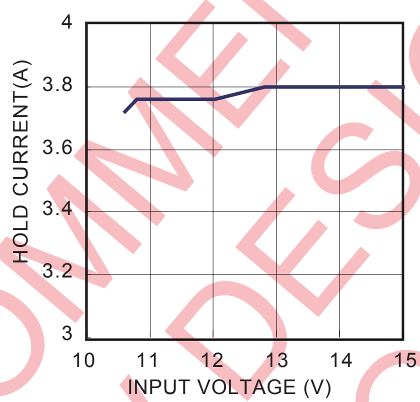
I_{OUT}=1A



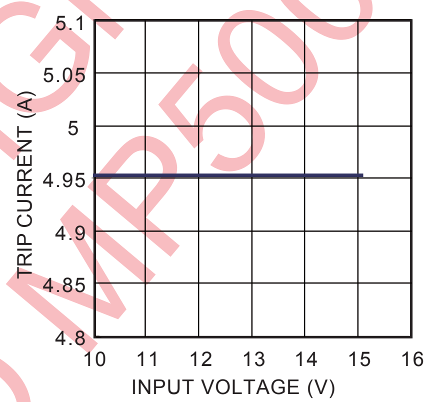
Input to Output Voltage vs. Load Current



Hold Current vs. Input Voltage

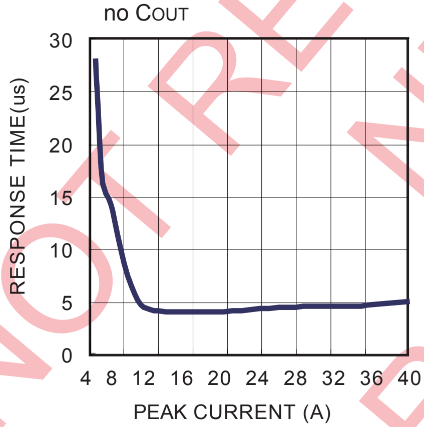


Trip Current Vs. Input Voltage

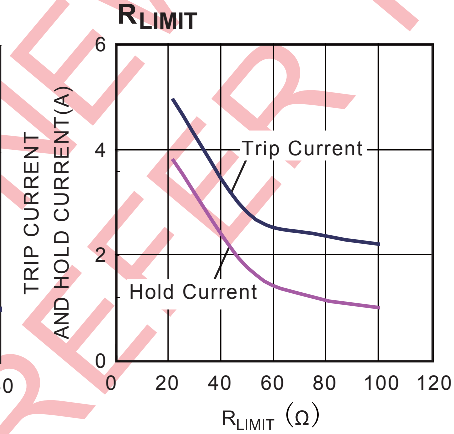


Current Limit Response Vs. Peak Current

no COUT



Trip Current and Hold Current vs. R_{LIMIT}

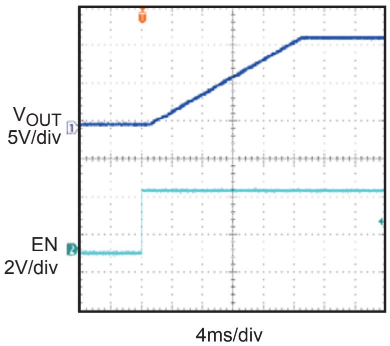


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN}=3.3V, R_{LIMIT}=22Ω, C_{OUT}=10uF, $C_{dv/dt}$=1nF, T_A=25°C, unless otherwise noted.

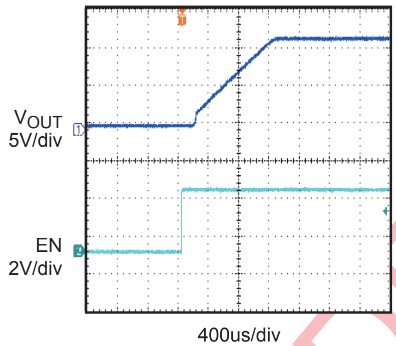
Turn On Delay and Rise Time with 1uF Load

C_{OUT}=1uF, no load, Cdv/dt=1nF



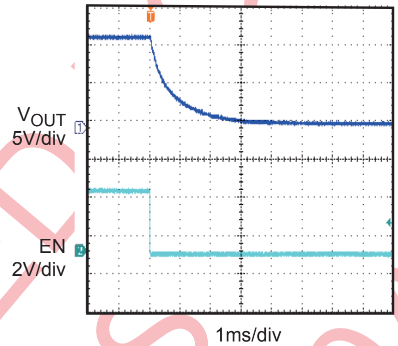
Turn On Delay and Rise Time with 1uF Load

C_{OUT}=1uF, no load, no Cdv/dt



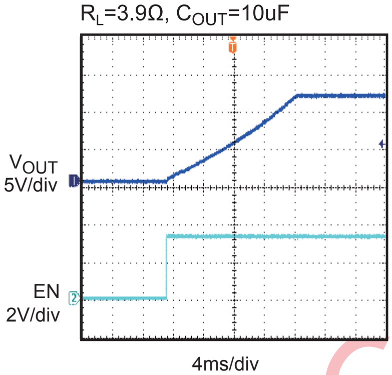
Turn Off Delay and Fall Time with 1uF Load

C_{OUT}=1uF, no load, Cdv/dt=1nF



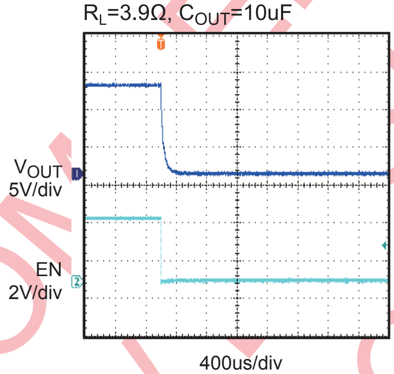
Turn Off Delay and Rise Time with 10uF Load

R_L=3.9Ω, C_{OUT}=10uF

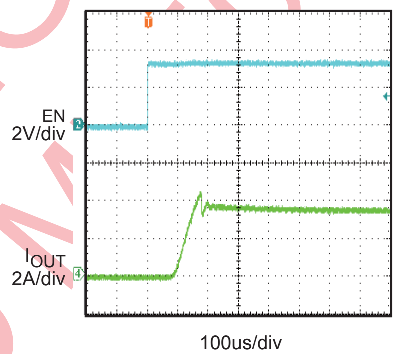


Turn Off Delay and Fall Time with 10uF Load

R_L=3.9Ω, C_{OUT}=10uF

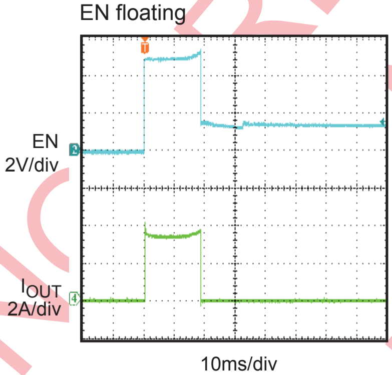


Short Circuit Current Device Enabled into Short

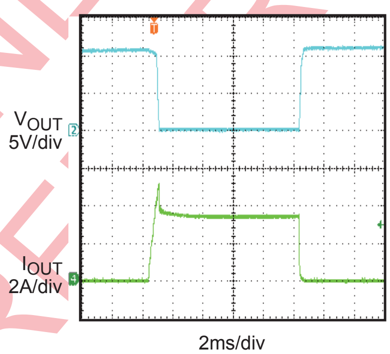


Short Circuit Current Device Enabled into Short and Thermal Shut Down

EN floating

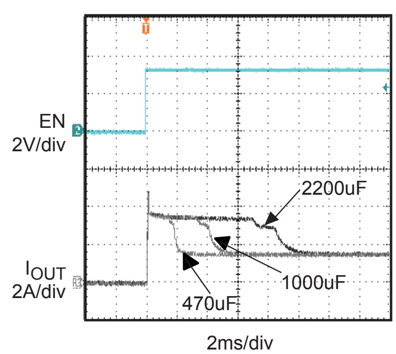


Trip Current with Ramped Load on Enabled Device



Inrush Current with Different Load Capacitance

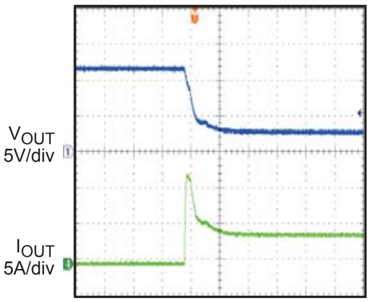
R_L=7.8Ω, no Cdv/dt, EN floating



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

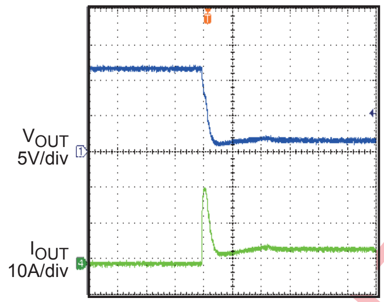
V_{IN} = 12V, V_{EN}=3.3V, R_{LIMIT}=22Ω, C_{OUT}=10uF, $C_{dv/dt}$=1nF, T_A=25°C, unless otherwise noted.

0.66Ω Load
Connected to Enabled Device



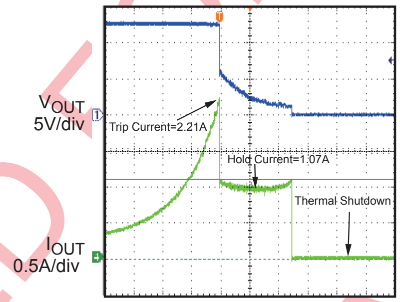
20us/div

0.33Ω Load
Connected to Enabled Device



20us/div

Current Limit
R_{LIMIT}=100Ω



40ms/div

BLOCK DIAGRAM

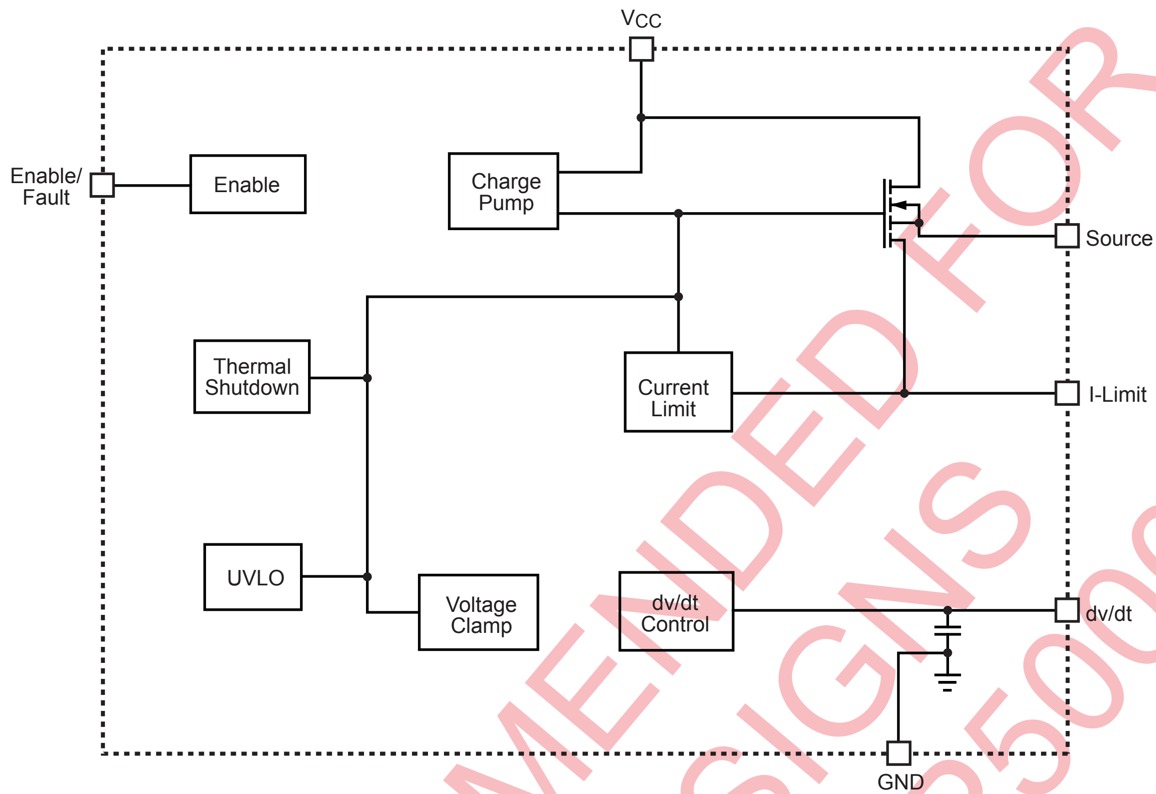


Figure 1—Function Block Diagram

CURRENT LIMIT

The desired current limit is a function of the external current limit resistor.

Table 1—Current Limit vs. Current Limit Resistor (V_{CC}=12V)

Current Limit Resistor (Ω)	22	50	100
Trip Current (A)	5	2.7	2.3
Hold Current (A)	3.7	1.63	1.1

When the part is active, if load reaches trip current (minimum threshold current triggering overcurrent protection) or a short is present, the part switches into to a constant-current (hold current) mode. Part will be shutdown only if the overcurrent condition stays long enough to trigger thermal protection.

However, when the part is powered up by V_{CC} or EN, the load current should be smaller than hold current. Otherwise, the part can't be fully turned on.

In a typical application using a current limit resistor of 22Ω, the trip current will be 5A and the hold current will be 3.7A. If the device is in its normal operating state and passing 2.0A it will need to dissipate only 176mW with the very low on resistance of 44mΩ. For the package dissipation of 50°C/Watt, the temperature rise will only be + 9°C. Combined with a 25°C ambient, this is only 34°C total package temperature.

During a short circuit condition, the device now has 12V across it and the hold current clamps at 3.7A and therefore must dissipate 44W. At 50°C/watt, if uncontrolled, the temperature would rise above the MP5000 thermal protection (+175°C) and shutdown the device to cause the temperature to drop below a hysteresis level. Proper heat sink must be used if the device is intended to supply the hold current and not shutdown. Without a heat sink, hold current should be maintained below 250mA at + 25°C and below 150mA at +85°C to prevent the device from activating the thermal shutdown feature.

RISE TIME

The rise time is a function of the capacitor (Cdvdt) on the dv/dt pin.

Table 2—Rise Time vs. Cdv/dt

Cdvdt	none	50pF	500pF	1nF
Rise Time (TYPICAL) (ms)	1.1	2.2	12.3	23.5

* **Notes:** Rise Time = K_{RT}*(50pF+$C_{dv/dt}$), K_{RT} =22E6

The "rise time" is measured by from 10% to 90% of output voltage.

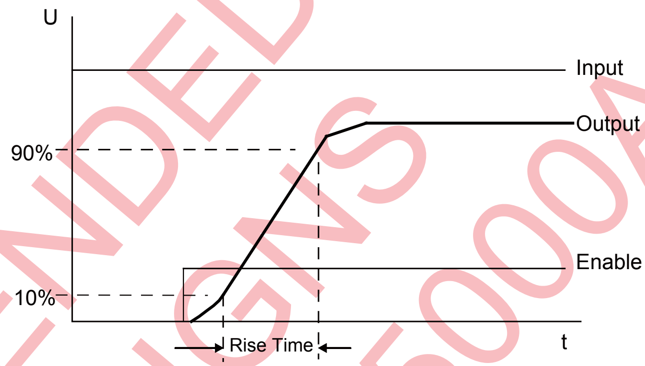


Figure 2—Rise Time

ENABLE / FAULT PIN

The Enable/Fault Pin is a Bi-Directional three levels I/O with a weak pull up current (25uA typical). The three levels are low, mid and high. It functions to enable/disable the part and to relay Fault information.

Enable/Fault pin as an input:

1. Low and mid disable the part.
2. Low, in addition to disabling the part, clears the fault flag.
3. High enables the part (if the fault flag is clear).

Enable/Fault pin as an output:

1. The pull up current may (if not over ridden) allow a "wired nor" pull up to enable the part.
2. An under voltage will cause a low on the Enable/Fault pin, and will clear the fault flag.

3. A thermal fault will cause a mid level on the Enable/Fault pin, and will set the fault flag.

The Enable/Fault line must be above the mid level for the output to be turned on.

The fault flag is an internal flip-flop that can be set or reset under various conditions:

1. Thermal Shutdown: set fault flag
2. Under Voltage: reset fault flag
3. low voltage on Enable/Fault pin: reset fault flag
4. mid voltage on Enable/Fault pin: no effect

Under a fault, the Enable/Fault pin is driven to the mid level.

There are 4 types of faults, and each fault has a direct and indirect effect on the Enable/Fault pin and the internal fault flag.

In a typical application there are one or more of the MP5000 (or MP5001) chips in a system. The Enable/Fault lines will typically be connected together.

Table 3—Fault Function Influence in Application

Fault description	Internal action	Effect on Fault Pin	Effect on Flag	Effect on secondary Part
Short/over current	Limit current	none	none	none
Under Voltage	Output is turned off	Internally drives Enable/Fault pin to Logic low	Flag is reset	Secondary part output is disabled, and fault flag is reset.
Over Voltage	Limit output voltage	None	None	None
Thermal Shutdown	Shutdown part. The part is latched off until a UVLO or externally driven to ground.	Internally drives Enable/Fault pin to mid level	Flag is set	Secondary part output is disabled.

UNDER VOLTAGE LOCK OUT OPERATION

If the supply (input) is below the UVLO threshold, the output is disabled, and the fault line is driven low.

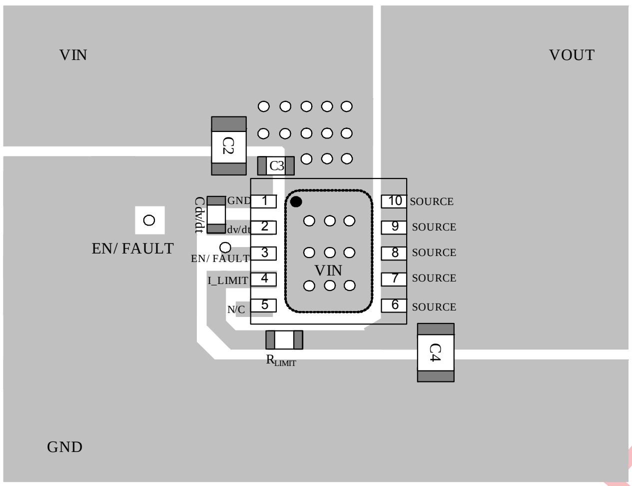
When the supply goes above the UVLO threshold, the output is enabled and the fault line is released. When the fault line is released it will be pulled high by a 25uA current source. No external pull up resistor is required. In addition, the pull up voltage is limited to 5 volts.

THERMAL PROTECTION

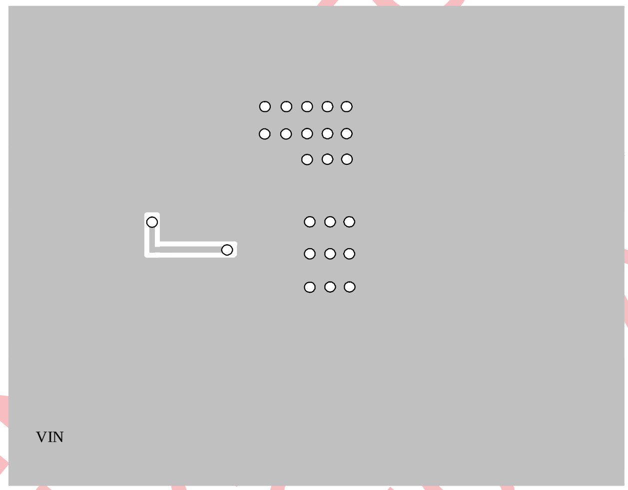
When thermal protection is detected, the output is disabled and the fault line is driven to the mid level. The thermal fault condition is latched (meaning the fault flag is set), and the part will remain latched off until the fault (enable) line is brought low. Cycling the power below the UVLO threshold will also reset the fault flag.

PCB LAYOUT

PCB layout is very important to achieve stable operation. Please follow these guidelines and take below figure for reference. Place Rlimit close to I_limit pin, Cdv/dt close to dv/dt pin and input cap close to V_{CC} pin. Keep the N/C pin float. Put vias in thermal pad and ensure enough copper area near V_{CC} and source to achieve better thermal performance.



Top Layer



Bottom Layer

Figure 3—PCB Layout