The Future of Analog IC Technology®

# MP6900

## Fast Turn-off Intelligent Controller

## DESCRIPTION

The MP6900 is a low-drop, fast turn-off intelligent controller that combined with an external switch replaces Schottky diodes in high-efficiency, Flyback converters. The chip regulates the forward drop of an external switch to about 70mV and switches it off as soon as the voltage becomes negative. Package choices are a space saving TSOT23-5, QFN6 (3x3mm) or SOIC-8.

## FEATURES

- Works with both Standard and Logic Level FETS
- Compatible with Energy Star, 1W Standby Requirements
- $V_{DD}$ Range From 8V to 24V
- 70mV $V_{DS}$ Regulation Function (1)
- Fast Turn-off Total Delay of 20ns
- Max 400kHz Switching Frequency
- <3mA Low Quiescent Current
- Supports CCM, DCM and Quasi-Resonant Topologies
- Supports High-side and Low-side Rectification
- Power Savings of Up to 1.5W in a Typical Notebook Adapter

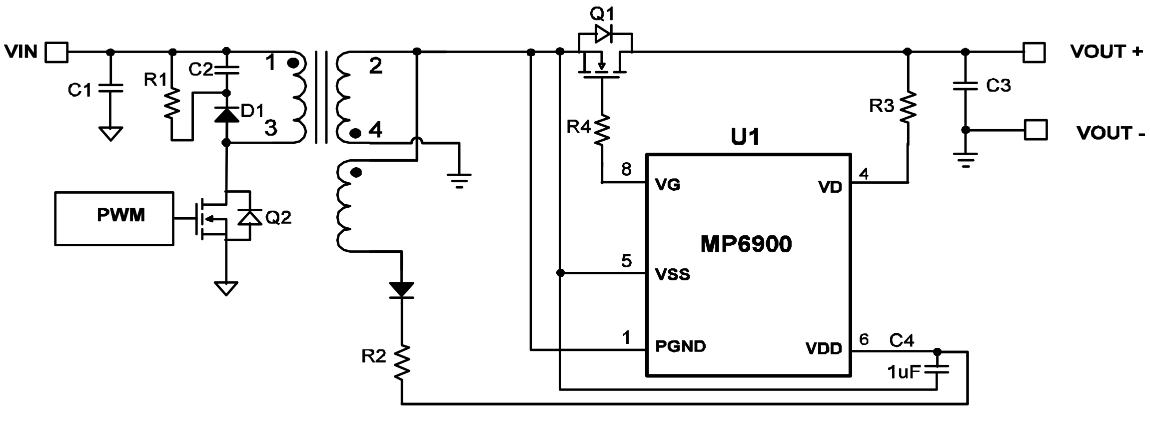
## APPLICATIONS

- Industrial Power Systems
- Distributed Power Systems
- Battery Powered Systems
- Flyback Converters

**Notes:**

1) Related issued patent: US Patent US8,067,973; CN Patent ZL201010504140.4. Other patents pending.

## TYPICAL APPLICATION



# ORDERING INFORMATION

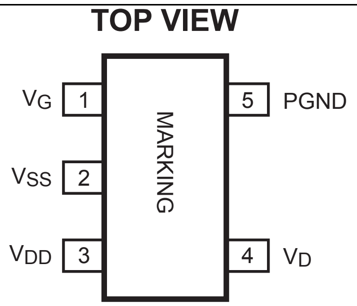
| Part Number | Package | Top Marking |
|---|---|---|
| MP6900DJ* | TSOT23-5 | 6D |
| MP6900DS** | SOIC-8 | MP6900DS |
| MP6900DQ*** | QFN6 (3x3mm) | 5D |

* For Tape & Reel, add suffix –Z (e.g. MP6900DJ–Z).
For RoHS Compliant Packaging, add suffix –LF (e.g. MP6900DJ–LF–Z)

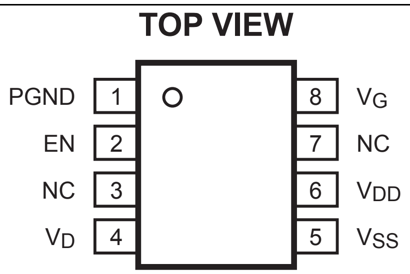
** For Tape & Reel, add suffix –Z (e.g. MP6900DS–Z).
For RoHS Compliant Packaging, add suffix –LF (e.g. MP6900DS–LF–Z)

*** For Tape & Reel, add suffix –Z (e.g. MP6900DQ–Z).
For RoHS Compliant Packaging, add suffix –LF (e.g. MP6900DQ–LF–Z)

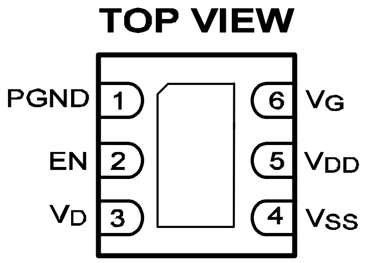
# PACKAGE REFERENCE



TSOT23-5



SOIC-8



QFN6 (3x3mm)

## ABSOLUTE MAXIMUM RATINGS [2]

| | |
|---|---|
| $V_{DD}$ to $V_{ss}$ | -0.3V to +27V |
| PGND to $V_{Ss}$ | -0.3V to +0.3V |
| $V_G$ to $V_{SS}$ | -0.3V to $V_{CC}$ |
| $V_D$ to $V_{SS}$ | -0.7V to +180V |
| EN to $V_{SS}$ | -0.3V to +6.5V |
| Maximum Operating Frequency | 400kHz |
| Continuous Power Dissipation ($T_A$ = +25°C) [3] | |
| SOIC8 | 1.39W |
| TSOT23-5 | 0.57W |
| QFN6 (3x3mm) | 2.5W |
| Junction Temperature | 150°C |
| Lead Temperature (Solder) | 260°C |
| Storage Temperature | -55°C to +150°C |

### *Recommended Operation Conditions* [4]

| | |
|---|---|
| $V_{DD}$ to $V_{ss}$ | 8V to 24V |
| Operating Junction Temp. ($T_J$) | -40°C to +125°C |

### *Thermal Resistance* [5]

| | $\theta_{JA}$ | $\theta_{JC}$ | |
|---|---|---|---|
| SOIC8 | 90 | 45 | °C/W |
| TSOT23-5 | 220 | 110 | °C/W |
| QFN6 (3x3mm) | 50 | 12 | °C/W |

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**Notes:**

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature. $T_J$(MAX) the junction-to-ambient thermal resistance $\theta_{JA}$ and the ambient temperature $T_A$. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_D(MAX)=(T_J(MAX)-T_A)/\ \theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

# ELECTRICAL CHARACTERISTICS

## $V_{DD}$ = 12V, $T_A$= +25°C, unless otherwise noted.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{DD}$ Voltage Range | | 8 | | 24 | V |
| $V_{DD}$ UVLO Rising | | 5.0 | 6.0 | 7.0 | V |
| $V_{DD}$ UVLO Hysteresis | | | 1.2 | | V |
| Operating Current | $C_{LOAD}$=5nF, $_{SW}$=100kHz | | 8 | 12 | mA |
| Quiescent Current | No Switching | | 2 | 3 | mA |
| Shutdown Current | $V_{DD}$ =4 V | | 100 | 150 | μA |
| $V_{DD}$=20V | EN=0V (50kΩ) | | | 250 | μA |
| Thermal Shutdown | | | 170 | | °C |
| Thermal Shutdown hysteresis | | | 50 | | °C |
| Enable (Low) | SOIC-8 only | | | 0.8 | V |
| Enable (High) | SOIC-8 only | 2 | | | V |
| Pull-up Current On Enable | SOIC-8 only | 5 | 10 | | μA |
| **CONTROL CIRCUITRY SECTION** | | | | | |
| $V_{SS}$ –$V_D$ Forward Voltage, Vfwd | | 55 | 70 | 85 | mV |
| Turn-on Delay | $C_{LOAD}$ = 5nF | | 150 | | ns |
| | $C_{LOAD}$ = 10nF | | 200 | | ns |
| Pull-down Resistance of $V_G$ Pin | | | 10 | 20 | kΩ |
| Input Bias Current On $V_D$ Pin | -0.3V > $V_D$ >180V | | | 10 | μA |
| Minimum On-time | $C_{LOAD}$ = 5nF | | 200 | | ns |
| **GATE DRIVER SECTION** | | | | | |
| $V_G$ (Low) | $I_{LOAD}$=1mA | | 0.05 | 0.5 | V |
| $V_G$ (High) | $V_{DD}$ >17V | 12 | 13.5 | 15 | V |
| | $V_{DD}$ <17V | $V_{DD}$-2.2 | | | |
| Turn-off Threshold ($V_{SS}$-$V_D$) | | 20 | 30 | 40 | mV |
| Turn-off Propagation Delay | $V_D$=$V_{SS}$, $R_{GATE}$=0Ω | | 15 | | ns |
| Turn-off Total Delay [6] | $V_D$ =$V_{SS}$, $C_{LOAD}$=5nF, $R_{GATE}$=0Ω | | 20 | 35 | ns |
| | $V_D$ =$V_{SS}$, $C_{LOAD}$=10nF, $R_{GATE}$=0Ω | | 30 | 45 | ns |
| Pull-down Impedance | | | 1 | 2 | Ω |
| Pull-down Current | 3V <$V_G$ <10V | | 2 | | A |

**Notes:**

6) Guaranteed by Design and Characterization

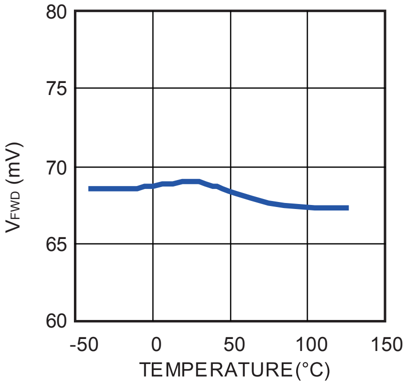
## PIN FUNCTIONS

| TSOT23-5 Pin # | SOIC8 Pin # | QFN6 (3x3mm) Pin # | Name | Description |
|---|---|---|---|---|
| 1 | 8 | 6 | VG | Gate drive output |
| 2 | 5 | 4 | VSS | Ground, also used as reference for VD |
| 3 | 6 | 5 | VDD | Supply Voltage |
| 4 | 4 | 3 | VD | FET drain voltage sense |
| 5 | 1 | 1 | PGND | Power Ground, return for driver switch |
| - | 2 | 2 | EN | Enable pin, active high |
| - | 3 |  | NC | No connection |
| - | 7 |  | NC | No connection |

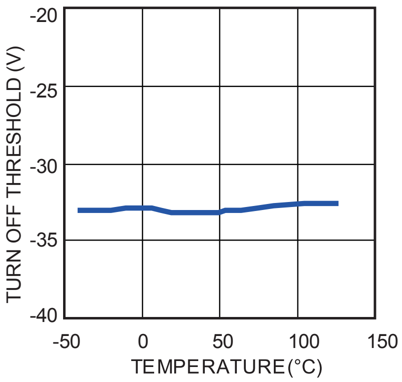
## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{DD}$ = 12V, unless otherwise noted.**

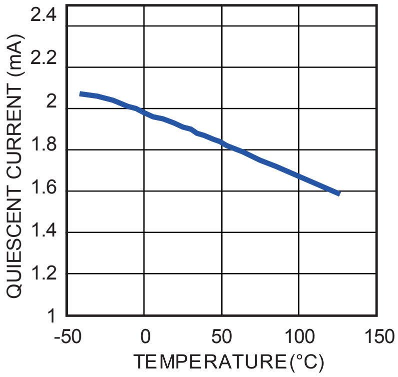
**$V_{FWD}$ vs. Temperature**



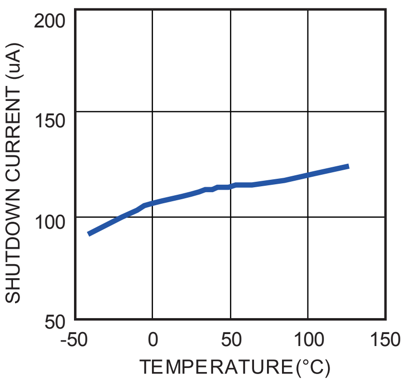
**Turn off threshold vs. Temperature**



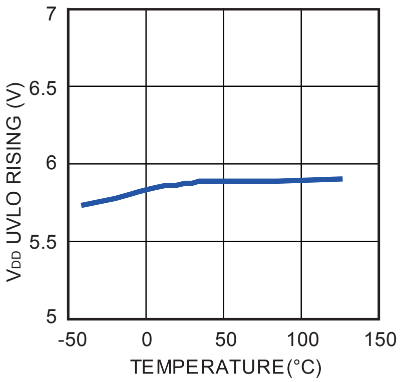
**Quiescent Current vs. Temperature**



**Shutdown Current vs. Temperature**

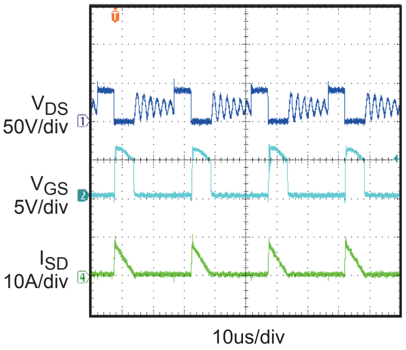


**$V_{DD}$ UVLO Rising vs. Temperature**



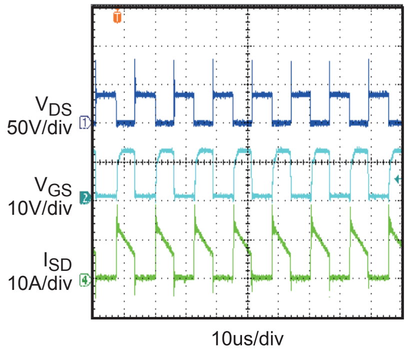
**Operation in 90W Flyback Application(5)**

($V_{IN}$=90Vac, $I_{OUT}$=1A)



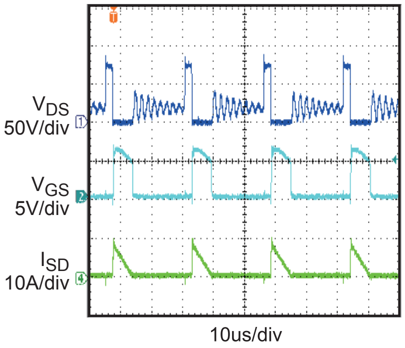
**Operation in 90W Flyback Application**

($V_{IN}$=90Vac, $I_{OUT}$=4.7A)



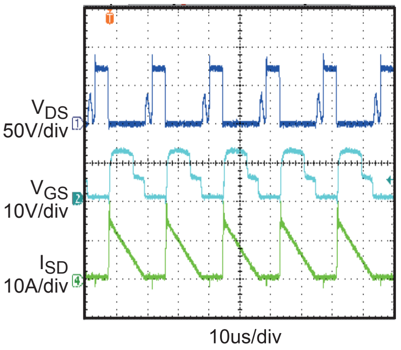
**Operation in 90W Flyback Application**

($V_{IN}$=250Vac, $I_{OUT}$=1A)



**Operation in 90W Flyback Application**

($V_{IN}$=250Vac, $I_{OUT}$=4.7A)



**Notes:**

7) See Fig.7 for the test circuit..

## BLOCK DIAGRAM

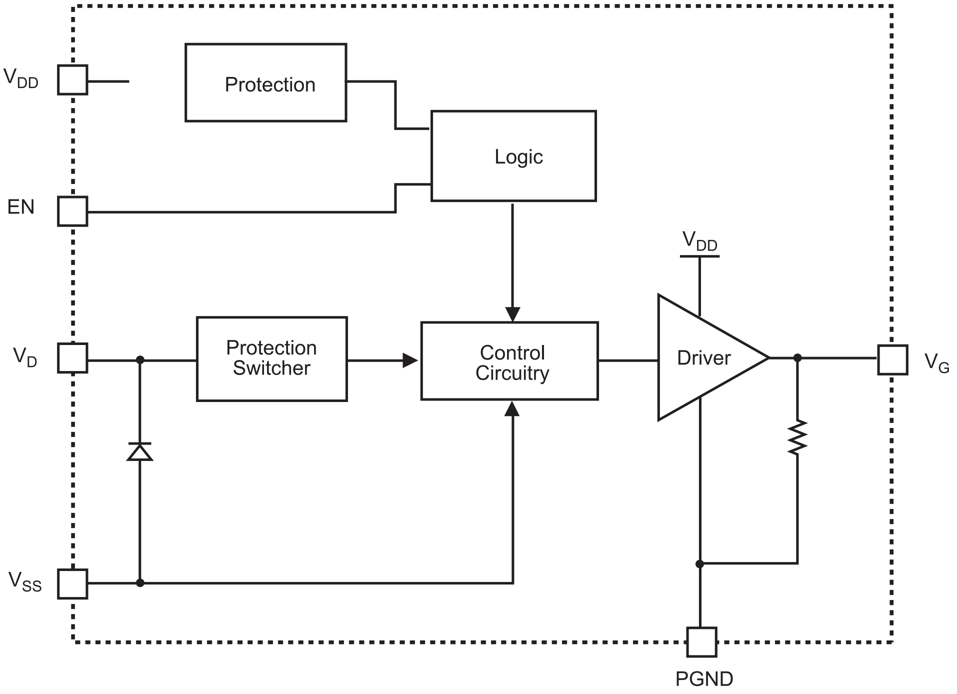


**Figure 1—Functional Block Diagram**

## OPERATION

The MP6900 supports operation in CCM, DCM and Quasi-Resonant topologies. Operating in either a DCM or Quasi-Resonant topology, the control circuitry controls the gate in forward mode and will turn the gate off when the MOSFET current is fairly low. In CCM operation, the control circuitry turns off the gate when very fast transients occur.

### Blanking

The control circuitry contains a blanking function. When it pulls the MOSFET on/off, it makes sure that the on/off state at least lasts for some time. The turn on blanking time is 200ns, which determines the minimum on-time. During the turn on blanking period, the turn off threshold is not totally blanked, but changes the threshold voltage to ~+50mV (instead of -30mV). This assures that the part can always be turned off even during the turn on blanking period. (Albeit slower, so it is not recommended to set the synchronous period less than 200ns at CCM condition in flyback converter, otherwise shoot through may occur)

### VD Clamp

Because $V_D$ can go as high as 180V, a High-Voltage JFET is used at the input. To avoid excessive currents when Vg goes below -0.7V, a small resistor is recommended between $V_D$ and the drain of the external MOSFET.

### Under-Voltage Lockout (UVLO)

When the VDD is below UVLO threshold, the part is in sleep mode and the Vg pin is pulled low by a 10kΩ resistor.

### Enable pin

The Enable function is only available on the SOIC-8 package. If EN is pulled low, the part is in sleep mode.

### Thermal shutdown

If the junction temperature of the chip exceeds 170°C, the Vg will be pulled low and the part stops switching. The part will return to normal function after the junction temperature has dropped to 120°C.

### Thermal Design

If the dissipation of the chip is higher than 100mW due to switching frequencies above 100kHz, VDD higher than 15V and/or Cload larger than 5nF, it is recommended to use the thermally-enhanced SOIC-8.

### Turn-on Phase

When the synchronous MOSFET is conducting, current will flow through its body diode which generates a negative Vds across it. Because this body diode voltage drop (<-500mV) is much smaller than the turn on threshold of the control circuitry (-70mV), which will then pull the gate driver voltage high to turn on the synchronous MOSFET after about 150ns turn on delay (Defined in Fig.2).

As soon as the turn on threshold (-70mV) is triggered, a blanking time (Minimum on-time: ~200ns) will be added during which the turn off threshold will be changed from -30mV to +50mV. This blanking time can help to avoid error trigger on turn off threshold caused by the turn on ringing of the synchronous MOSFET.

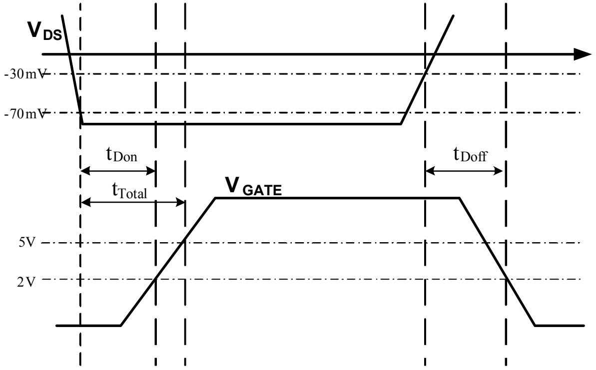


**Figure 2—Turn on and Turn off delay**

### Conducting Phase

When the synchronous MOSFET is turned on, Vds becomes to rise according to its on resistance, as soon as Vds rises above the turn on threshold (-70mV), the control circuitry stops pulling up the gate driver which leads the gate voltage is pulled down by the internal pull-down resistance (10kΩ) to larger the on resistance of synchronous MOSFET to ease the rise of Vds. By doing that, Vds is adjusted to be around -70mV even when the current through the MOS is fairly small, this function can make the driver voltage fairly low when the synchronous MOSFET is turned off to fast the turn off speed (this function is still active during turn on blanking time which means the gate driver could still be turned off even with very small duty of the synchronous MOSFET).

### Turn-off Phase

When Vds rises to trigger the turn off threshold (-30mV), the gate voltage is pulled to low after about 20ns turn off delay (defined in Fig.2) by the control circuitry. Similar with turn-on phase, a 200ns blanking time is added after the synchronous MOSFET is turned off to avoid error trigger.

Fig.3 shows synchronous rectification operation at heavy load condition. Due to the high current, the gate driver will be saturated at first. After Vds goes to above -70mV, gate driver voltage decreases to adjust the Vds to typical -70mV.

Fig 4 shows synchronous rectification operation at light load condition. Due to the low current, the gate driver voltage never saturates but begins to decrease as soon as the synchronous MOSFET is turned on and adjust the Vds.

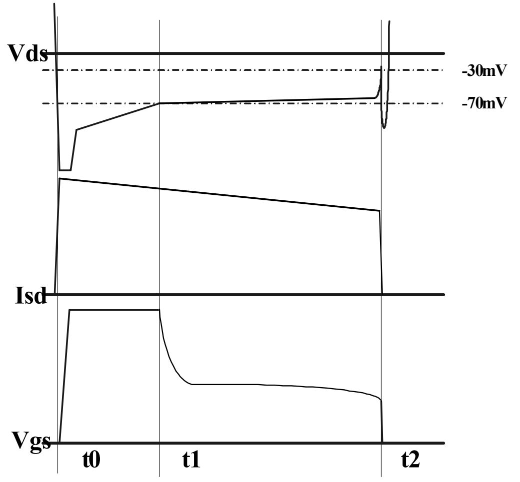


**Figure 3—Synchronous Rectification Operation at heavy load**

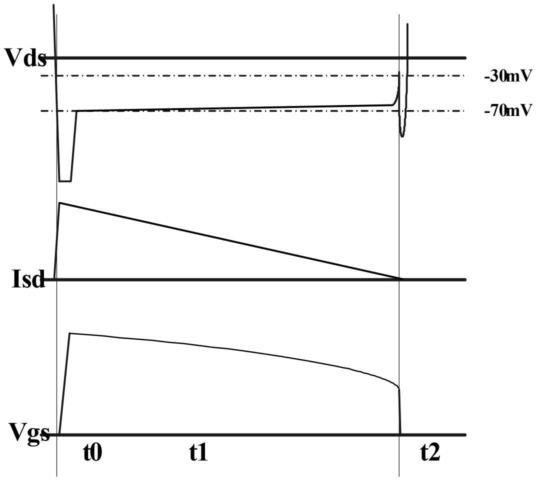


**Figure 4—Synchronous Rectification Operation at light load**

### SR Mosfet Selection and Driver ability

The Power Mosfet selection proved to be a trade off between Ron and Qg. In order to achieve high efficiency, the Mosfet with smaller Ron is always preferred, while the Qg is usually larger with smaller Ron, which makes the turn-on/off speed lower and lead to larger power loss. For MP6900, because Vds is regulated at ~-70mV during the driving period, the Mosfet with too small Ron is not recommend, because the gate driver may be pulled down to a fairly low level with too small Ron when the Mosfet current is still fairly high, which make the advantage of the low Ron inconspicuous.

Fig.5 shows the typical waveform of QR flyback. Assume 50% duty cycle and the output current is $I_{OUT}$.

To achieve fairly high usage of the Mosfet's Ron, it is expected that the Mosfet be fully turned on at least 50% of the SR conduction period:

$$Vds = -Ic \times Ron = -2 \cdot I_{OUT} \times Ron \le -Vfwd$$

Where $V_{ds}$ is Drain-Source voltage of the Mosfet and $V_{fwd}$ is the forward voltage threshold of MP6902, which is ~70mV.

So the Mosfet's Ron is recommended to be no lower than ~35/$I_{OUT}$ (mΩ). (For example, for 5A application, the Ron of the Mosfet is recommended to be no lower than 7mΩ)

Fig.6 shows the corresponding total delay during turn-on period ($t_{Total}$, see Fig.2) with driving different Qg Mosfet by MP6902. From Fig.6, with driving a 120nC Qg Mosfet, the driver ability of MP6900 is able to pull up the gate driver voltage of the Mosfet to ~5V in 300ns as soon as the body diode of the Mosfet is conducting, which greatly save the turn-on power loss in the Mosfet's body diode.

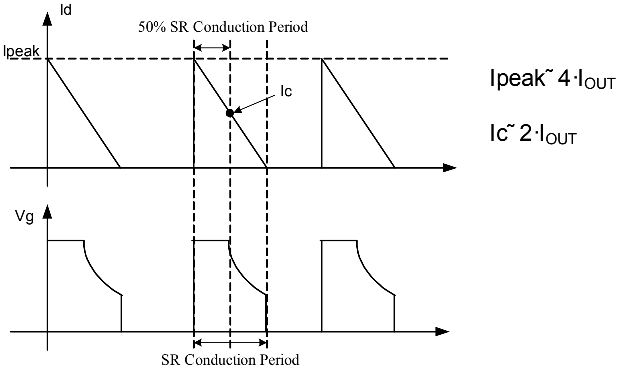


**Figure 5—Synchronous Rectification typical waveforms in QR Flyback**

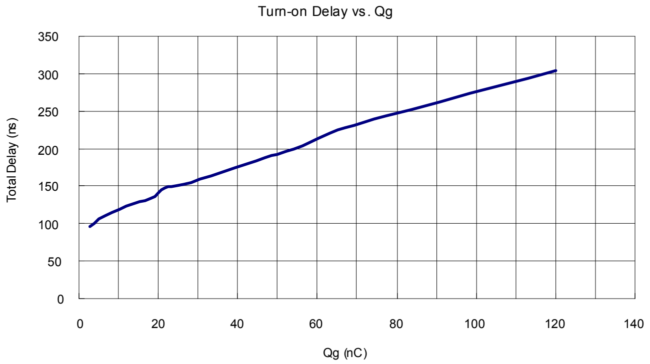


**Figure 6—Total Turn-on Delay vs. Q**

# TYPICAL APPLICATION CIRCUIT

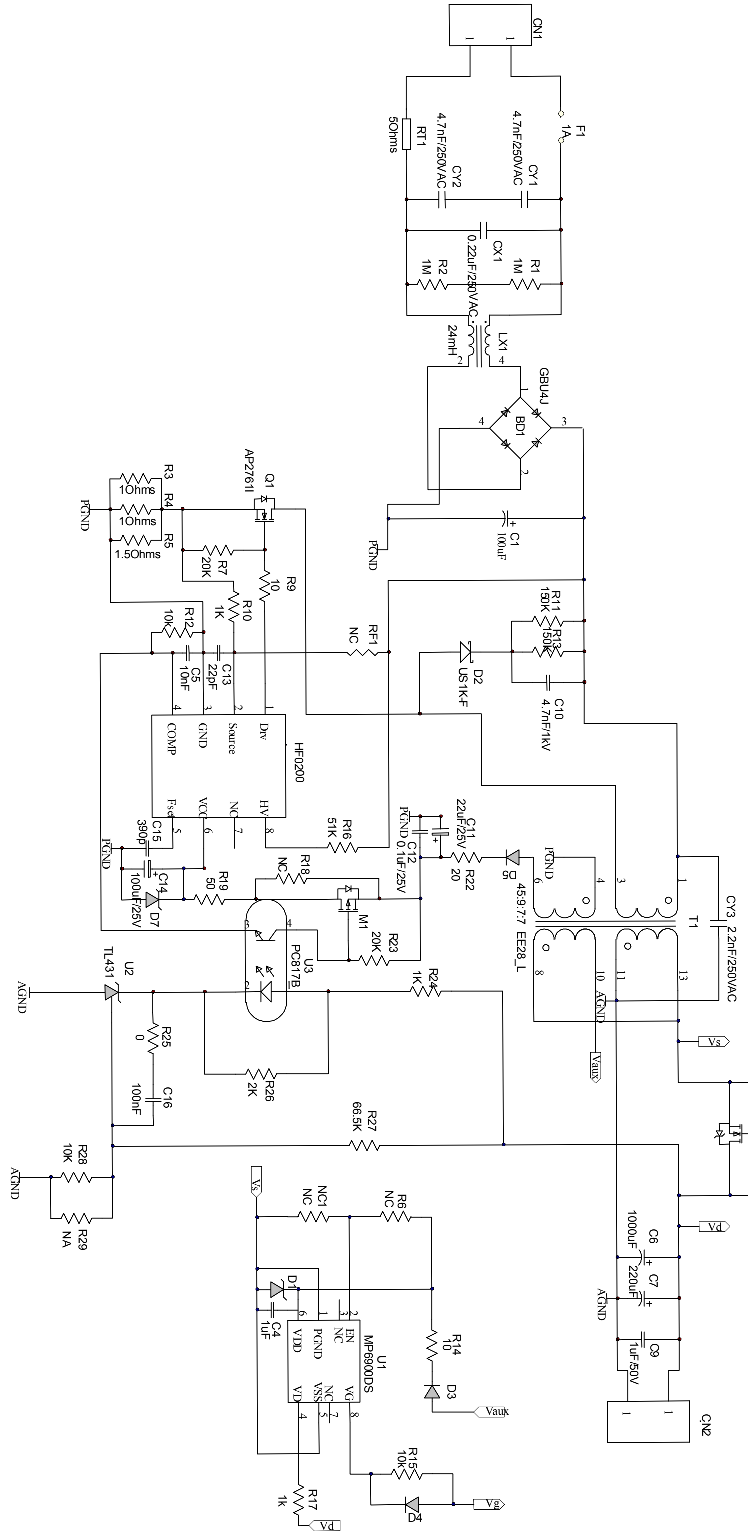
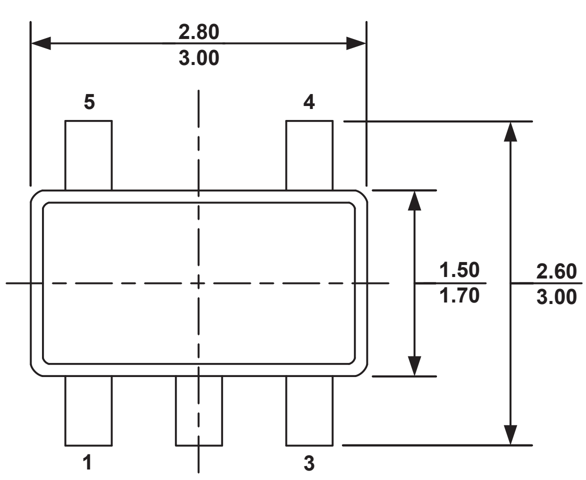


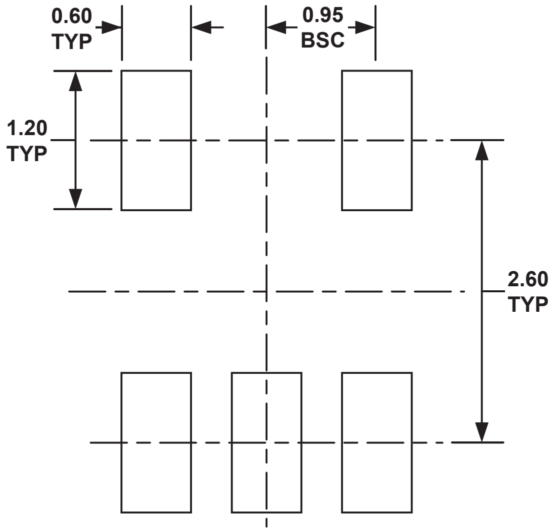
Figure 7—MP6900 for Secondary Synchronous Controller in 90W Flyback Application

# PACKAGE INFORMATION

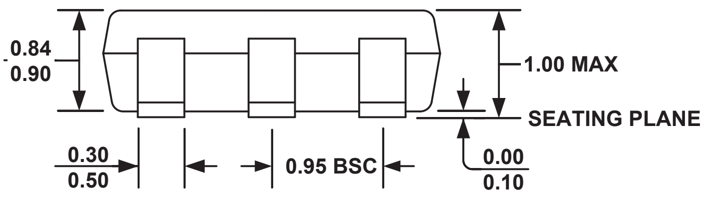
## TSOT23-5



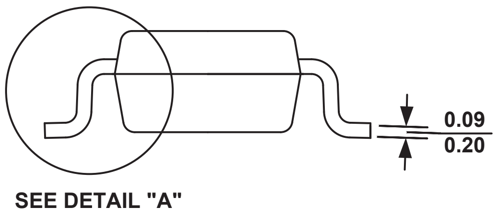
**TOP VIEW**



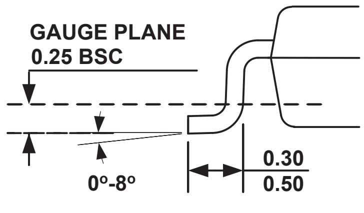
**RECOMMENDED LAND PATTERN**



**FRONT VIEW**



**SIDE VIEW**

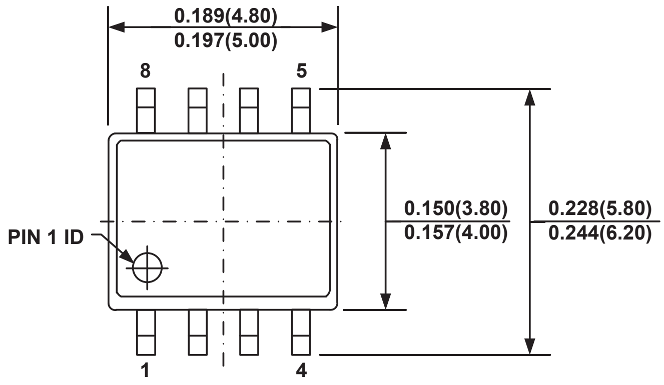


**DETAIL "A"**

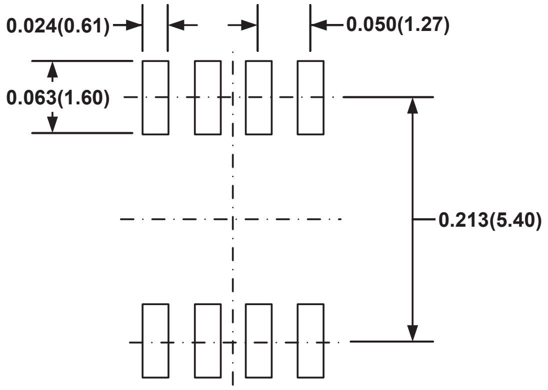
**NOTE:**

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

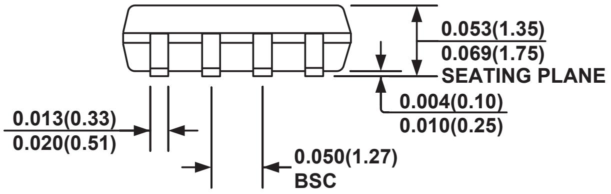
## SOIC8



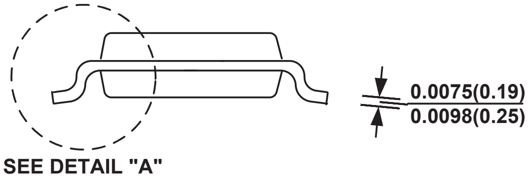
TOP VIEW



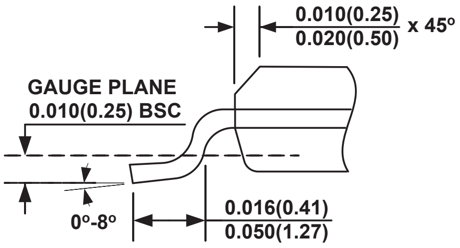
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.