MP6919

CCM/DCM Flyback Ideal Diode with Integrated 100V/13mΩ MOSFET and No Need for Auxiliary Winding

DESCRIPTION

The MP6919 is a fast turn-off, intelligent rectifier for flyback converters that integrates a 100V MOSFET. It offers higher efficiency and power density than a diode rectifier. The chip regulates the forward voltage drop of the internal power switch to 40mV [(1)], and turns off before the drain-source voltage reverses.

The device generates its own supply voltage without requiring auxiliary winding. This feature makes it suitable for charger applications with a low output voltage requirement, or any other adapter applications with high-side set-up. The internal ringing detection circuitry prevents the MP6919 from falsely turning on during discontinuous conduction mode (DCM) or quasi-resonant operations.

The MP6919 is available in an SOIC-8 package.

FEATURES

- Integrated 100V/13mΩ MOSFET
- Wide Output Range Down to 0V
- Does not Require Auxiliary Winding for High-Side or Low-Side Rectification
- Ringing Detection Prevents False Turn-On during DCM Operations
- Compatible with Energy Star
- 110µA Quiescent Current
- Supports DCM, CCM, and Quasi-Resonant Operations
- Available in an SOIC-8 Package

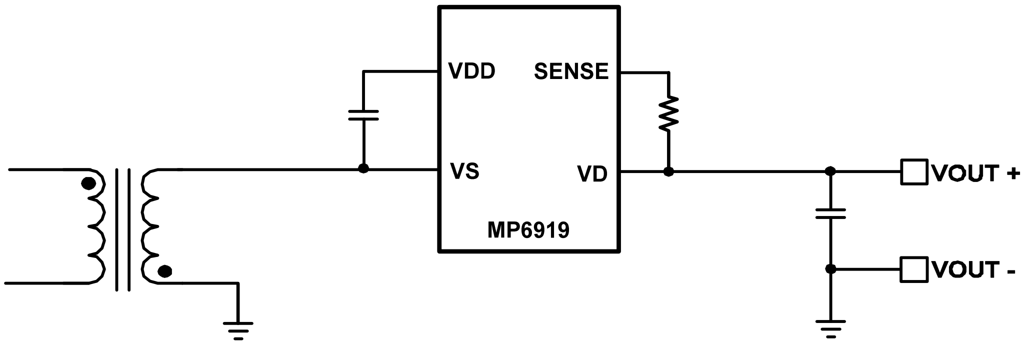
APPLICATIONS

- Laptop Adapters
- QC and USB PD Chargers
- High-Efficiency Flyback Converters

Note:

1) Related issued patent: US Patent US8, 067,973; CN Patent ZL201010504140.4. Other patents pending.

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MP6919GS*	SOIC-8	*See Below*	*3*

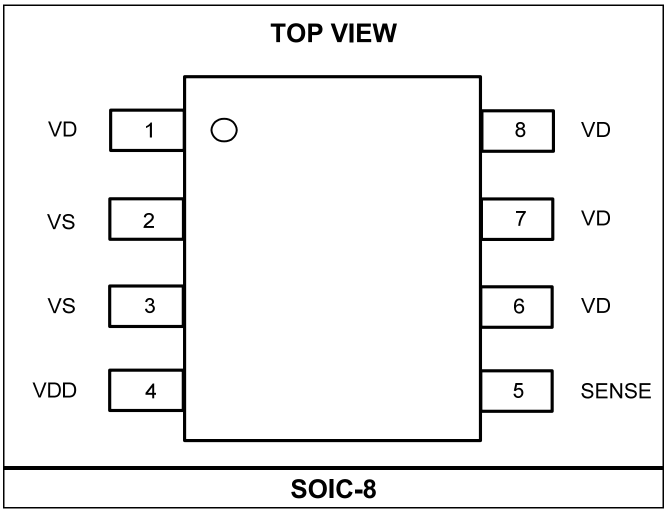
* For Tape & Reel, add suffix –Z (e.g. MP6919GS–Z).

TOP MARKING

MP6919
LLLLLLLL
MPSYWW

MP6919: Part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1, 6, 7, 8	VD	**MOSFET drain.**
2, 3	VS	**MOSFET source.** VS is also used as a reference for VDD.
4	VDD	**Linear regulator output.** VDD is the supply of the MP6919.
5	SENSE	**MOSFET drain voltage sensing.** SENSE is also used as the linear regulator input.

ABSOLUTE MAXIMUM RATINGS [2]

VDD to VS....................................-0.3V to +14V
VD to VS.....................................-1.5V to +100V
SENSE to VS.................................-1V to +180V
Continuous drain current (T_C = 25°C)........14.1A
Continuous drain current (T_C = 100°C)........8.9A
Pulsed drain current [3]..................................50A
Maximum power dissipation [4]...................1.7W
Junction temperature................................150°C
Lead temperature (solder)........................260°C
Storage temperature ....-55°C to +150°C

ESD Rating

Human-body model (HBM)...............±1200V
Charged-device model (CDM)...........±2000V

Recommended Operation Conditions [5]

VDD to VS....................................... 4.5V to 13V
Operating junction temp (T_J).....-40°C to +125°C

Thermal Resistance [6]	θ_{JA}	θ_{JC}	
SOIC-8	70	32	°C/W

Notes:

2) Exceeding these ratings may damage the device.
3) Repetitive rating: Pulse width = 100μs, duty cycle limited by maximum junction temperature.
4) T_A = 25°C. The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
5) The device is not guaranteed to function outside of its operating conditions.
6) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VDD = V_{DD_REG}, T_J = -40 to +125°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-source breakdown voltage	$V_{(BR)DSS}$	T_J = 25°C	100			V
VDD regulation voltage	V_{DD_REG}	SENSE = 12V, C_{DD} = 1µF	6.3	6.7	7	V
VDD UVLO rising			4.0	4.2	4.4	V
VDD UVLO hysteresis			0.1	0.24	0.38	V
VDD maximum charging current	I_{VDD}	VDD = 5.5V, SENSE = 30V		63		mA
Operating current	I_{CC}	f_{SW} = 100kHz		2.4	4	mA
Quiescent current	$I_{Q(VDD)}$	VDD = 7V		110	135	µA
Control Circuitry Section						
Forward regulation voltage (VS-VD) [7]	V_{fwd}		25	40	55	mV
Turn-on threshold (VDS)			-115	-80	-57	mV
Turn-off threshold (VS-VD) [7]			-6	3	+12	mV
Turn-on delay [8]	t_{DON}			20		ns
Turn-off delay [7]	t_{DOFF}			25		ns
Turn-on blanking time	t_{B-ON}		0.8	1.2	1.55	µs
Turn-off blanking threshold (VDS)	V_{B-OFF}		2		3	V
Turn-off threshold during minimum on time (VDS)				1.8		V
Turn-on slew rate detection time [8]				30		ns
Power Switch Section						
Single pulse avalanche energy	E_{AS}	V_{PS} = 50V, V_{GS} = 6.7V, L = 1.0mH, T_J = 25°C		100		mJ
Drain-source on state resistance	$R_{DS(ON)}$	I_D = 2A, T_J = 25°C		13	16.3	mΩ
Input capacitance	C_{ISS}	V_{DS} = 40V, V_{GS} = 0V, f = 1MHz		1925		pF
Output capacitance	C_{OSS}			307		pF
Reverse transfer capacitance	C_{RSS}			20		pF
Source-Drain Diode Characteristics						
Source-drain diode forward voltage	V_{SD}	I_S = 20A, V_{GS} = 0V		0.8	1.2	V
Reverse recovery time	t_{rr}	I_F = 10A, dI/dt = 100A/µs		79		ns
Diode reverse change	Q_{rr}			106		nC

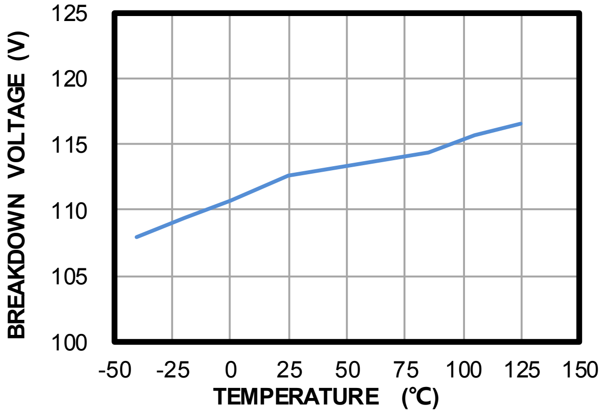
Notes:

7) Guaranteed by characterization.
8) Guaranteed by design.

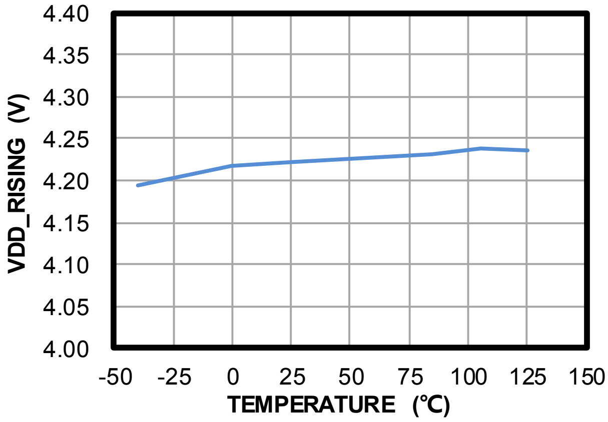
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = V_{DD_REG}, unless otherwise noted.

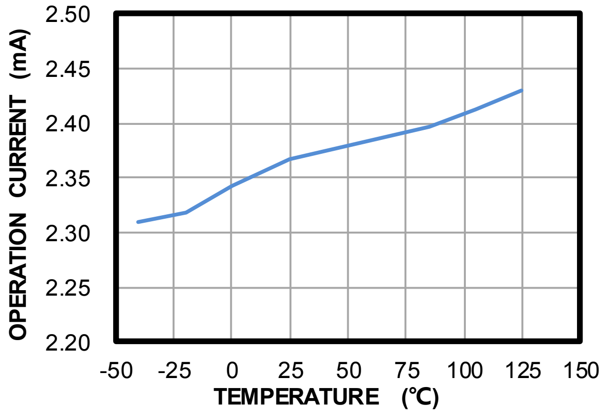
VD-VS Breakdown Voltage vs. Temperature



VDD Rising vs. Temperature

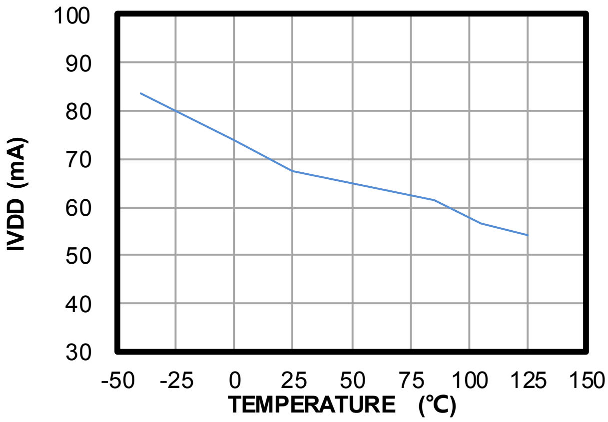


Operation Current vs. Temperature



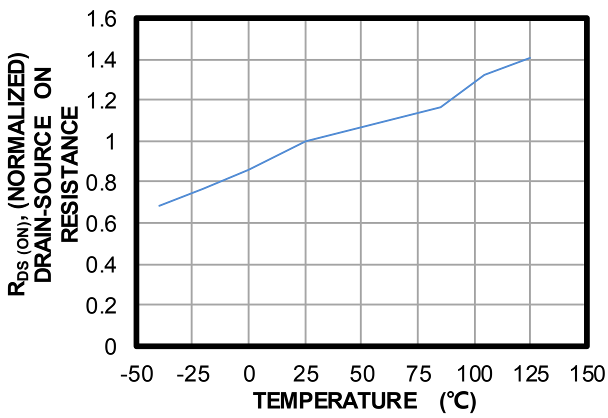
I_{VDD} Maximum Charging Current vs. Temperature

VDD = 5.5V, SENSE = 30V



$R_{DS(ON)}$ vs. Temperature

Normalized, drain-source on resistance

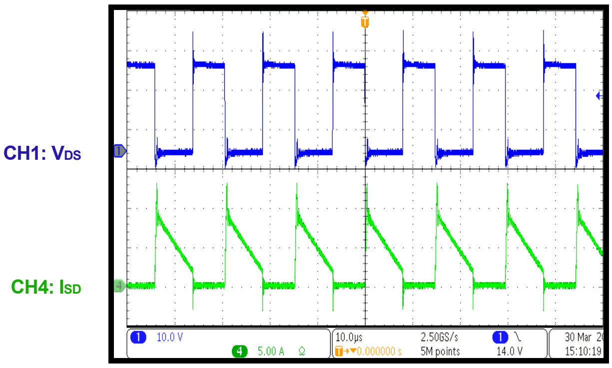


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{DD} = V_{DD_REG}, unless otherwise noted.

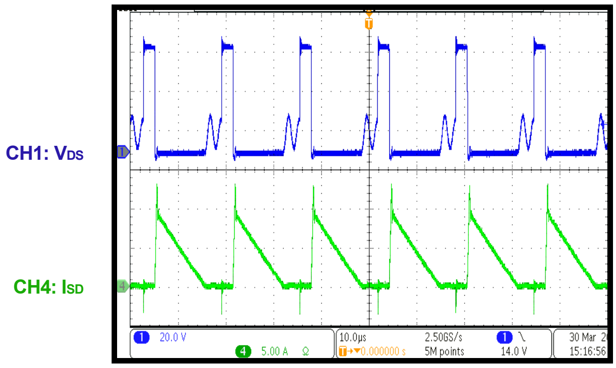
Operation in 36W Flyback Application

V_{IN} = 90V_{AC}, I_{OUT} = 3.0A



Operation in 36W Flyback Application

V_{IN} = 265V_{AC}, I_{OUT} = 3.0A



FUNCTIONAL BLOCK DIAGRAM

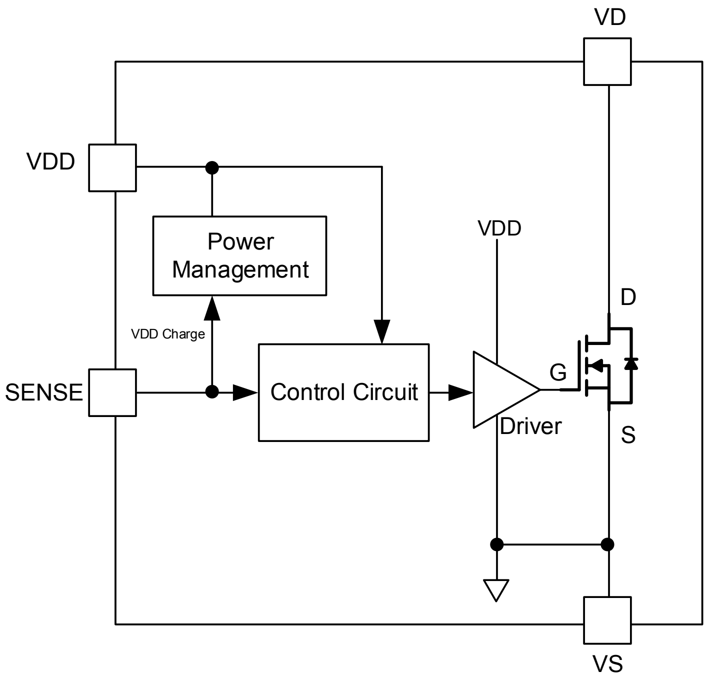


Figure 1: Functional Block Diagram

OPERATION

The MP6919 supports operation in discontinuous conduction mode (DCM), continuous conduction mode (CCM), and quasi-resonant flyback converters. The control circuitry controls the gate in forward mode, and turns the gate off when the synchronous rectification (SR) MOSFET current drops to zero.

VDD Generation

SENSE is the input for the linear regulator, the output of which is VDD. VDD supplies the MP6919, and is regulated at V_{DD_REG} (about 6.7V).

When SENSE is below 4.7V, a 40mA current source from SENSE charges up VDD. When SENSE is above 4.7V, the linear regulator's maximum charging current is limited at I_{VDD} to charge the external capacitor at VDD.

Start-Up and Under-Voltage Lockout (UVLO)

When VDD rises above 4.2V, the MP6919 exits under-voltage lockout (UVLO) and is enabled. Once VDD drops below 4.0V, the MP6919 enters sleep mode and V_{GS} is maintained low.

Turn-On Phase

When V_{DS} drops to about 2V, a turn-on timer begins. If V_{DS} reaches the -80mV turn-on threshold from 2V within the slew rate detection time (about 30ns), the MOSFET turns on after a turn-on delay, t_{DON} (about 20ns).

If V_{DS} crosses -80mV after the timer ends, the gate voltage remains off (see Figure 2). This turn-on timer prevents the device from falsely turning on due to ringing from DCM and quasi-resonant operations.

Turn-On Blanking

The control circuitry contains a blanking function. When the MOSFET turns on, the control circuit ensures that the on state lasts for a specific period of time. The turn-on blanking time is t_{B-ON} (about 1.2μs), and it prevents an accidental turn-off due to ringing. If V_{DS} reaches 1.8V within the turn-on blanking time, V_{GS} pulls low immediately.

Conduction Phase

When V_{DS} rises above the forward voltage drop, $-V_{FWD}$ (-40mV), according to the decrease of the switching current, the MP6919 lowers the gate voltage level to enlarge the on resistance of the synchronous MOSFET.

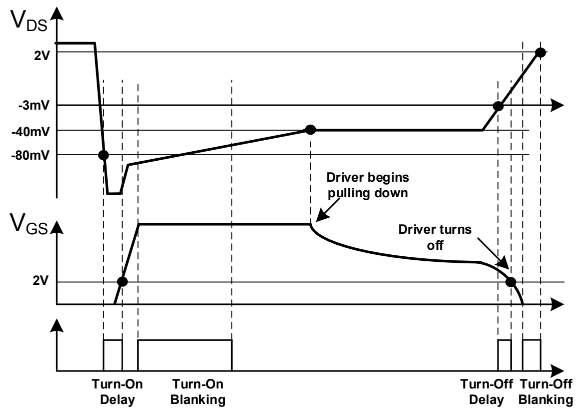


Figure 2: Turn-On/Turn-Off Timing Diagram

With this control scheme, V_{DS} adjusts to be about $-V_{FWD}$ even when the current through the MOSFET is fairly low. This function maintains the driver voltage at a very low level when the synchronous MOSFET turns off. It also boosts the turn-off speed, and is used for CCM operation.

Turn-Off Phase

When V_{DS} rises to trigger the turn-off threshold (about -3mV), the gate voltage pulls to zero after a short turn-off delay of t_{DOFF} (about 25ns) (see Figure 2).

Turn-Off Blanking

After the gate driver (V_{GS}) pulls to zero when V_{DS} reaches the turn-off threshold (-3mV), a turn-off blanking time is applied (see Figure 2). During this process, the gate driver signal latches off. Turn-off blanking is removed when V_{DS} exceeds V_{B-OFF} (about 2V).

APPLICATION INFORMATION

Slew Rate Detection Function

In DCM operations, the demagnetizing ringing may force V_{DS} below 0V. If V_{DS} reaches the turn-on threshold during the ringing, SR controllers without slew rate detection may turn on the MOSFET by mistake. This increases power loss, and may also lead to shoot-through if the primary-side MOSFET turns on within the minimum on time.

The slew rate during ringing is always lower than when the primary MOSFET is completely turned off. This false turn-on situation is prevented by the slew rate detection function. When the slew rate is below the threshold, the IC does not turn on the gate, even when V_{DS} reaches the turn-on threshold. See the Turn-On Phase section on page 8 for more details.

External Resistor on SENSE

Over-voltage conditions can damage the MP6919, and appropriate application design guarantees safe operation, especially on the high voltage pin.

One common over-voltage condition is when the body diode of the SR MOSFET turns on because the forward voltage drop exceeds the negative rating on the SENSE pin. If this occurs, it is recommended to place an external resistor between SENSE and the MOSFET drain. The recommended resistance is about 100Ω to 300Ω.

Do not use a resistor that is too large, because it may compromise the VDD supply and slow down the slew rate on the V_{DS} detection. It is not recommended to use a resistor greater than 300Ω. The resistor should be chosen based on the VDD supply and the slew rate.

Typical System Implementations

Figure 3 and Figure 4 show the typical system IC implementation in low-side rectification and high-side rectification, respectively.

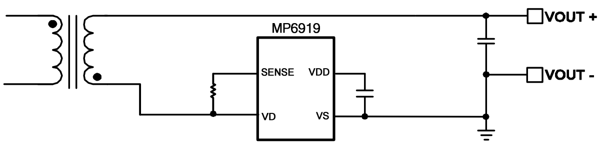


Figure 3: Low-Side Rectification

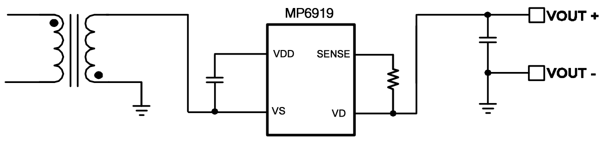


Figure 4: High-Side Rectification

Maximum Output Current

The allowed temperature rise of the MP6919 limits the maximum output current the device can handle. The temperature rise is determined by the device's power loss. For a universal input adapter, the recommended rated output current for the MP6919 is 3A. For certain designs, the power loss can be calculated to determine the maximum output current.

The MP6919 loses power due to controller consumption or integrated MOSFET conduction loss. If the MP6919 works in continuous conduction mode (CCM), reverse-recovery power loss of the integrated MOSFET must also be considered.

The power loss from controller consumption can be calculated with Equation (1):

$$P_{LOSS\_Controller} = V_{SENSE\_P} \times I_{DD} \quad (1)$$

Where I_{DD} is the MP6919's current, and V_{SENSE_P} is the corresponding plateau voltage on the SENSE pin when the primary side MOSFET turns on.

The power loss from integrated MOSFET conduction loss can be estimated with Equation (2):

$$P_{LOSS\_SR\_Conduction} = \frac{1}{t_{s\_on}} \times \int_0^{t_{s\_on}} V_{SR\_SD}(t) \times I_{SR\_SD}(t)dt \quad (2)$$

Where t_{s_on} is the SR on period, V_{SR_SD} is the voltage drop from the SR, and I_{SR_SD} is the current flowing through the SR.

The power loss during reverse-recovery can be calculated with Equation (3):

$$P_{LOSS\_SR\_RR} = \frac{1}{2} \times V_{DS} \times I_{rr} \times t_{rr} \times f_{sw} \quad (3)$$

Where I_{rr} is the peak reverse current, and t_{rr} is reverse-recovery time.

The total loss of the MP6919 (P_{LOSS}) is the sum of the above losses. When using an RC snubber, be sure to also consider the power loss caused by the snubber.

The junction and case temperature rises can be calculated with the junction-to-ambient (θ_{JA}) thermal resistance and junction-to-case (θ_{JC}) thermal resistance. The junction temperature must be within ABS (typically 150°C). ΔT_{JA} can be calculated with Equation (4):

$$\Delta T_{JA} = P_{LOSS} \times \theta_{JA} \quad (4)$$

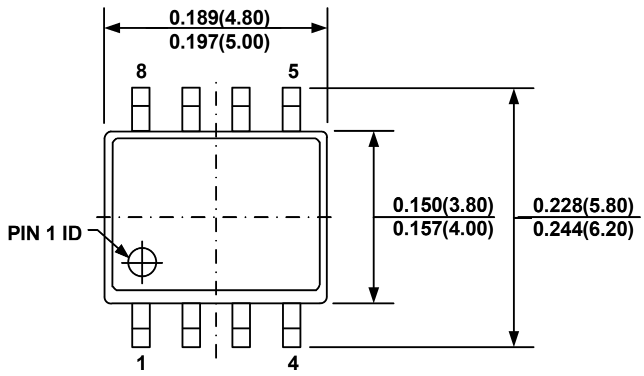
ΔT_{JC} can be estimated with Equation (5):

$$\Delta T_{JC} = P_{LOSS} \times \theta_{JC} \quad (5)$$

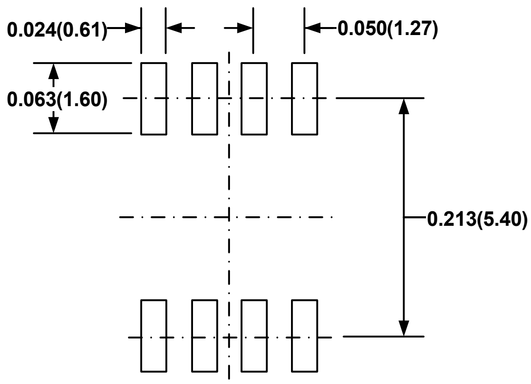
Reduce thermal resistance by adding a thicker copper layer, placing more thermal dissipation vias, and adopting a heatsink. The maximum output current can be set by combining the real tested data.

PACKAGE INFORMATION

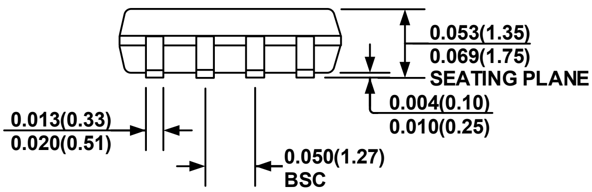
SOIC-8



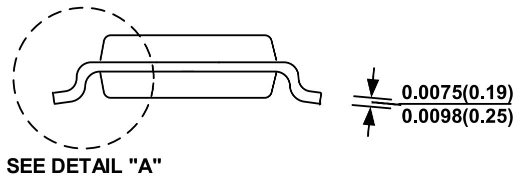
TOP VIEW



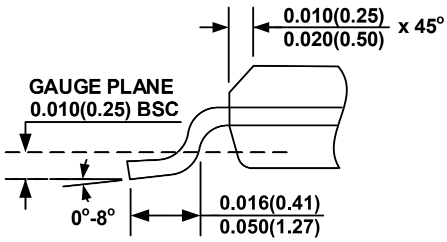
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.