MP8124

500mA LNB Power Supply and Control Regulator

The Future of Analog IC Technology

DESCRIPTION

The MP8124 is a highly integrated voltage regulator designed to provide efficient, low-noise power and interface signals to the low-noise block (LNB) of a satellite receiver. It provides a 22kHz tone signal output, which is compatible with DiSEqC 1.x.

The MP8124 integrates a current-mode boost regulator followed by a tracking linear regulator. Also, it has output voltage selection and a 22kHz tone shaper from an external signal. The boost regulator provides a clean power source, which is 1V higher than the final output voltage while the tracking linear regulator protects the output against overloads and shorts.

Full protection features include over-current protection (OCP), short-circuit protection (SCP), boost over-voltage protection (OVP), and over-temperature protection (OTP), offering a simple solution with a low component count and high efficiency.

The MP8124 is available in a 14-pin QFN (2mmx3mm) package.

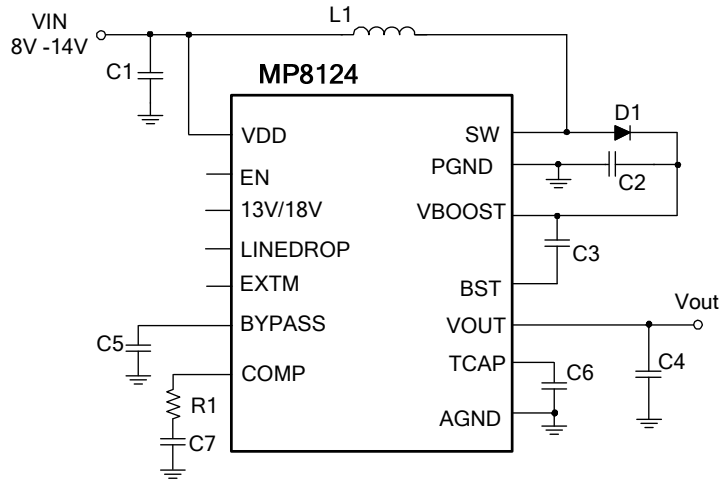
FEATURES

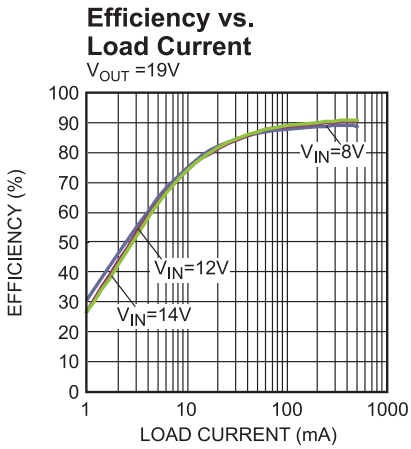
- Compatible with DiSEqC 1.x
- 600mA Accurate Current Limit
- 8V to 14V Input Voltage
- 40V V_{OUT} Rating
- Low-Noise LDO Output
- High Efficiency at Light Load: >85% at a 40mA Load
- High Frequency for Small Component Sizes
- Built-In 22kHz Signal Shaper
- Selectable Output Voltage
- Over-Current Protection (OCP) Short-Circuit Protection (SCP)
- Boost Over-Voltage Protection (OVP)
- Over-Temperature Protection (OTP)
- Available in a QFN-14 (2mmx3mm) Package

APPLICATIONS

- LNB Power Supply and Control for Satellite Set-Top Boxes
- TV Satellite Receivers
- PC Card Satellite Receivers

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP8124GD	QFN-14 (2mmx3mm)	*See Below*

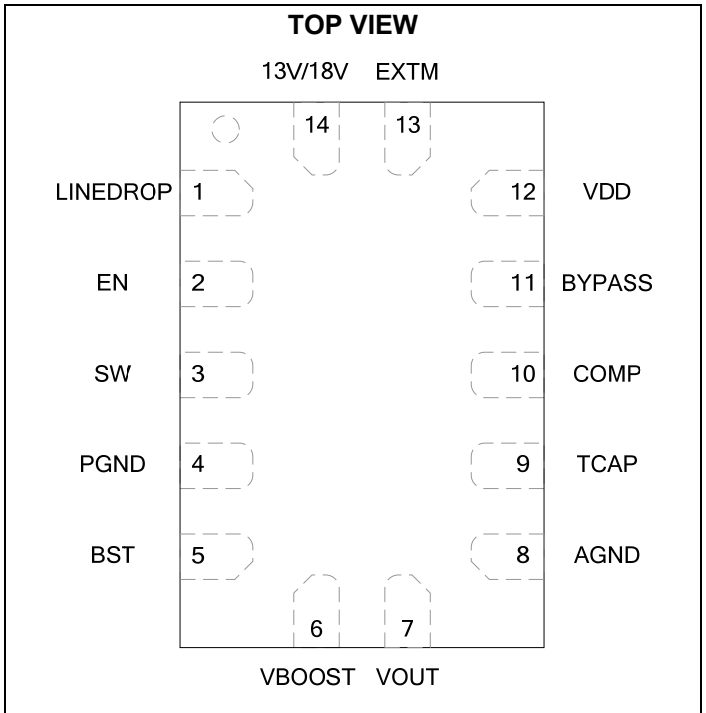
*For Tape & Reel, add suffix –Z (e.g. MP8124GD–Z)

TOP MARKING

AMMY
LLL

AMM: Product code of MP8124GD
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



QFN-14 (2mmx3mm)

ABSOLUTE MAXIMUM RATINGS (1)

VDD .....-0.3V to 20V
VOUT, SW, VBOOST….....-0.3V to 40V
BST.....V_{BOOST} + 6.5V
All other pins .....-0.3V to 6.5 V
Continuous power dissipation (T_A = +25°C) (2)
..... 1.78W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....8V to 14V
Operating junction temp. (T_J)... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-14 (2mmx3mm) ……...…..70.....15....°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 3.3V, T_J = -40°C to 125°C. Typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
General						
Input voltage range	V_{IN}		8	12	14	V
Shutdown current	I_{SD}	EN = low			15	μA
Input supply current(5)	I_{IN}	EN = high, V_{OUT} = 19V, no load EXTM = 0		4		mA
		EN = high, V_{OUT} = 19V, no load EXTM = 22kHz		12		mA
Under-voltage lockout	UVLO	V_{IN} rising	6.8	7.25	7.7	V
UVLO hysteresis				350		mV
Voltage on BYPASS	V_{BYP}	I_{LOAD} = 0mA - 10mA	4.5	5	5.5	V
Over-temperature shutdown(5)				160		°C
Over-temperature protection hysteresis(5)				20		°C
Boost Regulator						
Boost switch-on resistance	R_{DSON}	I_{SW} = 500mA		120		mΩ
Boost MOSFET switching current limit		Duty = 60%	3	3.75	4.5	A
Boost frequency	Fs	T_J = 25°C	390	440	490	kHz
		T_J = -40°C to 125°C	360	440	520	
Linear Regulator						
Dropout voltage	V_{DROP}	V_{BOOST} - V_{OUT}, I_{OUT} = 50mA		1		V
Output voltage accuracy	V_{OUT}	V_{OUT} = 13V/14V/18V/19V, I_{OUT} = 10mA	-2.5		+2.5	%
Output line regulation(5)		8V ≤ V_{IN} ≤ 14V, I_{OUT} = 500mA		10		mV
Output load regulation(5)		0mA ≤ I_{OUT} ≤ 500mA, V_{OUT} = 13V		10		mV
		0mA ≤ I_{OUT} ≤ 500mA, V_{OUT} = 18V		25		mV
Output current limit	I_{LIMIT}		530	600	670	mA
Dynamic overload protection off time	T_{OFF}	Time of attempt to restart		1.9		s
Dynamic overload protection on time	T_{ON}	Time to onset of shutdown		50		ms
TCAP current	I_{CHA}	TCAP capacitor charging, T_J = 25°C	5	6.8	8.5	μA
		T_J = -40°C to 125°C	4.5	6.8	9	
Output backward leakage current(6)	I_{BKLK}	EN = low, V_{OUT} is clamped to 24V, VBOOST floats		0.8	1.5	mA
LDO output sink current	I_{SINK}	V_{OUT} = 18V, EXTM = 22kHz, clamp V_{OUT} to 19V		45		mA
		V_{OUT} = 18V, EXTM = 0V, clamp V_{OUT} to 19V		7		mA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 3.3V, T_J = -40°C to 125°C. Typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
LDO sink current protection on time[5]	T_{SINK_ON}	V_{OUT} = 18V, EXTM = 22kHz, clamp V_{OUT} to 19V		9		ms
		V_{OUT} = 18V, EXTM = 0V, clamp V_{OUT} to 19V		9		ms
LDO sink current protection off time[5]	T_{SINK_OFF}	V_{OUT} = 18V, EXTM = 22kHz, clamp V_{OUT} to 19V		450		ms
		V_{OUT} = 18V, EXTM = 0V, clamp V_{OUT} to 19V		450		ms
Tone Signal						
External tone source frequency range[7]		V_{EXTM-H} = 3.3V, V_{EXTM-L} = 0V, duty = 50%	20	22	24	kHz
Peak-to-peak amplitude	V_{PP}	I_{OUT} = 0 to 500mA	0.45	0.65	0.85	V
Duty cycle		R_{LOAD} = 1kΩ, C_{LOAD} = 0.1μF	40	50	60	%
Rise and fall time		R_{LOAD} = 1kΩ, C_{LOAD} = 0.1μF	5	10	15	μs
Logic Interface[8] (EN, LINEDROP, 13V/18V, EXTM)						
Input logic low voltage	VLI				0.8	V
Input logic high voltage	VHI		2			V
Logic input current		Connect to 5V or 0V	-10		10	μA

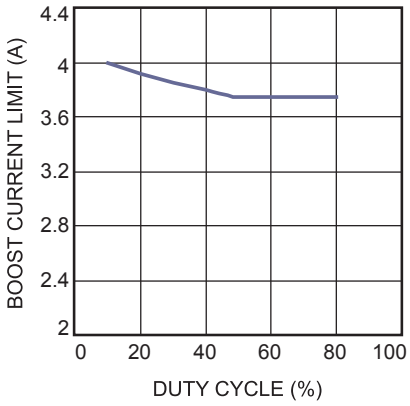
NOTES:

5) Guaranteed by characterization test, not tested in production.
6) Can withstand the back voltage for an indefinite period of time. Once the fault condition is removed, the device resumes normal operation.
7) The input tone signal source must be limited in this range to guarantee EXTM function.
8) The input voltage connected to these logic pins should be limited below the absolute maximum ratings and cannot be pulled directly up to a high voltage through one pull-up resistor. For default high-level input connection, pull LINEDROP and 13V/18V to the BYPASS voltage and pull EN to VIN through the resistor divider. Refer to Figure 4 on page 20 for connection details.

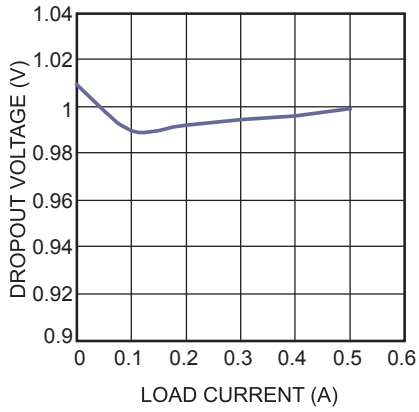
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 19V, L = 10µH, T_A = 25°C, unless otherwise noted.

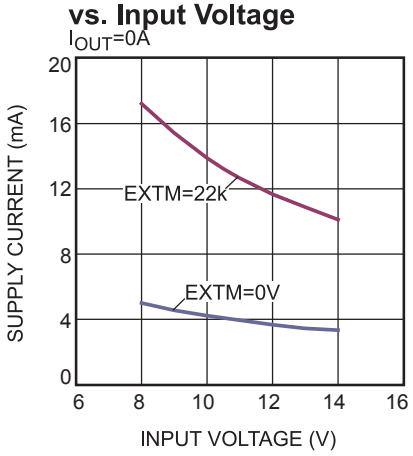
Boost Current Limit vs. Duty



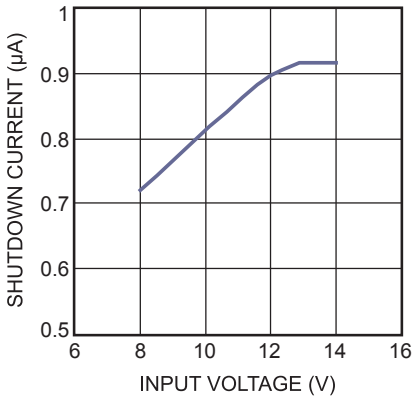
LDO Dropout Voltage vs. Load Current



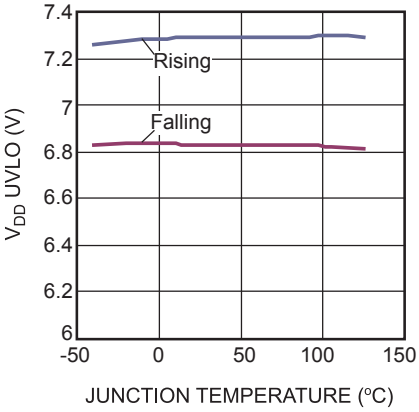
Supply Current vs. Input Voltage



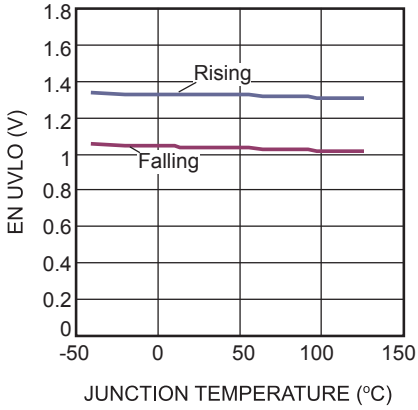
Shutdown Current vs. Input Voltage



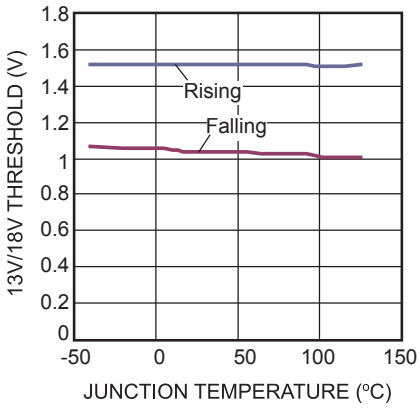
V_{DD} UVLO vs. Junction Temperature



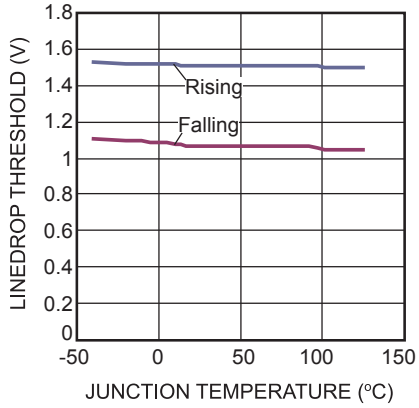
EN UVLO vs. Junction Temperature



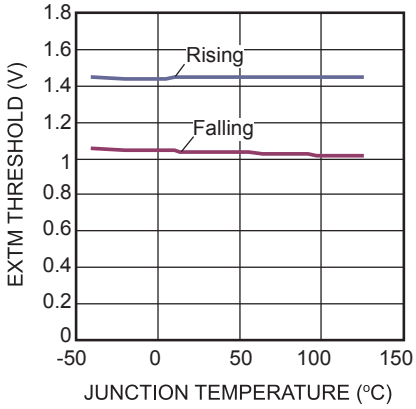
13V/18V Threshold vs. Junction Temperature



Linedrop Threshold vs. Junction Temperature



EXTM Threshold vs. Junction Temperature

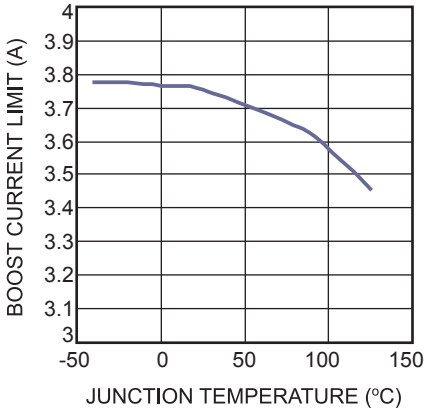


TYPICAL CHARACTERISTICS *(continued)*

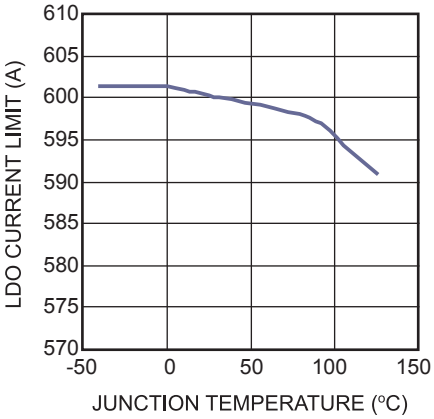
V_{IN} = 12V, V_{OUT} = 19V, L = 10µH, T_A = 25°C, unless otherwise noted.

Boost Current Limit vs. Junction Temperature

Duty=60%

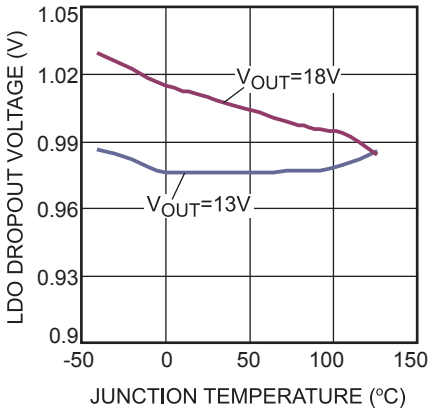


LDO Current Limit vs. Junction Temperature

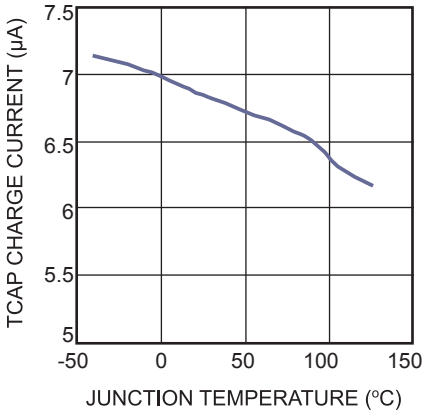


LDO Dropout Voltage vs. Junction Temperature

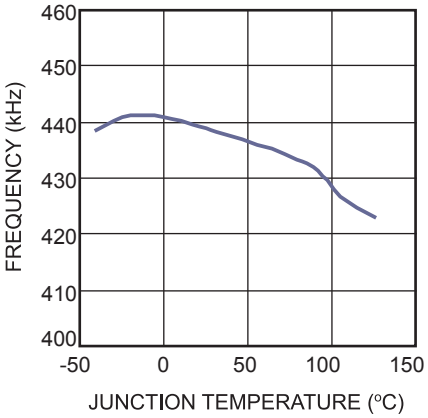
I_{OUT}=50mA



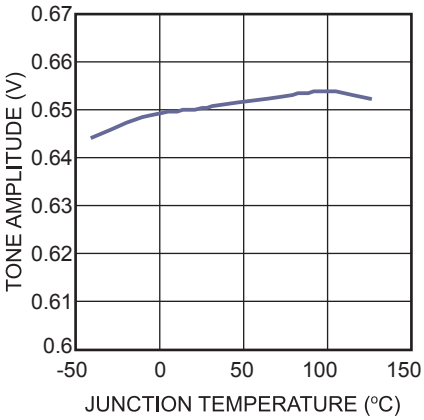
TCAP Charge Current vs. Junction Temperature



Frequency vs. Junction Temperature



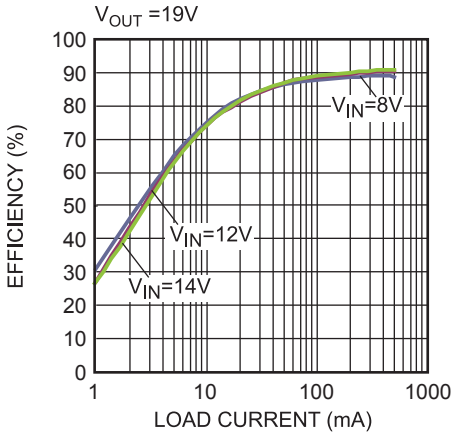
Tone Amplitude vs. Junction Temperature



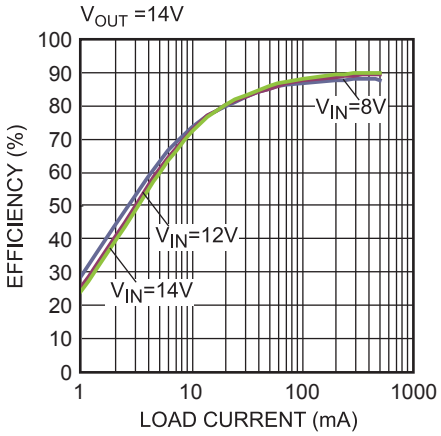
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 19V, L = 10µH, C_{OUT} = 0.1µF, T_A = 25°C, unless otherwise noted.

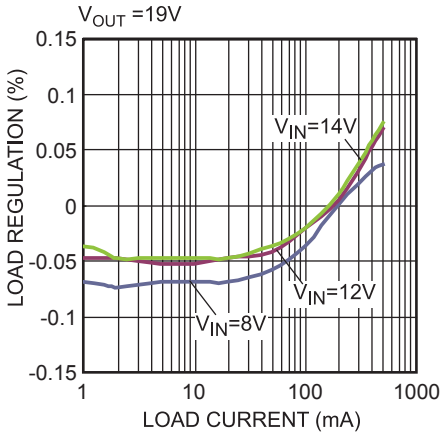
Efficiency vs. Load Current



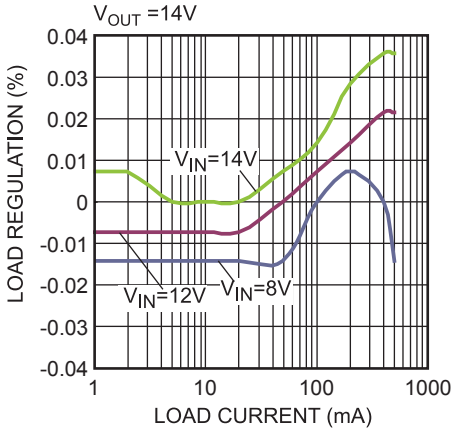
Efficiency vs. Load Current



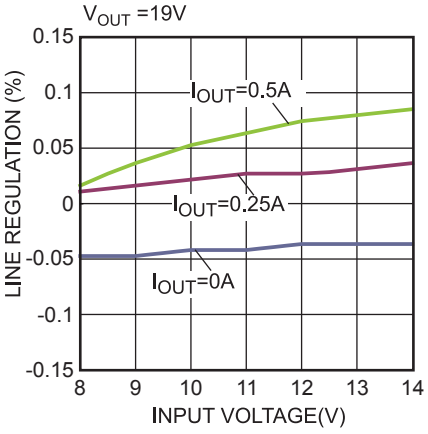
Load Regulation



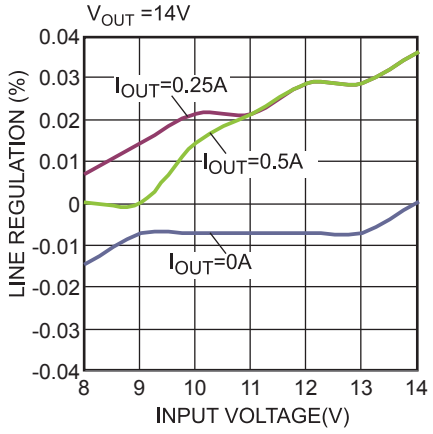
Load Regulation



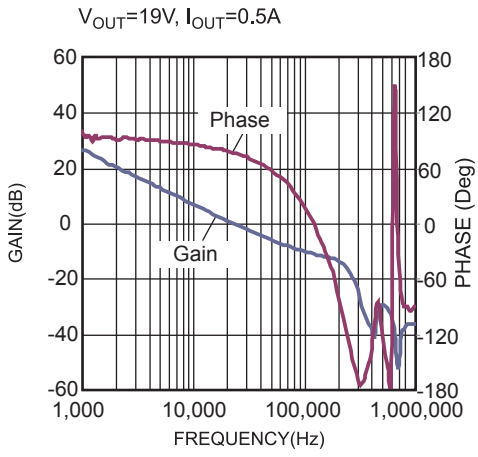
Line Regulation



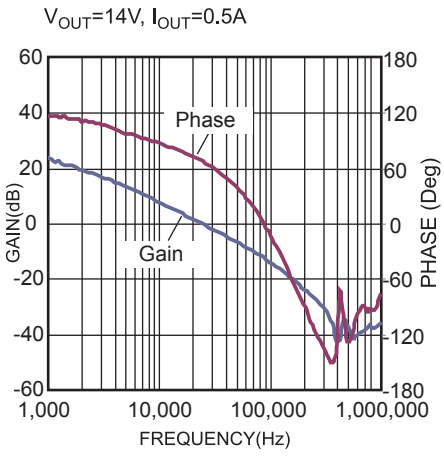
Line Regulation



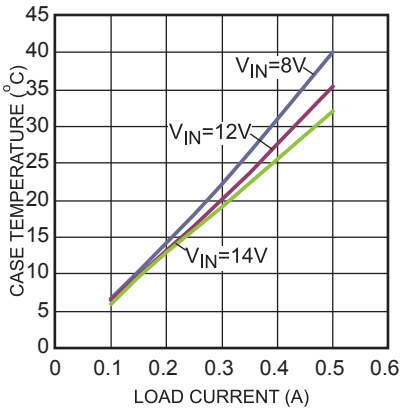
Bode Plot



Bode Plot



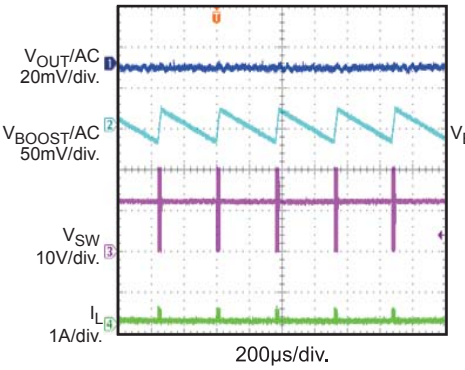
Case Temperature Rise vs. Load Current



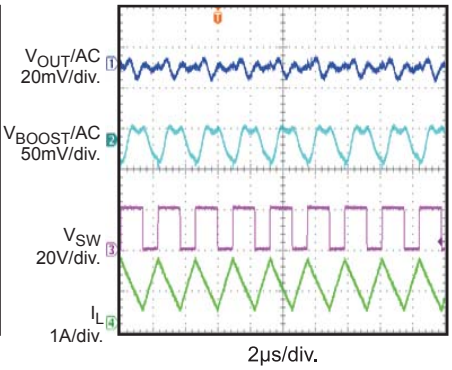
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 19V, L = 10µH, C_{OUT} = 0.1µF, T_A = 25°C, unless otherwise noted.

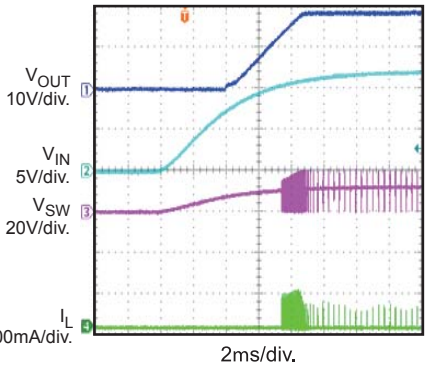
Steady State
I_{OUT} = 0A



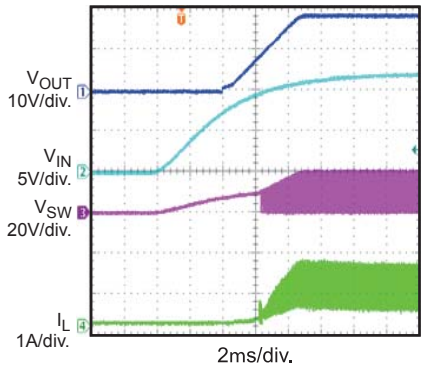
Steady State
I_{OUT} = 0.5A



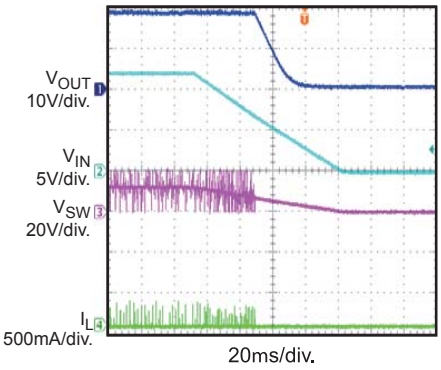
V_{IN} Start-Up
I_{OUT} = 0A



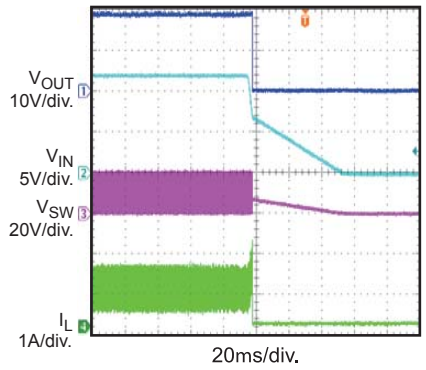
V_{IN} Start-Up
I_{OUT} = 0.5A



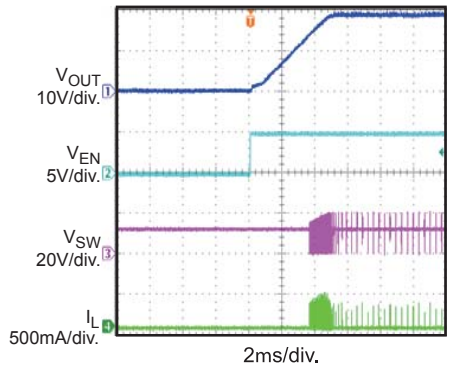
V_{IN} Shutdown
I_{OUT} = 0A



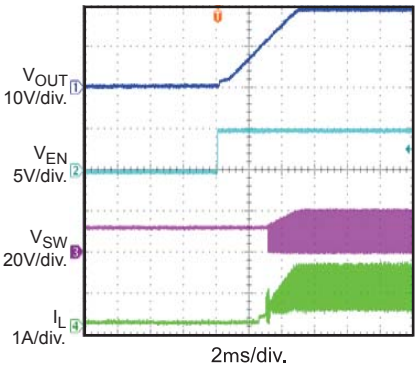
V_{IN} Shutdown
I_{OUT} = 0.5A



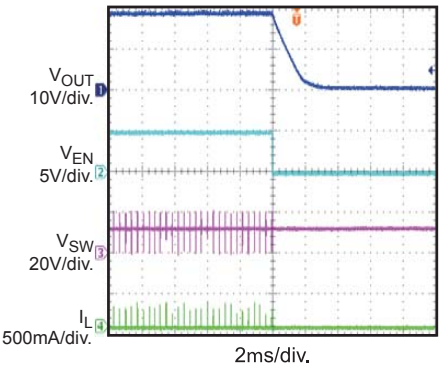
EN Start-Up
I_{OUT} = 0A



EN Start-Up
I_{OUT} = 0.5A



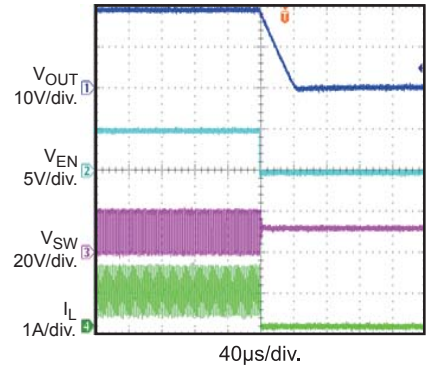
EN Shutdown
I_{OUT} = 0A



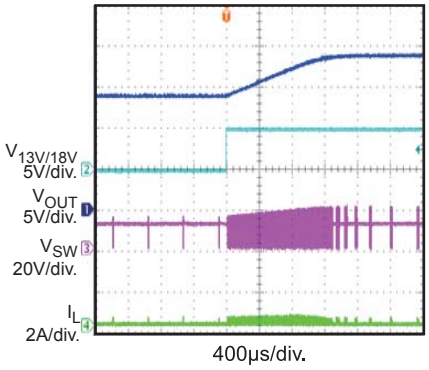
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 19V, L = 10µH, C_{OUT} = 0.1µF, T_A = 25°C, unless otherwise noted.

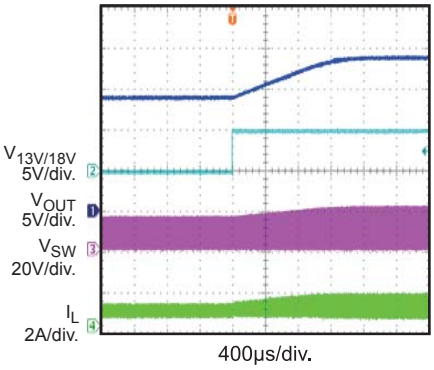
EN Shutdown
I_{OUT} = 0.5A



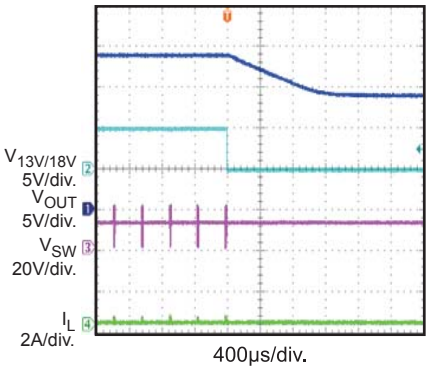
14V to 19V Switching
I_{OUT} = 0A



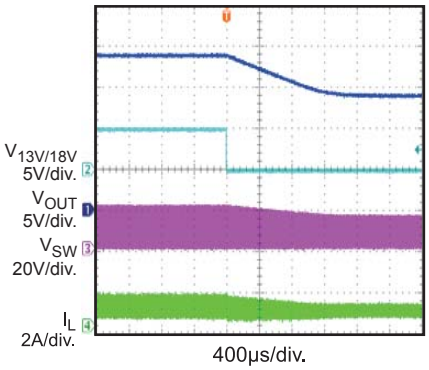
14V to 19V Switching
I_{OUT} = 0.5A



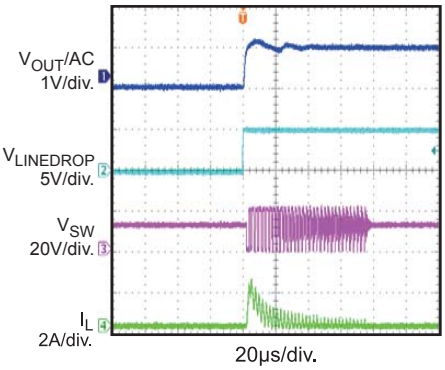
19V to 14V Switching
I_{OUT} = 0A



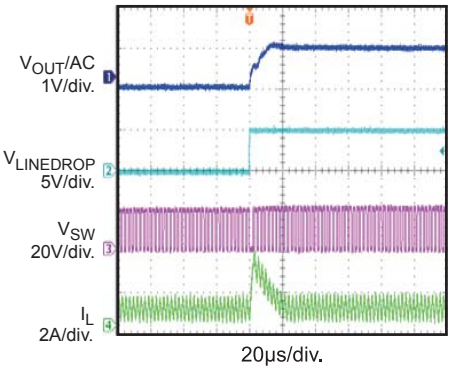
19V to 14V Switching
I_{OUT} = 0.5A



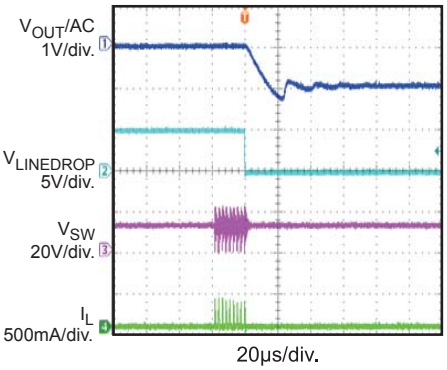
18V to 19V Switching
I_{OUT} = 0A



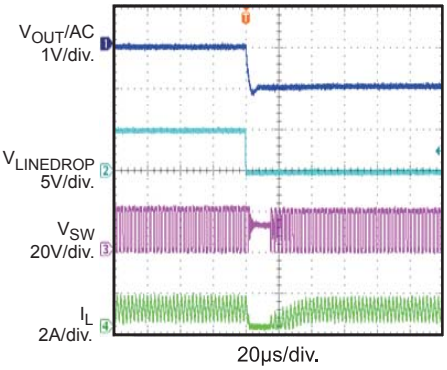
18V to 19V Switching
I_{OUT} = 0.5A



19V to 18V Switching
I_{OUT} = 0A



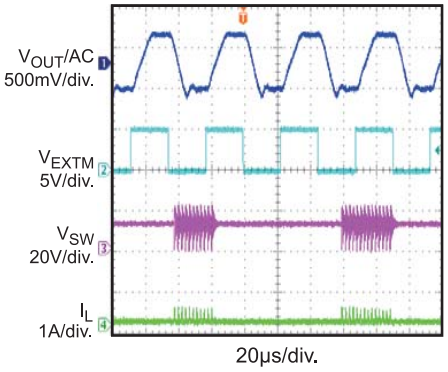
19V to 18V Switching
I_{OUT} = 0.5A



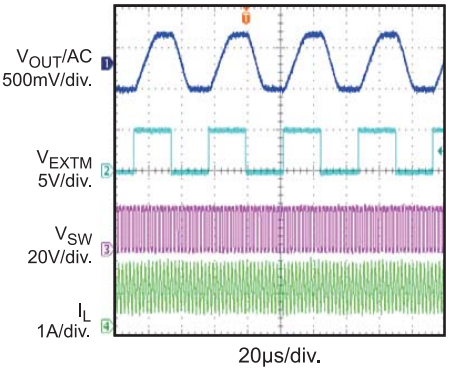
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 19V, L = 10µH, C_{OUT} = 0.1µF, T_A = 25°C, unless otherwise noted.

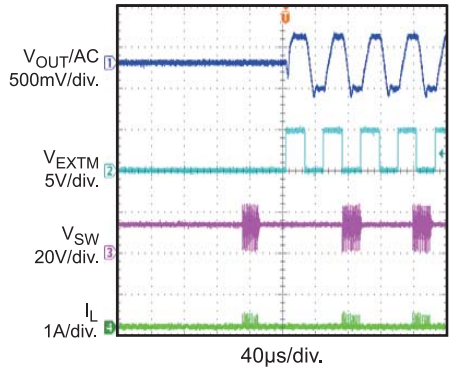
Tone Steady State
I_{OUT} = 0A



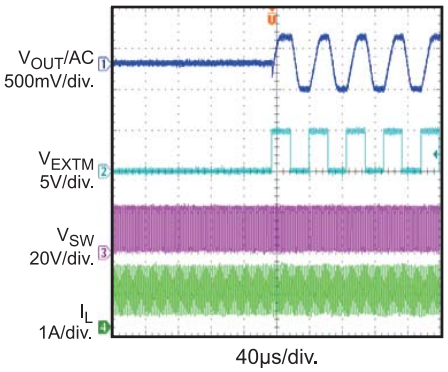
Tone Steady State
I_{OUT} = 0.5A



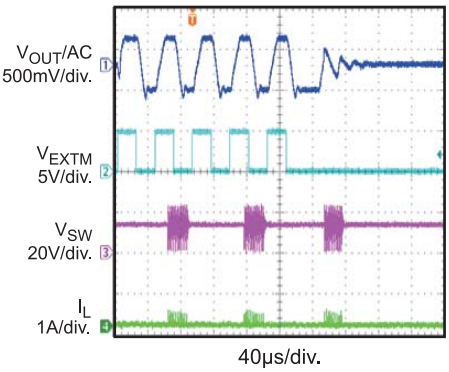
Tone Entry
I_{OUT} = 0A



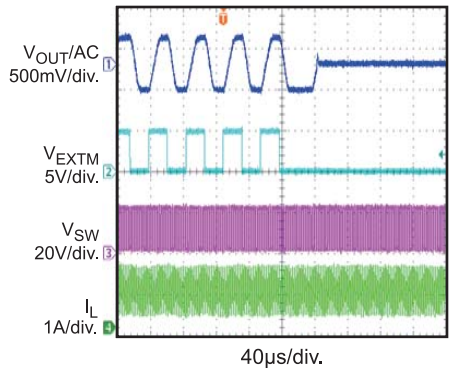
Tone Entry
I_{OUT} = 0.5A



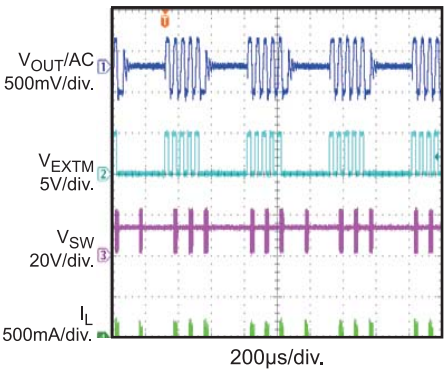
Tone Exit
I_{OUT} = 0A



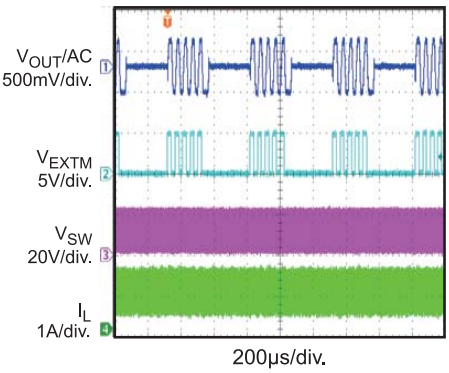
Tone Exit
I_{OUT} = 0.5A



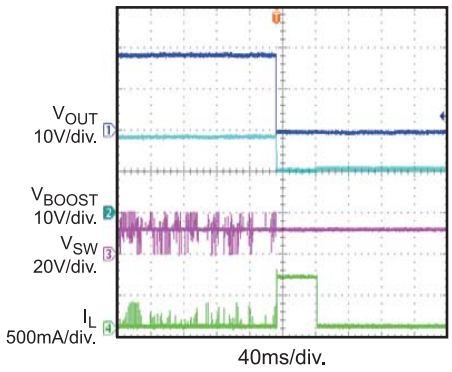
Tone Burst
I_{OUT} = 0A



Tone Burst
I_{OUT} = 0.5A



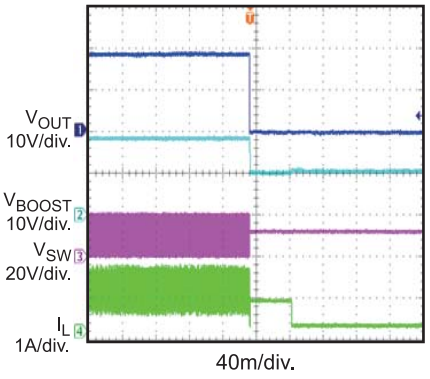
SCP Entry
I_{OUT} = 0A to Short



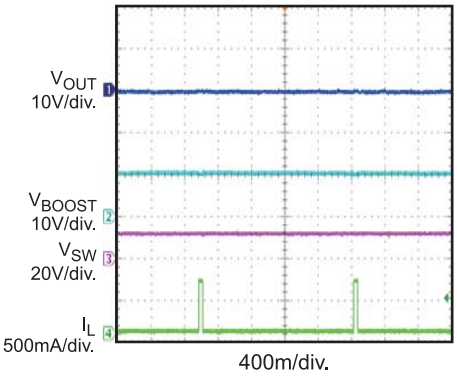
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 19V, L = 10µH, C_{OUT} = 0.1µF, T_A = 25°C, unless otherwise noted.

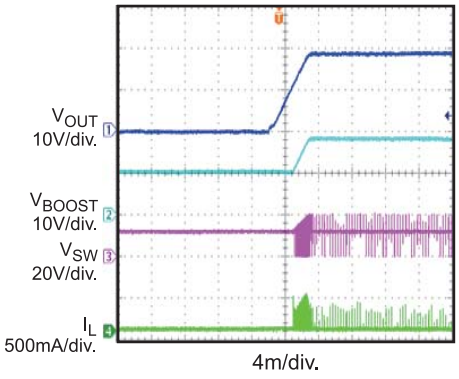
SCP Entry
I_{OUT} = 0.5A to Short



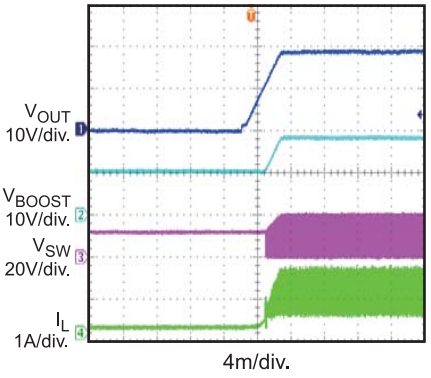
SCP Steady State
V_{OUT} Short



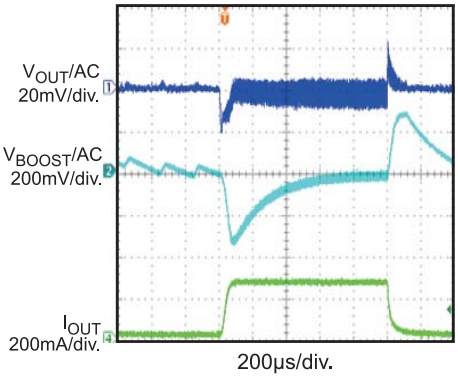
SCP Recovery
I_{OUT} = Short to 0A



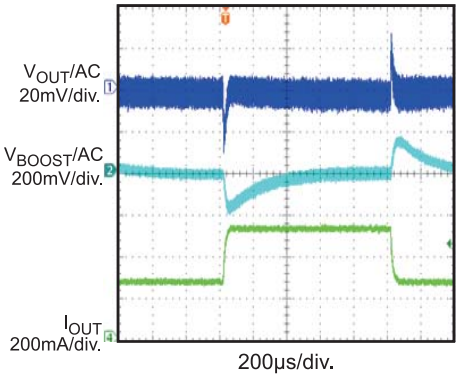
SCP Recovery
I_{OUT} = Short to 0.5A



Load Transient
I_{OUT} = 0A to 0.25A



Load Transient
I_{OUT} = 0.25A to 0.5A



PIN FUNCTIONS

Pin #	Name	Description
1	LINEDROP	**LINEDROP provides a selectable V_{OUT} compensation for the voltage drop on the long coaxial cable.** When LINEDROP is high, the LDO output increases by 1V. LINEDROP cannot be left floating. Pull it to the BYPASS voltage for automatic 1V voltage compensation after start-up.
2	EN	**Regulator on/off control input.** Apply a high level at EN to turn on the regulator; apply a low level at EN to turn off the regulator. Connect EN to the input source through a resistor divider for automatic start-up. Do NOT leave EN floating.
3	SW	**Power switch output.** SW is the drain of the internal MOSFET switch of the boost stage. Connect the power inductor and output rectifier to SW.
4	PGND	**Power ground.**
5	BST	**Internal LDO driver supply.**
6	VBOOST	**Internal LDO power input.**
7	VOUT	**Output voltage.**
8	AGND	**Analog ground.**
9	TCAP	**Soft start.** Connect a capacitor from TCAP to ground to set a rise time for the output voltage. The TCAP voltage is the feedback reference voltage and should be placed far away from the noise source.
10	COMP	**Compensation for the boost regulator.**
11	BYPASS	**Power bias for internal circuit.** Connect a 0.22μF bypass capacitor for the internal regulator.
12	VDD	**Input power supply.**
13	EXTM	**External modulation input for 22kHz tone signal.** EXTM is shaped inside the MP8124 and transferred onto the output. Tie EXTM to ground if not used.
14	13V/18V	**Select 13V or 18V as the output voltage.** Use 18V for high levels and 13V for low levels. Do NOT leave 13V/18V floating. Pull 13V/18V to the BYPASS voltage for an automatic 18V output after start-up.

FUNCTIONAL BLOCK DIAGRAM

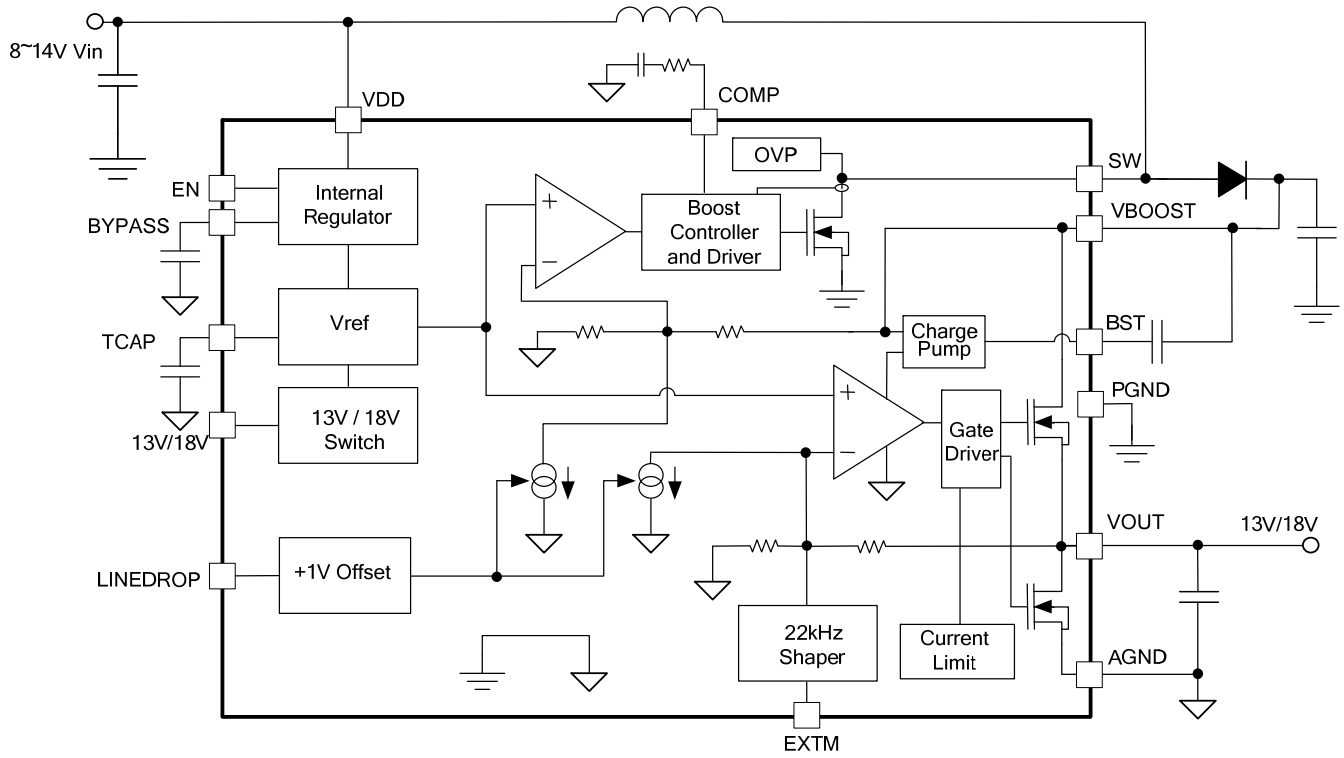


Figure 1: Functional Block Diagram

OPERATION

The MP8124 is a single-output voltage regulator that provides both a supply voltage and a control signal from satellite set-top box modules to the low-noise block (LNB) of the antenna port.

The MP8124 uses an integrated boost converter between 8V and 14V from a single supply source. It generates the voltage to enable the linear regulator to work at minimum dissipated power.

Boost Converter/Linear Regulator

The boost converter is a fixed-frequency, non-synchronous voltage regulator with peak-current-mode control. The operating frequency is 440kHz typically.

To reduce power dissipation, the boost converter operates in a pulse-skipping mode at light load. The output voltage of the boost converter tracks the requested output to allow the linear regulator to work with minimum drop-out voltage.

13V/18V Switching

The output voltage can be set to 13V or 18V to select different polarization directions of the LNB. A logic high level on 13V/18V sets the output to 18V; a low level sets it to 13V. Pull 13V/18V up to BYPASS for a default 18V output during start-up.

LINEDROP Control

To compensate for the excess voltage drop along the coaxial cable, the MP8124 employs a voltage compensation function. If LINEDROP is set at a high level, the output voltage can be increased by 1V. A low level disables the function. Pull LINEDROP to BYPASS for a default 1V compensation.

Output Slew Rate Control

The MP8124 integrates a soft-start function to reduce the inrush current during start-up. A soft start is implemented via the external capacitor (C_{TCAP}) at TCAP. When V_{OUT} = 13V or 18V with the required output voltage rising time (T_{RISE}), the value of C_{TCAP} can be estimated using Equation (1):

$$C_{TCAP} = \frac{(13.5 \times I_{CHA} \times T_{RISE})}{V_{OUT}} \quad (1)$$

Where I_{CHA} is 6.8μA, typically.

For V_{OUT} = 14V/19V, the rising time is the same as V_{OUT} = 13V/18V; however, V_{OUT} increases by 1V immediately after the IC is enabled, and it is then controlled by the TCAP voltage.

The output voltage rising and falling times are also controlled by the soft-start circuit during the 13V/18V transient.

Current Limit

The output current is limited to about 600mA. When an overload or a short circuit is detected, the output current is regulated at the current limit level for 50ms. If the overload is still detected after this time period, the output shuts down for 1.9 seconds before it resumes. If an overload occurs, the window is registered and lasts for 30μs. If another overload is detected within this 30μs window, another 30μs window begins. This detection mode ensures that OCP hiccup mode occurs in the event of a high oscillatory current.

The boost converter integrates a cycle-by-cycle over-current limit function that supports the part in a full load.

Boost Over-Voltage Protection (OVP)

The MP8124 features an over-voltage protection (OVP) circuit on SW. If VBOOST is disconnected on the board, the boost output voltage cannot feed back to the boost control circuit, and the boost output voltage runs away. A typical 32V OVP circuit on SW shuts down the MP8124 to prevent damage to the IC once the over-voltage condition is detected. A blanking time in the detection circuit is added to avoid mistriggering OVP by the SW spike voltage. Once the MP8124 experiences OVP, the part cannot restart until power is applied at VIN or the EN input.

Tone Generation

In accordance with DiSEqC 1.x standards, the part can detect a 22kHz signal through EXTM, shape it with the built-in amplitudes and rise and fall times, and modulate the output (see Figure 2).

The external tone source on EXTM should be within the 20kHz to 24kHz range to meet DiSEqC 1.x standards. The MP8124 responds to the tone rising and returns to a normal voltage if there is no signal input from EXTM after about 40μs. Tie EXTM to GND if the 22kHz signal is not needed.

The 22kHz tone signal is shaped on VOUT by the linear regulator. The MP8124 is able to provide an optimal tone signal, even when there is no load on VOUT.

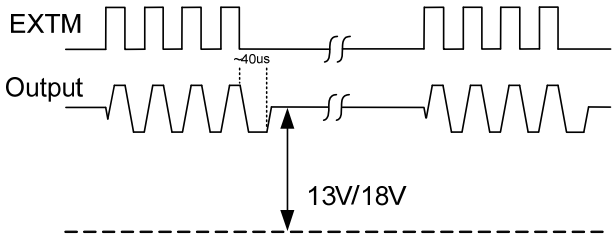


Figure 2: Tone Signal on Output

LDO Pull-Down Current and Protection

VOUT sinks the current when the output is higher than the set voltage, so the voltage transient from 18V to 13V or the 22kHz tone signal works well, even though there is no load current on the output. To prevent power loss and thermal issues caused by the sink current when the output is biased to a higher voltage, a timer with a typical 9ms period is enabled when the sink current triggers the sink current limit. If the LDO sink current limit signal still remains after 9ms, the sink current circuit is turned off. The sink current circuit is enabled again after a delay of about 450ms and continues monitoring the sink over-current condition.

The LDO has different sink current capabilities based on whether the tone is available or not.

Thermal Protection

When the junction temperature exceeds +160°C, the part shuts down. Once the junction temperature drops below 140°C, the part restarts automatically.

APPLICATION INFORMATION

Selecting the Input Capacitor

The input capacitor (C1) is used to maintain the DC input voltage. Low ESR ceramic capacitors with 10μF X7R dielectrics are recommended. The input voltage ripple can be estimated with Equation (2):

$$\Delta V_{IN} = \frac{V_{IN}}{8f_s^2 \cdot L \cdot C1} \cdot \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \quad (2)$$

Where f_S is the boost switching frequency and L is the boost inductor value.

Setting the Boost Output Capacitor

The output current to the boost converter is discontinuous, and therefore requires an output capacitor (C2) to supply AC current to the load. For best performance, low ESR capacitors are recommended. The output voltage ripple can be estimated with Equation (3):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \cdot R_L \cdot C2} \cdot \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \quad (3)$$

Where R_L is the value of the load resistor.

Ceramic capacitors with X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. Typically, two-piece 10μF X7R ceramic capacitors are recommended. Place one close to the boost switching loop and the other close to the LDO input.

Tantalum or low ESR electrolytic capacitors are also sufficient for the boost output. In this condition, it is recommended to place two small ceramic capacitors (0.1μF or higher) close to both the boost-switching loop output and the LDO input. When using electrolytic capacitors, ESRs that are too high may introduce more voltage ripple on the boost output. Additional filters may be necessary to minimize the ripple.

Selecting the Inductor of the Boost Converter

An inductor is required to transfer the energy between the input source and the boost output capacitors. An inductor with a larger value results in less ripple current and a lower peak inductor current, and therefore it reduces the stress on the power MOSFET. However, the larger value inductor has a larger physical size, a higher series resistance, and a lower saturation current.

For most designs, the inductance value can be calculated with Equation (4):

$$L = \frac{V_{IN}(V_{OUT} - V_{IN})}{f_s \cdot V_{OUT} \cdot \Delta I_L} \quad (4)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30%~50% of the maximum inductor peak current. Typically, a 10μH inductor is recommended. Ensure that the inductor does not saturate under a worst-case load transient condition. The inductor should have a low series resistance (DCR) to reduce the resistive power loss.

Selecting the Rectifier Diode of the Boost Converter

The high switching frequency demands high-speed rectifiers. Schottky diodes are recommended for most applications because of their fast recovery times and low forward voltage. Typically, a 2A or 3A high efficiency Schottky diode is recommended for the boost converter; the diode voltage rating should be higher than the output voltage. A higher rating may be needed based on other protections, such as surge protection.

LDO Output Capacitor and Diode

To permit transport of the 22kHz tone signal, a 0.1μF output capacitor is recommended for the LDO regulator. A capacitance that is too high may affect the 22kHz signal shape, and a capacitance that is too low may lead to LDO instability.

For the OCP or SCP conditions on the far end of the bus line (cable), the MP8124 shuts down for protection, and VOUT may drop to a negative voltage due to the long cable parasitic inductance. One low-voltage drop Schottky diode (i.e., 1N5819 or better) placed between VOUT and GND is recommended to clamp the negative voltage.

Soft-Start (SS) Capacitor Setting

With the required output voltage rising time (T_{RISE}), the value of C_{TCAP} can be calculated using Equation (5):

$$C_{TCAP} = \frac{(13.5 \times I_{CHA} \times T_{RISE})}{V_{OUT}} \quad (5)$$

Where I_{CHA} is the charging current, typically 6.8μA.

The TCAP soft-start capacitor also controls the voltage transient slew rate between 13V and 18V.

TCAP is the feedback reference voltage of the boost and LDO output. One small capacitor is necessary to decouple TCAP. Typically, a 22nF capacitor is recommended to control the soft start and decouple the reference voltage.

Compensation Circuits Setting for the Boost Converter

The output of the transconductance error amplifier (COMP) is used to compensate the regulation control system. R1 and C7 in series compensate the feedback loop gain and phase. Typically, R1 = 60.4kΩ and C7 = 3.3nF is recommended for the ceramic output condition. Please refer to Figure 4 on page 20 for details.

If the electrolytic capacitor is used to replace the ceramic capacitor at the boost's output during application, one small capacitor from COMP to GND is recommended. This forms a pole with R1 to compensate for the effect of the zero formed by the electrolytic capacitor ESR.

BYPASS Capacitor

The MP8124 integrates the V_{CC} power for internal circuit bias at 5V, typically. One 0.22μF ceramic bypass capacitor is necessary for the internal regulator. The V_{CC} power supplies the internal control circuit and does not connect the external load to the V_{CC} power.

BST Capacitor

The MP8124 uses one charge pump to power the N-channel MOSFET for the LDO regulator. One external bootstrap capacitor is necessary to bypass the charge pump power. A 0.1μF ceramic capacitor between BST and VBOOST is recommended.

Logic Input Connection

For EN, LINEDROP, 13V/18V, and EXTM, one high-level voltage (>2V) or low-level voltage (<0.8V) sets the different function states. The high-level input voltage connected to these pins should not be higher than 6.5V. For high-voltage inputs, <5.5V signals are recommended.

The EN signal can be connected to VIN through a resistor divider to set the automatic start-up once the input power is available. Do not pull up to VIN through one resistor. The resistor divider must keep the EN voltage within the 2V to 5.5V range for an input power range of 8V to 14V. Typically, a divider with a 249kΩ high-side resistor and a 100kΩ low-side resistor are recommended for normal application.

It is suggested that LINEDROP and 13V/18V are pulled to the BYPASS voltage for a default high input or pulled to GND for a default low input. The EXTM input signal should also be lower than 5.5V.

PCB Layout Guidelines

Efficient PCB layout is critical for high-frequency switching power supplies. A poor layout can result in reduced performance, excessive EMI, resistive loss, and system instability. For best results, refer to Figure 3 and follow the guidelines below.

1. Keep the boost output loop (IC-SW, D1, C2B, and IC-PGND) as small as possible.
2. Place the LDO input capacitor (C2A) and the output capacitor (C4) as close to VBOOST and VOUT as possible.
3. Connect the LDO output capacitor and the other signal ground to AGND.
4. Connect the boost output ground to PGND and then to AGND with a single point.
5. Keep all high-frequency AC current power traces (VDD, SW, PGND) as short and wide as possible.
6. Keep the TCAP voltage trace far away from any noise sources, such as the SW node.
7. Place a small decoupling capacitor as close to VDD as possible to reduce the input voltage ripple.
8. Place the bypass capacitor as close to BYPASS and VOUT as possible.
9. Keep the BST voltage path as short as possible.
10. Use a wide copper trace for GND to improve thermal performance. Vias on GND and copper around and under the MP8124 are also recommended to improve thermal performance.

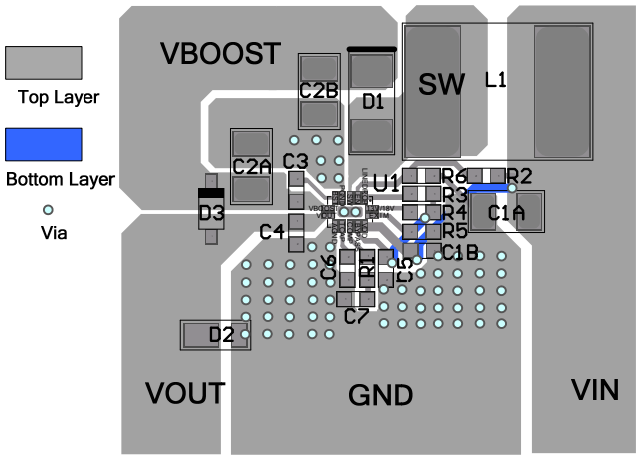


Figure 3: Layout Recommendation

Design Example

Table 1 is a design example following the application guidelines for the specifications below:

Table 1: Design Example

V_{IN}	8V - 14V
V_{OUT}	13V/ 14V/ 18V/ 19V
I_{OUT}	0A ~ 0.5A

The detailed application schematic is shown in Figure 4. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to related evaluation board datasheet.

TYPICAL APPLICATION CIRCUITS

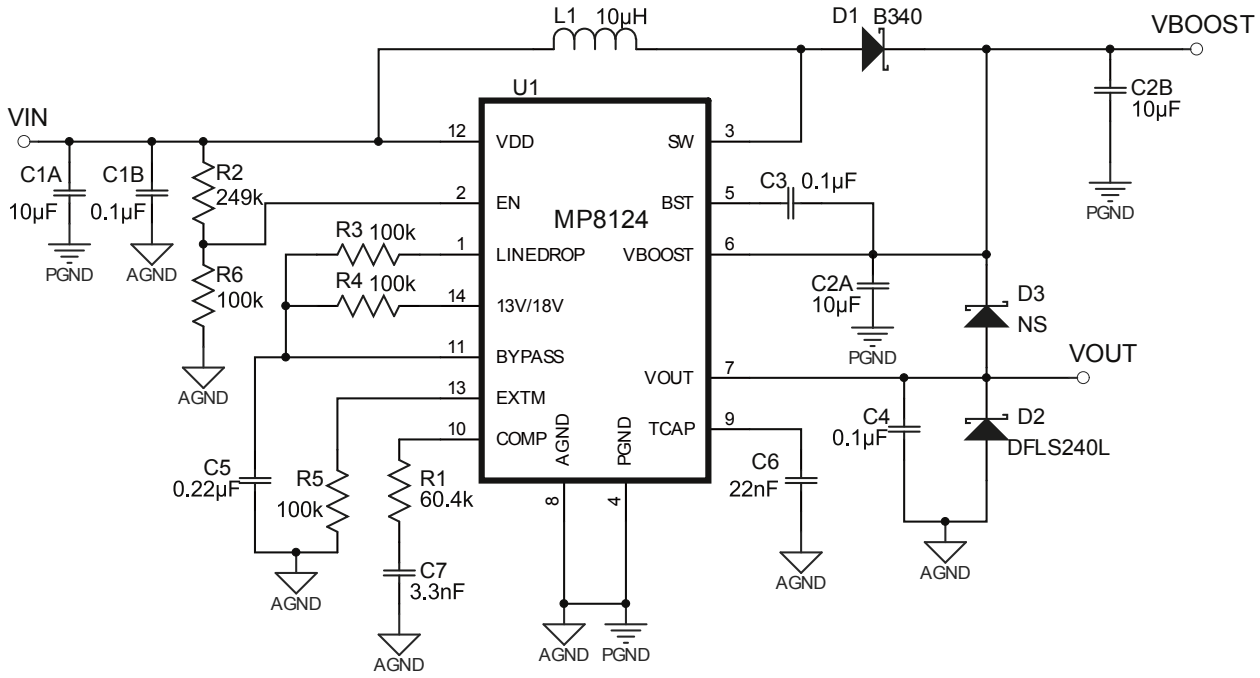


Figure 4: Typical Application Circuit, V_{IN} = 8V to 14V, V_{OUT} = 19V, I_{OUT} = 0A~0.5A