MP8761

High Efficiency, 8A, 18V, Synchronous, Step-Down Converter

DESCRIPTION

The MP8761 is a fully-integrated, high-frequency, synchronous, rectified, step-down, switch-mode converter. It offers a very compact solution to achieve a 8A output current over a wide input-supply range with excellent load and line regulation. The MP8761 operates at high efficiency over a wide output-current load range.

The MP8761 uses Constant-On-Time (COT) control mode to provide fast transient response and ease loop stabilization.

An external resistor programs the operating frequency from 200kHz to 1MHz. The frequency stays nearly constant as the input supply varies with the feed-forward compensation.

The default under voltage lockout threshold is internally set at less than 4.1V, but a resistor network on the enable pin can increase this threshold. The soft start pin controls the output voltage startup ramp. An open drain power good signal indicates that the output is within nominal voltage range.

It has full integrated protection features that include over-current protection, over-voltage protection and thermal shutdown.

The MP8761 is available in a 3mm×4mm QFN package, and requires a minimal number of readily-available components.

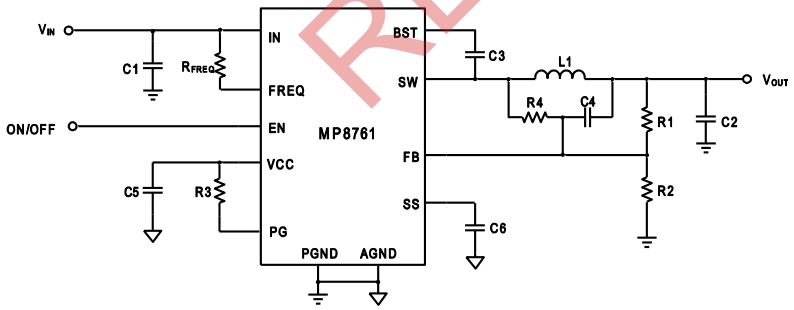
FEATURES

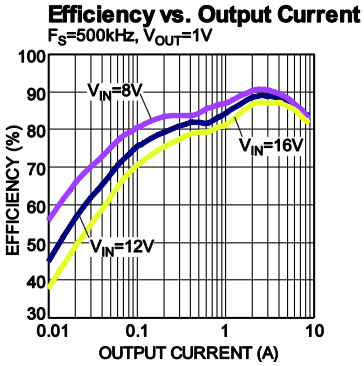
- 2.5V to 18V Operating Input Range with External 5V Bias
- 4.5V to 18V Operating Input Range with Internal Bias
- 8A Output Current
- Low $R_{DS(ON)}$ Internal Power MOSFETs
- Proprietary Switching-Loss-Reduction Technique
- Adaptive COT for Ultrafast Transient Response
- 1% Reference Voltage Over Junction Temperature Range (0°C to +125°C)
- Programmable Soft-Start Time
- Pre-Bias Start-Up
- Programmable Switching Frequency from 200kHz to 1MHz
- Non-Latch OCP, OVP, and Thermal Shutdown
- Output Adjustable from 0.611V to 13V

APPLICATIONS

- Set-Top Boxes
- XDSL Modem/DSLAM
- Small-Cell Base Stations
- Personal Video Recorders
- Flat-Panel Televisions and Monitors
- Distributed Power Systems

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number	Package	Top Marking
MP8761GL*	QFN-13 (3mm×4mm)	MP8761
MP8761GLE**	QFN-16 (3mm×4mm)	MP8761E

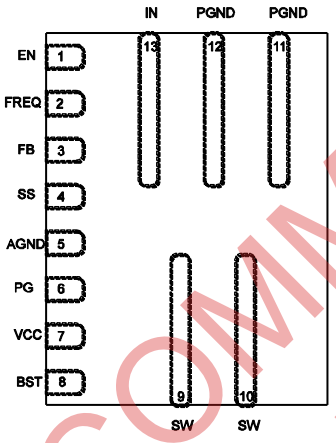
* For Tape & Reel, add suffix –Z (e.g. MP8761GL–Z)

** For Tape & Reel, add suffix –Z (e.g. MP8761GLE–Z)

Note: The 16-pin QFN package is preferred and recommended for new designs

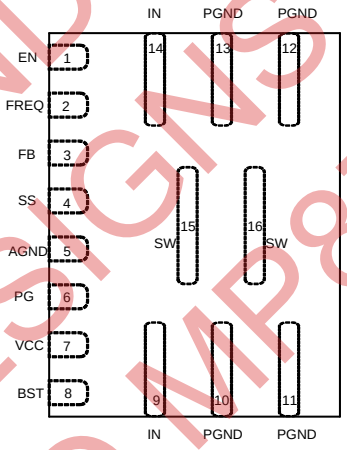
PACKAGE REFERENCE

TOP VIEW



13-Pin QFN (3x4mm)
Not Recommended for New Design

TOP VIEW



16-Pin QFN (3x4mm)
Recommended for New Design

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 21V
V_{SW} ..... −0.3V to V_{IN} + 0.3V
V_{SW} (30ns) ..... −3V to V_{IN} + 3V
V_{BST} ..... V_{SW} + 6V
Enable Current I_{EN} (2) 2.5mA
All Other Pins ..... –0.3V to +6V
Continuous Power Dissipation (T_A=+25°) (3)
QFN3×4 ..... 2.7W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... −65°C to +150°C

Recommended Operating Conditions (4)

Supply Voltage V_{IN} ..... 4.5V to 18V
Output Voltage V_{OUT} ..... 0.611V to 13V
I_{EN} ..... 0mA to 1mA
Operating Junction Temp. (T_J). −40°C to +125°C

Follow Layout Recommendation for Best Performance

Thermal Resistance (5) θ_{JA} θ_{JC}

QFN (3×4mm) ..... 46 ..... 9 .... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Refer to the section “Configuring the EN Control”.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V		0	1	μA
Supply Current (Quiescent)	I_{IN}	V_{EN} = 2V, V_{FB} = 1V	760	860	1000	μA
MOSFET						
High-Side Switch-On Resistance	HS_{RDS-ON}	T_J =25°C		28		mΩ
Low-Side Switch-On Resistance	LS_{RDS-ON}	T_J =25°C		16		mΩ
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V or 12V		0	1	μA
Current Limit						
Low-Side Valley Current Limit(6)	I_{LIMIT_VALLEY}		8	10	12	A
Low-Side Negative Current Limit(6)	$I_{LIMIT\_NEGATIVE}$		-4	-2.5	-1	A
Timer						
One-Shot ON Time	τ_{ON}	R_{FREQ}=453kΩ, V_{OUT}=1.2V		250		ns
Minimum ON Time(6)	τ_{ON_MIN}			30		ns
Minimum OFF Time(6)	τ_{OFF_MIN}			360		ns
Over-Voltage and Under-Voltage Protection						
OVP Non-Latch Threshold	$V_{OVP\_NON-LATCH}$		117%	120%	123%	V_{FB}
OVP Delay	τ_{OVP}			2		μs
UVP Threshold(6)	V_{UVP}			50%		V_{FB}
Reference And Soft-Start						
Reference Voltage	V_{REF}	T_J = -40°C to +125°C (7)	602	611	620	mV
		T_J = 0°C to +125°C (7)	605	611	617	
		T_J = +25°C	605	611	617	
Feedback Current	I_{FB}	V_{FB} = 650mV		50	100	nA
Soft-Start Charging Current	I_{SS}	V_{SS}=0V	16	20	25	μA
Enable And UVLO						
Enable Input High Voltage	VIH_{EN}		1.1	1.3	1.5	V
Enable Hysteresis	V_{EN-HYS}			250		mV
Enable Input Current	I_{EN}	V_{EN} = 2V		0		μA
		V_{EN} = 0V		0		

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VCC Regulator						
VCC Under-Voltage Lockout Threshold Rising	VCC_{Vth}		3.75	3.9	4.05	V
VCC Under-Voltage Lockout Threshold Hysteresis	VCC_{HYS}			500		mV
VCC Regulator	V_{CC}		4.65	4.8	4.95	V
VCC Load Regulation		Icc=5mA		0.5		%
Power Good						
Power-Good, Rising Threshold	PG_{Vth-Hi}		87%	91%	94%	V_{FB}
Power-Good, Falling Threshold	PG_{Vth-Lo}			80%		V_{FB}
Power-Good, Low-to-High Delay	PG_{Td}			2.5		ms
Power Good, Sink Current Capability	V_{PG}	Sink 4mA			0.4	V
Power Good, Leakage Current	I_{PG_LEAK}	V_{PG} = 3.3V		10	100	nA
Thermal Protection						
Thermal Shutdown(6)	T_{SD}		150			°C
Thermal Shutdown Hysteresis(6)				25		°C

Note:

6) Guaranteed by design.

7) Not production test, guaranteed by characterization

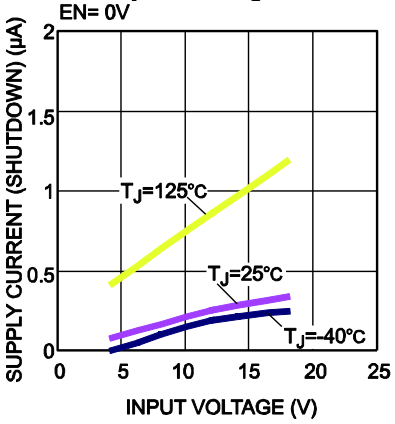
PIN FUNCTIONS

PIN # 13-Pin QFN	PIN# 16-Pin QFN	Name	Description
1	1	EN	Enable. Digital input to turn the regulator ON or OFF. Drive EN HIGH to turn on the regulator. Drive it LOW to turn it off. Connect EN to IN through a pull-up resistor or a resistive voltage divider for automatic startup. Do not float this pin.
2	2	FREQ	Frequency Set. Requires a resistor connected between FREQ and IN to set the switching frequency. The input voltage and the resistor connected to the FREQ pin determine the ON time. The connection to the IN pin provides line feed-forward and stabilizes the frequency during input voltage variation.
3	3	FB	Feedback. Connect to the tab of an external resistor divider from the output to GND to set the output voltage. FB is also configured to realize over-voltage protection (OVP) by monitoring output voltage. Place the resistor divider as close to FB pin as possible. Avoid using vias on the FB traces.
4	4	SS	Soft-Start. Connect an external capacitor to program the soft start time for the switch mode regulator.
5	5	AGND	Analog ground. The control circuit reference.
6	6	PG	Power Good, the output is an open drain signal. Require a pull-up resistor to a DC voltage to indicate high if the output voltage exceeds 91% of the nominal voltage. There is a delay from FB ≥ 91% to PG goes high.
7	7	VCC	Internal 4.8V LDO output. Power the driver and control circuits. 5V external bias can disable the internal LDO. Decoupling with ≥1µF ceramic capacitor as close to the pin as possible. Use X7R or X5R dielectric ceramic capacitors for their stable temperature characteristics.
8	8	BST	Bootstrap. Require a capacitor connected between SW and BST pins to form a floating supply across the high-side switch driver.
9, 10	15, 16	SW	Switch Output. Connect to the inductor and bootstrap capacitor. The high-side switch drives the pin up to the V_{IN} voltage during PWM duty cycle's ON time. The inductor current drives the SW pin negative during the OFF-time. The low-side switch's ON-resistance and the internal Schottky diode clamp the negative voltage. Connect using wide PCB traces
11, 12	10, 11, 12, 13	PGND	System Ground. Reference ground of the regulated output voltage. PCB layout requires extra care. Connect using wide PCB traces.
13	9,14	IN	Supply Voltage. Supplies power to the internal MOSFET and regulator. The MP8761 operates from a +2.5V to +18V input rail with 5V external bias and a +4.5V to +18V input rail with internal bias. Requires an input decoupling capacitor. Connect using wide PCB traces and multiple vias.

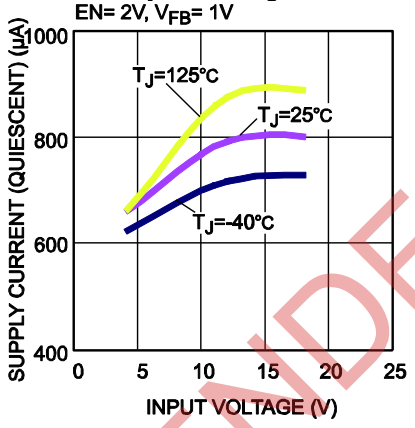
TYPICAL CHARACTERISTICS

VIN = 12V, V_{OUT} = 1V, L = 1µH, T_A = 25°C, unless otherwise noted.

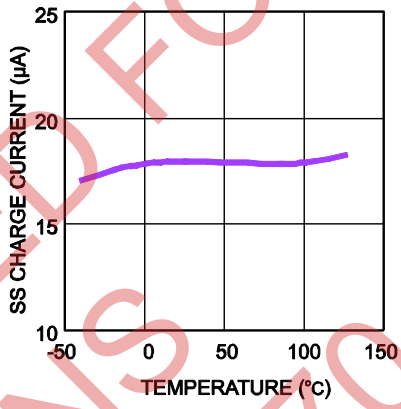
Supply Current (Shutdown) vs. Input Voltage



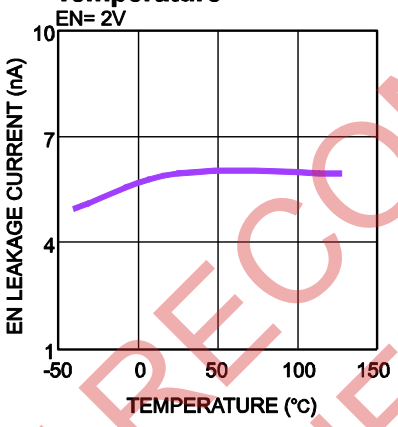
Supply Current (Quiescent) vs. Input Voltage



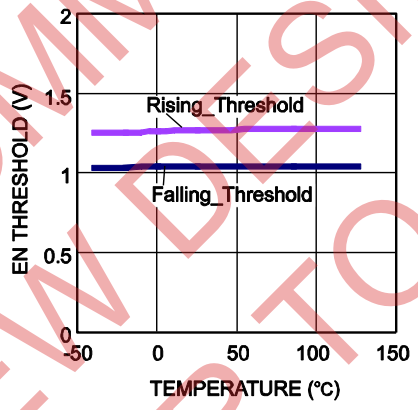
SS Charge Current vs. Temperature



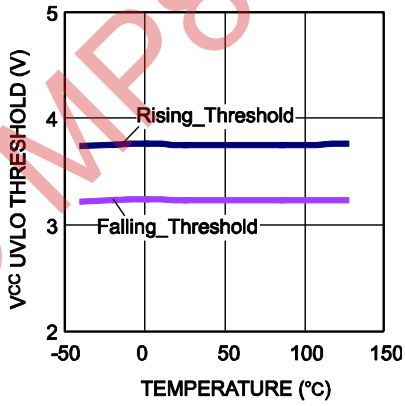
EN Leakage Current vs. Temperature



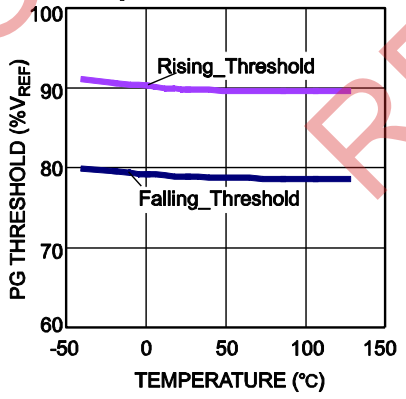
EN Threshold vs. Temperature



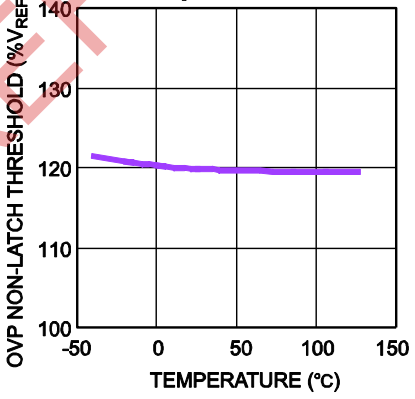
V_{CC} UVLO Threshold vs. Temperature



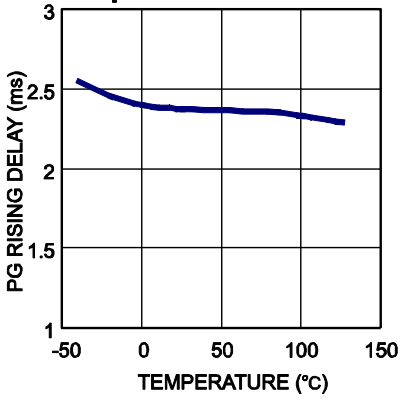
PG Threshold vs. Temperature



OVP Non-Latch Threshold vs. Temperature



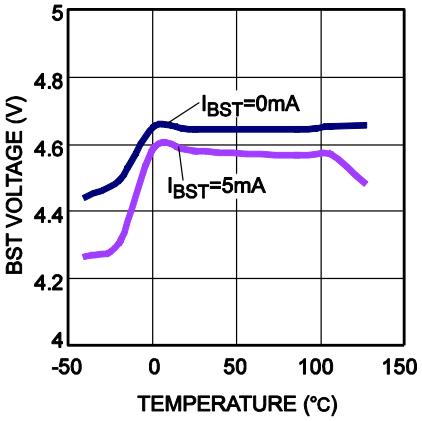
PG Rising Delay vs. Temperature



TYPICAL CHARACTERISTICS *(continued)*

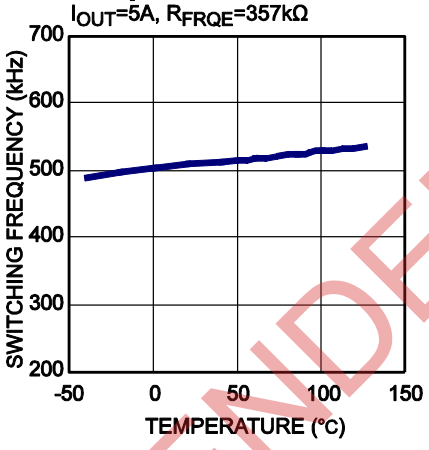
V_{IN} = 12V, V_{OUT} = 1V, L = 1µH, T_A = 25°C, unless otherwise noted.

BST Voltage vs. Temperature

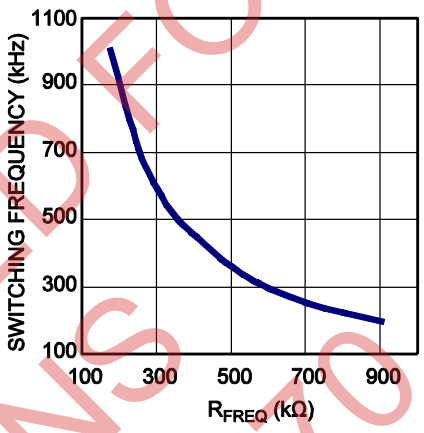


Switching Frequency vs. Temperature

I_{OUT}=5A, R_{FRQE}=357kΩ

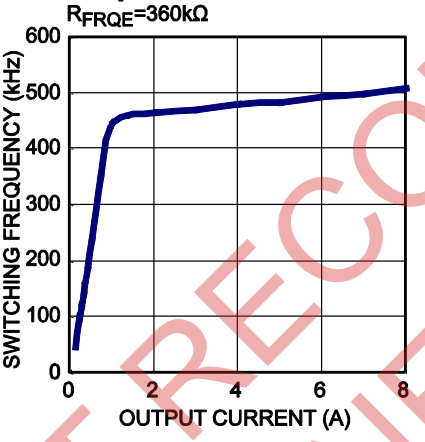


Switching Frequency vs. R_{FREQ}



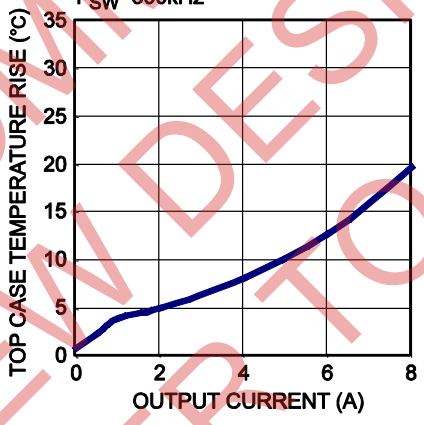
Switching Frequency vs. Output Current

R_{FRQE}=360kΩ

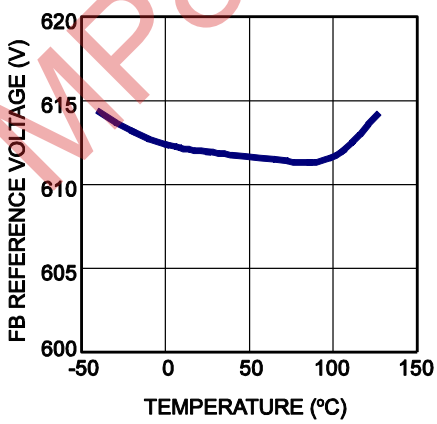


Case Temperature Rise vs. Output Current

F_{SW}=500kHz



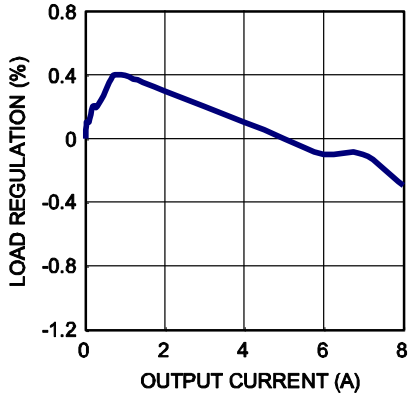
FB Reference Voltage vs. Temperature



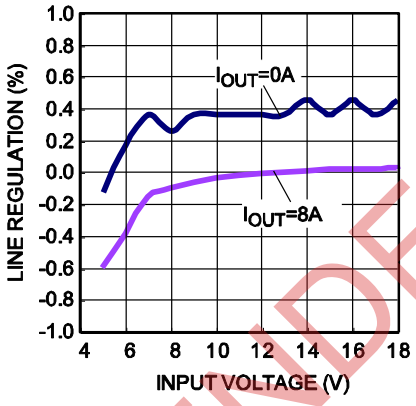
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1V, L = 1µH, T_A = 25°C, unless otherwise noted.

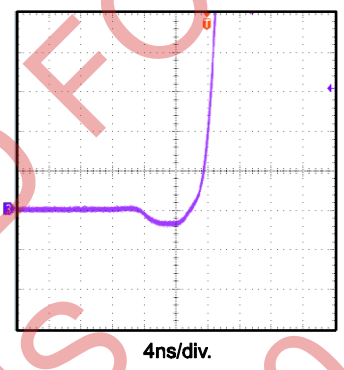
Load Regulation



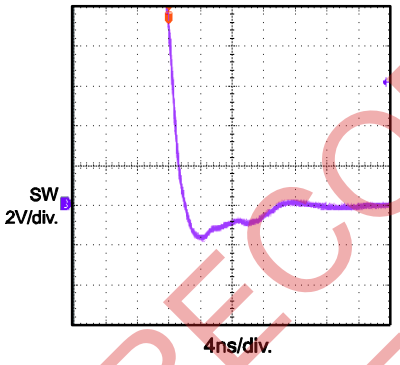
Line Regulation



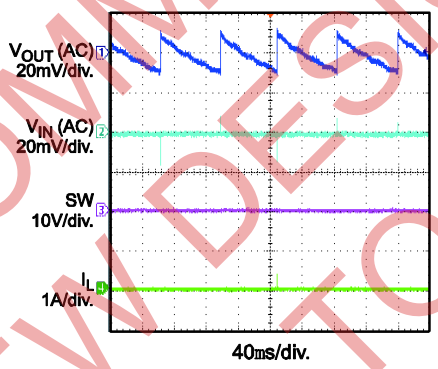
Dead Time (on)
I_{OUT} = 6A



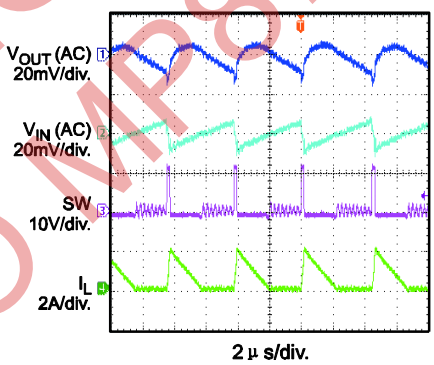
Dead Time (off)
I_{OUT} = 6A



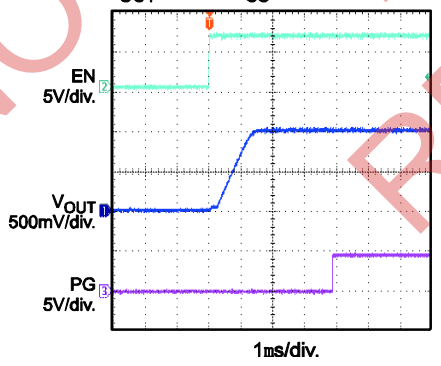
Input/Output Voltage Ripple
I_{OUT} = 0A



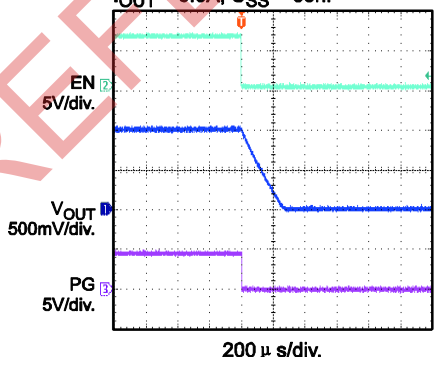
Input/Output Voltage Ripple
I_{OUT} = 0.5A



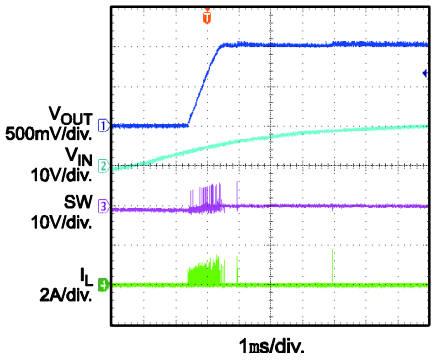
Power Good through EN Start Up
I_{OUT} = 0.5A, C_{SS} = 33nF



Power Good through EN Shutown
I_{OUT} = 0.5A, C_{SS} = 33nF



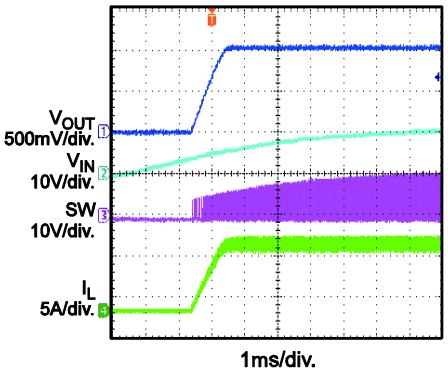
Start Up Through V_{IN}
I_{OUT} = 0A



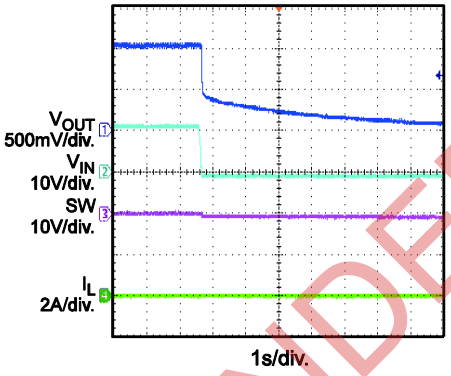
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, V_{OUT} =1V, L=1µH, T_A=+25°C, unless otherwise noted.

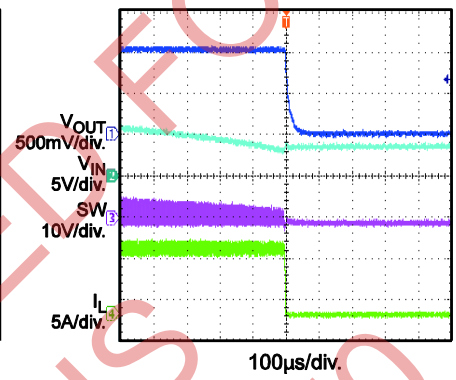
Start Up Through V_{IN}
I_{OUT} = 8A



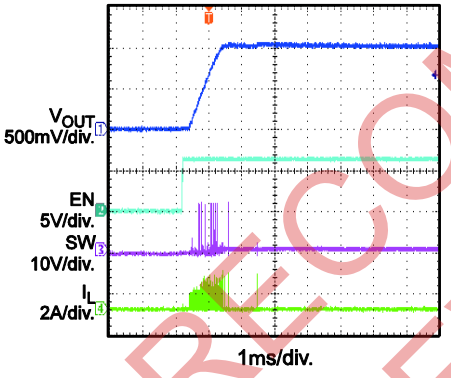
Shutdown Through V_{IN}
I_{OUT} = 0A



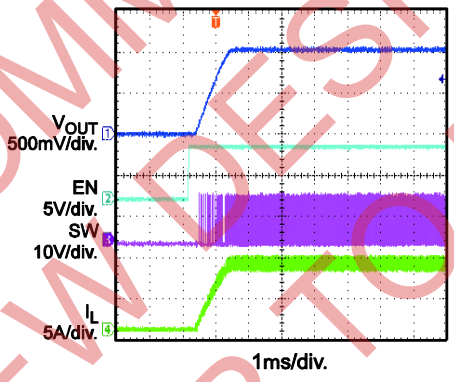
Shutdown Through V_{IN}
I_{OUT} = 8A



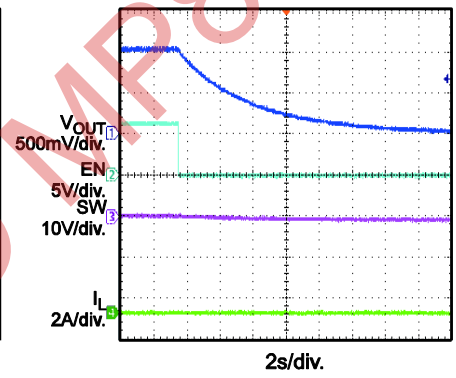
Start up through EN
I_{OUT} = 0A



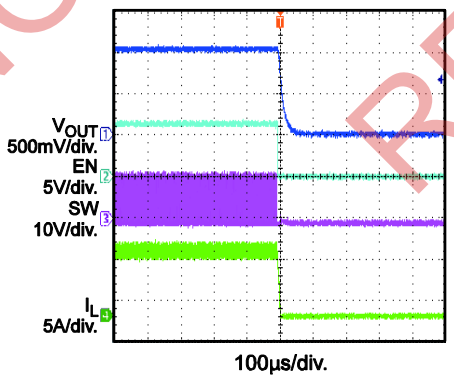
Start up through EN
I_{OUT} = 8A



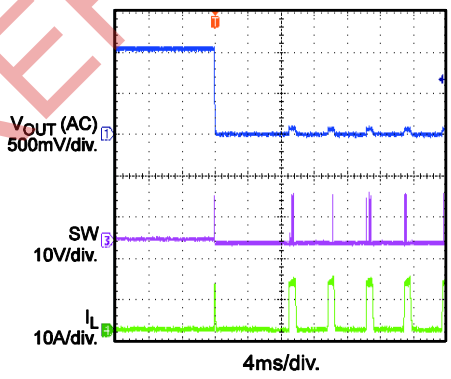
Shutdown Through EN
I_{OUT} = 0A



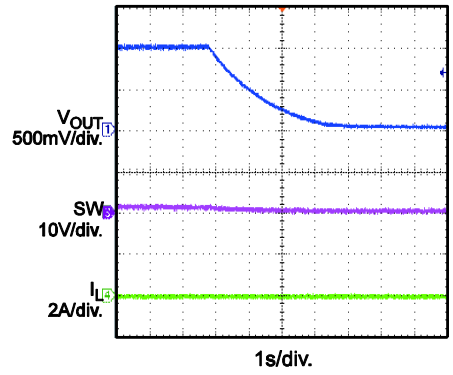
Shutdown Through EN
I_{OUT} = 8A



Short Circuit Protection



Thermal Shutdown
I_{OUT} = 0A

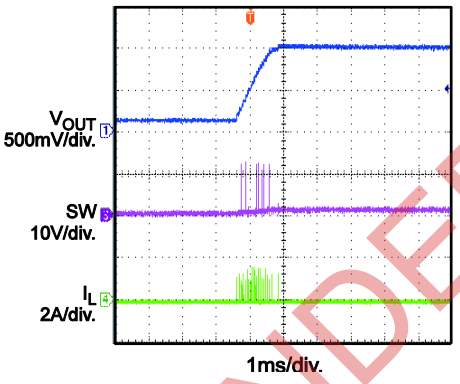


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, V_{OUT} =1V, L=1µH, T_A=+25°C, unless otherwise noted.

Thermal Recovery

I_{OUT} = 0A



BLOCK DIAGRAM

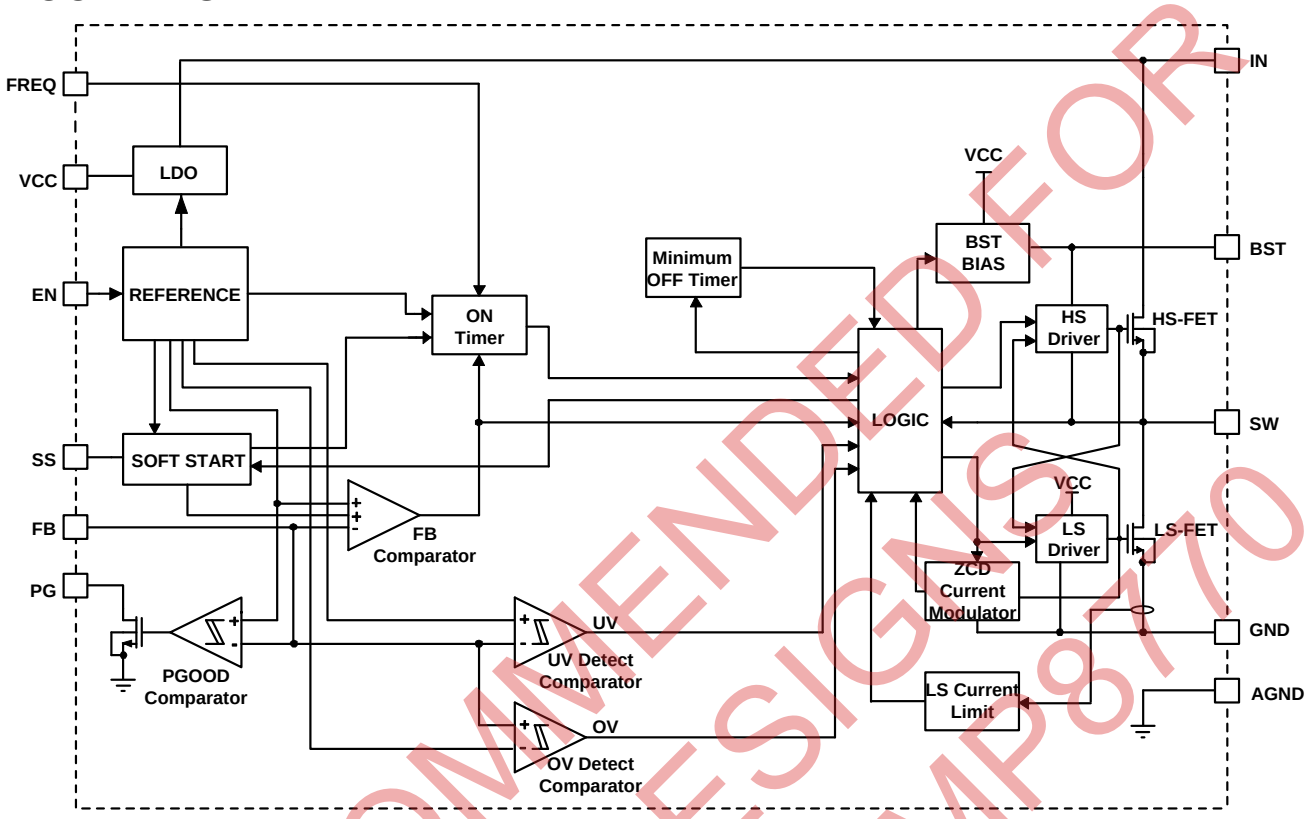


Figure 1: Functional Block Diagram

OPERATION

PWM Operation

The MP8761 is a fully-integrated, synchronous, rectified, step-down, switch-mode converter. It uses constant-on-time (COT) control to provide a fast transient response and ease loop stabilization.

At the beginning of each cycle, the high-side MOSFET (HS-FET) turns ON when the feedback voltage (V_{FB}) drops below the reference voltage (V_{REF}), which indicates an insufficient output voltage. The input voltage and the frequency-set resistor determine the ON period as follows:

$$\tau_{ON}(ns) = \frac{6.1 \times R_{FREQ}(k\Omega)}{V_{IN}(V) - 0.4} \quad (1)$$

After the ON period elapses, the HS-FET turns off. It turns ON again when V_{FB} drops below V_{REF}. By repeating this operation, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns ON when the HS-FET is OFF to minimize conduction loss and avoid a dead short (or shoot-through) between input and GND if both HS-FET and LS-FET turn on at the same time. An internally-generated dead-time (DT) between HS-FET OFF and LS-FET ON or LS-FET OFF and HS-FET ON avoids shoot-through.

Heavy-Load Operation

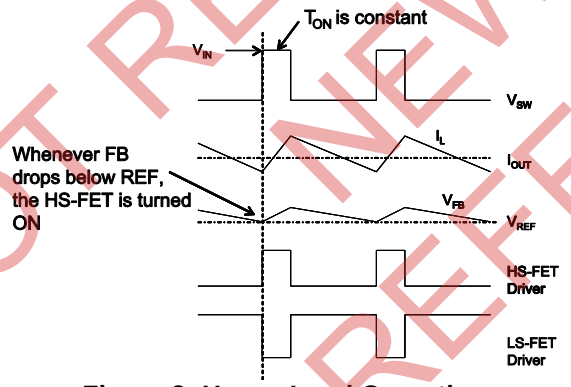


Figure 2: Heavy-Load Operation

When the output current is high and the inductor current is always above zero amps, it is called continuous-conduction-mode (CCM). Figure 2 shows the CCM operation. When $V_{FB}<V_{REF}$, HS-FET turns ON for a fixed interval determined by the one-shot ON-timer as per equation 1. When the HS-FET turns OFF, the LS-FET turns ON until the next period.

In CCM, the switching frequency is fairly constant and it is also called PWM mode.

Light-Load Operation

As the load decreases, the inductor current decreases. The operation transitions from CCM to discontinuous-conduction-mode (DCM) when the inductor current reaches 0A.

Figure 3 shows light-load operation. When V_{FB} drops below V_{REF}, HS-FET turns ON for a fixed interval determined by the one- shot ON-timer as per equation 1. When the HS-FET turns OFF, the LS-FET turns ON until the inductor current reaches zero. In DCM, the V_{FB} does not reach V_{REF} when the inductor current reaches zero: Instead, the LS-FET driver enters tri-state (high Z). A current modulator then controls the LS-FET and limits the inductor current to less than −1mA. Hence, the output capacitors discharge slowly to GND through LS-FET, and the HS-FET doesn't turn ON as frequently as under heavy-load conditions, thus greatly improving light-load and no-load efficiency. This is called skip mode.

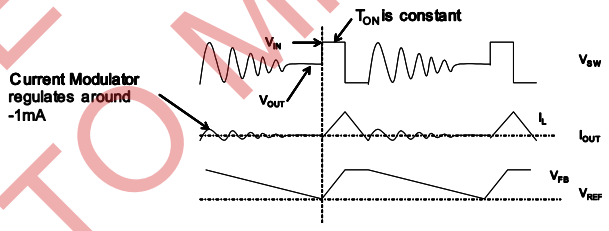


Figure 3: Light-Load Operation

As the output current increases from the light-load, the current modulator shortens the operating period to turn the HS-FET ON more frequently. Hence, the switching frequency increases. The output current reaches its critical threshold when the current modulator time decreases to zero. Determine the critical output current level as follows:

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (2)$$

Where f_{SW} is the switching frequency.

The IC enters PWM mode once the output current exceeds its critical level. Then the switching frequency stays fairly constant over the output current range.

Switching Frequency

Selecting the switching frequency requires trading off between efficiency and component size. Low-frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductor and capacitor values to minimize the output voltage ripple.

For the MP8761, set the ON time using the FREQ pin, thus setting the frequency for steady-state operation at CCM.

The MP8761 uses adaptive constant-on-time (COT) control, though the IC lacks a dedicated oscillator. Connect the FREQ pin to the IN pin through the resistor (R_{FREQ}) so that the input voltage is feed-forwarded to the one-shot on-time timer. When operating in steady-state in CCM, the duty ratio stays at V_{OUT}/V_{IN} so the switching frequency is fairly constant over the input voltage range. Set switching frequency as follows:

$$f_{SW}(kHz) = \frac{10^6}{\frac{6.1 \times R_{FREQ}(k\Omega)}{V_{IN}(V) - 0.4} \times \frac{V_{IN}(V)}{V_{OUT}(V)} + \tau_{DELAY}(ns)} \quad (3)$$

Where τ_{DELAY} is the comparator delay (5ns). After adding load, the frequency may be affected a little because power MOSFET voltage drop will affect the duty cycle.

Typically, the MP8761 is set between 200kHz and 1MHz. It is optimized to operate efficiently at high switching frequencies, which allow for physically smaller LC filter components to reduce the PCB footprint.

Jitter and FB Ramp Slope

Figure 4 and Figure 5 show jitter occurring in both PWM mode and skip mode. When there is noise on the V_{FB} descending slope, the HS-FET ON time deviates from its intended appoint, introducing jitter that influences the system's stability. The V_{FB} ripple's slope steepness dominates the noise immunity though its magnitude has no direct effect.

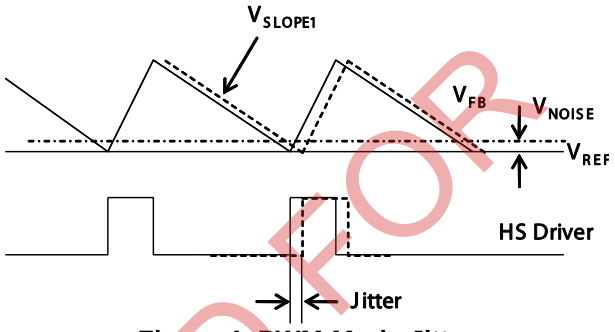


Figure 4: PWM-Mode Jitter

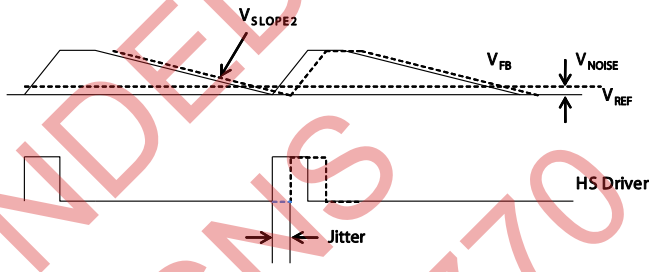


Figure 5: Skip-Mode Jitter

Ramp with a Large ESR Capacitor

Using POSCAPs or other large-ESR capacitors as the output capacitor results in the ESR ripple dominating the output ripple. The ESR also significantly influences the V_{FB} slope. Figure 6 shows the simplified equivalent circuit in PWM mode with the HS-FET OFF and without an external ramp circuit.

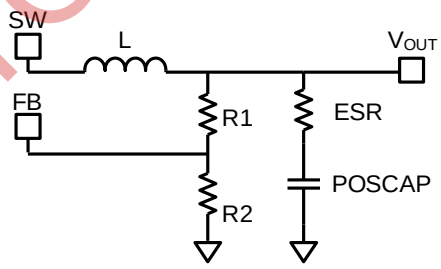


Figure 6: Simplified PWM-Mode Circuit without External Ramp Compensation

To realize the stability without an external ramp, select the ESR value as follows:

$$R_{ESR} \geq \frac{\frac{\tau_{SW}}{0.7 \times \pi} + \frac{\tau_{ON}}{2}}{C_{OUT}} \quad (4)$$

Where τ_{SW} is the switching period.

Ramp with a Small ESR Capacitor

Use an external ramp when using ceramic output capacitors, because the ESR ripple is not high enough to stabilize the system.

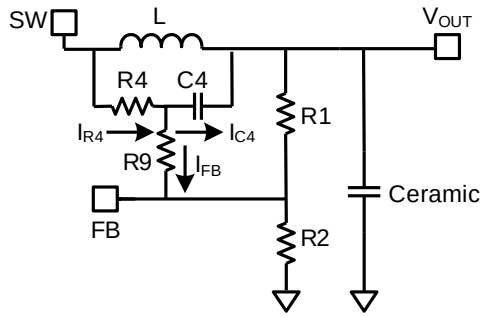


Figure 7: Simplified PWM-Mode Circuit with External Ramp Compensation

Figure 7 shows the simplified circuit in PWM mode with the HS-FET OFF and an external ramp compensation circuit (R4, C4). Design the external ramp based on the inductor ripple current. Select C4, R9, R1 and R2 to meet the following condition:

$$\frac{1}{2\pi \times f_{SW} \times C4} < \frac{1}{5} \times \left(\frac{R1 \times R2}{R1 + R2} + R9 \right) \quad (5)$$

Where:

$$I_{R4} = I_{C4} + I_{FB} \approx I_{C4} \quad (6)$$

Then estimate the ramp on V_{FB} as:

$$V_{RAMP} = \frac{V_{IN} - V_{OUT}}{R4 \times C4} \times \tau_{ON} \times \left(\frac{R1 // R2}{R1 // R2 + R9} \right) \quad (7)$$

The V_{FB} ripple's descending slope is then:

$$V_{SLOPE1} = \frac{V_{RAMP}}{\tau_{OFF}} = \frac{-V_{OUT}}{R4 \times C4} \quad (8)$$

Equation 8 shows that if there is instability in PWM mode, reduce either R4 or C4. If C4 is irreducible due to limitations from equation 5, then reduce R4. For stable PWM operation, design V_{slope1} based on equation 9.

$$-V_{SLOPE1} \geq \frac{\frac{T_{SW}}{0.7 \times \pi} + \frac{T_{ON}}{2} - R_{ESR} \times C_{OUT}}{2 \times L \times C_{OUT}} \times V_{OUT} + \frac{I_{OUT} \times 10^{-3}}{T_{SW} - T_{ON}} \quad (9)$$

Where I_{OUT} is the load current.

In skip mode, the V_{FB} ripple's descending slope is almost the same whether the external ramp is used or not. Figure 8 shows the simplified circuit in skip mode when both the HS-FET and LS-FET are off.

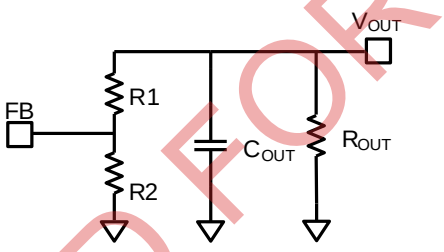


Figure 8: Simplified Skip-Mode Circuit

Determine the V_{FB} ripple's descending slope in skip mode as follows:

$$V_{SLOPE2} = \frac{-V_{REF}}{[(R1 + R2) // R_{OUT}] \times C_{OUT}} \quad (10)$$

Where R_{OUT} is the equivalent load resistor.

Figures 5 shows that V_{SLOPE2} in skip mode is lower than it is in PWM mode, so it is reasonable that the jitter in skip mode is larger. To achieve less jitter during ultra-light-load conditions, reduce R1 and R2, though that will decrease the light-load efficiency.

Configuring the EN Control

The regulator turns on when EN goes HIGH. Conversely it turns OFF when EN goes LOW. Do not float the pin.

For automatic start-up, pull the EN pin up to the input voltage through a resistive voltage divider. Choose the values of the pull-up resistor (R_{UP}, from the IN pin to the EN pin) and the pull-down resistor (R_{DOWN}, from the EN pin to GND) to determine the automatic start-up voltage:

$$V_{IN-START} = 1.5 \times \frac{(R_{UP} + R_{DOWN})}{R_{DOWN}} (V) \quad (11)$$

For example, for R_{UP}=100kΩ and R_{DOWN}=20kΩ, the $V_{IN-START}$ is set at 9V.

To reduce noise, add a 10nF ceramic capacitor from EN to GND.

An internal zener diode on the EN pin clamps the EN pin voltage to prevent runaway. The maximum pull-up current (assuming the worst case, 6V) for the internal zener clamp should be less than 1mA.

Therefore, when driving EN with an external logic signal, use an EN voltage less than 6V; when

connecting EN to IN through a pull-up resistor or a resistive voltage divider, select a resistance that ensures a maximum pull up current less than 1mA.

If using a resistive voltage divider and V_{IN} exceeds 6V, then the minimum resistance for the pull-up resistor R_{UP} should meet:

$$\frac{V_{IN}-6V}{R_{UP}}-\frac{6V}{R_{DOWN}}\le 1mA \quad (12)$$

With only R_{UP} (the pull-down resistor R_{DOWN} is not connected), then the VCC UVLO threshold determines $V_{IN-START}$ so the minimum resistor value is:

$$R_{UP}\ge\frac{V_{IN}-6V}{1mA}(\Omega) \quad (13)$$

A typical pull-up resistor is 100kΩ.

External VCC bias

An external 5V VCC bias can disable the internal LDO, in this case, Vin can be as low as 2.5V.

Soft-Start

The MP8761 employs soft-start (SS) to ensure a smooth output during power-up. When the EN pin goes HIGH, an internal current source (20μA) charges the SS capacitor. The SS capacitor voltage takes over the REF voltage to the PWM comparator. The output voltage smoothly ramps up with the SS voltage. It continues ramping up while V_{REF} takes over the PWM comparator. At this point, soft-start finishes and the device enters steady state operation.

Determine the SS capacitor value as follows:

$$C_{SS}(nF)=\frac{T_{SS}(ms)\times I_{SS}(\mu A)}{V_{REF}(V)} \quad (14)$$

If the output capacitors are large, then avoid setting a short SS time otherwise it would risk hitting the current limit during SS.

Pre-Bias Startup

The MP8761 is designed for monotonic startup for pre-biased loads. If the output is pre-biased to a certain voltage during startup, the IC will disable switching for both high-side and low-side switches until the voltage on the soft-start capacitor exceeds the sensed output voltage at the FB pin.

Power Good (PG)

The MP8761 has a power-good (PG) output. The PG pin is the open drain of a MOSFET. Connect it to VCC or some other voltage source that measures less than 5.5V through a pull-up resistor (typically 100kΩ). After applying the input voltage, the MOSFET turns ON so that the PG pin is pulled to GND before the SS is ready. After the FB voltage reaches 91% of the REF voltage, the PG pin is pulled HIGH after a 2.5ms delay.

When the FB voltage drops to 80% of the REF voltage or exceeds 120% of the nominal REF voltage, the PG pin is pulled LOW.

If the input supply fails to power the MP8761, the PG pin is also pulled low even though this pin is tied to an external DC source through a pull-up resistor (typically. 100kΩ).

Over-Current Protection (OCP)

The MP8761 features two current limit levels for over-current conditions: low-side valley current limit and low-side negative current limit.

Low-Side Valley Current Limit: The device monitors the inductor current during LS-FET ON state. At the end of LS-FET on time, the LS-FET sourcing current is compared to the internal positive-valley-current limit. If the valley current limit is less than LS-FET sourcing current, the HS-FET remains OFF and LS-FET remains ON. When LS-FET sourcing current drops below the valley current limit, the LS-FET turns OFF and the HS-FET turns ON for a fixed time determined by frequency-set resistor R_{FREQ} and input voltage.

During OCP, the device tries to recover from the over-current fault with hiccup mode: the chip disables the output power stage, discharges the soft-start capacitor and then automatically retries soft-start. If the over-current condition still holds after soft-start ends, the device repeats this operation cycle until the over-current conditions disappear and then output rises back to regulation level. OCP offers non-latch protection.

Low-Side Negative Current Limit: If the sensed LS-FET negative current exceeds the negative current limit, the LS-FET turns OFF immediately and stays OFF for the reminder for the OFF period. In this situation, both MOSFETs are OFF until the end of a fixed interval. The HS-FET body diode conducts the inductor current for the fixed time.

Over-Voltage Protection (OVP)

The MP8761 monitors the output voltage using the FB pin connected to the tap of a resistor divider.

If the FB voltage exceeds the nominal REF voltage but remains below 120% of the REF voltage (0.611V), both MOSFETs are OFF.

If the FB voltage exceeds 120% of the REF voltage but remains below 130%, the LS-FET turns ON while the HS-FET remains OFF. The LS-FET remains ON until the FB voltage drops below 110% of the REF voltage or the low-side negative current limit triggers.

If the FB voltage exceeds 130% of the REF voltage, the device enters a non-latch OFF mode. Once the FB voltage rises to a reasonable value, it will exit OVP and operate normally.

UVLO protection

The MP8761 has under-voltage lockout (UVLO). When the VCC voltage exceeds the UVLO-rising threshold, the MP8761 powers up. It shuts OFF when the VCC voltage falls below the UVLO falling threshold. This is non-latch protection.

The MP8761 is disabled when the VCC voltage falls below 3.4V. If an application requires a higher UVLO threshold, use the two external resistors connected to the EN pin as shown in Figure 9 to adjust the startup input voltage. For best results, use the enable resistors to set the input voltage falling threshold (V_{STOP}) above 4 V. Set the rising threshold (V_{START}) to provide enough hysteresis to account for any input supply variations.

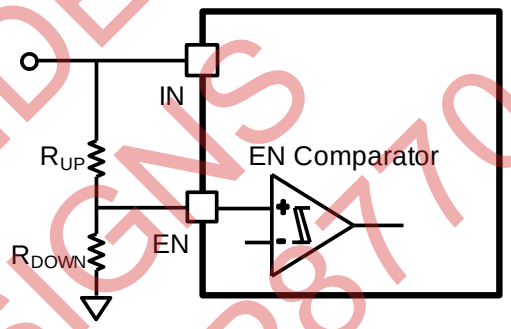


Figure 9: Adjustable UVLO

Thermal Shutdown

The MP8761 has thermal shutdown. The IC internally monitors the junction temperature. If the junction temperature exceeds the threshold value (minimum 150°C), the converter shuts off. This is a non-latch protection. There is ~25°C hysteresis. Once the junction temperature drops to ~125°C, it initiates a soft-start.

APPLICATION INFORMATION

Output-Voltage, Large-ESR Capacitors

For applications that use electrolytic or POS capacitors with large ESR values as output capacitors, the feedback resistors—R1 and R2 as shown in Figure 10—set the output voltage.

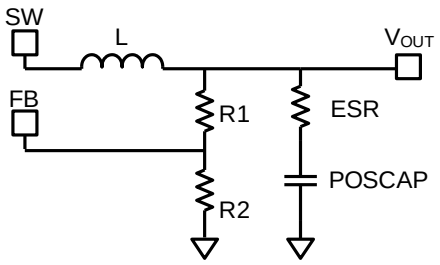


Figure 10: Simplified POSCAP Circuit

First, choose an R2 that balances between high quiescent current loss (lower R2) and high noise sensitive on FB (higher R2). A typical value falls within 5kΩ-50kΩ, using a comparatively larger R2 when V_{OUT} is low, and a smaller R2 when V_{OUT} is high. Then calculate R1 as follows:

$$R1 = \frac{V_{OUT} - \frac{1}{2} \times \Delta V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (15)$$

Where ΔV_{OUT} is the output ripple determined by equation 24.

Output-Voltage, Small-ESR Capacitors

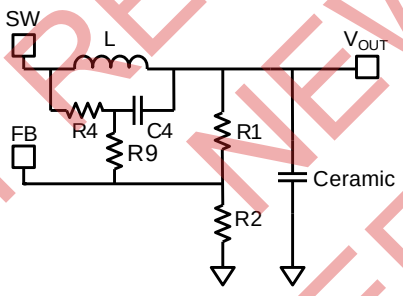


Figure 11: Simplified Ceramic Capacitor Circuit

When using a low-ESR, ceramic capacitor on the output, add an external voltage ramp to the FB pin (R4 and C4). The ramp voltage (V_{RAMP}) and the resistor divider (shown in Figure 11) influence the output voltage . Calculate V_{RAMP} as shown in equation 7. Select R2 to balance between high quiescent current loss and FB noise sensitivity. Choose R2 within 5kΩ-50kΩ, using a larger R2 when V_{OUT} is low, and a smaller R2 when V_{OUT} is high. Determine the value of R1 as follows:

$$R1 = \frac{R2}{\frac{V_{FB(AVG)}}{V_{OUT} - V_{FB(AVG)}} - \frac{R2}{R4 + R9}} \quad (16)$$

Where $V_{FB(AVG)}$ is the average FB voltage. $V_{FB(AVG)}$ varies with the V_{IN}, V_{OUT}, and load condition, where the load regulation is strictly related to the $V_{FB(AVG)}$. Also the line regulation is related to the $V_{FB(AVG)}$—improving load or line regulation involves a lower V_{RAMP} that meets equation 9.

For PWM operation, estimate VFB (AVG) from equation 17.

$$V_{FB(AVG)} = V_{REF} + \frac{1}{2} \times V_{RAMP} \quad (17)$$

Usually, R9 is 0Ω, though it can also be set following equation 18 for better noise immunity. It should also be less than 20% of R1//R2 to minimize its influence on V_{RAMP}.

$$R9 < \frac{1}{5} \times \frac{R1 \times R2}{R1 + R2} \quad (18)$$

Using equations 16 and 17 to calculate the output voltage can be complicated. To simplify the R1 calculation in equation 16, add a DC-blocking capacitor (C_{DC}) to filter the DC influence from R4 and R9. Figure 12 shows a simplified circuit with external ramp compensation and a DC-blocking capacitor. The addition of this capacitor simplifies the R1 calculation as per equation 19 for PWM mode operation.

$$R1 = \frac{V_{OUT} - V_{REF} - \frac{1}{2} \times V_{RAMP}}{V_{REF} + \frac{1}{2} \times V_{RAMP}} \times R2 \quad (19)$$

For best results, select a C_{DC} value at least 10×C4 for better DC blocking performance, but smaller than 0.47uF to account for start-up performance. To use a larger C_{DC} for better FB noise immunity, reduce R1 and R2 to limit their effects on system start-up. Note that even with C_{DC}, the load and line regulation are still related to V_{RAMP}.

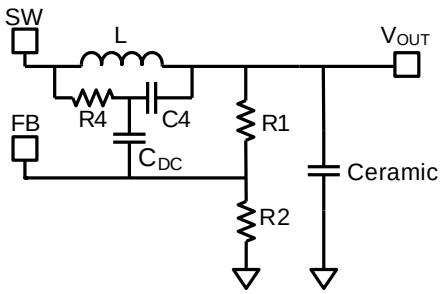


Figure 12: Simplified Ceramic Capacitor Circuit with DC-Blocking Capacitor

Input Capacitor

The input current to the step-down converter is discontinuous, and therefore, requires a capacitor to supply the AC current to the step-down converter while maintaining the DC-input voltage. Use ceramic capacitors for best performance. During layout, place the input capacitors as close to the IN pin as possible.

The capacitance can vary significantly with temperature. Use capacitors with X5R and X7R ceramic dielectrics because they are fairly stable over a wide temperature range.

The capacitors must also have a ripple-current rating that exceeds the converter's maximum input ripple current. Estimate the input ripple current as follows:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (20)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (21)$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half the maximum load current.

The input capacitance value determines the converter input voltage ripple. Select a capacitor value that meets the input voltage ripple requirement

Estimate the input voltage ripple as follows:

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (22)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (23)$$

Output Capacitor

The output capacitor maintains the DC output voltage. Use ceramic capacitors or POSCAPs Estimate the output voltage ripple as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (24)$$

When using ceramic capacitors, the capacitance dominates the impendence at the switching frequency. The capacitance also dominates the output voltage ripple. For simplification, estimate the output voltage ripple as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (25)$$

The ESR contributes minimally to the output voltage ripple, thus requiring an external ramp to stabilize the system. Design the external ramp with R4 and C4 as per equations 5, 8, and 9.

The ESR dominates the switching-frequency impedance for POSCAPs. The ESR ramp voltage is high enough to stabilize the system thus eliminating the need for an external ramp. Select a minimum ESR value of ~12mΩ to ensure stable operation. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (26)$$

Inductor

The inductor supplies constant current to the output load while being driven by the switching input voltage. A larger value inductor results in less ripple current and lower output ripple voltage, but is physically larger, has a higher series resistance, and often a lower saturation current. Generally, select an inductor value that allows the inductor peak-to-peak ripple current that is 30% to 40% of the maximum switch current limit. Also, design for a peak inductor current that is

below the maximum switch-current limit. Calculate the inductance value as:

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (27)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated as:

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (28)$$

Table 1 lists a few highly-recommended high-efficiency inductors.

Table 1: Inductor Selection Guide

Part Number	Manufacturer	Inductance (µH)	DCR (mΩ)	Current Rating (A)	Dimensions L × W × H (mm³)	Switching Frequency (kHz)
744325072	Wurth	0.72	1.35	35	10.2 × 10.5 × 4.7	500
744325180	Wurth	1.8	3.5	18	10.2 × 10.5 × 4.7	500
FDA1055-2R2M	TOKO	2.2	3.94	20.6	11.6 × 10.8 × 5.5	500

Typical Design Parameters

Tables 2 and 3 list recommended component values for typical output voltages (1V, 2.5V, 3.3V) and switching frequency (500kHz). Refer to Table 2 for design cases without external ramp compensation and Table 3 for design cases with external ramp compensation. An external ramp is not needed when using high-ESR capacitors, such as electrolytics or POSCAPs. Use an external ramp when using low-ESR capacitors, such as ceramic capacitors. For cases not listed in this datasheet, conctact a local sales representative for an Excel spreadsheet to assist with the calculation.

Table 2—F_{SW}=500kHz, V_{IN}=12V

V_{OUT} (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R7 [8] (kΩ)
1	1	12.7	20	357
2.5	2.2	61.9	20	825
3.3	3.3	88.7	20	1083

Table 3—F_{SW}=500kHz, V_{IN}=12V

V_{OUT} (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R4 (kΩ)	C4 (pF)	R7 [8] (kΩ)
1	1	12.7	20	750	220	357
2.5	2.2	64.9	20	1000	220	825
3.3	3.3	93.1	20	1200	220	1083

Notes:

8) Frequency is about 500kHz at full load condition in test. R_{FREQ} is a little different from equation (3) due to the voltage drop on MOSFET.

LAYOUT RECOMMENDATIONS

1. MPS offers two packages, but recommends MP8761GLE with its 16-pin QFN package for all new designs due to its smaller parasitical inductance.
2. Place high current paths (GND, IN, and SW) very close to the device with short, direct and wide traces.
3. The 13-pin QFN package requires two copper IN layers for better performance. Respectively put at least one decoupling capacitor on both Top and Bottom layers and as close to the IN and GND pins as possible. Add several vias with 18mil and 8mil hole diameters under the device and near the input capacitors to help dissipate heat and to reduce parasitic inductances.
4. Place a decoupling capacitor as close to the VCC and AGND pins as possible.
5. Keep the switching node (SW) plane as small as possible and far away from the feedback network.
6. Place the external feedback resistors next to the FB pin. Make sure that there are no vias on the FB trace. The feedback resistors should refer to AGND instead of PGND.
7. Keep the BST voltage path (BST, C3, and SW) as short as possible.
8. MPS strongly recommends a four-layer layout to improve thermal performance.

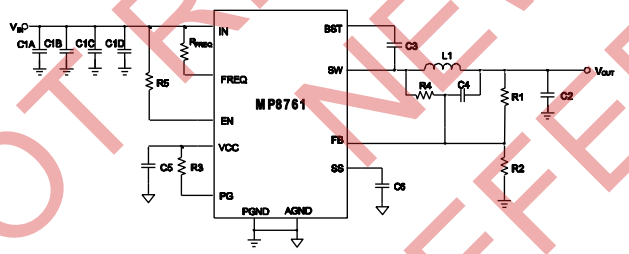
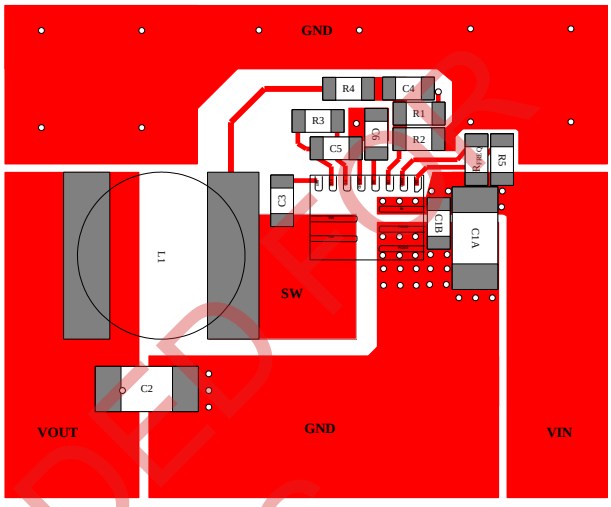
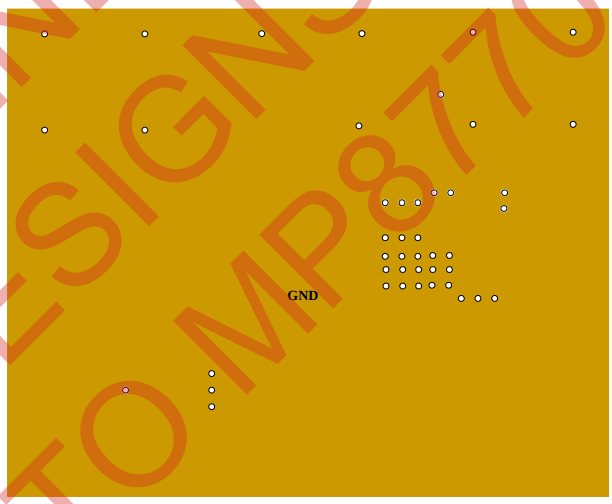


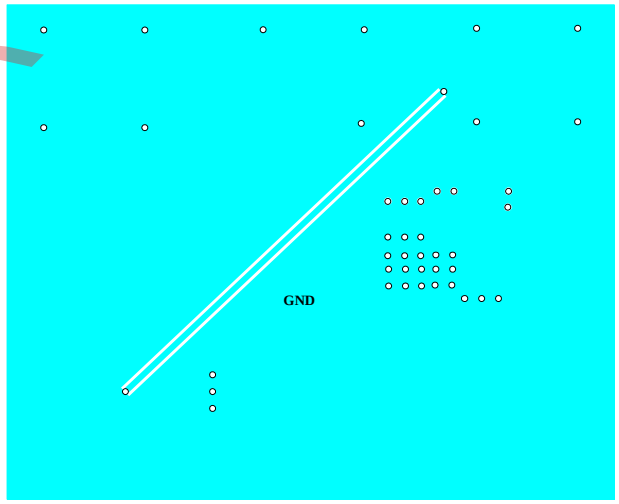
Figure 13: Schematic Reference for PCB Layout



Top Layer



Inner1 Layer



Inner2 Layer

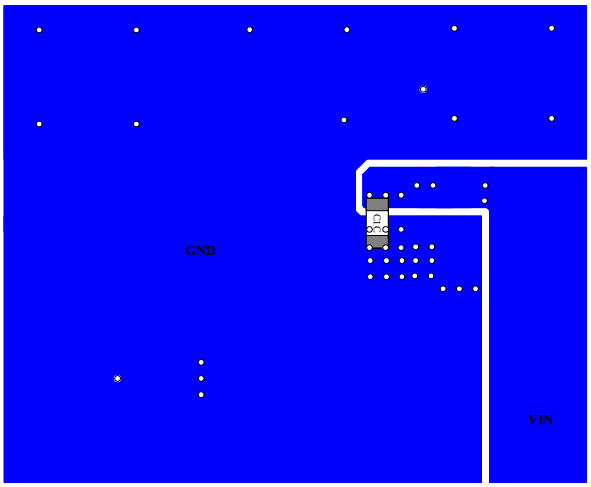
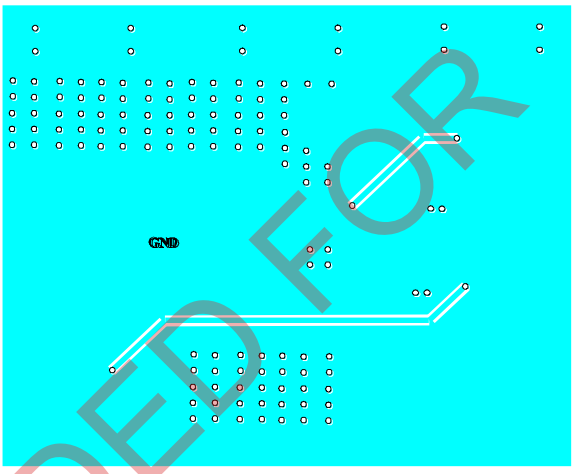
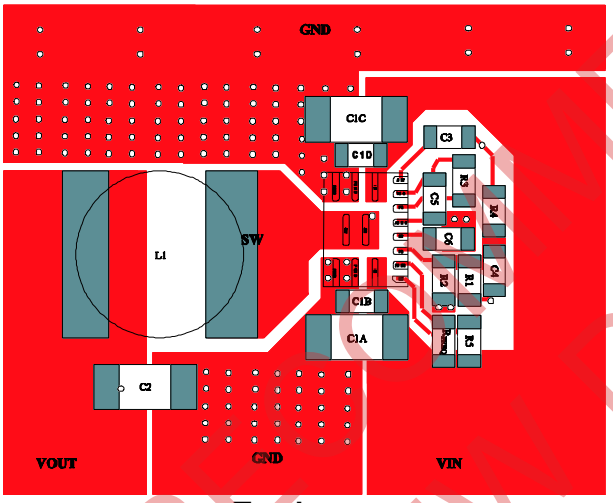


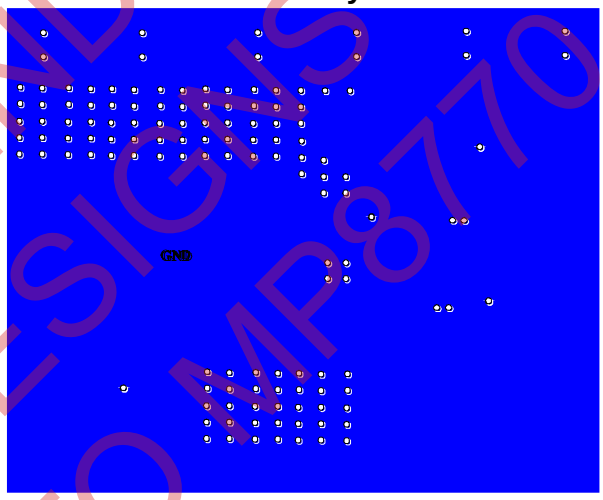
Figure 14: Bottom Layer, 13-Pin PFN MP8761 PCB Layout Guide



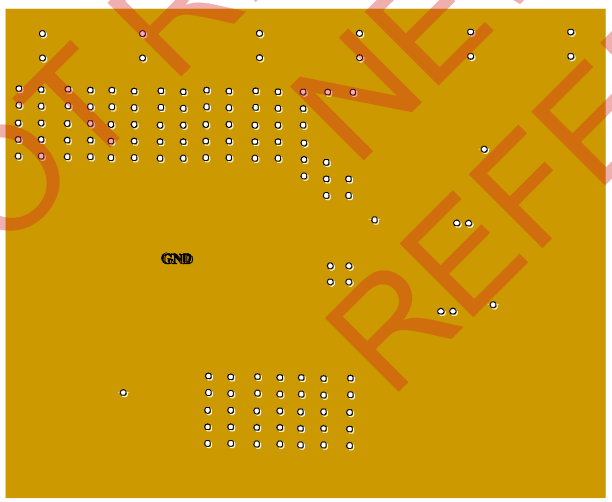
Inner2 Layer



Top Layer



Bottom Layer



Inner1 Layer

Figure 15—PCB Layout Guide for MP8761GLE (16-Pin QFN)

Design Example

Table 4 lists the specifications for a design example that follows the application guidelines:

Table 4: Design Example

V_{IN}	12V
V_{OUT}	1V
F_{SW}	500kHz

The detailed application schematic is shown in Figure 16. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheet.

TYPICAL APPLICATION

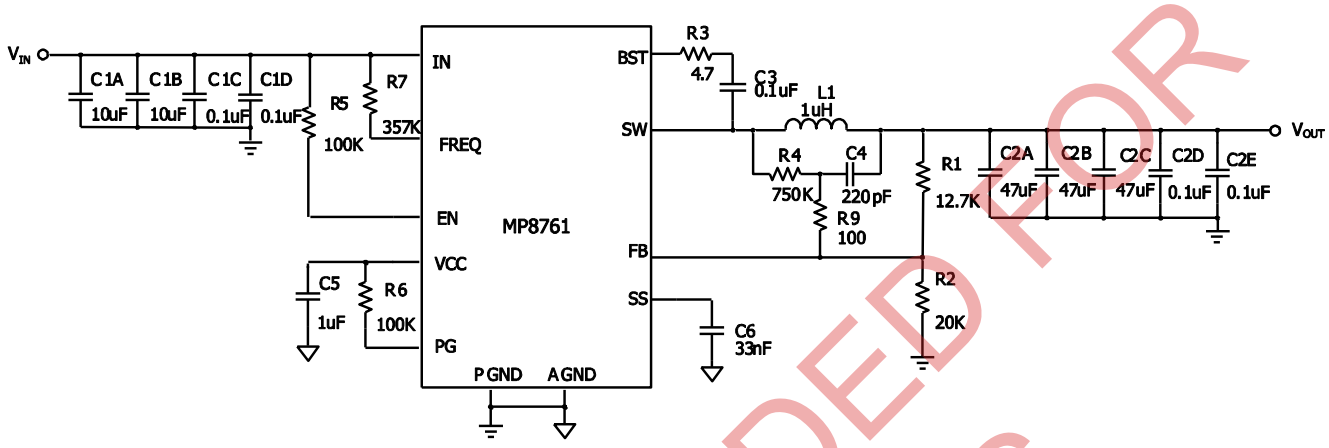
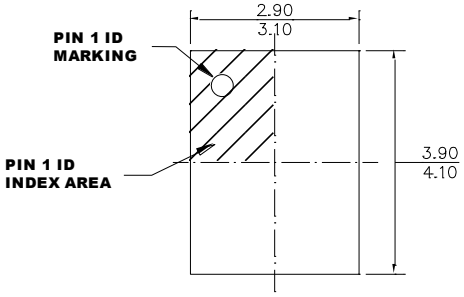


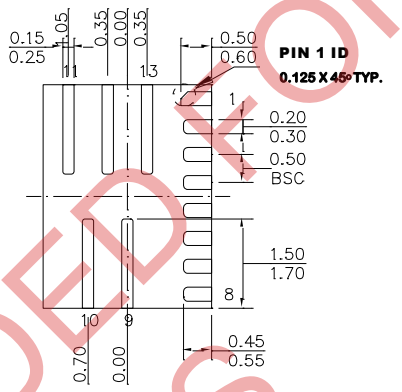
Figure 16—Typical Application Circuit with Low ESR Ceramic Capacitor for 1V Output

PACKAGE INFORMATION

13-Pin QFN (3×4mm)

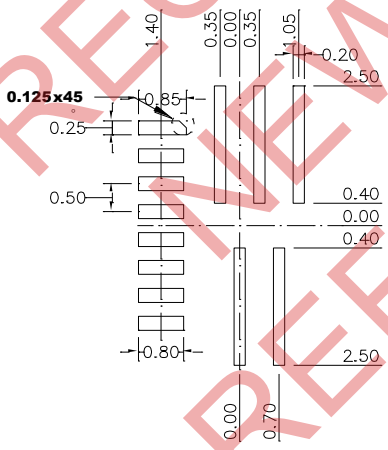


TOP VIEW



BOTTOM VIEW

SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.