

MPC8313E

PowerQUICC II Pro Processor

Hardware Specifications

This document provides an overview of the MPC8313E PowerQUICC™ II Pro processor features, including a block diagram showing the major functional components. The MPC8313E is a cost-effective, low-power, highly integrated host processor that addresses the requirements of several printing and imaging, consumer, and industrial applications, including main CPUs and I/O processors in printing systems, networking switches and line cards, wireless LANs (WLANs), network access servers (NAS), VPN routers, intelligent NIC, and industrial controllers. The MPC8313E extends the PowerQUICC™ family, adding higher CPU performance, additional functionality, and faster interfaces while addressing the requirements related to time-to-market, price, power consumption, and package size.

NOTE

The information in this document is accurate for revisions 1.0, 2.x, and later. See [Section 23.1, “Part Numbers Fully Addressed by this Document.”](#)

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1 Overview

The MPC8313E incorporates the e300c3 core, which includes 16 Kbytes of L1 instruction and data caches and on-chip memory management units (MMUs). The MPC8313E has interfaces to dual enhanced three-speed 10/100/1000 Mbps Ethernet controllers, a DDR1/DDR2 SDRAM memory controller, an enhanced local bus controller, a 32-bit PCI controller, a dedicated security engine, a USB 2.0 dual-role controller and an on-chip high-speed PHY, a programmable interrupt controller, dual I²C controllers, a 4-channel DMA controller, and a general-purpose I/O port. This figure shows a block diagram of the MPC8313E.

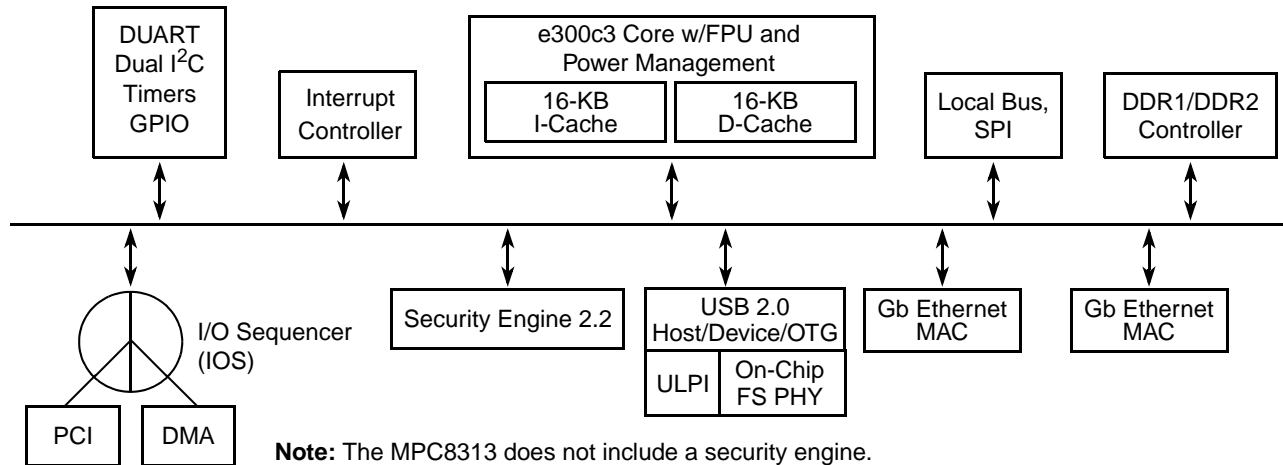


Figure 1. MPC8313E Block Diagram

The MPC8313E security engine (SEC 2.2) allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, AES, SHA-1, and MD-5 algorithms.

1.1 MPC8313E Features

The following features are supported in the MPC8313E:

- Embedded PowerPC™ e300 processor core built on Power Architecture™ technology; operates at up to 333 MHz.
- High-performance, low-power, and cost-effective host processor
- DDR1/DDR2 memory controller—one 16-/32-bit interface at up to 333 MHz supporting both DDR1 and DDR2
- 16-Kbyte instruction cache and 16-Kbyte data cache, a floating point unit, and two integer units
- Peripheral interfaces such as 32-bit PCI interface with up to 66-MHz operation, 16-bit enhanced local bus interface with up to 66-MHz operation, and USB 2.0 (high speed) with an on-chip PHY.
- Security engine provides acceleration for control and data plane security protocols
- Power management controller for low-power consumption
- High degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration

1.2 Serial Interfaces

The following interfaces are supported in the MPC8313E: dual UART, dual I²C, and an SPI interface.

1.3 Security Engine

The security engine is optimized to handle all the algorithms associated with IPSec, IEEE Std 802.11i®, and iSCSI. The security engine contains one crypto-channel, a controller, and a set of crypto execution units (EUs). The execution units are as follows:

- Data encryption standard execution unit (DEU), supporting DES and 3DES
- Advanced encryption standard unit (AESU), supporting AES
- Message digest execution unit (MDEU), supporting MD5, SHA1, SHA-224, SHA-256, and HMAC with any algorithm
- One crypto-channel supporting multi-command descriptor chains

1.4 DDR Memory Controller

The MPC8313E DDR1/DDR2 memory controller includes the following features:

- Single 16- or 32-bit interface supporting both DDR1 and DDR2 SDRAM
- Support for up to 333 MHz
- Support for two physical banks (chip selects), each bank independently addressable
- 64-Mbit to 2-Gbit (for DDR1) and to 4-Gbit (for DDR2) devices with x8/x16/x32 data ports (no direct x4 support)
- Support for one 16-bit device or two 8-bit devices on a 16-bit bus, or one 32-bit device or two 16-bit devices on a 32-bit bus
- Support for up to 16 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 1.8-/2.5-V SSTL2 compatible I/O

1.5 PCI Controller

The MPC8313E PCI controller includes the following features:

- PCI specification revision 2.3 compatible
- Single 32-bit data PCI interface operates at up to 66 MHz
- PCI 3.3-V compatible (not 5-V compatible)
- Support for host and agent modes
- On-chip arbitration, supporting three external masters on PCI
- Selectable hardware-enforced coherency

1.6 USB Dual-Role Controller

The MPC8313E USB controller includes the following features:

- Supports USB on-the-go mode, which includes both device and host functionality, when using an external ULPI (UTMI + low-pin interface) PHY
- Compatible with *Universal Serial Bus Specification, Rev. 2.0*
- Supports operation as a stand-alone USB device
 - Supports one upstream facing port
 - Supports three programmable USB endpoints
- Supports operation as a stand-alone USB host controller
 - Supports USB root hub with one downstream-facing port
 - Enhanced host controller interface (EHCI) compatible
- Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operation. Low-speed operation is supported only in host mode.
- Supports UTMI + low pin interface (ULPI) or on-chip USB 2.0 full-speed/high-speed PHY

1.7 Dual Enhanced Three-Speed Ethernet Controllers (eTSECs)

The MPC8313E eTSECs include the following features:

- Two RGMII/SGMII/MII/RMII/RTBI interfaces
- Two controllers designed to comply with IEEE Std 802.3®, 802.3u®, 802.3x®, 802.3z®, 802.3au®, and 802.3ab®
- Support for Wake-on-Magic Packet™, a method to bring the device from standby to full operating mode
- MII management interface for external PHY control and status
- Three-speed support (10/100/1000 Mbps)
- On-chip high-speed serial interface to external SGMII PHY interface
- Support for IEEE Std 1588™
- Support for two full-duplex FIFO interface modes
- Multiple PHY interface configuration
- TCP/IP acceleration and QoS features available
- IP v4 and IP v6 header recognition on receive
- IP v4 header checksum verification and generation
- TCP and UDP checksum verification and generation
- Per-packet configurable acceleration
- Recognition of VLAN, stacked (queue in queue) VLAN, IEEE Std 802.2®, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
- Transmission from up to eight physical queues.
- Reception to up to eight physical queues



- Full and half-duplex Ethernet support (1000 Mbps supports only full-duplex):
 - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
 - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE 802.1 virtual local area network (VLAN) tags and priority
 - VLAN insertion and deletion
 - Per-frame VLAN control word or default VLAN for each eTSEC
 - Extracted VLAN control word passed to software separately
 - Retransmission following a collision
 - CRC generation and verification of inbound/outbound packets
 - Programmable Ethernet preamble insertion and extraction of up to 7 bytes
- MAC address recognition:
 - Exact match on primary and virtual 48-bit unicast addresses
 - VRRP and HSRP support for seamless router fail-over
 - Up to 16 exact-match MAC addresses supported
 - Broadcast address (accept/reject)
 - Hash table match on up to 512 multicast addresses
 - Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- MII management interface for control and status

1.8 Programmable Interrupt Controller (PIC)

The programmable interrupt controller (PIC) implements the necessary functions to provide a flexible solution for general-purpose interrupt control. The PIC programming model supports 5 external and 34 internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.

1.9 Power Management Controller (PMC)

The MPC8313E power management controller includes the following features:

- Provides power management when the device is used in both host and agent modes
- Supports PCI power management 1.2 D0, D1, D2, D3hot, and D3cold states
- On-chip split power supply controlled through external power switch for minimum standby power
- Support for PME generation in PCI agent mode, PME detection in PCI host mode
- Supports wake-up from Ethernet (Magic Packet), USB, GPIO, and PCI (PME input as host)

1.10 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) allows the MPC8313E to exchange data between other PowerQUICC family chips, Ethernet PHYs for configuration, and peripheral devices such as EEPROMs, real-time clocks, A/D converters, and ISDN devices.

The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (receive, transmit, clock, and slave select). The SPI block consists of transmitter and receiver sections, an independent baud-rate generator, and a control unit.

1.11 DMA Controller, Dual I²C, DUART, Local Bus Controller, and Timers

The MPC8313E provides an integrated four-channel DMA controller with the following features:

- Allows chaining (both extended and direct) through local memory-mapped chain descriptors (accessible by local masters)
- Supports misaligned transfers

There are two I²C controllers. These synchronous, multi-master buses can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. The 16-byte FIFOs are supported for both the transmitter and the receiver.

The MPC8313E local bus controller (LBC) port allows connections with a wide variety of external DSPs and ASICs. Three separate state machines share the same external pins and can be programmed separately to access different types of devices. The general-purpose chip select machine (GPCM) controls accesses to asynchronous devices using a simple handshake protocol. The three user programmable machines (UPMs) can be programmed to interface to synchronous devices or custom ASIC interfaces. Each chip select can be configured so that the associated chip interface can be controlled by the GPCM or UPM controller. The FCM provides a glueless interface to parallel-bus NAND Flash E2PROM devices. The FCM contains three basic configuration register groups—BR n , OR n , and FMR. Both may exist in the same system. The local bus can operate at up to 66 MHz.

The MPC8313E system timers include the following features: periodic interrupt timer, real time clock, software watchdog timer, and two general-purpose timer blocks.

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8313E. The MPC8313E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings¹

| Characteristic | | Symbol | Max Value | Unit | Note |
|--|--|---------------------|--|------|------|
| Core supply voltage | | V_{DD} | -0.3 to 1.26 | V | — |
| PLL supply voltage | | AV_{DD} | -0.3 to 1.26 | V | — |
| Core power supply for SerDes transceivers | | $XCOREV_{DD}$ | -0.3 to 1.26 | V | — |
| Pad power supply for SerDes transceivers | | $XPADV_{DD}$ | -0.3 to 1.26 | V | — |
| DDR and DDR2 DRAM I/O voltage | | GV_{DD} | -0.3 to 2.75 -0.3 to 1.98 | V | — |
| PCI, local bus, DUART, system control and power management, I ² C, and JTAG I/O voltage | | NV_{DD}/LV_{DD} | -0.3 to 3.6 | V | — |
| eTSEC, USB | | LV_{DDA}/LV_{DDB} | -0.3 to 3.6 | V | — |
| Input voltage | DDR DRAM signals | MV_{IN} | -0.3 to ($GV_{DD} + 0.3$) | V | 2, 5 |
| | DDR DRAM reference | MV_{REF} | -0.3 to ($GV_{DD} + 0.3$) | V | 2, 5 |
| | Enhanced three-speed Ethernet signals | LV_{IN} | -0.3 to ($LV_{DDA} + 0.3$) or -0.3 to ($LV_{DDB} + 0.3$) | V | 4, 5 |
| | Local bus, DUART, SYS_CLK_IN, system control, and power management, I ² C, and JTAG signals | NV_{IN} | -0.3 to ($NV_{DD} + 0.3$) | V | 3, 5 |
| | PCI | NV_{IN} | -0.3 to ($NV_{DD} + 0.3$) | V | 6 |
| Storage temperature range | | T_{STG} | -55 to 150 | °C | — |

Notes:

- Functional and tested operating conditions are given in [Table 2](#). Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- Caution:** NV_{IN} must not exceed NV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- Caution:** LV_{IN} must not exceed LV_{DDA}/LV_{DDB} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

2.1.2 Power Supply Voltage Specification

This table provides the recommended operating conditions for the MPC8313E. Note that the values in this table are the recommended and tested operating conditions. If a particular block is given a voltage falling within the range in the Recommended Value column, the MPC8313E is capable of delivering the amount of current listed in the Current Requirement column; this is the maximum current possible. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

| Characteristic | Symbol | Recommended Value ¹ | Unit | Current Requirement |
|---|-------------------------|---|------|---------------------|
| Core supply voltage | V_{DD} | 1.0 V \pm 50 mV | V | 469 mA |
| Internal core logic constant power | V_{DDC} | 1.0 V \pm 50 mV | V | 377 mA |
| SerDes internal digital power | $XCOREV_{DD}$ | 1.0 | V | 170 mA |
| SerDes internal digital ground | $XCOREV_{SS}$ | 0.0 | V | — |
| SerDes I/O digital power | $XPADV_{DD}$ | 1.0 | V | 10 mA |
| SerDes I/O digital ground | $XPADV_{SS}$ | 0.0 | V | — |
| SerDes analog power for PLL | $SDAV_{DD}$ | 1.0 V \pm 50 mV | V | 10 mA |
| SerDes analog ground for PLL | $SDAV_{SS}$ | 0.0 | V | — |
| Dedicated 3.3 V analog power for USB PLL | USB_PLL_PWR3 | 3.3 V \pm 300 mV | V | 2–3 mA |
| Dedicated 1.0 V analog power for USB PLL | USB_PLL_PWR1 | 1.0 V \pm 50 mV | V | 2–3 mA |
| Dedicated analog ground for USB PLL | USB_PLL_GND | 0.0 | V | — |
| Dedicated USB power for USB bias circuit | USB_VDDA_BIAS | 3.3 V \pm 300 mV | V | 4–5 mA |
| Dedicated USB ground for USB bias circuit | USB_VSSA_BIAS | 0.0 | V | — |
| Dedicated power for USB transceiver | USB_VDDA | 3.3 V \pm 300 mV | V | 75 mA |
| Dedicated ground for USB transceiver | USB_VSSA | 0.0 | V | — |
| Analog power for e300 core APLL | AV_{DD1} ⁶ | 1.0 V \pm 50 mV | V | 2–3 mA |
| Analog power for system APLL | AV_{DD2} ⁶ | 1.0 V \pm 50 mV | V | 2–3 mA |
| DDR1 DRAM I/O voltage (333 MHz, 32-bit operation) | GV_{DD} | 2.5 V \pm 125 mV | V | 131 mA |
| DDR2 DRAM I/O voltage (333 MHz, 32-bit operation) | GV_{DD} | 1.8 V \pm 80 mV | V | 140 mA |
| Differential reference voltage for DDR controller | MV_{REF} | 1/2 DDR supply ($0.49 \times GV_{DD}$ to $0.51 \times GV_{DD}$) | V | — |
| Standard I/O voltage | NV_{DD} | 3.3 V \pm 300 mV ² | V | 74 mA |
| eTSEC2 I/O supply | LV_{DDA} | 2.5 V \pm 125 mV/ 3.3 V \pm 300 mV | V | 22 mA |
| eTSEC1/USB DR I/O supply | LV_{DDB} | 2.5 V \pm 125 mV/ 3.3 V \pm 300 mV | V | 44 mA |
| Supply for eLBC IOs | LV_{DD} | 3.3 V \pm 300 mV | V | 16 mA |
| Analog and digital ground | V_{SS} | 0.0 | V | — |
| Junction temperature range | T_A/T_J ³ | 0 to 105 | °C | |

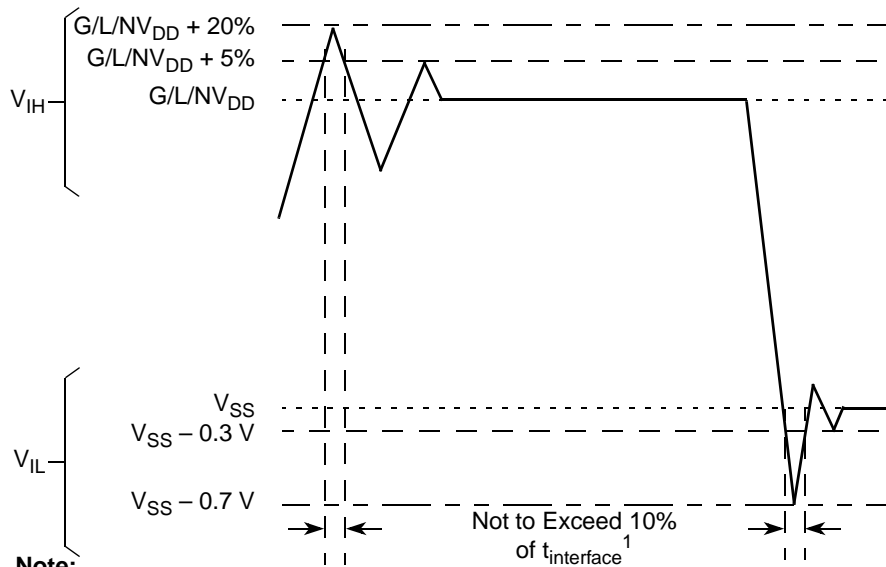
Table 2. Recommended Operating Conditions (continued)

| Characteristic | Symbol | Recommended Value ¹ | Unit | Current Requirement |
|----------------|--------|--------------------------------|------|---------------------|
|----------------|--------|--------------------------------|------|---------------------|

Note:

1. GV_{DD} , NV_{DD} , AV_{DD} , and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.
2. Some GPIO pins may operate from a 2.5-V supply when configured for other functions.
3. Min temperature is specified with T_A ; Max temperature is specified with T_J .
4. All Power rails must be connected and power applied to the MPC8313 even if the IP interfaces are not used.
5. All I/O pins should be interfaced with peripherals operating at same voltage level.
6. This voltage is the input to the filter discussed in [Section 22.2, “PLL Power Supply Filtering”](#) and not necessarily the voltage at the AVDD pin, which may be reduced from VDD by the filter.

This figure shows the undershoot and overshoot voltages at the interfaces of the MPC8313E.



Note:

1. Note that $t_{interface}$ refers to the clock period associated with the bus clock interface.

Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/NV_{DD}/LV_{DD}$

2.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths.

Table 3. Output Drive Capability

| Driver Type | Output Impedance (Ω) | Supply Voltage |
|---------------------------------------|-------------------------------|--------------------------|
| Local bus interface utilities signals | 42 | $NV_{DD} = 3.3\text{ V}$ |
| PCI signals | 25 | |
| DDR signal | 18 | $GV_{DD} = 2.5\text{ V}$ |

Table 3. Output Drive Capability (continued)

| Driver Type | Output Impedance (Ω) | Supply Voltage |
|--|-------------------------------|---|
| DDR2 signal | 18 | $GV_{DD} = 1.8\text{ V}$ |
| DUART, system control, I ² C, JTAG, SPI | 42 | $NV_{DD} = 3.3\text{ V}$ |
| GPIO signals | 42 | $NV_{DD} = 3.3\text{ V}$ |
| eTSEC signals | 42 | $LV_{DDA}, LV_{ddb} = 2.5/3.3\text{ V}$ |
| USB signals | 42 | $LV_{ddb} = 2.5/3.3\text{ V}$ |

2.2 Power Sequencing

The MPC8313E does not require the core supply voltage (V_{DD} and V_{DDC}) and I/O supply voltages (GV_{DD} , LV_{DD} , and NV_{DD}) to be applied in any particular order. Note that during power ramp-up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there might be a period of time that all input and output pins are actively driven and cause contention and excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD} and V_{DDC}) before the I/O voltage (GV_{DD} , LV_{DD} , and NV_{DD}) and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V; see Figure 3. Once both the power supplies (I/O voltage and core voltage) are stable, wait for a minimum of 32 clock cycles before negating $\overline{\text{PORESET}}$.

Note that there is no specific power down sequence requirement for the MPC8313E. I/O voltage supplies (GV_{DD} , LV_{DD} , and NV_{DD}) do not have any ordering requirements with respect to one another.

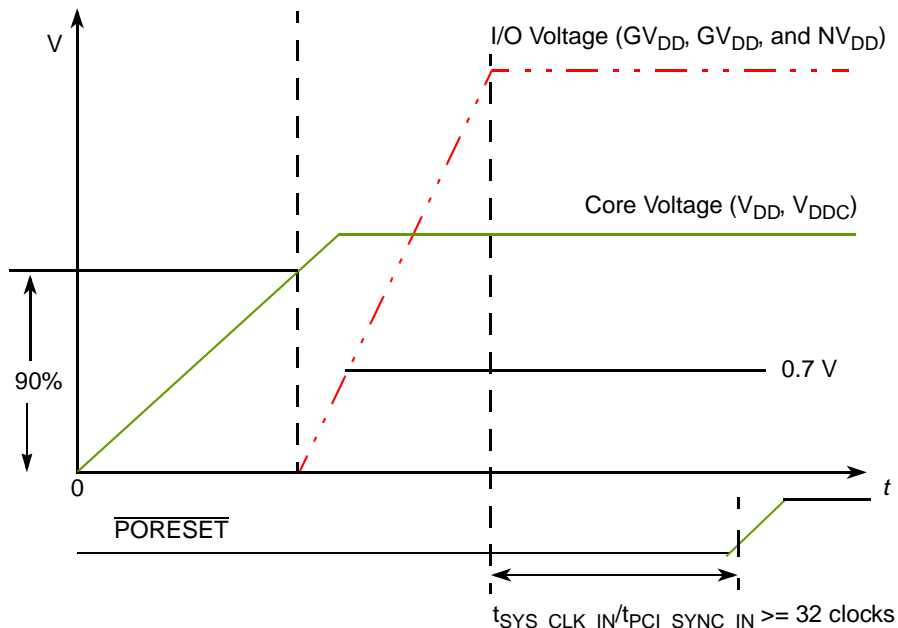


Figure 3. Power-Up Sequencing Example

3 Power Characteristics

The estimated typical power dissipation, not including I/O supply power, for this family of MPC8313E devices is shown in this table. [Table 5](#) shows the estimated typical I/O power dissipation.

Table 4. MPC8313E Power Dissipation¹

| Core Frequency (MHz) | CSB Frequency (MHz) | Typical ² | Maximum for Rev. 1.0 Silicon ³ | Maximum for Rev. 2.x or Later Silicon ³ | Unit |
|----------------------|---------------------|----------------------|---|--|------|
| 333 | 167 | 820 | 1020 | 1200 | mW |
| 400 | 133 | 820 | 1020 | 1200 | mW |

Note:

1. The values do not include I/O supply power or AV_{DD} , but do include core, USB PLL, and a portion of SerDes digital power (not including $XCOREV_{DD}$, $XPADV_{DD}$, or $SDAV_{DD}$, which all have dedicated power supplies for the SerDes PHY).
2. Typical power is based on a voltage of $V_{DD} = 1.05$ V and an artificial smoker test running at room temperature.
3. Maximum power is based on a voltage of $V_{DD} = 1.05$ V, a junction temperature of $T_J = 105^\circ\text{C}$, and an artificial smoker test.

This table describes a typical scenario where blocks with the stated percentage of utilization and impedances consume the amount of power described.

Table 5. MPC8313E Typical I/O Power Dissipation

| Interface | Parameter | GV_{DD} (1.8 V) | GV_{DD} (2.5 V) | NV_{DD} (3.3 V) | $LV_{DDA}/$ LV_{DDB} (3.3 V) | $LV_{DDA}/$ LV_{DDB} (2.5 V) | LV_{DD} (3.3 V) | Unit | Comments |
|---|---------------------|----------------------|----------------------|----------------------|--------------------------------------|--------------------------------------|----------------------|------|--|
| DDR 1, 60% utilization, 50% read/write $R_s = 22 \Omega$ $R_t = 50 \Omega$ single pair of clock capacitive load: data = 8 pF, control address = 8 pF, clock = 8 pF | 333 MHz, 32 bits | — | 0.355 | — | — | — | — | W | — |
| | 266 MHz, 32 bits | — | 0.323 | — | — | — | — | W | — |
| DDR 2, 60% utilization, 50% read/write $R_s = 22 \Omega$ $R_t = 75 \Omega$ single pair of clock capacitive load: data = 8 pF, control address = 8 pF, clock = 8 pF | 333 MHz, 32 bits | 0.266 | — | — | — | — | — | W | — |
| | 266 MHz, 32 bits | 0.246 | — | — | — | — | — | W | — |
| PCI I/O load = 50 pF | 33 MHz | — | — | 0.120 | — | — | — | W | — |
| | 66 MHz | — | — | 0.249 | — | — | — | W | — |
| Local bus I/O load = 20 pF | 66 MHz | — | — | — | — | — | 0.056 | W | — |
| | 50 MHz | — | — | — | — | — | 0.040 | W | — |
| TSEC I/O load = 20 pF | MII, 25 MHz | — | — | — | 0.008 | — | — | W | Multiple by number of interface used |
| | RGMII, 125 MHz | — | — | — | 0.078 | 0.044 | — | W | |

Table 5. MPC8313E Typical I/O Power Dissipation (continued)

| Interface | Parameter | GV _{DD} (1.8 V) | GV _{DD} (2.5 V) | NV _{DD} (3.3 V) | LV _{DDA} / LV _{DDB} (3.3 V) | LV _{DDA} / LV _{DDB} (2.5 V) | LV _{DD} (3.3 V) | Unit | Comments |
|-------------------------------|-----------|-----------------------------|-----------------------------|-----------------------------|---|---|-----------------------------|------|----------|
| USBDR controller load = 20 pF | 60 MHz | — | — | — | 0.078 | — | — | W | — |
| Other I/O | — | — | — | 0.015 | — | — | — | W | — |

This table shows the estimated core power dissipation of the MPC8313E while transitioning into the D3 warm low-power state.

Table 6. MPC8313E Low-Power Modes Power Dissipation¹

| 333-MHz Core, 167-MHz CSB ² | Rev. 1.0 ³ | Rev. 2.x or Later ³ | Unit |
|--|-----------------------|--------------------------------|------|
| D3 warm | 400 | 425 | mW |

Note:

1. All interfaces are enabled. For further power savings, disable the clocks to unused blocks.
2. The interfaces are run at the following frequencies: DDR: 333 MHz, eLBC 83 MHz, PCI 33 MHz, eTSEC1 and TSEC2: 167 MHz, SEC: 167 MHz, USB: 167 MHz. See the SCCR register for more information.
3. This is maximum power in D3 Warm based on a voltage of 1.05 V and a junction temperature of 105°C.

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8313E.

4.1 DC Electrical Characteristics

This table provides the system clock input (SYS_CLK_IN/PCI_SYNC_IN) DC timing specifications for the MPC8313E.

Table 7. SYS_CLK_IN DC Electrical Characteristics

| Parameter | Condition | Symbol | Min | Max | Unit |
|---------------------------|--|-----------------|------|------------------------|------|
| Input high voltage | — | V _{IH} | 2.4 | NV _{DD} + 0.3 | V |
| Input low voltage | — | V _{IL} | -0.3 | 0.4 | V |
| SYS_CLK_IN input current | 0 V ≤ V _{IN} ≤ NV _{DD} | I _{IN} | — | ±10 | μA |
| PCI_SYNC_IN input current | 0 V ≤ V _{IN} ≤ 0.5 V or NV _{DD} - 0.5 V ≤ V _{IN} ≤ NV _{DD} | I _{IN} | — | ±10 | μA |
| PCI_SYNC_IN input current | 0.5 V ≤ V _{IN} ≤ NV _{DD} - 0.5 V | I _{IN} | — | ±50 | μA |

4.2 AC Electrical Characteristics

The primary clock source for the MPC8313E can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. This table provides the system clock input (SYS_CLK_IN/PCI_CLK) AC timing specifications for the MPC8313E.

Table 8. SYS_CLK_IN AC Timing Specifications

| Parameter/Condition | Symbol | Min | Typ | Max | Unit | Note |
|-------------------------------|--|-----|-----|-------|------|------|
| SYS_CLK_IN/PCI_CLK frequency | $f_{\text{SYS_CLK_IN}}$ | 24 | — | 66.67 | MHz | 1 |
| SYS_CLK_IN/PCI_CLK cycle time | $t_{\text{SYS_CLK_IN}}$ | 15 | — | — | ns | — |
| SYS_CLK_IN rise and fall time | $t_{\text{KH}}, t_{\text{KL}}$ | 0.6 | 0.8 | 4 | ns | 2 |
| PCI_CLK rise and fall time | $t_{\text{PCH}}, t_{\text{PCL}}$ | 0.6 | 0.8 | 1.2 | ns | 2 |
| SYS_CLK_IN/PCI_CLK duty cycle | $t_{\text{KHK}}/t_{\text{SYS_CLK_IN}}$ | 40 | — | 60 | % | 3 |
| SYS_CLK_IN/PCI_CLK jitter | — | — | — | ±150 | ps | 4, 5 |

Notes:

- Caution:** The system, core, security block must not exceed their respective maximum or minimum operating frequencies.
- Rise and fall times for SYS_CLK_IN/PCI_CLK are measured at 0.4 and 2.4 V.
- Timing is guaranteed by design and characterization.
- This represents the total input jitter—short term and long term—and is guaranteed by design.
- The SYS_CLK_IN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYS_CLK_IN drivers with the specified jitter.

5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8313E.

5.1 RESET DC Electrical Characteristics

This table provides the DC electrical characteristics for the RESET pins.

Table 9. RESET Pins DC Electrical Characteristics

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---------------------|-----------------|--|------|------------------------|------|
| Input high voltage | V_{IH} | — | 2.1 | $NV_{\text{DD}} + 0.3$ | V |
| Input low voltage | V_{IL} | — | -0.3 | 0.8 | V |
| Input current | I_{IN} | $0 \text{ V} \leq V_{\text{IN}} \leq NV_{\text{DD}}$ | — | ±5 | μA |
| Output high voltage | V_{OH} | $I_{\text{OH}} = -8.0 \text{ mA}$ | 2.4 | — | V |
| Output low voltage | V_{OL} | $I_{\text{OL}} = 8.0 \text{ mA}$ | — | 0.5 | V |
| Output low voltage | V_{OL} | $I_{\text{OL}} = 3.2 \text{ mA}$ | — | 0.4 | V |

5.2 RESET AC Electrical Characteristics

This table provides the reset initialization AC timing specifications.

Table 10. RESET Initialization Timing Specifications

| Parameter/Condition | Min | Max | Unit | Note |
|---|-----|-----|----------------------------|------|
| Required assertion time of $\overline{\text{HRESET}}$ or $\overline{\text{SRESET}}$ (input) to activate reset flow | 32 | — | $t_{\text{PCI_SYNC_IN}}$ | 1 |
| Required assertion time of $\overline{\text{PORESET}}$ with stable clock and power applied to SYS_CLK_IN when the device is in PCI host mode | 32 | — | $t_{\text{SYS_CLK_IN}}$ | 2 |
| Required assertion time of $\overline{\text{PORESET}}$ with stable clock and power applied to PCI_SYNC_IN when the device is in PCI agent mode | 32 | — | $t_{\text{PCI_SYNC_IN}}$ | 1 |
| $\overline{\text{HRESET}}$ assertion (output) | 512 | — | $t_{\text{PCI_SYNC_IN}}$ | 1 |
| Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:3] and CFG_CLK_IN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI host mode | 4 | — | $t_{\text{SYS_CLK_IN}}$ | 2 |
| Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI agent mode | 4 | — | $t_{\text{PCI_SYNC_IN}}$ | 1 |
| Input hold time for POR configuration signals with respect to negation of $\overline{\text{HRESET}}$ | 0 | — | ns | — |
| Time for the device to turn off POR configuration signal drivers with respect to the assertion of $\overline{\text{HRESET}}$ | — | 4 | ns | 3 |
| Time for the device to turn on POR configuration signal drivers with respect to the negation of $\overline{\text{HRESET}}$ | 1 | — | $t_{\text{PCI_SYNC_IN}}$ | 1, 3 |

Notes:

- $t_{\text{PCI_SYNC_IN}}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the device is in PCI host mode the primary clock is applied to the SYS_CLK_IN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV.
- $t_{\text{SYS_CLK_IN}}$ is the clock period of the input clock applied to SYS_CLK_IN. It is only valid when the device is in PCI host mode.
- POR configuration signals consists of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

This table provides the PLL lock times.

Table 11. PLL Lock Times

| Parameter/Condition | Min | Max | Unit | Note |
|---------------------|-----|-----|---------------|------|
| PLL lock times | — | 100 | μs | — |

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface. Note that DDR SDRAM is $G_{V_{\text{DD}}}(\text{typ}) = 2.5 \text{ V}$ and DDR2 SDRAM is $G_{V_{\text{DD}}}(\text{typ}) = 1.8 \text{ V}$.

6.1 DDR and DDR2 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR2 SDRAM component(s) when $GV_{DD}(typ) = 1.8\text{ V}$.

Table 12. DDR2 SDRAM DC Electrical Characteristics for $GV_{DD}(typ) = 1.8\text{ V}$

| Parameter/Condition | Symbol | Min | Max | Unit | Note |
|--|------------|-----------------------|-----------------------|---------------|------|
| I/O supply voltage | GV_{DD} | 1.7 | 1.9 | V | 1 |
| I/O reference voltage | MV_{REF} | $0.49 \times GV_{DD}$ | $0.51 \times GV_{DD}$ | V | 2 |
| I/O termination voltage | V_{TT} | $MV_{REF} - 0.04$ | $MV_{REF} + 0.04$ | V | 3 |
| Input high voltage | V_{IH} | $MV_{REF} + 0.125$ | $GV_{DD} + 0.3$ | V | — |
| Input low voltage | V_{IL} | -0.3 | $MV_{REF} - 0.125$ | V | — |
| Output leakage current | I_{OZ} | -9.9 | 9.9 | μA | 4 |
| Output high current ($V_{OUT} = 1.420\text{ V}$) | I_{OH} | -13.4 | — | mA | — |
| Output low current ($V_{OUT} = 0.280\text{ V}$) | I_{OL} | 13.4 | — | mA | — |

Notes:

- GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
- MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed $\pm 2\%$ of the DC value.
- V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF} . This rail should track variations in the DC level of MV_{REF} .
- Output leakage is measured with all outputs disabled, $0\text{ V} \leq V_{OUT} \leq GV_{DD}$.

This table provides the DDR2 capacitance when $GV_{DD}(typ) = 1.8\text{ V}$.

Table 13. DDR2 SDRAM Capacitance for $GV_{DD}(typ) = 1.8\text{ V}$

| Parameter/Condition | Symbol | Min | Max | Unit | Note |
|--|-----------|-----|-----|------|------|
| Input/output capacitance: DQ, DQS, $\overline{\text{DQS}}$ | C_{IO} | 6 | 8 | pF | 1 |
| Delta input/output capacitance: DQ, DQS, $\overline{\text{DQS}}$ | C_{DIO} | — | 0.5 | pF | 1 |

Note:

- This parameter is sampled. $GV_{DD} = 1.8\text{ V} \pm 0.090\text{ V}$, $f = 1\text{ MHz}$, $T_A = 25^\circ\text{C}$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the recommended operating conditions for the DDR SDRAM component(s) when $GV_{DD}(typ) = 2.5\text{ V}$.

Table 14. DDR SDRAM DC Electrical Characteristics for $GV_{DD}(typ) = 2.5\text{ V}$

| Parameter/Condition | Symbol | Min | Max | Unit | Note |
|-------------------------|------------|-----------------------|-----------------------|------|------|
| I/O supply voltage | GV_{DD} | 2.3 | 2.7 | V | 1 |
| I/O reference voltage | MV_{REF} | $0.49 \times GV_{DD}$ | $0.51 \times GV_{DD}$ | V | 2 |
| I/O termination voltage | V_{TT} | $MV_{REF} - 0.04$ | $MV_{REF} + 0.04$ | V | 3 |
| Input high voltage | V_{IH} | $MV_{REF} + 0.15$ | $GV_{DD} + 0.3$ | V | — |
| Input low voltage | V_{IL} | -0.3 | $MV_{REF} - 0.15$ | V | — |

Table 14. DDR SDRAM DC Electrical Characteristics for $GV_{DD}(typ) = 2.5\text{ V}$ (continued)

| Parameter/Condition | Symbol | Min | Max | Unit | Note |
|---|----------|-------|------|---------------|------|
| Output leakage current | I_{OZ} | -9.9 | -9.9 | μA | 4 |
| Output high current ($V_{OUT} = 1.95\text{ V}$) | I_{OH} | -16.2 | — | mA | — |
| Output low current ($V_{OUT} = 0.35\text{ V}$) | I_{OL} | 16.2 | — | mA | — |

Note:

- GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
- MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed $\pm 2\%$ of the DC value.
- V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF} . This rail should track variations in the DC level of MV_{REF} .
- Output leakage is measured with all outputs disabled, $0\text{ V} \leq V_{OUT} \leq GV_{DD}$.

This table provides the DDR capacitance when $GV_{DD}(typ) = 2.5\text{ V}$.

Table 15. DDR SDRAM Capacitance for $GV_{DD}(typ) = 2.5\text{ V}$

| Parameter/Condition | Symbol | Min | Max | Unit | Note |
|---|-----------|-----|-----|-------------|------|
| Input/output capacitance: DQ, DQS | C_{IO} | 6 | 8 | pF | 1 |
| Delta input/output capacitance: DQ, DQS | C_{DIO} | — | 0.5 | pF | 1 |

Note:

- This parameter is sampled. $GV_{DD} = 2.5\text{ V} \pm 0.125\text{ V}$, $f = 1\text{ MHz}$, $T_A = 25^\circ\text{C}$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the current draw characteristics for MV_{REF} .

Table 16. Current Draw Characteristics for MV_{REF}

| Parameter/Condition | Symbol | Min | Max | Unit | Note |
|-----------------------------|-------------|-----|-----|---------------|------|
| Current draw for MV_{REF} | I_{MVREF} | — | 500 | μA | 1 |

Note:

- The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.

6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR2 SDRAM when $GV_{DD}(typ) = 1.8\text{ V}$.

Table 17. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GV_{DD} of $1.8 \pm 5\%$.

| Parameter | Symbol | Min | Max | Unit | Note |
|-----------------------|----------|-------------------|-------------------|------|------|
| AC input low voltage | V_{IL} | — | $MV_{REF} - 0.25$ | V | — |
| AC input high voltage | V_{IH} | $MV_{REF} + 0.25$ | — | V | — |

This table provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(\text{typ}) = 2.5 \text{ V}$.

Table 18. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions with GV_{DD} of $2.5 \pm 5\%$.

| Parameter | Symbol | Min | Max | Unit | Note |
|-----------------------|----------|-------------------|-------------------|------|------|
| AC input low voltage | V_{IL} | — | $MV_{REF} - 0.31$ | V | — |
| AC input high voltage | V_{IH} | $MV_{REF} + 0.31$ | — | V | — |

This table provides the input AC timing specifications for the DDR2 SDRAM interface.

Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions, with GV_{DD} of $2.5 \pm 5\%$.

| Parameter | Symbol | Min | Max | Unit | Note |
|------------------------------|--------------|------|-----|------|------|
| Controller skew for MDQS—MDQ | t_{CISKEW} | — | — | ps | 1, 2 |
| 333 MHz | — | -750 | 750 | — | — |
| 266 MHz | — | -750 | 750 | — | — |

Notes:

- t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
- The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW} . This can be determined by the following equation: $t_{DISKEW} = \pm (T/4 - \text{abs}(t_{CISKEW}))$ where T is the clock period and $\text{abs}(t_{CISKEW})$ is the absolute value of t_{CISKEW} .

This figure illustrates the DDR input timing diagram showing the t_{DISKEW} timing parameter.

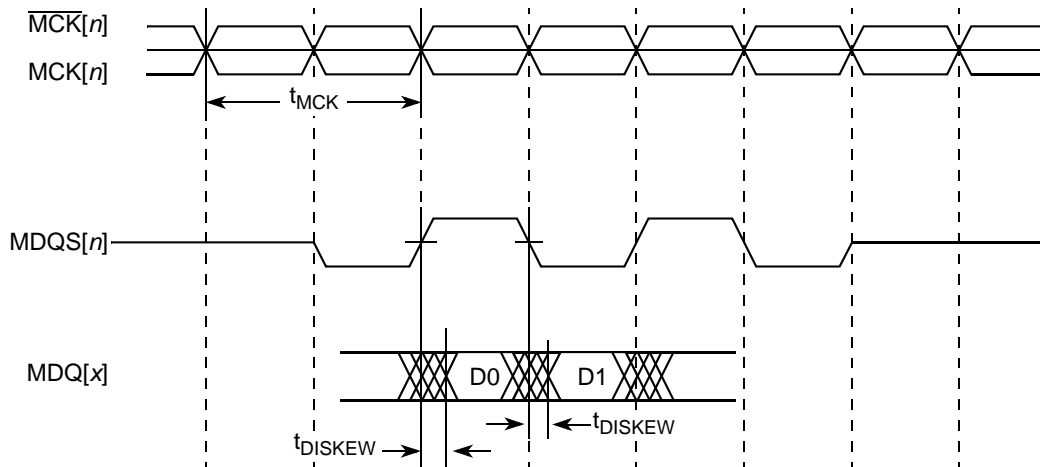


Figure 4. DDR Input Timing Diagram

6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications for Rev. 1.0 Silicon

| Parameter | Symbol ¹ | Min | Max | Unit | Note |
|---|--|------------------------------------|------------------------------------|------|------|
| MCK[n] cycle time, MCK[n]/ $\overline{\text{MCK}}[n]$ crossing | t_{MCK} | 6 | 10 | ns | 2 |
| ADDR/CMD output setup with respect to MCK 333 MHz 266 MHz | t_{DDKHAS} | 2.1 2.5 | — — | ns | 3 |
| ADDR/CMD output hold with respect to MCK 333 MHz 266 MHz | t_{DDKHAX} | 2.4 3.15 | — — | ns | 3 |
| $\overline{\text{MCS}}[n]$ output setup with respect to MCK 333 MHz 266 MHz | t_{DDKHCS} | 2.4 3.15 | — — | ns | 3 |
| $\overline{\text{MCS}}[n]$ output hold with respect to MCK 333 MHz 266 MHz | t_{DDKHGX} | 2.4 3.15 | — — | ns | 3 |
| MCK to MDQS Skew | t_{DDKMHM} | -0.6 | 0.6 | ns | 4 |
| MDQ/MDM output setup with respect to MDQS 333 MHz 266 MHz | t_{DDKHDS} , t_{DDKLDS} | 800 900 | — — | ps | 5 |
| MDQ/MDM output hold with respect to MDQS 333 MHz 266 MHz | t_{DDKHDX} , t_{DDKLDX} | 900 1100 | — — | ps | 5 |
| MDQS preamble start | t_{DDKHMP} | $-0.5 \times t_{\text{MCK}} - 0.6$ | $-0.5 \times t_{\text{MCK}} + 0.6$ | ns | 6 |
| MDQS epilogue end | t_{DDKHME} | -0.6 | 0.6 | ns | 6 |

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
- All MCK/ $\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ± 0.1 V.
- ADDR/CMD includes all DDR SDRAM output signals except MCK/ $\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MDM/MDQS.
- Note that t_{DDKMHM} follows the symbol conventions described in note 1. For example, t_{DDKMHM} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKMHM} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual*, for a description and understanding of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
- All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

Table 21. DDR and DDR2 SDRAM Output AC Timing Specifications for Silicon Rev 2.x or Later

| Parameter | Symbol ¹ | Min | Max | Unit | Note |
|---|--------------------------------|-----------------------------|-----------------------------|------|------|
| MCK[n] cycle time, MCK[n]/MCK[n] crossing | t_{MCK} | 6 | 10 | ns | 2 |
| ADDR/CMD output setup with respect to MCK 333 MHz 266 MHz | t_{DDKHAS} | 2.1 2.5 | — — | ns | 3 |
| ADDR/CMD output hold with respect to MCK 333 MHz 266 MHz | t_{DDKHAX} | 2.0 2.7 | — — | ns | 3 |
| MCS[n] output setup with respect to MCK 333 MHz 266 MHz | t_{DDKHCS} | 2.1 3.15 | — — | ns | 3 |
| MCS[n] output hold with respect to MCK 333 MHz 266 MHz | t_{DDKHCS} | 2.0 2.7 | — — | ns | 3 |
| MCK to MDQS Skew | t_{DDKMHM} | -0.6 | 0.6 | ns | 4 |
| MDQ/MDM output setup with respect to MDQS 333 MHz 266 MHz | t_{DDKHDS} , t_{DDKLDS} | 800 900 | — — | ps | 5 |
| MDQ/MDM output hold with respect to MDQS 333 MHz 266 MHz | t_{DDKHDX} , t_{DDKLDX} | 750 1000 | — — | ps | 5 |
| MDQS preamble start | t_{DDKHMP} | $-0.5 \times t_{MCK} - 0.6$ | $-0.5 \times t_{MCK} + 0.6$ | ns | 6 |
| MDQS epilogue end | t_{DDKHME} | -0.6 | 0.6 | ns | 6 |

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/MCK referenced measurements are made from the crossing of the two signals ± 0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ/MDM/MDQS.
4. Note that t_{DDKMHM} follows the symbol conventions described in note 1. For example, t_{DDKMHM} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKMHM} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual*, for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

NOTE

For the ADDR/CMD setup and hold specifications in [Table 21](#), it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.

This figure shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

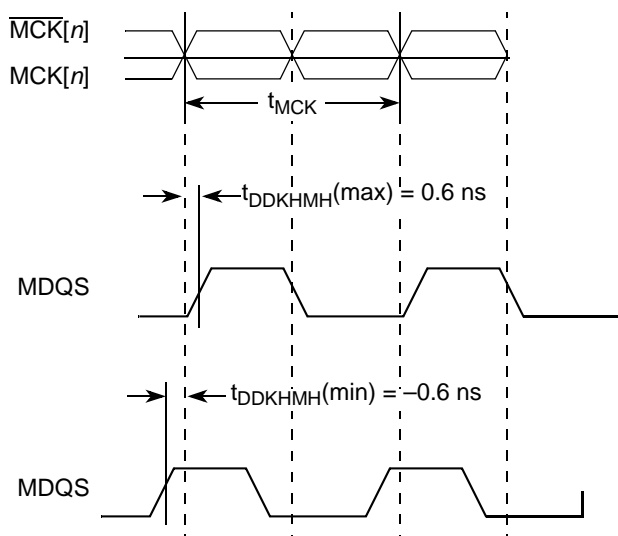


Figure 5. Timing Diagram for t_{DDKHMH}

This figure shows the DDR and DDR2 SDRAM output timing diagram.

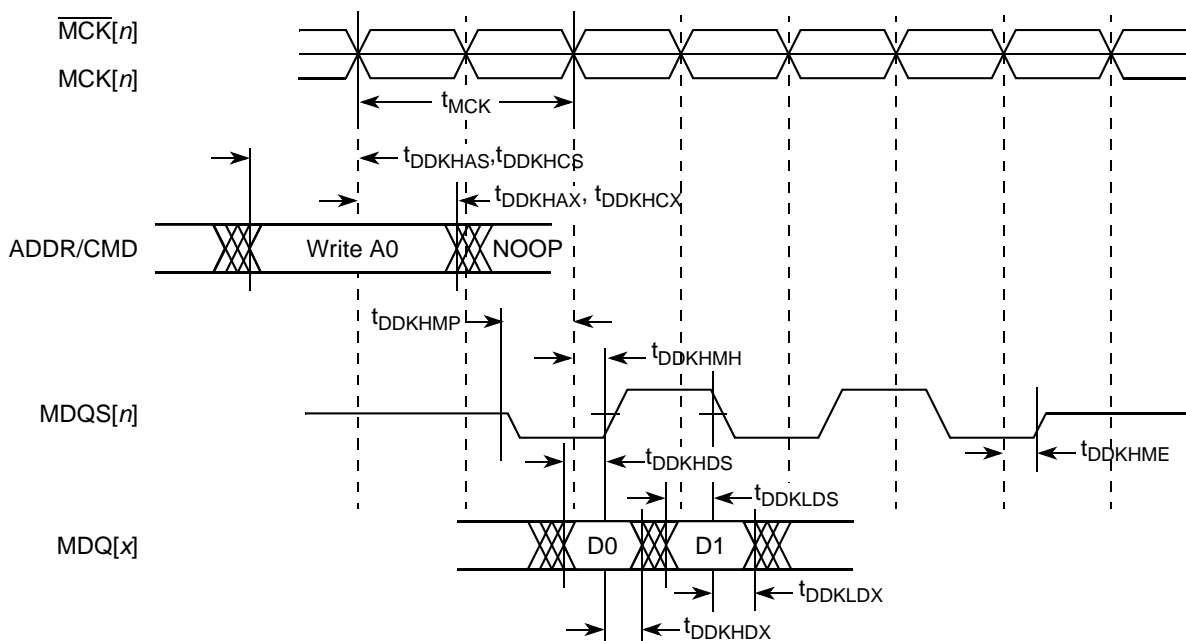


Figure 6. DDR and DDR2 SDRAM Output Timing Diagram

This figure provides the AC test load for the DDR bus.

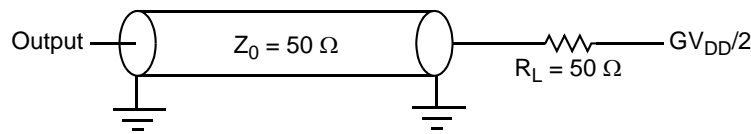


Figure 7. DDR AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface.

7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

Table 22. DUART DC Electrical Characteristics

| Parameter | Symbol | Min | Max | Unit |
|--|----------|-----------------|-----------------|---------|
| High-level input voltage | V_{IH} | 2.0 | $NV_{DD} + 0.3$ | V |
| Low-level input voltage NV_{DD} | V_{IL} | -0.3 | 0.8 | V |
| High-level output voltage, $I_{OH} = -100 \mu A$ | V_{OH} | $NV_{DD} - 0.2$ | — | V |
| Low-level output voltage, $I_{OL} = 100 \mu A$ | V_{OL} | — | 0.2 | V |
| Input current ($0 V \leq V_{IN} \leq NV_{DD}$) | I_{IN} | — | ± 5 | μA |

7.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

Table 23. DUART AC Timing Specifications

| Parameter | Value | Unit | Note |
|-------------------|-------------|------|------|
| Minimum baud rate | 256 | baud | — |
| Maximum baud rate | > 1,000,000 | baud | 1 |
| Oversample rate | 16 | — | 2 |

Notes:

1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all the media independent interface (MII), reduced gigabit media independent interface (RGMII), serial gigabit media independent interface (SGMII), and reduced ten-bit interface (RTBI) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5 V, while the MII interface can be operated at 3.3 V. The RMII and SGMII interfaces can be operated at either 3.3 or 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for *Gigabit Ethernet Physical Layer Device Specification Version 1.2a* (9/22/2000). The electrical characteristics for MDIO and MDC are specified in [Section 8.5, “Ethernet Management Interface Electrical Characteristics.”](#)

8.1.1 TSEC DC Electrical Characteristics

All RGMII, RMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in [Table 24](#) and [Table 25](#). The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

NOTE

eTSEC should be interfaced with peripheral operating at same voltage level.

Table 24. MII DC Electrical Characteristics

| Parameter | Symbol | Conditions | | Min | Max | Unit |
|----------------------|--------------------------------------|---|--|-----------------|--|------|
| Supply voltage 3.3 V | LV _{DDA} /LV _{DDB} | — | | 2.97 | 3.63 | V |
| Output high voltage | V _{OH} | I _{OH} = -4.0 mA | LV _{DDA} or LV _{DDB} = Min | 2.40 | LV _{DDA} + 0.3 or LV _{DDB} + 0.3 | V |
| Output low voltage | V _{OL} | I _{OL} = 4.0 mA | LV _{DDA} or LV _{DDB} = Min | V _{SS} | 0.50 | V |
| Input high voltage | V _{IH} | — | — | 2.0 | LV _{DDA} + 0.3 or LV _{DDB} + 0.3 | V |
| Input low voltage | V _{IL} | — | — | -0.3 | 0.90 | V |
| Input high current | I _{IH} | V _{IN} ¹ = LV _{DDA} or LV _{DDB} | | — | 40 | μA |
| Input low current | I _{IL} | V _{IN} ¹ = V _{SS} | | -600 | — | μA |

Note:

1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

Table 25. RGMII/RTBI DC Electrical Characteristics

| Parameters | Symbol | Conditions | Min | Max | Unit |
|----------------------|--------------------------------------|------------|------|------|------|
| Supply voltage 2.5 V | LV _{DDA} /LV _{DDB} | — | 2.37 | 2.63 | V |

Table 25. RGMII/RTBI DC Electrical Characteristics (continued)

| Parameters | Symbol | Conditions | | Min | Max | Unit |
|---------------------|----------|-------------------------------------|---------------------------------------|----------------|--|---------------|
| Output high voltage | V_{OH} | $I_{OH} = -1.0 \text{ mA}$ | LV_{DDA} or $LV_{DDB} = \text{Min}$ | 2.00 | $LV_{DDA} + 0.3$ or $LV_{DDB} + 0.3$ | V |
| Output low voltage | V_{OL} | $I_{OL} = 1.0 \text{ mA}$ | LV_{DDA} or $LV_{DDB} = \text{Min}$ | $V_{SS} - 0.3$ | 0.40 | V |
| Input high voltage | V_{IH} | — | LV_{DDA} or $LV_{DDB} = \text{Min}$ | 1.7 | $LV_{DDA} + 0.3$ or $LV_{DDB} + 0.3$ | V |
| Input low voltage | V_{IL} | — | LV_{DDA} or $LV_{DDB} = \text{Min}$ | -0.3 | 0.70 | V |
| Input high current | I_{IH} | $V_{IN}^1 = LV_{DDA}$ or LV_{DDB} | | — | 10 | μA |
| Input low current | I_{IL} | $V_{IN}^1 = V_{SS}$ | | -15 | — | μA |

Note:

- Note that the symbol V_{IN} , in this case, represents the LV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

8.2 MII, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for MII, RMII, RGMII, and RTBI are presented in this section.

8.2.1 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.1.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

Table 26. MII Transmit AC Timing Specifications

At recommended operating conditions with $LV_{DDA}/LV_{DDB}/NV_{DD}$ of $3.3 \text{ V} \pm 0.3 \text{ V}$.

| Parameter/Condition | Symbol ¹ | Min | Typ | Max | Unit |
|---|---------------------|-----|-----|-----|------|
| TX_CLK clock period 10 Mbps | t_{MTX} | — | 400 | — | ns |
| TX_CLK clock period 100 Mbps | t_{MTX} | — | 40 | — | ns |
| TX_CLK duty cycle | t_{MTXH}/t_{MTX} | 35 | — | 65 | % |
| TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay | t_{MTKHDX} | 1 | 5 | 15 | ns |
| TX_CLK data clock rise $V_{IL}(\text{min})$ to $V_{IH}(\text{max})$ | t_{MTXR} | 1.0 | — | 4.0 | ns |
| TX_CLK data clock fall $V_{IH}(\text{max})$ to $V_{IL}(\text{min})$ | t_{MTXF} | 1.0 | — | 4.0 | ns |

Note:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the MII transmit AC timing diagram.



Figure 8. MII Transmit AC Timing Diagram

8.2.1.2 MII Receive AC Timing Specifications

This table provides the MII receive AC timing specifications.

Table 27. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DDA}/LV_{ddb}/NV_{DD} of 3.3 V ± 0.3 V.

| Parameter/Condition | Symbol ¹ | Min | Typ | Max | Unit |
|---|-------------------------------------|------|-----|-----|------|
| RX_CLK clock period 10 Mbps | t _{MRX} | — | 400 | — | ns |
| RX_CLK clock period 100 Mbps | t _{MRX} | — | 40 | — | ns |
| RX_CLK duty cycle | t _{MRXH} /t _{MRX} | 35 | — | 65 | % |
| RXD[3:0], RX_DV, RX_ER setup time to RX_CLK | t _{MRDVKH} | 10.0 | — | — | ns |
| RXD[3:0], RX_DV, RX_ER hold time to RX_CLK | t _{MRDXKH} | 10.0 | — | — | ns |
| RX_CLK clock rise V _{IL} (min) to V _{IH} (max) | t _{MRXR} | 1.0 | — | 4.0 | ns |
| RX_CLK clock fall time V _{IH} (max) to V _{IL} (min) | t _{MRXF} | 1.0 | — | 4.0 | ns |

Note:

- The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- The frequency of RX_CLK should not exceed the TX_CLK by more than 300 ppm

This figure provides the AC test load for TSEC.

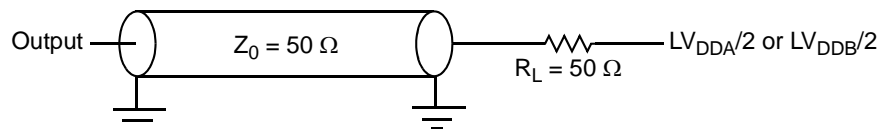


Figure 9. TSEC AC Test Load

8.2.1.4 RMI Receive AC Timing Specifications

This table provides the RMI receive AC timing specifications.

Table 29. RMI Receive AC Timing Specifications

At recommended operating conditions with NV_{DD} of $3.3\text{ V} \pm 0.3\text{ V}$.

| Parameter/Condition | Symbol ¹ | Min | Typ | Max | Unit |
|--|---------------------|-----|-----|-----|------|
| REF_CLK clock period | t_{RMX} | — | 20 | — | ns |
| REF_CLK duty cycle | t_{RMXH}/t_{RMX} | 35 | — | 65 | % |
| RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK | $t_{RMRDVKH}$ | 4.0 | — | — | ns |
| RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK | $t_{RMRDXKH}$ | 2.0 | — | — | ns |
| REF_CLK clock rise $V_{IL}(\text{min})$ to $V_{IH}(\text{max})$ | t_{RMXR} | 1.0 | — | 4.0 | ns |
| REF_CLK clock fall time $V_{IH}(\text{max})$ to $V_{IL}(\text{min})$ | t_{RMXF} | 1.0 | — | 4.0 | ns |

Note:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first three letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMI receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMI receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMI (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This table provides the AC test load.



Figure 12. AC Test Load

This table shows the RMI receive AC timing diagram.

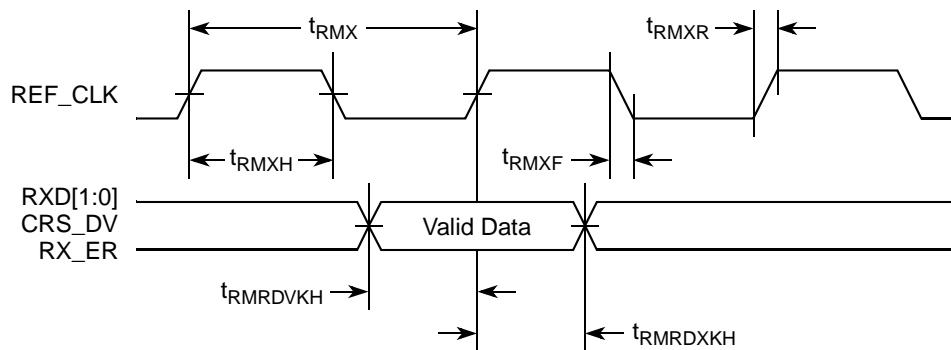


Figure 13. RMI Receive AC Timing Diagram

8.2.2 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 30. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with V_{DDA}/V_{DDB} of 2.5 V \pm 5%.

| Parameter/Condition | Symbol ¹ | Min | Typ | Max | Unit |
|--|----------------------|------|-----|------|------|
| Data to clock output skew (at transmitter) | t_{SKRGT} | -0.5 | — | 0.5 | ns |
| Data to clock input skew (at receiver) ² | t_{SKRGT} | 1.0 | — | 2.6 | ns |
| Clock cycle duration ³ | t_{RGT} | 7.2 | 8.0 | 8.8 | ns |
| Duty cycle for 1000Base-T ^{4, 5} | t_{RGTH}/t_{RGT} | 45 | 50 | 55 | % |
| Duty cycle for 10BASE-T and 100BASE-TX ^{3, 5} | t_{RGTH}/t_{RGT} | 40 | 50 | 60 | % |
| Rise time (20%–80%) | t_{RGTR} | — | — | 0.75 | ns |
| Fall time (20%–80%) | t_{RGTF} | — | — | 0.75 | ns |
| GTX_CLK125 reference clock period | t_{G12}^6 | — | 8.0 | — | ns |
| GTX_CLK125 reference clock duty cycle | t_{G125H}/t_{G125} | 47 | — | 53 | % |

Note:

- Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the RTBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
- This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
- For 10 and 100 Mbps, t_{RGT} scales to 400 ns \pm 40 ns and 40 ns \pm 4 ns, respectively.
- Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
- Duty cycle reference is $V_{DDA}/2$ or $V_{DDB}/2$.
- This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.
- The frequency of RX_CLK should not exceed the GTX_CLK125 by more than 300 ppm

This figure shows the RGMII and RTBI AC timing and multiplexing diagrams.

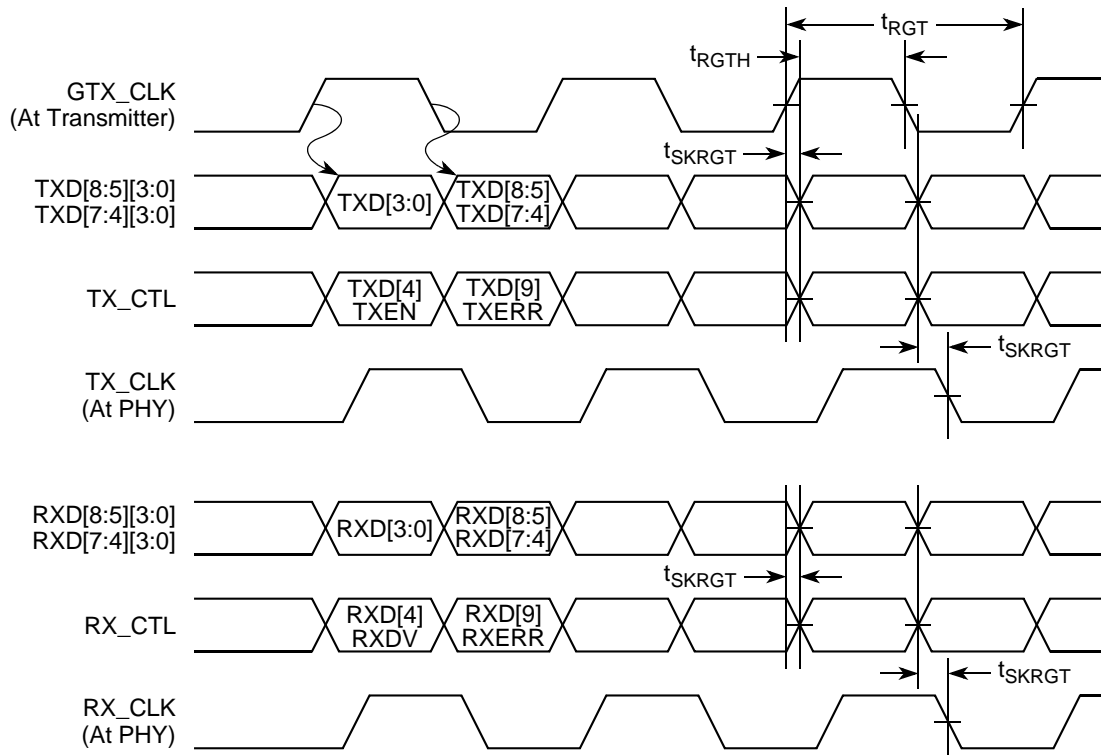


Figure 14. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.3 SGMII Interface Electrical Characteristics

Each SGMII port features a 4-wire AC-coupled serial link from the dedicated SerDes interface of MPC8313E as shown in [Figure 15](#), where C_{TX} is the external (on board) AC-coupled capacitor. Each output pin of the SerDes transmitter differential pair features a 50- Ω output impedance. Each input of the SerDes receiver differential pair features 50- Ω on-die termination to XCOREVSS. The reference circuit of the SerDes transmitter and receiver is shown in [Figure 33](#).

When an eTSEC port is configured to operate in SGMII mode, the parallel interface's output signals of this eTSEC port can be left floating. The input signals should be terminated based on the guidelines described in [Section 22.5, "Connection Recommendations,"](#) as long as such termination does not violate the desired POR configuration requirement on these pins, if applicable.

When operating in SGMII mode, the TSEC_GTX_CLK125 clock is not required for this port. Instead, the SerDes reference clock is required on SD_REF_CLK and SD_REF_CLK pins.

8.3.1 DC Requirements for SGMII SD_REF_CLK and SD_REF_CLK

The characteristics and DC requirements of the separate SerDes reference clock are described in [Section 9, "High-Speed Serial Interfaces \(HSSI\)."](#)

8.3.2 AC Requirements for SGMII SD_REF_CLK and $\overline{\text{SD_REF_CLK}}$

This table lists the SGMII SerDes reference clock AC requirements. Note that SD_REF_CLK and $\overline{\text{SD_REF_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

Table 31. SD_REF_CLK and $\overline{\text{SD_REF_CLK}}$ AC Requirements

| Symbol | Parameter Description | Min | Typ | Max | Unit |
|--------------------|--|-----|-----|-----|------|
| t_{REF} | REFCLK cycle time | — | 8 | — | ns |
| t_{REFCJ} | REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles | — | — | 100 | ps |
| t_{REFPJ} | Phase jitter. Deviation in edge location with respect to mean edge location | -50 | — | 50 | ps |

8.3.3 SGMII Transmitter and Receiver DC Electrical Characteristics

Table 32 and Table 33 describe the SGMII SerDes transmitter and receiver AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD_TX[n] and $\overline{\text{SD_TX[n]}}$) as depicted in Figure 16.

Table 32. SGMII DC Transmitter Electrical Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|-----------------------------------|---|-----|---|------|----------------------------|
| Supply voltage | XCOREV _{DD} | 0.95 | 1.0 | 1.05 | V | |
| Output high voltage | V _{OH} | — | — | $\frac{\text{XCOREV}_{\text{DD-Typ}}}{2} + \frac{ V_{\text{OD-max}} }{2}$ | mV | 1 |
| Output low voltage | V _{OL} | $\frac{\text{XCOREV}_{\text{DD-Typ}}}{2} - \frac{ V_{\text{OD-max}} }{2}$ | — | — | mV | 1 |
| Output ringing | V _{RING} | — | — | 10 | % | |
| Output differential voltage ^{2, 3} | V _{OD} | 323 | 500 | 725 | mV | Equalization setting: 1.0x |
| Output offset voltage | V _{OS} | 425 | 500 | 575 | mV | 1, 4 |
| Output impedance (single-ended) | R _O | 40 | — | 60 | Ω | |
| Mismatch in a pair | ΔR _O | — | — | 10 | % | |
| Change in V _{OD} between 0 and 1 | Δ V _{OD} | — | — | 25 | mV | |
| Change in V _{OS} between 0 and 1 | ΔV _{OS} | — | — | 25 | mV | |
| Output current on short to GND | I _{SA} , I _{SB} | — | — | 40 | mA | |

Notes:

1. This will not align to DC-coupled SGMII. XCOREV_{DD-Typ} = 1.0 V.
2. |V_{OD}| = |V_{TXn} - V _{$\overline{\text{TXn}}$} |. |V_{OD}| is also referred as output differential peak voltage. V_{TX-DIFFp-p} = 2*|V_{OD}|.
3. The |V_{OD}| value shown in the Typ column is based on the condition of XCOREV_{DD-Typ} = 1.0 V, no common mode offset variation (V_{OS} = 500 mV), SerDes transmitter is terminated with 100-Ω differential load between TX[n] and $\overline{\text{TX[n]}}$.
4. V_{OS} is also referred to as output common mode voltage.

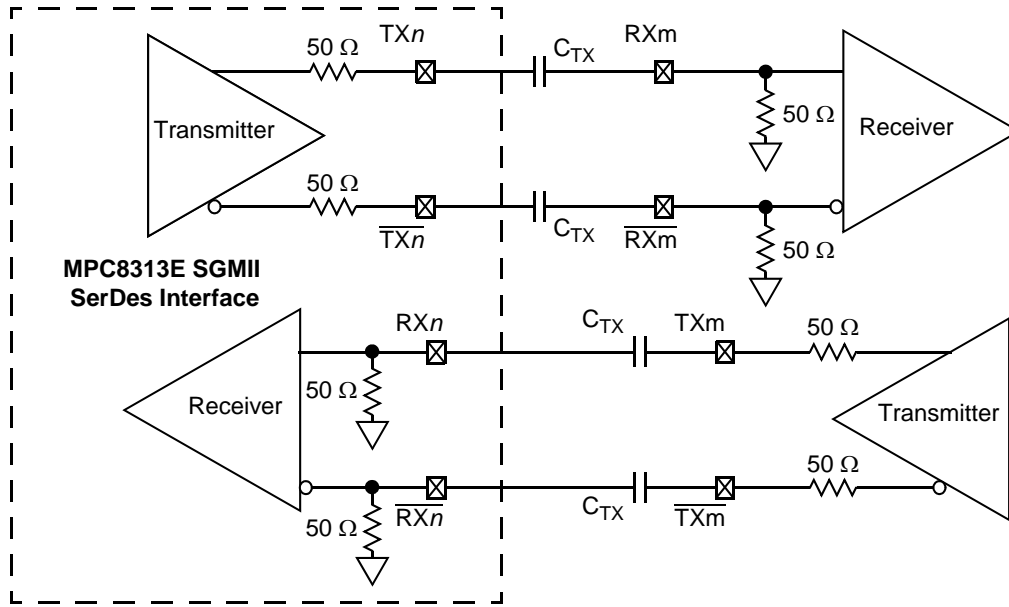


Figure 15. 4-Wire AC-Coupled SGMII Serial Link Connection Example

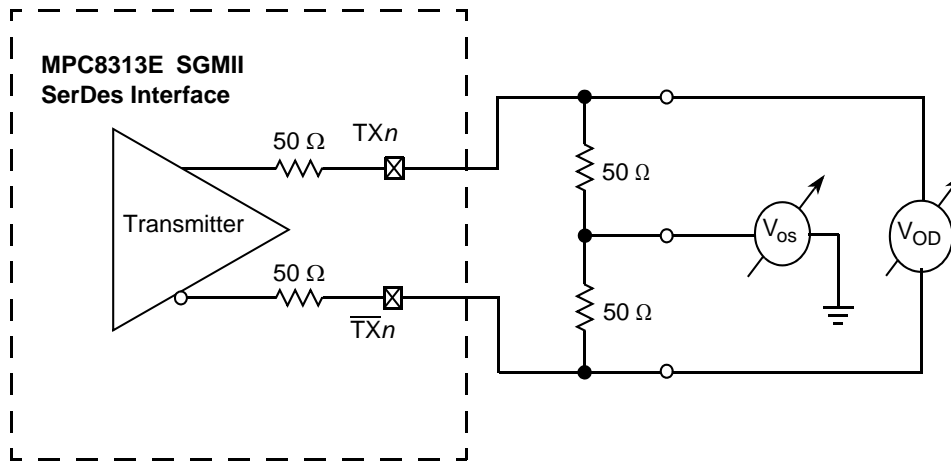


Figure 16. SGMII Transmitter DC Measurement Circuit

Table 33. SGMII DC Receiver Electrical Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---------------------------------------|-------------------------|------|-----|------|------|------|
| Supply voltage | XCOREV _{DD} | 0.95 | 1.0 | 1.05 | V | |
| DC Input voltage range | | N/A | | | | 1 |
| Input differential voltage | V _{RX_DIFFp-p} | 100 | — | 1200 | mV | 2 |
| Loss of signal threshold | V _{LOS} | 30 | — | 100 | mV | |
| Input AC common mode voltage | V _{CM_ACP-p} | — | — | 100 | mV | 3 |
| Receiver differential input impedance | Z _{RX_DIFF} | 80 | 100 | 120 | Ω | |
| Receiver common mode input impedance | Z _{RX_CM} | 20 | — | 35 | Ω | |

Table 33. SGMII DC Receiver Electrical Characteristics (continued)

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---------------------------|----------|-----|----------------|-----|------|------|
| Common mode input voltage | V_{CM} | — | $V_{XCOREVSS}$ | — | V | 4 |

Notes:

1. Input must be externally AC-coupled.
2. $V_{RX_DIFFp-p}$ is also referred to as peak to peak input differential voltage
3. V_{CM_ACp-p} is also referred to as peak to peak AC common mode voltage.
4. On-chip termination to $XCOREV_{SS}$.

8.3.4 SGMII AC Timing Specifications

This section describes the SGMII transmit and receive AC timing specifications. Transmitter and receiver characteristics are measured at the transmitter outputs (TX[n] and $\overline{TX}[n]$) or at the receiver inputs (RX[n] and $\overline{RX}[n]$) as depicted in Figure 18, respectively.

8.3.4.1 SGMII Transmit AC Timing Specifications

This table provides the SGMII transmit AC timing targets. A source synchronous clock is not provided.

Table 34. SGMII Transmit AC Timing Specifications

At recommended operating conditions with $XCOREV_{DD} = 1.0\text{ V} \pm 5\%$.

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|------------------------------|-------------------|--------|-----|--------|--------|------|
| Deterministic jitter | JD | — | — | 0.17 | UI p-p | |
| Total jitter | JT | — | — | 0.35 | UI p-p | |
| Unit interval | UI | 799.92 | 800 | 800.08 | ps | 1 |
| V_{OD} fall time (80%–20%) | t _{fall} | 50 | — | 120 | ps | |
| V_{OD} rise time (20%–80%) | t _{rise} | 50 | — | 120 | ps | |

Note:

1. Each UI is 800 ps \pm 100 ppm.

8.3.4.2 SGMII Receive AC Timing Specifications

This table provides the SGMII receive AC timing specifications. Source synchronous clocking is not supported. Clock is recovered from the data. Figure 17 shows the SGMII receiver input compliance mask eye diagram.

Table 35. SGMII Receive AC Timing Specifications

At recommended operating conditions with $XCOREV_{DD} = 1.0\text{ V} \pm 5\%$.

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|--|--------|------|-----|-----|--------|------|
| Deterministic jitter tolerance | JD | 0.37 | — | — | UI p-p | 1 |
| Combined deterministic and random jitter tolerance | JDR | 0.55 | — | — | UI p-p | 1 |
| Sinusoidal jitter tolerance | JSIN | 0.1 | — | — | UI p-p | 1 |

Table 35. SGMII Receive AC Timing Specifications (continued)

At recommended operating conditions with $XCOREV_{DD} = 1.0\text{ V} \pm 5\%$.

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|------------------------|----------|--------|-----|------------|--------|------|
| Total jitter tolerance | JT | 0.65 | — | — | UI p-p | 1 |
| Bit error ratio | BER | — | — | 10^{-12} | | |
| Unit interval | UI | 799.92 | 800 | 800.08 | ps | 2 |
| AC coupling capacitor | C_{TX} | 5 | — | 200 | nF | 3 |

Notes:

1. Measured at receiver.
2. Each UI is $800\text{ ps} \pm 100\text{ ppm}$.
3. The external AC coupling capacitor is required. It is recommended to be placed near the device transmitter outputs.

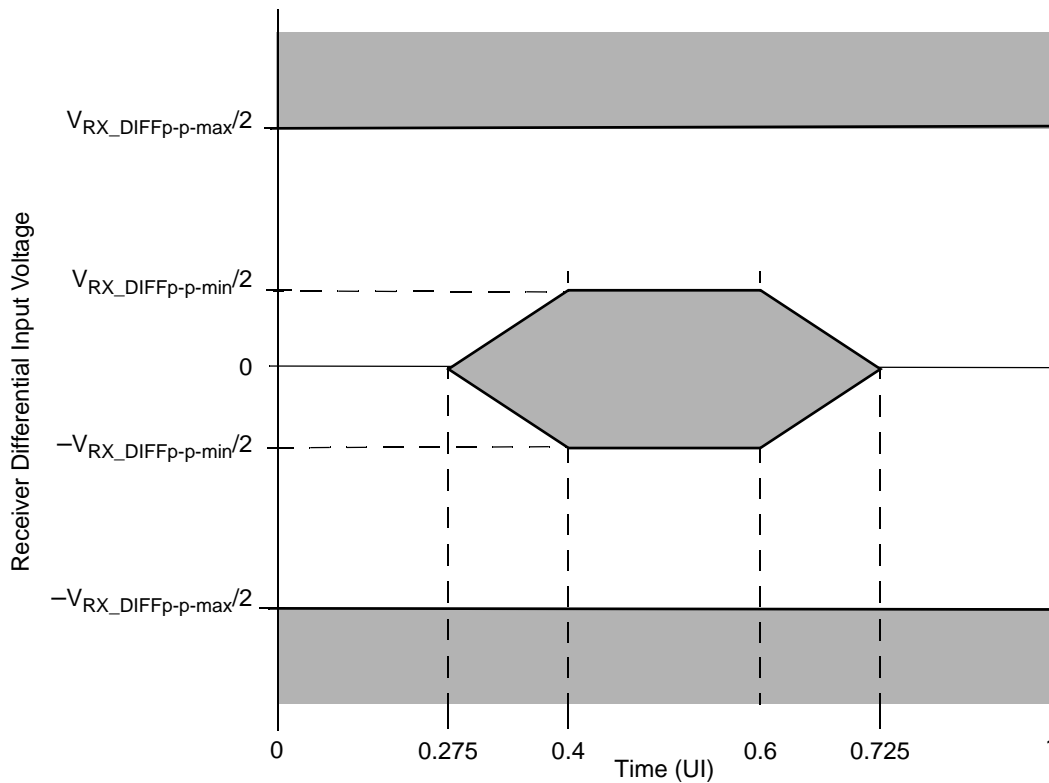


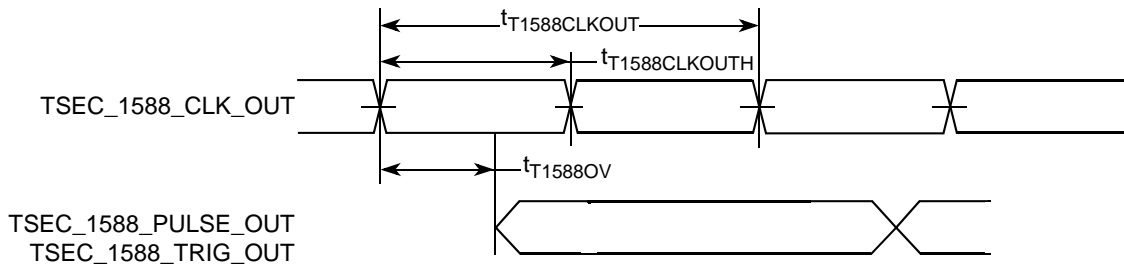
Figure 17. SGMII Receiver Input Compliance Mask



Figure 18. SGMII AC Test/Measurement Load

8.4 eTSEC IEEE 1588 AC Specifications

This figure provides the data and command output timing diagram.



Note: The output delay is count starting rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is count starting falling edge.

Figure 19. eTSEC IEEE 1588 Output AC Timing

This figure provides the data and command input timing diagram.

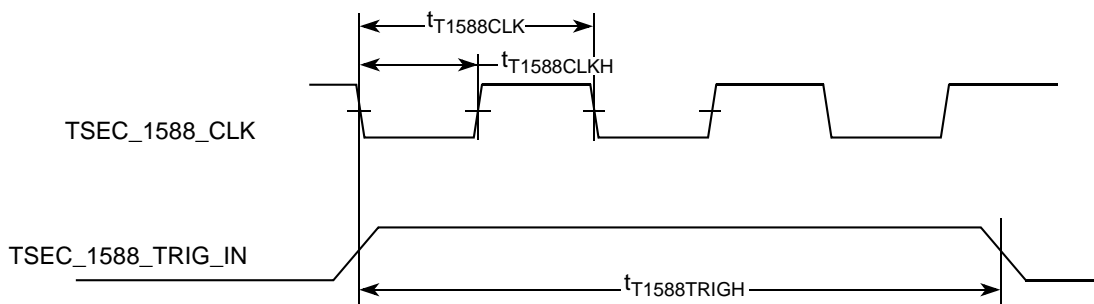


Figure 20. eTSEC IEEE 1588 Input AC Timing

This table lists the IEEE 1588 AC timing specifications.

Table 36. eTSEC IEEE 1588 AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of $3.3\text{ V} \pm 5\%$.

| Parameter/Condition | Symbol | Min | Typ | Max | Unit | Note |
|----------------------------|------------------------------|-----|-----|------------------------|------|------|
| TSEC_1588_CLK clock period | $t_{T1588CLK}$ | 3.8 | — | $T_{RX_CLK} \times 9$ | ns | 1, 3 |
| TSEC_1588_CLK duty cycle | $t_{T1588CLKH}/t_{T1588CLK}$ | 40 | 50 | 60 | % | |

Table 36. eTSEC IEEE 1588 AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

| Parameter/Condition | Symbol | Min | Typ | Max | Unit | Note |
|------------------------------------|---|-------------------------------|-----|-----|------|------|
| TSEC_1588_CLK peak-to-peak jitter | t _{T1588CLKINJ} | — | — | 250 | ps | |
| Rise time eTSEC_1588_CLK (20%–80%) | t _{T1588CLKINR} | 1.0 | — | 2.0 | ns | |
| Fall time eTSEC_1588_CLK (80%–20%) | t _{T1588CLKINF} | 1.0 | — | 2.0 | ns | |
| TSEC_1588_CLK_OUT clock period | t _{T1588CLKOUT} | 2 × t _{T1588CLK} | — | — | ns | |
| TSEC_1588_CLK_OUT duty cycle | t _{T1588CLKOTH} / t _{T1588CLKOUT} | 30 | 50 | 70 | % | |
| TSEC_1588_PULSE_OUT | t _{T1588OV} | 0.5 | — | 3.0 | ns | |
| TSEC_1588_TRIG_IN pulse width | t _{T1588TRIGH} | 2 × t _{T1588CLK_MAX} | — | — | ns | 2 |

Notes:

1. T_{RX_CLK} is the max clock period of eTSEC receiving clock selected by TMR_CTRL[CKSEL]. See the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual*, for a description of TMR_CTRL registers.
2. It need to be at least two times of clock period of clock selected by TMR_CTRL[CKSEL]. See the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual*, for a description of TMR_CTRL registers.
3. The maximum value of t_{T1588CLK} is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of t_{T1588CLK} is 3600, 280, and 56 ns, respectively.

8.5 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII, RMII, RGMII, SGMII, and RTBI are specified in [Section 8.1, “Enhanced Three-Speed Ethernet Controller \(eTSEC\) \(10/100/1000 Mbps\)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics.”](#)

8.5.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. [Table 37](#) provide the DC electrical characteristics for MDIO and MDC.

Table 37. MII Management DC Electrical Characteristics When Powered at 3.3 V

| Parameter | Symbol | Conditions | | Min | Max | Unit |
|------------------------|------------------|---------------------------|--------------------------------------|-----------------|------------------------|------|
| Supply voltage (3.3 V) | NV _{DD} | — | | 2.97 | 3.63 | V |
| Output high voltage | V _{OH} | I _{OH} = -1.0 mA | NV _{DD} = Min | 2.10 | NV _{DD} + 0.3 | V |
| Output low voltage | V _{OL} | I _{OL} = 1.0 mA | NV _{DD} = Min | V _{SS} | 0.50 | V |
| Input high voltage | V _{IH} | — | | 2.0 | — | V |
| Input low voltage | V _{IL} | — | | — | 0.80 | V |
| Input high current | I _{IH} | NV _{DD} = Max | V _{IN} ¹ = 2.1 V | — | 40 | μA |
| Input low current | I _{IL} | NV _{DD} = Max | V _{IN} = 0.5 V | -600 | — | μA |

Table 37. MII Management DC Electrical Characteristics When Powered at 3.3 V (continued)

Note:

- Note that the symbol V_{IN} , in this case, represents the NV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

8.5.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 38. MII Management AC Timing Specifications

At recommended operating conditions with NV_{DD} is 3.3 V \pm 0.3V

| Parameter/Condition | Symbol ¹ | Min | Typ | Max | Unit | Note |
|----------------------------|---------------------|-----|-----|-----|------|------|
| MDC frequency | f_{MDC} | — | 2.5 | — | MHz | 2 |
| MDC period | t_{MDC} | — | 400 | — | ns | |
| MDC clock pulse width high | t_{MDCH} | 32 | — | — | ns | |
| MDC to MDIO delay | t_{MDKHDX} | 10 | — | 170 | ns | |
| MDIO to MDC setup time | t_{MDDVKH} | 5 | — | — | ns | |
| MDIO to MDC hold time | t_{MDDXKH} | 0 | — | — | ns | |
| MDC rise time | t_{MDCR} | — | — | 10 | ns | |
| MDC fall time | t_{MDHF} | — | — | 10 | ns | |

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- This parameter is dependent on the `csb_clk` speed. (The `MIIMCFG[Mgmt Clock Select]` field determines the clock frequency of the Mgmt Clock `EC_MDC`.)

This figure shows the MII management AC timing diagram.

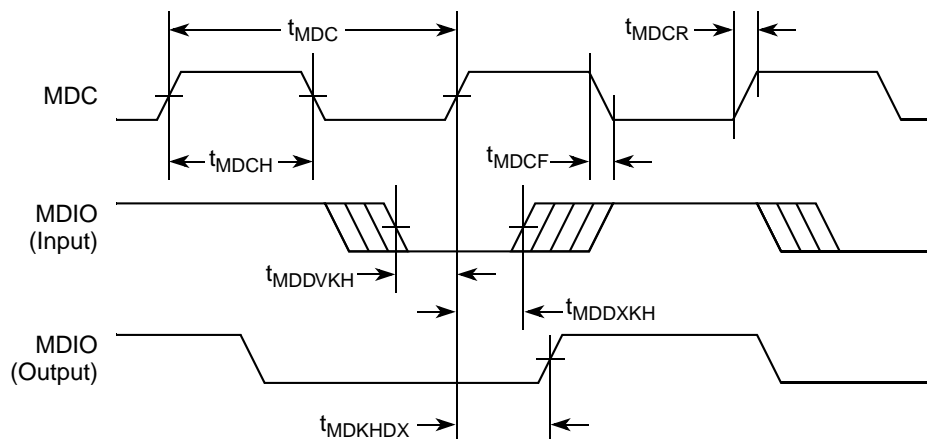


Figure 21. MII Management Interface Timing Diagram

9 High-Speed Serial Interfaces (HSSI)

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

9.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 22 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (TX_n and $\overline{TX_n}$) or a receiver input (RX_n and $\overline{RX_n}$). Each signal swings between A volts and B volts where $A > B$.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. Single-ended swing
The transmitter output signals and the receiver input signals TX_n , $\overline{TX_n}$, RX_n , and $\overline{RX_n}$ each have a peak-to-peak swing of $A - B$ volts. This is also referred as each signal wire's single-ended swing.
2. Differential output voltage, V_{OD} (or differential output swing):
The differential output voltage (or swing) of the transmitter, V_{OD} , is defined as the difference of the two complimentary output voltages: $V_{TX_n} - V_{\overline{TX_n}}$. The V_{OD} value can be either positive or negative.
3. Differential input voltage, V_{ID} (or differential input swing):
The differential input voltage (or swing) of the receiver, V_{ID} , is defined as the difference of the two complimentary input voltages: $V_{RX_n} - V_{\overline{RX_n}}$. The V_{ID} value can be either positive or negative.
4. Differential peak voltage, V_{DIFFp}
The peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak voltage, $V_{DIFFp} = |A - B|$ volts.
5. Differential peak-to-peak, $V_{DIFFp-p}$
Since the differential output signal of the transmitter and the differential input signal of the receiver each range from $A - B$ to $-(A - B)$ volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |A - B|$ volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.
6. Differential waveform
The differential waveform is constructed by subtracting the inverting signal (TX_n , for example) from the non-inverting signal ($\overline{TX_n}$, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 22 as an example for differential waveform.
7. Common mode voltage, V_{cm}

The common mode voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = (V_{TXn} + V_{\overline{TXn}})/2 = (A + B)/2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It's also referred as the DC offset in some occasion.

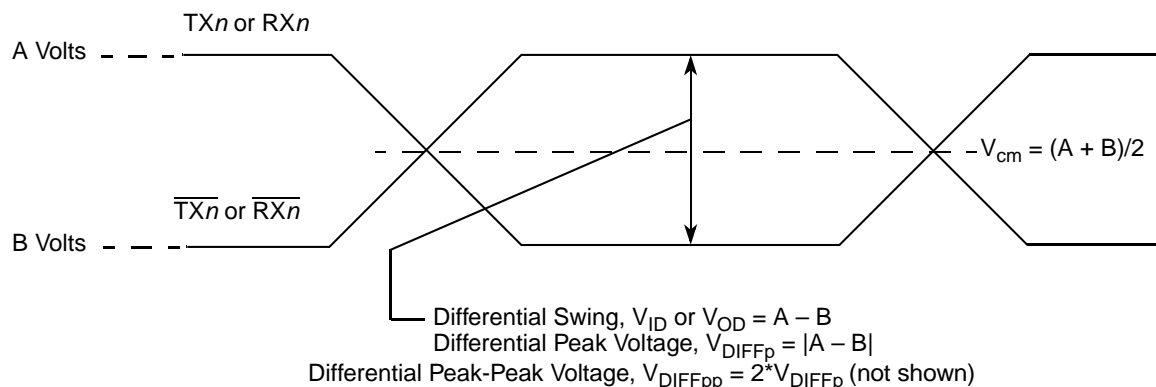


Figure 22. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and \overline{TD} , has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or \overline{TD}) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 and -500 mV, in other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

9.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks input is SD_REF_CLK and $\overline{SD_REF_CLK}$ for SGMII interface.

The following sections describe the SerDes reference clock requirements and some application information.

9.2.1 SerDes Reference Clock Receiver Characteristics

Figure 23 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for $XCOREV_{DD}$ are specified in Table 1 and Table 2.
- SerDes reference clock receiver reference circuit structure:

- The SD_REF_CLK and $\overline{\text{SD_REF_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 23. Each differential clock input (SD_REF_CLK or $\overline{\text{SD_REF_CLK}}$) has a 50- Ω termination to XCOREV_{SS} followed by on-chip AC coupling.
- The external reference clock driver must be able to drive this termination.
- The SerDes reference clock input can be either differential or single-ended. Refer to the differential mode and single-ended mode description below for further detailed requirements.
- The maximum average current requirement that also determines the common mode voltage range:
 - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
 - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1 V above XCOREV_{SS}. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
 - If the device driving the SD_REF_CLK and $\overline{\text{SD_REF_CLK}}$ inputs cannot drive 50 Ω to XCOREV_{SS} DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement. This requirement is described in detail in the following sections.

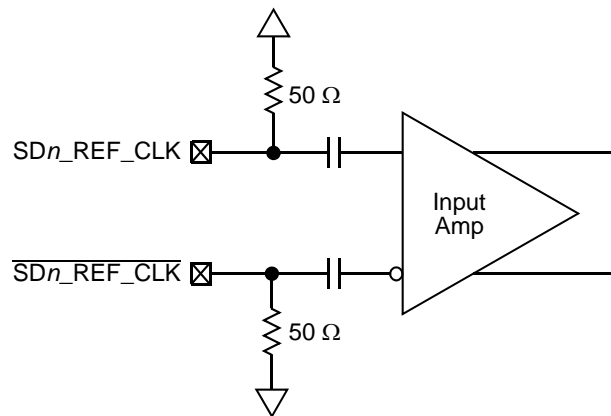


Figure 23. Receiver of SerDes Reference Clocks

9.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the MPC8313E SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- Differential mode
 - The input amplitude of the differential clock must be between 400 and 1600 mV differential peak-to-peak (or between 200 and 800 mV differential peak). In other words, each signal wire

of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.

- For external DC-coupled connection, as described in [Section 9.2.1, “SerDes Reference Clock Receiver Characteristics,”](#) the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 and 400 mV. [Figure 24](#) shows the SerDes reference clock input requirement for the DC-coupled connection scheme.
- For external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to $XCOREV_{SS}$. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage ($XCOREV_{SS}$). [Figure 25](#) shows the SerDes reference clock input requirement for AC-coupled connection scheme.
- Single-ended mode
 - The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400 and 800 mV peak-to-peak (from V_{min} to V_{max}) with SD_REF_CLK either left unconnected or tied to ground.
 - The SD_REF_CLK input average voltage must be between 200 and 400 mV. [Figure 26](#) shows the SerDes reference clock input requirement for the single-ended signaling mode.
 - To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC coupled externally. For the best noise performance, the reference of the clock could be DC or AC coupled into the unused phase (SD_REF_CLK) through the same source impedance as the clock input (SD_REF_CLK) in use.



Figure 24. Differential Reference Clock Input DC Requirements (External DC-Coupled)



Figure 25. Differential Reference Clock Input DC Requirements (External AC-Coupled)



Figure 26. Single-Ended Reference Clock Input DC Requirements

9.2.3 Interfacing With Other Differential Signaling Levels

- With on-chip termination to $XCOREV_{SS}$, the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce a signal with too large of an amplitude and may need to be DC-biased at the clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC coupling.

NOTE

Figure 27 through Figure 30 are for conceptual reference only. Due to the fact that the clock driver chip's internal structure, output impedance, and termination requirements are different between various clock driver chip manufacturers, it is possible that the clock circuit reference designs provided by clock driver chip vendors are different from what is shown in the figures. They might also vary from one vendor to the other. Therefore, Freescale can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. It is recommended that the system designer contact the selected clock driver chip vendor for the optimal reference circuits for the MPC8313E SerDes reference clock receiver requirement provided in this document.

This figure shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8313E SerDes reference clock input's DC requirement.

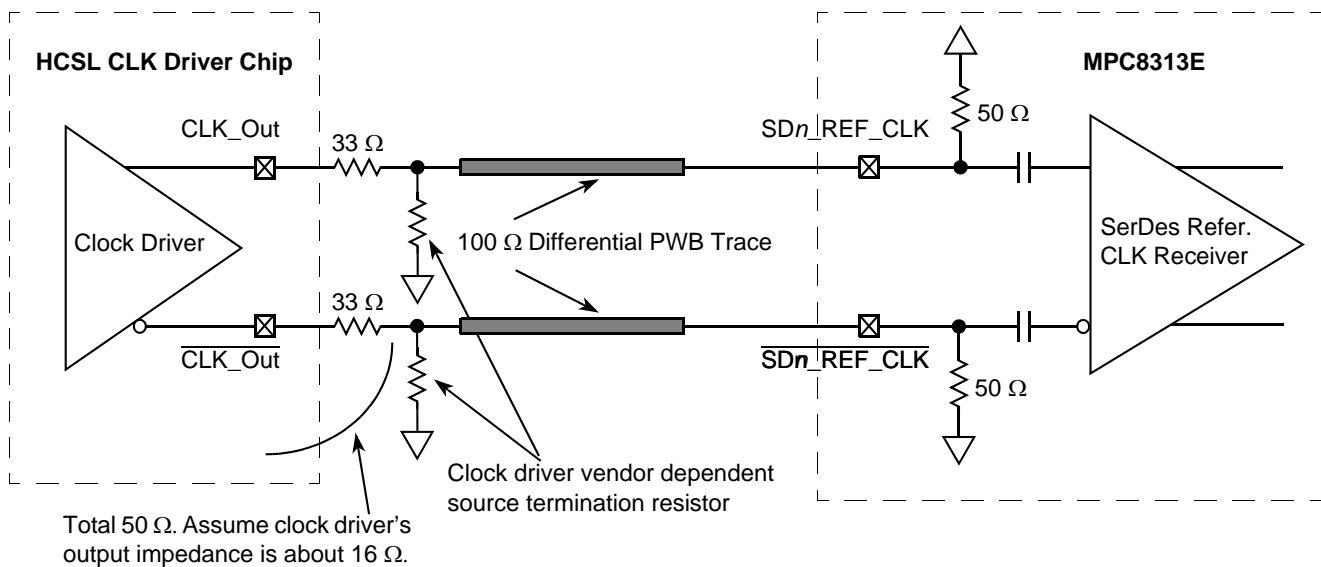


Figure 27. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the MPC8313E SerDes reference clock input's allowed range (100 to 400 mV), the AC-coupled connection scheme must be used. It assumes the LVDS output driver features a 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

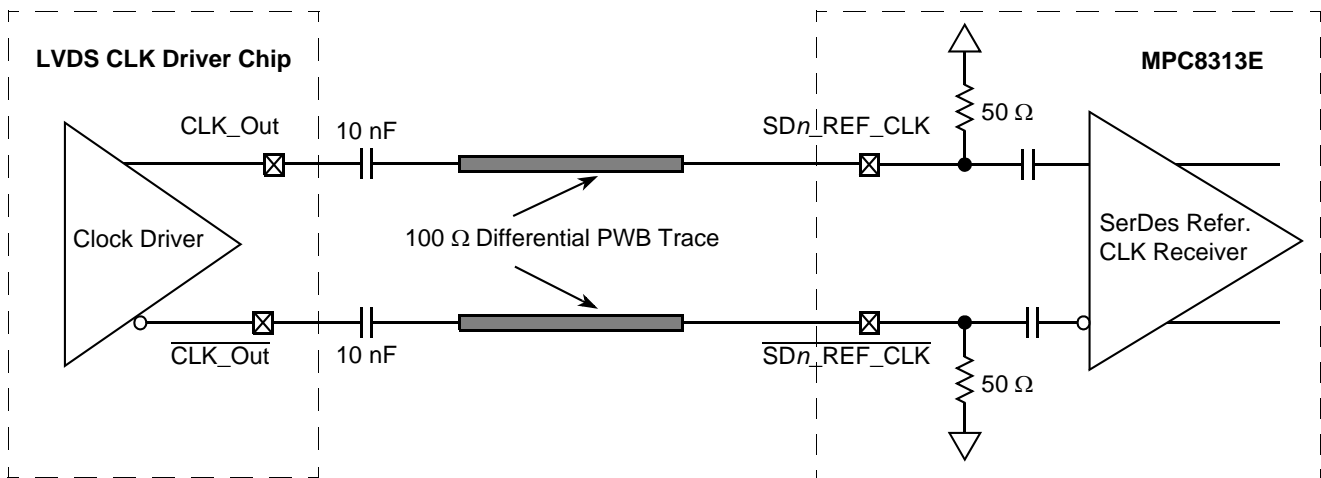


Figure 28. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with the MPC8313E SerDes reference clock input's DC requirement, AC coupling has to be used. [Figure 29](#)

assumes that the LVPECL clock driver's output impedance is $50\ \Omega$. R1 is used to DC-bias the LVPECL outputs prior to AC coupling. Its value could be ranged from 140 to $240\ \Omega$ depending on the clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's $50\text{-}\Omega$ termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8313E SerDes3 reference clock's differential input amplitude requirement (between 200 and $800\ \text{mV}$ differential peak). For example, if the LVPECL output's differential peak is $900\ \text{mV}$ and the desired SerDes reference clock input amplitude is selected as $600\ \text{mV}$, the attenuation factor is 0.67 , which requires $R2 = 25\ \Omega$. Consult with the clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

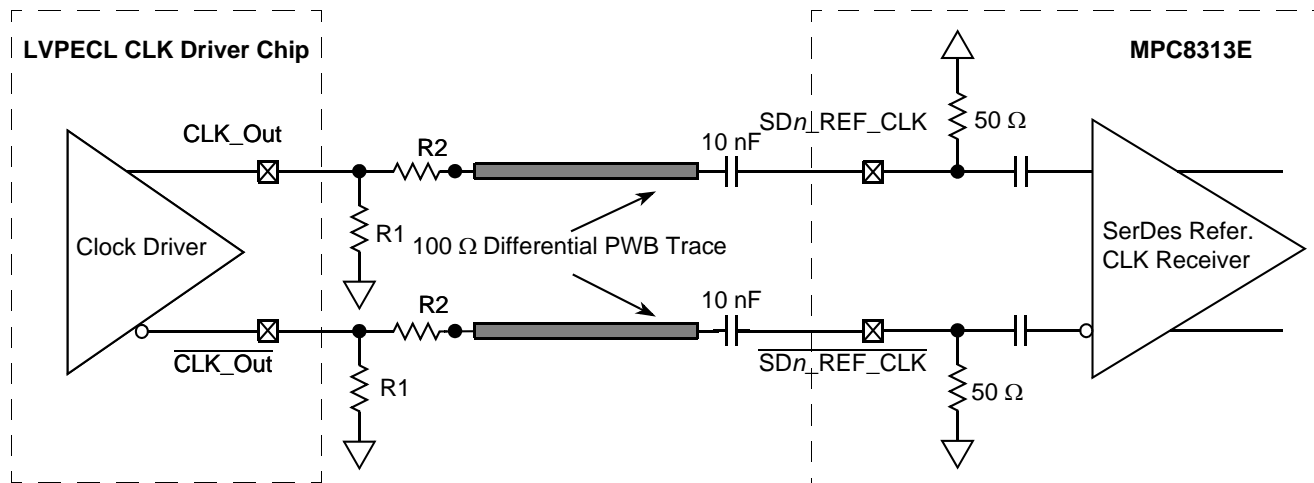


Figure 29. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with the MPC8313E SerDes reference clock input's DC requirement.

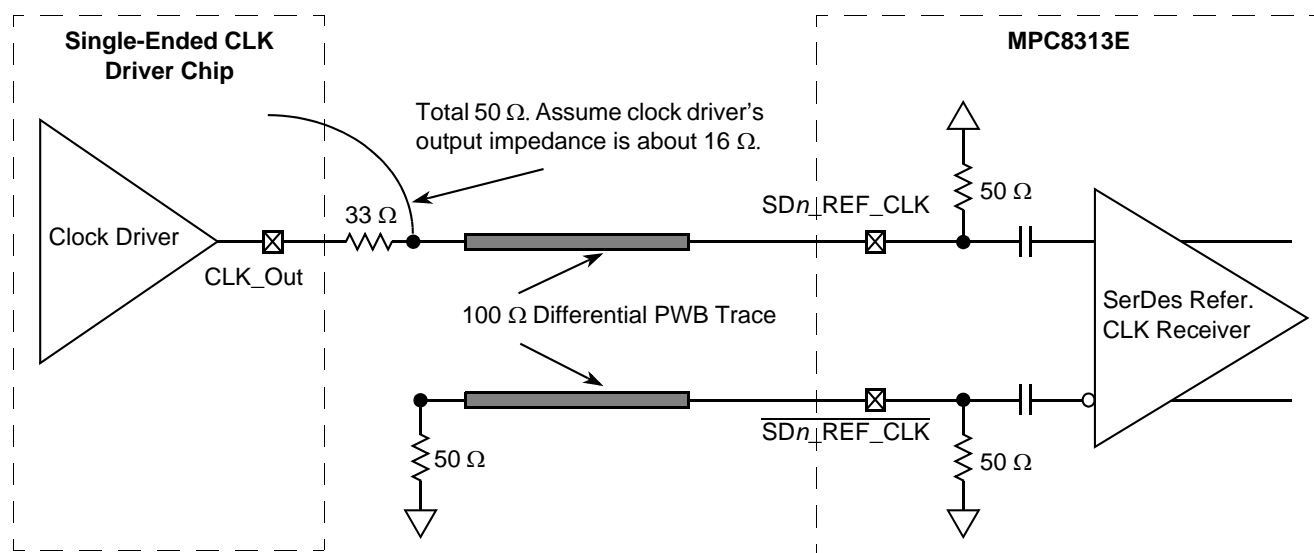


Figure 30. Single-Ended Connection (Reference Only)

9.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low-phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

This table describes some AC parameters for SGMII protocol.

Table 39. SerDes Reference Clock Common AC Parameters

At recommended operating conditions with XV_{DD_SRDS1} or $XV_{DD_SRDS2} = 1.0\text{ V} \pm 5\%$.

| Parameter | Symbol | Min | Max | Unit | Note |
|---|--------------------|------|------|------|------|
| Rising edge rate | Rise edge rate | 1.0 | 4.0 | V/ns | 2, 3 |
| Falling edge rate | Fall edge rate | 1.0 | 4.0 | V/ns | 2, 3 |
| Differential input high voltage | V_{IH} | +200 | — | mV | 2 |
| Differential input low voltage | V_{IL} | — | -200 | mV | 2 |
| Rising edge rate (SDn_REF_CLK) to falling edge rate ($\overline{SDn_REF_CLK}$) matching | Rise-fall matching | — | 20 | % | 1, 4 |

Notes:

1. Measurement taken from single-ended waveform.
2. Measurement taken from differential waveform.
3. Measured from -200 to +200 mV on the differential waveform (derived from SDn_REF_CLK minus $\overline{SDn_REF_CLK}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See [Figure 31](#).
4. Matching applies to rising edge rate for SDn_REF_CLK and falling edge rate for $\overline{SDn_REF_CLK}$. It is measured using a 200 mV window centered on the median cross point, where SDn_REF_CLK rising meets $\overline{SDn_REF_CLK}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rise edge rate of SDn_REF_CLK should be compared to the fall edge rate of $\overline{SDn_REF_CLK}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See [Figure 32](#).



Figure 31. Differential Measurement Points for Rise and Fall Time

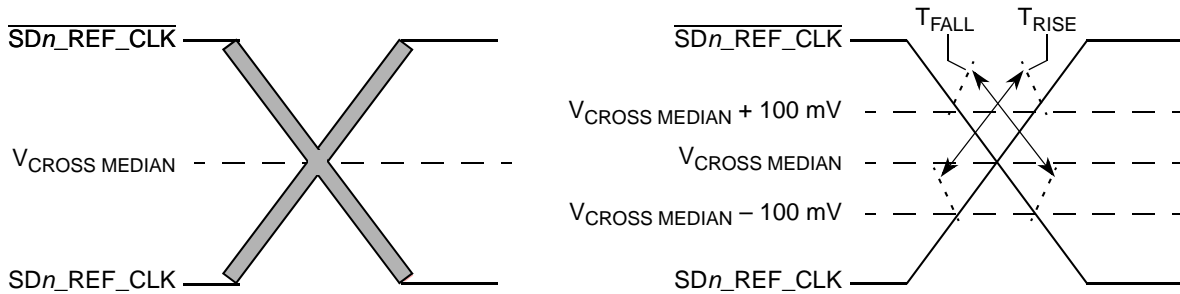


Figure 32. Single-Ended Measurement Points for Rise and Fall Time Matching

The other detailed AC requirements of the SerDes reference clocks is defined by each interface protocol based on application usage. Refer to the following section for detailed information:

- [Section 8.3.2, “AC Requirements for SGMII SD_REF_CLK and SD_REF_CLK”](#)

9.2.4.1 Spread Spectrum Clock

$\overline{\text{SD_REF_CLK}}/\text{SD_REF_CLK}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

9.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for the SerDes data lane’s transmitter and receiver.

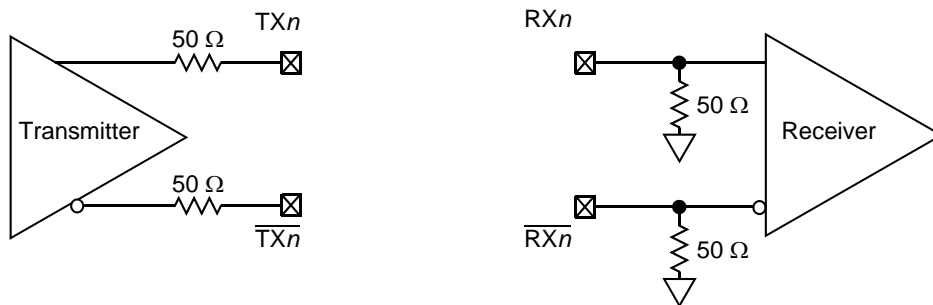


Figure 33. SerDes Transmitter and Receiver Reference Circuits

The SerDes data lane’s DC and AC specifications are defined in the interface protocol section listed below (SGMII) based on the application usage:

- [Section 8.3, “SGMII Interface Electrical Characteristics”](#)

Please note that a external AC-coupling capacitor is required for the above serial transmission protocol with the capacitor value defined in the specifications of the protocol section.

10 USB

10.1 USB Dual-Role Controllers

This section provides the AC and DC electrical specifications for the USB interface.

10.1.1 USB DC Electrical Characteristics

This table provides the DC electrical characteristics for the USB interface.

Table 40. USB DC Electrical Characteristics

| Parameter | Symbol | Min | Max | Unit |
|--|----------|------------------|------------------|---------|
| High-level input voltage | V_{IH} | 2.0 | $LV_{DDB} + 0.3$ | V |
| Low-level input voltage | V_{IL} | -0.3 | 0.8 | V |
| Input current | I_{IN} | — | ± 5 | μA |
| High-level output voltage, $I_{OH} = -100 \mu A$ | V_{OH} | $LV_{DDB} - 0.2$ | — | V |
| Low-level output voltage, $I_{OL} = 100 \mu A$ | V_{OL} | — | 0.2 | V |

10.1.2 USB AC Electrical Specifications

This table describes the general timing parameters of the USB interface.

Table 41. USB General Timing Parameters (ULPI Mode Only)

| Parameter | Symbol ¹ | Min | Max | Unit | Note |
|--|---------------------|-----|-----|------|------|
| USB clock cycle time | t_{USCK} | 15 | — | ns | |
| Input setup to USB clock—all inputs | t_{USIVKH} | 4 | — | ns | |
| input hold to USB clock—all inputs | t_{USIXKH} | 1 | — | ns | |
| USB clock to output valid—all outputs | t_{USKHOV} | — | 7 | ns | |
| Output hold from USB clock—all outputs | t_{USKHOX} | 2 | — | ns | |

Note:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (USB) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes us timing (USB) for the USB clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.

The following two figures provide the AC test load and signals for the USB, respectively.

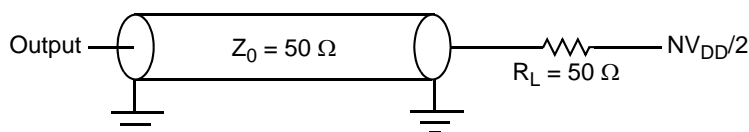


Figure 34. USB AC Test Load

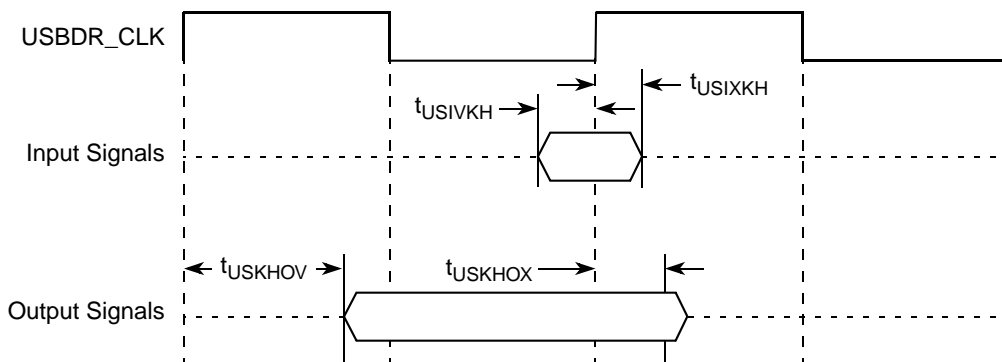


Figure 35. USB Signals

10.2 On-Chip USB PHY

This section describes the DC and AC electrical specifications for the on-chip USB PHY of the MPC8313E. See Chapter 7 in the *USB Specifications Rev. 2*, for more information.

This table provides the USB clock input (USB_CLK_IN) DC timing specifications.

Table 42. USB_CLK_IN DC Electrical Characteristics

| Parameter | Symbol | Min | Max | Unit |
|--------------------|----------|------|-----------------|------|
| Input high voltage | V_{IH} | 2.7 | $NV_{DD} + 0.3$ | V |
| Input low voltage | V_{IL} | -0.3 | 0.4 | V |

This table provides the USB clock input (USB_CLK_IN) AC timing specifications.

Table 43. USB_CLK_IN AC Timing Specifications

| Parameter/Condition | Conditions | Symbol | Min | Typ | Max | Unit |
|--|---|--------------------|--------|-----|-------|------|
| Frequency range | — | $f_{USB_CLK_IN}$ | — | 24 | 48 | MHz |
| Clock frequency tolerance | — | t_{CLK_TOL} | -0.005 | 0 | 0.005 | % |
| Reference clock duty cycle | Measured at 1.6 V | t_{CLK_DUTY} | 40 | 50 | 60 | % |
| Total input jitter/time interval error | Peak-to-peak value measured with a second order high-pass filter of 500 kHz bandwidth | t_{CLK_PJ} | — | — | 200 | ps |

11 Enhanced Local Bus

This section describes the DC and AC electrical specifications for the local bus interface.

11.1 Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the local bus interface.

Table 44. Local Bus DC Electrical Characteristics at 3.3 V

| Parameter | Symbol | Min | Max | Unit |
|---|----------|-----------------|-----------------|---------|
| High-level input voltage for Rev 1.0 | V_{IH} | 2.0 | $LV_{DD} + 0.3$ | V |
| High-level input voltage for Rev 2.x or later | V_{IH} | 2.1 | $LV_{DD} + 0.3$ | V |
| Low-level input voltage | V_{IL} | -0.3 | 0.8 | V |
| Input current, ($V_{IN}^1 = 0$ V or $V_{IN} = LV_{DD}$) | I_{IN} | — | ± 5 | μA |
| High-level output voltage, ($LV_{DD} = \text{min}$, $I_{OH} = -2$ mA) | V_{OH} | $LV_{DD} - 0.2$ | — | V |
| Low-level output voltage, ($LV_{DD} = \text{min}$, $I_{OH} = 2$ mA) | V_{OL} | — | 0.2 | V |

Note: The parameters stated in above table are valid for all revisions unless explicitly mentioned.

11.2 Local Bus AC Electrical Specifications

This table describes the general timing parameters of the local bus interface.

Table 45. Local Bus General Timing Parameters

| Parameter | Symbol ¹ | Min | Max | Unit | Note |
|---|---------------------|------|-----|------|------|
| Local bus cycle time | t_{LBK} | 15 | — | ns | 2 |
| Input setup to local bus clock | t_{LBIVKH} | 7 | — | ns | 3, 4 |
| Input hold from local bus clock | t_{LBIXKH} | 1.0 | — | ns | 3, 4 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT1}$ | 1.5 | — | ns | 5 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT2}$ | 3 | — | ns | 6 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT3}$ | 2.5 | — | ns | 7 |
| LALE output rise to LCLK negative edge | $t_{LALEHOV}$ | — | 3.0 | ns | |
| LALE output fall to LCLK negative edge | $t_{LALETOT1}$ | -1.5 | — | ns | 5 |
| LALE output fall to LCLK negative edge | $t_{LALETOT2}$ | -5.0 | — | ns | 6 |
| LALE output fall to LCLK negative edge | $t_{LALETOT3}$ | -4.5 | — | ns | 7 |
| Local bus clock to output valid | t_{LBKHOV} | — | 3 | ns | 3 |
| Local bus clock to output high impedance for LAD | t_{LBKHOZ} | — | 4 | ns | 8 |

Table 45. Local Bus General Timing Parameters (continued)

| Parameter | Symbol ¹ | Min | Max | Unit | Note |
|-----------|---------------------|-----|-----|------|------|
|-----------|---------------------|-----|-----|------|------|

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{\text{L BK}}$ clock reference (K) goes high (H), in this case for clock one (1).
2. All timings are in reference to falling edge of LCLK0 (for all outputs and for $\overline{\text{LGTA}}$ and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
3. All signals are measured from $NV_{\text{DD}}/2$ of the rising/falling edge of LCLK0 to $0.4 \times NV_{\text{DD}}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. t_{LBOTOT1} and t_{LALETOT1} should be used when RCWH[LALE] is not set and the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
6. t_{LBOTOT2} and t_{LALETOT2} should be used when RCWH[LALE] is set and the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
7. t_{LBOTOT3} and t_{LALETOT3} should be used when RCWH[LALE] is set and the load on LALE output pin equals to the load on LAD output pins.
8. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

This figure provides the AC test load for the local bus.

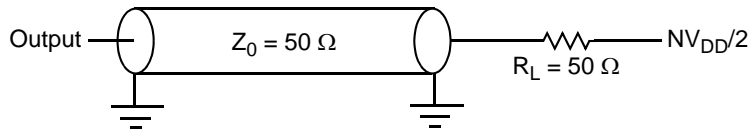


Figure 36. Local Bus AC Test Load

Figure 37 through Figure 40 show the local bus signals.

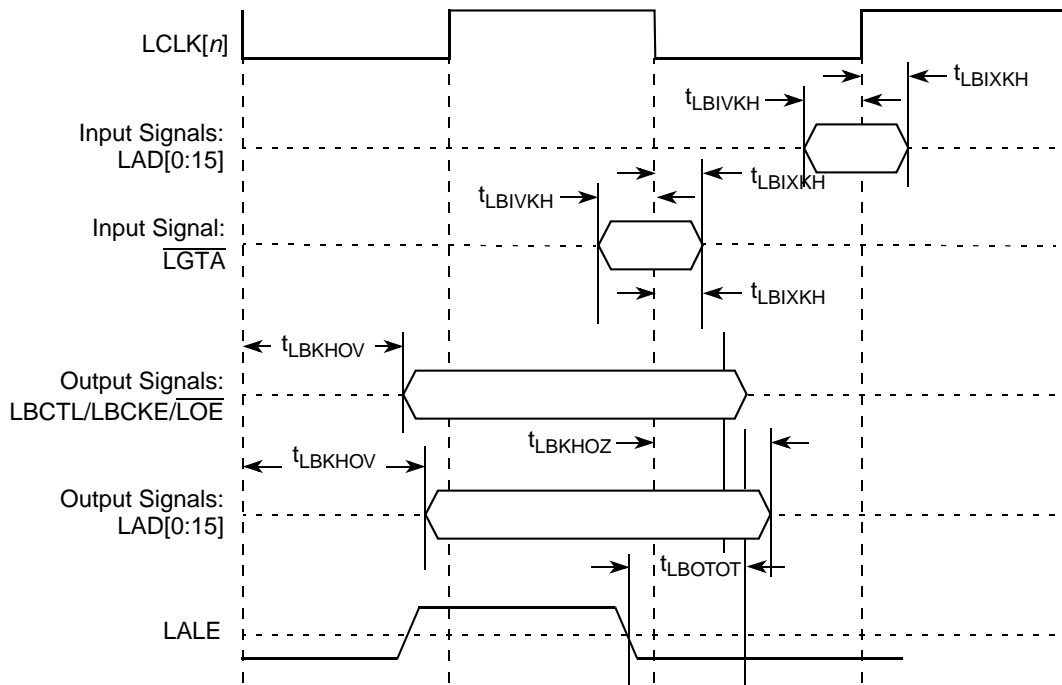


Figure 37. Local Bus Signals, Non-Special Signals Only

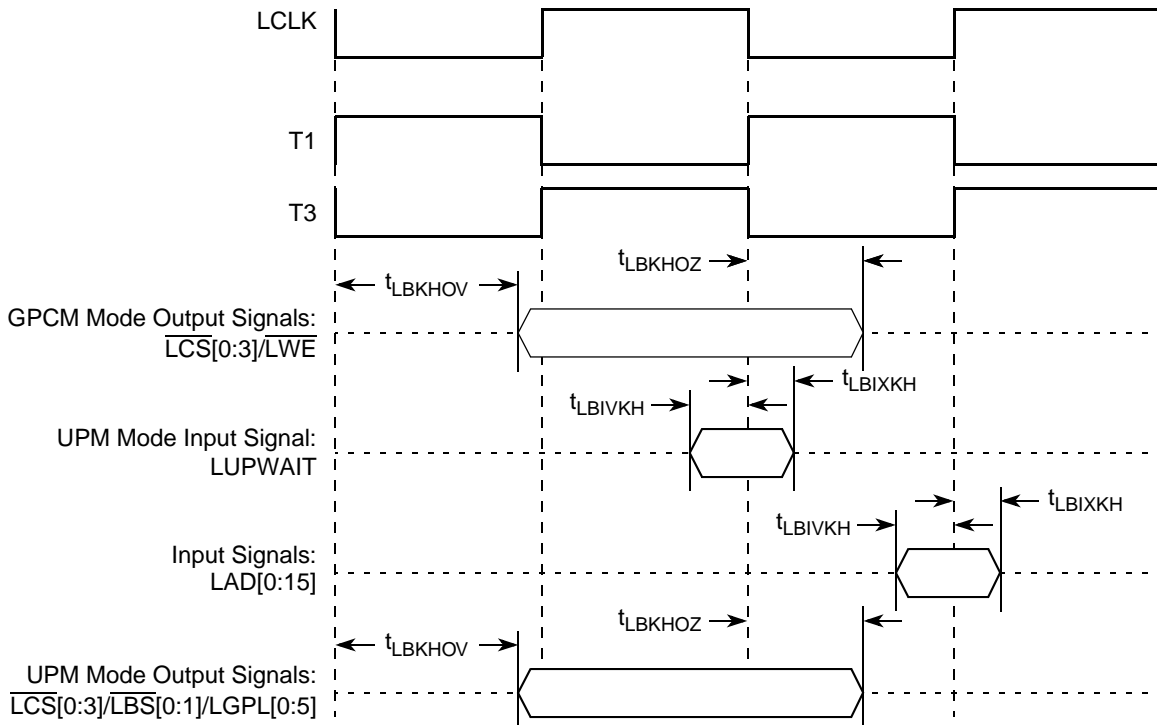


Figure 38. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2

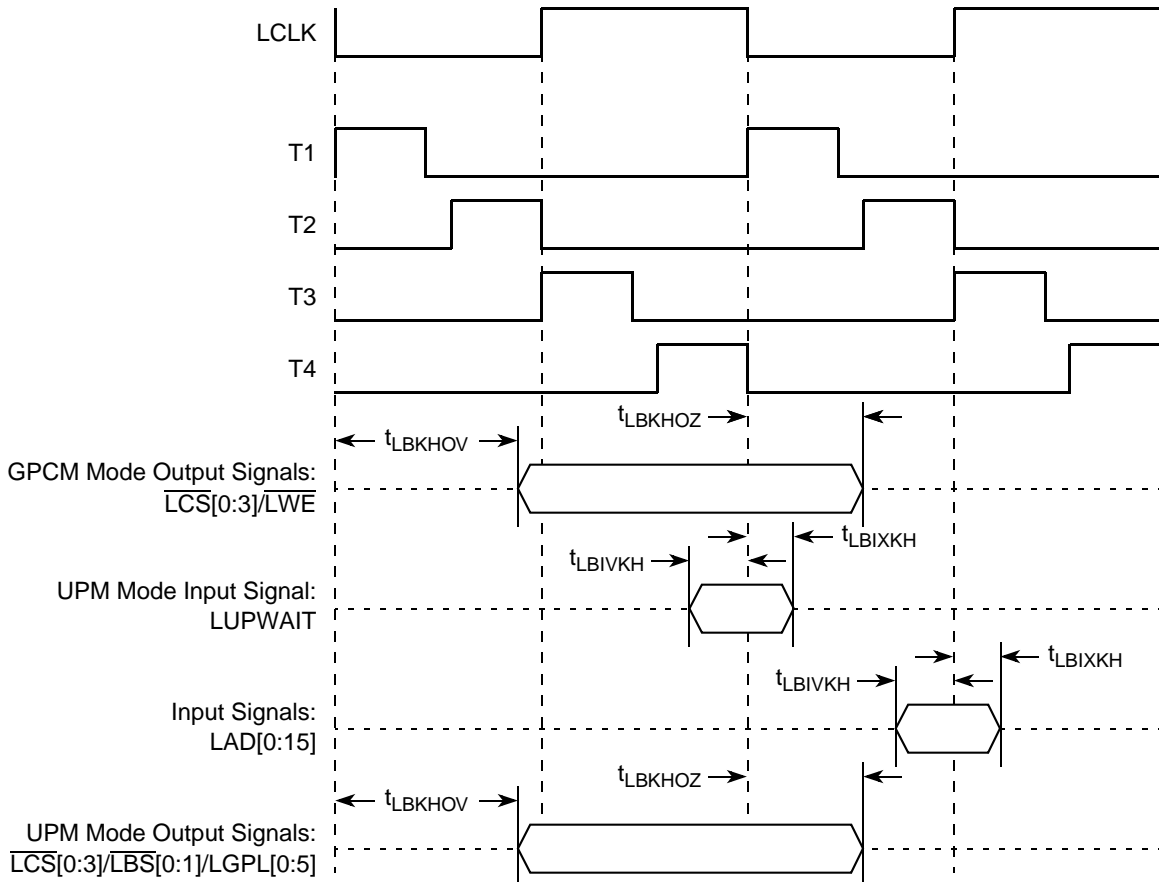


Figure 39. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4

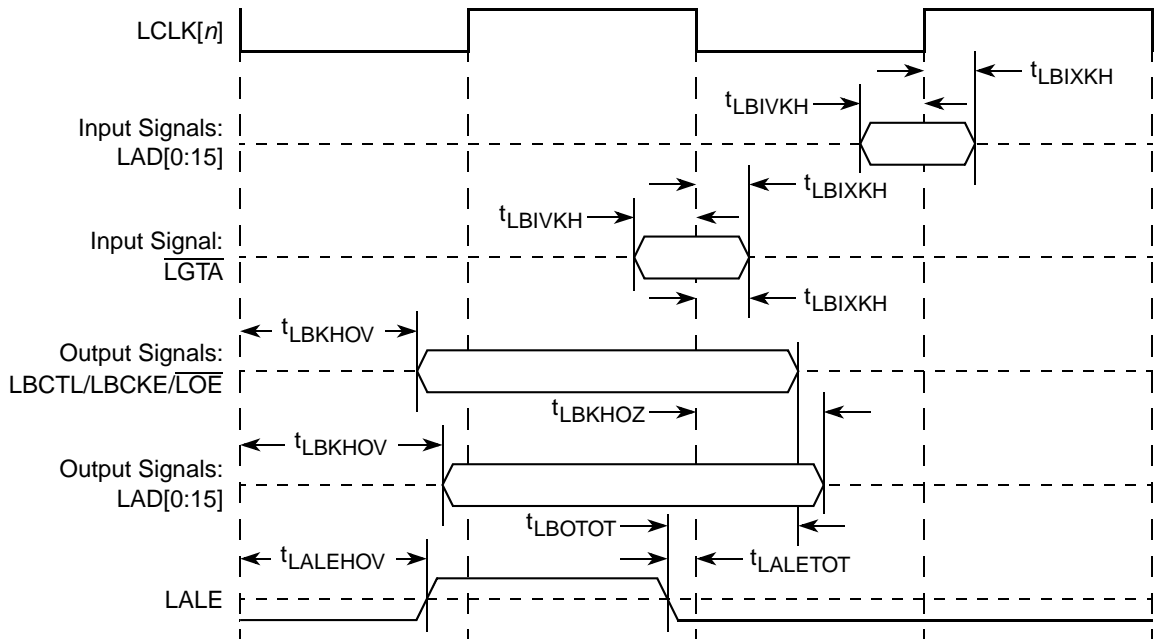


Figure 40. Local Bus Signals, LALE with Respect to LCLK

12 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std 1149.1™ (JTAG) interface.

12.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the IEEE Std 1149.1 (JTAG) interface.

Table 46. JTAG Interface DC Electrical Characteristics

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---------------------|----------|--------------------|------|-----------------|---------|
| Input high voltage | V_{IH} | — | 2.1 | $NV_{DD} + 0.3$ | V |
| Input low voltage | V_{IL} | — | -0.3 | 0.8 | V |
| Input current | I_{IN} | — | — | ± 5 | μA |
| Output high voltage | V_{OH} | $I_{OH} = -8.0$ mA | 2.4 | — | V |
| Output low voltage | V_{OL} | $I_{OL} = 8.0$ mA | — | 0.5 | V |
| Output low voltage | V_{OL} | $I_{OL} = 3.2$ mA | — | 0.4 | V |

12.2 JTAG AC Timing Specifications

This section describes the AC electrical specifications for the IEEE Std 1149.1 (JTAG) interface. This table provides the JTAG AC timing specifications as defined in [Figure 41](#) through [Figure 45](#).

Table 47. JTAG AC Timing Specifications (Independent of SYS_CLK_IN)¹

At recommended operating conditions (see [Table 2](#)).

| Parameter | Symbol ² | Min | Max | Unit | Note |
|---|-------------------------|-----|------|------|------|
| JTAG external clock frequency of operation | f_{JTG} | 0 | 33.3 | MHz | |
| JTAG external clock cycle time | t_{JTG} | 30 | — | ns | |
| JTAG external clock pulse width measured at 1.4 V | t_{JTKHKL} | 15 | — | ns | |
| JTAG external clock rise and fall times | t_{JTGR} & t_{JTGF} | 0 | 2 | ns | |
| \overline{TRST} assert time | t_{TRST} | 25 | — | ns | 3 |
| Input setup times: | | | | ns | |
| Boundary-scan data | t_{JTDVKH} | 4 | — | | 4 |
| TMS, TDI | t_{JTIVKH} | 4 | — | | |
| Input hold times: | | | | ns | |
| Boundary-scan data | t_{JTDXKH} | 10 | — | | 4 |
| TMS, TDI | t_{JTIXKH} | 10 | — | | |
| Valid times: | | | | ns | |
| Boundary-scan data | t_{JTKLDV} | 2 | 11 | | 5 |
| TDO | t_{JTKLOV} | 2 | 11 | | |
| Output hold times: | | | | ns | |
| Boundary-scan data | t_{JTKLDX} | 2 | — | | 5 |
| TDO | t_{JTKLOX} | 2 | — | | |

Table 47. JTAG AC Timing Specifications (Independent of SYS_CLK_IN)¹ (continued)

At recommended operating conditions (see Table 2).

| Parameter | Symbol ² | Min | Max | Unit | Note |
|---|---------------------|-----|-----|------|------|
| JTAG external clock to output high impedance: | | | | | |
| Boundary-scan data | t_{JTKLDZ} | 2 | 19 | ns | 5, 6 |
| TDO | t_{JTKLOZ} | 2 | 9 | | |

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50- Ω load (see Figure 34). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{\text{JT D V K H}}$ symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the $t_{\text{J T G}}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{\text{J T D X K H}}$ symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the $t_{\text{J T G}}$ clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK} .
5. Non-JTAG signal output timing with respect to t_{TCLK} .
6. Guaranteed by design and characterization.

This figure provides the AC test load for TDO and the boundary-scan outputs.

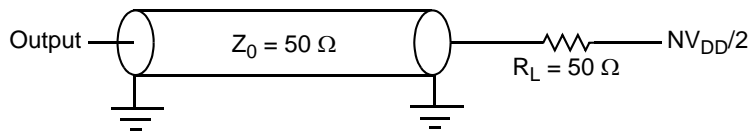


Figure 41. AC Test Load for the JTAG Interface

This figure provides the JTAG clock input timing diagram.

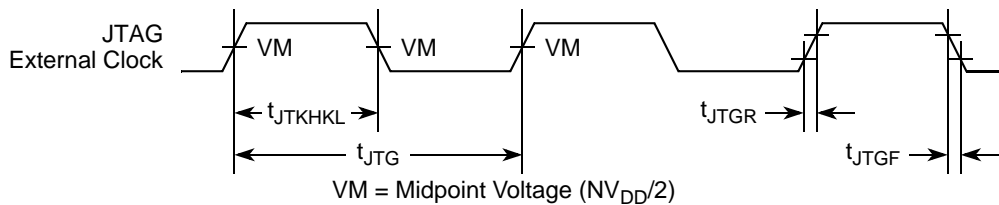


Figure 42. JTAG Clock Input Timing Diagram

This figure provides the $\overline{\text{TRST}}$ timing diagram.



Figure 43. $\overline{\text{TRST}}$ Timing Diagram

This figure provides the boundary-scan timing diagram.

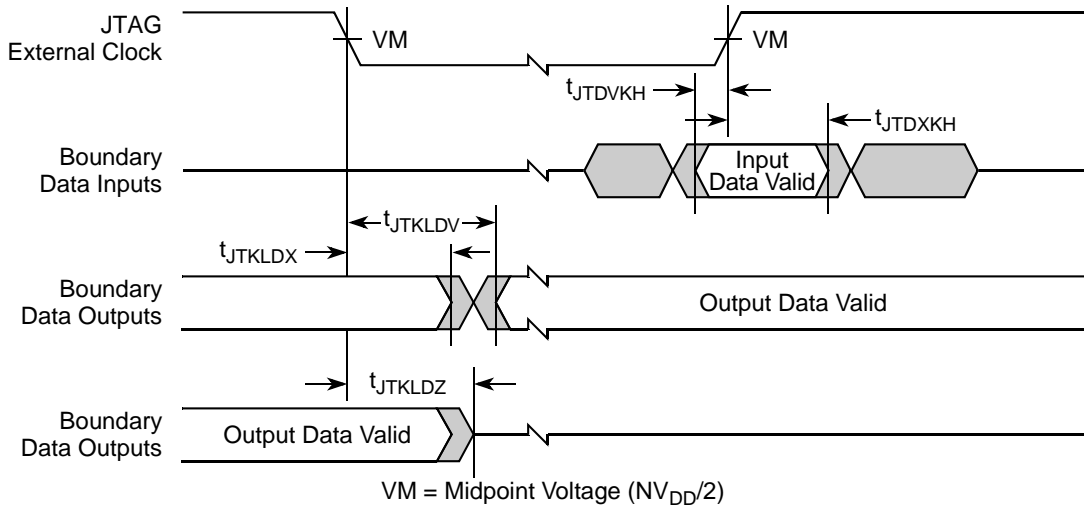


Figure 44. Boundary-Scan Timing Diagram

This figure provides the test access port timing diagram.

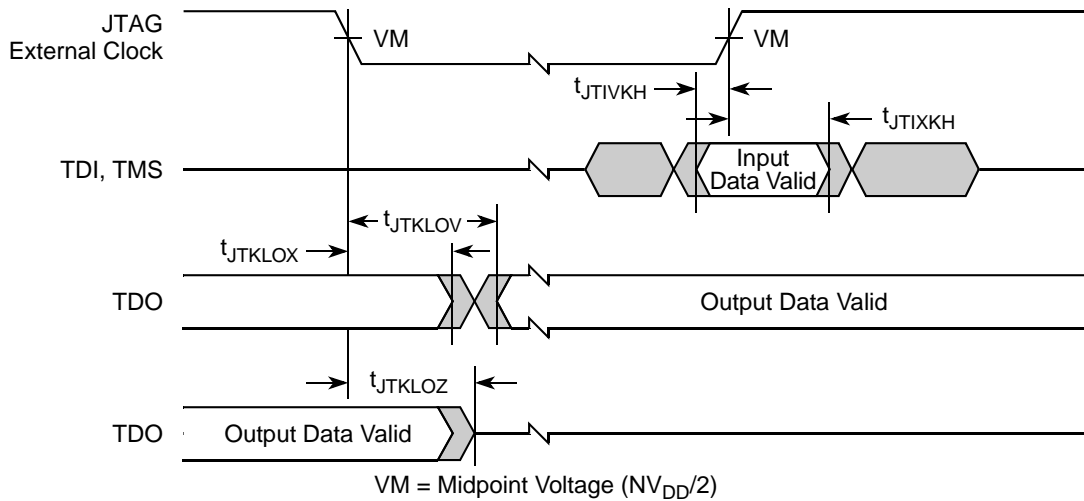


Figure 45. Test Access Port Timing Diagram

13 I²C

This section describes the DC and AC electrical characteristics for the I²C interface.

13.1 I²C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I²C interface.

Table 48. I²C DC Electrical Characteristics

At recommended operating conditions with NV_{DD} of 3.3 V ± 0.3 V.

| Parameter | Symbol | Min | Max | Unit | Note |
|---|--------------------|---------------------------|------------------------|------|------|
| Input high voltage level | V _{IH} | 0.7 × NV _{DD} | NV _{DD} + 0.3 | V | |
| Input low voltage level | V _{IL} | -0.3 | 0.3 × NV _{DD} | V | |
| Low level output voltage | V _{OL} | 0 | 0.2 × NV _{DD} | V | 1 |
| Output fall time from V _{IH} (min) to V _{IL} (max) with a bus capacitance from 10 to 400 pF | t _{12KLV} | 20 + 0.1 × C _B | 250 | ns | 2 |
| Pulse width of spikes which must be suppressed by the input filter | t _{12KHL} | 0 | 50 | ns | 3 |
| Capacitance for each I/O pin | C _I | — | 10 | pF | |
| Input current, (0 V ≤ V _{IN} ≤ NV _{DD}) | I _{IN} | — | ± 5 | μA | 4 |

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. Refer to the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual*, for information on the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if NV_{DD} is switched off.

13.2 I²C AC Electrical Specifications

This table provides the AC timing parameters for the I²C interface.

Table 49. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 48).

| Parameter | Symbol ¹ | Min | Max | Unit |
|--|---------------------|-----|-----|------|
| SCL clock frequency | f _{12C} | 0 | 400 | kHz |
| Low period of the SCL clock | t _{12CL} | 1.3 | — | μs |
| High period of the SCL clock | t _{12CH} | 0.6 | — | μs |
| Setup time for a repeated START condition | t _{12SVKH} | 0.6 | — | μs |
| Hold time (repeated) START condition (after this period, the first clock pulse is generated) | t _{12SXKL} | 0.6 | — | μs |
| Data setup time | t _{12DVKH} | 100 | — | ns |

Table 49. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 48).

| Parameter | Symbol ¹ | Min | Max | Unit |
|---|---------------------|----------------------|-----------------------|---------------|
| Data hold time: CBUS compatible masters I ² C bus devices | t_{I2DXKL} | — 0 ² | — 0.9 ³ | μs |
| Fall time of both SDA and SCL signals ⁵ | t_{I2CF} | — | 300 | ns |
| Setup time for STOP condition | t_{I2PVKH} | 0.6 | — | μs |
| Bus free time between a STOP and START condition | t_{I2KHDX} | 1.3 | — | μs |
| Noise margin at the LOW level for each connected device (including hysteresis) | V_{NL} | $0.1 \times NV_{DD}$ | — | V |
| Noise margin at the HIGH level for each connected device (including hysteresis) | V_{NH} | $0.2 \times NV_{DD}$ | — | V |

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- The MPC8313E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
- C_B = capacitance of one bus line in pF.
- The MPC8313E does not follow the *I²C-BUS Specifications, Version 2.1*, regarding the t_{I2CF} AC parameter.

This figure provides the AC test load for the I²C.

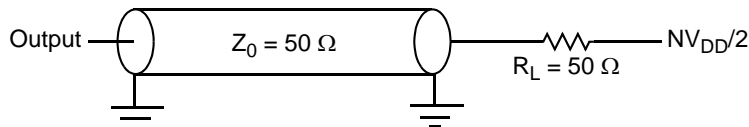


Figure 46. I²C AC Test Load

This figure shows the AC timing diagram for the I²C bus.

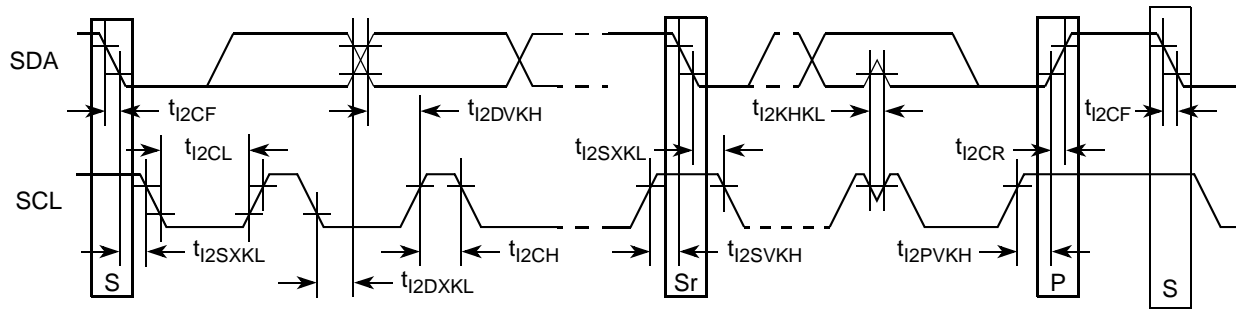


Figure 47. I²C Bus AC Timing Diagram

14 PCI

This section describes the DC and AC electrical specifications for the PCI bus.

14.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface.

Table 50. PCI DC Electrical Characteristics¹

| Parameter | Symbol | Test Condition | Min | Max | Unit |
|---------------------------|----------|---|----------------------|----------------------|---------------|
| High-level input voltage | V_{IH} | $V_{OUT} \geq V_{OH} (\text{min})$ or | $0.5 \times NV_{DD}$ | $NV_{DD} + 0.3$ | V |
| Low-level input voltage | V_{IL} | $V_{OUT} \leq V_{OL} (\text{max})$ | -0.5 | $0.3 \times NV_{DD}$ | V |
| High-level output voltage | V_{OH} | $NV_{DD} = \text{min}, I_{OH} = -100 \mu\text{A}$ | $0.9 \times NV_{DD}$ | — | V |
| Low-level output voltage | V_{OL} | $NV_{DD} = \text{min}, I_{OL} = 100 \mu\text{A}$ | — | $0.1 \times NV_{DD}$ | V |
| Input current | I_{IN} | $0 \text{ V} \leq V_{IN} \leq NV_{DD}$ | — | ± 5 | μA |

Note:

- Note that the symbol V_{IN} , in this case, represents the NV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

14.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the MPC8313E is configured as a host or agent device.

This table shows the PCI AC timing specifications at 66 MHz.

Table 51. PCI AC Timing Specifications at 66 MHz

| Parameter | Symbol ¹ | Min | Max | Unit | Note |
|------------------------|---------------------|-----|-----|------|------|
| Clock to output valid | t_{PCKHOV} | — | 6.0 | ns | 2 |
| Output hold from clock | t_{PCKHOX} | 1 | — | ns | 2 |

Table 51. PCI AC Timing Specifications at 66 MHz (continued)

| Parameter | Symbol ¹ | Min | Max | Unit | Note |
|--------------------------------|---------------------|-----|-----|------|------|
| Clock to output high impedance | t_{PCKHOZ} | — | 14 | ns | 2, 3 |
| Input setup to clock | t_{PCIVKH} | 3.0 | — | ns | 2, 4 |
| Input hold from clock | t_{PCIXKH} | 0 | — | ns | 2, 4 |

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS} , reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

This table shows the PCI AC timing specifications at 33 MHz.

Table 52. PCI AC Timing Specifications at 33 MHz

| Parameter | Symbol ¹ | Min | Max | Unit | Note |
|--------------------------------|---------------------|-----|-----|------|------|
| Clock to output valid | t_{PCKHOV} | — | 11 | ns | 2 |
| Output hold from clock | t_{PCKHOX} | 2 | — | ns | 2 |
| Clock to output high impedance | t_{PCKHOZ} | — | 14 | ns | 2, 3 |
| Input setup to clock | t_{PCIVKH} | 3.0 | — | ns | 2, 4 |
| Input hold from clock | t_{PCIXKH} | 0 | — | ns | 2, 4 |

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS} , reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

This figure provides the AC test load for PCI.

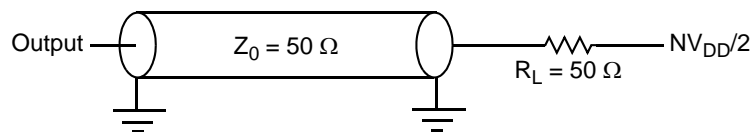


Figure 48. PCI AC Test Load

This figure shows the PCI input AC timing conditions.

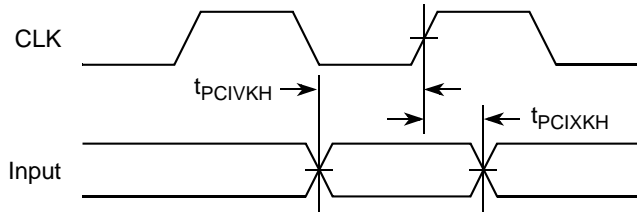


Figure 49. PCI Input AC Timing Measurement Conditions

This figure shows the PCI output AC timing conditions.

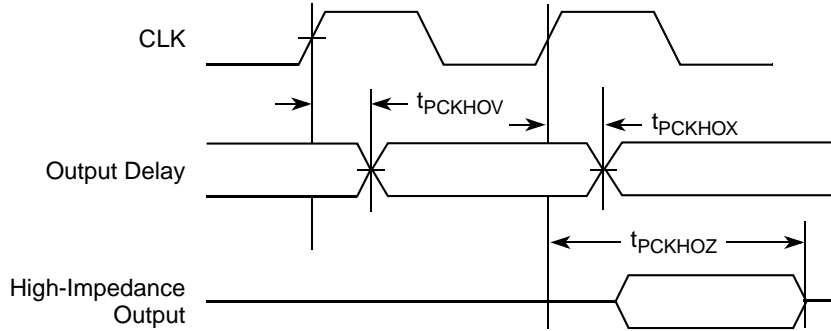


Figure 50. PCI Output AC Timing Measurement Condition

15 Timers

This section describes the DC and AC electrical specifications for the timers.

15.1 Timers DC Electrical Characteristics

This table provides the DC electrical characteristics for the MPC8313E timers pins, including \overline{TIN} , \overline{TOUT} , \overline{TGATE} , and RTC_CLK.

Table 53. Timers DC Electrical Characteristics

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---------------------|----------|--|------|-----------------|---------------|
| Output high voltage | V_{OH} | $I_{OH} = -8.0 \text{ mA}$ | 2.4 | — | V |
| Output low voltage | V_{OL} | $I_{OL} = 8.0 \text{ mA}$ | — | 0.5 | V |
| Output low voltage | V_{OL} | $I_{OL} = 3.2 \text{ mA}$ | — | 0.4 | V |
| Input high voltage | V_{IH} | — | 2.1 | $NV_{DD} + 0.3$ | V |
| Input low voltage | V_{IL} | — | -0.3 | 0.8 | V |
| Input current | I_{IN} | $0 \text{ V} \leq V_{IN} \leq NV_{DD}$ | — | ± 5 | μA |

15.2 Timers AC Timing Specifications

This table provides the Timers input and output AC timing specifications.

Table 54. Timers Input AC Timing Specifications¹

| Characteristic | Symbol ² | Min | Unit |
|-----------------------------------|---------------------|-----|------|
| Timers inputs—minimum pulse width | t_{TIVID} | 20 | ns |

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.
2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIVID} ns to ensure proper operation

This figure provides the AC test load for the Timers.

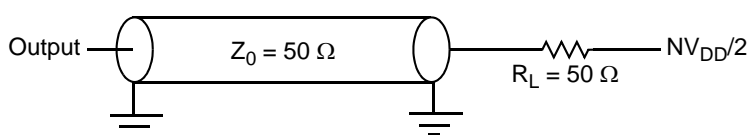


Figure 51. Timers AC Test Load

16 GPIO

This section describes the DC and AC electrical specifications for the GPIO.

16.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the GPIO when the GPIO pins are operating from a 3.3-V supply.

Table 55. GPIO (When Operating at 3.3 V) DC Electrical Characteristics

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---------------------|----------|--|------|-----------------|---------------|
| Output high voltage | V_{OH} | $I_{OH} = -8.0 \text{ mA}$ | 2.4 | — | V |
| Output low voltage | V_{OL} | $I_{OL} = 8.0 \text{ mA}$ | — | 0.5 | V |
| Output low voltage | V_{OL} | $I_{OL} = 3.2 \text{ mA}$ | — | 0.4 | V |
| Input high voltage | V_{IH} | — | 2.0 | $NV_{DD} + 0.3$ | V |
| Input low voltage | V_{IL} | — | -0.3 | 0.8 | V |
| Input current | I_{IN} | $0 \text{ V} \leq V_{IN} \leq NV_{DD}$ | — | ± 5 | μA |

Note:

1. This specification only applies to GPIO pins that are operating from a 3.3-V supply. See [Table 62](#) for the power supply listed for the individual GPIO signal.

This table provides the DC electrical characteristics for the GPIO when the GPIO pins are operating from a 2.5-V supply.

Table 56. GPIO (When Operating at 2.5 V) DC Electrical Characteristics¹

| Parameters | Symbol | Conditions | | Min | Max | Unit |
|----------------------|-----------|----------------------------|------------------------|----------------|-----------------|---------------|
| Supply voltage 2.5 V | NV_{DD} | — | | 2.37 | 2.63 | V |
| Output high voltage | V_{OH} | $I_{OH} = -1.0 \text{ mA}$ | $NV_{DD} = \text{min}$ | 2.00 | $NV_{DD} + 0.3$ | V |
| Output low voltage | V_{OL} | $I_{OL} = 1.0 \text{ mA}$ | $NV_{DD} = \text{min}$ | $V_{SS} - 0.3$ | 0.40 | V |
| Input high voltage | V_{IH} | — | $NV_{DD} = \text{min}$ | 1.7 | $NV_{DD} + 0.3$ | V |
| Input low voltage | V_{IL} | — | $NV_{DD} = \text{min}$ | -0.3 | 0.70 | V |
| Input high current | I_{IH} | $V_{IN} = NV_{DD}$ | | — | 10 | μA |
| Input low current | I_{IL} | $V_{IN} = V_{SS}$ | | -15 | — | μA |

Note:

1. This specification only applies to GPIO pins that are operating from a 2.5-V supply. See [Table 62](#) for the power supply listed for the individual GPIO signal

16.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 57. GPIO Input AC Timing Specifications¹

| Characteristic | Symbol ² | Min | Unit |
|---------------------------------|---------------------|-----|------|
| GPIO inputs—minimum pulse width | t_{PIWID} | 20 | ns |

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

This figure provides the AC test load for the GPIO.

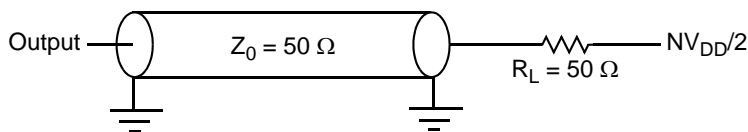


Figure 52. GPIO AC Test Load

17 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins.

17.1 IPIC DC Electrical Characteristics

This table provides the DC electrical characteristics for the external interrupt pins.

Table 58. IPIC DC Electrical Characteristics

| Characteristic | Symbol | Condition | Min | Max | Unit |
|--------------------|----------|---------------------------|------|-----------------|---------|
| Input high voltage | V_{IH} | — | 2.1 | $NV_{DD} + 0.3$ | V |
| Input low voltage | V_{IL} | — | -0.3 | 0.8 | V |
| Input current | I_{IN} | — | — | ± 5 | μA |
| Output low voltage | V_{OL} | $I_{OL} = 8.0 \text{ mA}$ | — | 0.5 | V |
| Output low voltage | V_{OL} | $I_{OL} = 3.2 \text{ mA}$ | — | 0.4 | V |

17.2 IPIC AC Timing Specifications

This table provides the IPIC input and output AC timing specifications.

Table 59. IPIC Input AC Timing Specifications¹

| Characteristic | Symbol ² | Min | Unit |
|---------------------------------|---------------------|-----|------|
| IPIC inputs—minimum pulse width | t_{PIWID} | 20 | ns |

Note:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

18 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8313E.

18.1 SPI DC Electrical Characteristics

This table provides the DC electrical characteristics for the MPC8313E SPI.

Table 60. SPI DC Electrical Characteristics

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---------------------|----------|----------------------------|-----|-----|------|
| Output high voltage | V_{OH} | $I_{OH} = -6.0 \text{ mA}$ | 2.4 | — | V |
| Output low voltage | V_{OL} | $I_{OL} = 6.0 \text{ mA}$ | — | 0.5 | V |
| Output low voltage | V_{OL} | $I_{OL} = 3.2 \text{ mA}$ | — | 0.4 | V |

Table 60. SPI DC Electrical Characteristics (continued)

| Characteristic | Symbol | Condition | Min | Max | Unit |
|--------------------|----------|---------------------------------------|------|-----------------|---------------|
| Input high voltage | V_{IH} | — | 2.1 | $NV_{DD} + 0.3$ | V |
| Input low voltage | V_{IL} | — | -0.3 | 0.8 | V |
| Input current | I_{IN} | $0\text{ V} \leq V_{IN} \leq NV_{DD}$ | — | ± 5 | μA |

18.2 SPI AC Timing Specifications

This table and provide the SPI input and output AC timing specifications.

Table 61. SPI AC Timing Specifications¹

| Characteristic | Symbol ² | Min | Max | Unit |
|--|---------------------|-----|-----|------|
| SPI outputs—master mode (internal clock) delay | $t_{NIKH OV}$ | 0.5 | 6 | ns |
| SPI outputs—slave mode (external clock) delay | $t_{NEKH OV}$ | 2 | 8 | ns |
| SPI inputs—master mode (internal clock) input setup time | t_{NIIVKH} | 6 | — | ns |
| SPI inputs—master mode (internal clock) input hold time | t_{NIIXKH} | 0 | — | ns |
| SPI inputs—slave mode (external clock) input setup time | t_{NEIVKH} | 4 | — | ns |
| SPI inputs—slave mode (external clock) input hold time | t_{NEIXKH} | 2 | — | ns |

Note:

1. Output specifications are measured from the 50% level of the rising edge of SYS_CLK_IN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{NIKH OV}$ symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).

This figure provides the AC test load for the SPI.

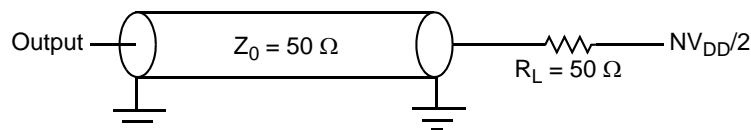


Figure 53. SPI AC Test Load

Figure 54 and Figure 55 represent the AC timing from Table 61. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the SPI timing in slave mode (external clock).

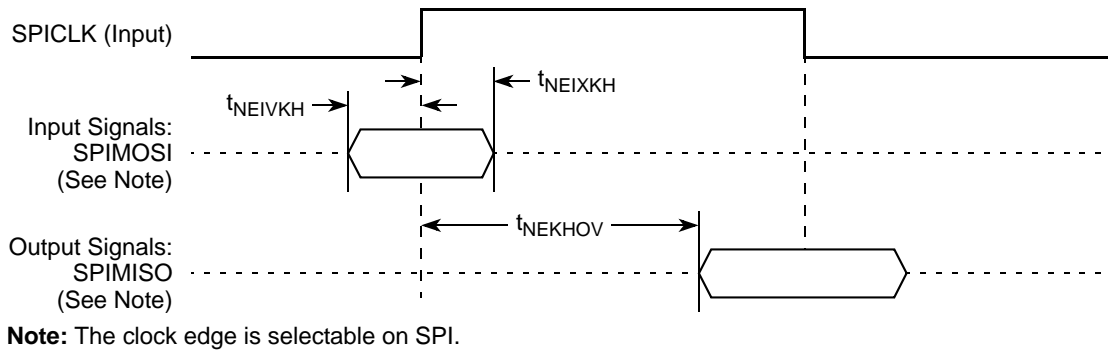


Figure 54. SPI AC Timing in Slave Mode (External Clock) Diagram

This figure shows the SPI timing in master mode (internal clock).

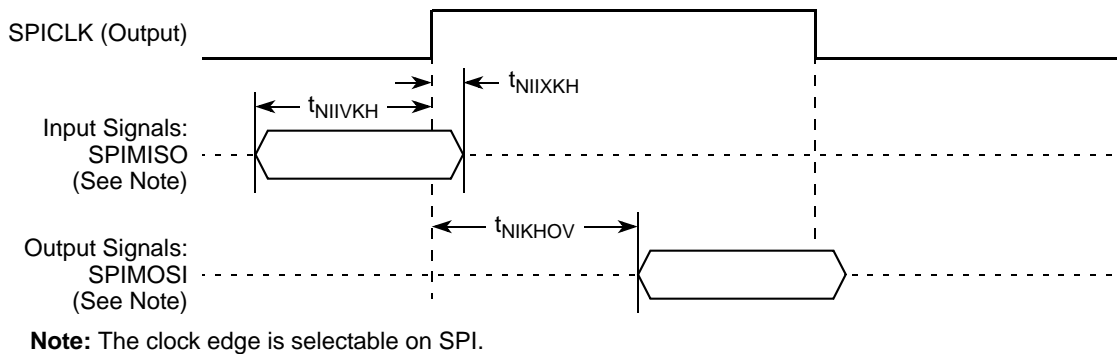


Figure 55. SPI AC Timing in Master Mode (Internal Clock) Diagram

19 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8313E is available in a thermally enhanced plastic ball grid array (TEPBGAII), see [Section 19.1, “Package Parameters for the MPC8313E TEPBGAII,”](#) and [Section 19.2, “Mechanical Dimensions of the MPC8313E TEPBGAII,”](#) for information on the TEPBGAII.

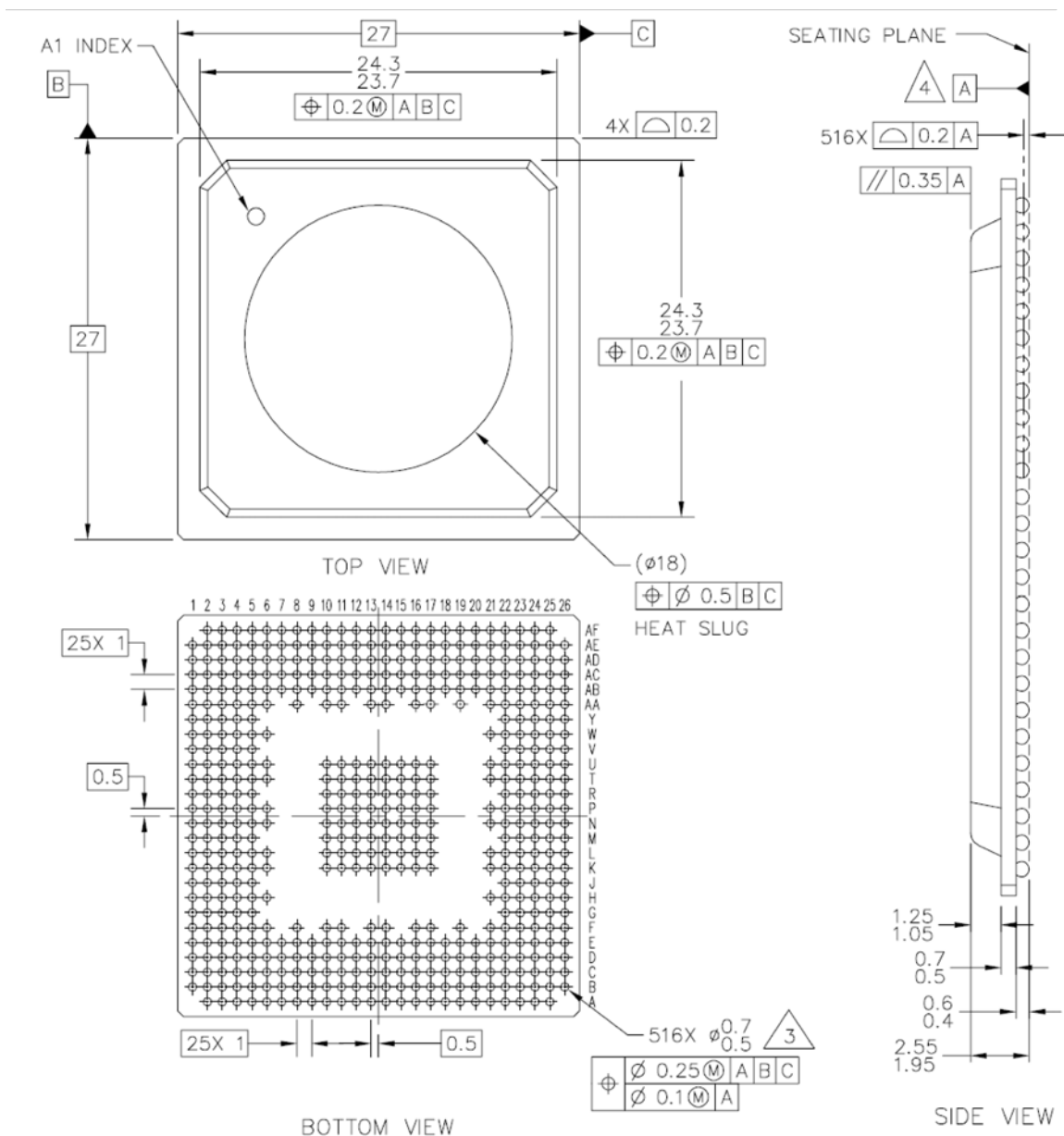
19.1 Package Parameters for the MPC8313E TEPBGAII

The package parameters are as provided in the following list. The package type is 27 mm × 27 mm, 516 TEPBGAII.

| | |
|-------------------------|--|
| Package outline | 27 mm × 27 mm |
| Interconnects | 516 |
| Pitch | 1.00 mm |
| Module height (typical) | 2.25 mm |
| Solder Balls | 96.5 Sn/3.5 Ag (VR package) , 62 Sn/36 Pb/2 Ag (ZQ package) Ball diameter (typical) |
| 0.6 mm | |

19.2 Mechanical Dimensions of the MPC8313E TEPBGAI

This figure shows the mechanical dimensions and bottom surface nomenclature of the 516-TEPBGAI package.



Notes:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Package code 5368 is to account for PGE and the built-in heat spreader.

Figure 56. Mechanical Dimension and Bottom Surface Nomenclature of the MPC8313E TEPBGAI

19.3 Pinout Listings

This table provides the pin-out listing for the MPC8313E, TEPBGAI package.

Table 62. MPC8313E TEPBGAI Pinout Listing

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|--|--------------------|----------|------------------|------|
| DDR Memory Controller Interface | | | | |
| MEMC_MDQ0 | A8 | I/O | GV _{DD} | — |
| MEMC_MDQ1 | A9 | I/O | GV _{DD} | — |
| MEMC_MDQ2 | C10 | I/O | GV _{DD} | — |
| MEMC_MDQ3 | C9 | I/O | GV _{DD} | — |
| MEMC_MDQ4 | E9 | I/O | GV _{DD} | — |
| MEMC_MDQ5 | E11 | I/O | GV _{DD} | — |
| MEMC_MDQ6 | E10 | I/O | GV _{DD} | — |
| MEMC_MDQ7 | C8 | I/O | GV _{DD} | — |
| MEMC_MDQ8 | E8 | I/O | GV _{DD} | — |
| MEMC_MDQ9 | A6 | I/O | GV _{DD} | — |
| MEMC_MDQ10 | B6 | I/O | GV _{DD} | — |
| MEMC_MDQ11 | C6 | I/O | GV _{DD} | — |
| MEMC_MDQ12 | C7 | I/O | GV _{DD} | — |
| MEMC_MDQ13 | D7 | I/O | GV _{DD} | — |
| MEMC_MDQ14 | D6 | I/O | GV _{DD} | — |
| MEMC_MDQ15 | A5 | I/O | GV _{DD} | — |
| MEMC_MDQ16 | A19 | I/O | GV _{DD} | — |
| MEMC_MDQ17 | D18 | I/O | GV _{DD} | — |
| MEMC_MDQ18 | A17 | I/O | GV _{DD} | — |
| MEMC_MDQ19 | E17 | I/O | GV _{DD} | — |
| MEMC_MDQ20 | E16 | I/O | GV _{DD} | — |
| MEMC_MDQ21 | C18 | I/O | GV _{DD} | — |
| MEMC_MDQ22 | D19 | I/O | GV _{DD} | — |
| MEMC_MDQ23 | C19 | I/O | GV _{DD} | — |
| MEMC_MDQ24 | E19 | I/O | GV _{DD} | — |
| MEMC_MDQ25 | A22 | I/O | GV _{DD} | — |
| MEMC_MDQ26 | C21 | I/O | GV _{DD} | — |
| MEMC_MDQ27 | C20 | I/O | GV _{DD} | — |
| MEMC_MDQ28 | A21 | I/O | GV _{DD} | — |

Table 62. MPC8313E TEPBGAI Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|------------|--------------------|----------|------------------|------|
| MEMC_MDQ29 | A20 | I/O | GV _{DD} | — |
| MEMC_MDQ30 | C22 | I/O | GV _{DD} | — |
| MEMC_MDQ31 | B22 | I/O | GV _{DD} | — |
| MEMC_MDM0 | B7 | O | GV _{DD} | — |
| MEMC_MDM1 | E6 | O | GV _{DD} | — |
| MEMC_MDM2 | E18 | O | GV _{DD} | — |
| MEMC_MDM3 | E20 | O | GV _{DD} | — |
| MEMC_MDQS0 | A7 | I/O | GV _{DD} | — |
| MEMC_MDQS1 | E7 | I/O | GV _{DD} | — |
| MEMC_MDQS2 | B19 | I/O | GV _{DD} | — |
| MEMC_MDQS3 | A23 | I/O | GV _{DD} | — |
| MEMC_MBA0 | D15 | O | GV _{DD} | — |
| MEMC_MBA1 | A18 | O | GV _{DD} | — |
| MEMC_MBA2 | A15 | O | GV _{DD} | — |
| MEMC_MA0 | E12 | O | GV _{DD} | — |
| MEMC_MA1 | D11 | O | GV _{DD} | — |
| MEMC_MA2 | B11 | O | GV _{DD} | — |
| MEMC_MA3 | A11 | O | GV _{DD} | — |
| MEMC_MA4 | A12 | O | GV _{DD} | — |
| MEMC_MA5 | E13 | O | GV _{DD} | — |
| MEMC_MA6 | C12 | O | GV _{DD} | — |
| MEMC_MA7 | E14 | O | GV _{DD} | — |
| MEMC_MA8 | B15 | O | GV _{DD} | — |
| MEMC_MA9 | C17 | O | GV _{DD} | — |
| MEMC_MA10 | C13 | O | GV _{DD} | — |
| MEMC_MA11 | A16 | O | GV _{DD} | — |
| MEMC_MA12 | C15 | O | GV _{DD} | — |
| MEMC_MA13 | C16 | O | GV _{DD} | — |
| MEMC_MA14 | E15 | O | GV _{DD} | — |
| MEMC_MWE | B18 | O | GV _{DD} | — |
| MEMC_MRAS | C11 | O | GV _{DD} | — |
| MEMC_MCAS | B10 | O | GV _{DD} | — |

Table 62. MPC8313E TEPBGAI Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---------------------------------------|--------------------|----------|-------------------------|------|
| $\overline{\text{MEMC_MCS0}}$ | D10 | O | GV_{DD} | — |
| $\overline{\text{MEMC_MCS1}}$ | A10 | O | GV_{DD} | — |
| MEMC_MCKE | B14 | O | GV_{DD} | 3 |
| MEMC_MCK | A13 | O | GV_{DD} | — |
| $\overline{\text{MEMC_MCK}}$ | A14 | O | GV_{DD} | — |
| MEMC_MODT0 | B23 | O | GV_{DD} | — |
| MEMC_MODT1 | C23 | O | GV_{DD} | — |
| Local Bus Controller Interface | | | | |
| LAD0 | K25 | I/O | LV_{DD} | 11 |
| LAD1 | K24 | I/O | LV_{DD} | 11 |
| LAD2 | K23 | I/O | LV_{DD} | 11 |
| LAD3 | K22 | I/O | LV_{DD} | 11 |
| LAD4 | J25 | I/O | LV_{DD} | 11 |
| LAD5 | J24 | I/O | LV_{DD} | 11 |
| LAD6 | J23 | I/O | LV_{DD} | 11 |
| LAD7 | J22 | I/O | LV_{DD} | 11 |
| LAD8 | H24 | I/O | LV_{DD} | 11 |
| LAD9 | F26 | I/O | LV_{DD} | 11 |
| LAD10 | G24 | I/O | LV_{DD} | 11 |
| LAD11 | F25 | I/O | LV_{DD} | 11 |
| LAD12 | E25 | I/O | LV_{DD} | 11 |
| LAD13 | F24 | I/O | LV_{DD} | 11 |
| LAD14 | G22 | I/O | LV_{DD} | 11 |
| LAD15 | F23 | I/O | LV_{DD} | 11 |
| LA16 | AC25 | O | LV_{DD} | 11 |
| LA17 | AC26 | O | LV_{DD} | 11 |
| LA18 | AB22 | O | LV_{DD} | 11 |
| LA19 | AB23 | O | LV_{DD} | 11 |
| LA20 | AB24 | O | LV_{DD} | 11 |
| LA21 | AB25 | O | LV_{DD} | 11 |
| LA22 | AB26 | O | LV_{DD} | 11 |
| LA23 | E22 | O | LV_{DD} | 11 |

Table 62. MPC8313E TEPBGAI Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|--|--------------------|----------|------------------|------|
| LA24 | E23 | O | LV _{DD} | 11 |
| LA25 | D22 | O | LV _{DD} | 11 |
| $\overline{\text{LCS0}}$ | D23 | O | LV _{DD} | 10 |
| $\overline{\text{LCS1}}$ | J26 | O | LV _{DD} | 10 |
| $\overline{\text{LCS2}}$ | F22 | O | LV _{DD} | 10 |
| $\overline{\text{LCS3}}$ | D26 | O | LV _{DD} | 10 |
| $\overline{\text{LWE0/LFWE}}$ | E24 | O | LV _{DD} | 10 |
| $\overline{\text{LWE1}}$ | H26 | O | LV _{DD} | 10 |
| LBCTL | L22 | O | LV _{DD} | 10 |
| LALE/M1LALE/M2LALE | E26 | O | LV _{DD} | 11 |
| LGPL0/LFCLE | AA23 | O | LV _{DD} | — |
| LGPL1/LFALE | AA24 | O | LV _{DD} | — |
| LGPL2/ $\overline{\text{LOE/LFRE}}$ | AA25 | O | LV _{DD} | 10 |
| LGPL3/ $\overline{\text{LFWP}}$ | AA26 | O | LV _{DD} | — |
| LGPL4/ $\overline{\text{LGTA/LUPWAIT/LFRB}}$ | Y22 | I/O | LV _{DD} | 2 |
| LGPL5 | E21 | O | LV _{DD} | 10 |
| LCLK0 | H22 | O | LV _{DD} | 11 |
| LCLK1 | G26 | O | LV _{DD} | 11 |
| LA0/GPIO0/MSRCID0 | AC24 | I/O | LV _{DD} | — |
| LA1/GPIO1/MSRCID1 | Y24 | I/O | LV _{DD} | — |
| LA2/GPIO2/MSRCID2 | Y26 | I/O | LV _{DD} | — |
| LA3/GPIO3/MSRCID3 | W22 | I/O | LV _{DD} | — |
| LA4/GPIO4/MSRCID4 | W24 | I/O | LV _{DD} | — |
| LA5/GPIO5/MDVAL | W26 | I/O | LV _{DD} | — |
| LA6/GPIO6 | V22 | I/O | LV _{DD} | — |
| LA7/GPIO7/TSEC_1588_TRIG2 | V23 | I/O | LV _{DD} | 8 |
| LA8/GPIO13/TSEC_1588_ALARM1 | V24 | I/O | LV _{DD} | 8 |
| LA9/GPIO14/TSEC_1588_PP3 | V25 | I/O | LV _{DD} | 8 |
| LA10/TSEC_1588_CLK | V26 | O | LV _{DD} | 8 |
| LA11/TSEC_1588_GCLK | U22 | O | LV _{DD} | 8 |
| LA12/TSEC_1588_PP1 | AD24 | O | LV _{DD} | 8 |
| LA13/TSEC_1588_PP2 | L25 | O | LV _{DD} | 8 |

Table 62. MPC8313E TEPBGAI Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|-------------------------------------|--------------------|----------|------------------|------|
| LA14/TSEC_1588_TRIG1 | L24 | O | LV _{DD} | 8 |
| LA15/TSEC_1588_ALARM2 | K26 | O | LV _{DD} | 8 |
| DUART | | | | |
| UART_SOUT1/MSRCID0 | N2 | O | NV _{DD} | — |
| UART_SIN1/MSRCID1 | M5 | I/O | NV _{DD} | — |
| UART_CTS1/GPIO8/MSRCID2 | M1 | I/O | NV _{DD} | — |
| UART_RTS1/GPIO9/MSRCID3 | K1 | I/O | NV _{DD} | — |
| UART_SOUT2/MSRCID4/TSEC_1588_CLK | M3 | O | NV _{DD} | 8 |
| UART_SIN2/MDVAL/TSEC_1588_GCLK | L1 | I/O | NV _{DD} | 8 |
| UART_CTS2/TSEC_1588_PP1 | L5 | I/O | NV _{DD} | 8 |
| UART_RTS2/TSEC_1588_PP2 | L3 | I/O | NV _{DD} | 8 |
| I²C interface | | | | |
| IIC1_SDA/CKSTOP_OUT/TSEC_1588_TRIG1 | J4 | I/O | NV _{DD} | 2, 8 |
| IIC1_SCL/CKSTOP_IN/TSEC_1588_ALARM2 | J2 | I/O | NV _{DD} | 2, 8 |
| IIC2_SDA/PMC_PWR_OK/GPIO10 | J3 | I/O | NV _{DD} | 2 |
| IIC2_SCL/GPIO11 | H5 | I/O | NV _{DD} | 2 |
| Interrupts | | | | |
| MCP_OUT | G5 | O | NV _{DD} | 2 |
| IRQ0/MCP_IN | K5 | I | NV _{DD} | — |
| IRQ1 | K4 | I | NV _{DD} | — |
| IRQ2 | K2 | I | NV _{DD} | — |
| IRQ3/CKSTOP_OUT | K3 | I/O | NV _{DD} | — |
| IRQ4/CKSTOP_IN/GPIO12 | J1 | I/O | NV _{DD} | — |
| Configuration | | | | |
| CFG_CLKIN_DIV | D5 | I | NV _{DD} | — |
| EXT_PWR_CTRL | J5 | O | NV _{DD} | — |
| CFG_LBIU_MUX_EN | R24 | I | NV _{DD} | — |
| JTAG | | | | |
| TCK | E1 | I | NV _{DD} | — |
| TDI | E2 | I | NV _{DD} | 4 |
| TDO | E3 | O | NV _{DD} | 3 |

Table 62. MPC8313E TEPBGAI Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|-------------------------------------|--------------------|----------|------------------|------|
| TMS | E4 | I | NV _{DD} | 4 |
| $\overline{\text{TRST}}$ | E5 | I | NV _{DD} | 4 |
| TEST | | | | |
| TEST_MODE | F4 | I | NV _{DD} | 6 |
| DEBUG | | | | |
| $\overline{\text{QUIESCE}}$ | F5 | O | NV _{DD} | — |
| System Control | | | | |
| $\overline{\text{HRESET}}$ | F2 | I/O | NV _{DD} | 1 |
| $\overline{\text{PORESET}}$ | F3 | I | NV _{DD} | — |
| $\overline{\text{SRESET}}$ | F1 | I | NV _{DD} | — |
| Clocks | | | | |
| SYS_CR_CLK_IN | U26 | I | NV _{DD} | — |
| SYS_CR_CLK_OUT | U25 | O | NV _{DD} | — |
| SYS_CLK_IN | U23 | I | NV _{DD} | — |
| USB_CR_CLK_IN | T26 | I | NV _{DD} | — |
| USB_CR_CLK_OUT | R26 | O | NV _{DD} | — |
| USB_CLK_IN | T22 | I | NV _{DD} | — |
| PCI_SYNC_OUT | U24 | O | NV _{DD} | 3 |
| RTC_PIT_CLOCK | R22 | I | NV _{DD} | — |
| PCI_SYNC_IN | T24 | I | NV _{DD} | — |
| MISC | | | | |
| THERM0 | N1 | I | NV _{DD} | 7 |
| THERM1 | N3 | I | NV _{DD} | 7 |
| PCI | | | | |
| $\overline{\text{PCI_INTA}}$ | AF7 | O | NV _{DD} | — |
| $\overline{\text{PCI_RESET_OUT}}$ | AB11 | O | NV _{DD} | — |
| PCI_AD0 | AB20 | I/O | NV _{DD} | — |
| PCI_AD1 | AF23 | I/O | NV _{DD} | — |
| PCI_AD2 | AF22 | I/O | NV _{DD} | — |
| PCI_AD3 | AB19 | I/O | NV _{DD} | — |
| PCI_AD4 | AE22 | I/O | NV _{DD} | — |
| PCI_AD5 | AF21 | I/O | NV _{DD} | — |

Table 62. MPC8313E TEPBGAI Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|-----------|--------------------|----------|------------------|------|
| PCI_AD6 | AD19 | I/O | NV _{DD} | — |
| PCI_AD7 | AD20 | I/O | NV _{DD} | — |
| PCI_AD8 | AC18 | I/O | NV _{DD} | — |
| PCI_AD9 | AD18 | I/O | NV _{DD} | — |
| PCI_AD10 | AB18 | I/O | NV _{DD} | — |
| PCI_AD11 | AE19 | I/O | NV _{DD} | — |
| PCI_AD12 | AB17 | I/O | NV _{DD} | — |
| PCI_AD13 | AE18 | I/O | NV _{DD} | — |
| PCI_AD14 | AD17 | I/O | NV _{DD} | — |
| PCI_AD15 | AF19 | I/O | NV _{DD} | — |
| PCI_AD16 | AB14 | I/O | NV _{DD} | — |
| PCI_AD17 | AF15 | I/O | NV _{DD} | — |
| PCI_AD18 | AD14 | I/O | NV _{DD} | — |
| PCI_AD19 | AE14 | I/O | NV _{DD} | — |
| PCI_AD20 | AF12 | I/O | NV _{DD} | — |
| PCI_AD21 | AE11 | I/O | NV _{DD} | — |
| PCI_AD22 | AD12 | I/O | NV _{DD} | — |
| PCI_AD23 | AB13 | I/O | NV _{DD} | — |
| PCI_AD24 | AF9 | I/O | NV _{DD} | — |
| PCI_AD25 | AD11 | I/O | NV _{DD} | — |
| PCI_AD26 | AE10 | I/O | NV _{DD} | — |
| PCI_AD27 | AB12 | I/O | NV _{DD} | — |
| PCI_AD28 | AD10 | I/O | NV _{DD} | — |
| PCI_AD29 | AC10 | I/O | NV _{DD} | — |
| PCI_AD30 | AF10 | I/O | NV _{DD} | — |
| PCI_AD31 | AF8 | I/O | NV _{DD} | — |
| PCI_C/BE0 | AC19 | I/O | NV _{DD} | — |
| PCI_C/BE1 | AB15 | I/O | NV _{DD} | — |
| PCI_C/BE2 | AF14 | I/O | NV _{DD} | — |
| PCI_C/BE3 | AF11 | I/O | NV _{DD} | — |
| PCI_PAR | AD16 | I/O | NV _{DD} | — |
| PCI_FRAME | AF16 | I/O | NV _{DD} | 5 |

Table 62. MPC8313E TEPBGAI Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|--|--------------------|----------|-------------------|-------|
| $\overline{\text{PCI_TRDY}}$ | AD13 | I/O | NV _{DD} | 5 |
| $\overline{\text{PCI_IRDY}}$ | AC15 | I/O | NV _{DD} | 5 |
| $\overline{\text{PCI_STOP}}$ | AF13 | I/O | NV _{DD} | 5 |
| $\overline{\text{PCI_DEVSEL}}$ | AC14 | I/O | NV _{DD} | 5 |
| PCI_IDSEL | AF20 | I | NV _{DD} | — |
| $\overline{\text{PCI_SERR}}$ | AE15 | I/O | NV _{DD} | 5 |
| $\overline{\text{PCI_PERR}}$ | AD15 | I/O | NV _{DD} | 5 |
| $\overline{\text{PCI_REQ0}}$ | AB10 | I/O | NV _{DD} | — |
| $\overline{\text{PCI_REQ1/CPCI_HS_ES}}$ | AD9 | I | NV _{DD} | — |
| $\overline{\text{PCI_REQ2}}$ | AD8 | I | NV _{DD} | — |
| $\overline{\text{PCI_GNT0}}$ | AC11 | I/O | NV _{DD} | — |
| $\overline{\text{PCI_GNT1/CPCI_HS_LED}}$ | AE7 | O | NV _{DD} | — |
| $\overline{\text{PCI_GNT2/CPCI_HS_ENUM}}$ | AD7 | O | NV _{DD} | — |
| M66EN | AD21 | I | NV _{DD} | — |
| PCI_CLK0 | AF17 | O | NV _{DD} | — |
| PCI_CLK1 | AB16 | O | NV _{DD} | — |
| PCI_CLK2 | AF18 | O | NV _{DD} | — |
| $\overline{\text{PCI_PME}}$ | AD22 | I/O | NV _{DD} | 5 |
| ETSEC1/_USBULPI | | | | |
| TSEC1_COL/USBDR_TXDRXD0 | AD2 | I/O | LV _{DDB} | — |
| TSEC1_CRS/USBDR_TXDRXD1 | AC3 | I/O | LV _{DDB} | — |
| TSEC1_GTX_CLK/USBDR_TXDRXD2 | AF3 | I/O | LV _{DDB} | 3, 12 |
| TSEC1_RX_CLK/USBDR_TXDRXD3 | AE3 | I/O | LV _{DDB} | — |
| TSEC1_RX_DV/USBDR_TXDRXD4 | AD3 | I/O | LV _{DDB} | — |
| TSEC1_RXD3/USBDR_TXDRXD5 | AC6 | I/O | LV _{DDB} | — |
| TSEC1_RXD2/USBDR_TXDRXD6 | AF4 | I/O | LV _{DDB} | — |
| TSEC1_RXD1/USBDR_TXDRXD7 | AB6 | I/O | LV _{DDB} | — |
| TSEC1_RXD0/USBDR_NXT/TSEC_1588_TRIG1 | AB5 | I | LV _{DDB} | — |
| TSEC1_RX_ER/USBDR_DIR/TSEC_1588_TRIG2 | AD4 | I | LV _{DDB} | — |
| TSEC1_TX_CLK/USBDR_CLK/TSEC_1588_CLK | AF5 | I | LV _{DDB} | — |
| TSEC1_TXD3/TSEC_1588_GCLK | AE6 | O | LV _{DDB} | — |
| TSEC1_TXD2/TSEC_1588_PP1 | AC7 | O | LV _{DDB} | — |

Table 62. MPC8313E TEPBGAI Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|--|--------------------|----------|-------------------|-------|
| TSEC1_TXD1/TSEC_1588_PP2 | AD6 | O | LV _{DDB} | — |
| TSEC1_TXD0/USBDR_STP/TSEC_1588_PP3 | AD5 | O | LV _{DDB} | — |
| TSEC1_TX_EN/TSEC_1588_ALARM1 | AB7 | O | LV _{DDB} | — |
| TSEC1_TX_ER/TSEC_1588_ALARM2 | AB8 | O | LV _{DDB} | — |
| TSEC1_GTX_CLK125 | AE1 | I | LV _{DDB} | — |
| TSEC1_MDC/LB_POR_CFG_BOOT_ECC_DIS | AF6 | O | NV _{DD} | 9, 11 |
| TSEC1_MDIO | AB9 | I/O | NV _{DD} | — |
| ETSEC2 | | | | |
| TSEC2_COL/GTM1_TIN4/GTM2_TIN3/GPIO15 | AB4 | I/O | LV _{DDA} | — |
| TSEC2_CRS/GTM1_TGATE4/GTM2_TGATE3/GPIO16 | AB3 | I/O | LV _{DDA} | — |
| TSEC2_GTX_CLK/GTM1_TOUT4/GTM2_TOUT3/GPIO17 | AC1 | I/O | LV _{DDA} | 12 |
| TSEC2_RX_CLK/GTM1_TIN2/GTM2_TIN1/GPIO18 | AC2 | I/O | LV _{DDA} | — |
| TSEC2_RX_DV/GTM1_TGATE2/GTM2_TGATE1/GPIO19 | AA3 | I/O | LV _{DDA} | — |
| TSEC2_RXD3/GPIO20 | Y5 | I/O | LV _{DDA} | — |
| TSEC2_RXD2/GPIO21 | AA4 | I/O | LV _{DDA} | — |
| TSEC2_RXD1/GPIO22 | AB2 | I/O | LV _{DDA} | — |
| TSEC2_RXD0/GPIO23 | AA5 | I/O | LV _{DDA} | — |
| TSEC2_RX_ER/GTM1_TOUT2/GTM2_TOUT1/GPIO24 | AA2 | I/O | LV _{DDA} | — |
| TSEC2_TX_CLK/GPIO25 | AB1 | I/O | LV _{DDA} | — |
| TSEC2_TXD3/CFG_RESET_SOURCE0 | W3 | I/O | LV _{DDA} | — |
| TSEC2_TXD2/CFG_RESET_SOURCE1 | Y1 | I/O | LV _{DDA} | — |
| TSEC2_TXD1/CFG_RESET_SOURCE2 | W5 | I/O | LV _{DDA} | — |
| TSEC2_TXD0/CFG_RESET_SOURCE3 | Y3 | I/O | LV _{DDA} | — |
| TSEC2_TX_EN/GPIO26 | AA1 | I/O | LV _{DDA} | — |
| TSEC2_TX_ER/GPIO27 | W1 | I/O | LV _{DDA} | — |
| SGMII PHY | | | | |
| TXA | U3 | O | | — |
| $\overline{\text{TXA}}$ | V3 | O | | — |
| RXA | U1 | I | | — |
| $\overline{\text{RXA}}$ | V1 | I | | — |
| TXB | P4 | O | | — |
| $\overline{\text{TXB}}$ | N4 | O | | — |

Table 62. MPC8313E TEPBGAI Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|--|--------------------|----------|------------------|-------------------------------|
| RXB | R1 | I | | — |
| $\overline{\text{RXB}}$ | P1 | I | | — |
| SD_IMP_CAL_RX | V5 | I | | 200 Ω \pm 10% to GND |
| SD_REF_CLK | T5 | I | | — |
| SD_REF_CLK | T4 | I | | — |
| SD_PLL_TPD | T2 | O | | — |
| SD_IMP_CAL_TX | N5 | I | | 100 Ω \pm 10% to GND |
| SDAVDD | R5 | I/O | | — |
| SD_PLL_TPA_ANA | R4 | O | | — |
| SDAVSS | R3 | I/O | | — |
| USB PHY | | | | |
| USB_DP | P26 | I/O | | — |
| USB_DM | N26 | I/O | | — |
| USB_VBUS | P24 | I/O | | — |
| USB_TPA | L26 | I/O | | — |
| USB_RBIAS | M24 | I/O | | — |
| USB_PLL_PWR3 | M26 | I/O | | — |
| USB_PLL_GND | N24 | I/O | | — |
| USB_PLL_PWR1 | N25 | I/O | | — |
| USB_VSSA_BIAS | M25 | I/O | | — |
| USB_VDDA_BIAS | M22 | I/O | | — |
| USB_VSSA | N22 | I/O | | — |
| USB_VDDA | P22 | I/O | | — |
| GTM/USB | | | | |
| USBDR_DRIVE_VBUS/GTM1_TIN1/GTM2_TIN2/LSRCID0 | AD23 | I/O | NV _{DD} | — |
| USBDR_PWRFAULT/GTM1_TGATE1/GTM2_TGATE2/LSRCID1 | AE23 | I/O | NV _{DD} | — |
| USBDR_PCTL0/GTM1_TOUT1/LSRCID2 | AC22 | O | NV _{DD} | — |
| USBDR_PCTL1/LBC_PM_REF_10/LSRCID3 | AB21 | O | NV _{DD} | — |

Table 62. MPC8313E TEPBGAI Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|--|--|------------------|------|
| SPI | | | | |
| SPI MOSI/GTM1_TIN3/GTM2_TIN4/GPIO28/LSRCID4 | H1 | I/O | NV _{DD} | — |
| SPI MISO/GTM1_TGATE3/GTM2_TGATE4/GPIO29/LDVAL | H3 | I/O | NV _{DD} | — |
| SPI CLK/GTM1_TOUT3/GPIO30 | G1 | I/O | NV _{DD} | — |
| SPI SEL/GPIO31 | G3 | I/O | NV _{DD} | — |
| Power and Ground Supplies | | | | |
| AV _{DD1} | F14 | Power for e300 core APLL (1.0 V) | — | — |
| AV _{DD2} | P21 | Power for system APLL (1.0 V) | — | — |
| GV _{DD} | A2,A3,A4,A24,A25,B3,B4,B5,B12,B13,B20,B21,B24,B25,B26,D1,D2,D8,D9,D16,D17 | Power for DDR1 and DDR2 DRAM I/O voltage (1.8/2.5 V) | — | — |
| LV _{DD} | D24,D25,G23,H23,R23,T23,W25,Y25,AA22,AC23 | Power for local bus (3.3 V) | — | — |
| LV _{DDA} | W2,Y2 | Power for eTSEC2 (2.5 V, 3.3 V) | — | — |
| LV _{DDB} | AC8,AC9,AE4,AE5 | Power for eTSEC1/USB DR (2.5 V, 3.3 V) | — | — |
| MV _{REF} | C14,D14 | Reference voltage signal for DDR | — | — |
| NV _{DD} | G4,H4,L2,M2,AC16,AC17,AD25,AD26,AE12,AE13,AE20,AE21,AE24,AE25,AE26,AF24,AF25 | Standard I/O voltage (3.3 V) | — | — |
| V _{DD} | K11,K12,K13,K14,K15,K16,L10,L17,M10,M17,N10,N17,U12,U13, | Power for core (1.0 V) | — | — |
| V _{DDC} | F6,F10,F19,K6,K10,K17,K21,P6,P10,P17,R10,R17,T10,T17,U10,U11,U14,U15,U16,U17,W6,W21,AA6,AA10,AA14,AA19 | Internal core logic constant power (1.0 V) | — | — |

Table 62. MPC8313E TEPBGAI Pinout Listing (continued)

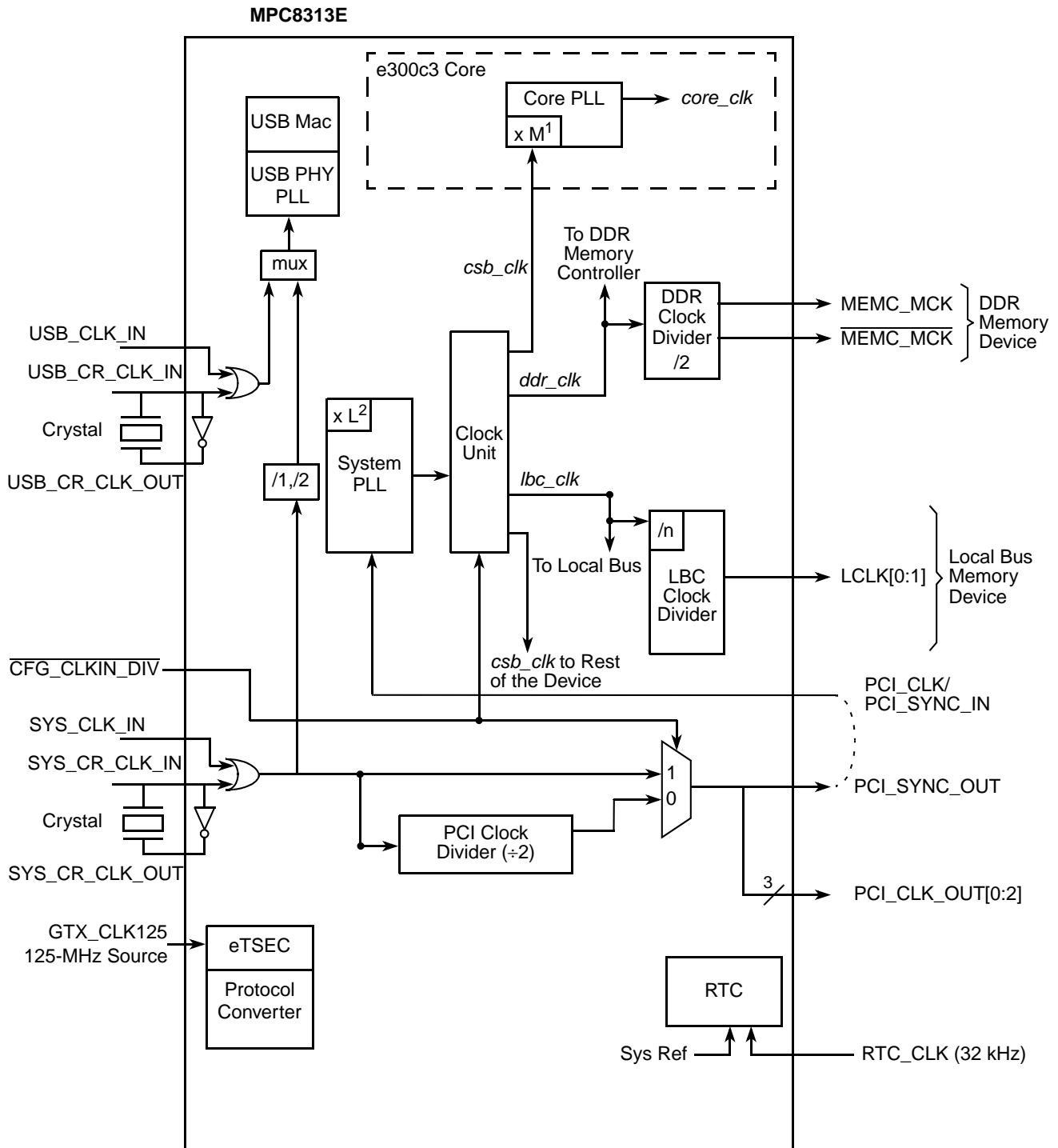
| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|----------------------|--|--|--------------|------|
| V _{SS} | B1,B2,B8,B9,B16,B17,C1,C2,C3,C4,C5,C24,C25,C26,D3,D4,D12,D13,D20,D21,F8,F11,F13,F16,F17,F21,G2,G25,H2,H6,H21,H25,L4,L6,L11,L12,L13,L14,L15,L16,L21,L23,M4,M11,M12,M13,M14,M15,M16,M23,N6,N11,N12,N13,N14,N15,N16,N21,N23,P11,P12,P13,P14,P15,P16,P23,P25,R11,R12,R13,R14,R15,R16,R25,T6,T11,T12,T13,T14,T15,T16,T21,T25,U5,U6,U21,W4,W23,Y4,Y23,AA8,AA11,AA13,AA16,AA17,AA21,AC4,AC5,AC12,AC13,AC20,AC21,AD1,AE2,AE8,AE9,AE16,AE17,AF2 | — | — | — |
| XCOREV _{DD} | T1,U2,V2 | Core power for SerDes transceivers (1.0 V) | — | — |
| XCOREV _{SS} | P2,R2,T3 | — | — | — |
| XPADV _{DD} | P5,U4 | Pad power for SerDes transceivers (1.0 V) | — | — |
| XPADV _{SS} | P3,V4 | — | — | — |

Notes:

1. This pin is an open drain signal. A weak pull-up resistor (1 k Ω) should be placed on this pin to NV_{DD}.
2. This pin is an open drain signal. A weak pull-up resistor (2–10 k Ω) should be placed on this pin to NV_{DD}.
3. This output is actively driven during reset rather than being three-stated during reset.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI specifications recommendation.
6. This pin must always be tied to V_{SS}.
7. Internal thermally sensitive resistor, resistor value varies linearly with temperature. Useful for determining the junction temperature.
8. 1588 signals are available on these pins only in MPC8313 Rev 2.x or later.
9. LB_POR_CFG_BOOT_ECC_DIS is available only in MPC8313 Rev 2.x or later.
10. This pin has an internal pull-up.
11. This pin has an internal pull-down.
12. In MII mode, GTX_CLK should be pulled down by 300 Ω to V_{SS}.

20 Clocking

This figure shows the internal distribution of clocks within the MPC8313E.



¹ Multiplication factor $M = 1, 1.5, 2, 2.5,$ and 3 . Value is decided by RCWLR[COREPLL].

² Multiplication factor $L = 2, 3, 4, 5,$ and 6 . Value is decided by RCWLR[SPMF].

Figure 57. MPC8313E Clock Subsystem

The primary clock source for the MPC8313E can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. When the device is configured as a PCI host device, SYS_CLK_IN is its primary input clock. SYS_CLK_IN feeds the PCI clock divider ($\div 2$) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration input selects whether SYS_CLK_IN or SYS_CLK_IN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCICOEn] parameters select whether the PCI_SYNC_OUT is driven out on the PCI_CLK_OUT_n signals.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the device to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input clock. When the device is configured as a PCI agent device the SYS_CLK_IN signal should be tied to VSS.

As shown in [Figure 57](#), the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (*csb_clk*), the internal clock for the DDR controller (*ddr_clk*), and the internal clock for the local bus interface unit (*lbc_clk*).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb_clk = \{PCI_SYNC_IN \times (1 + \overline{\sim CFG_CLKIN_DIV})\} \times SPMF$$

In PCI host mode, $PCI_SYNC_IN \times (1 + \overline{\sim CFG_CLKIN_DIV})$ is the SYS_CLK_IN frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies up the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See Chapter 4, “Reset, Clocking, and Initialization,” in the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual*, for more information on the clock subsystem.

The internal *ddr_clk* frequency is determined by the following equation:

$$ddr_clk = csb_clk \times (1 + RCWL[DDRCM])$$

Note that *ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider ($\div 2$) to create the differential DDR memory bus clock outputs (MCK and \overline{MCK}). However, the data rate is the same frequency as *ddr_clk*.

The internal *lbc_clk* frequency is determined by the following equation:

$$lbc_clk = csb_clk \times (1 + RCWL[LBCM])$$

Note that *lbc_clk* is not the external local bus frequency; *lbc_clk* passes through the a LBC clock divider to create the external local bus clock outputs (LCLK[0:1]). The LBC clock divider ratio is controlled by LCRR[CLKDIV].

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. [Table 63](#) specifies which units have a configurable clock frequency.

Table 63. Configurable Clock Units

| Unit | Default Frequency | Options |
|---|-------------------|---|
| TSEC1 | <i>csb_clk</i> | Off, <i>csb_clk</i> , <i>csb_clk/2</i> , <i>csb_clk/3</i> |
| TSEC2 | <i>csb_clk</i> | Off, <i>csb_clk</i> , <i>csb_clk/2</i> , <i>csb_clk/3</i> |
| Security Core, I ² C, SAP, TPR | <i>csb_clk</i> | Off, <i>csb_clk</i> , <i>csb_clk/2</i> , <i>csb_clk/3</i> |
| USB DR | <i>csb_clk</i> | Off, <i>csb_clk</i> , <i>csb_clk/2</i> , <i>csb_clk/3</i> |
| PCI and DMA complex | <i>csb_clk</i> | Off, <i>csb_clk</i> |

This table provides the operating frequencies for the MPC8313E TEPBGAI under recommended operating conditions (see [Table 2](#)).

Table 64. Operating Frequencies for TEPBGAI

| Characteristic ¹ | Maximum Operating Frequency | Unit |
|--|-----------------------------|------|
| e300 core frequency (<i>core_clk</i>) | 333 | MHz |
| Coherent system bus frequency (<i>csb_clk</i>) | 167 | MHz |
| DDR1/2 memory bus frequency (MCK) ² | 167 | MHz |
| Local bus frequency (LCLKn) ³ | 66 | MHz |
| PCI input frequency (SYS_CLK_IN or PCI_CLK) | 66 | MHz |

Note:

1. The SYS_CLK_IN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCK, LCLK[0:1], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies. The value of SCCR[ENCCM] and SCCR[USBDRCM] must be programmed such that the maximum internal operating frequency of the security core and USB modules do not exceed their respective value listed in this table.
2. The DDR data rate is 2x the DDR memory bus frequency.
3. The local bus frequency is 1/2, 1/4, or 1/8 of the *lbc_clk* frequency (depending on LCRR[CLKDIV]), which is in turn, 1x or 2x the *csb_clk* frequency (depending on RCWL[LBCM]).

20.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. This table shows the multiplication factor encodings for the system PLL.

Table 65. System PLL Multiplication Factors

| RCWL[SPMF] | System PLL Multiplication Factor |
|------------|----------------------------------|
| 0000 | Reserved |
| 0001 | Reserved |
| 0010 | × 2 |
| 0011 | × 3 |

Table 65. System PLL Multiplication Factors (continued)

| RCWL[SPMF] | System PLL Multiplication Factor |
|------------|----------------------------------|
| 0100 | × 4 |
| 0101 | × 5 |
| 0110 | × 6 |
| 0111–1111 | Reserved |

Note:

1. If RCWL[DDRCM] and RCWL[LBCM] are both cleared, the system PLL VCO frequency = (CSB frequency) × (System PLL VCO Divider).
2. If either RCWL[DDRCM] or RCWL[LBCM] are set, the system PLL VCO frequency = 2 × (CSB frequency) × (System PLL VCO Divider).
3. The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 450–750 MHz

As described in [Section 20, “Clocking,”](#) the LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (SYS_CLK_IN or PCI_SYNC_IN) and the internal coherent system bus clock (*csb_clk*). This table shows the expected frequency values for the CSB frequency for select *csb_clk* to SYS_CLK_IN/PCI_SYNC_IN ratios.

Table 66. CSB Frequency Options

| CFG_CLKIN_DIV at Reset ¹ | SPMF | <i>csb_clk</i> :Input Clock Ratio ² | Input Clock Frequency (MHz) ² | | | |
|-------------------------------------|------|--|--|-----|-------|-------|
| | | | 24 | 25 | 33.33 | 66.67 |
| | | | <i>csb_clk</i> Frequency (MHz) | | | |
| High | 0010 | 2:1 | | | | 133 |
| High | 0011 | 3:1 | | | | 100 |
| High | 0100 | 4:1 | | | 100 | 133 |
| High | 0101 | 5:1 | 120 | 125 | 167 | |
| High | 0110 | 6:1 | 144 | 150 | | |
| Low | 0010 | 2:1 | | | | 133 |
| Low | 0011 | 3:1 | | | | 100 |
| Low | 0100 | 4:11 | | | 100 | 133 |
| Low | 0101 | 5:1 | 120 | 125 | 167 | |
| Low | 0110 | 6:1 | 144 | 150 | | |

¹ CFG_CLKIN_DIV select the ratio between SYS_CLK_IN and PCI_SYNC_OUT.

² SYS_CLK_IN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

20.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). This table shows the encodings for RCWL[COREPLL]. COREPLL values that are not listed in this table should be considered as reserved.

NOTE

Core VCO frequency = core frequency × VCO divider. The VCO divider, which is determined by RCWLR[COREPLL], must be set properly so that the core VCO frequency is in the range of 400–800 MHz.

Table 67. e300 Core PLL Configuration

| RCWL[COREPLL] | | | <i>core_clk</i> : <i>csb_clk</i> Ratio ¹ | VCO Divider (VCOD) ³ |
|---------------|-------------|---|--|--|
| 0–1 | 2–5 | 6 | | |
| <i>nn</i> | 0000 | 0 | PLL bypassed (PLL off, <i>csb_clk</i> clocks core directly) | PLL bypassed (PLL off, <i>csb_clk</i> clocks core directly) |
| 11 | <i>nnnn</i> | n | n/a | n/a |
| 00 | 0001 | 0 | 1:1 | 2 |
| 01 | 0001 | 0 | 1:1 | 4 |
| 10 | 0001 | 0 | 1:1 | 8 |
| 00 | 0001 | 1 | 1.5:1 | 2 |
| 01 | 0001 | 1 | 1.5:1 | 4 |
| 10 | 0001 | 1 | 1.5:1 | 8 |
| 00 | 0010 | 0 | 2:1 | 2 |
| 01 | 0010 | 0 | 2:1 | 4 |
| 10 | 0010 | 0 | 2:1 | 8 |
| 00 | 0010 | 1 | 2.5:1 | 2 |
| 01 | 0010 | 1 | 2.5:1 | 4 |
| 10 | 0010 | 1 | 2.5:1 | 8 |
| 00 | 0011 | 0 | 3:1 | 2 |
| 01 | 0011 | 0 | 3:1 | 4 |
| 10 | 0011 | 0 | 3:1 | 8 |

Note:

1. For *core_clk:csb_clk* ratios of 2.5:1 and 3:1, the *core_clk* must not exceed its maximum operating frequency of 333 MHz.
2. Core VCO frequency = core frequency × VCO divider. Note that VCO divider has to be set properly so that the core VCO frequency is in the range of 400–800 MHz.

20.3 Example Clock Frequency Combinations

This table shows several possible frequency combinations that can be selected based on the indicated input reference frequencies, with RCWLR[LBCM] = 0 and RCWLR[DDRCM] = 1, such that the LBC operates with a frequency equal to the frequency of *csb_clk* and the DDR controller operates at twice the frequency of *csb_clk*.

Table 68. System Clock Frequencies

| SYS_CLK_IN/ PCI_CLK | SPMF ¹ | VCOD ² | VCO ³ | CSB (<i>csb_clk</i>) ⁴ | DDR (<i>ddr_clk</i>) | LBC(<i>lbc_clk</i>) | | | | e300 Core(<i>core_clk</i>) | | | | |
|------------------------|-------------------|-------------------|------------------|--|---------------------------|-----------------------|-------|------|-------------------------|------------------------------|-------|-----|-------|-----|
| | | | | | | /2 | /4 | /8 | USB ref ⁵ | × 1 | × 1.5 | × 2 | × 2.5 | × 3 |
| 25.0 | 6 | 2 | 600.0 | 150.0 | 300.0 | — | 37.5 | 18.8 | Note ⁶ | 150.0 | 225 | 300 | 375 | — |
| 25.0 | 5 | 2 | 500.0 | 125.0 | 250.0 | 62.5 | 31.25 | 15.6 | Note 6 | 125.0 | 188 | 250 | 313 | 375 |
| 33.3 | 5 | 2 | 666.0 | 166.5 | 333.0 | — | 41.63 | 20.8 | Note 6 | 166.5 | 250 | 333 | — | — |
| 33.3 | 4 | 2 | 532.8 | 133.2 | 266.4 | 66.6 | 33.3 | 16.7 | Note 6 | 133.2 | 200 | 266 | 333 | 400 |
| 48.0 | 3 | 2 | 576.0 | 144.0 | 288.0 | — | 36 | 18.0 | 48.0 | 144.0 | 216 | 288 | 360 | — |
| 66.7 | 2 | 2 | 533.4 | 133.3 | 266.7 | 66.7 | 33.34 | 16.7 | Note 6 | 133.3 | 200 | 267 | 333 | 400 |

Note:

1. System PLL multiplication factor.
2. System PLL VCO divider.
3. When considering operating frequencies, the valid core VCO operating range of 400–800 MHz must not be violated.
4. Due to erratum eTSEC40, *csb_clk* frequencies of less than 133 MHz do not support gigabit Ethernet data rates. The core frequency must be 333 MHz for gigabit Ethernet operation. This erratum will be fixed in revision 2 silicon.
5. Frequency of USB PLL input reference.
6. USB reference clock must be supplied from a separate source as it must be 24 or 48 MHz, the USB reference must be supplied from a separate external source using USB_CLK_IN.

21 Thermal

This section describes the thermal specifications of the MPC8313E.

21.1 Thermal Characteristics

This table provides the package thermal characteristics for the 516, 27 × 27 mm TEPBGAIL.

Table 69. Package Thermal Characteristics for TEPBGAIL

| Characteristic | Board Type | Symbol | TEPBGA II | Unit | Note |
|--|-------------------------|-------------------|-----------|------|---------|
| Junction-to-ambient natural convection | Single layer board (1s) | R _{θJA} | 25 | °C/W | 1, 2 |
| Junction-to-ambient natural convection | Four layer board (2s2p) | R _{θJA} | 18 | °C/W | 1, 2, 3 |
| Junction-to-ambient (@200 ft/min) | Single layer board (1s) | R _{θJMA} | 20 | °C/W | 1, 3 |
| Junction-to-ambient (@200 ft/min) | Four layer board (2s2p) | R _{θJMA} | 15 | °C/W | 1, 3 |
| Junction-to-board | — | R _{θJB} | 10 | °C/W | 4 |

Table 69. Package Thermal Characteristics for TEPBGAll (continued)

| Characteristic | Board Type | Symbol | TEPBGA II | Unit | Note |
|-------------------------|--------------------|-----------------|-----------|------|------|
| Junction-to-case | — | $R_{\theta JC}$ | 8 | °C/W | 5 |
| Junction-to-package top | Natural convection | Ψ_{JT} | 7 | °C/W | 6 |

Note:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

21.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

21.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J , can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

21.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter

(edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (°C)

T_B = board temperature at the package perimeter (°C)

$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

21.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

21.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to- ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the airflow around the device, the interface material, the mounting arrangement on the printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, airflow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Table 70. Thermal Resistance for TEPBGAll with Heat Sink in Open Flow

| Heat Sink Assuming Thermal Grease | Airflow | Thermal Resistance (°C/W) |
|------------------------------------|--------------------|---------------------------|
| Wakefield 53 × 53 × 2.5 mm pin fin | Natural convection | 13.0 |
| | 0.5 m/s | 10.6 |
| | 1 m/s | 9.7 |
| | 2 m/s | 9.2 |
| | 4 m/s | 8.9 |
| Aavid 35 × 31 × 23 mm pin fin | Natural convection | 14.4 |
| | 0.5 m/s | 11.3 |
| | 1 m/s | 10.5 |
| | 2 m/s | 9.9 |
| | 4 m/s | 9.4 |
| Aavid 30 × 30 × 9.4 mm pin fin | Natural convection | 16.5 |
| | 0.5 m/s | 13.5 |
| | 1 m/s | 12.1 |
| | 2 m/s | 10.9 |
| | 4 m/s | 10.0 |
| Aavid 43 × 41 × 16.5 mm pin fin | Natural convection | 14.5 |
| | 0.5 m/s | 11.7 |
| | 1 m/s | 10.5 |
| | 2 m/s | 9.7 |
| | 4 m/s | 9.2 |

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in [Table 70](#). More detailed thermal models can be made available on request.

Heat sink Vendors include the following list:

| | |
|--|--------------|
| Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com | 603-224-9988 |
| Alpha Novatech 473 Sapena Ct. #12 Santa Clara, CA 95054 Internet: www.alphanovatech.com | 408-749-7601 |
| International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com | 818-842-7277 |
| Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-thermal.com | 408-436-8770 |
| Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105 Internet: www.chipcoolers.com | 800-522-6752 |
| Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com | 603-635-2800 |

Interface material vendors include the following:

| | |
|---|--------------|
| Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com | 781-935-4850 |
| Dow-Corning Corporation Corporate Center PO BOX 994 Midland, MI 48686-0994 Internet: www.dowcorning.com | 800-248-2481 |
| Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com | 888-642-7674 |
| The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com | 800-347-4572 |

21.3 Heat Sink Attachment

When attaching heat sinks to these devices, an interface material is required. The best method is to use thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces which would lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. Recommended maximum force on the top of the package is 10 lb (4.5 kg) force. If an adhesive attachment is planned, the adhesive should be intended for attachment to painted or plastic surfaces and its performance verified under the application requirements.

21.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction to case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

- T_J = junction temperature (°C)
- T_C = case temperature of the package
- $R_{\theta JC}$ = junction-to-case thermal resistance
- P_D = power dissipation

22 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8313E SYS_CLK_IN

22.1 System Clocking

The MPC8313E includes three PLLs.

1. The platform PLL (AV_{DD2}) generates the platform clock from the externally supplied SYS_CLK_IN input in PCI host mode or SYS_CLK_IN/PCI_SYNC_IN in PCI agent mode. The frequency ratio between the platform and SYS_CLK_IN is selected using the platform PLL ratio configuration bits as described in [Section 20.1, “System PLL Configuration.”](#)
2. The e300 core PLL (AV_{DD1}) generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in [Section 20.2, “Core PLL Configuration.”](#)
3. There is a PLL for the SerDes block.

22.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD1} , AV_{DD2} , and $SDAV_{DD}$, respectively). The AV_{DD} level should always be equivalent to V_{DD} , and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits as illustrated in [Figure 58](#), one to each of the five AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

This figure shows the PLL power supply filter circuits.

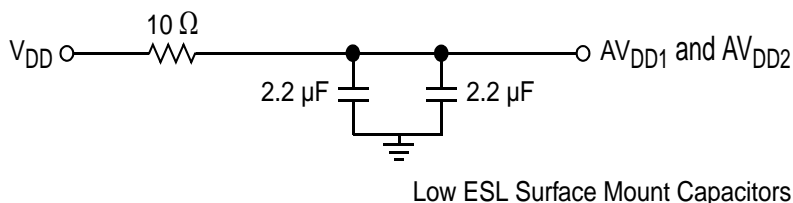
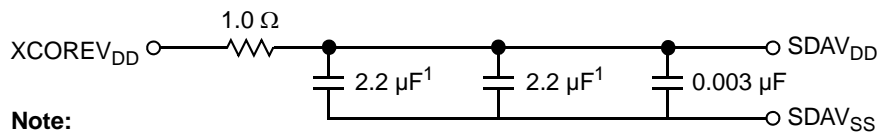


Figure 58. PLL Power Supply Filter Circuit

The $SDAV_{DD}$ signal provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit like the one shown in [Figure 59](#). For maximum effectiveness, the filter circuit should be placed as closely as possible to the $SDAV_{DD}$ ball to ensure it filters out as much noise as possible. The ground connection should be near the $SDAV_{DD}$ ball. The 0.003- μ F capacitor is closest to the ball, followed by the two 2.2- μ F capacitors, and finally the 1- Ω resistor to the board supply plane. The capacitors are connected from traces from $SDAV_{DD}$ to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide, and direct.



Note:

1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 59. SerDes PLL Power Supply Filter Circuit

Note the following:

- $SDAV_{DD}$ should be a filtered version of $XCOREV_{DD}$.



- Output signals on the SerDes interface are fed from the $XPADV_{DD}$ power plane. Input signals and sensitive transceiver analog circuits are on the $XCOREV_{DD}$ supply.
- Power: $XPADV_{DD}$ consumes less than 300 mW; $XCOREV_{DD} + SDAV_{DD}$ consumes less than 750 mW.

22.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8313E system, and the MPC8313E itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} , NV_{DD} , GV_{DD} , LV_{DD} , LV_{DDA} , and LV_{DDB} pin of the device. These decoupling capacitors should receive their power from separate V_{DD} , NV_{DD} , GV_{DD} , LV_{DD} , LV_{DDA} , LV_{DDB} , and VSS power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 μF . Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} , NV_{DD} , GV_{DD} , LV_{DD} , LV_{DDA} , and LV_{DDB} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100 to 330 μF (AVX TPS tantalum or Sanyo OSCON). However, customers should work directly with their power regulator vendor for best values and types of bulk capacitors.

22.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power ($XCOREV_{DD}$ and $XPADV_{DD}$) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only SMT capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least $10 \times 10\text{-nF}$ SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a 1- μF ceramic chip capacitor from each SerDes supply ($XCOREV_{DD}$ and $XPADV_{DD}$) to the board ground plane on each side of the device. This should be done for all SerDes supplies.

- Third, between the device and any SerDes voltage regulator there should be a 10- μ F, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100- μ F, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

22.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to NV_{DD} , GV_{DD} , LV_{DD} , LV_{DDA} , or LV_{DDB} as required. Unused active high inputs should be connected to V_{SS} . All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD} , NV_{DD} , GV_{DD} , LV_{DD} , LV_{DDA} , LV_{DDB} , and V_{SS} pins of the device.

22.6 Output Buffer DC Impedance

The MPC8313E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I²C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to NV_{DD} or V_{SS} . Then, the value of each resistor is varied until the pad voltage is $NV_{DD}/2$ (see Figure 60). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $NV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

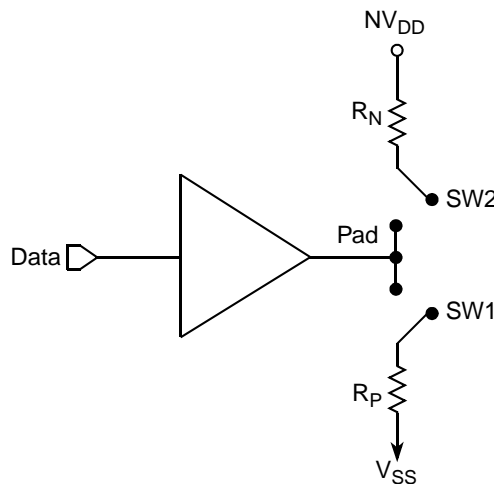


Figure 60. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term} . The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

This table summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD} , nominal NV_{DD} , 105°C.

Table 71. Impedance Characteristics

| Impedance | Local Bus, Ethernet, DUART, Control, Configuration, Power Management | PCI Signals (Not Including PCI Output Clocks) | PCI Output Clocks (Including PCI_SYNC_OUT) | DDR DRAM | Symbol | Unit |
|--------------|--|---|--|-----------|------------|----------|
| R_N | 42 Target | 25 Target | 42 Target | 20 Target | Z_0 | Ω |
| R_P | 42 Target | 25 Target | 42 Target | 20 Target | Z_0 | Ω |
| Differential | NA | NA | NA | NA | Z_{DIFF} | Ω |

Note: Nominal supply voltages. See Table 1, $T_J = 105^\circ\text{C}$.

22.7 Configuration Pin Muxing

The MPC8313E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 k Ω on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{PORESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

22.8 Pull-Up Resistor Requirements

The MPC8313E requires high resistance pull-up resistors (10 k Ω is recommended) on open drain type pins including I²C, and IPIC (integrated programmable interrupt controller).

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 61. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions because most have asynchronous behavior and spurious assertion, which give unpredictable results.

Refer to the *PCI 2.2 Specification*, for all pull-ups required for PCI.

22.9 JTAG Configuration Signals

Boundary scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in IEEE 1149.1, but is provided on any Freescale devices that are built on Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, systems generally assert $\overline{\text{TRST}}$ during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{PORESET}}$ is not practical.

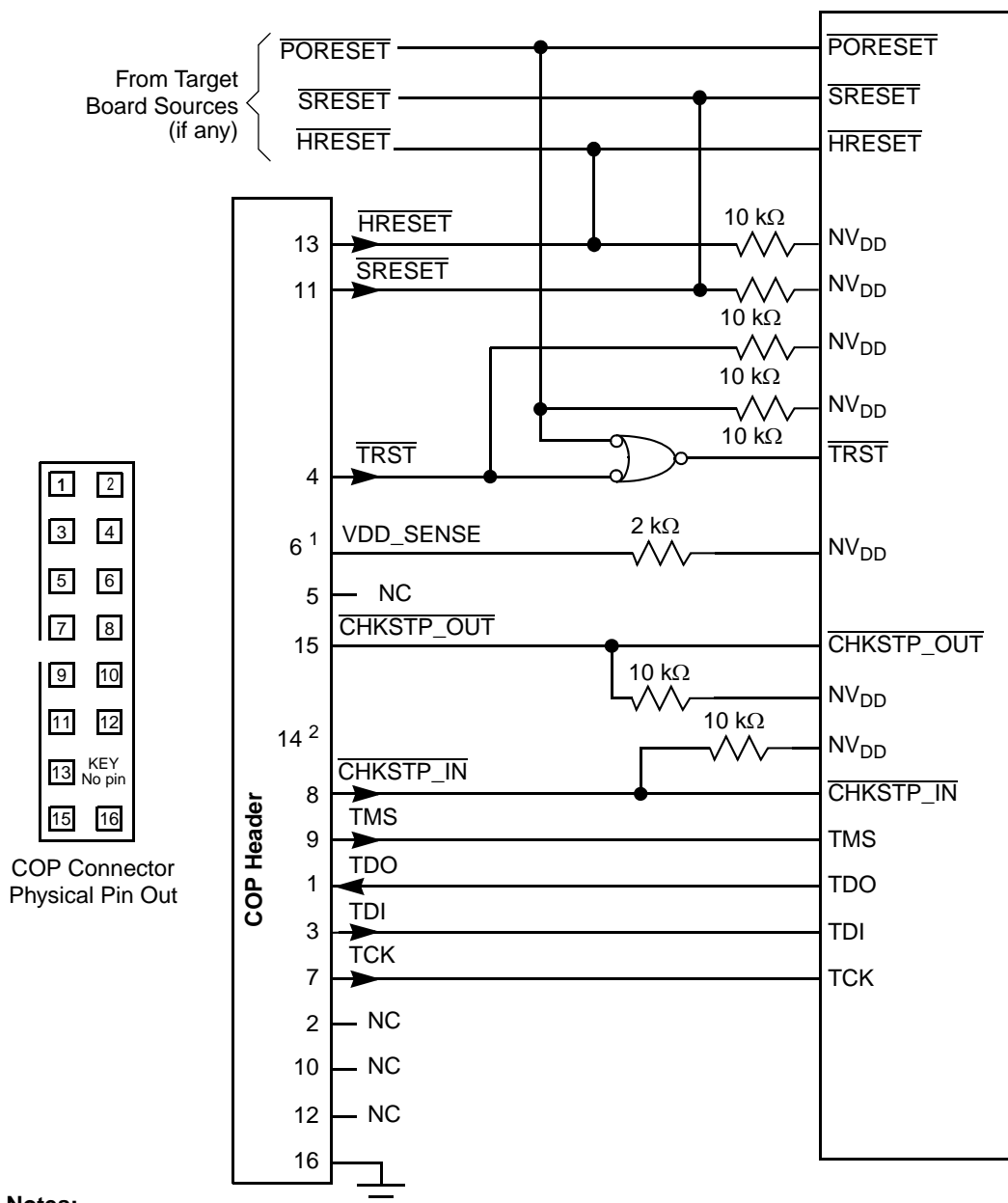
The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{TRST}}$ without causing $\overline{\text{PORESET}}$. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in [Figure 61](#) allows the COP to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header are not used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{PORESET}}$ so that it is asserted when the system reset signal ($\overline{\text{PORESET}}$) is asserted.

The COP header shown in [Figure 61](#) adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header).

There is no standardized way to number the COP header shown in [Figure 61](#); consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in [Figure 61](#) is common to all known emulators.



- Notes:**
1. Some systems require power to be fed from the application board into the debugger repeater card via the COP header. In this case the resistor value for VDD_SENSE should be around 20 Ω.
 2. Key location; pin 14 is not physically present on the COP header.

Figure 61. JTAG Interface Connection

23 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in [Section 23.1, “Part Numbers Fully Addressed by this Document.”](#)

23.1 Part Numbers Fully Addressed by this Document

This table provides the Freescale part numbering nomenclature for the MPC8313E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 72. Part Numbering Nomenclature

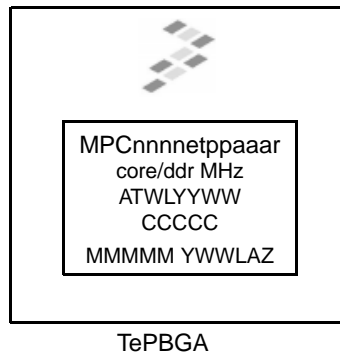
| MPC | <i>nnnn</i> | <i>e</i> | <i>t</i> | <i>pp</i> | <i>aa</i> | <i>a</i> | <i>x</i> |
|--------------|-----------------|--------------------------------------|--|---|--|----------------------------|--|
| Product Code | Part Identifier | Encryption Acceleration | Temperature Range ³ | Package ^{1, 4} | e300 core Frequency ² | DDR Frequency | Revision Level |
| MPC | 8313 | Blank = Not included E = included | Blank = 0° to 105°C C = -40° to 105°C | ZQ = PB TEPBGAII VR = PB free TEPBGAII | AD = 266 MHz AF = 333 MHz AG = 400 MHz | D = 266 MHz F = 333 MHz | Blank = 1.0 A = 2.0 B = 2.1 C = 2.2 |

Note:

1. See [Section 19, "Package and Pin Listings,"](#) for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.
3. Contact local Freescale office on availability of parts with °C temperature range.
4. ZQ package was available for Rev 1.0. For Rev 2.x, only VR package is available.

23.2 Part Marking

Parts are marked as shown in this figure.



Notes:

- MPCnnnnnetppaar is the orderable part number.
- ATWLYYWW is the standard assembly, test, year, and work week codes.
- CCCCC is the country code.
- MMMMM is the mask number.

Figure 62. Part Marking for TEPBGAII Device

24 Revision History

This table summarizes a revision history for this document.

Table 73. Document Revision History

| Rev. Number | Date | Substantive Change(s) |
|-------------|---------|--|
| 4 | 11/2011 | <ul style="list-style-type: none"> • In Table 2, added following notes: <ul style="list-style-type: none"> – Note 3: Min temperature is specified with T_A; Max temperature is specified with T_J – Note 4: All Power rails must be connected and power applied to the MPC8313 even if the IP interfaces are not used. – Note 5: All I/O pins should be interfaced with peripherals operating at same voltage level. – Note 6: This voltage is the input to the filter discussed in Section 22.2, “PLL Power Supply Filtering.” and not necessarily the voltage at the AVDD pin, which may be reduced from VDD by the filter • Decoupled PCI_CLK and SYS_CLK_IN rise and fall times in Table 8. Relaxed maximum rise/fall time of SYS_CLK_IN to 4ns. • Added a note in Table 27 stating “The frequency of RX_CLK should not exceed the TX_CLK by more than 300 ppm.” • In Table 30: <ul style="list-style-type: none"> – Changed max value of t_{skrgt} in “Data to clock input skew (at receiver)” row from 2.8 to 2.6. – Added Note 7, stating that, “The frequency of RX_CLK should not exceed the GTX_CLK125 by more than 300 ppm.” • Added a note stating “eTSEC should be interfaced with peripheral operating at same voltage level” in Section 8.1.1, “TSEC DC Electrical Characteristics.” • TSEC1_MDC and TSEC_MDIO are powered at 3.3V by NVDD. Replaced LVDDA/LVDDDB with NVDD and removed instances of 2.5V at several places in Section 8.5, “Ethernet Management Interface Electrical Characteristics.” • In Table 43, changed min/max values of t_{CLK_TOL} from 0.05 to 0.005. • In Table 62: <ul style="list-style-type: none"> – Added Note 2 for LGPL4 in showing LGPL4 as open-drain. – Removed Note 2 from TSEC1_MDIO. – Added Note 10: This pin has an internal pull-up. – Added Note 11: This pin has an internal pull-down. – Added Note 12: “In MII mode, GTX_CLK should be pulled down by $300\ \Omega$ to V_{SS}” to TSEC1_GTX_CLK and TSEC2_GTX_CLK. • In Section 19.1, “Package Parameters for the MPC8313E TEPBGAII,” replaced “5.5 Sn/0.5 Cu/4 Ag” with “Sn/3.5 Ag.” • Added foot note 3 in Table 65 stating “The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 450–750 MHz.” • In Table 72: <ul style="list-style-type: none"> – Added AD = 266 and D = 266. – Added “C = 2.2” in “Revision level” column. – Added Note 4. • Changed resistor from $1.0\ \Omega$ to $10\ \Omega$ in Figure 58. • Replaced LCCR with LCRR throughout. • Added high-speed to USB Phy description. |
| 3 | 01/2009 | <ul style="list-style-type: none"> • Table 72, in column aa, changed to AG = 400 MHz. |
| 2.2 | 12/2008 | <ul style="list-style-type: none"> • Made cross-references active for sections, figures, and tables. |
| 2.1 | 12/2008 | <ul style="list-style-type: none"> • Added Figure 2, after Table 2 and renumbered the following figures. |

Table 73. Document Revision History (continued)

| Rev. Number | Date | Substantive Change(s) |
|-------------|---------|--|
| 2 | 10/2008 | <ul style="list-style-type: none"> • Added Note “The information in this document is accurate for revision 1.0, and 2.x and later. See Section 24.1, “Part Numbers Fully Addressed by this Document,” before Section 1, “Overview.” • Added part numbering details for all the silicon revisions in Table 74. • Changed V_{IH} from 2.7 V to 2.4 V in Table 7. • Added a row for V_{IH} level for Rev 2.x or later in Table 45. • Added a column for maximum power dissipation in low power mode for Rev 2.x or later silicon in Table 6. • Added a column for Power Nos for Rev 2.x or later silicon and added a row for 400 MHz in Table 4. • Removed footnote, “These are preliminary estimates.” from Table 4. • Added Table 21 for DDR AC Specs on Rev 2.x or later silicon. • Added Section 9, “High-Speed Serial Interfaces (HSSI).” • Added \overline{LFW}, \overline{LFCLE}, \overline{LFALE}, \overline{LOE}, \overline{LFRE}, \overline{LFWP}, \overline{LGTA}, $\overline{LUPWAIT}$, and \overline{LFRB} in Table 63. • In Table 39, added note 2: “This parameter is dependent on the <code>csb_clk</code> speed. (The <code>MIIMCFG[Mgmt Clock Select]</code> field determines the clock frequency of the Mgmt Clock <code>EC_MDC</code>.)” • Removed mentions of SGMII (SGMII has separate specs) from Section 8.1, “Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics.” • Corrected Section 8.1, “Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics,” to state that RGMII/RTBI interfaces only operate at 2.5 V, not 3.3 V. • Added ZQ package to ordering information In Table 74 and Section 19.1, “Package Parameters for the MPC8313E TEPBGAI1” (applicable to both silicon rev. 1.0 and 2.1) • Removed footnotes 5 and 6 from Table 1 (left over when the PCI undershoot/overshoot voltages and maximum AC waveforms were removed from Section 2.1.2, “Power Supply Voltage Specification”). • Removed <code>SD_PLL_TPD</code> (T2) and <code>SD_PLL_TPA_ANA</code> (R4) from Table 63. • Added Section 8.3, “SGMII Interface Electrical Characteristics.” Removed Section 8.5.3 SGMII DC Electrical Characteristics. • Removed “HRESET negation to SRESET negation (output)” spec and changed “HRESET/SRESET assertion (output)” spec to “HRESET assertion (output)” in Table 10. • Clarified POR configuration signal specs to “Time for the device to turn off POR configuration signal drivers with respect to the assertion of HRESET” and “Time for the device to turn on POR configuration signal drivers with respect to the negation of HRESET” in Table 10. • Added Section 24.2, “Part Marking,” and Figure 62. |

Table 73. Document Revision History (continued)

| Rev. Number | Date | Substantive Change(s) |
|-------------|--------|---|
| 1 | 3/2008 | <ul style="list-style-type: none"> • Replaced OVDD with NV_{DD} everywhere • Added XCOREVDD and XPADVDD to Table 1 • Moved VDD and VDDC to the top of the table before SerDes supplies in Table 2 • In Table 2 split DDR row into two from total current requirement of 425 mA. One for DDR1 (131 mA) and other for DDR2 (140 mA). • In Table 2 corrected current requirement numbers for NV_{DD} from 27 mA to 74 mA, LV_{DD} from 60 mA to 16 mA, LV_{DDA} from 85 mA to 22 mA and LV_{ddb} from 85 mA to 44 mA. • In Table 2 corrected Vdd and Vddc current requirements from 560 mA and 454 mA to 469 and 377 mA, respectively. Corrected Avdd1 and Avdd2 current requirements from 10 mA to 2–3 mA, and XCOREVDD from 100 mA to 170 mA. • In Table 2, added row stating junction temperature range of 0 to 105°C. Added footnote 2 stating GPIO pins may operate from 2.5-V supply as well when configured for different functionality. • In Section 2.1.2, “Power Supply Voltage Specification,” added a note describing the purpose of Table 2. • In Section 3, “Power Characteristics,” added a note describing the purpose of Table 5. • Rewrote Section 2.2, “Power Sequencing,” and added Figure 3. • In Table 4, added “but do include core, USB PLL, and a portion of SerDes digital power...” to Note 1. • In Table 4 corrected “Typical power” to “Maximum power” in note 2 and added a note for Typical Power. • In Table 4 removed 266-MHz row as 266-MHz core parts are not offered. • In Table 5, moved Local bus typical power dissipation under LVdd. • Added Table 6 to show the low power mode power dissipation for D3warm mode. • In Table 8 corrected SYS_CLK_IN frequency range from 25–66 MHz to 24–66.67 MHz. • Added Section 8.4, “eTSEC IEEE 1588 AC Specifications” • In Table 42 changed minimum value of USB input hold t_{USIXKH} from 0 to 1ns • Added Table 43 and Table 44 showing USB clock in specifications • In Table 46, added rows for t_{LALEHOV}, t_{LALETOT1}, t_{LALETOT2}, and t_{LALETOT3} parameters. Added Figure 40. • In Table 50, removed row for rise time (t_{I2CR}). Removed minimum value of t_{I2CF}. Added note 5 stating that the device does not follow the I2C-BUS Specifications version 2.1 regarding the t_{I2CF} AC parameter. • In Table 56, added a note stating: “This specification only applies to GPIO pins that are operating from a 3.3-V supply. See Table 63 for the power supply listed for the individual GPIO signal.” [• Added Table 57 to show DC characteristics for GPIO pins supplied by a 2.5-V supply. Same as eTSEC DC characteristics when operating at 2.5 V. • In Section 20, “Clocking,” corrected the sentence “When the device is configured as a PCI agent device, PCI_SYNC_IN is the primary input clock.” to state “When the device is configured as a PCI agent device, PCI_CLK is the primary input clock.” • Added “Value is decided by RCWLR[COREPLL]” to note 1 of Figure 57 • Added paragraph and Figure 59 to Section 22.2, “PLL Power Supply Filtering.” • Added Section 22.4, “SerDes Block Power Supply Decoupling Recommendations • Removed the two figures on PCI undershoot/overshoot voltages and maximum AC waveforms from Section 2.1.2, “Power Supply Voltage Specification,” |

Table 73. Document Revision History (continued)

| Rev. Number | Date | Substantive Change(s) |
|-------------|--------|--|
| 1 | 3/2008 | <ul style="list-style-type: none"> • In Table 63, added LBC_PM_REF_10 & LSRCID3 as muxed with USBDR_PCTL1 • In Table 63, added LSRCID2 as muxed with USBDR_PCTL0 • In Table 63, added LSRCID1 as muxed with USBDR_PWRFAULT • In Table 63, added LSRCID0 as muxed with USBDR_DRIVE_VBUS • In Table 63, moved T1, U2, & V2 from V_{DD} to XCOREVDD. • In Table 63, moved P2, R2, & T3 from V_{SS} to XCOREVSS. • In Table 63, moved P5, & U4 from V_{DD} to XPADVDD. • In Table 63, moved P3, & V4 from V_{SS} to XPADVSS. • In Table 63, removed “Double with pad” for AV_{DD1} and AV_{DD2} and moved AV_{DD1} and AV_{DD2} to Power and Ground Supplies section • In Table 63, added impedance control requirements for SD_IMP_CAL_TX (100 ohms to GND) and SD_IMP_CAL_RX (200 ohms to GND). • In Table 63, updated muxing in pinout to show new options for selecting IEEE 1588 functionality. Added footnote 8 • In Table 63, updated muxing in pinout to show new LBC ECC boot enable control muxed with eTSEC1_MDC • Added pin type information for power supplies. • Removed N1 and N3 from Vss section of Table 63. Added Therm0 and Therm1 (N1 and N3, respectively). Added note 7 to state: “Internal thermally sensitive resistor, resistor value varies linearly with temperature. Useful for determining the junction temperature.” • In Table 65 corrected maximum frequency of Local Bus Frequency from “33–66” to 66 MHz • In Table 65 corrected maximum frequency of PCI from “24–66” to 66 MHz • Added “which is determined by RCWLR[COREPLL],” to the note in Section 20.2, “Core PLL Configuration” about the VCO divider. • Added “(VCOD)” next to VCO divider column in Table 68. Added footnote stating that core_clk frequency must not exceed its maximum, so 2.5:1 and 3:1 core_clk:csb_clk ratios are invalid for certain csb_clk values. • In Table 69, notes were confusing. Added note 3 for VCO column, note 4 for CSB (csb_clk) column, note 5 for USB ref column, and note 6 to replace “Note 1”. Clarified note 4 to explain erratum eTSEC40. • In Table 69, updated note 6 to specify USB reference clock frequencies limited to 24 and 48 for rev. 2 silicon. • Replaced Table 71 “Thermal Resistance for TEPBGAll with Heat Sink in Open Flow”. • Removed last row of Table 19. • Removed 200 MHz rows from Table 21 and Table 5. • Changed VIH minimum spec from 2.0 to 2.1 for clock, PIC, JTAG, SPI, and reset pins in Table 9, Table 47, Table 54, Table 59, and Table 61. • Added Figure 4 showing the DDR input timing diagram. • In Table 19, removed “MDM” from the “MDQS-MDQ/MECC/MDM” text under the Parameter column for the tCISKEW parameter. MDM is an output signal and should be removed from the input AC timing spec table (tCISKEW). • Added “and power” to rows 2 and 3 in Table 10 • Added the sentence “Once both the power supplies...” and PORESET to Section 2.2, “Power Sequencing,” and Figure 3. • In Figure 35, corrected “USB0_CLK/USB1_CLK/DR_CLK” with “USBDR_CLK” • In Table 42, clarified that AC specs are for ULPI only. |
| 0 | 6/2007 | Initial release. |