PF5030_SDS

Fail-safe system basis chip with multiple SMPSs and LDOs

Rev. 2 — 17 March 2023 Product short data sheet

1 General description

PF5030 is a power management integrated circuit (PMIC) designed for S32Z2/E2 processors. Its input voltage of up to 5.25 V maximum makes it ideal to work in conjunction with NXP front system supply families (FS86, FS6x) or any other front supply in the automotive drive train market.

Built-in One-Time Programmable (OTP) memory stores key start-up configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through I^2C after start-up, offering flexibility for different system states.

2 Features and benefits

Voltage Range

- 5.25 V DC maximum operating voltage
- Support operating voltage range down to 3.3 V
- Low power OFF mode with low sleep current (15 µA typical)

Power Supplies

- BUCK1/2: Low voltage integrated synchronous buck converter
  - Configurable output voltage from 0.7 V to 1.5 V and current capability up to 3.5 A DC
  - Capable of multiphase operation for up to 7.0 A DC
- BUCK3: Low voltage integrated synchronous buck converter
  - Configurable output voltage from 1.0 V to 4.1 V and current capability up to 2.5 A DC
- LDO1/2: Low voltage LDO regulator for MCU I/O and system peripheral
  - Configurable Output voltage from 1.1 V to 4.1 V and current capability up to 400 mA DC

System support

- 1x input pin for power-ON detection, 1.8 V, 3.3 V, and 5.0 V compatible
- Analog multiplexer with full system voltages and temperature monitoring
- Enhanced leader / follower power-up sequencing management through XFAILB pin
- 10 ms optional RSTB release delay during power-up for certain MCU compliance
- Device control via 32 bits I^2C interface with 8-bit CRC

Compliancy

- EMC optimization techniques on switching regulators including spread spectrum and manual frequency tuning
- EMI robustness supporting various automotive EMI test standards
- Conducted emission: IEC 61967-4
- Conducted immunity: IEC 62132-4

Functional Safety

- ASIL D capability on safety goal 1 (SG1/CSG_01) on UV/OV for all S32Z2/E2 power rails (0.8 V, 1.1 V, 1.8 V, and 3.3 V)

- Configurable ASIL from QM to ASIL D on safety goal 2 (SG2/CSG_02) on MCU monitoring function (watchdog)
- Independent voltage monitoring circuitry
- Up to 6 voltage monitoring inputs with 1.0 % target accuracy
- Logical and analog built-in self-test (LBIST/ABIST)
- Safety outputs with latent fault detection mechanism (PGOOD, RSTB, FS0B)

Configuration and enablement

- QFN 40 pins with exposed pad for optimized thermal management
- OTP programming for device customization

3 Applications

- EV propulsion and power train domain controller
- Chassis-integrated systems
- S32Z2/E2 companion chip

4 Simplified application diagram

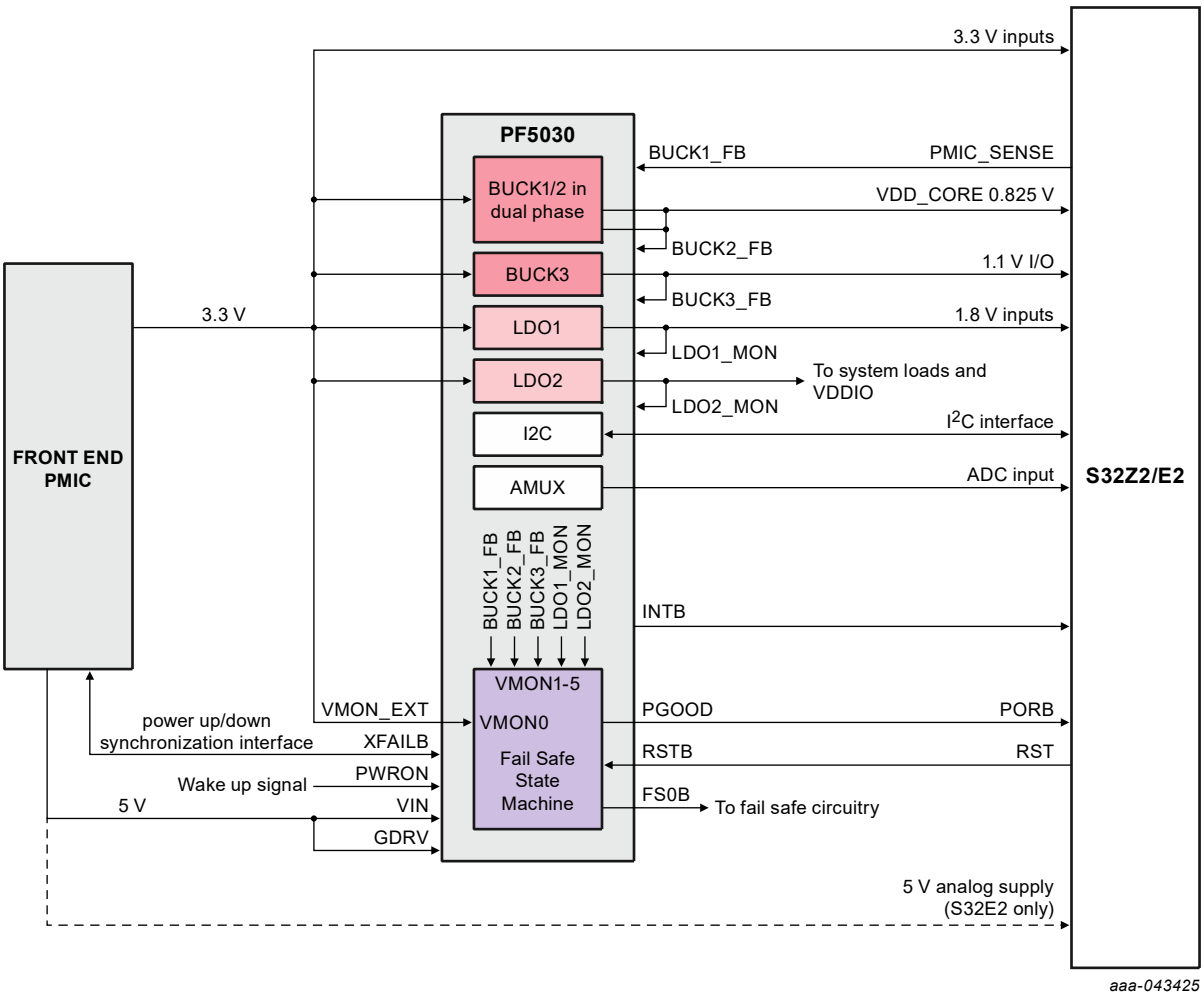


Figure 1. Simplified application diagram

5 Ordering information

5.1 Device family

The PF5030 device family (called PF5030 hereafter) provides selectable features based on part numbering and OTP configuration.

Table 1. Device options

Family	ASIL		Watchdog	BUCK1/2	BUCK3	LDO1/2
	SG1	SG2				
PF5030xxM	D	QM	Disabled	Enabled	Enabled	Enabled
PF5032xxM					Disabled	Enabled
PF5030xxB	D	B	Simple	Enabled	Enabled	Enabled
PF5032xxB					Disabled	Enabled
PF5030xxD	D	D	Challenger	Enabled	Enabled	Enabled
PF5032xxD					Disabled	Enabled

5.2 Part numbering

M	PF	5030	A	M	D	A0	ES
P: prototype M: standard S: custom	LV PMIC	PF5030 core ID[1]	Silicon revision A: A0 B: A1	Ambient temperature (T_A) M: -40 °C to 125 °C	ASIL on SG2 M: QM B: ASIL B D: ASIL D	OTP code A0: OTP A0 xx: OTP xx	Package type ES: dimple wettable flank

[1] See Table 1

Table 2. Ordering information

Part Number[1]	Application	ASIL		Package		
		SG1	SG2	Name	Description	Version
MPF5030BMMA0ES		D	QM	HVQFN40eP	HVQFN40, plastic, thermally enhanced very thin quad flat package, no lead, wettable flanks	SOT618-18(D)
MPF5032BMMA0ES		D	QM			
MPF5030BMBA0ES		D	B			
MPF5032BMBA0ES		D	B			
MPF5030BMDA0ES		D	D			
MPF5032BMDA0ES		D	D			
MPF5030BMMA4ES	Greenbox III S32Z2 DC2 EVB S32E2 DC4 EVB FS86 + S32Z2 (21x21 mm) FS86 + S32E2 (27x27 mm)	D	QM			
MPF5032BMMA5ES	S32Z2 DC1 EVB FS86 + S32Z2 (17x17 mm)	D	QM			
PPF5030AMDA0ES[2]	Prototype / Evaluation	D	QM, B, D			

Table 2. Ordering information*...continued*

Part Number[1]	Application	ASIL		Package		
		SG1	SG2	Name	Description	Version
PPF5030BMDA0ES[3]	Prototype / Evaluation	D	QM, B, D			

[1] To order parts in tape and reel, add the R2 suffix to the part number.
[2] Superset part number that can cover all features for prototype ordering (A0 silicon pass / obsolete).
[3] Superset part number that can cover all features for prototype ordering (A1 silicon pass).

Part numbers ending with A0 OTP code are non-programmed OTP configuration. Preprogrammed OTP configurations are managed through part number extension. For a custom OTP configuration, contact your local NXP sales representative.

6 Internal block diagram

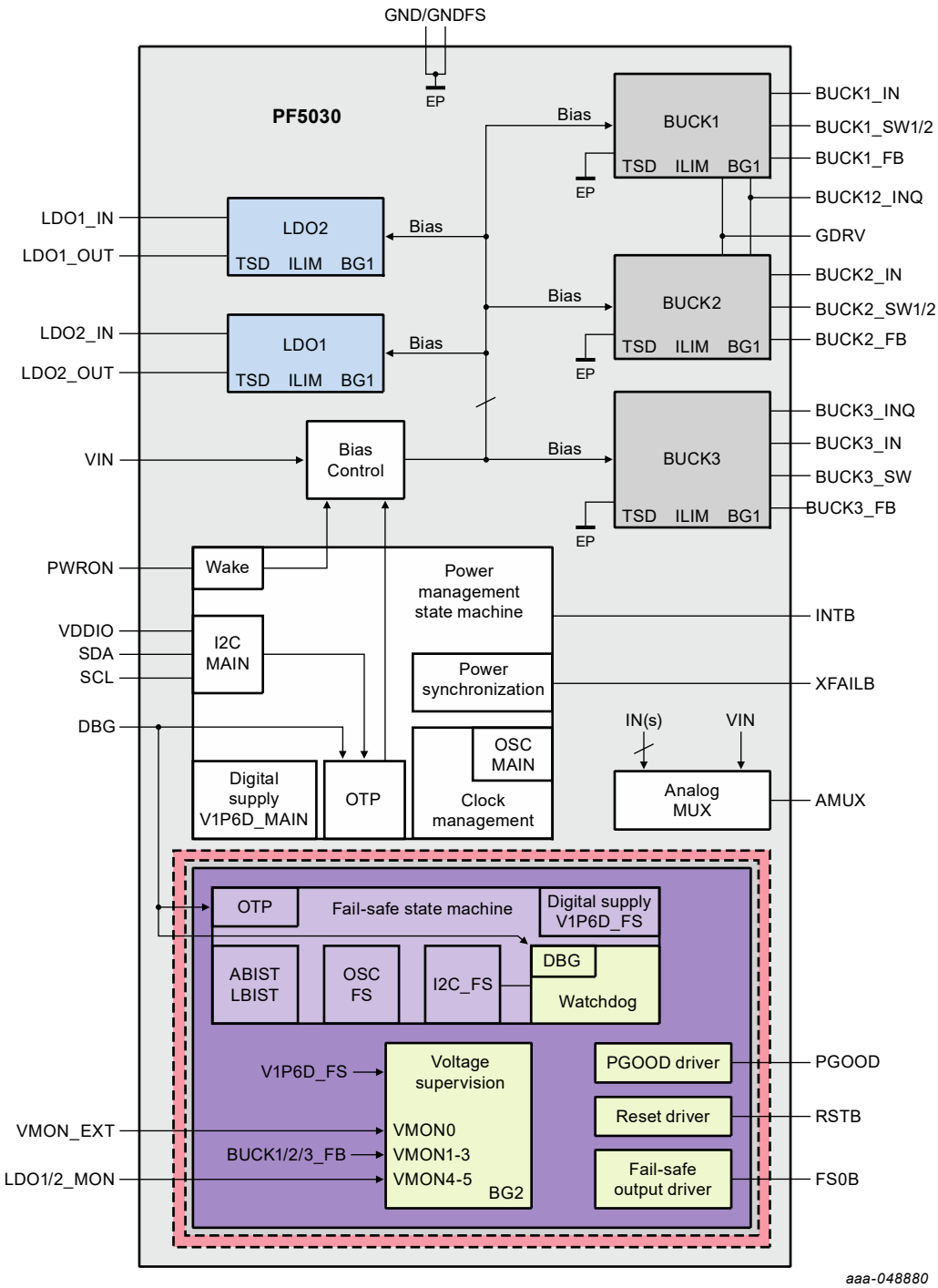


Figure 2. Block diagram

7 Pinning information

7.1 Pinout

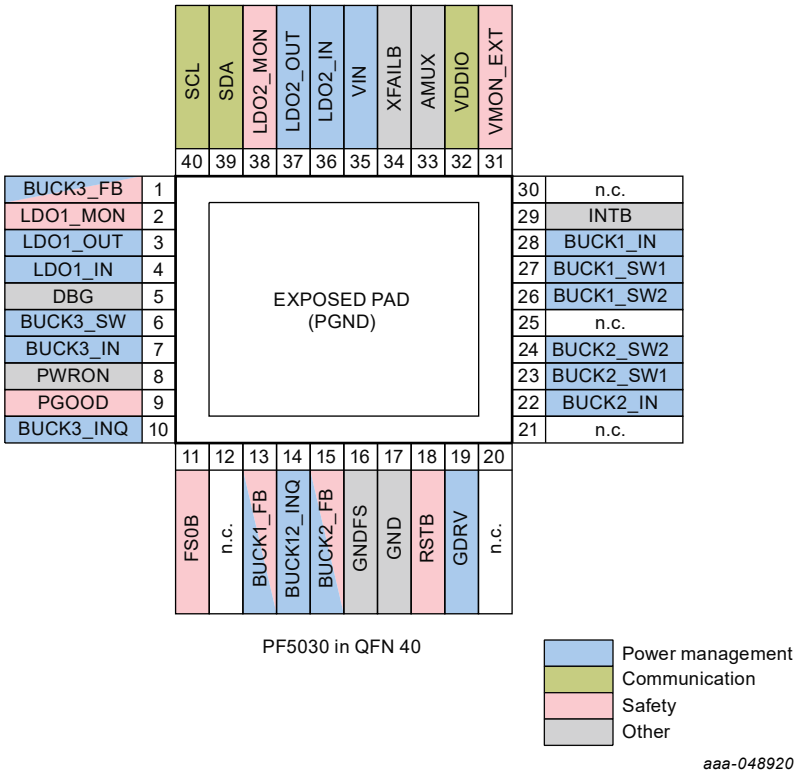


Figure 3. Pin configuration

7.2 Pin description

Table 3. Pin description

Pin	Name	Type	Description
1	BUCK3_FB	Analog input	BUCK3 voltage feedback
2	LDO1_MON	Analog input	LDO1 / VMON4 voltage monitor input
3	LDO1_OUT	Analog output	LDO1 output voltage
4	LDO1_IN	Analog input	LDO1 input voltage
5	DBG	Analog input	Debug mode entry and OTP programming input supply
6	BUCK3_SW	Analog output	BUCK3 switching node
7	BUCK3_IN	Analog input	BUCK3 input voltage
8	PWRON	Digital input	PWRON input for power-up
9	PGOOD	Digital output	Power good output. Active Low. Open drain structure.
10	BUCK3_INQ	Analog input	Quiet input voltage for BUCK3
11	FS0B	Digital output	Fail-safe output 0. Active Low. Open drain structure.

Table 3. Pin description*...continued*

Pin	Name	Type	Description
12	n.c.	Not connected	Not connected pin
13	BUCK1_FB	Analog input	BUCK1 voltage feedback
14	BUCK12_INQ	Analog input	Quiet input voltage for BUCK1 and BUCK2
15	BUCK2_FB	Analog input	BUCK2 voltage feedback
16	GNDFS	Ground	Analog ground pin for fail-safe domain
17	GND	Ground	Analog ground pin for main domain
18	RSTB	Digital input/output	Reset input/output. Active Low. Open drain structure.
19	GDRV	Analog input	Gate drive supply pin for BUCK1 and BUCK2
20	n.c.	Not connected	Not connected pin
21	n.c.	Not connected	Not connected pin
22	BUCK2_IN	Analog input	BUCK2 input voltage
23	BUCK2_SW1	Analog output	BUCK2 switching node pin #1
24	BUCK2_SW2	Analog output	BUCK2 switching node pin #2
25	n.c.	Not connected	Not connected pin
26	BUCK1_SW2	Analog output	BUCK1 switching node pin #2
27	BUCK1_SW1	Analog output	BUCK1 switching node pin #1
28	BUCK1_IN	Analog input	BUCK1 input voltage
29	INTB	Digital output	Interrupt output
30	n.c.	Not connected	Not connected pin
31	VMON_EXT	Analog input	External voltage monitoring
32	VDDIO	Analog input	I/O supply voltage
33	AMUX	Analog output	Analog multiplexer output
34	XFAILB	Digital input/output	External PMIC synchronization pin
35	VIN	Analog input	Main input supply
36	LDO2_IN	Analog input	LDO2 input voltage
37	LDO2_OUT	Analog output	LDO2 output voltage
38	LDO2_MON	Analog input	LDO2 / VMON5 voltage monitor input
39	SDA	Digital input/output	I^2C data signal
40	SCL	Digital input	I^2C clock signal
EP	Exposed pad	Ground	Exposed pad must be connected to GND

8 Limiting values

Table 4. Maximum ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Conditions	Parameter	Min	Max	Unit
Voltage ratings					
GND, GNDFS	DC voltage	GND pins	−0.3	0.3	V
FS0B	DC voltage	FS0B pin	−0.3	40	V
DBG	DC voltage	DBG pin	−0.3	10	V
VIN	DC voltage	VIN pin	−0.3	5.5	V
	Transient voltage up to 2.2 µs		−0.3	6	
BUCKx_IN	DC Voltage	BUCKx_IN pin x from 1 to 3	−0.3	5.5	V
	Transient voltage < 3 µs		−0.3	6.5	
BUCKx_SWy	Transient voltage < 20 ns	BUCKx_SWy pin x from 1 to 3, y = none, 1 or 2	−0.3	6.5	V
All other pins	DC voltage	all other pins	−0.3	5.5	V

9 Electrostatic discharge

9.1 Human body model (JESD22/A114)

The device is protected up to ±2 kV, according to the human body model standard with 100 pF and 1.5 kΩ. This protection is ensured at all pins.

9.2 Charged device model

The device is protected up to ±750 V on corner pins and up to ±500 V on all other pins, according to the AEC Q100 - 011 charged device model standard.

9.3 Discharged contact test

The FS0B pin is protected up to ±8 kV, according to the following discharged contact tests.

- Discharged contact test (IEC61000-4-2) at 150 pF and 330 Ω
- Discharged contact test (ISO10605.2008) at 150 pF and 2 kΩ
- Discharged contact test (ISO10605.2008) at 330 pF and 2 kΩ

10 Thermal characteristics

Table 5. Temperature ranges

Symbol	Description (Rating)	Min	Max	Unit
Thermal ratings				
T_A	Ambient temperature (Grade 1)	−40	125	°C
T_J	Junction temperature (Grade 1)	−40	150	°C

Table 5. Temperature ranges*...continued*

Symbol	Description (Rating)	Min	Max	Unit
T_{STG}	Storage Temperature	−55	150	°C

Table 6. Thermal resistance (per JEDEC JESD51-2)

Symbol	Description	Value[1]	Unit
$R_{\theta JA}$	Thermal resistance Junction to Ambient[2]	30.1	°C/W
$R_{\theta JCBOTTOM}$	Thermal resistance Junction to Case Bottom[3][4] (with uniform power dissipation on the silicon die)	2.4	°C/W
$R_{\theta JCTOP}$	Thermal resistance Junction to Case Top[5] (with uniform power dissipation on the silicon die)	20.6	°C/W
Ψ_{JT}	Thermal characterization parameter Junction to Top[2]	0.3	°C/W

[1] Thermal test board meets JEDEC specification for this package (JESD51-7).
[2] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
[3] Thermal resistance between the die and the printed circuit board. Board temperature is measured on the top surface of the board near the package.
[4] For exposed pad packages where the pad would be expected to be soldered, junction to case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.
[5] Junction-to-Case Top thermal resistance determined using an isothermal cold plate. Case temperature refers to the mold surface temperature at the package top side dead center.

11 Package outline

PF5030 package is a QFN, thermally enhanced, wettable flanks, 6 x 6 x 0.85 mm, 0.5 mm pitch, 40 pins.

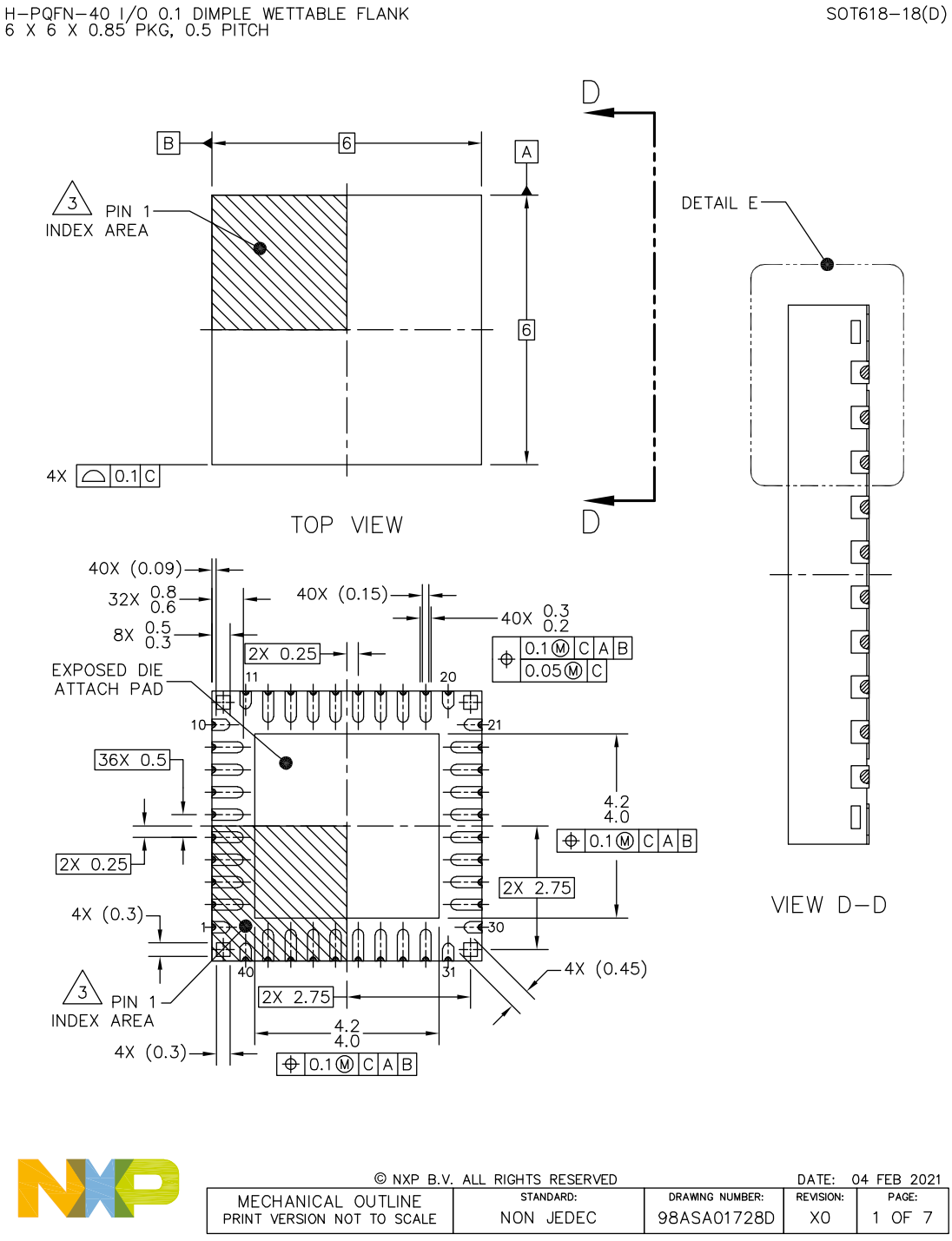
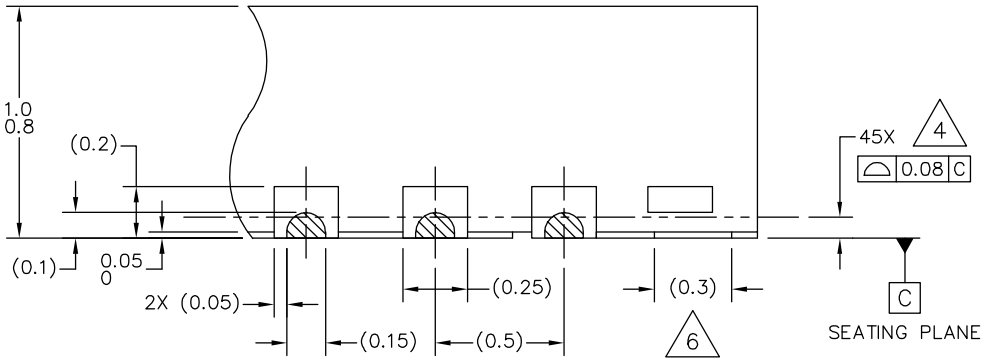


Figure 4. Package drawing - top and bottom view

H–PQFN–40 I/O 0.1 DIMPLE WETTABLE FLANK
6 X 6 X 0.85 PKG, 0.5 PITCH

SOT618–18(D)



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DATE: 04 FEB 2021

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01728D	REVISION: X0	PAGE: 2

Figure 5. Package drawing - dimple wettable flank

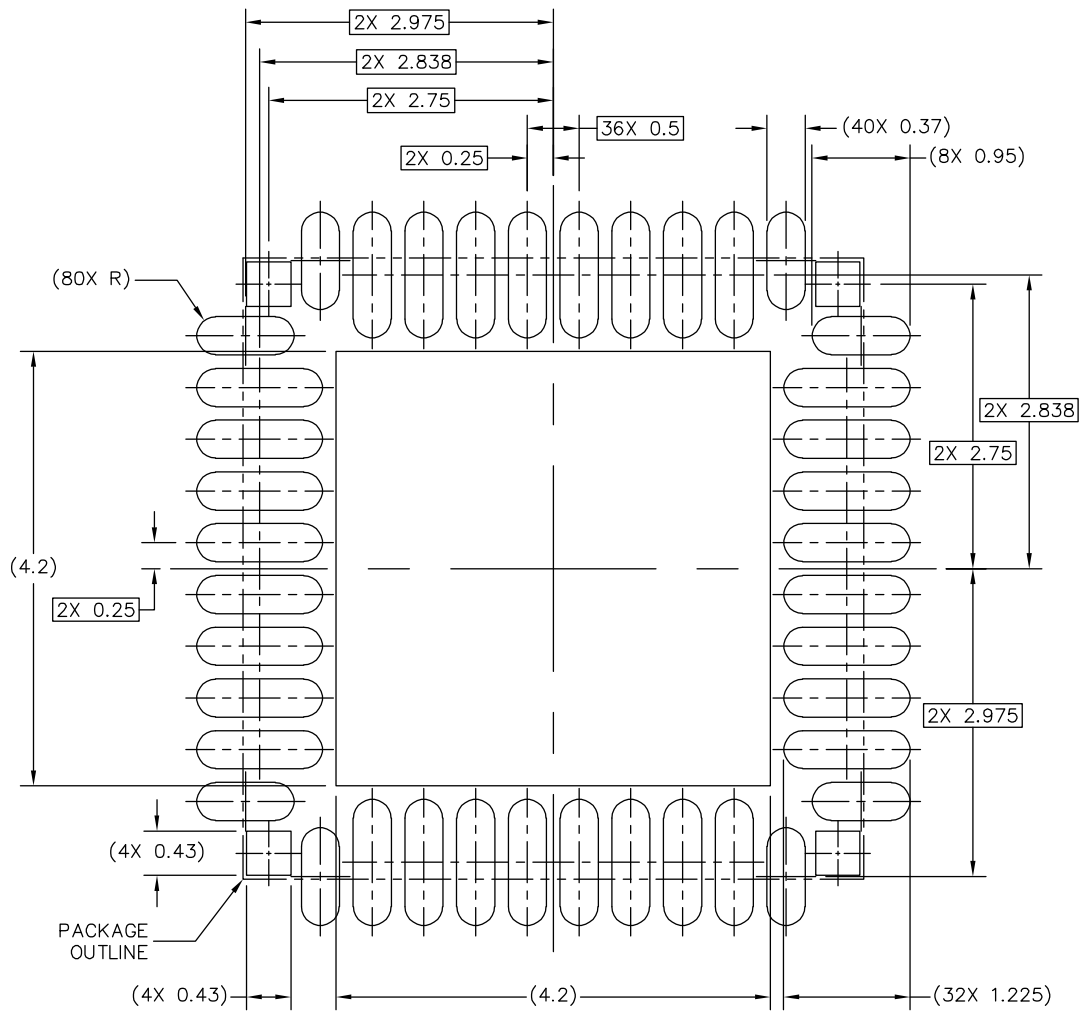

Figure 6. PCB design guidelines - solder mask opening pattern

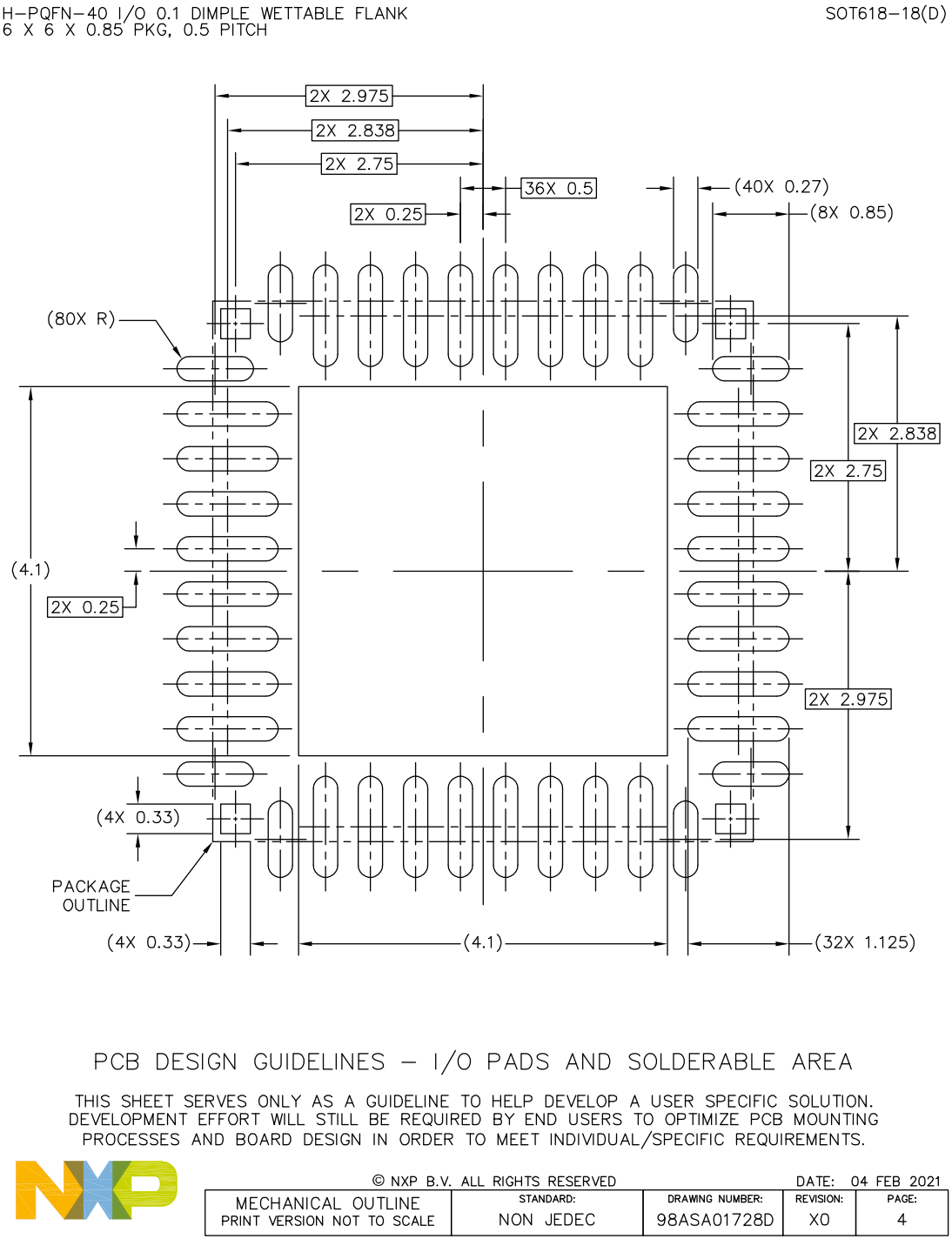

Figure 7. PCB design guidelines - I/O pads and solderable area

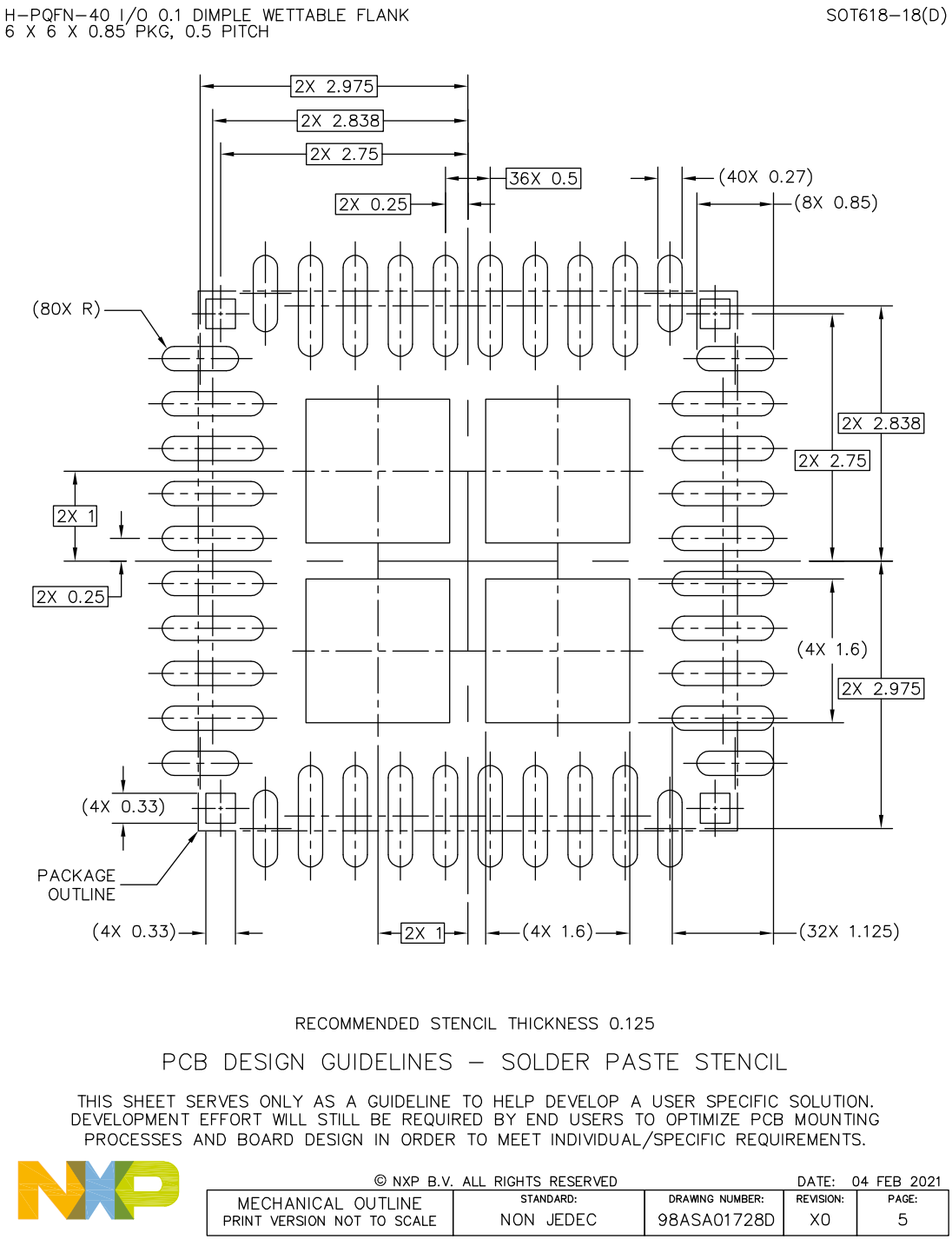

Figure 8. PCB design guidelines - solder paste stencil

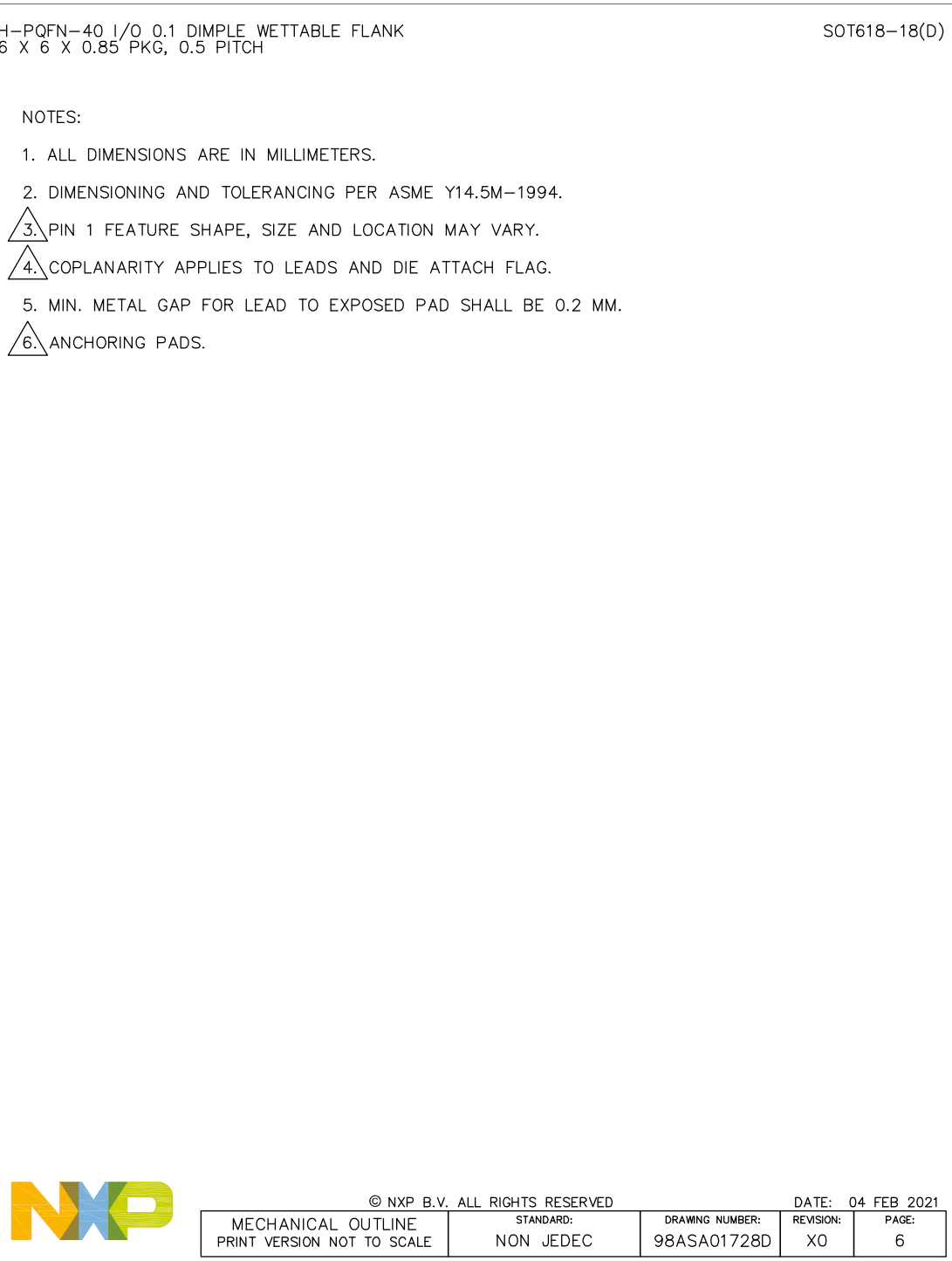

Figure 9. Notes

12 Revision History

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PF5030_SDS v. 2	20230317	Product Data Sheet	202303007I	PF5030_SDS v. 1
	• Revised Section 1 • Revised Section 2 • Changed titles of Section 7, Section 8, and Section 11 to conform to NXP template • Revised Table 1 • Revised Table 2 • Revised title and content of Table 5 • Added Table 6			
PF5030_SDS v. 1	20221122	Product Data Sheet	—	—
Modifications:	• Initial Release			

13 Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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