PolarFire® SoC FPGA Video Kit

Introduction

Microchip PolarFire® SoC FPGA video kit (MPFS250-VIDEO-KIT) is RoHS compliant. It enables you to evaluate the PolarFire SoC MPFS250TS-1FCG1152I FPGA for the following interfaces:

- MIPI CSI-2 RX Interface
- MIPI TX DSI-Application
- MikroBus
- CAN Interface
- UART Interface
- Gigabit Ethernet
- USB ULPI
- PCIe Gen2
- eMMC/MicroSD Card
- HDMI2.0
- eFP6 (Embedded FlashPro6)
- DDR4 memory
- LPDDR4 memory
- FMC HPC with eight Transceiver lanes
- SPI Interface

Table of Contents

1. Getting Started

This section provides a high-level overview of the PolarFire SoC video kit.

1.1 Kit Contents

The following table lists the contents of the PolarFire SoC video kit.

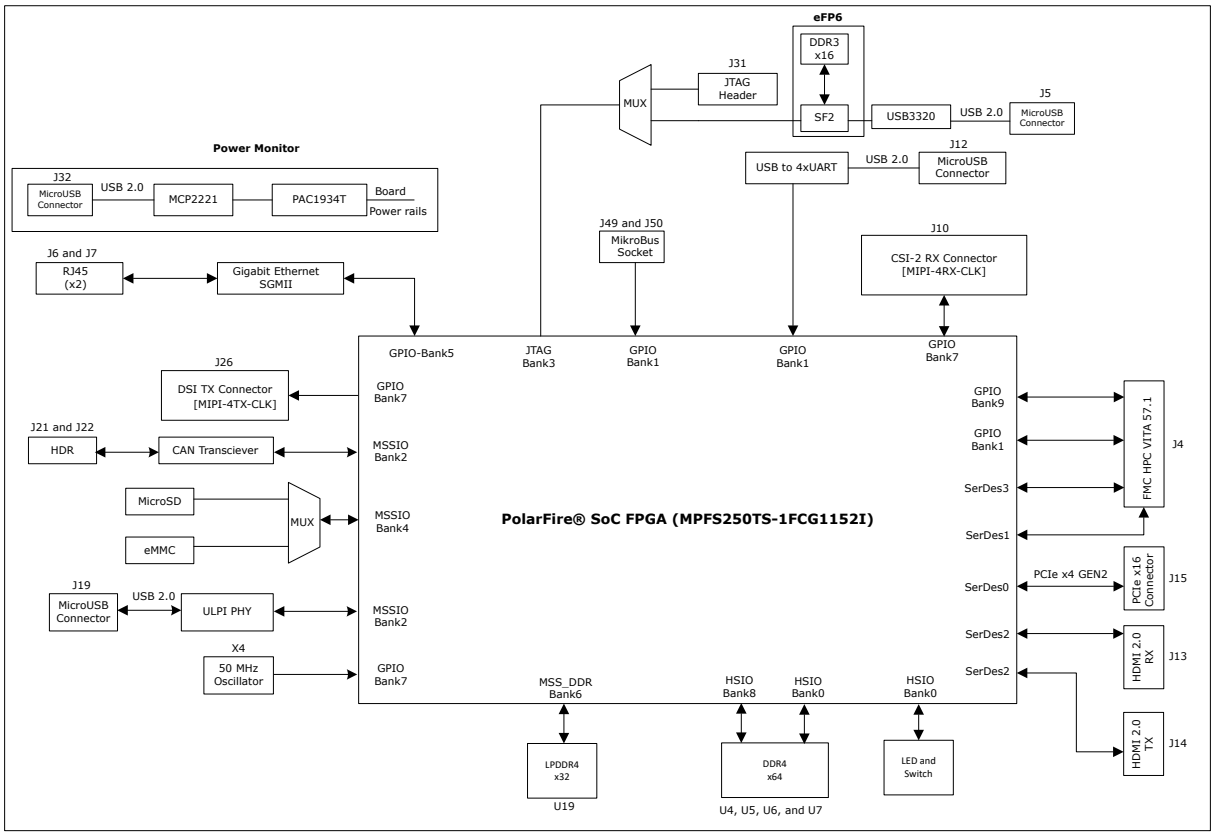
Table 1-1. Kit Contents

Item	Quantity
Dual Camera Sensor Module	1
PolarFire® SoC Video Board featuring the MPFS250TS-1FCG1152I device with 250K logic elements	1
12V, 5A AC power adapter and cord	1
MicroUSB cable	2
HDMI cable	1
Ethernet cable	1
Quickstart card	1

1.2 Block Diagram

The following figure shows the block diagram of the PolarFire SoC video kit.

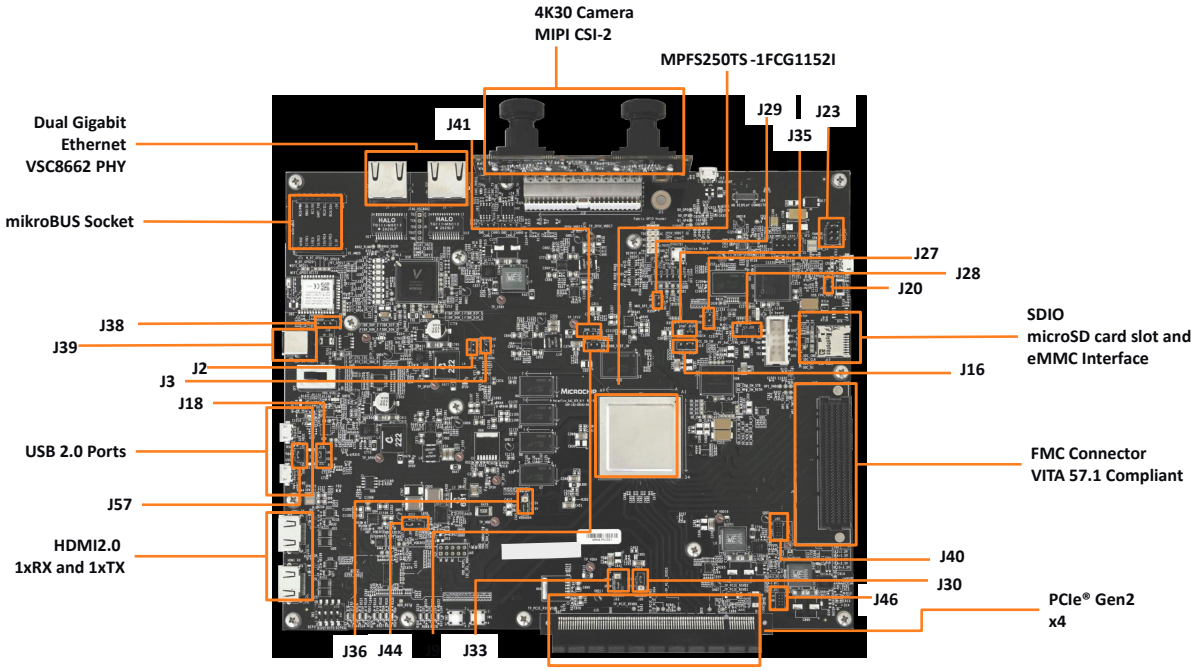
Figure 1-1. Block Diagram



1.3 Board Overview

The following figure shows a labeled image of the PolarFire SoC video kit highlighting its components.

Figure 1-2. Board Callout



The following table lists the components of the PolarFire SoC video kit.

Table 1-2. Board Components

Component	Label on Board	Description
Featured Device		
PolarFire® SoC FPGA	—	MPFS250TS-1FCG1152I FPGA with data security feature.
Power Supply		
12V power supply	J39	The board is powered by a 12V power source using an external 12V or 5A DC jack.
ON/OFF switch	SW5	Power ON/OFF switch from 12V external DC jack.
Clocks		
On-board 50 MHz clock oscillator	X4	50 MHz clock oscillator with single-ended output.
XCVR reference clock	Y1	148.5 MHz oscillator (differential LVDS output) that provides reference clock (REFCLK) through PolarFire SoC device pins AF29 and AF30. These pins are connected to the XCVR.
FPGA Programming and Debugging		
Micro USB	J5	Connector for programming the device using embedded FlashPro6 (eFP6).
JTAG programming header	J31	Header for programming and debugging the PolarFire SoC device using external FlashPro4 or FlashPro5. In the FlashPro software, the appropriate programmer (FlashPro4 or FlashPro5) must be selected.

.....continued

Component	Label on Board	Description
SPI Flash	U48	One 1 Gb SPI Flash from Micron MT25QL01GBBB8ESF-0SIT (P/N) is connected to SPI pins on Bank3 of the PolarFire® SoC device.
Memory Chips		
DDR4 memory	U4, U5, U6, and U7	Four 8 Gb (MT40A512M16LY-075:E) chips are connected in Fly-by topology with a 64-bit data bus for storing data bits.
LPDDR4 memory	U19	LPDDR4 (x32) memory (MT53D512M32D2DS-053) with maximum data rate of 1600 Mbps.
FMC HPC connector	J4	FMC connector with eight SerDes lanes (SerDes1, 3).
Video Interfaces		
CSI-2 RX connector	J10	MIPI CSI-2 connector for receiving data and clock signals from Camera sensor board.
DSI TX connector	J26	MIPI data and clock signals are connected to this display connector.
General Purpose I/O		
Switches	SW1 and SW2	Push-button switches for debugging applications.
DIP Switches	SW3	Four DIP switches for testing.
Light-emitting diodes (LEDs)		Four Active-High LEDs connected to some of the user I/Os for debugging, and thirteen Active-High LEDs used for indicating power supply.
Device reset	SW4	Device Reset.

2. Hardware Settings

This section provides information about jumper settings, switches, LEDs, and DIP switches on the PolarFire SoC Video Kit.

2.1 Jumper Settings

The following table lists the jumper settings and their corresponding functions.

Table 2-1. Jumper Settings

Jumper	Pin(s)	Functionality	Default Position
J28	1 and 2	Close pin 1 and 2 to program through the embedded FlashPro6. Open pin 1 and 2 to program through the external FlashPro4 or FlashPro5.	1 and 2 are opened.
J29	1 and 2	Close pin 1 and 2 for the SPI Header. Open pin 1 and 2 for the external on board SPI Flash.	1 and 2 are opened.
J36	1, 2, and 3	Close pin 1 and 2 for setting VDDAUX4 to 3.3V. Close pin 2 and 3 for setting VDDAUX4 to 2.5V.	1 and 2 are opened. 2 and 3 are closed.
J30	1,2, and 3	Close pin 1 and 2 for setting VDDAUX1 to 3.3V. Close pin 2 and 3 for setting VDDAUX1 to 2.5V.	1 and 2 are closed. 2 and 3 are opened.
J33	1, 2, and 3	Close pin 1 and 2 for setting VDDAUX9 to 3.3V. Close pin 2 and 3 for setting VDDAUX9 to 2.5V.	1 and 2 are closed. 2 and 3 are opened.
J44	1, 2, and 3	Close pin 1 and 2 for setting VDD to 1.05V. Close pin 2 and 3 for setting VDD to 1.0V.	1 and 2 are closed. 2 and 3 are opened.

Table 2-2. Additional Jumper Settings

Jumper	Default Position	Description
J46	9 and 10 are closed.	Bank1 voltage
J40	9 and 10 are closed.	Bank9 voltage
J35	2 and 3 are closed.	Bank4 voltage
J2 and J3	Open	DDR4 ref voltage
J20	1 and 2 are closed.	VBUS for FP6
J23	1 and 2 are closed.	Backlight led driver VANODE
J27	Open	JTAG TRSTB
J16	2 and 3 are closed.	V+ for SD Interface
J41	1 and 2 are closed.	125 MHz output
J9	Open	MSS DDR Vref
J38	Open	WiFi chip I^2C clk and data
J18	Open	USB ID

.....continued		
Jumper	**Default Position**	**Description**
J57	1 and 2 are closed.	USB VBUS

Note: For more information on jumper settings, see *Board Level Schematics* (provided separately).

2.2 LEDs

The following table lists the power supply LEDs.

Table 2-3. LEDs

LED	Description
12P0V-Blue	12V voltage rail
5P0V-Green	5V voltage rail
3P3V-Green	3.3V voltage rail
2P5V-Green	2.5V voltage rail
1P8V-Green	1.8V voltage rail
VDD-Green	1.05 or 1.0V voltage rail
VDDA-Green	1.05V voltage rail
1P1V-Green	1.10V voltage rail
VDDI1-Green	Bank1 voltage rail
1P2V-Green	1.2V voltage rail
VDDI9-Green	Bank9 voltage rail
1P5V_DDR3-Green	DDR3 1.5V voltage rail
2P5V_VDDI7-Green	Bank7 voltage rail

2.3 Power Sources

The PolarFire SoC video kit board uses Microchip power supply devices. For more information about these power supply devices, see DC-DC Linear Voltage Regulators, Switching Regulators, LDOs, and Charge Pumps.

The following table lists the key power supplies required for normal operation of the PolarFire SoC video kit.

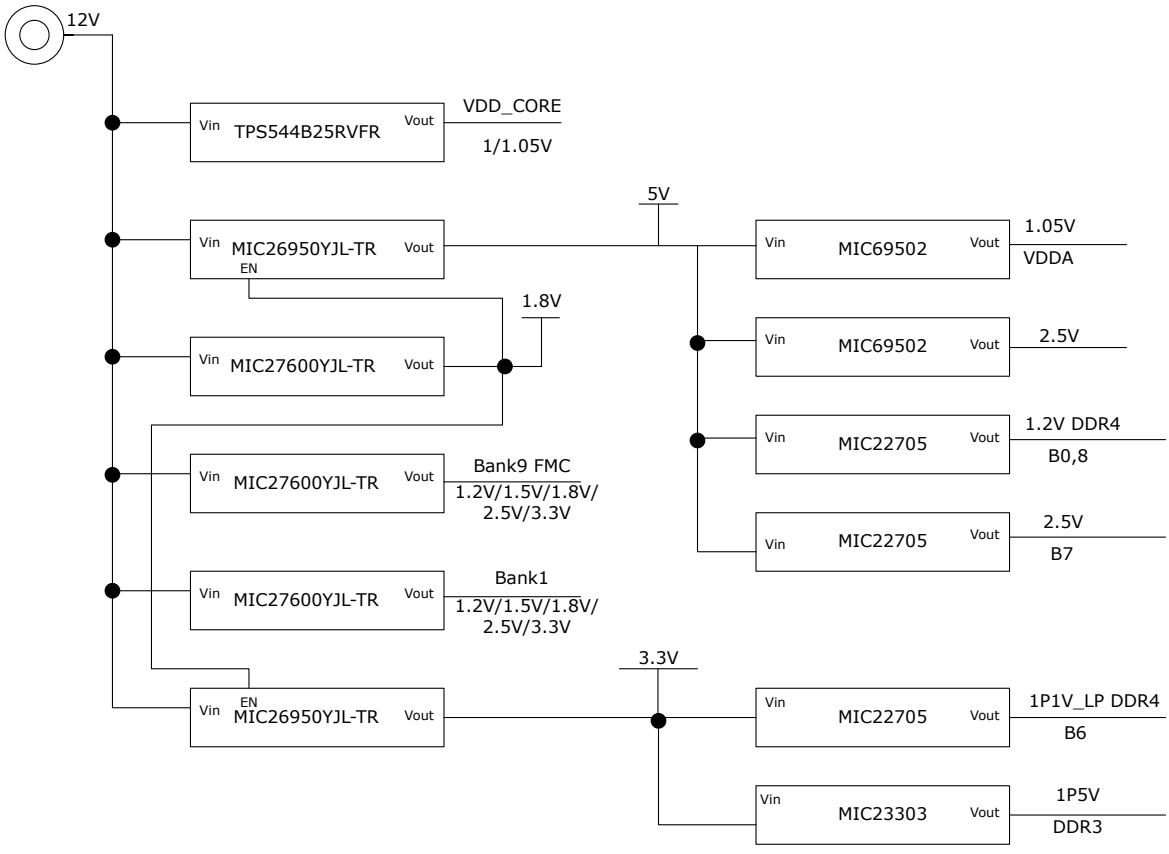
Table 2-4. Voltage Rails in PolarFire SoC Video Kit

PolarFire® SoC Bank	I/O Rail	Voltage
Bank0	1P2V	1.2V
Bank1	1P2V 3P3V	1.2V (DSI MIPI TX) 3.3V (UART, PCIE, GbE, MikroBus, WIFI BT)
Bank2	3P3V	3.3V
Bank3	3P3V	3.3V

.....continued		
PolarFire® SoC Bank	**I/O Rail**	**Voltage**
Bank4	1P8V 3P3V	1.8V (HS200, HS400) 3.3V (Legacy MMC and High-speed DDR)
Bank5	3P3V	3.3V
Bank6	1P1V	1.1V
Bank7	2P5V	2.5V
Bank8	1P2V	1.2V
Bank9	3P3V	3.3V (default)

The following figure shows the power supply scheme used on the PolarFire SoC video kit.

Figure 2-1. Power Supply Topology



The following table lists the Microchip power regulators for PolarFire SoC FPGA voltage rails.

Table 2-5. Power Regulators

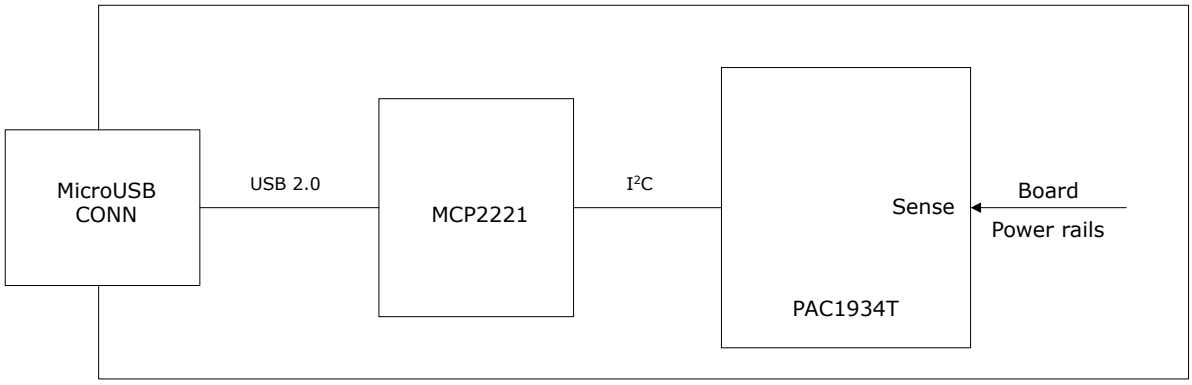
Voltage Rail	Part Number	Description	Current
5P0V (5V)	MIC26950YJL-TR	IC REG BUCK ADJUSTABLE 12A 28MLF	12A
VDD (1V/1.05V)	TPS544B25RVFT	IC REG BUCK ADJ 20A 40LQFN	20A
1P2V (1.2V)	MIC22705YML-TR	IC REG BUCK ADJUSTABLE 7A 24MLF	7A
2P5V_VDDI7 (2.5V)	MIC22705YML-TR	IC REG BUCK ADJUSTABLE 7A 24MLF	7A
1P8V (1.8V)	MIC27600YJL-TR	IC REG BUCK ADJUSTABLE 7A 28MLF	7A
VDDI9 (1.2/1.5/1.8/2.5V/3.3V)	MIC27600YJL-TR	IC REG BUCK ADJUSTABLE 7A 28MLF	7A
0P6V_VTT_DDR4, 0P6V_VREF_DDR4	MIC5166YML-TR	ICPWR SUP 3A HS DDR TERM 10MLF	3A
0P75V_VTT_DDR3, 0P75V_VREF_DDR3	MIC5166YML-TR	ICPWR SUP 3A HS DDR TERM 10MLF	3A
VDDI1 (1.2/1.5/1.8/2.5V/3.3V)	MIC27600YJL-TR	IC REG BUCK ADJUSTABLE 7A 28MLF	7A
2P5V (VDD25, VDDA25, VDD_XCVR_CLK)	MIC69502WR	ICREG LINEAR POS ADJ 5A SPAK-7	5A
3P3V (3.3V)	MIC26950YJL-TR	IC REG BUCK ADJUSTABLE 12A 28MLF	12A
1P5V_DDR3 (1.5V)	MIC23303YML-T5	IC REG BUCK ADJUSTABLE 3A 12DFN	3A
1P1V (1.1V)	MIC22705YML-TR	IC REG BUCK ADJUSTABLE 7A 24MLF	7A
VDDA (1.05V)	MIC69502WR	ICREG LINEAR POS ADJ 5A SPAK-7	5A

2.4 Power Monitor (Voltage and Current Monitoring)

The board includes a 4-channel PAC1934T-I/JQ power monitor chip for monitoring all power rails on the board. Multiple PAC1934T parts can be used to measure power for all power rails on the board. A10 mohm sense resistor is added on all power rails on the board. The drop across a sense resistor is measured in finding the current flowing through a voltage rail. Voltage and current measurements are read through USB to I^2C bridge MCP2221.

The following figure shows the power monitoring scheme used on the board.

Figure 2-2. Power Monitoring Scheme



3. Board Components and Operations

This section describes the key components of the PolarFire SoC Video Kit board and important board operations.

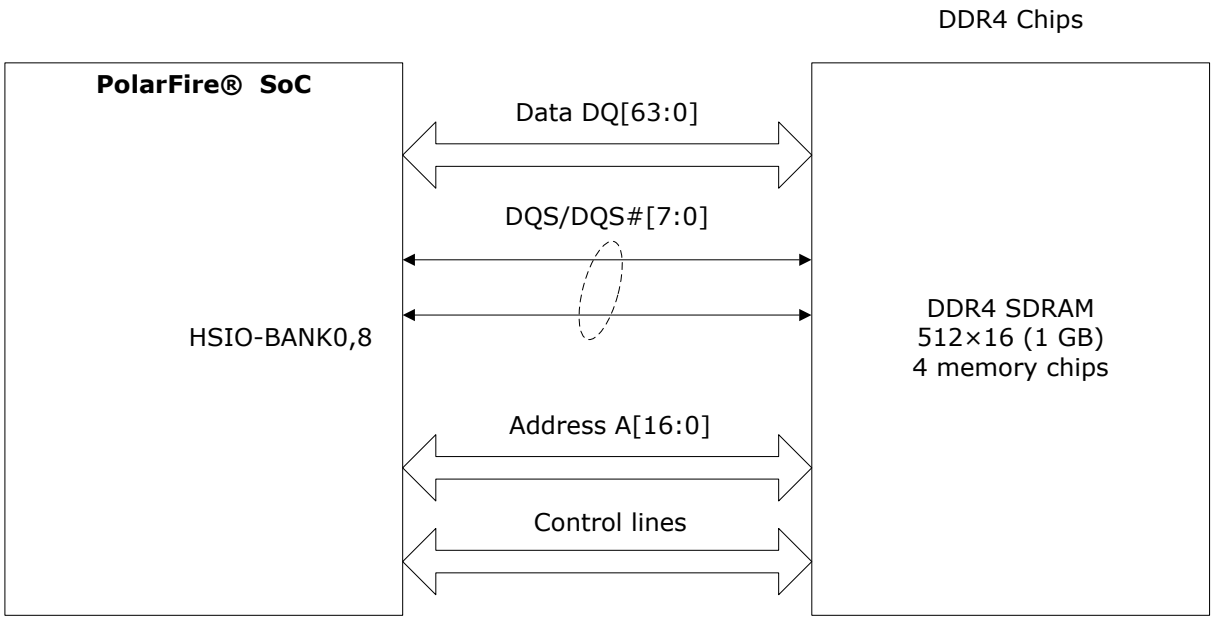
3.1 Memory Interface

This section describes DDR4, LPDDR4, and eMMC/MicroSD card memory interface with the PolarFire SoC device.

3.1.1 DDR4 Memory

The following figure shows the DDR4 memory interface scheme.

Figure 3-1. DDR4 Memory Interface



The DDR4 memory (x64 configuration) is connected to the PolarFire SoC fabric I/O Bank0 and Bank8 (HSIO). Four of x16 DDR4 chips have been used to form x64 configuration.

The DDR4 SDRAM specifications are as follows:

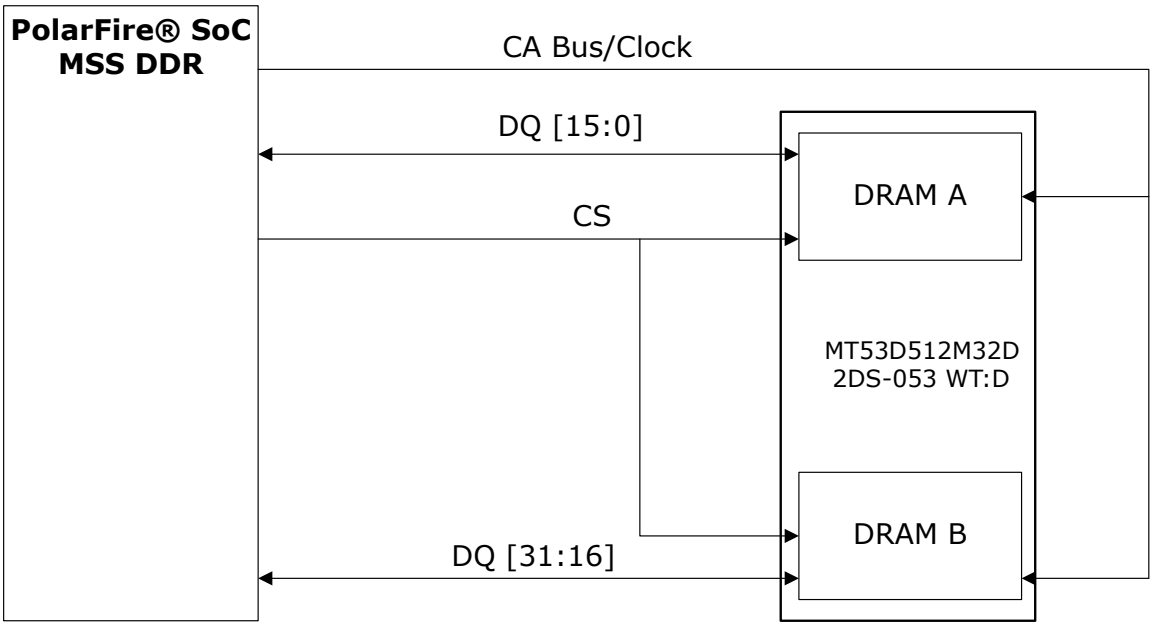
Part number:	MT40A512M16LY-075:E
Manufacturer:	Micron
Quantity:	Four chips are connected in fly-by topology
Density:	32 Gb

The PolarFire SoC video kit uses DDR4 and POD12 standards for the DDR4 interface. The default board assembly for the DDR4 standard uses RC terminations.

3.1.2 LPDDR4 Memory

The following figure shows the LPDDR4 single rank x32 memory interface scheme.

Figure 3-2. LPDDR4 Memory Interface

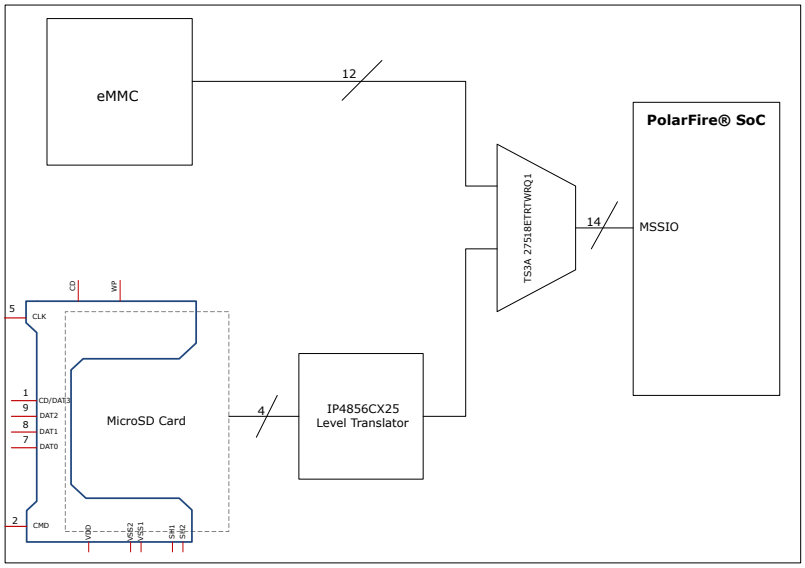


The LPDDR4 (x32) memory is connected to the dedicated MSS DDR (Bank6) of the PolarFire SoC device. The MSS DDR supports single channel x32 LPDDR4 with maximum data rate of 1600 Mbps. The part number of the LPDDR4 memory is MT53D512M32D2DS-053 WT:D TR.

3.1.3 eMMC/MicroSD Card

The following figure shows the eMMC/MicroSD Card interface.

Figure 3-3. eMMC/MicroSD Interface

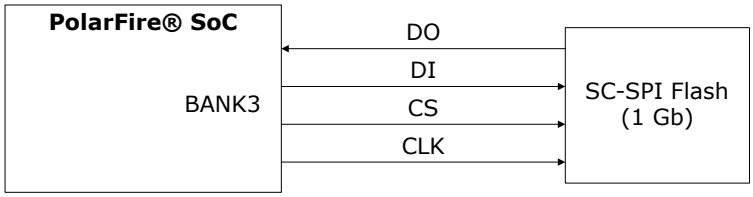


The PolarFire SoC video kit includes an 8 GB eMMC 5.1 NAND Flash and a MicroSD card interface to store PolarFire SoC Linux boot code. A high-speed multiplexer is used to select either eMMC or MicroSD card.

3.2 SPI Serial Flash

The following figure shows the SPI Flash and its interface with the PolarFire SoC device.

Figure 3-4. SPI Flash Interface



A 1 Gb SPI Flash memory is connected to the PolarFire SoC system controller's SPI controller for IAP programming. This SPI Flash is used to store bit streams.

The specifications of the SPI Flash are as follows:

Part Number:	MT25QL01GBBB8ESF-0SIT
Manufacturer:	Micron
Density:	1 Gb
Voltage:	2.7V to 3.6V
Frequency:	90 MHz
Quantity:	1
SPI Mode:	Mode 0 and Mode 3

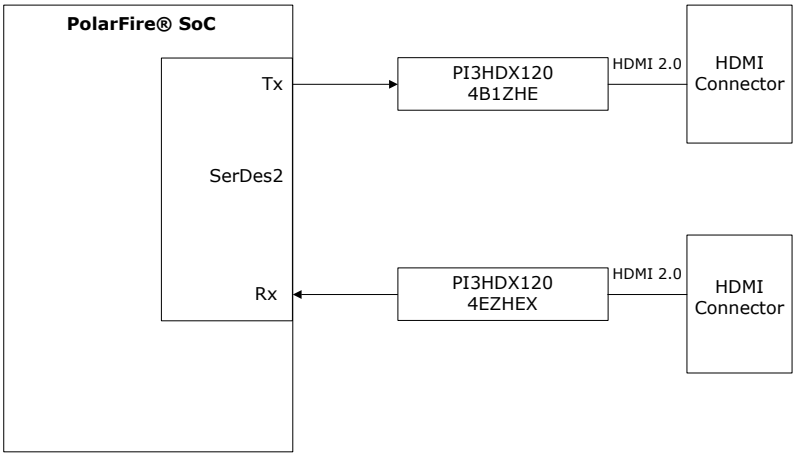
3.3 HDMI 2.0 Interface

This section describes HDMI 2.0 Tx and Rx interface.

3.3.1 HDMI 2.0 Tx

The following figure shows the HDMI 2.0 Tx interface on the board.

Figure 3-5. HDMI 2.0 Interface



The HDMI 2.0 Transmitter interface is connected to Tx SerDes2 of the PolarFire SoC device. HDMI 2.0 Re-driver is used for converting SerDes CML levels to HDMI 2.0 compliant level.

The HDMI 2.0 connector specifications are as follows:

Part number:	RAHHD19TR
Manufacturer:	Switchcraft Inc.

The HDMI 2.0 Re-Driver specifications are as follows:

Part number:	PI3HDX1204B1ZHE
Manufacturer:	Diodes

3.3.2 HDMI 2.0 Rx

The HDMI 2.0 receiver interface is connected to Rx SerDes2 of the PolarFire SoC device. HDMI 2.0 Re-driver is used for converting HDMI 2.0 levels to SerDes CML.

The HDMI 2.0 Rx connector specifications are as follows:

Part Number:	RAHHD19TR
Manufacturer:	Switchcraft Inc.

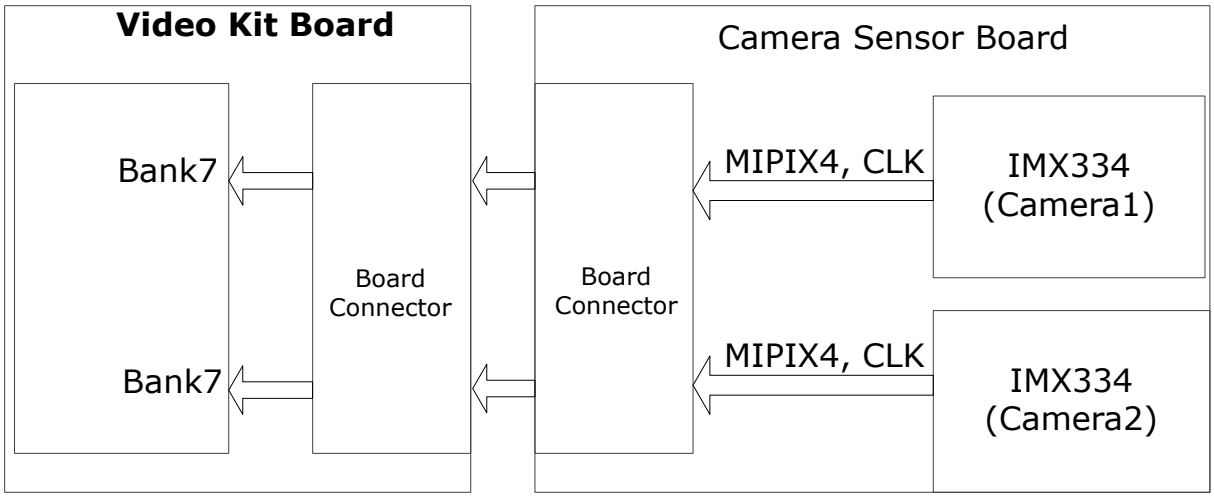
The HDMI 2.0 re-driver specifications are as follows:

Part Number:	PI3HDX1204EZHEX
Manufacturer:	Diodes

3.4 MIPI-RX Connector (CSI-2 Application)

The board supports a dual camera image sensor daughter card that can be connected using the CSI-2 RX interface (J10) for CSI-2 RX applications. The daughter card includes two IMX334 cameras. Each image sensor supports a four-lane MIPI interface. The daughter card is connected to the board through the board-to-board connector, as shown in the following figure. The MIPI output signals are connected to Bank7.

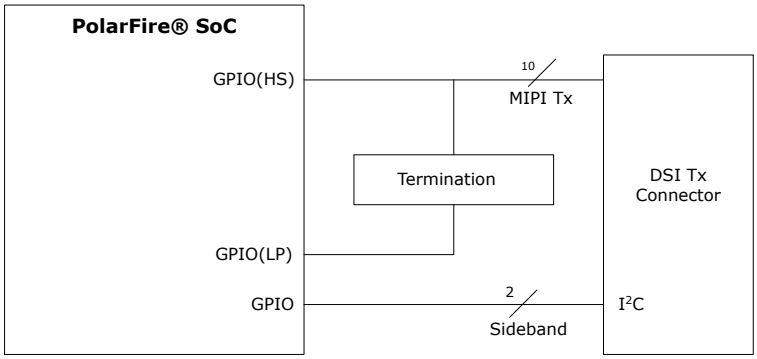
Figure 3-6. MIPI-RX Connection



3.5 MIPI-TX Connector (DSI Application)

The board supports the MIPI transmitter x4 lanes and clock for DSI application, as shown in the following figure. MIPI TX signals are interfaced to J26 connector on the board. For more information, see the *Board Level Schematics* (provided separately).

Figure 3-7. MIPI-TX Connection (DSI Application)



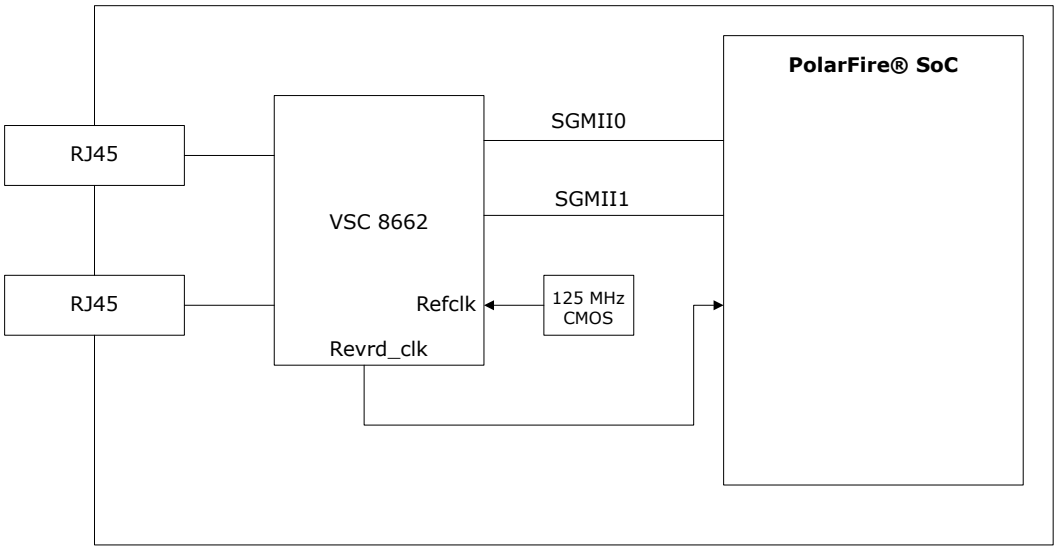
MIPI Tx includes five pairs of high-speed differential LVDS data (with clock) as well as five pairs of low-power LVCMOS12 data (with clock). The video kit supports LS055T3SX05 LCD module over MIPI Tx.

Part Number of the Display Connector:	AXE540127A
Manufacturer:	Panasonic

3.6 Gigabit Ethernet

For Ethernet applications, the kit includes two Gigabit Ethernet interfaces, which connect to Microchip's PHY VSC8662XIC as shown in the following figure. The PHY interfaces with the PolarFire SoC device.

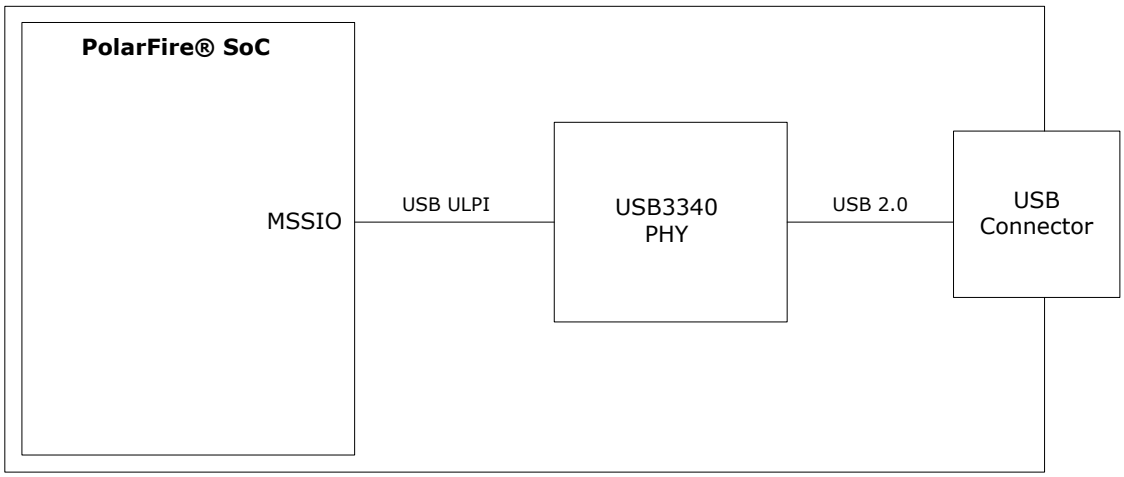
Figure 3-8. SGMII Interface



3.7 USB 2.0

The following figure shows the USB 2.0 interface scheme.

Figure 3-9. USB 2.0 Interface



The on-board USB chip is accessed through PolarFire SoC MSS I/Os. USB 2.0 controller integrated in PolarFire SoC is connected to ULPI PHY. USB physical transceiver is connected to USB 2.0 controller integrated in PolarFire SoC device.

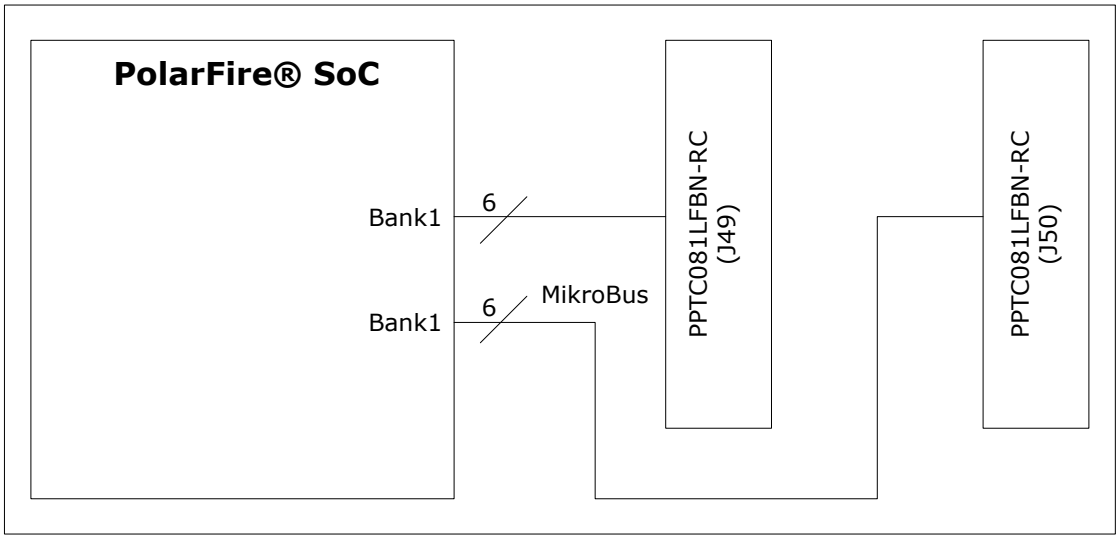
The on-board USB chip specifications are as follows:

Part Number:	USB3340
Manufacturer:	Microchip

3.8 MikroBus

The following figure shows the MikroBus interface scheme.

Figure 3-10. MikroBus Interface



The kit supports two 8-pin MikroBus connectors (J49 and J50). The MikroBus connectors specifications are as follows:

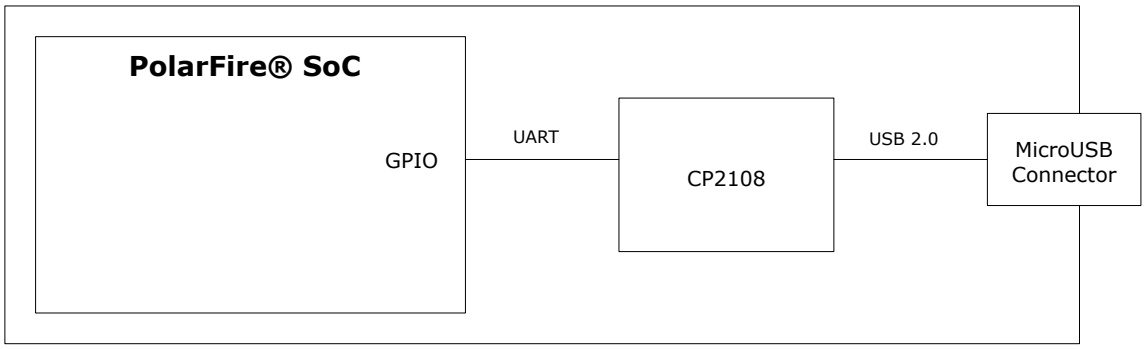
Part number:	PPTC081LFBN-RC

Manufacturer:	Sullins Connector Solutions

3.9 UART

The following figure shows the UART interface scheme.

Figure 3-11. UART Interface

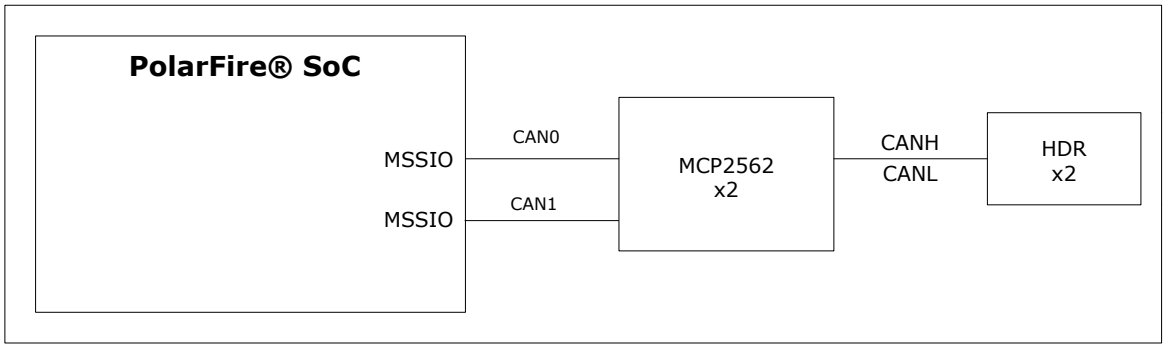


The video kit includes four UART ports. USB to four channel UART bridge.

3.10 Controller Area Network (CAN)

The following figure shows the CAN interface scheme.

Figure 3-12. CAN Interface



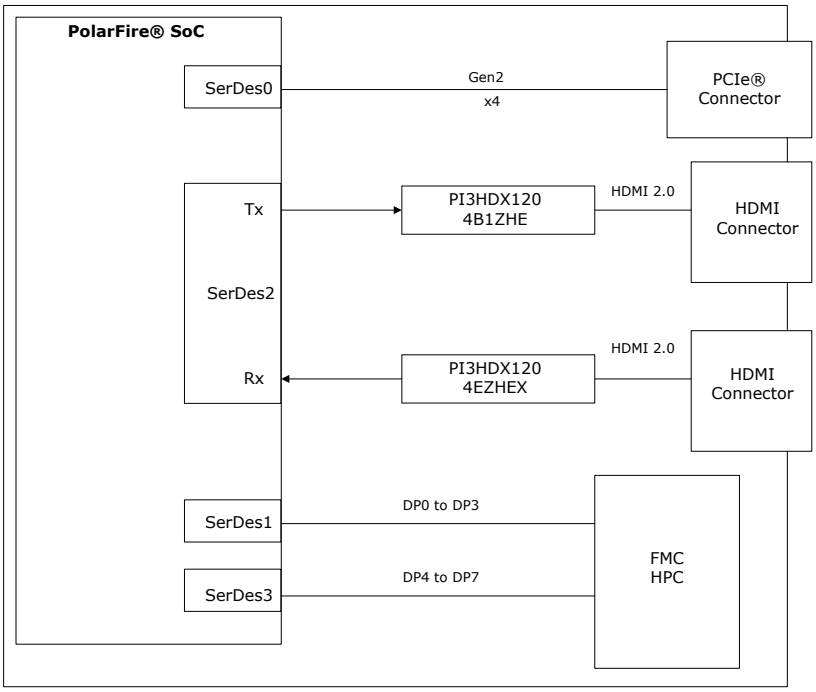
The video kit includes two CAN transceivers connected to two CAN controllers (CAN0, CAN1) integrated in the PolarFire SoC device.

CAN Transceiver Part Number:	MCP2562FDT-E/SN
Manufacturer:	Microchip
Connection:	100 mil pitch generic connectors are used on board.
Part Number:	61300311121

3.11 Transceivers

The PolarFire SoC MPFS250T-1FCG1152 device includes four SerDes blocks. The following figure shows the allocation of each SerDes block.

Figure 3-13. Transceiver Block Diagram



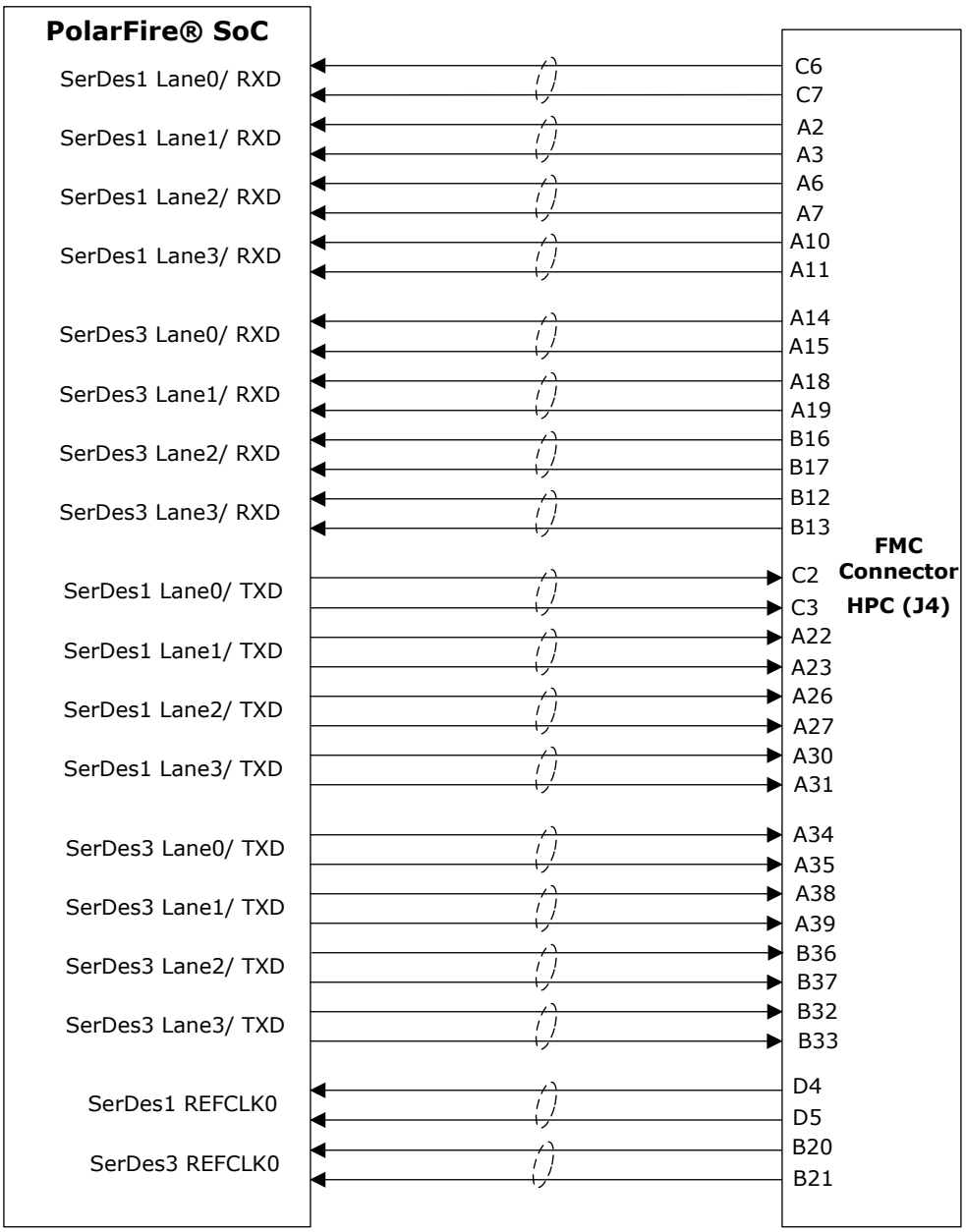
3.11.1 SerDes0

SerDes0 is allocated for PCIe x4 Gen2 in the Root port mode. x16 straddle mount connector is used on the board, which supports x4 SSD and graphic cards.

3.11.2 SerDes1 and SerDes3 Blocks

SerDes1 and SerDes3 blocks have four lanes each. These lanes are connected to the FMC HPC connector. The SerDes1 and SerDes3 reference clock is routed directly from the HPC connector to the PolarFire SoC device. The following figure shows the SerDes1 and SerDes3 interface.

Figure 3-14. SerDes1 and SerDes3 Interface

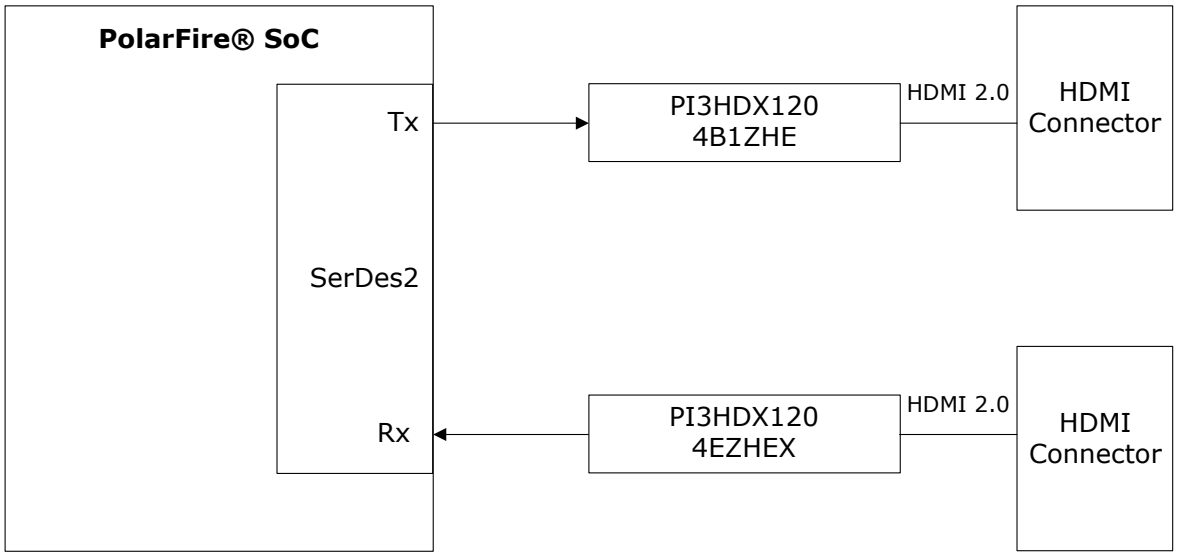


3.11.3 SerDes2 Block

The lanes of the SerDes2 block are connected to HDMI 2.0 TX and RX through the line driver chips.

The following figure shows the SerDes2 interface.

Figure 3-15. SerDes2 Interface

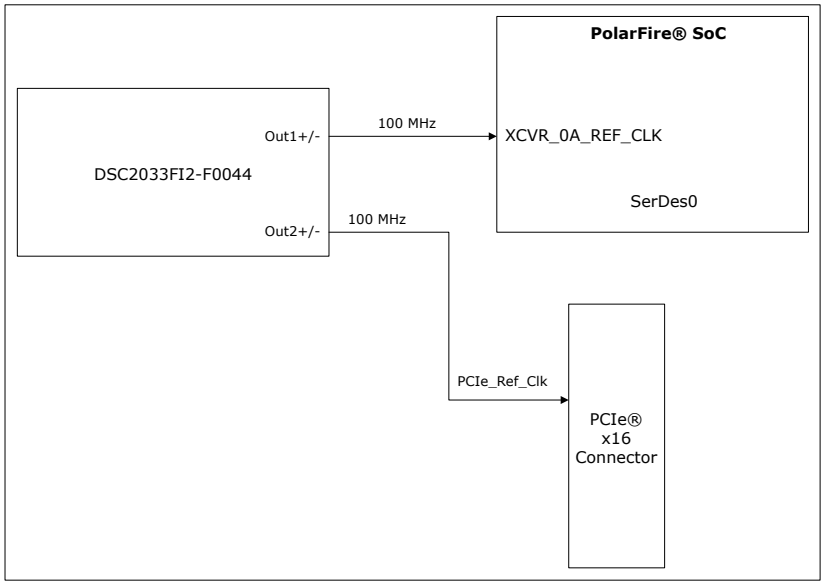


3.11.4 SerDes Reference Clock

SerDes0

The following figure shows the clock source for the SerDes0 block.

Figure 3-16. SerDes0 Clock Scheme

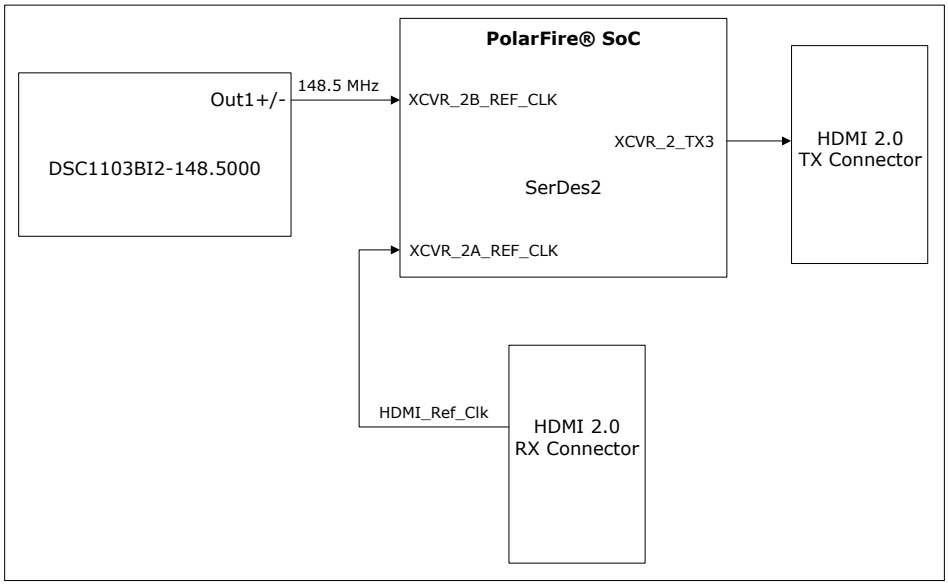


As shown in the preceding figure, a 100 MHz LVDS reference clock is provided to SerDes0 and PCIe end point over PCIe connector from the DSC2033FI2-F0044 oscillator.

SerDes2

The following figure shows the clock source for the SerDes2 block.

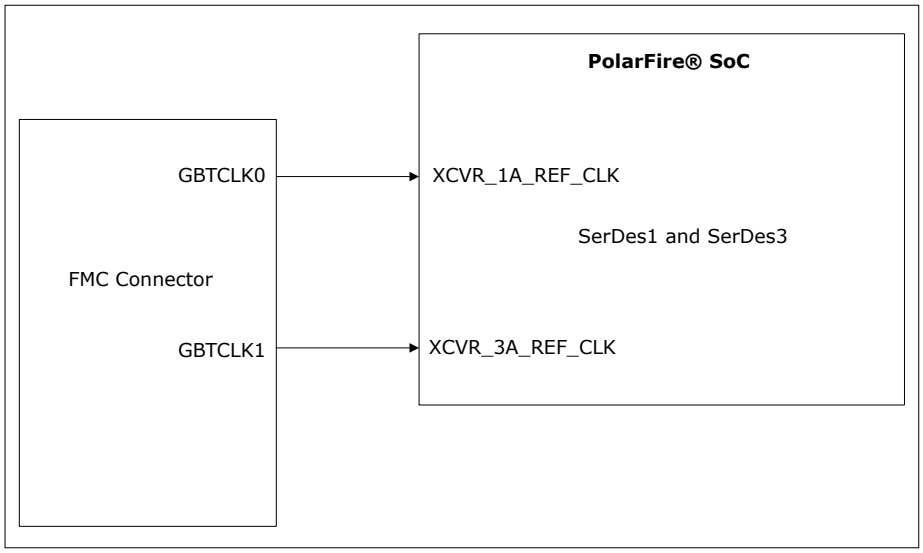
Figure 3-17. HDMI 2.0 Clock Scheme



FMC Clock Scheme

The following figure shows clock source for SerDes1 and SerDes3 from the FMC.

Figure 3-18. FMC Clock Scheme



3.12 Programming

The PolarFire SoC video kit supports the following programming schemes:

- **JTAG Programming**: In this scheme, the device is programmed via JTAG Bank3 I/Os by any of the following programmers:
  - On-board embedded FlashPro6 (eFP6), when J28 is closed.
  - External FashPro programmer (FlashPro4 and above) via JTAG header (J31), when J28 is open.

- **SPI Slave Programing**: In this scheme, the device is programmed using an external master via the SPI Connector (J24).
- **SPI Master Programming**: In this scheme, the device is programmed using the System Controller's SC_SPI interface available in the PolarFire SoC device.

3.13 50 MHz Oscillator

A 50 MHz clock oscillator with an accuracy of ±10 ppm is available on the board. This clock oscillator is connected to the FPGA fabric to provide a system reference clock. An on-chip PLL can be configured to generate a wide range of high-precision clock frequencies.

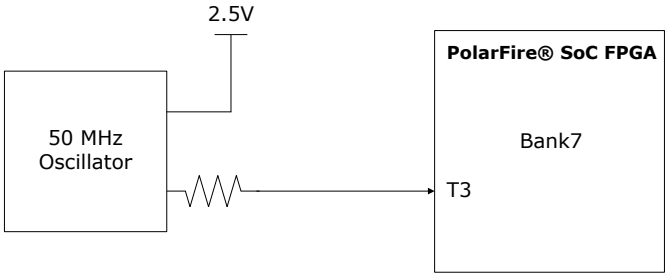
The pin details of the 50 MHz oscillator are listed in the following table.

Table 3-1. Pin Details

Pin Number	Pin Name
T3	GPIO143PB7/CLKIN_W_4/CCC_NW_CLKIN_W_4

The following figure shows the on-board 50 MHz oscillator's interface with PolarFire SoC.

Figure 3-19. 50 MHz Oscillator Interface



3.14 Device Reset

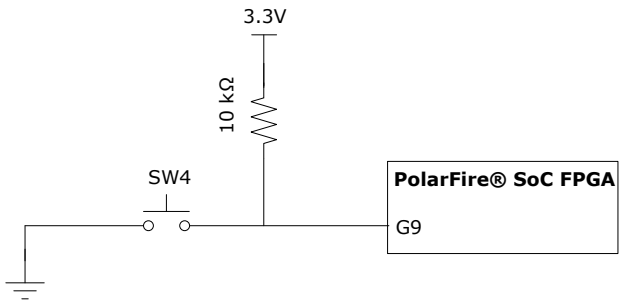
As shown in the following figure, DEVRST_N (SW4 push button) is an input-only reset switch that allows the assertion of a full reset of the chip at any time. The DEVRST_N signal is an active-low signal.

The pin details of the device reset are listed in the following table.

Table 3-2. Pin Details

Pin Number	Pin Name
G9	DEVRST_N

Figure 3-20. Device Reset



3.15 User Interface

LEDs and push-button switches are available on the board for the user interface.

3.15.1 User LEDs

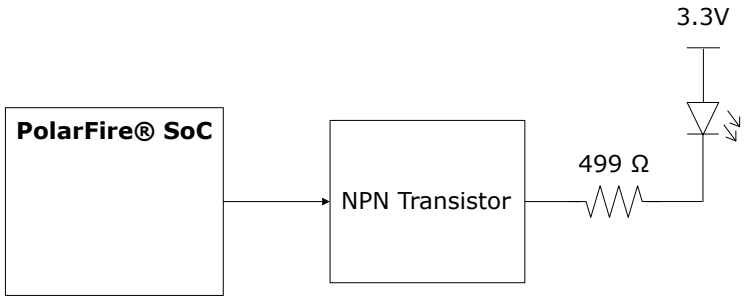
Four active-high LEDs are connected to the PolarFire SoC device. The following table lists the on-board label of these switches, the associated PolarFire SoC pin number, name, and Bank.

Table 3-3. User LEDs

Label On Board	PolarFire® SoC Pin Number	PolarFire SoC Pin Name	PolarFire SoC Bank
LED1	AE27	HSIO80PB0/CLKIN_N_6	Bank0
LED2	AE22	HSIO86PB0/CLKIN_N_4	Bank0
LED3	AP28	HSIO67PB0/CCC_NE_PLL0_OUT1	Bank0
LED4	AP29	HSIO67NB0	Bank0

The following figure shows how each user LED interfaces with the PolarFire SoC device.

Figure 3-21. User LED Interface



3.15.2 Push-Button Switches

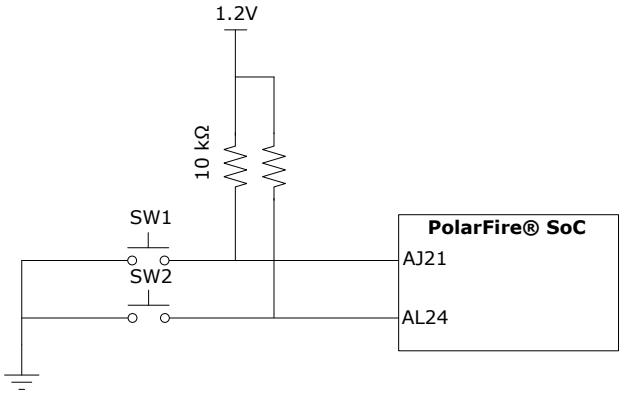
Two push-button tactile switches are connected to the PolarFire SoC device. The following table lists the on-board label of these switches, the associated PolarFire pin number, name, and Bank.

Table 3-4. Push-Button Switches

Label On Board	PolarFire® SoC Pin Number	PolarFire SoC Pin Name	PolarFire SoC Bank
SW1	AJ21	HSIO95PB0/CCC_NW_CLKIN_N_0	Bank0
SW2	AL24	HSIO74PB0/CLKIN_N_8/ CCC_NE_CLKIN_N_8/ CCC_NE_PLL1_OUT0	Bank0

The following figure shows how these push-button switches interface with the PolarFire SoC device.

Figure 3-22. Push-Button Interface



3.15.3 Slide Switches (DPDT)

The SW5 slide switch powers the device ON or OFF.

3.15.4 DIP Switches (SPST)

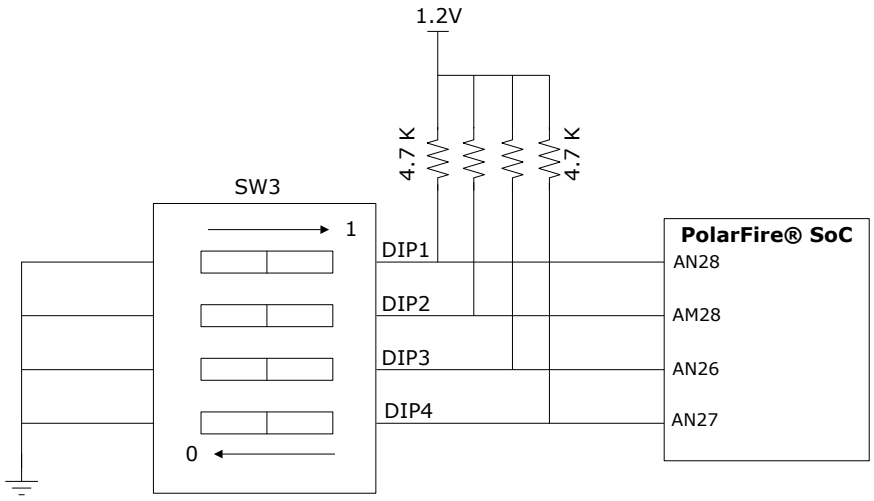
The SW6 DIP switch includes eight connections to the PolarFire device. The following table lists on-board label of these switches, the associated PolarFire SoC pin number, name, and Bank.

Table 3-5. DIP Switch

Label On Board	PolarFire® SoC Pin Number	PolarFire SoC Pin Name	PolarFire SoC Bank
DIP1	AN28	HSIO68PB0/CCC_NE_CLKIN_N_10/ CCC_NE_PLL0_OUT0	Bank0
DIP2	AM28	HSIO68NB0	Bank0
DIP3	AN26	HSIO69PB0/DQS/CCC_NE_PLL0_OUT0	Bank0
DIP4	AN27	HSIO69NB0/DQS	Bank0

The following figure shows how the DIP switch interfaces with the PolarFire SoC device.

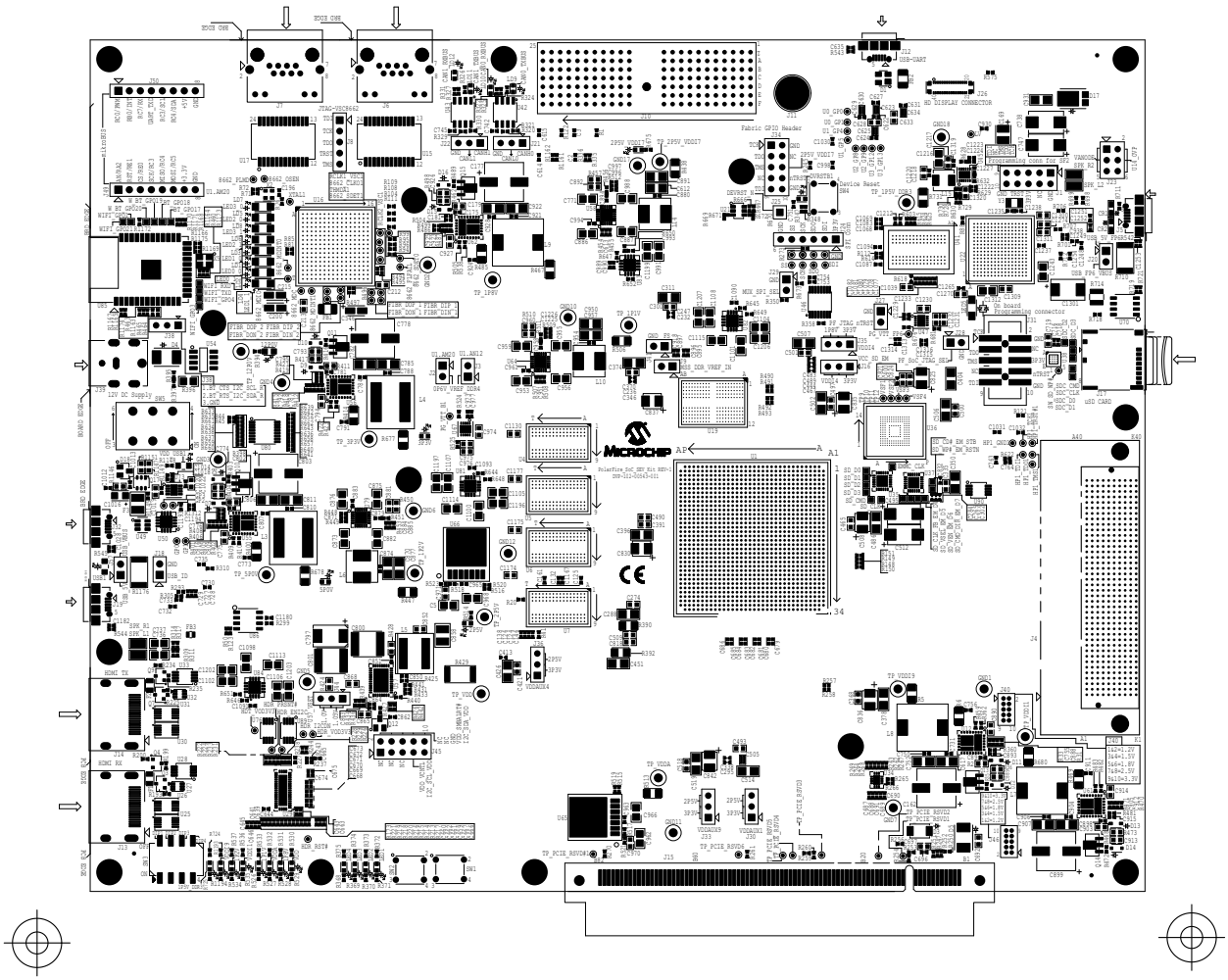
Figure 3-23. DIP Switch Interface



3.16 Board Components Placement

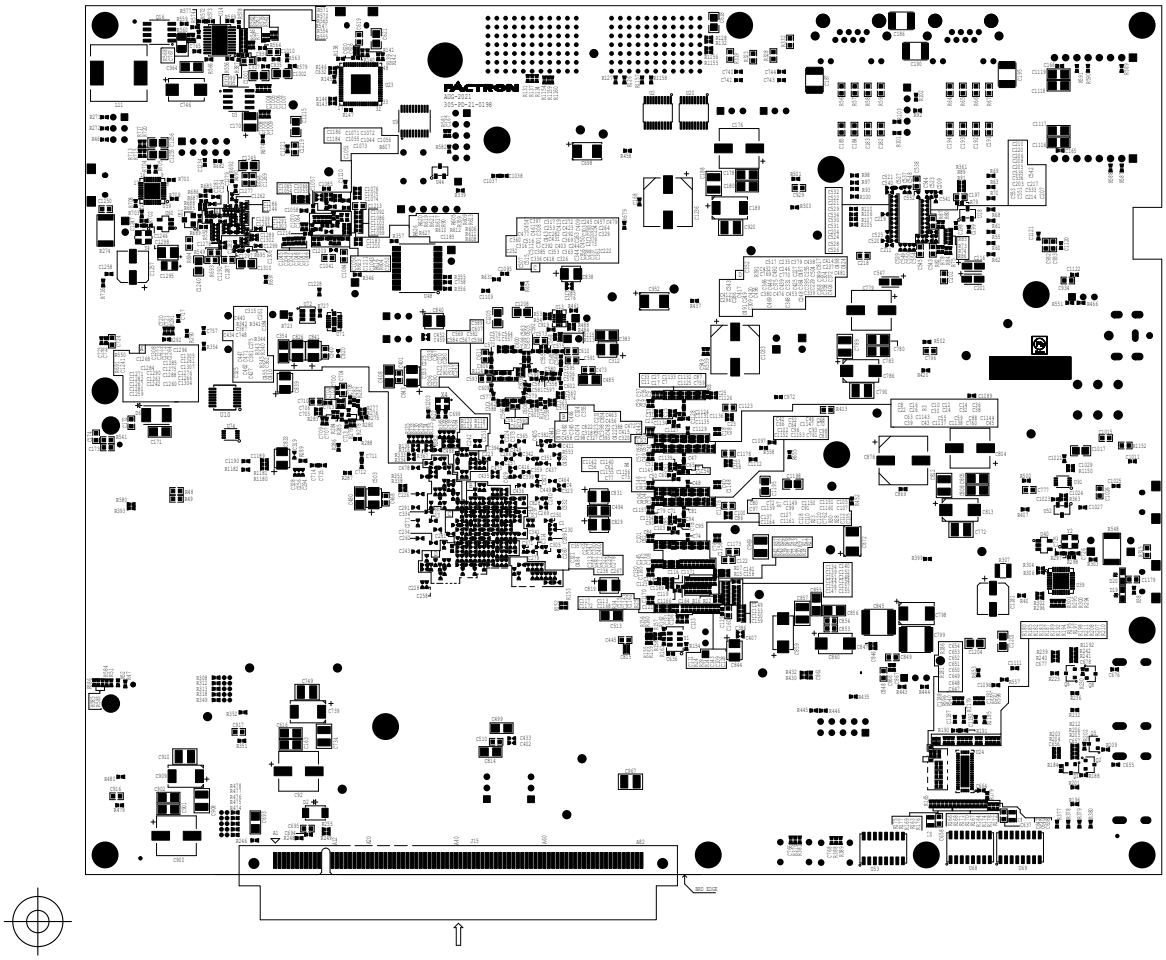
The following figure shows the top-view of the board components.

Figure 3-24. Silkscreen Top-View



The following figure shows the bottom view of the placement of board components.

Figure 3-25. Silkscreen Bottom-View



4. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
A	09/2022	Initial Revision

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