MPM3515

36V, 1.5A Module, Synchronous, Step-Down Converter with an Integrated Inductor AEC-Q100 Qualified

The Future of Analog IC Technology

DESCRIPTION

The MPM3515 is a synchronous, rectified, step-down converter with built-in power MOSFETs, inductors, and capacitors. The MPM3515 offers a very compact solution and requires only four external components to achieve 1.5A of continuous output current with excellent load and line regulation over a wide input supply range. The MPM3515 operates with a 2.2MHz switching frequency to achieve a fast load transient response.

Full protection features include over-current protection (OCP) and thermal shutdown.

The MPM3515 eliminates design and manufacturing risks while improving the time to market dramatically.

The MPM3515 is available in a space-saving QFN-17 (3mmx5mmx1.6mm) package.

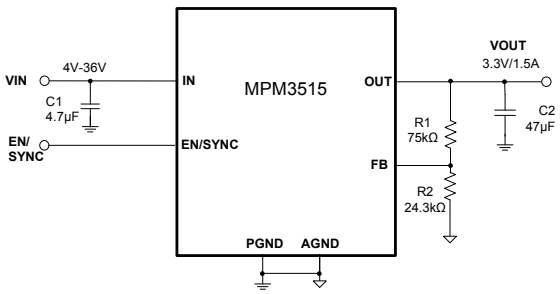
FEATURES

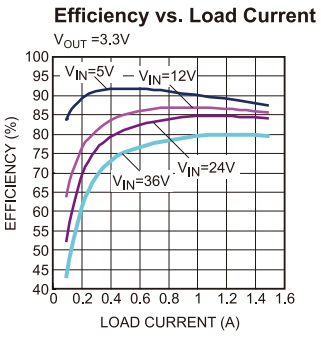
- Complete Switch-Mode Power Supply
- Wide 4V to 36V Operating Input Range
- 1.5A Continuous Load Current
- 90mΩ/50mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- Fixed 2.2MHz Switching Frequency
- Frequency Foldback at a High Input Voltage
- 450kHz to 2.2MHz Frequency Sync
- Forced Continuous Conduction Mode (CCM)
- Power Good (PG) Indicator
- Over-Current Protection (OCP) with Valley-Current Detection and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in a QFN-17 (3mmx5mmx1.6mm) Package
- CISPR25 Class 5 Compliant
- Available in a Wettable Flank Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Industrial Controls
- Automotive
- Medical and Imaging Equipment
- Telecom Applications
- Distributed Power Systems

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating***
MPM3515GQV*	QFN-17 (3mmx5mmx1.6mm)	*See Below*	3
MPM3515GQV-AEC1			
MPM3515GQVE-AEC1**			

* For Tape & Reel, add suffix –Z (e.g. MPM3515GQV–Z)
** Wettable flank
*** Moisture Sensitivity Level Rating

TOP MARKING (MPM3515GQV & MPM3515GQV-AEC1)

MPYW
3515
LLL
M

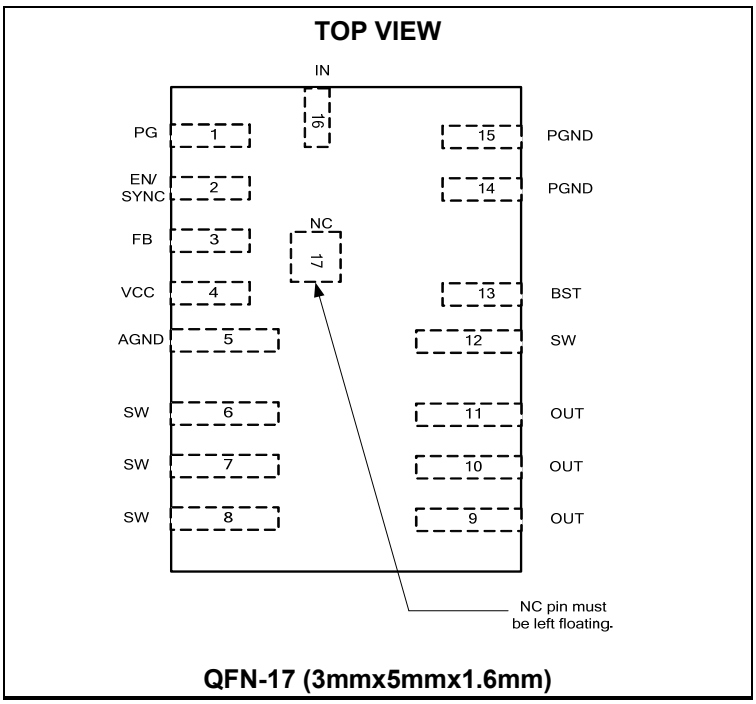
MP: MPS prefix
Y: Year code
W: Week code
3515: First four digits of the part number
LLL: Lot number
M: Module

TOP MARKING (MPM3515GQVE-AEC1)

MPYW
3515
LLL
EM

MP: MPS prefix:
Y: Year code;
W: Week code:
3515: First four digits of the part number;
LLL: Lot number;
E: Wettable lead flank
M: Module

PACKAGE REFERENCE



QFN-17 (3mmx5mmx1.6mm)

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to 40V
V_{SW}, V_{OUT} ..... -0.3V to V_{IN} + 0.3V
V_{BST} ..... V_{SW} + 6V
All other pins ..... -0.3V to 6V (2)
Continuous power dissipation (T_A = +25°C) (3) 2.7W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to 150°C

Electrostatic Discharge (ESD rating)

HBM (Human Body Model) ..... ±2kV
CDM (Charged Device Model) ..... ±750V

Recommended Operating Conditions

Supply voltage (V_{IN}) ..... 4V to 36V
Output voltage (V_{OUT}) ..... 0.8V to V_{IN}*D_{Max}
Operating junction temp. (T_J) .... -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}
QFN-17 (3mmx5mmx1.6mm)	46	10 ... °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) For details on EN/SYNC's ABS MAX rating, please refer to the EN/SYNC section on page 13.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_J = +25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	$V_{EN/SYNC}$ = 0V			8	μA
Supply current (quiescent)	I_q	$V_{EN/SYNC}$ = 2V , V_{FB} = 1V, no switching		0.6	0.8	mA
HS switch on resistance	$HS_{RDS(ON)}$	V_{BST-SW} = 5V		90	155	mΩ
LS switch on resistance	$LS_{RDS(ON)}$	V_{CC} = 5V		50	105	mΩ
Inductor DC resistance	L_{DCR}			75		mΩ
Switch leakage	SW_{LKG}	$V_{EN/SYNC}$ = 0V, V_{SW} = 12V			1	μA
Current limit (5)	I_{LIMIT}	20% duty cycle	2.4	4.0	5.5	A
Low-side valley current limit			1.5	2.5	3.5	A
Reverse current limit				1.2		A
Oscillator frequency	f_{SW}	V_{FB} = 700mV	1800	2200	2600	kHz
Foldback frequency during soft start (5)	f_{FB}	V_{FB} = 200mV		0.2		f_{SW}
Maximum duty cycle	D_{MAX}	V_{FB} = 700mV		85		%
Minimum on time (5)	T_{ON_MIN}			40		ns
Feedback voltage	V_{FB}	T_A = 25°C	795	807	819	mV
		T_A = -40°C to 125°C	790	807	824	mV
Feedback current	I_{FB}	V_{FB} = 820mV		10	50	nA
EN/SYNC rising threshold	V_{EN_RISING}		1.2	1.45	1.7	V
EN/SYNC falling threshold	$V_{EN\_FALLING}$		0.8	1	1.3	V
EN/SYNC input current	I_{EN}	$V_{EN/SYNC}$ = 2V		5	10	μA
EN/SYNC turn off delay	EN_{Td_off}			3		μs
EN/SYNC frequency range			450		2200	kHz
V_{IN} under-voltage lockout threshold rising	$INUV_{Vth}$		3	3.5	3.8	V
V_{IN} under-voltage lockout threshold hysteresis	$INUV_{HYS}$			330		mV
PG rising threshold	PG_{Vth_Hi}		0.83	0.88	0.93	V_{FB}
PG falling threshold	PG_{Vth_Lo}		0.78	0.83	0.88	V_{FB}
PG rising delay	PG_{TD_RISING}		40	90	160	μs
PG falling delay	$PG_{TD\_FALLING}$		30	55	95	μs
PG sink current capability	V_{PG}	Sink 4mA			0.4	V
PG leakage current	I_{PG_LEAK}				100	nA
VCC regulator	V_{CC}		4.5	4.8	5.1	V
VCC load regulation		I_{CC} = 5mA		1.5	4	%
Soft-start time	t_{SS}	V_{OUT} from 10% to 90%	0.5	1.7	3	ms
Thermal shutdown (5)				170		°C
Thermal hysteresis (5)				20		°C

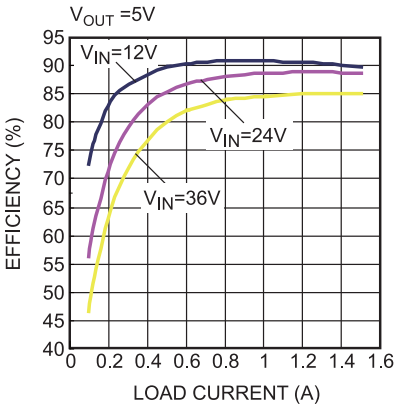
NOTE:

5) Not tested in production and guaranteed by over-temperature correlation.

TYPICAL PERFORMANCE CHARACTERISTICS

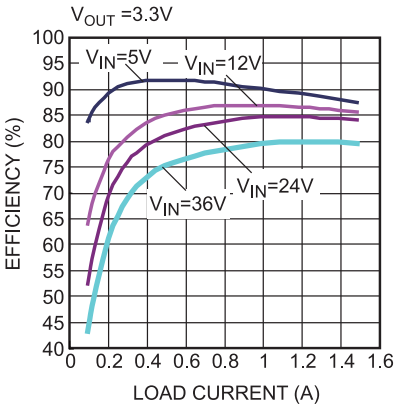
Efficiency vs. Load Current

V_{OUT} =5V



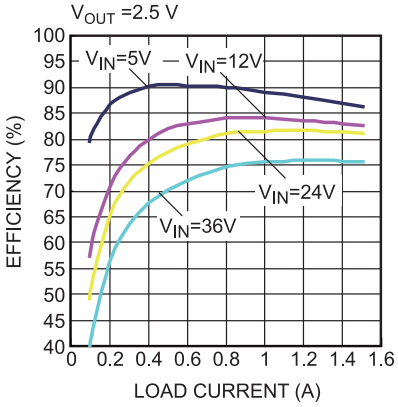
Efficiency vs. Load Current

V_{OUT} =3.3V



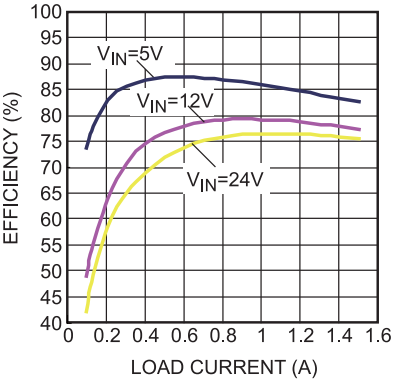
Efficiency vs. Load Current

V_{OUT} =2.5 V



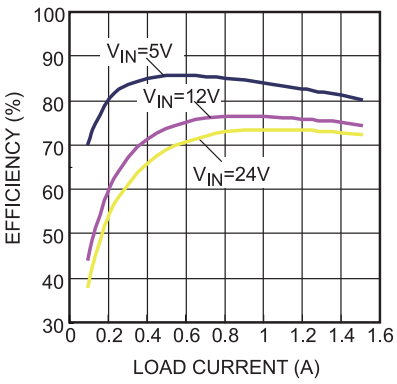
Efficiency vs. Load Current

V_{OUT} =1.8V



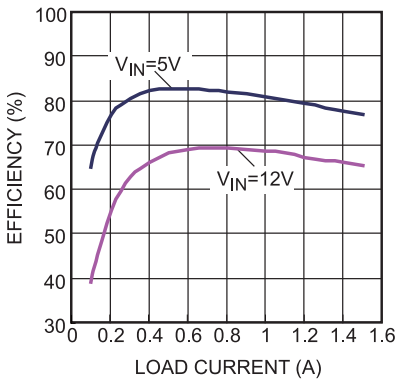
Efficiency vs. Load Current

V_{OUT} =1.5V



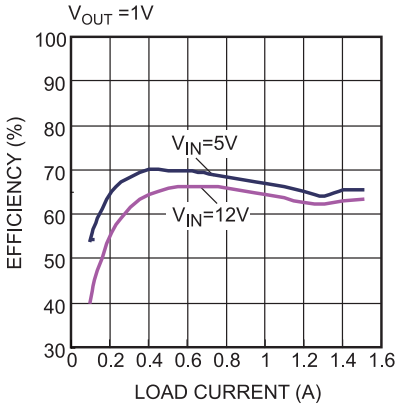
Efficiency vs. Load Current

V_{OUT} =1.2V

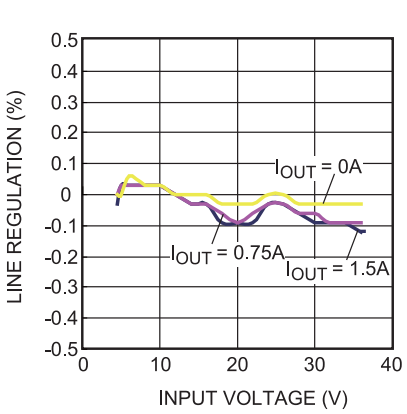


Efficiency vs. Load Current

V_{OUT} =1V

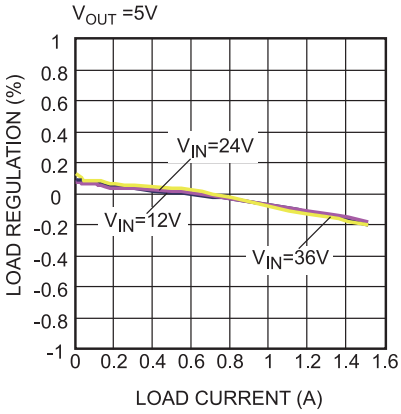


Line Regulation



Load Regulation

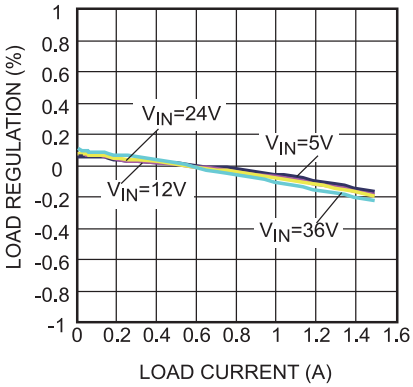
V_{OUT} =5V



TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

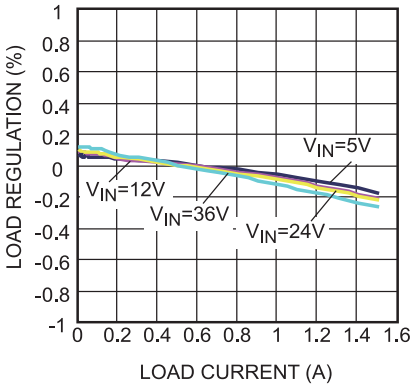
Load Regulation

V_{OUT} =3.3V



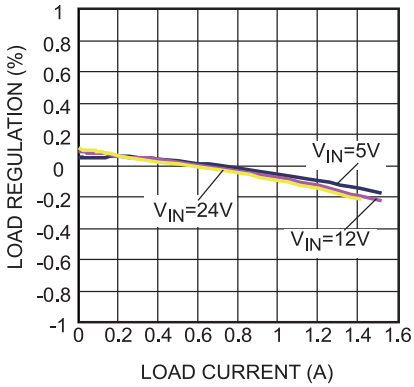
Load Regulation

V_{OUT} =2.5V



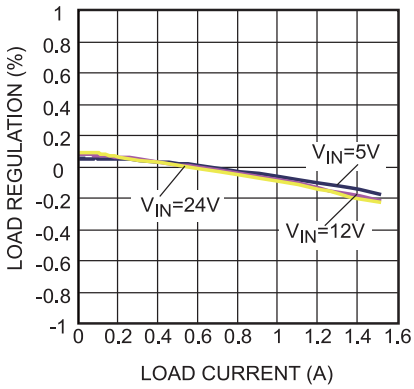
Load Regulation

V_{OUT} =1.8V



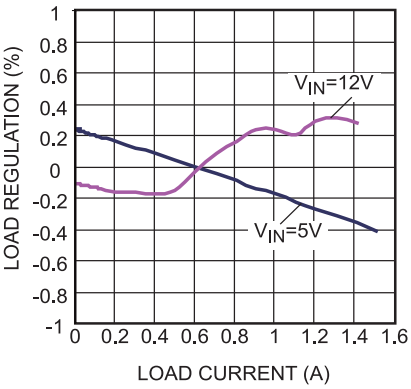
Load Regulation

V_{OUT} =1.5V



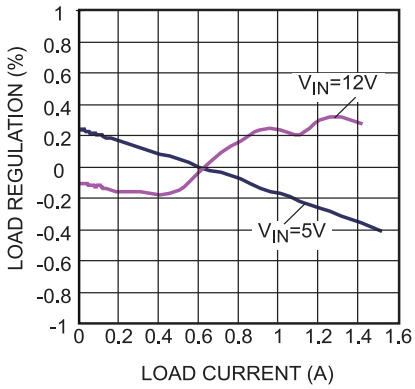
Load Regulation

V_{OUT} =1.2V

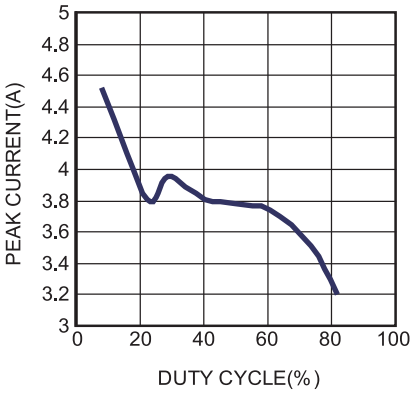


Load Regulation

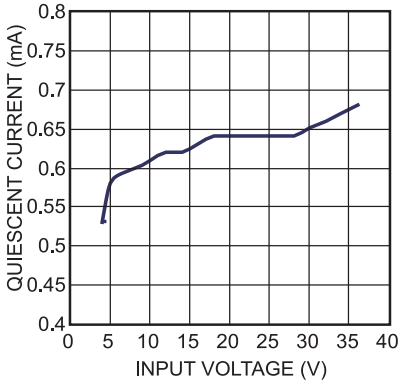
V_{OUT} =1V



Peak Current vs. Duty Cycle

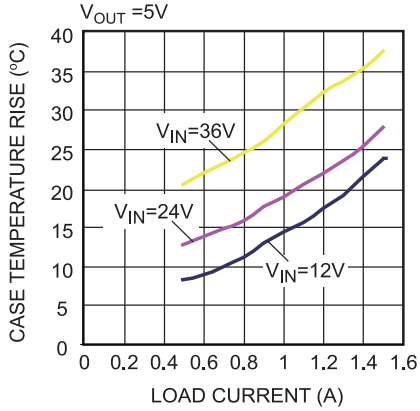


Quiescent Current vs. Input Voltage



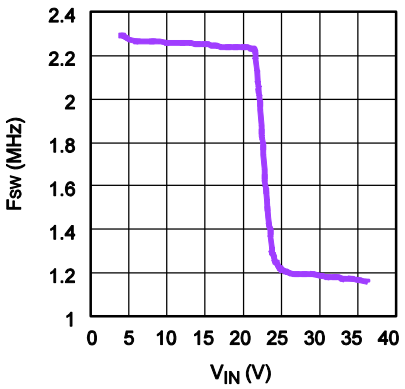
Case Temperature Rise vs. Output Current

V_{OUT} =5V

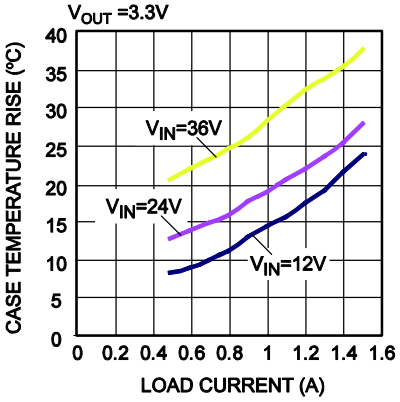


TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

Frequency vs.V_{IN}



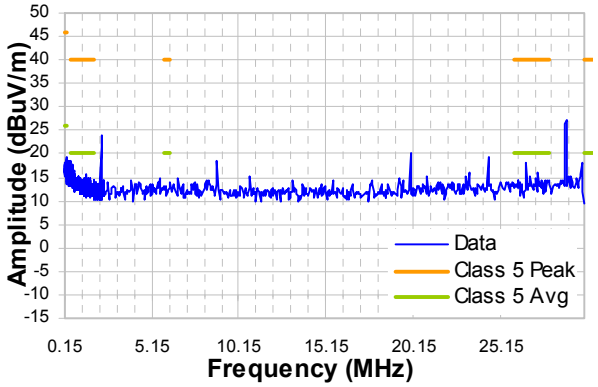
Case Temperature Rise vs. Output Current



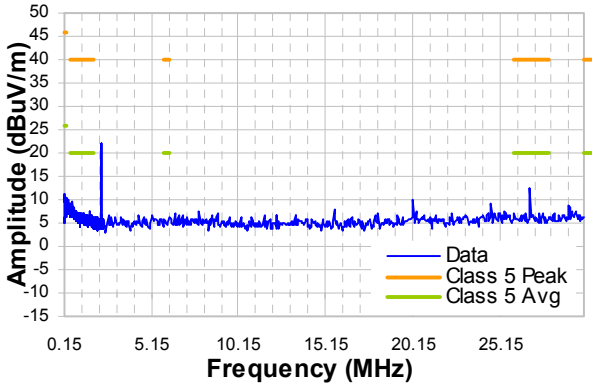
TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

V_{IN} = 12V, V_{out} = 3.3V, I_{OUT} = 1.5A, L = 2.2µH, F_{SW} = 2.2MHz, with EMI filters, T_A = +25°C, unless otherwise noted.(6)

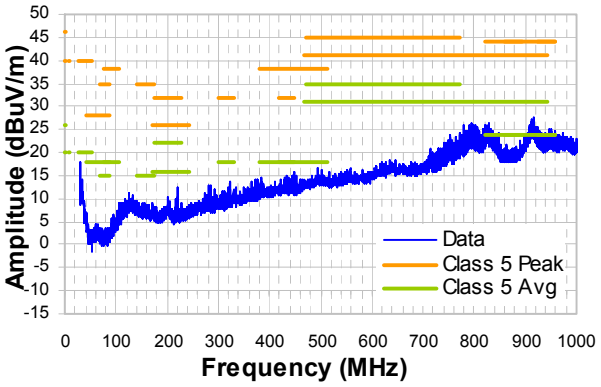
CISPR25 Class 5 Peak Radiated Emissions (150kHz - 30MHz)



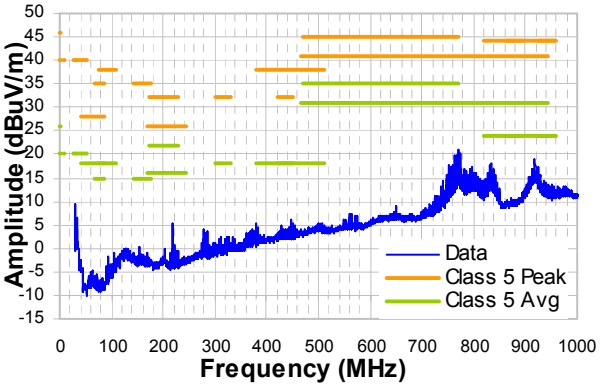
CISPR25 Class 5 Average Radiated Emissions (150kHz - 30MHz)



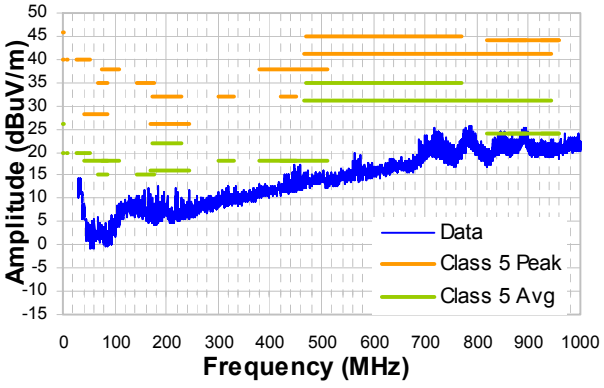
CISPR25 Class 5 Peak Radiated Emissions (Vertical, 30MHz - 1GHz)



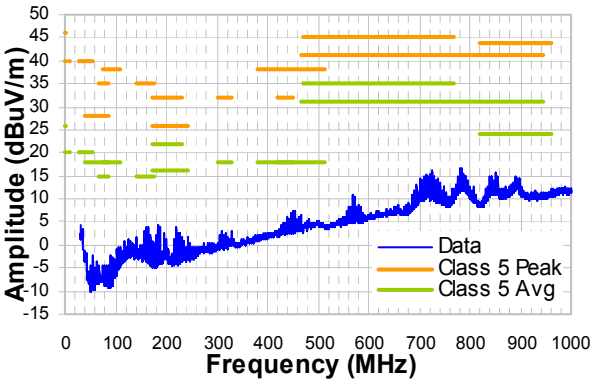
CISPR25 Class 5 Average Radiated Emissions (Vertical, 30MHz - 1GHz)



CISPR25 Class 5 Peak Radiated Emissions (Horizontal, 30MHz - 1GHz)



CISPR25 Class 5 Average Radiated Emissions (Horizontal, 30MHz - 1GHz)

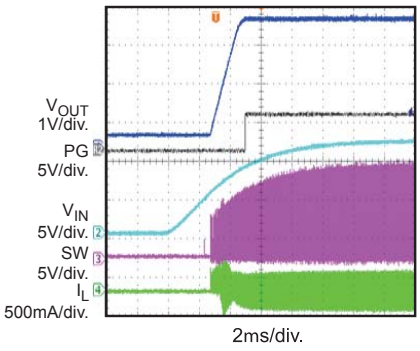


NOTE:

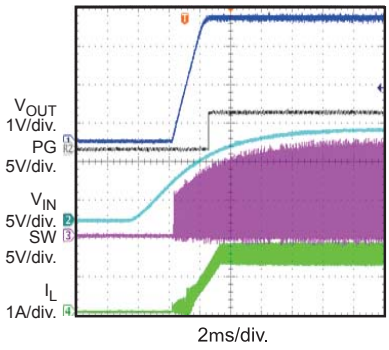
6) The EMC test results are based on the application circuit with EMI filters (see Figure 12).

TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

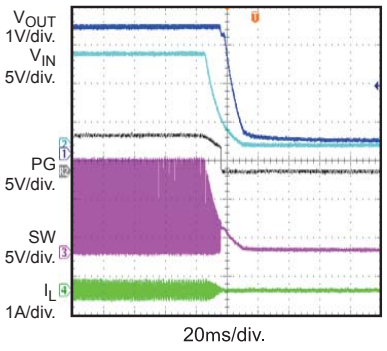
Start-Up through Input Voltage
I_{OUT}=0A



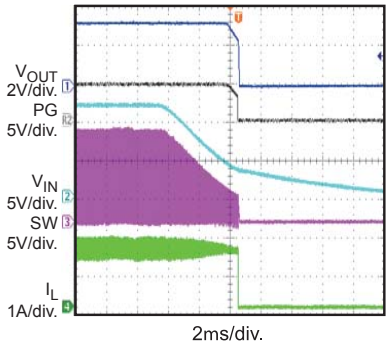
Start-Up through Input Voltage
I_{OUT}=1.5A



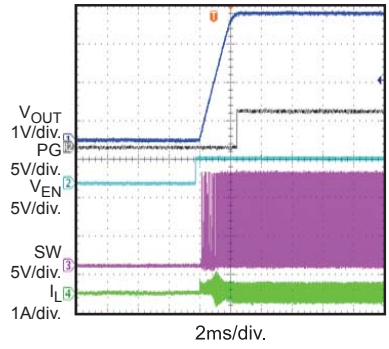
Shutdown through Input Voltage
I_{OUT} = 0A



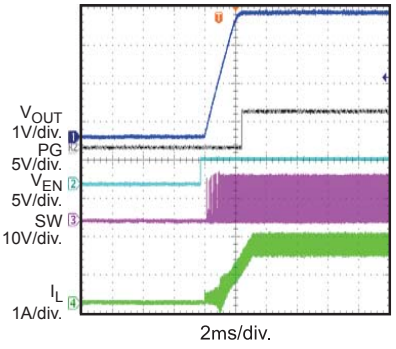
Shutdown through Input Voltage
I_{OUT}=1.5A



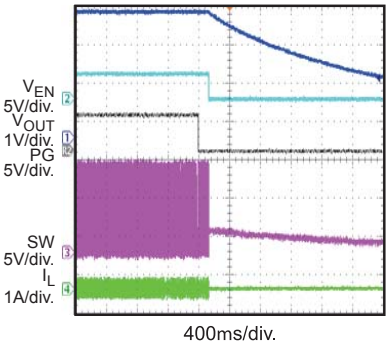
Start-Up through EN/SYNC
I_{OUT} = 0A



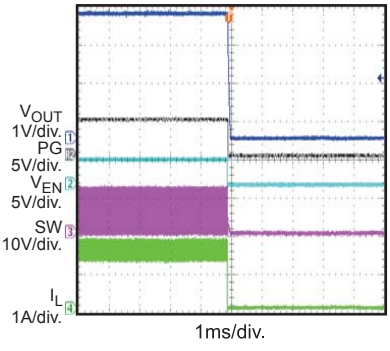
Start-Up through EN/SYNC
I_{OUT}=1.5A



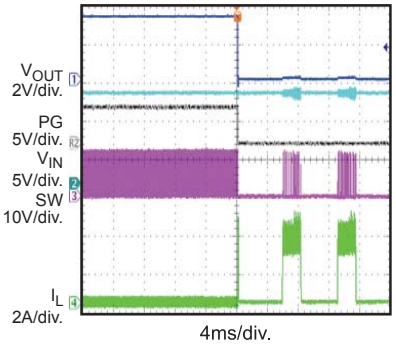
Shutdown through EN/SYNC
I_{OUT} = 0A



Shutdown through EN/SYNC
I_{OUT} = 1.5A

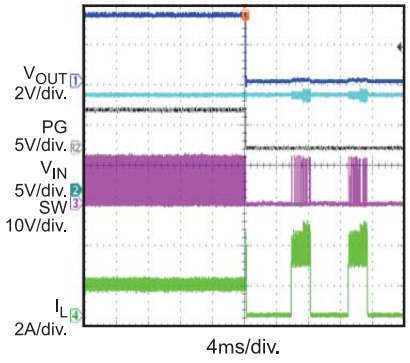


SCP Entry
I_{OUT} = 0A

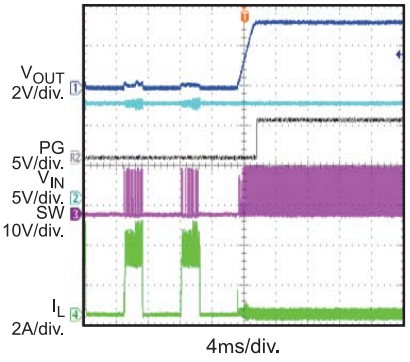


TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

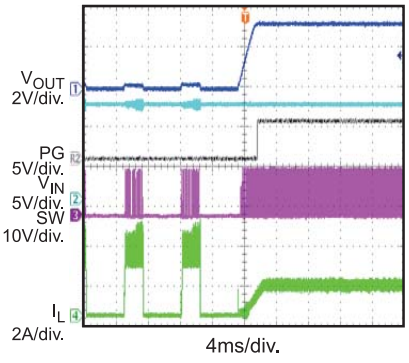
SCP Entry
I_{OUT} = 1.5A



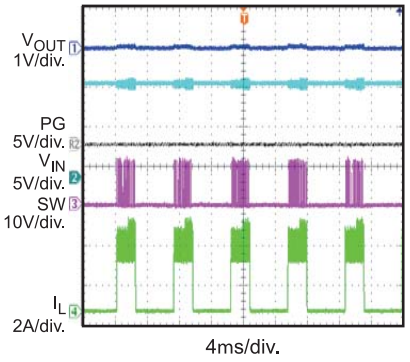
SCP Recovery
I_{OUT} = 0A



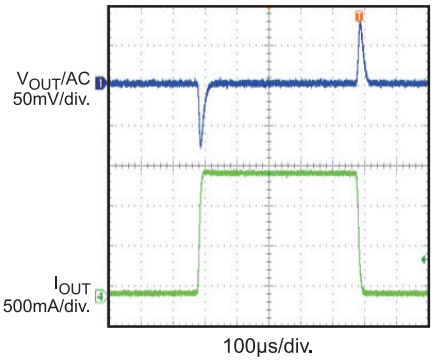
SCP Recovery
I_{OUT} = 1.5A



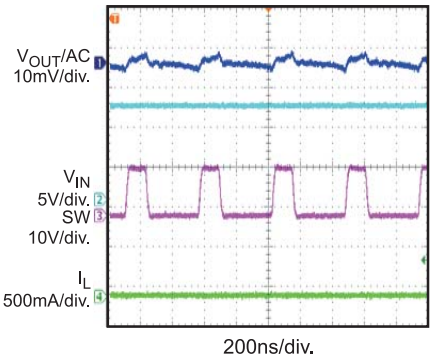
SCP Steady State
I_{OUT} = 0A



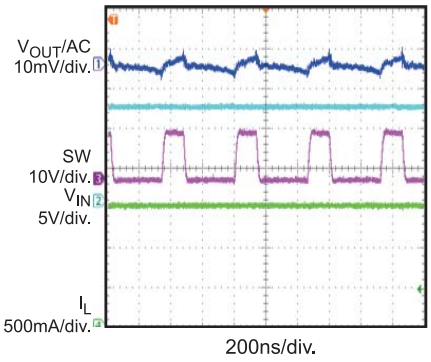
Load Transient
I_{OUT} = 0A-1.5A



Output Ripple
I_{OUT} = 0A



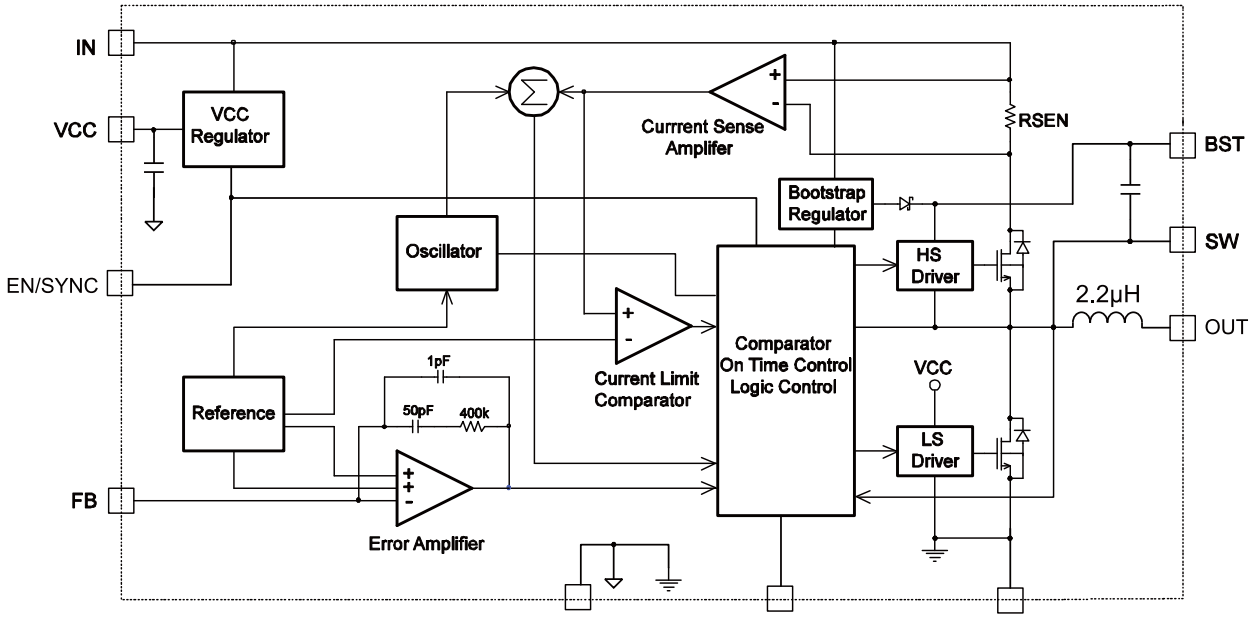
Output Ripple
I_{OUT} = 1.5A



PIN FUNCTIONS

Package Pin #	Name	Description
1	PG	**Power good indicator.** PG is an open-drain structure.
2	EN/SYNC	**Enable/sync.** Pull EN/SYNC high to enable the MPM3515. Float EN/SYNC or connect EN/SYNC to ground to disable the MPM3515. Apply an external clock to EN/SYNC to change the switching frequency.
3	FB	**Feedback.** Connect FB to the tap of an external resistor divider from the output to AGND to set the output voltage. The frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 400mV to prevent current-limit runaway during a short-circuit fault. Place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces.
4	VCC	**Internal 4.8V LDO output.** Since an internal circuit integrates the LDO output capacitor, there is no need to add an external capacitor.
5	AGND	**Analog ground.** Reference ground of the logic circuit. AGND is connected to PGND internally. There is no need to add external connections to PGND.
6, 7, 8, 12	SW	**Switch output.** There is no need to connect these SW pins, but a large copper plane is recommended on pins 6, 7, and 8 for better heat sinking.
9, 10, 11	OUT	**Power output.** Connect the load to OUT. An output capacitor is required.
13,	BST	**Bootstrap.** The bootstrap capacitor is integrated internally. There is no need for external connections.
14,15	PGND	**Power ground.** PGND is the reference ground of the power device and requires careful consideration during PCB layout. For best results, connect PGND with copper pours and vias.
16	IN	**Supply voltage.** IN supplies power for the internal MOSFET and regulator. The MPM3515 operates from a +4V to +36V input rail. A low-ESR and low-inductance capacitor is required to decouple the input rail. Place the input capacitor very close to IN and connect it with wide PCB traces and multiple vias.
17	NC	**Do not connect.** NC must be left floating.

BLOCK DIAGRAM



OPERATION

The MPM3515 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs, an integrated inductor, and two capacitors. The MPM3515 offers a very compact solution that achieves 1.5A of continuous output current with excellent load and line regulation over a 4V to 36V input supply range.

The MPM3515 operates in a fixed-frequency, peak-current-control mode to regulate the output voltage. An internal clock initiates a PWM cycle. The integrated high-side power MOSFET (HS-FET) turns on and remains on until the current reaches the value set by the COMP voltage (V_{COMP}). When the power switch is off, it remains off until the next clock cycle begins. If the current in the power MOSFET does not reach the value set by V_{COMP} within 85% of one PWM period, the power MOSFET is forced off.

Internal Regulator

A 4.8V internal regulator powers most of the internal circuitries. This regulator takes V_{IN} and operates in the full V_{IN} range. When V_{IN} is higher than 4.8V, the output of the regulator is in full regulation. When V_{IN} is lower than 4.8V, the output decreases. The MPM3515 integrates an internal decoupling capacitor, so there is no need to add an external VCC output capacitor.

CCM Operation

The MPM3515 uses continuous conduction mode (CCM) to ensure that the part works with a fixed frequency from a no-load to a full-load range. The advantage of CCM is the controllable frequency and lower output ripple at light load.

Frequency Foldback

The MPM3515 enters frequency foldback when the input voltage is higher than about 21V. The frequency decreases to half the nominal value and changes to 1.1MHz. Frequency foldback also occurs during soft start and short-circuit protection.

Error Amplifier (EA)

The error amplifier compares the FB voltage to the internal 0.807V reference (V_{REF}) and outputs a current proportional to the difference between the two. This output current then charges or discharges the internal compensation network to form V_{COMP}, which controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 3.5V, while its falling threshold is 3.17V.

Enable/SYNC

EN/SYNC is a control pin that turns the regulator on and off. Drive EN/SYNC high to turn on the regulator; drive EN/SYNC low to turn off the regulator. An internal 500kΩ resistor from EN/SYNC to GND allows EN/SYNC to be floated to shut down the chip.

EN/SYNC is clamped internally using a 6.5V series Zener diode (see Figure 2). Connecting the EN/SYNC input through a pull-up resistor to the voltage on V_{IN} limits the EN/SYNC input current below 100μA. For example, with 12V connected to V_{IN}, R_{PULLUP} ≥ (12V - 6.5V) ÷ 100μA = 55kΩ.

Connecting EN/SYNC to a voltage source directly without a pull-up resistor requires limiting the amplitude of the voltage source to ≤6V to prevent damage to the Zener diode.

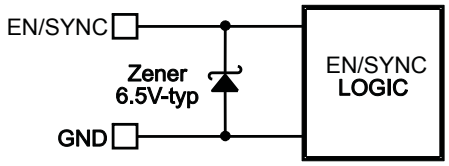


Figure 2: 6.5V Zener Diode Connection

Connect an external clock with a range of 450kHz to 2.2MHz to synchronize the internal clock rising edge to the external clock rising edge. The pulse wide of the external clock

signal should be below 350ns, and the off time of external clock signal should be below 1.9µs.

Internal Soft Start (SS)

The soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start (SS) voltage that ramps up from 0V to 4.8V. When SS is lower than REF, the error amplifier uses SS as the reference. When SS is higher than REF, the error amplifier uses REF as the reference. The SS time is set to 1.7ms internally.

Over-Current Protection (OCP) and Hiccup

The MPM3515 has cycle-by-cycle peak-current-limit protection and valley-current detection protection. The inductor current is monitored during the HS-FET on-state. If the inductor current exceeds the current-limit value set by the COMP high-clamp voltage, the HS-FET turns off immediately. The low-side MOSFET (LS-FET) then turns on to discharge the energy, and the inductor current decreases. The HS-FET remains off unless the inductor valley current is lower than a certain current threshold (the valley current limit), even though the internal clock pulses high. If the inductor current does not drop below the valley current limit when the internal clock pulses high, the HS-FET misses the clock, and the switching frequency decreases to half the nominal value. Both the peak and valley current limits assist in keeping the inductor current from running away during an overload or short-circuit condition.

If the output voltage drops below the under-voltage (UV) threshold (typically 50% below the reference), the MPM3515 enters hiccup mode to restart the part periodically. Simultaneously, the peak-current limit is reached.

This protection mode is useful when the output is dead-shorted to ground and reduces the average short-circuit current greatly to alleviate thermal issues and protect the regulator. The MPM3515 exits hiccup mode once the over-current condition is removed.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the die temperatures exceed 170°C, the device stops switching. When the temperature drops below its lower threshold (typically 150°C), the power supply resumes operation.

Floating Driver and Bootstrap Charging

An internal bootstrap capacitor powers the floating power MOSFET driver. A dedicated internal regulator charges and regulates the bootstrap capacitor voltage to ~4.8V (see Figure 3). When the voltage between the BST and SW nodes drops below the regulation voltage, a PMOS pass transistor connected from V_{IN} to BST turns on. The charging current path is from V_{IN} to BST to SW. The external circuit should provide enough voltage headroom to facilitate charging. As long as V_{IN} is higher than SW significantly, the bootstrap capacitor remains charged. When the HS-FET is on, $V_{IN} \approx V_{SW}$, so the bootstrap capacitor cannot charge. When the LS-FET is on, V_{IN} - V_{SW} reaches its maximum for fast charging. When there is no inductor current, V_{SW} is equal to V_{OUT}, so the difference between V_{IN} and V_{OUT} can charge the bootstrap capacitor. The floating driver has its own UVLO protection with a rising threshold of 2.2V and hysteresis of 150mV.

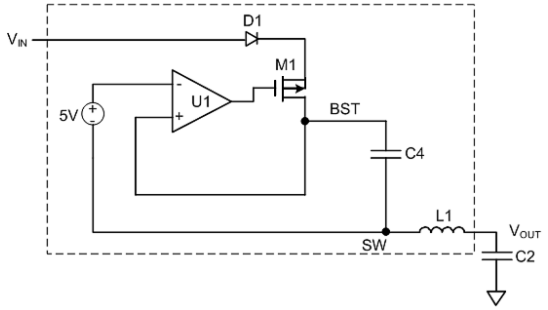


Figure 3: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If V_{IN} exceeds its thresholds, the MPM3515 starts up. The reference block starts first, generating a stable reference voltage and current. The internal regulator is then enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: V_{IN} low, EN/SYNC low, and thermal shutdown. During the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (see the Typical Application on page 1). The feedback resistor (R1) sets the feedback loop bandwidth with the internal compensation capacitor. Choose R1 to be around 75kΩ when $V_{OUT} \geq 1V$. R2 can then be calculated with Equation (1):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.807V} - 1} \quad (1)$$

Figure 4 shows the feedback network.

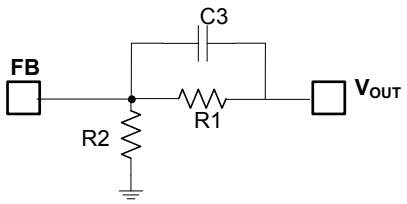


Figure 4: Feedback Network

Table 1 lists recommended resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.5	75	87
1.8	75	61
2.5	75	35.7
3.3	75	24.3
5	75	14.3

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, use a 4.7µF capacitor.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (2):

$$I_{C1} = I_{LOAD} x \sqrt{\frac{V_{OUT}}{V_{IN}} x \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (2)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (3):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (3)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g.: 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (4):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S x C1} x \frac{V_{OUT}}{V_{IN}} x \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (4)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (5):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S x L_1} x \left(1 - \frac{V_{OUT}}{V_{IN}}\right) x \left(R_{ESR} + \frac{1}{8 x f_S x C2}\right) \quad (5)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple.

For simplification, the output voltage ripple can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{1}{8xf_S{}^2xL_1xC2}x\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S xL_1}x\left(1-\frac{V_{OUT}}{V_{IN}}\right)xR_{ESR} \quad (7)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPM3515 can be optimized for a wide range of capacitance and ESR values.

External Bootstrap Diode

An external bootstrap diode can enhance the efficiency of the regulator given the following conditions:

- V_{OUT} is 5V or 3.3V
- Duty cycle is high: $D = \frac{V_{OUT}}{V_{IN}} > 65\%$

In these cases, add an external BST diode from VCC to BST (see Figure 5).

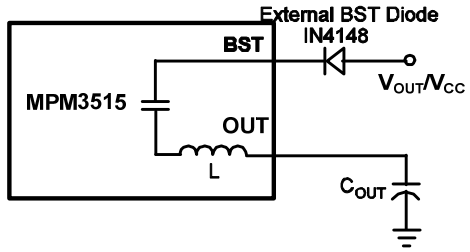


Figure 5: Optional External Bootstrap Diode Added to Enhance Efficiency

The recommended external BST diode is IN4148.

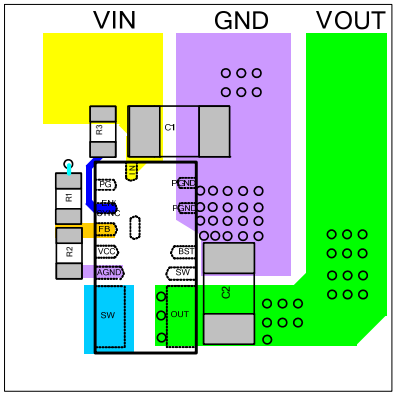
PCB Layout Guidelines [7]

Efficient PCB layout, especially of the input capacitor placement, is critical for stable operation. For best results, refer to Figure 6 and follow the guidelines below.

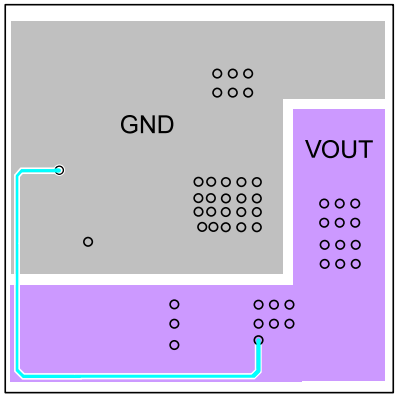
1. Connect a large ground plane to PGND directly. If the bottom layer is a ground plane, add vias near PGND.
2. Ensure that the high-current paths at GND and IN have short, direct, and wide traces.
3. Place the ceramic input capacitor close to IN and PGND.
4. Keep the connection of the input capacitor and IN as short and wide as possible.
5. Place the external feedback resistors next to FB.
6. Keep the feedback network away from the switching node.

NOTE:

7) The recommended layout is based on Figure 8.



Top Layer



Bottom Layer

Figure 6: Recommended PCB Layout

Design Example

Table 2 is a design example following the application guidelines for the specifications below.

Table 2: Design Example

V_{IN}	12V
V_{OUT}	3.3V
I_{OUT}	1.5A

The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheet.

TYPICAL APPLICATION CIRCUITS

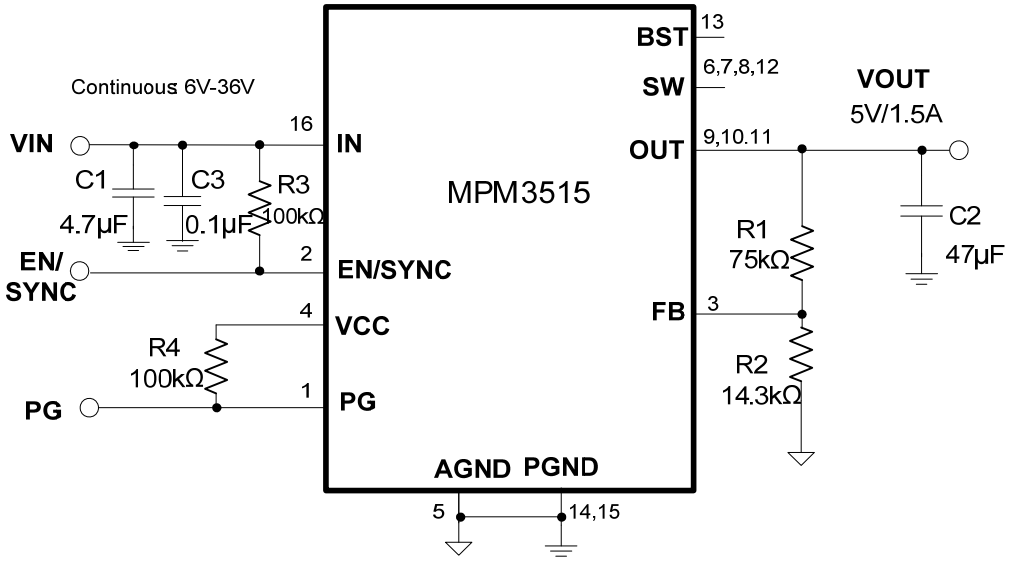


Figure 7: V_{OUT} = 5V, I_{OUT} = 1.5A

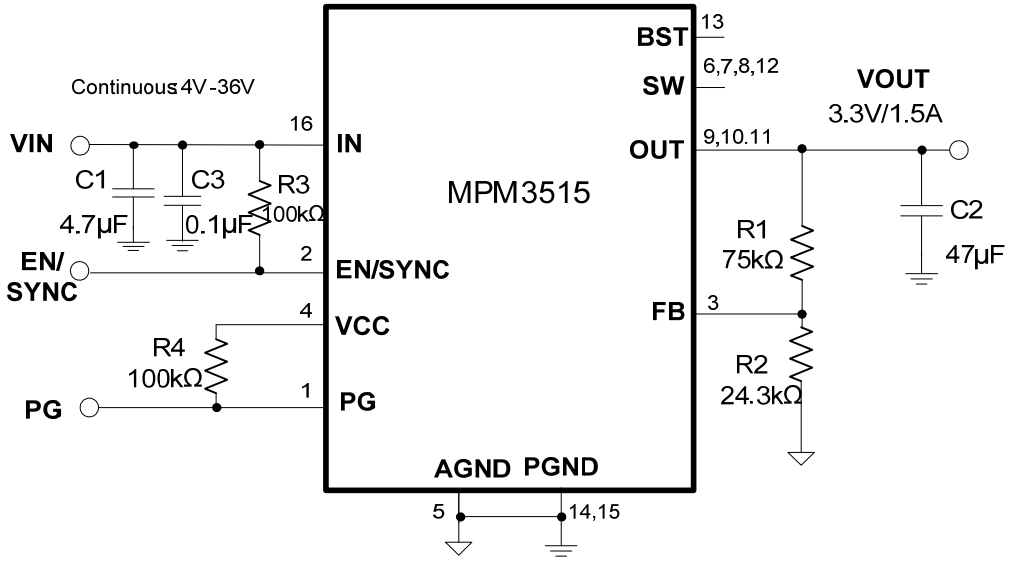


Figure 8: V_{OUT} = 3.3V, I_{OUT} = 1.5A

TYPICAL APPLICATION CIRCUITS *(continued)*

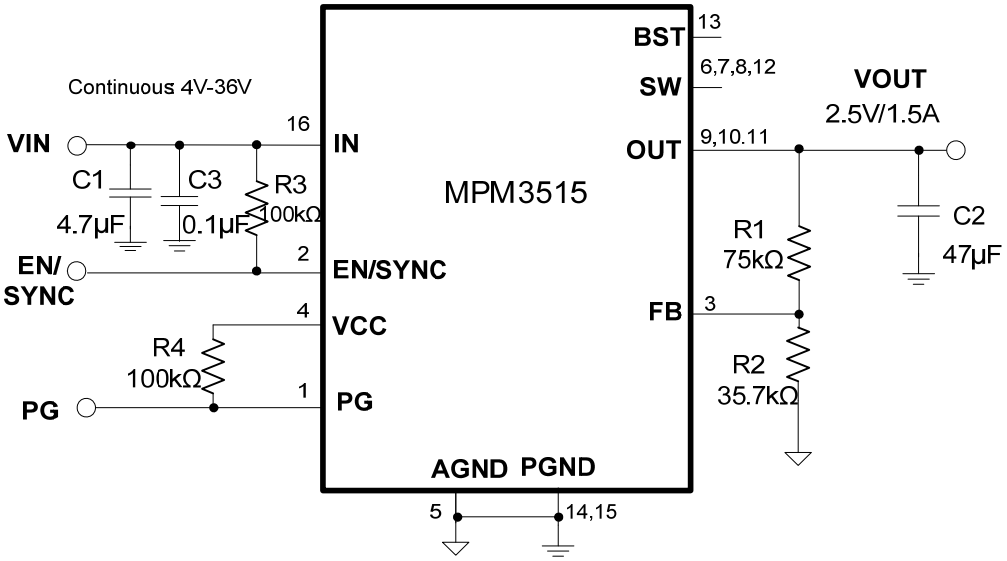


Figure 9: V_{OUT} = 2.5V, I_{OUT} = 1.5A

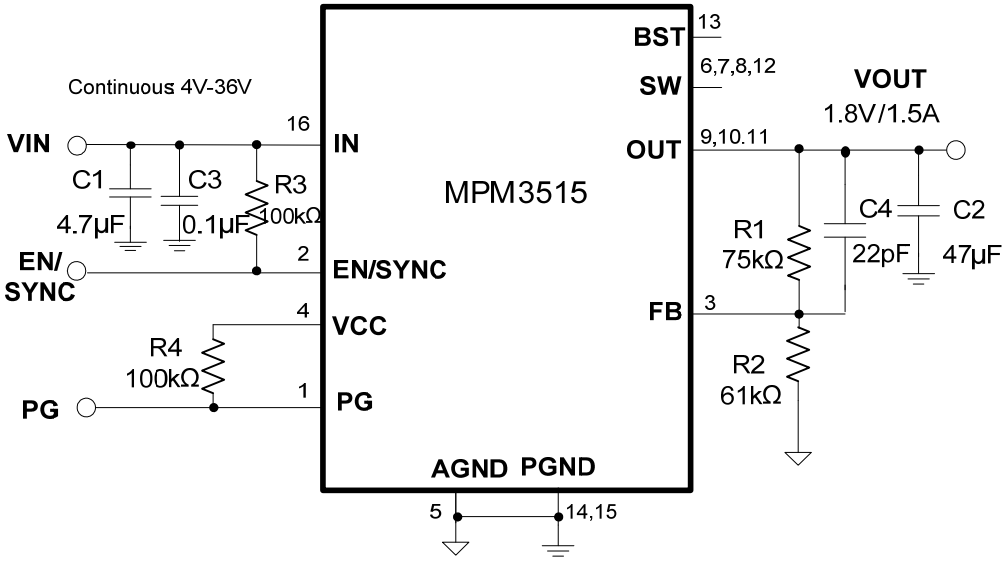


Figure 10: V_{OUT} = 1.8V, I_{OUT} = 1.5A

TYPICAL APPLICATION CIRCUITS *(continued)*

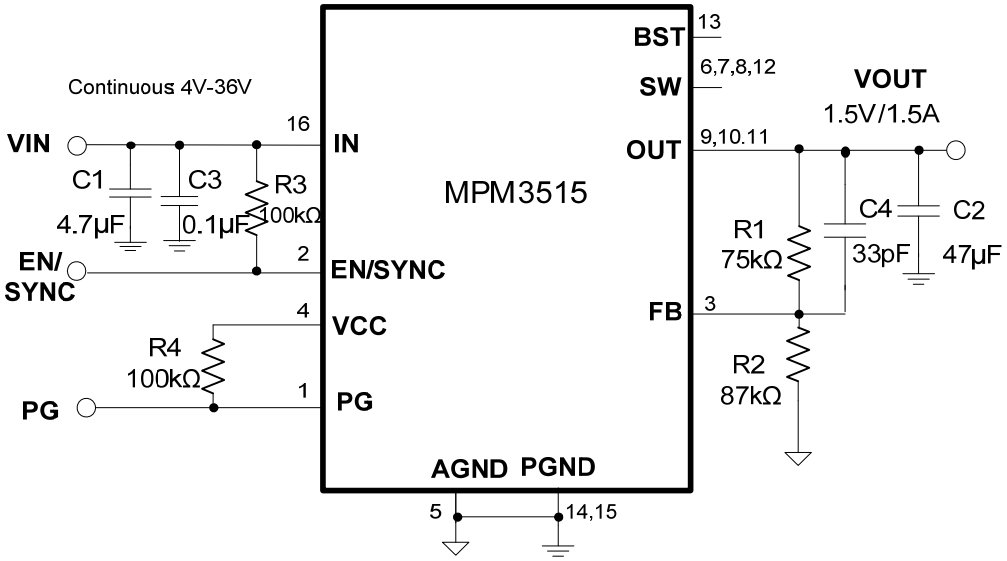


Figure 11: V_{OUT} = 1.5V, I_{OUT} = 1.5A

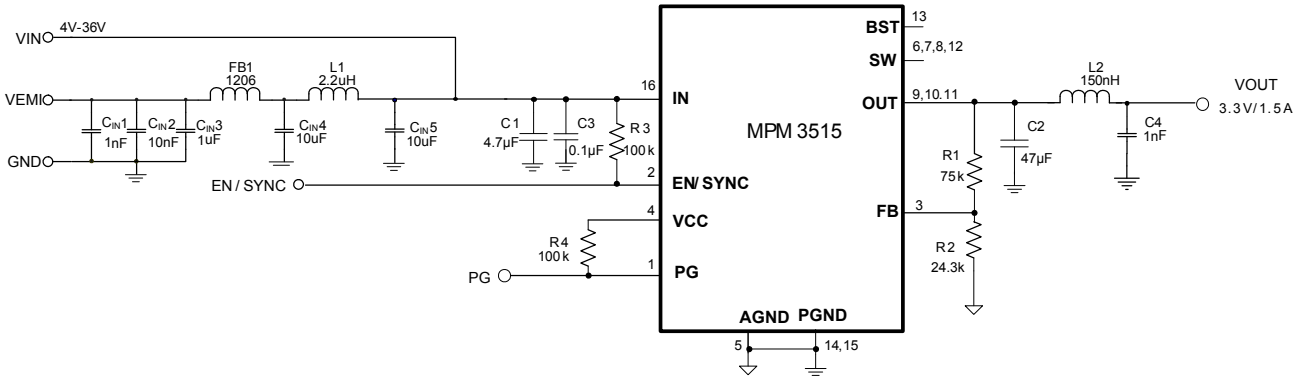
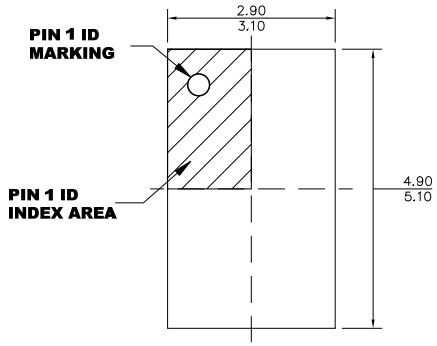


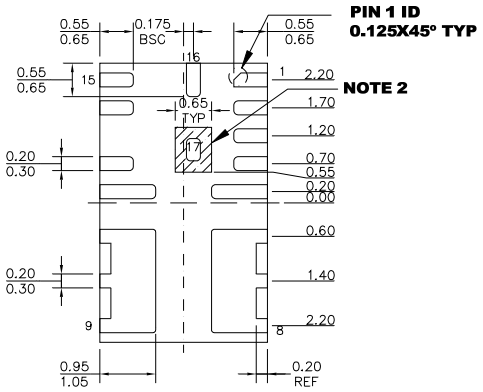
Figure 12: V_{OUT} = 3.3V, I_{OUT} = 1.5A with EMI Filter

PACKAGE INFORMATION

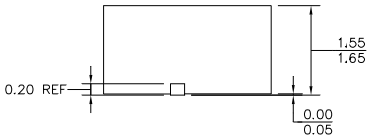
QFN-17 (3mmx5mmx1.6mm)
Non-Wettable Flank



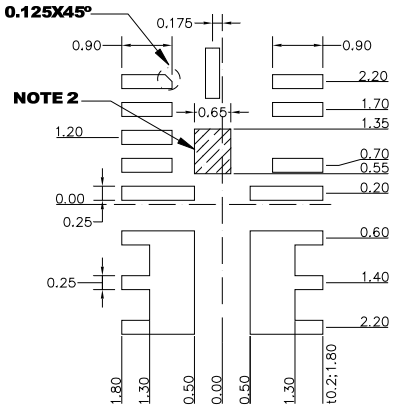
TOP VIEW



BOTTOM VIEW



SIDE VIEW



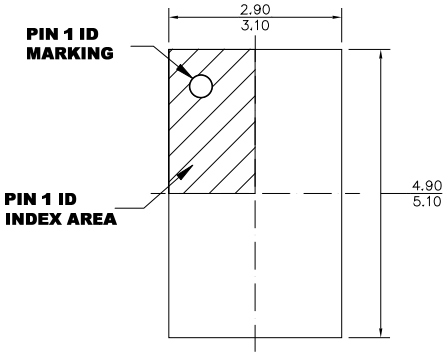
RECOMMENDED LAND PATTERN

NOTE:

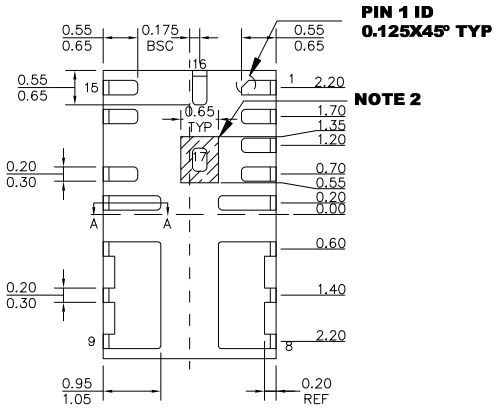
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) SHADED AREA IS THE KEEP-OUT ZONE. ANY PCB METAL TRACE AND VIA ARE NOT ALLOWED TO CONNECT TO THIS AREA ELECTRICALLY OR MECHANICALLY.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(CONTINUED)*

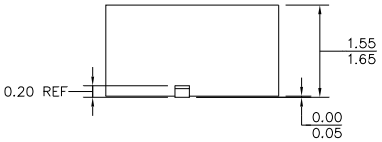
QFN-17 (3mmx5mmx1.6mm)
Wettable Flank



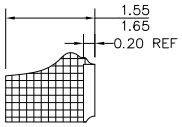
TOP VIEW



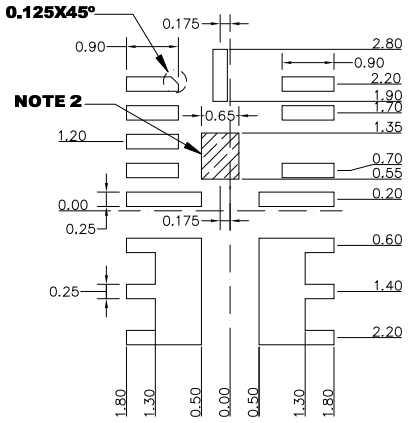
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) SHADED AREA IS THE KEEP-OUT ZONE. ANY PCB METAL TRACE AND VIA ARE NOT ALLOWED TO CONNECT TO THIS AREA ELECTRICALLY OR MECHANICALLY.
3) THE LEAD SIDE IS WETTABLE.
4) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.