



### DESCRIPTION

The MPM3808 is an easy-to-use, fully integrated, synchronous step-down power module with a built-in inductor and power MOSFETs. It can achieve up to 3A of continuous output current ( $I_{OUT}$ ), with excellent load and line regulation.

The constant-on-time (COT) control scheme provides fast transient response and eases loop stabilization. Fault protections include cycle-by-cycle current limiting and thermal shutdown. An open-drain power good (PG) signal indicates that the output voltage ( $V_{OUT}$ ) exceeds 90% of its nominal voltage.

The MPM3808 is ideal for a wide range of applications, including high-performance digital signal processors (DSPs), advanced driver-assistance system (ADAS) sensors, portable and mobile devices, and other low-power systems with constrained area.

The MPM3808 requires a minimal number of readily available, standard external components, and is available in a small QFN-15 (3mmx4mmx1.6mm) package.

### FEATURES

- **Designed for Automotive Applications:**
  - Wide 2.5V to 5.5V Operating  $V_{IN}$  Range
  - Up to 3A  $I_{OUT}$
  - 1% Feedback (FB) Accuracy
  - -40°C to +150°C Operating  $T_J$  Range
  - Available in AEC-Q100 Grade 1
- **Increased Battery Life:**
  - 21 $\mu$ A Sleep Mode  $I_Q$
  - AAM Mode for Increased Efficiency under Light-Load Conditions
- **High Performance for Improved Thermals:**
  - 65m $\Omega$  and 35m $\Omega$  Integrated Internal Power MOSFETs
- **Optimized for EMC and EMI:**
  - 2.4MHz  $f_{SW}$
  - MeshConnect™ Flip-Chip Package
- **Optimized for Board Size and BOM:**
  - Integrated Internal Power MOSFETs
  - Integrated Compensation Network
  - Available in a QFN-15 (3mmx4mmx1.6mm) Package
  - Fixed Output Options <sup>(1)</sup>: 0.8V, 1V, 1.1V, 1.2V, 1.25V, 1.5V, 1.8V, 2.5V, 2.8V, and 3.3V
- **Additional Features:**
  - Enable (EN) for Power Sequencing
  - Power Good (PG)
  - 100% Duty Cycle
  - External Soft Start (SS) Control
  - Output Discharge
  - OVP and SCP with Hiccup Mode
  - Available in a Wettable Flank Package

### APPLICATIONS

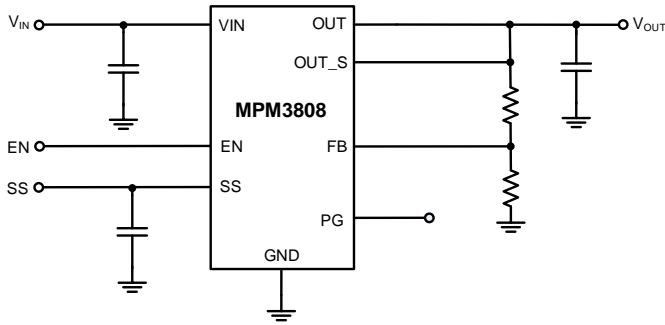
- Camera Modules
- ADAS Sensors
- Automotive Infotainment
- Automotive V2X

#### Note:

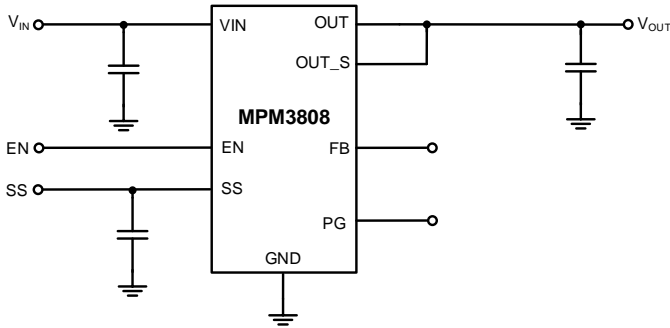
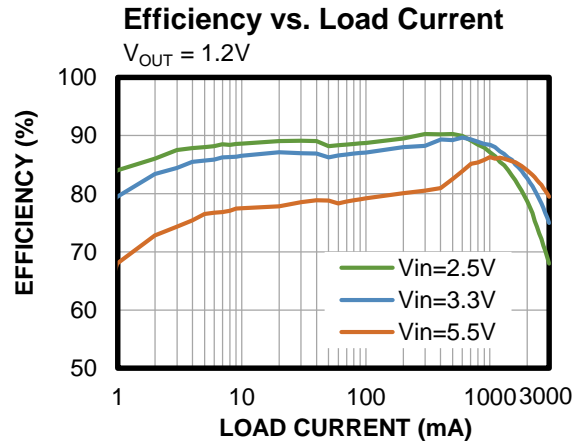
1) See the Ordering Information section on page 3 for the availability of each fixed output version. Contact MPS for details on additional output voltages that may be available.

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS", the MPS logo, and "Simple, Easy Solutions" are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

## TYPICAL APPLICATION



Typical Application (Adjustable Output)



Typical Application (Fixed Output)

### ORDERING INFORMATION

Part Number* (2)	Output Voltage	Package	Top Marking	MSL Rating**
MPM3808GLE-AEC1***	Adjustable	QFN-15 (3mmx4mmx1.6mm)	See Below	1
MPM3808GLE-12-AEC1***	Fixed 1.2V	QFN-15 (3mmx4mmx1.6mm)	See Below	1
MPM3808GLE-18-AEC1***	Fixed 1.8V	QFN-15 (3mmx4mmx1.6mm)	See Below	1

\* For Tape & Reel, add suffix -Z (e.g. MPM3808CGLE-AEC1-Z).

\*\* Moisture Sensitivity Level Rating

\*\*\* Wettable flank

**Note:**

2) Contact MPS for details on additional output voltages that may be available.

### TOP MARKING

**MPYW**  
**3808**  
**LLL**  
**ME**

MP: MPS prefix  
 Y: Year code  
 W: Week code  
 3808: First four digits of the part number  
 LLL: Lot number  
 M: Module  
 E: Wettable flank frame

### TOP MARKING

**MPYW**  
**3808**  
**LLL**  
**ME12**

MP: MPS prefix  
 Y: Year code  
 W: Week code  
 3808: First four digits of the part number  
 LLL: Lot number  
 M: Module  
 E: Wettable flank frame  
 12: 1.2V fixed-output version of the MPM3808

### TOP MARKING

MPYW

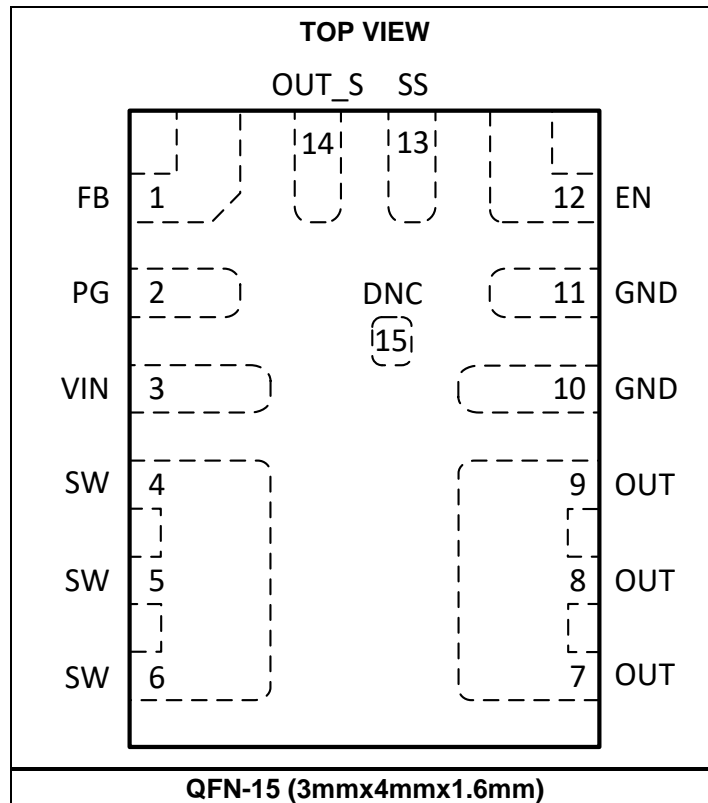
3808

LLL

ME18

MP: MPS prefix  
 Y: Year code  
 W: Week code  
 3808: First four digits of the part number  
 LLL: Lot number  
 M: Module  
 E: Wettable flank frame  
 18: 1.8V fixed-output version of the MPM3808

### PACKAGE REFERENCE



## PIN FUNCTIONS

Pin #	Name	Description
1	FB	<b>Feedback.</b> In the adjustable-output version of the MPM3808, connect the FB pin to an external resistor divider from the output to GND to set the output voltage ( $V_{OUT}$ ). To set the regulation voltage, the FB voltage ( $V_{FB}$ ) is compared to the 0.6V internal reference voltage ( $V_{REF}$ ). In the fixed-output version of the MPM3808, float this pin.
2	PG	<b>Power good indicator.</b> The PG pin is an open-drain output. Connect PG to a voltage source using an external resistor. When $V_{FB}$ exceeds 90% of $V_{REF}$ , PG is pulled high. If $V_{FB}$ drops below 85% of $V_{REF}$ , PG is pulled low to GND. Float this pin if it is not used.
3	VIN	<b>Input supply.</b> The MPM3808 operates from a 2.5V to 5.5V input voltage ( $V_{IN}$ ). A decoupling capacitor is required to prevent large voltage spikes at the input.
4, 5, 6	SW	<b>Switch output.</b> The SW pin is the internal, high-side P-channel MOSFET drain, and is connected internally to the power inductor.
7, 8, 9	OUT	<b>Power output.</b> Connect the OUT pin to the load. An output capacitor ( $C_{OUT}$ ) is required to reduce the voltage ripple.
10, 11	GND	<b>IC ground.</b> Connect the GND pin to the negative terminals of the input and output capacitors using large copper areas. Use several vias to connect GND to the ground plane.
12	EN	<b>Enable.</b> Pull EN below the 0.65V falling threshold to shut down the chip. Pull EN above the 0.9V rising threshold to enable the chip. There is an internal 2M $\Omega$ resistor from EN to ground.
13	SS	<b>Soft start.</b> Connect a capacitor between SS and GND to set the soft-start (SS) timer to avoid start-up inrush current. The minimum recommended soft-start capacitance ( $C_{SS}$ ) is 1nF.
14	OUT_S	<b>Output sense.</b> OUT_S is the sensing pin for $V_{OUT}$ and the discharge path to the 150 $\Omega$ resistor load.
15	DNC	<b>Do not connect.</b> This pad is connected internally to SW. Do not route or place vias under this area.

### ABSOLUTE MAXIMUM RATINGS <sup>(3)</sup>

All pins.....	-0.3V to +6.5V
Continuous power dissipation ( $T_A = 25^\circ\text{C}$ ) <sup>(4)</sup> <sup>(8)</sup>	
QFN-15 (3mmx4mmx1.6mm).....	2.4W
Operating junction temperature .....	150 $^\circ\text{C}$
Lead temperature.....	260 $^\circ\text{C}$
Storage temperature.....	-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$

### ESD Ratings

Human body model (HBM).....	Class 2 <sup>(5)</sup>
Charged device model (CDM).....	Class 2b <sup>(6)</sup>

### Recommended Operating Conditions

Input voltage ( $V_{IN}$ ).....	2.5V to 5.5V
Output voltage ( $V_{OUT}$ ).....	0.6V to $V_{IN} - 0.5V$
Load current range.....	0A to 3A
Operating junction temp ( $T_J$ )....	-40 $^\circ\text{C}$ to +150 $^\circ\text{C}$

### Thermal Resistance $\theta_{JA}$ $\theta_{JC}$

QFN-15 (3mmx4mmx1.6mm)	
JESD51-7.....	65.....14... $^\circ\text{C/W}$ <sup>(7)</sup>
EVM3808-LE-00A.....	53.....10... $^\circ\text{C/W}$ <sup>(8)</sup>

#### Notes:

- 3) Exceeding these ratings may damage the device.
- 4) The maximum allowable power dissipation is a function of the maximum junction temperature,  $T_J$  (MAX), the junction-to-ambient thermal resistance,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 5) Per AEC-Q100-002
- 6) Per AEC-Q100-011
- 7) Measured on JESD51-7, a 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The  $\theta_{JC}$  value shows the thermal resistance from the junction-to-case bottom.
- 8) Measured on the standard EVB, a 4-layer, 2oz, copper PCB (6.3cmx6.3cm). The  $\theta_{JC}$  value shows the thermal resistance from the junction-to-case top.

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 3.6V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , typical values are at  $T_J = 25^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>Input Supply</b>						
Under-voltage lockout (UVLO) rising threshold	$V_{UVLO\_RISING}$			2.3	2.45	V
Input voltage ( $V_{IN}$ ) UVLO falling threshold	$V_{UVLO\_FALLING}$			2.1		V
$V_{IN}$ UVLO hysteresis	$V_{UVLO\_HYS}$			0.2		V
$V_{IN}$ quiescent current	$I_Q$	$V_{EN} = 2V$ , $V_{FB} = 0.63V$ , $V_{IN} = 3.6V$ , $T_J = 25^{\circ}C$		21	30	$\mu A$
		$V_{EN} = 2V$ , $V_{FB} = 0.63V$ , $V_{IN} = 3.6V$ , $T_J = -40^{\circ}C$ to $+125^{\circ}C$ <sup>(9)</sup>			40	
		$V_{EN} = 2V$ , $V_{FB} = 0.63V$ , $V_{IN} = 3.6V$ , $T_J = -40^{\circ}C$ to $+150^{\circ}C$			80	
$V_{IN}$ shutdown current	$I_{SHDN}$	$V_{EN} = 0V$ , $T_J = 25^{\circ}C$		0.01	1	$\mu A$
		$V_{EN} = 0V$ , $T_J = -40^{\circ}C$ to $+125^{\circ}C$ <sup>(9)</sup>			3	
		$V_{EN} = 0V$ , $T_J = -40^{\circ}C$ to $+150^{\circ}C$			20	
$V_{IN}$ over-voltage protection (OVP) rising threshold	$V_{INOVP\_RISING}$	After output voltage ( $V_{OUT}$ ) OVP is enabled		6.15		V
$V_{IN}$ OVP falling threshold	$V_{INOVP\_FALLING}$			5.95		V
$V_{IN}$ OVP hysteresis	$V_{INOVP\_HYS}$			0.2		V
<b>Frequency, Switches, and Inductors</b>						
Switching frequency	$f_{SW}$		2000	2400	2640	kHz
Minimum on time <sup>(7)</sup>	$t_{ON\_MIN}$	$V_{IN} = 5V$		50		ns
Minimum off time <sup>(7)</sup>	$t_{OFF\_MIN}$	$V_{IN} = 5V$		80		ns
Maximum duty cycle	$D_{MAX}$			100		%
Switch leakage current	$I_{SW\_LKG}$	$V_{EN} = 0V$ , $V_{IN} = 6V$ , $V_{SW} = 0V$ or $6V$ , $T_J = 25^{\circ}C$		0.0	1	$\mu A$
		$V_{EN} = 0V$ , $V_{IN} = 6V$ , $V_{SW} = 0V$ or $6V$ , $T_J = -40^{\circ}C$ to $+125^{\circ}C$ <sup>(9)</sup>			30	
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	$V_{IN} = 5V$		65	85	m $\Omega$
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$	$V_{IN} = 5V$		35	55	m $\Omega$
Integrated inductor value <sup>(9)</sup>	L		376	470	564	nH
Integrated inductor DC resistance	$R_L$			25	65	m $\Omega$
Integrated inductor saturation current <sup>(9)</sup>	$I_{L\_SAT}$		4.8	5.4		A

**ELECTRICAL CHARACTERISTICS (continued)**
 $V_{IN} = 3.6V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , typical values are at  $T_J = 25^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>Output and Regulation</b>						
FB voltage (adjustable output)	$V_{FB}$	$T_J = 25^{\circ}C$	0.594	0.6	0.606	V
		$T_J = -40^{\circ}C$ to $+150^{\circ}C$	0.591	0.6	0.609	V
Output regulation voltage (fixed output)	$V_{OUT\_REG}$	1.2V fixed output	1.176	1.2	1.224	V
		1.8V fixed output	1.764	1.8	1.836	
FB input current	$I_{FB}$	Adjustable output		50	100	nA
		1.2V fixed output		3	8	$\mu A$
		1.8V fixed output		5	10	
$V_{OUT}$ discharge resistance	$R_{DIS}$	$V_{EN} = 0V$ , $V_{OUT} = 1.2V$		150		$\Omega$
<b>Enable (EN)</b>						
EN rising threshold	$V_{EN\_RISING}$			0.9	1.2	V
EN falling threshold	$V_{EN\_FALLING}$		0.4	0.65		V
EN threshold hysteresis	$V_{EN\_HYS}$			0.25		V
EN turn-on delay		Pull EN high to enable SW		100		$\mu s$
EN turn-off delay		Pull EN low to stop switching		30		$\mu s$
EN pull-down resistor				2		M $\Omega$
EN input current	$I_{EN}$	$V_{EN} = 2V$		1.2		$\mu A$
		$V_{EN} = 0V$		0		$\mu A$
<b>Soft Start (SS)</b>						
Soft-start current	$I_{SS}$		1.5	3	4.5	$\mu A$
<b>Power Good (PG)</b>						
PG rising threshold	$PG_{VTH\_RISING}$	FB rising edge	87%	90%	93%	$V_{FB}$
PG falling threshold	$PG_{VTH\_FALLING}$	FB falling edge	82%	85%	88%	$V_{FB}$
PG logic high voltage	$V_{PG\_HIGH}$	$V_{IN} = 5V$ , $V_{FB} = 0.6V$	4.9			V
PG sink current capability	$V_{PG\_LOW}$	Sink 1mA			0.4	V
PG rising deglitch	$t_{PGOOD\_R}$			80		$\mu s$
PG falling deglitch	$t_{PGOOD\_F}$			80		$\mu s$
PG leakage current (high)		5V logic high			100	nA
PG self-bias		$V_{IN} = 0V$ , $V_{EN} = 0V$ , PG is pulled up between 3V and 5.5V via a 100k $\Omega$ resistor			0.7	V
<b>Protections</b>						
Peak current limit	$I_{LIMIT\_PEAK}$		4	5	6	A
Valley current limit	$I_{LIMIT\_VALLEY}$		1.5	3	4.5	A
Reverse current limit	$I_{LIMIT\_REVERSE}$	Current flows from SW to GND		1.2		A
Zero-current detection (ZCD) threshold				50		mA

**ELECTRICAL CHARACTERISTICS (continued)**
 $V_{IN} = 3.6V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , typical values are at  $T_J = 25^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Thermal shutdown <sup>(9)</sup>	$T_{SD}$			170		$^{\circ}C$
Thermal shutdown hysteresis <sup>(9)</sup>	$T_{SD\_HYS}$			20		$^{\circ}C$
Output over-voltage (OV) threshold	$V_{OVP}$		110%	115%	120%	$V_{FB}$
Output OVP hysteresis	$V_{OVP\_HYS}$			10%		$V_{FB}$
OVP delay				2		$\mu s$

**Note:**

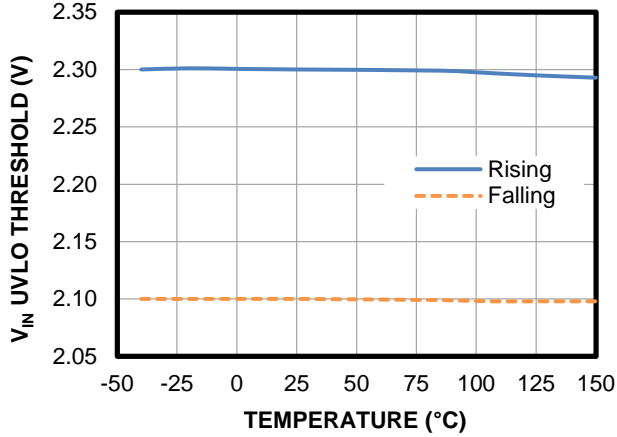
9) Not tested in production. Guaranteed by design and characterization.



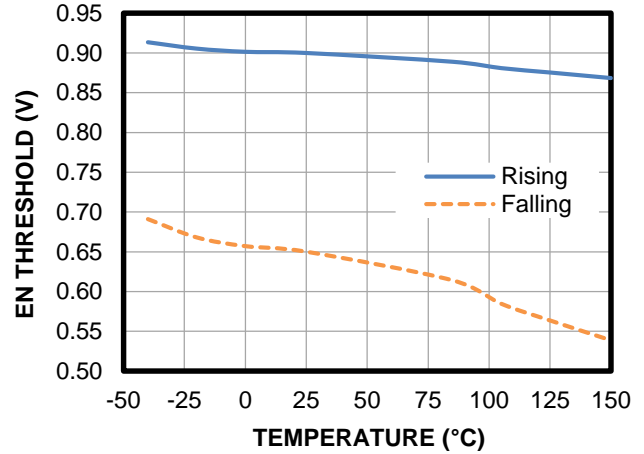
## TYPICAL CHARACTERISTICS

$V_{IN} = 3.6V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , unless otherwise noted.

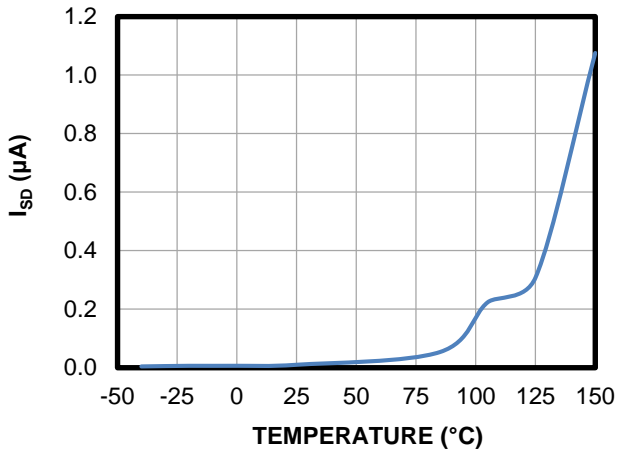
$V_{IN}$  UVLO Threshold vs. Temperature



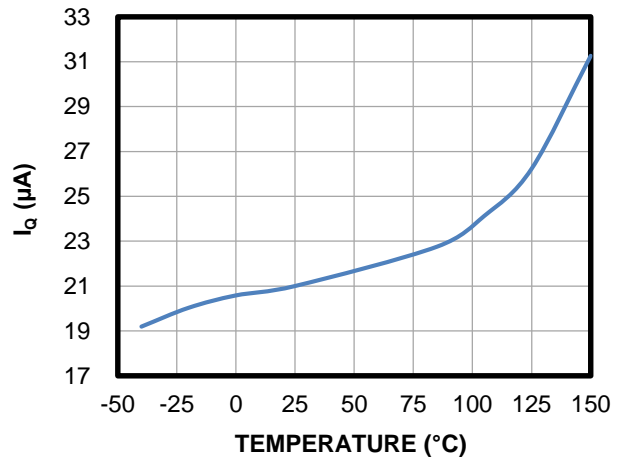
EN Threshold vs. Temperature



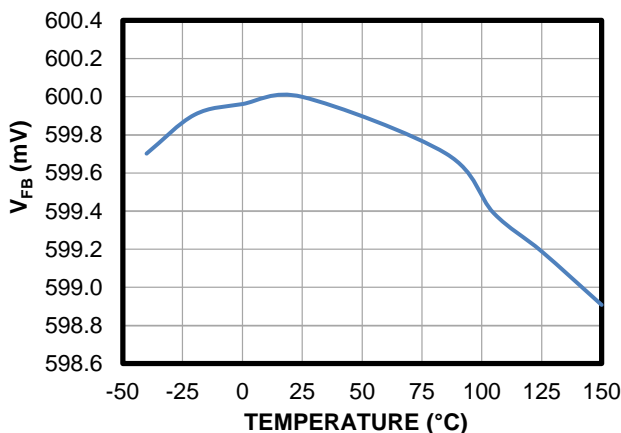
Shutdown Current vs. Temperature



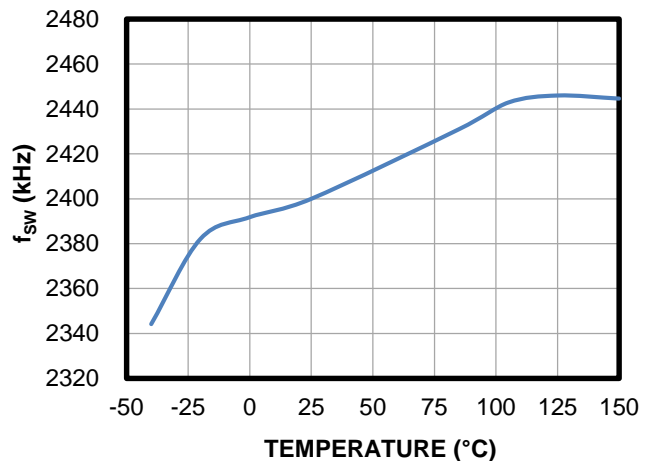
Quiescent Current vs. Temperature



Feedback Voltage vs. Temperature



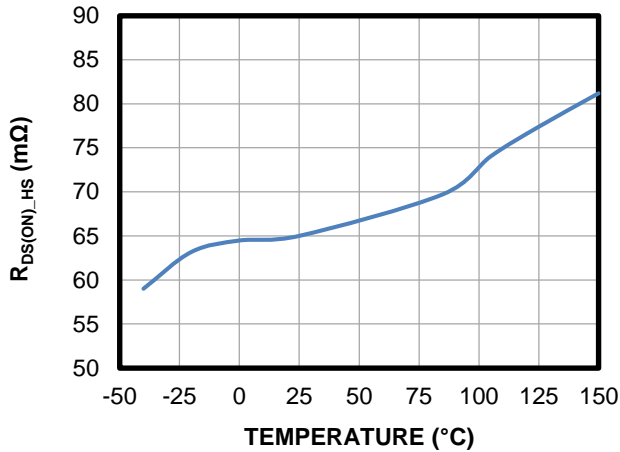
Switching Frequency vs. Temperature



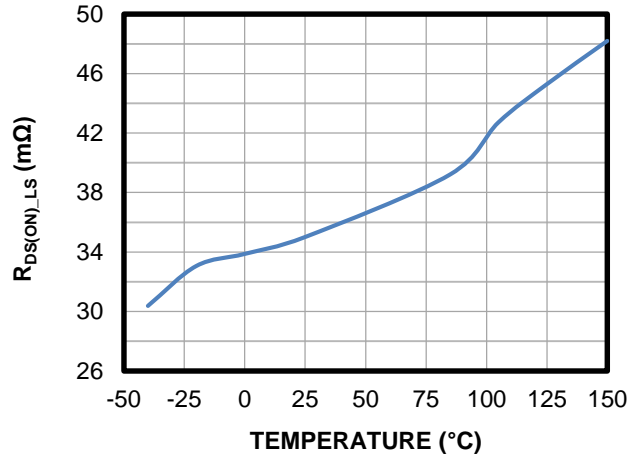
### TYPICAL CHARACTERISTICS (continued)

$V_{IN} = 3.6V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , unless otherwise noted.

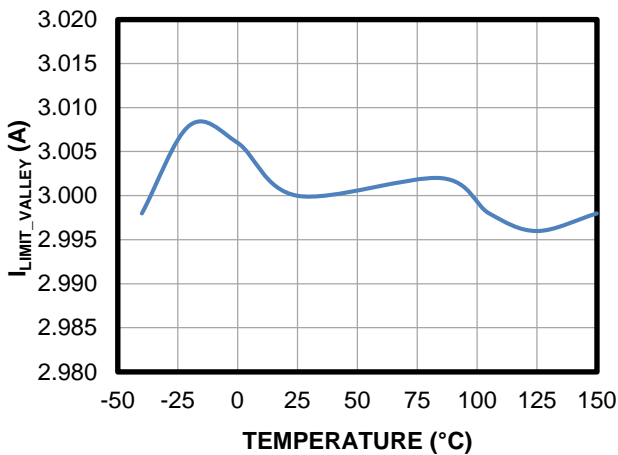
**HS-FET On Resistance vs. Temperature**



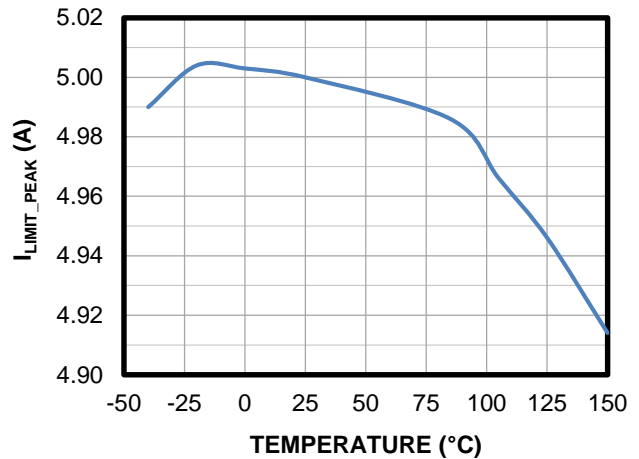
**LS-FET On Resistance vs. Temperature**



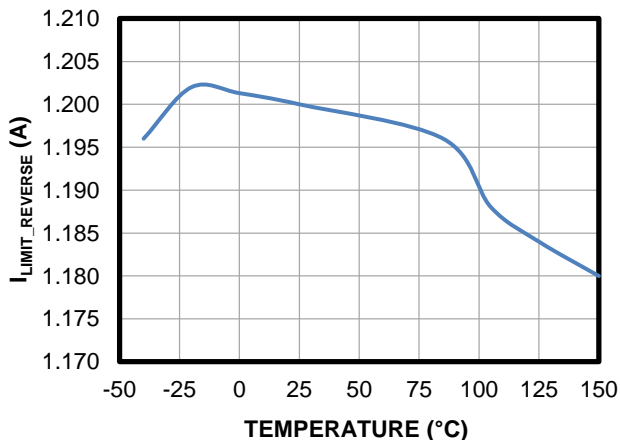
**Valley Current Limit vs. Temperature**



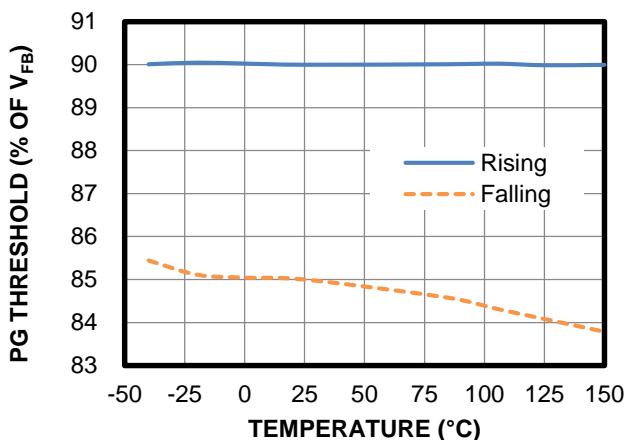
**Peak Current Limit vs. Temperature**



**Reverse Current Limit vs. Temperature**



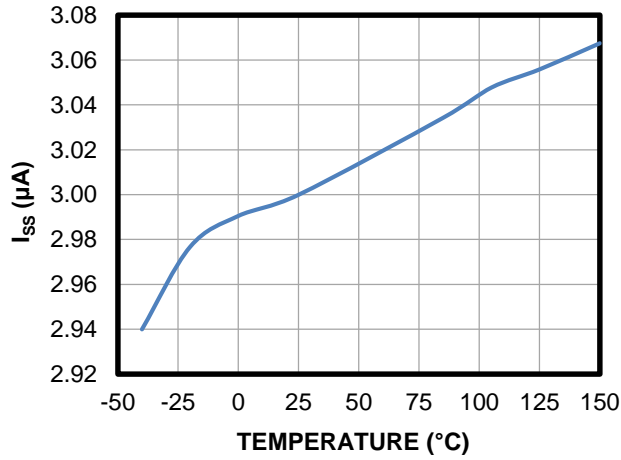
**PG Threshold vs. Temperature**



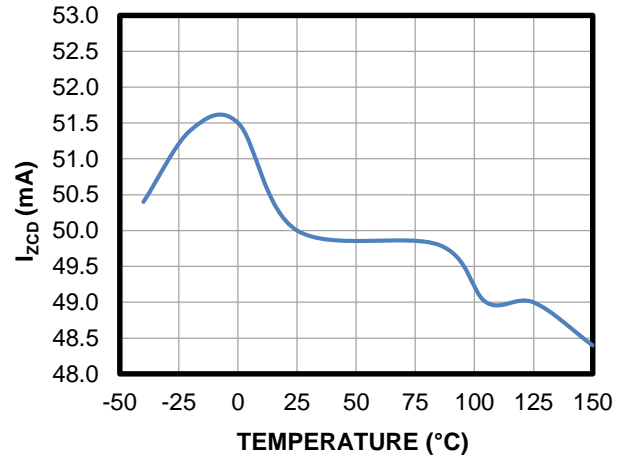
**TYPICAL CHARACTERISTICS** *(continued)*

$V_{IN} = 3.6V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , unless otherwise noted.

**Soft-Start Current vs. Temperature**

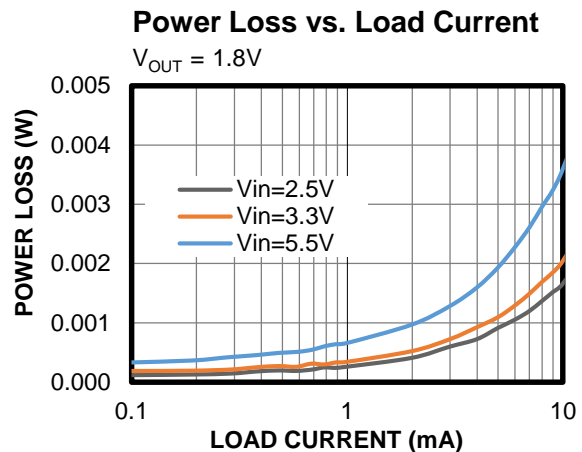
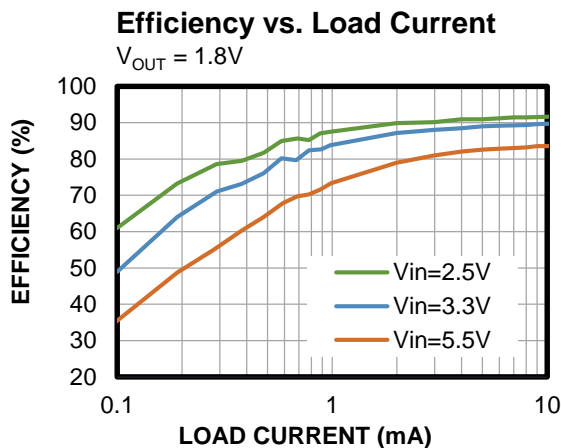
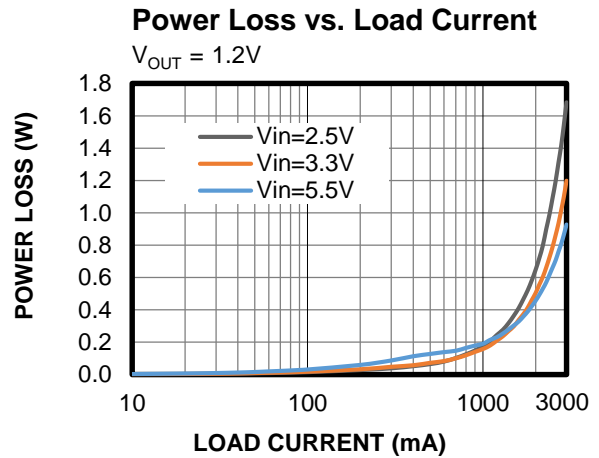
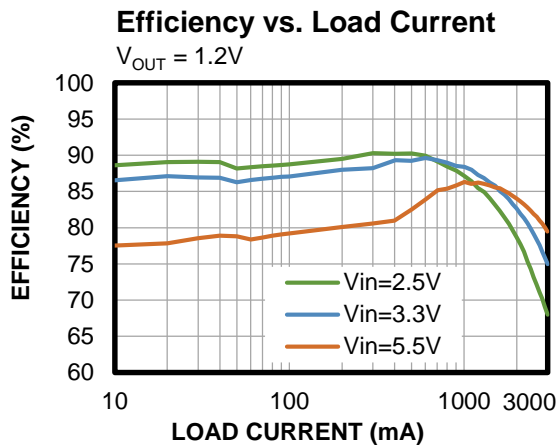
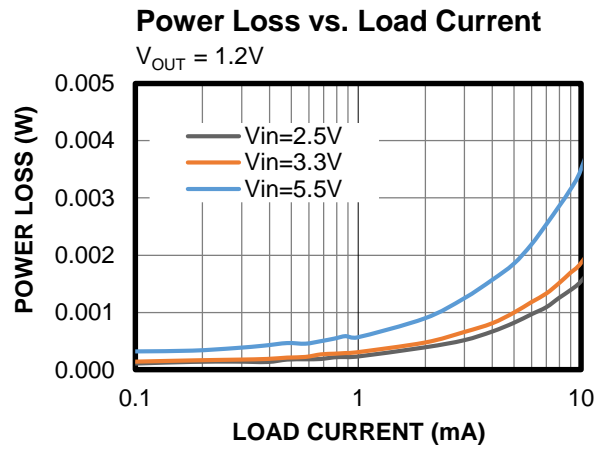
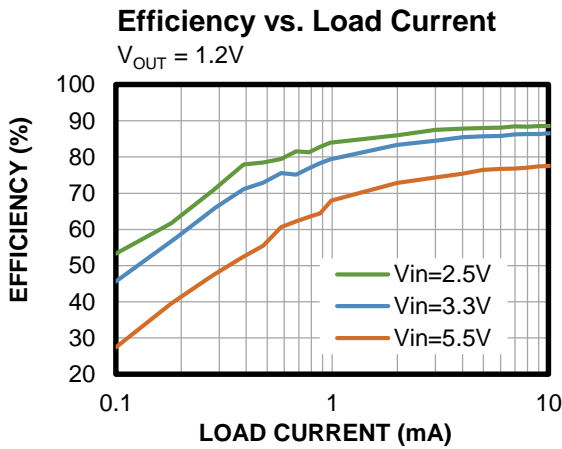


**Zero-Current Detection vs. Temperature**



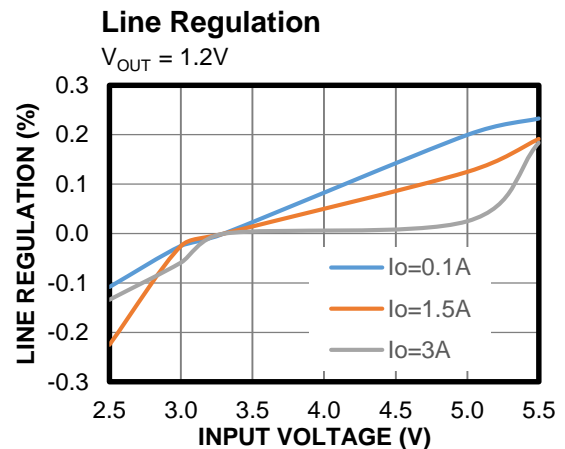
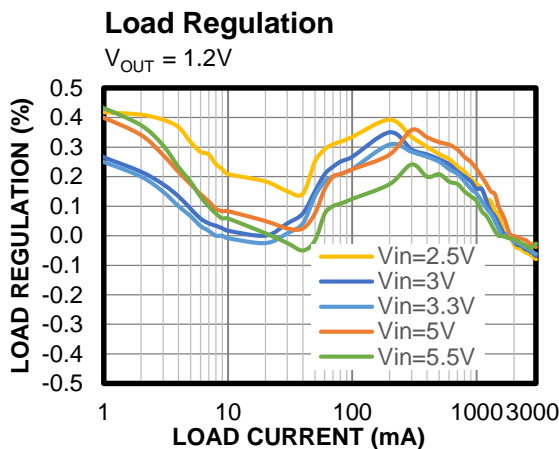
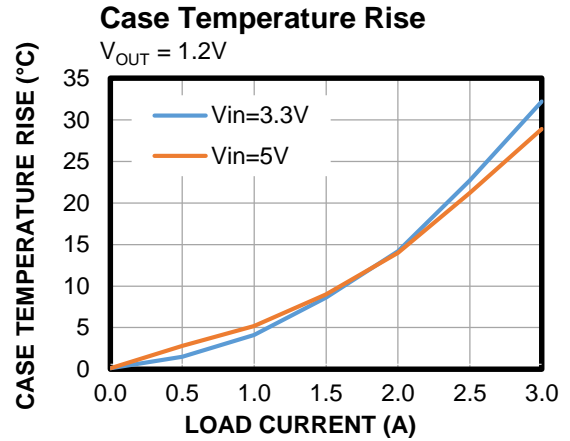
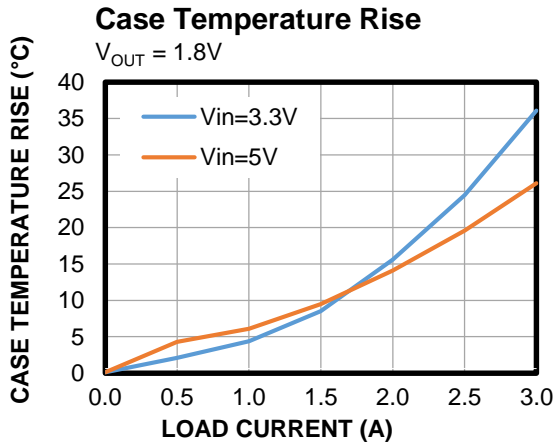
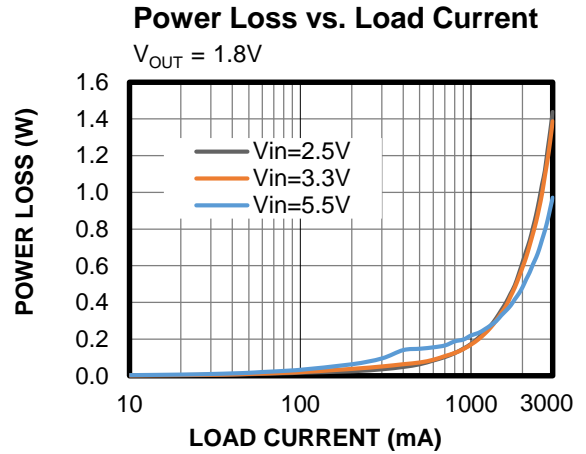
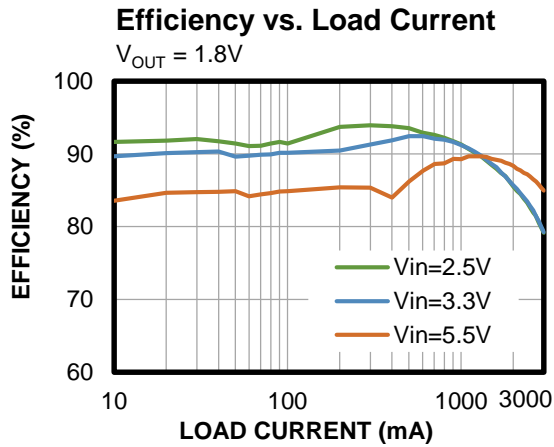
## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 3.3V$ ,  $V_{OUT} = 1.2V$ ,  $C_{OUT} = 22\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.



**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

$V_{IN} = 3.3V$ ,  $V_{OUT} = 1.2V$ ,  $C_{OUT} = 22\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

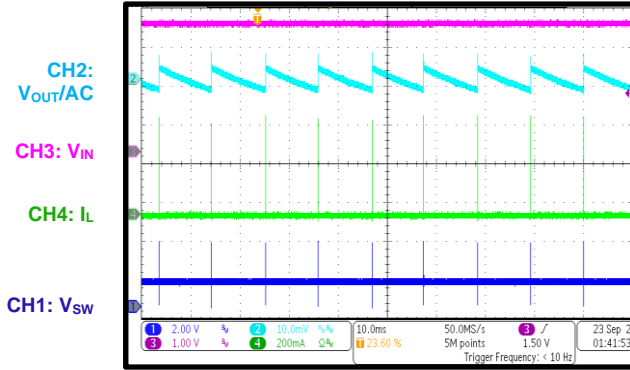


### TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 3.3V$ ,  $V_{OUT} = 1.2V$ ,  $C_{OUT} = 22\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

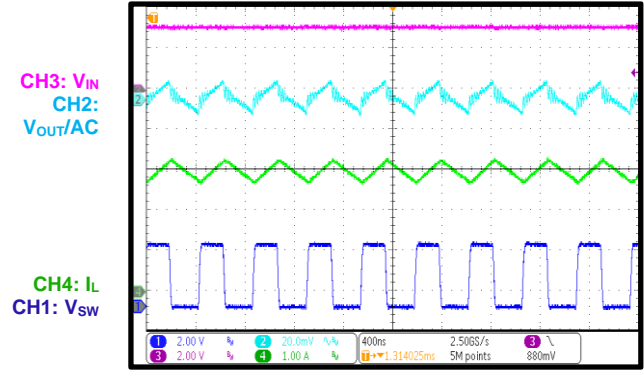
#### Steady State

$I_{OUT} = 0A$



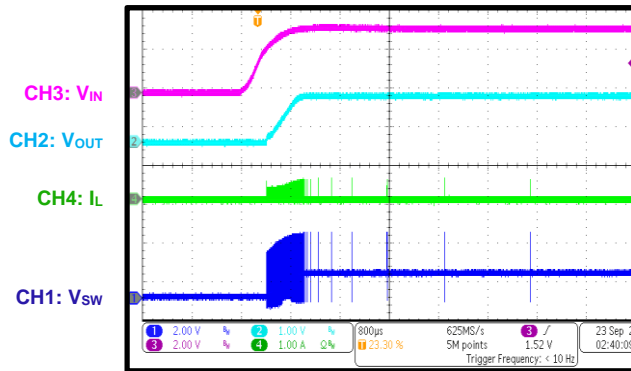
#### Steady State

$I_{OUT} = 3A$



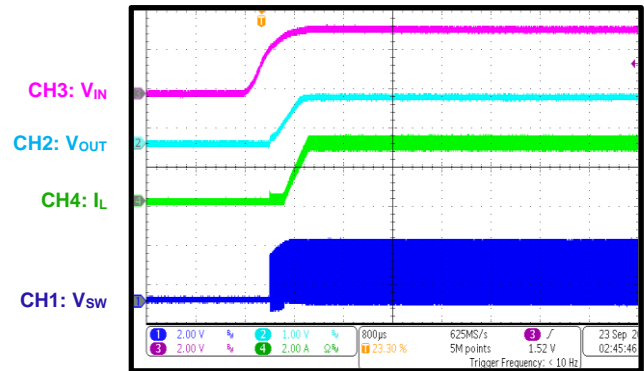
#### Start-Up through VIN

$I_{OUT} = 0A$



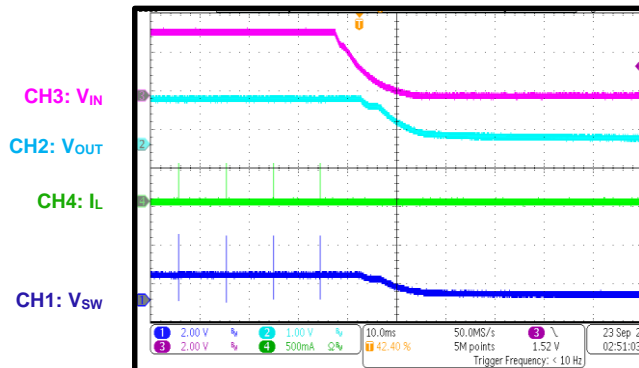
#### Start-Up through VIN

$I_{OUT} = 3A$



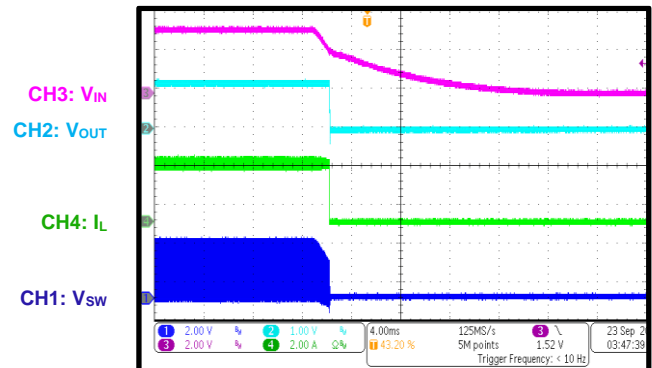
#### Shutdown through VIN

$I_{OUT} = 0A$



#### Shutdown through VIN

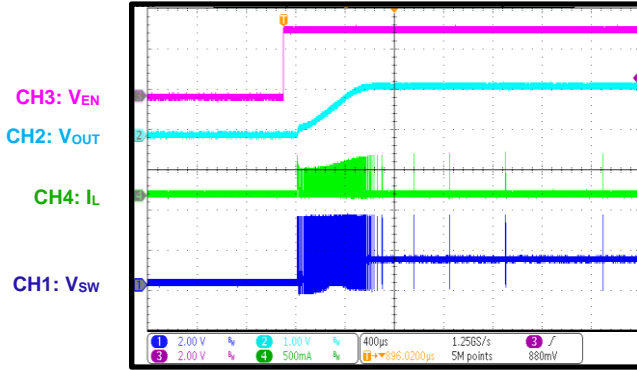
$I_{OUT} = 3A$



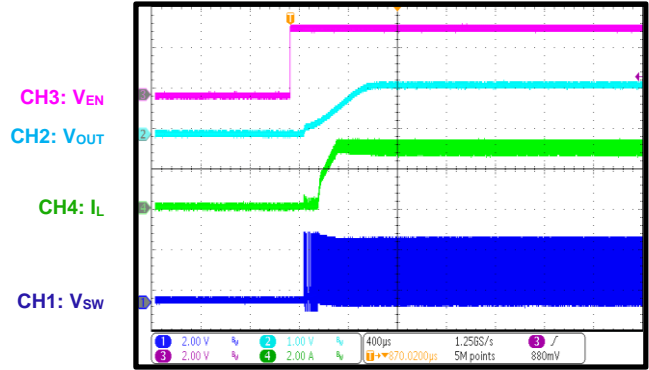
### TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 3.3V$ ,  $V_{OUT} = 1.2V$ ,  $C_{OUT} = 22\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

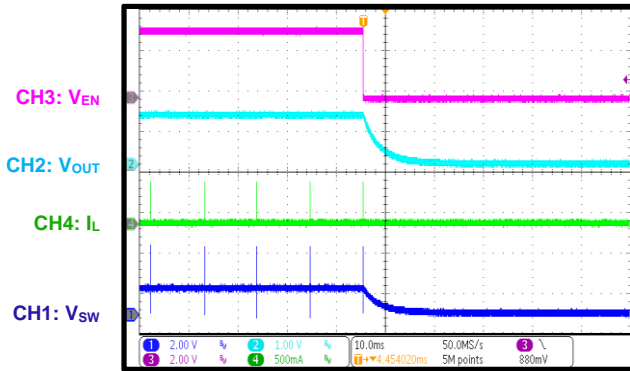
**Start-Up through EN**  
 $I_{OUT} = 0A$



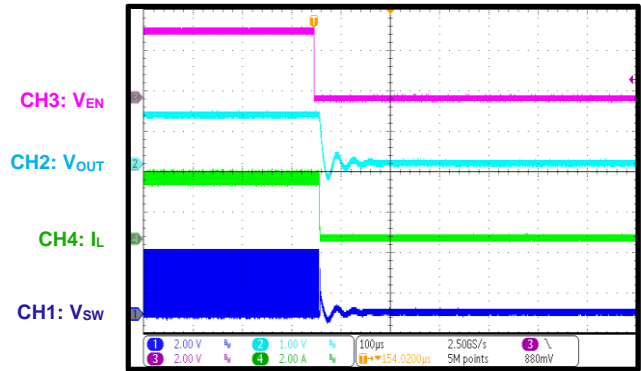
**Start-Up through EN**  
 $I_{OUT} = 3A$



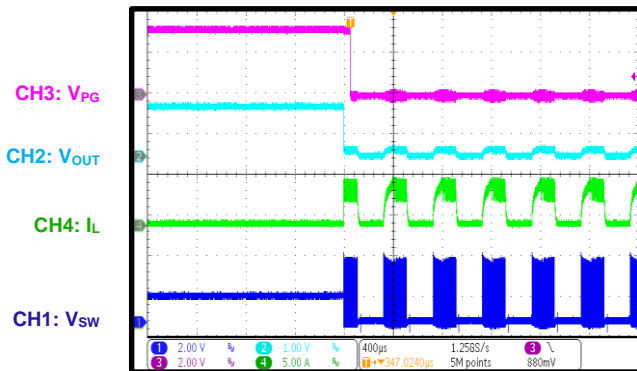
**Shutdown through EN**  
 $I_{OUT} = 0A$



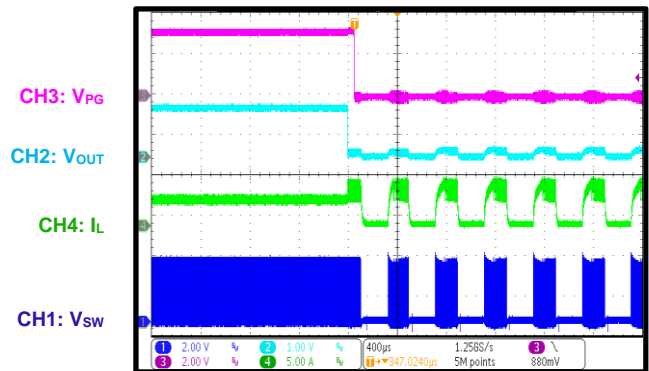
**Shutdown through EN**  
 $I_{OUT} = 3A$



**SCP Entry**  
 $I_{OUT} = 0A$



**SCP Entry**  
 $I_{OUT} = 3A$

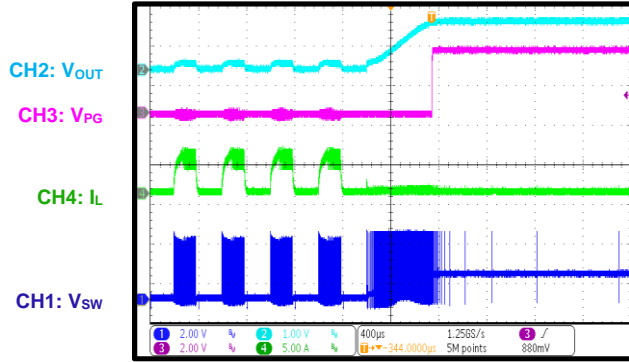


### TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 3.3V$ ,  $V_{OUT} = 1.2V$ ,  $C_{OUT} = 22\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

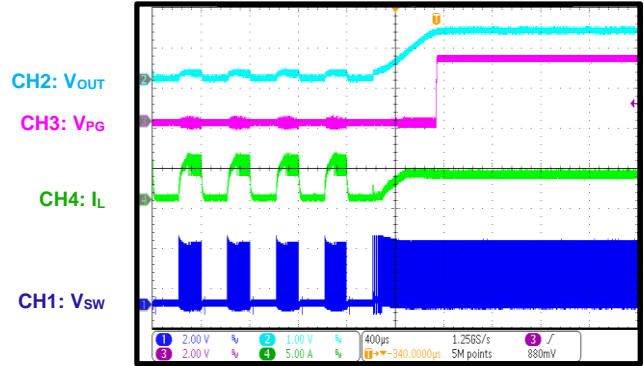
#### SCP Recovery

$I_{OUT} = 0A$

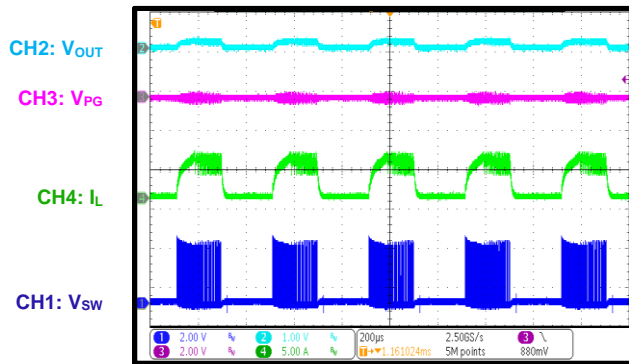


#### SCP Recovery

$I_{OUT} = 3A$

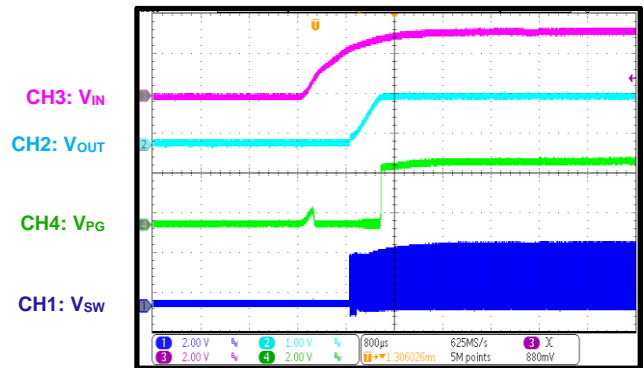


#### Short-Circuit Protection



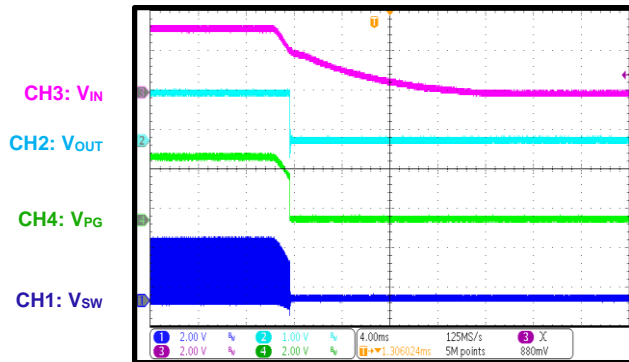
#### PG Start-Up through VIN

$I_{OUT} = 3A$



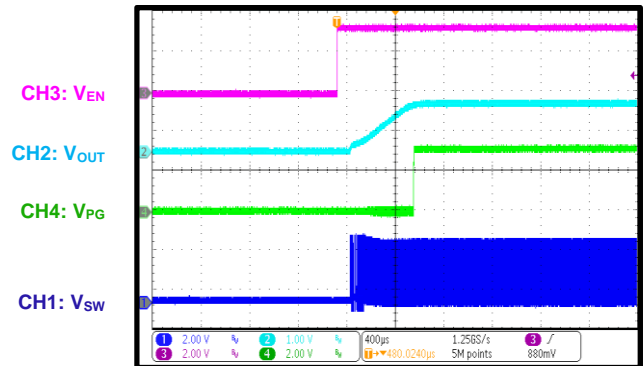
#### PG Shutdown through VIN

$I_{OUT} = 3A$



#### PG Start-Up through EN

$I_{OUT} = 3A$



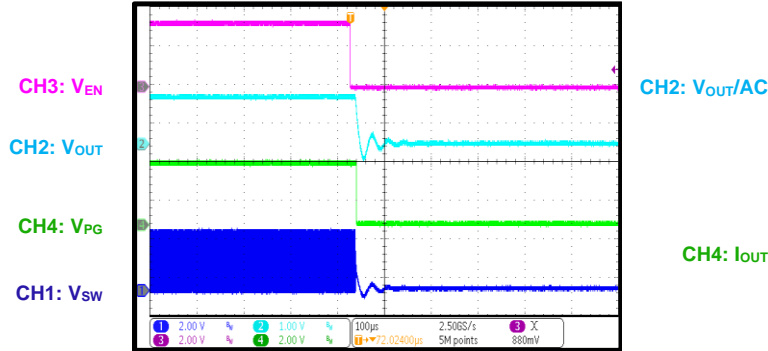


## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 3.3V$ ,  $V_{OUT} = 1.2V$ ,  $C_{OUT} = 22\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

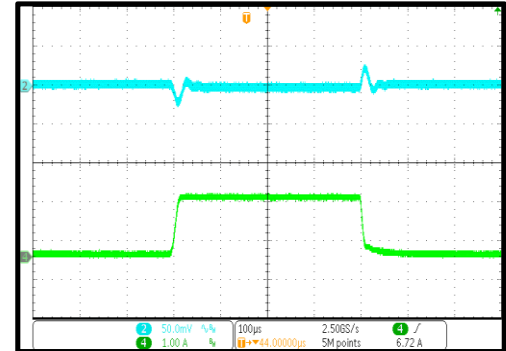
### PG Shutdown through EN

$I_{OUT} = 3A$



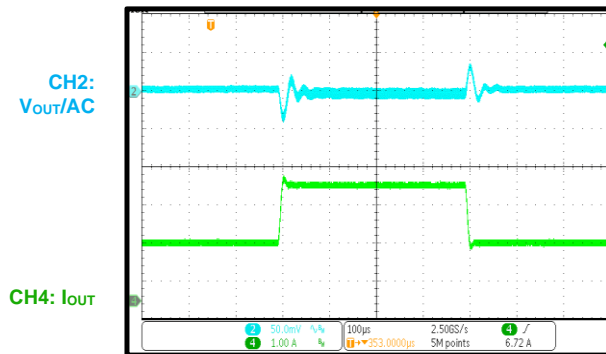
### Load Transient

$I_{OUT} = 0A$  to  $1.5A$ ,  $1A/\mu s$



### Load Transient

$I_{OUT} = 1.5A$  to  $3A$ ,  $1A/\mu s$



### FUNCTION BLOCK DIAGRAM

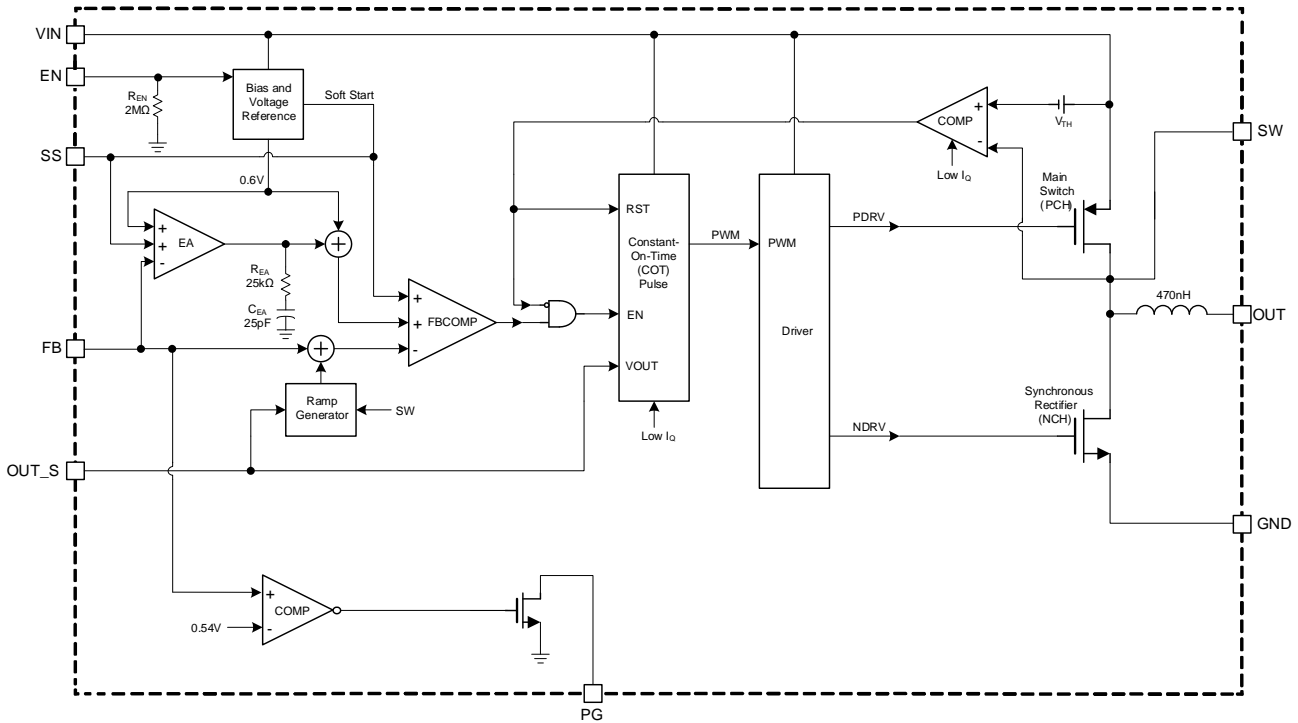


Figure 1: Functional Block Diagram (Adjustable Output)

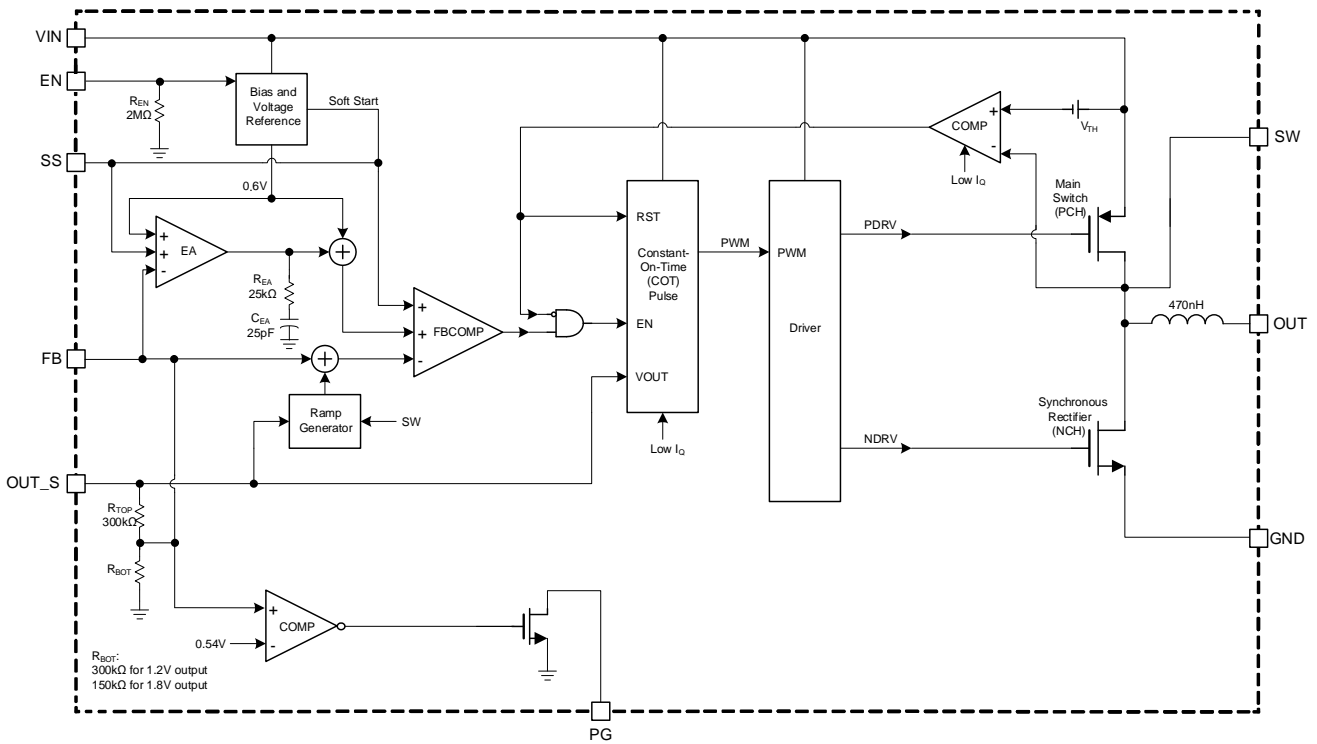


Figure 2: Functional Block Diagram (Fixed Output)

## OPERATION

The MPM3808 employs input voltage ( $V_{IN}$ ) feed-forward and constant-on-time (COT) control to stabilize the switching frequency ( $f_{SW}$ ) across the entire  $V_{IN}$  range. It can achieve 3A of output current ( $I_{OUT}$ ) across a 2.5V to 5.5V  $V_{IN}$  range, with excellent load and line regulation. The output voltage ( $V_{OUT}$ ) can be regulated to as low as 0.6V. A 100% maximum duty cycle can be reached in low-dropout (LDO) mode.

### Constant-On-Time (COT) Control

The MPM3808's COT control provides a simpler control loop and faster transient response. The switching cycles have a fixed minimum off time ( $t_{OFF\_MIN}$ ) to prevent inductor current ( $I_L$ ) runaway during load transient. If the low-side MOSFET (LS-FET) turns on, it remains on for at least  $t_{MIN\_OFF}$  (typically 80ns). The high-side MOSFET (HS-FET) turns on once the feedback (FB) voltage ( $V_{FB}$ ) drops below the reference voltage ( $V_{REF}$ ), which indicates an insufficient  $V_{OUT}$ .  $V_{IN}$  feed-forward allows the device to maintain a nearly constant  $f_{SW}$  across the input range and load range. The  $f_{SW}$  on time ( $t_{ON}$ ) can be calculated using Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 400ns \quad (1)$$

### Sleep Mode

The MPM3808 employs sleep mode for high efficiency under light-load conditions. In sleep mode, most of the circuit block input currents ( $I_{IN}$ ) decrease, specifically the error amplifier (EA) and pulse-width modulation (PWM) comparator.

As the load becomes lighter, the converter's  $f_{SW}$  decreases. If the load continues to decrease and the off time ( $t_{OFF}$ ) exceeds 3.5 $\mu$ s, then the MPM3808 enters sleep mode. To further improve light-load efficiency, the converter consumes a very low quiescent current ( $I_Q$ ) while in sleep mode.

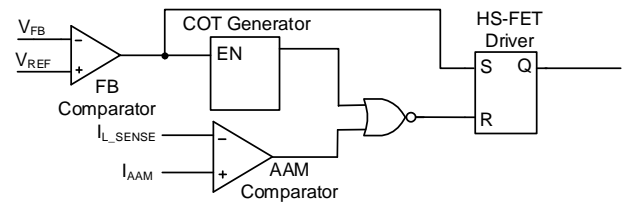
Once an HS-FET pulse occurs, the MPM3808 exits sleep mode.

### Advanced Asynchronous Modulation (AAM) Mode under Light-Load Conditions

The MPM3808 features advanced asynchronous modulation (AAM) mode and a

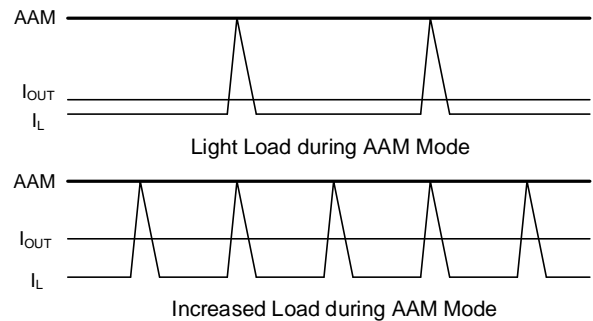
zero-current detection (ZCD) circuit for light-load operation.

The AAM current ( $I_{AAM}$ ) is set internally. The SW pin's on time ( $t_{ON}$ ) is determined by the on-timer generator and AAM comparator. Under light-load conditions, SW's  $t_{ON}$  exceeds the AAM comparator's  $t_{ON}$ . Figure 3 shows the simplified AAM control logic.



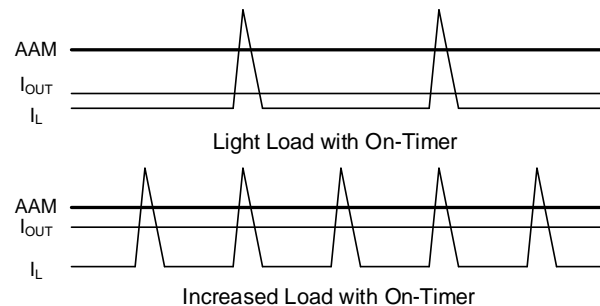
**Figure 3: Simplified AAM Control Logic**

If the AAM comparator's  $t_{ON}$  exceeds the on-timer's pulse, then the AAM comparator controls SW's  $t_{ON}$  (see Figure 4).



**Figure 4: AAM Comparator Controls SW's  $t_{ON}$**

When using a lower-value inductor, if the AAM comparator's  $t_{ON}$  is below the on-timer, the HS-FET depends on the on-timer. Therefore, the on-timer controls  $t_{ON}$  (see Figure 5).

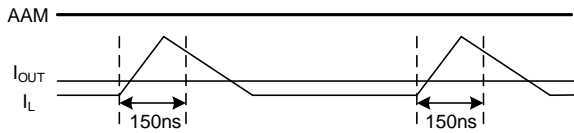


**Figure 5: On-Timer Controls SW's  $t_{ON}$**

Aside from the on-timer method, the AAM circuit has another AAM blanking time (150ns) for sleep mode. This means that if the on-timer drops

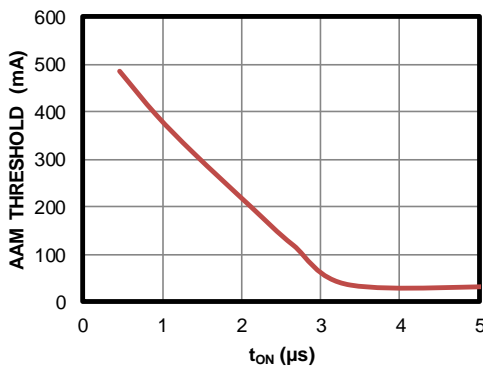
below 150ns, then the HS-FET turns off after an on-timer pulse is generated without AAM control.

In this scenario,  $I_L$  may not reach the AAM threshold (see Figure 6).



**Figure 6: AAM Blanking Time during Sleep Mode**

In sleep mode, the on-timer's pulse is about 40% above its pulse during discontinuous conduction mode (DCM) and continuous conduction mode (CCM). Figure 7 shows how the AAM threshold decreases as  $t_{ON}$  increases gradually. In CCM,  $I_{OUT}$  must exceed half of the AAM threshold.



**Figure 7: AAM Threshold Decreases as  $t_{ON}$  Increases**

The MPM3808 employs ZCD to determine whether  $I_L$  begins to reverse. If  $I_L$  reaches the ZCD threshold (typically 50mA), then the LS-FET turns off.

Even if  $V_{OUT}$  is close to  $V_{IN}$ , AAM mode and ZCD allow the device to operate continually in DCM under light-load conditions.

### Enable (EN) Control

The enable (EN) pin is a digital control pin that turns the MPM3808 on and off. Pull EN above 0.9V to turn the converter on; pull EN below 0.65V or float EN to turn it off. Pulling EN to GND also disables the device. There is an internal 2MΩ resistor connected between EN and GND.

### Output Discharge

If the MPM3808 shuts down, the device initiates output discharge mode. The internal discharge MOSFET provides a resistive discharge path for the output capacitor (C2) between the OUT pin and GND. To block the output discharge path,

add an external capacitor between  $V_{OUT}$  and the OUT pin (see the Output Discharge Blocking section on page 23).

### Soft Start (SS)

The MPM3808 features external soft start (SS). To avoid overshoot during start-up, the SS pin ramps up  $V_{OUT}$  at a controlled slew rate. SS's charge current is typically 3μA. The SS time ( $t_{SS}$ ) is determined by the external SS capacitor ( $C_{SS}$ ).  $t_{SS}$  can be calculated using Equation (2):

$$t_{SS}(\text{ms}) = \frac{C_{SS}(\text{nF}) \times 0.6\text{V}}{I_{SS}(\mu\text{A})} \quad (2)$$

Where  $I_{SS}$  is the internal SS charge current (3μA).

It is recommended for  $C_{SS}$  to be  $\geq 1\text{nF}$ .

The MPM3808 has a pre-biased start-up function. Once EN is pulled above 0.9V, the converter starts up, regardless of any pre-biased voltage on the output. Pre-biased start-up works even while the output discharge path is blocked.

### Peak Current Limit and Valley Current Limit

Both the HS-FET and LS-FET feature current-limit protection. If  $I_L$  reaches the HS-FET's peak current limit ( $I_{LIMIT\_PEAK}$ ) threshold (typically 5A), the HS-FET turns off and the LS-FET turns on to discharge the energy. The HS-FET does not turn on again until  $I_L$  drops below the valley current limit ( $I_{LIMIT\_VALLEY}$ ) threshold (typically 3A). This prevents current runaway during overload and short-circuit events. The valley current limit is blocked unless HS-FET turns off due to the triggered peak current limit.

### Short-Circuit Protection (SCP) and Recovery

When a short-circuit condition occurs, the MPM3808 reaches its current limit immediately. Meanwhile,  $V_{OUT}$  drops until  $V_{FB}$  falls below 50% of  $V_{REF}$ , which is considered an output dead short. Short-circuit protection (SCP) with hiccup mode is then triggered to periodically restart the part. In hiccup mode, the output power stage is disabled, and the SS voltage ( $V_{SS}$ ) is discharged. Once  $V_{SS}$  is discharged completely, the device initiates a new SS. This process repeats until the fault condition is removed.

### Over-Voltage Protection (OVP)

The MPM3808 monitors  $V_{FB}$  to detect over-voltage (OV) conditions. If  $V_{FB}$  exceeds 115% of  $V_{REF}$ , then the converter enters its dynamic regulation period. During this period, the LS-FET remains on until its current reaches -1.2A. This process discharges  $V_{OUT}$  to keep it within its normal range. If the OV condition still remains after this process, there is a 1.5 $\mu$ s delay before the LS-FET turns on again. Once  $V_{FB}$  falls below 105% of  $V_{REF}$ , the converter exits the regulation period. If the dynamic regulation period cannot prevent  $V_{OUT}$  from increasing and a 6.1V  $V_{IN}$  is detected, then over-voltage protection (OVP) is triggered. The device stops switching until  $V_{IN}$  drops below 6V. Once  $V_{IN}$  drops below 6V, the MPM3808 resumes normal operation.

### Power Good (PG) Indicator

The MPM3808 has a power good (PG) output to indicate whether the converter is operating normally after start-up. PG is the open drain of an internal MOSFET. It is recommended that this MOSFET's maximum on resistance ( $R_{DS(ON)}$ ) be below 400 $\Omega$ . PG can be connected to  $V_{IN}$  or an external voltage source via an external resistor (10k $\Omega$  to 100k $\Omega$ ). Once  $V_{IN}$  is applied, the MOSFET turns on and PG is pulled to GND before SS is ready. After  $V_{FB}$  reaches 90% of  $V_{REF}$ , PG is pulled high by the external voltage source. If  $V_{FB}$  drops to 85% of  $V_{REF}$ , then the PG voltage ( $V_{PG}$ ) is pulled to GND to indicate an output failure.

If  $V_{IN}$  and EN are not available, and PG is pulled up via an external power supply, then PG self-biases and asserts. If a 100k $\Omega$  pull-up resistor is being used, then  $V_{PG}$  should be below 0.7V.

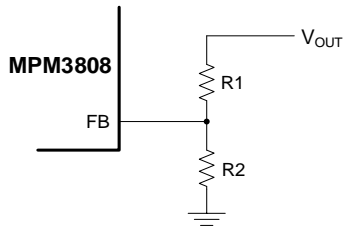
## APPLICATION INFORMATION

### Setting the Output Voltage

The external resistor divider sets the MPM3808's adjustable  $V_{OUT}$ . Select a feedback (FB) resistor (R1) to reduce the  $V_{OUT}$  leakage current (typically between 10k $\Omega$  and 100k $\Omega$ ). R2 can then be calculated using Equation (3):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6} - 1} \quad (3)$$

Figure 8 shows the FB network.



**Figure 8: Feedback Network**

Table 1 shows the recommended resistor values for common output voltages.

**Table 1: Resistor Values for Common Output Voltages**

$V_{OUT}$ (V)	R1 (k $\Omega$ )	R2 (k $\Omega$ )
1	30.9 (1%)	47 (1%)
1.2	100 (1%)	100 (1%)
1.8	36 (1%)	18 (1%)
2.5	51 (1%)	16 (1%)
3.3	68 (1%)	15 (1%)

For the fixed-output version of the MPM3808, it is not necessary to connect the external divider resistor. FB can be floated.

### Frequency Scaling at Low Input Voltages

Under heavy-load conditions, the HS-FET voltage decreases as  $t_{ON}$  increases and the duty cycle is extended. If the minimum off time ( $t_{OFF\_MIN}$ ) is reached at a low  $V_{IN}$  and under heavy-load conditions, then  $f_{SW}$  scales down. To maintain a constant  $f_{SW}$  during heavy-load operation, a larger  $V_{OUT}$  is required for a larger  $V_{IN}$ . For a 1.8V  $V_{OUT}$  at a 2A load,  $V_{IN}$  should be above 2.9V to keep  $f_{SW}$  above 2MHz. If the frequency begins to scale down,  $V_{IN}$  can be estimated using Equation (4):

$$V_{IN} = \frac{V_{OUT} + R_{DS(ON)\_HS} \times I_{OUT}}{1 - \frac{t_{OFF\_MIN}}{400 \times 10^{-9}}} \quad (4)$$

Where the maximum  $t_{OFF\_MIN}$  is 125ns. <sup>(8)</sup>

#### Note:

10) Guaranteed by design and bench characterization. Not tested in production.

### Selecting the Input Capacitor

The step-down converter has a discontinuous input current ( $I_{IN}$ ), and requires a capacitor to supply AC current to the converter while maintaining the DC  $V_{IN}$ . For the best performance, it is recommended to use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are strongly recommended due to their low ESR and small temperature coefficients. For most applications, a 10 $\mu$ F capacitor is sufficient. Higher output voltages may require a 22 $\mu$ F capacitor to increase system stability.

The input capacitor (C1) requires an adequate ripple current rating to absorb the switching  $I_{IN}$ .

C1's RMS current rating ( $I_{C1}$ ) can be estimated using Equation (5):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worst-case scenario occurs at  $V_{IN} = 2 \times V_{OUT}$ , which can be calculated using Equation (6):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current that exceeds half of the maximum load current.

C1 can be an electrolytic, tantalum, or ceramic capacitor. When using electrolytic or tantalum capacitors, place a small, high-quality, 0.1 $\mu$ F ceramic capacitor as close to the IC as possible. When using ceramic capacitors, ensure that the capacitor has enough capacitance to prevent excessive voltage ripple at the input. The input voltage ripple ( $\Delta V_{IN}$ ) can be estimated using Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

### Selecting the Output Capacitor

The output capacitor (C2) stabilizes the DC  $V_{OUT}$ . It is recommended to use ceramic capacitors for

C2, particularly low-ESR capacitors as they effectively limit the output voltage ripple ( $\Delta V_{OUT}$ ).  $\Delta V_{OUT}$  can be estimated using Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (8)$$

Where  $L_1$  is the inductance, and  $R_{ESR}$  is C2's equivalent series resistance (ESR).

When using ceramic capacitors, the capacitance dominates the impedance at  $f_{SW}$  and causes the majority of  $\Delta V_{OUT}$ . For simplification,  $\Delta V_{OUT}$  can be estimated using Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

Ceramic capacitors with X7R or X5R dielectrics are highly recommended due to their low ESR and small temperature coefficients.

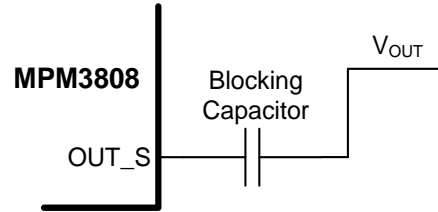
For tantalum or electrolytic capacitors, the ESR dominates the impedance at  $f_{SW}$ . For simplification,  $\Delta V_{OUT}$  can be estimated using Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (10)$$

C2's characteristics can also affect the stability of the regulation system.

### Output Discharge Blocking

If the device is disabled, an internal resistive discharge path between the OUT\_S pin and GND is enabled to discharge C2. The discharge path can be blocked by adding an external capacitor between  $V_{OUT}$  and the OUT\_S pin (see Figure 9).



**Figure 9: Circuit with  $V_{OUT}$  Discharge Blocking**

Discharge blocking is supported by the adjustable-output version. For the fixed-output versions, the OUT\_S pin should be connected to the output directly in order to regulate  $V_{OUT}$ .

To avoid influencing the loop and load transient, select a  $\geq 10\text{nF}$  blocking capacitor. It is recommended to use a 10nF to 100nF blocking capacitor. A larger-value blocking capacitor does not have an impact on loop performance, but is physically larger and is typically unnecessary for the best results.

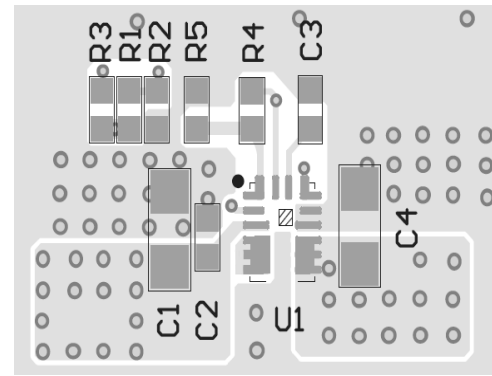
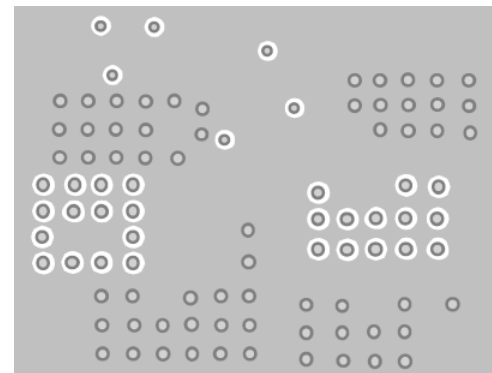
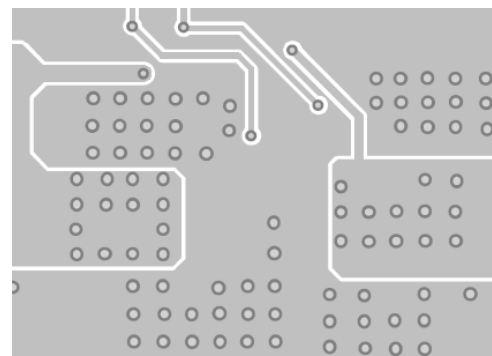
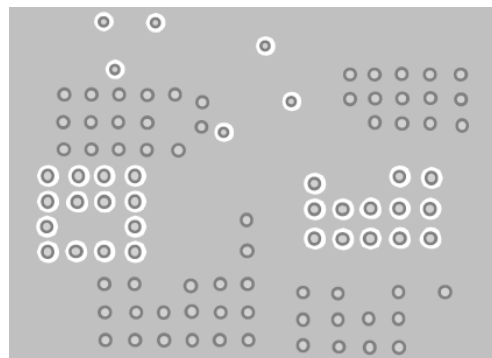
**PCB Layout Guidelines <sup>(9)</sup>**

Efficient PCB layout is critical for stable operation. The MPM3808’s integrated inductor simplifies the schematic and layout design, but some considerations must still be taken to ensure proper operation. A 4-layer layout is recommended to achieve improved EMC and thermal performance, although the device can operate sufficiently in a 2-layer layout. For the best results, refer to Figure 10 and follow the guidelines below:

1. Place the high-current paths (GND and VIN) very close to the device using short, direct, and wide traces.
2. Use large copper areas to minimize conduction loss and thermal stress.
3. Place the ceramic input capacitors as close to VIN as possible.
4. Place several vias close to the capacitor’s GND terminal and the GND pin on the IC to minimize high-frequency noise.
5. Place the FB resistors as close as possible to the FB pin to ensure that the trace connected to FB is as short as possible.
6. Use multiple vias to connect the power planes to the internal layer.

**Note:**

- 9) The recommended PCB layout is based on Figure 11 on page 25.


**Top Layer**

**Mid-Layer 1**

**Mid-Layer 2**

**Bottom Layer and Bottom Silk**
**Figure 10: Recommended PCB Layout**



### TYPICAL APPLICATION CIRCUITS

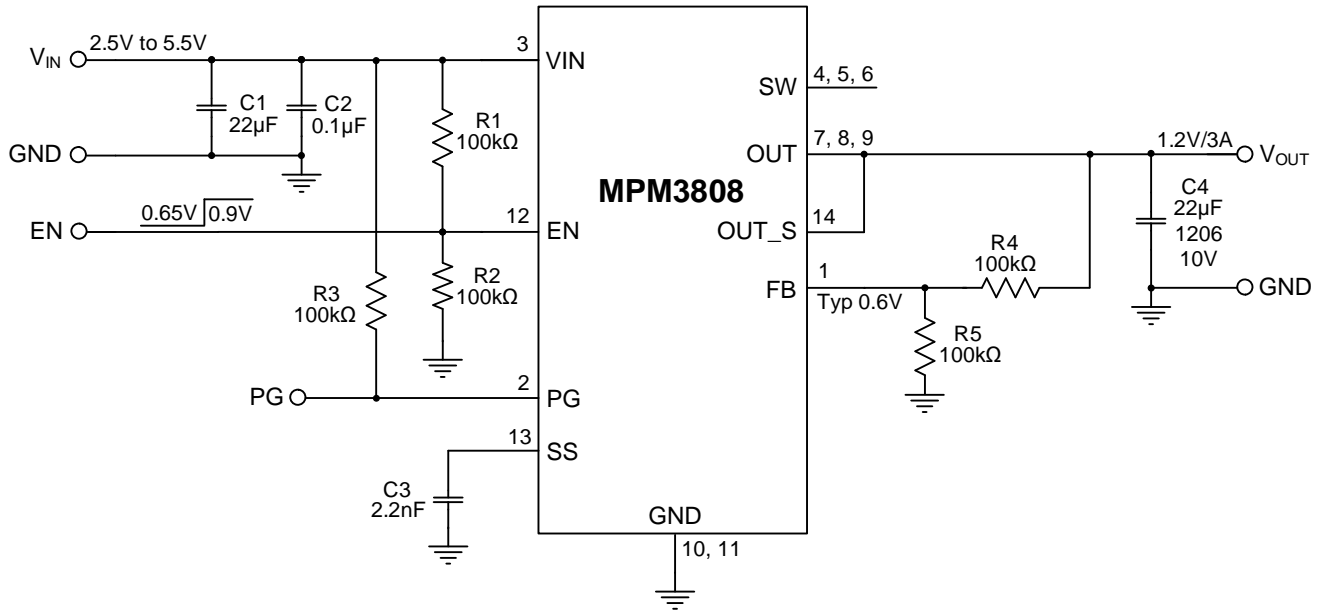


Figure 11: Typical Application (Adjustable Output,  $V_{OUT} = 1.2V$ )

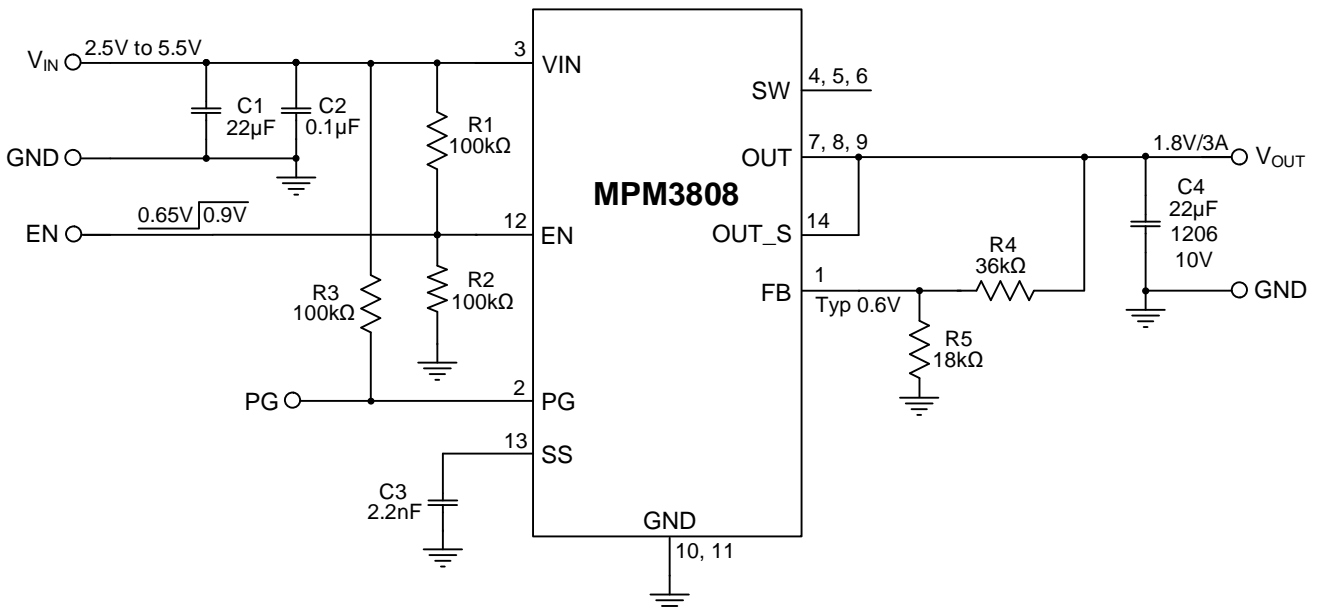


Figure 12: Typical Application (Adjustable Output,  $V_{OUT} = 1.8V$ )

TYPICAL APPLICATION CIRCUITS (continued)

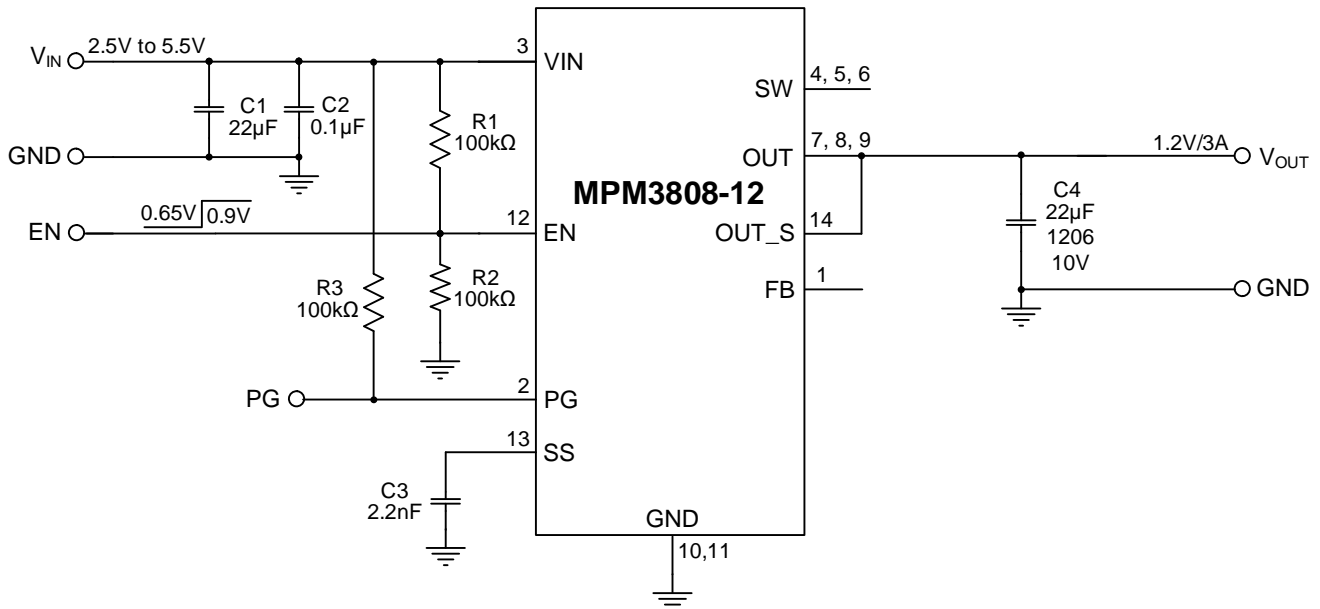


Figure 13: Typical Application (Fixed Output,  $V_{OUT} = 1.2V$ )

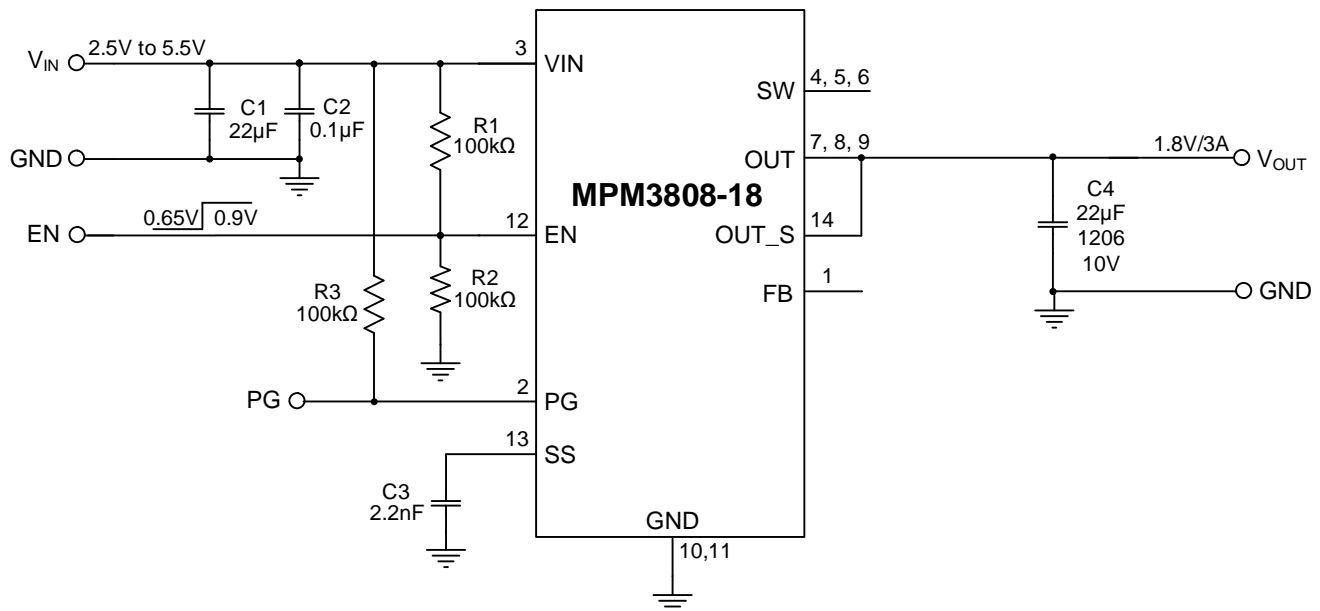
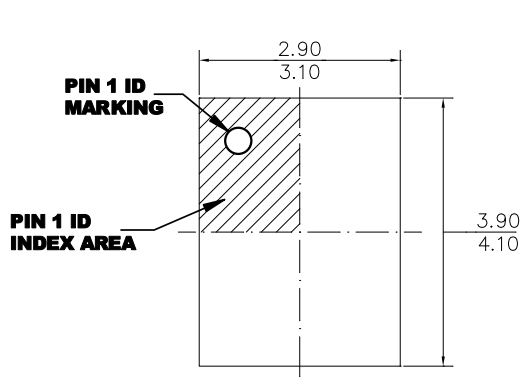


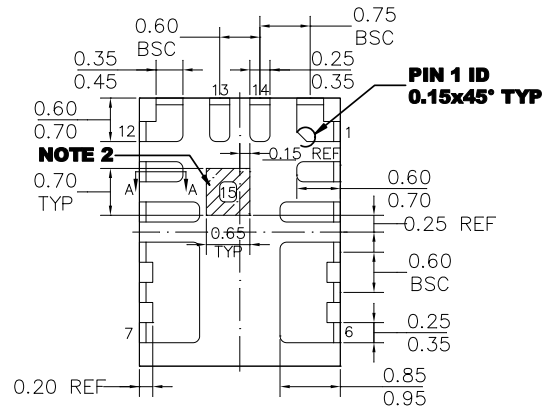
Figure 14: Typical Application (Fixed Output,  $V_{OUT} = 1.8V$ )

## PACKAGE INFORMATION

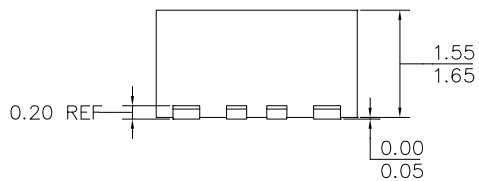
### QFN-15 (3mmx4mmx1.6mm) Wettable Flank



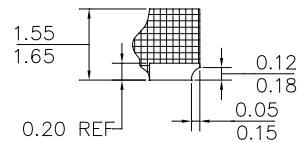
**TOP VIEW**



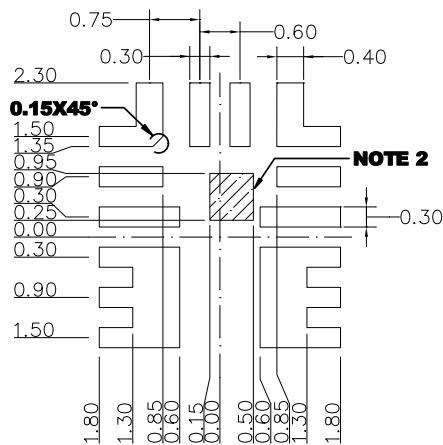
**BOTTOM VIEW**



**SIDE VIEW**



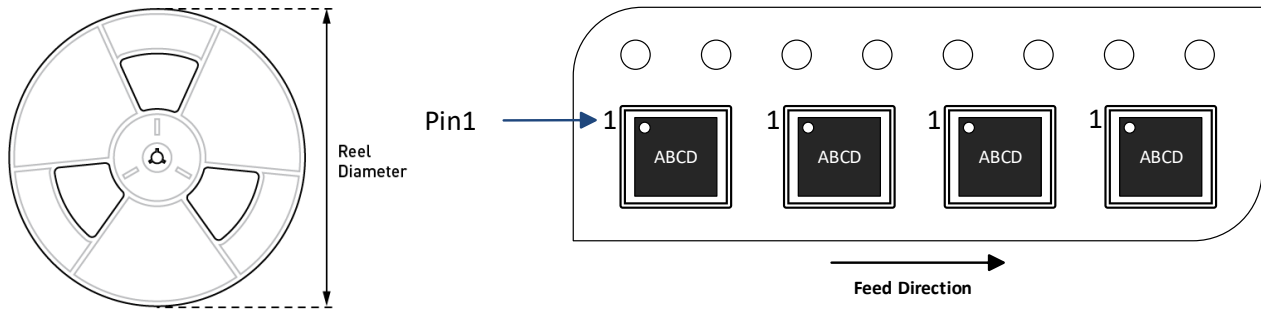
**SECTION A-A**



**RECOMMENDED LAND PATTERN**

**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) SHADED AREA IS THE KEEP-OUT ZONE. ANY PCB METAL TRACE AND VIA ARE NOT ALLOWED TO CONNECT TO THIS AREA ELECTRICALLY OR MECHANICALLY.
- 3) THE LEAD SIDE IS WETTABLE.
- 4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 5) JEDEC REFERENCE IS MO-220.
- 6) DRAWING IS NOT TO SCALE.

**CARRIER INFORMATION**


Part Number	Package Description	Quantity /Reel	Quantity /Tube	Quantity /Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM3808GLE-AEC1-Z	QFN-15 (3mmx4mmx1.6mm)	2500	N/A	N/A	13in	12mm	8mm
MPM3808GLE-12-AEC1-Z							
MPM3808GLE-18-AEC1-Z							