MPM6010

36V, 1.5A, High-Efficiency Module, Synchronous, Step-Down LED Driver with Integrated Inductor AEC-Q100 Qualified

The Future of Analog IC Technology

DESCRIPTION

The MPM6010 is a synchronous, rectified, step-down, LED driver with built-in power MOSFETs, inductor, and two capacitors. The MPM6010 offers a very compact solution with only four external components to achieve 1.5A of continuous output current with excellent load and line regulation over a wide input supply range. The MPM6010 uses synchronous mode operation to achieve high efficiency.

The MPM6010 eliminates design and manufacturing risks while improving the time to market dramatically.

Full protection features include over-current protection (OCP) and thermal shutdown.

The MPM6010 is available in a space-saving QFN-17 (3mmx5mmx1.6mm) package.

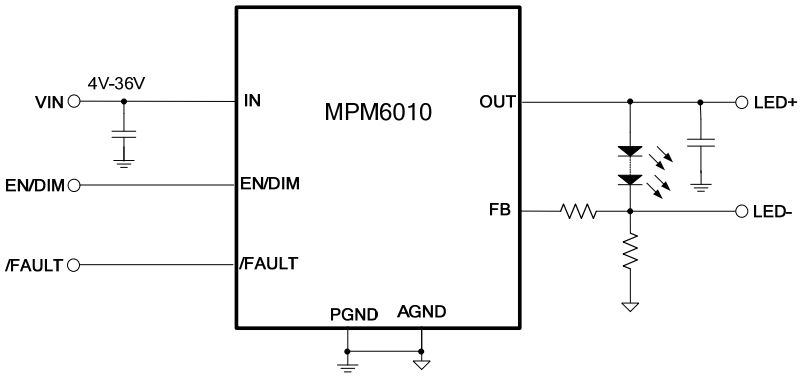
FEATURES

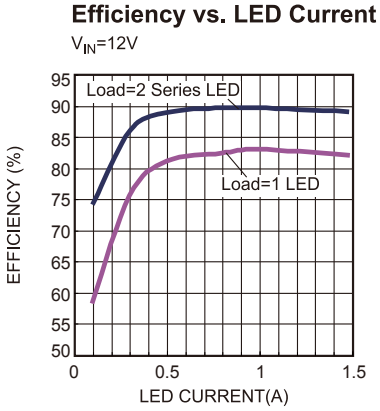
- Complete Switch Mode Power Supply
- Wide 4V to 36V Operating Input Range
- 85mΩ/50mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- High-Efficiency Synchronous Mode Operation
- Default 2.2MHz Switching Frequency
- PWM Dimming (Min 100Hz Dimming Frequency)
- Forced Continuous Conduction Mode (CCM)
- 0.2V Reference Voltage
- Internal Soft Start
- Fault Indication for LED Short, Open, and Thermal Shutdown
- Over-Current Protection (OCP) with Valley-Current Detection
- Thermal Shutdown
- Available in a QFN-17 (3mmx5mmx1.6mm) Package
- Available Wettable Flank
- AEC-Q100 Grade1

APPLICATIONS

- Automotive LED Lighting

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MPM6010GQV	QFN-17 (3mmx5mmx1.6mm)	*See Below*
MPM6010GQV-AEC1	QFN-17 (3mmx5mmx1.6mm)	*See Below*
MPM6010GQVE-AEC1**	QFN-17 (3mmx5mmx1.6mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MPM6010GQV–Z)

** Wettable Flank

TOP MARKING (MPM6010GQV & MPM6010GQV-AEC1)

MPYW
6010
LLL
M

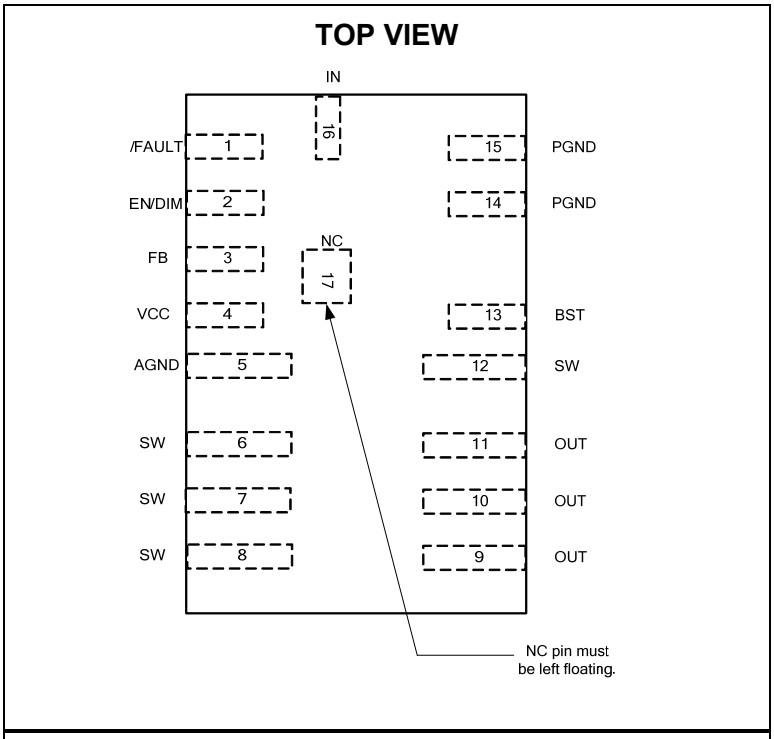
MP: MPS prefix
Y: Year code
W: Week code
6010: First four digits of the part number
LLL: Lot number
M: Module

TOP MARKING (MPM6010GQVE-AEC1)

MPYW
6010
LLL
EM

MP: MPS prefix
Y: Year code
W: Week code
6010: First four digits of the part number
LLL: Lot number
E: Wettable lead flank
M: Module

PACKAGE REFERENCE



QFN-17 (3mmx5mmx1.6mm)

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to 40V
V_{SW}, V_{OUT}.....-0.3V to V_{IN} + 0.3V
V_{BST} ..... V_{SW} + 6V
All other pins ..... -0.3V to 6V (2)
Continuous power dissipation (T_A = +25°C) (3)
..... 2.7W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to 150°C

Recommended Operating Conditions

Supply voltage (V_{IN}) .....4V to 36V
LED current (I_{LED}).....Up to 1.5A
Operating junction temp. (T_J).. -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-17 (3mmx5mmx1.6mm)	46	10 °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) For details on EN/DIM's ABS MAX rating, please refer to the Enable Control section on page 14.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_J = +25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{SHDN}	V_{EN} = 0V		12		μA
Supply current (quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 1V, no switching		0.6	0.8	mA
HS switch on resistance	$HS_{RDS(ON)}$	V_{BST-SW} = 5V		85	150	mΩ
LS switch on resistance	$LS_{RDS(ON)}$	V_{CC} = 5V		50	105	mΩ
Inductor DC resistance	L_{DCR}			75		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 12V			1	μA
Current limit (5)	I_{LIMIT}	Under 40% duty cycle	2.5	4	5.5	A
Reverse current limit				1.2		A
Oscillator frequency	f_{SW}	V_{FB} = 100mV	1800	2200	2600	kHz
Maximum duty cycle	D_{MAX}	V_{FB} = 100mV	80	87		%
Minimum on time (5)	T_{ON_MIN}			46		ns
Feedback voltage	V_{FB}	T_A = +25°C	192	200	208	mV
		T_A = -40°C to +125°C	184	200	216	mV
Feedback current	I_{FB}	V_{FB} = 250mV		30	100	nA
EN/DIM rising threshold	V_{EN_RISING}		1.1	1.45	1.8	V
EN/DIM falling threshold	$V_{EN\_FALLING}$		0.7	1	1.3	V
EN/DIM threshold hysteresis	V_{EN_HYS}			450		mV
EN/DIM input current	I_{EN}	V_{EN} = 2V		5	10	μA
EN/DIM turn-off delay	EN_{Td-off}		10	25	50	ms
V_{IN} under-voltage lockout threshold rising	$INUV_{Vth}$		3.2	3.5	3.8	V
V_{IN} under-voltage lockout threshold hysteresis	$INUV_{HYS}$			400		mV
Over-voltage detection (/FAULT pulled low)	FT_{th-Hi}			140%		V_{FB}
Over-voltage detection hysteresis				20%		V_{FB}
/FAULT delay	FT_{Td}			10		μs
/FAULT sink current capability	V_{FT}	Sink 4mA			0.4	V
/FAULT leakage current	$I_{FT-LEAK}$				100	nA
VCC regulator	V_{CC}	I_{CC} = 0mA	4.6	4.9	5.2	V
VCC load regulation		I_{CC} = 5mA		1.5	4	%
Soft-start time (5)	t_{SS}	I_{LED} = 1.5A, load = 2 series LED, I_{LED} from 10% to 90%		0.9		ms
Thermal shutdown (5)			150	170		°C
Thermal hysteresis (5)				30		°C

NOTE:

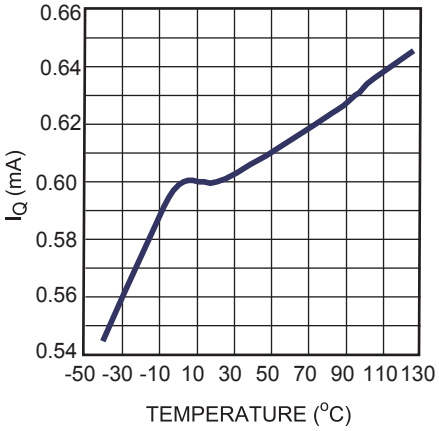
5) Not tested in production and guaranteed by over-temperature correlation.

PIN FUNCTIONS

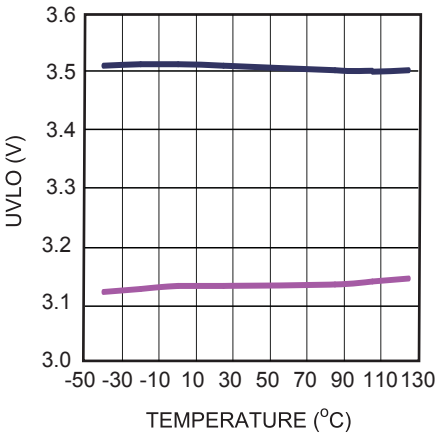
Package Pin #	Name	Description
1	/FAULT	**Fault indicator.** /FAULT is an open drain output. /FAULT is pulled low when the LED is short, open, or when thermal shutdown is occurring.
2	EN/DIM	**Enable/dimming control.** Pull EN/DIM high to enable the MPM6010. Apply a 100Hz to 2kHz external clock to EN/DIM for PWM dimming.
3	FB	**LED current feedback input.**
4	VCC	**Internal 4.9V LDO output.** Internal circuits integrate an LDO output capacitor, so there is no need to add an external capacitor to VCC.
5	AGND	**Analog ground.** AGND is the reference ground of the logic circuit. AGND is connected to PGND internally. There is no need to add external connections to PGND.
6, 7, 8, 12	SW	**Switch output.** Connection is not needed for these SW pins, but a large copper plane is recommended (especially on pin 6, 7, and 8) for better heat sinking.
9, 10, 11	OUT	**Power output.** Connect LED+ to OUT. An output capacitor is needed on OUT.
13	BST	**Bootstrap.** A bootstrap capacitor is integrated internally. External connections are not required on BST.
14, 15	PGND	**Power ground.** PGND is the reference ground of the power device. PGND requires extra care during PCB layout. For best results, connect PGND with copper pours and vias.
16	IN	**Supply voltage.** IN supplies power for the internal MOSFET and regulator. The MPM6010 operates from a +4V to +36V input rail. A low ESR and low-inductance capacitor is required to decouple the input rail. Place the input capacitor very close to IN and connect it with wide PCB traces and multiple vias.
17	NC	**No connection.** NC must be left floating.

TYPICAL CHARACTERISTICS

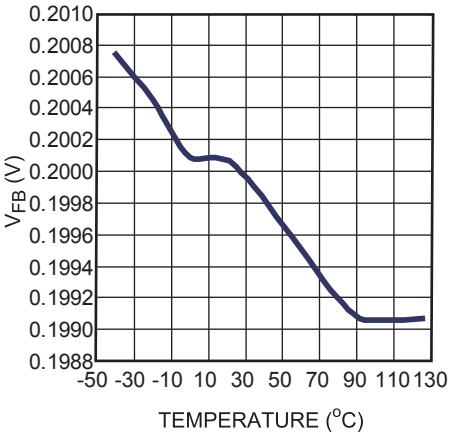
I_Q vs. Temperature



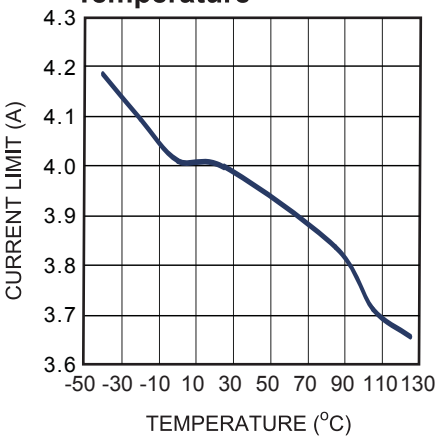
V_{IN} UVLO vs.Temperature



V_{FB} vs. Temperature



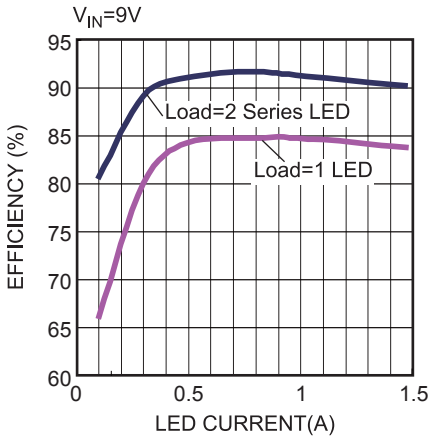
Current Limit vs. Temperature



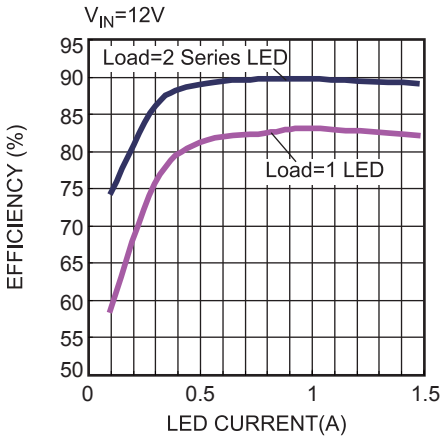
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, Load = 2 series LED, V_{LED+} - V_{LED-} = 2x3.0V @1.5A, F_{SW} = 2.2MHz, T_A = +25°C, unless otherwise noted.

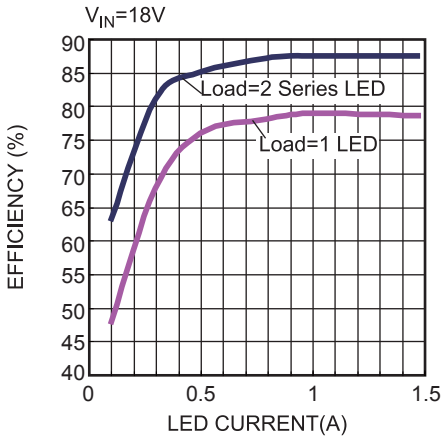
Efficiency vs. LED Current



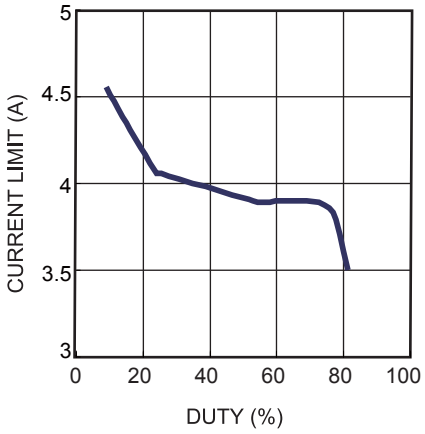
Efficiency vs. LED Current



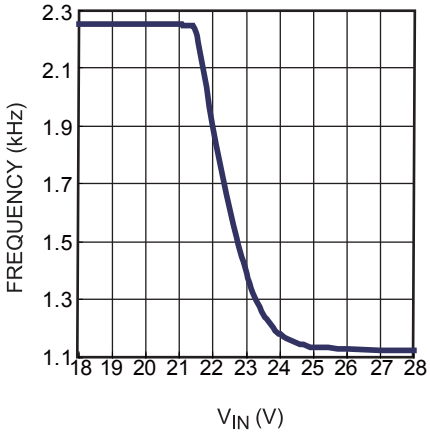
Efficiency vs. LED Current



Current Limit vs.Duty



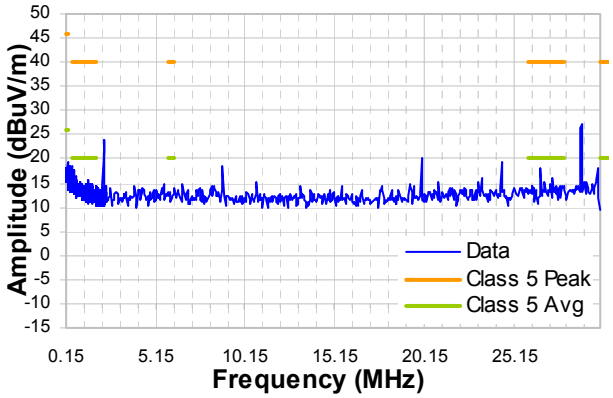
Frequency vs. V_{IN}



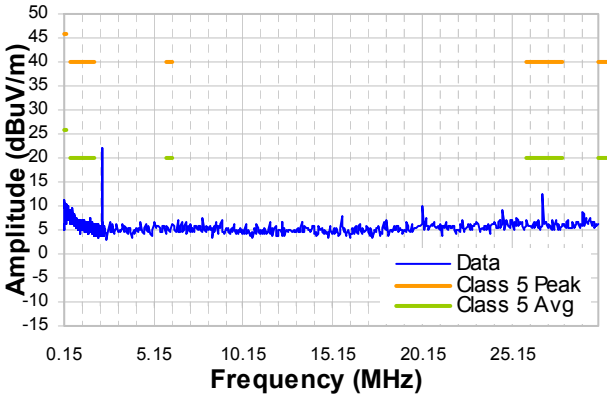
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, Load = 2 series LED, V_{LED+} - V_{LED-} = 2x3.0V @1.5A, I_{LED} = 1.5A, F_{SW} = 2.2MHz, with EMI filters, T_A = +25°C, unless otherwise noted. (6)

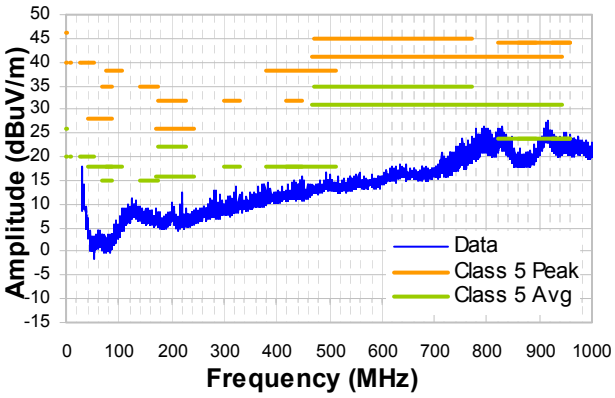
CISPR25 Class 5 Peak Radiated Emissions (150kHz - 30MHz)



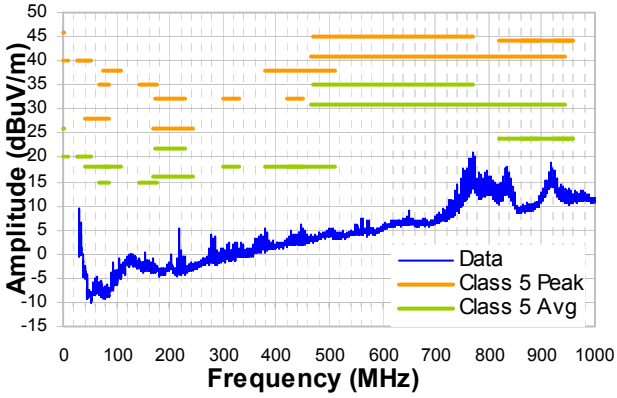
CISPR25 Class 5 Average Radiated Emissions (150kHz - 30MHz)



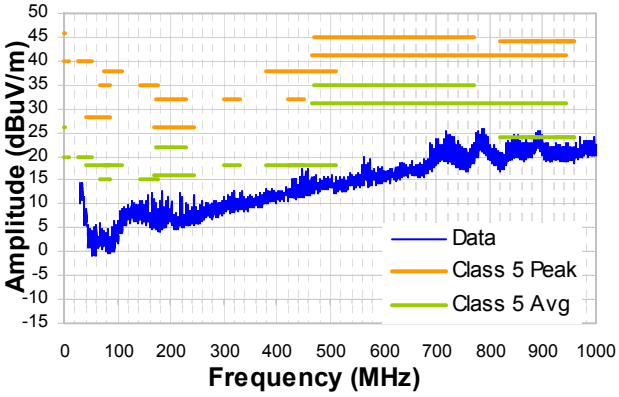
CISPR25 Class 5 Peak Radiated Emissions (Vertical, 30MHz - 1GHz)



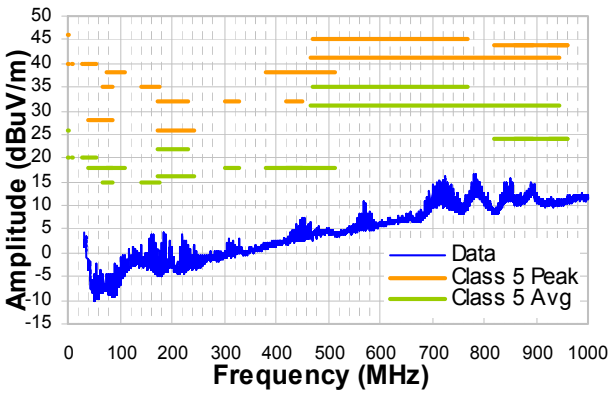
CISPR25 Class 5 Average Radiated Emissions (Vertical, 30MHz - 1GHz)



CISPR25 Class 5 Peak Radiated Emissions (Horizontal, 30MHz - 1GHz)



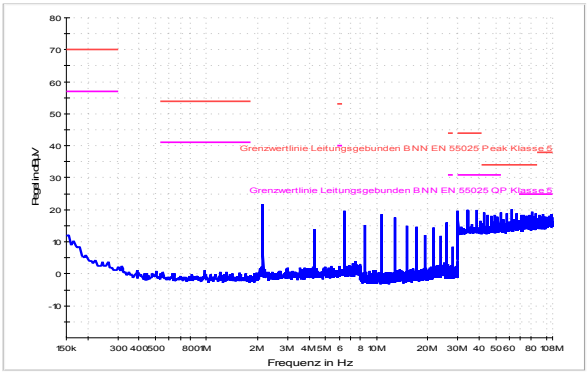
CISPR25 Class 5 Average Radiated Emissions (Horizontal, 30MHz - 1GHz)



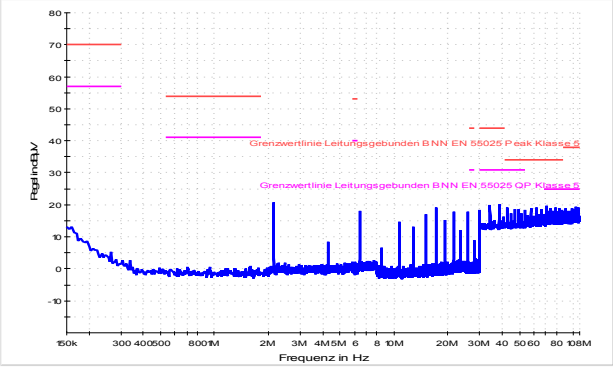
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, Load = 2 series LED, V_{LED+} - V_{LED-} = 2x3.0V @1.5A, I_{LED} = 1.5A, F_{SW} = 2.2MHz, with EMI filters, T_A = +25°C, unless otherwise noted. (6)

CISPR25 Class 5 Peak Conducted Emissions (150kHz -108MHz)



CISPR25 Class 5 Average Conducted Emissions (150kHz - 108MHz)



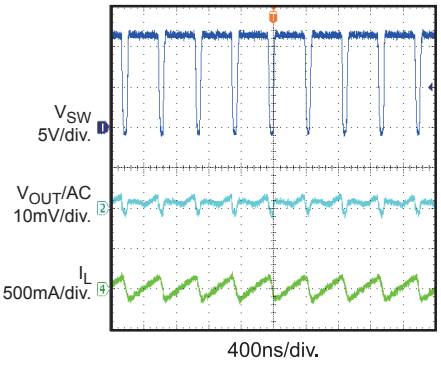
NOTE:

6) The EMC test results are based on the application circuit with EMI filters as shown in Figure 9.

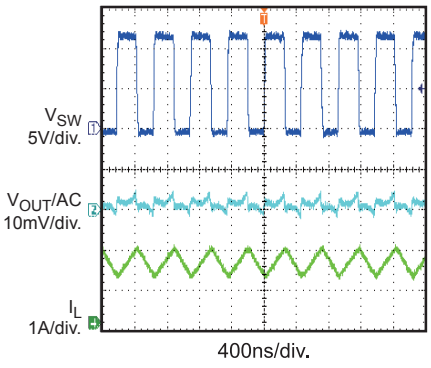
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, Load = 2 series LED, V_{LED+} - V_{LED-} = 2x3.0V @1.5A, F_{SW} = 2.2MHz, T_A = +25°C, unless otherwise noted.

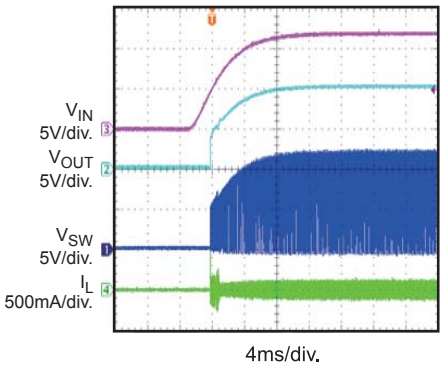
Steady State
I_{LED} = 0A



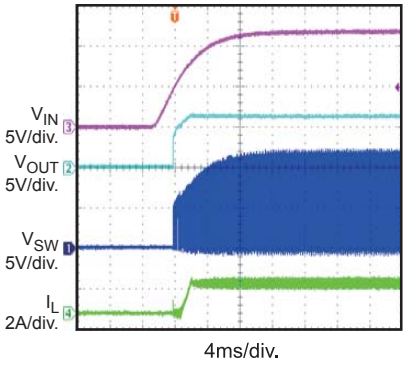
Steady State
I_{LED} = 1.5A



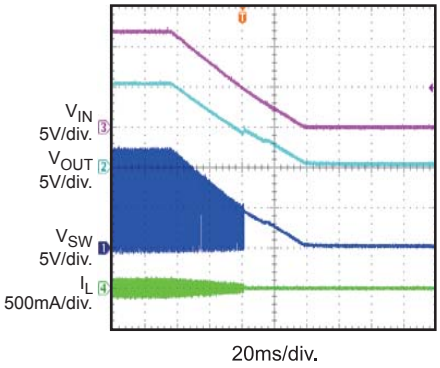
Start-Up through V_{IN}
I_{LED} = 0A



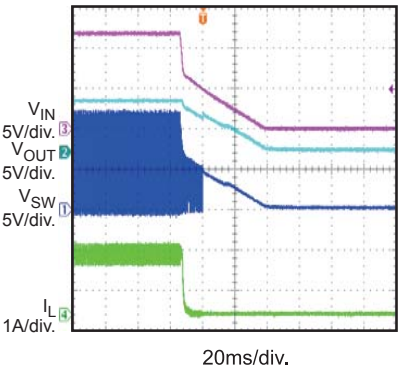
Start-Up through V_{IN}
I_{LED} = 1.5A



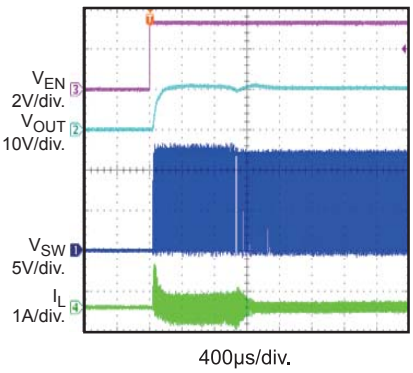
Shutdown through V_{IN}
I_{LED} = 0A



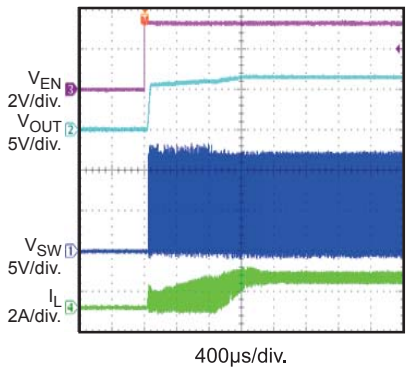
Shutdown through V_{IN}
I_{LED} = 1.5A



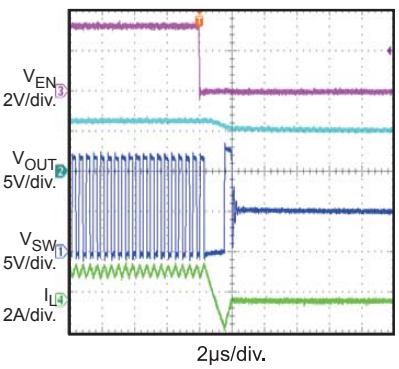
Start-Up through EN/DIM
I_{LED} = 0A



Start-Up through EN/DIM
I_{LED} = 1.5A



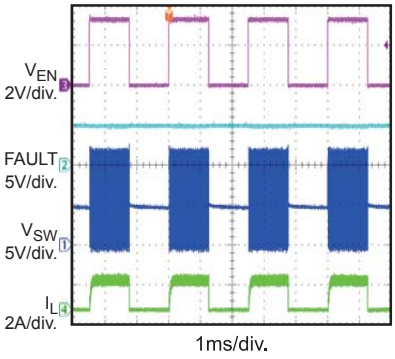
Shutdown through EN/DIM
I_{LED} = 1.5A



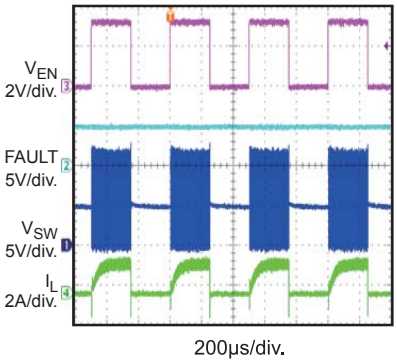
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, Load = 2 series LED, V_{LED+} - V_{LED-} = 2x3.0V @1.5A, F_{SW} = 2.2MHz, T_A = +25°C, unless otherwise noted.

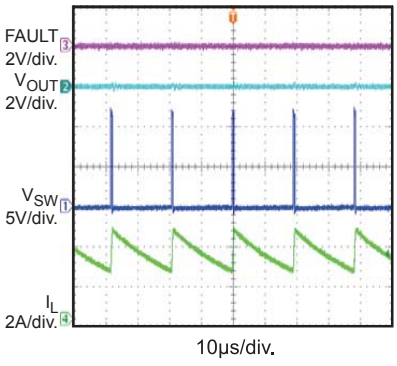
PWM Dimming
400Hz



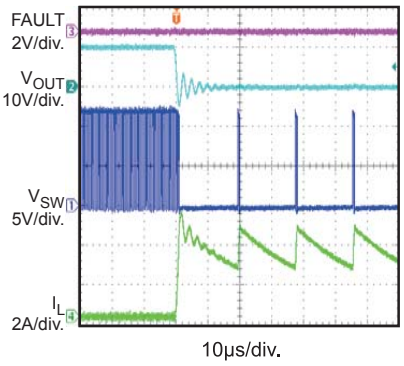
PWM Dimming
2kHz



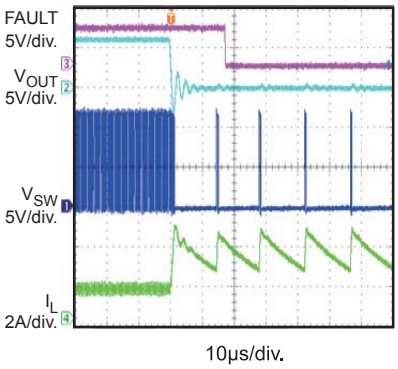
LED+ Short to GND Steady State



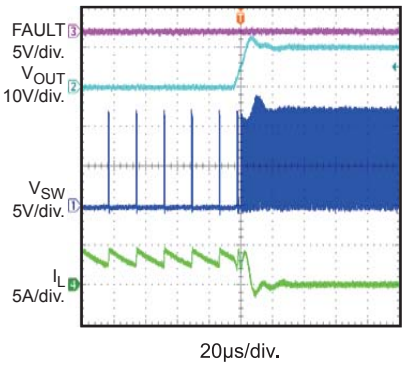
LED+ Short to GND Entry
I_{LED} = 0A



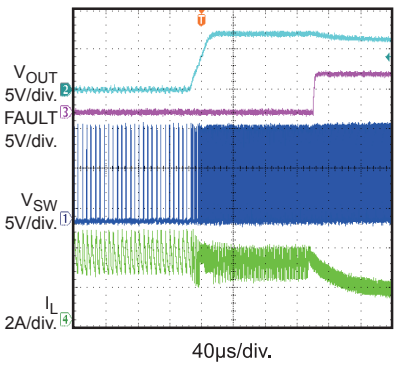
LED+ Short to GND Entry
I_{LED} = 1.5A



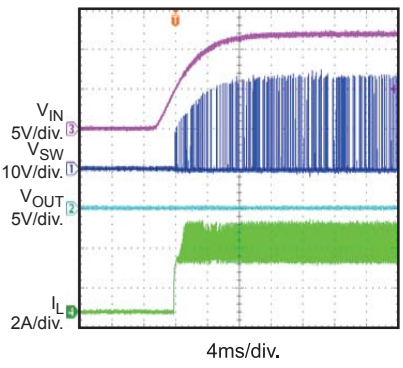
LED+ Short to GND Recovery
I_{LED} = 0A



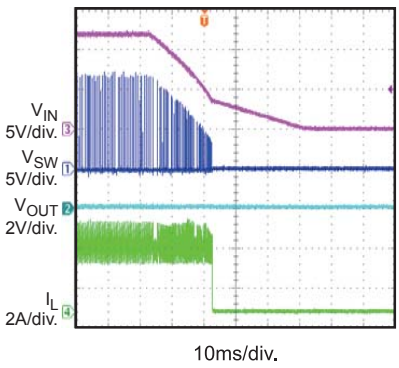
LED+ Short to GND Recovery
I_{LED} = 1.5A



LED+ Short to GND Input Power On



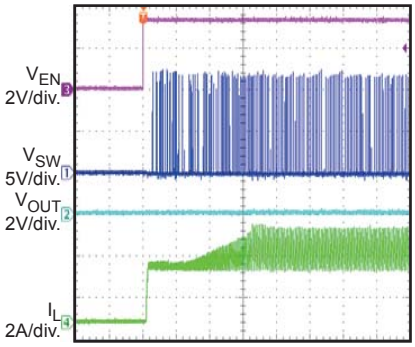
LED+ Short to GND Input Power Off



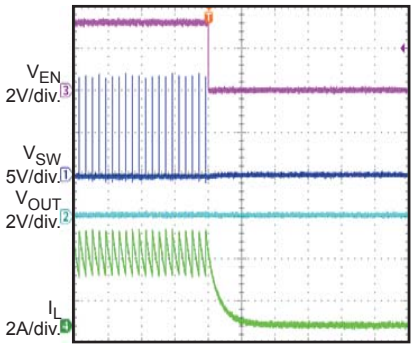
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, Load = 2 series LED, V_{LED+} - V_{LED-} = 2x3.0V @1.5A, F_{SW} = 2.2MHz, T_A = +25°C, unless otherwise noted.

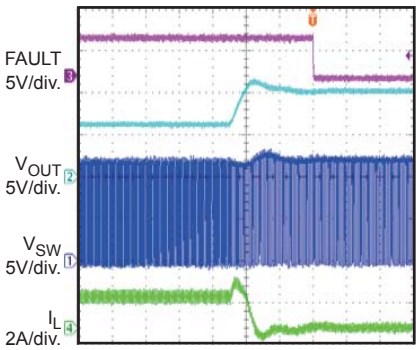
LED+ Short to GND EN/DIM On



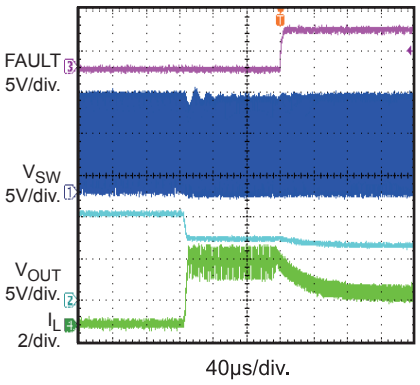
LED+ Short to GND EN/DIM Off



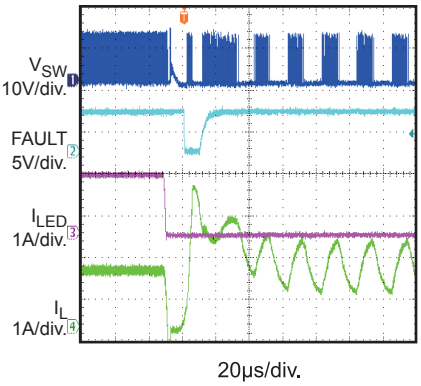
LED Open Entry



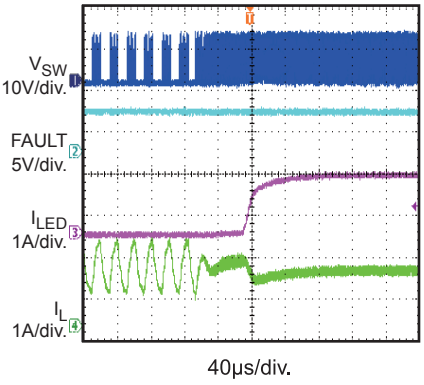
LED Open Recovery



LED+ and LED- Short Entry



LED+ and LED- Short Recovery



BLOCK DIAGRAM

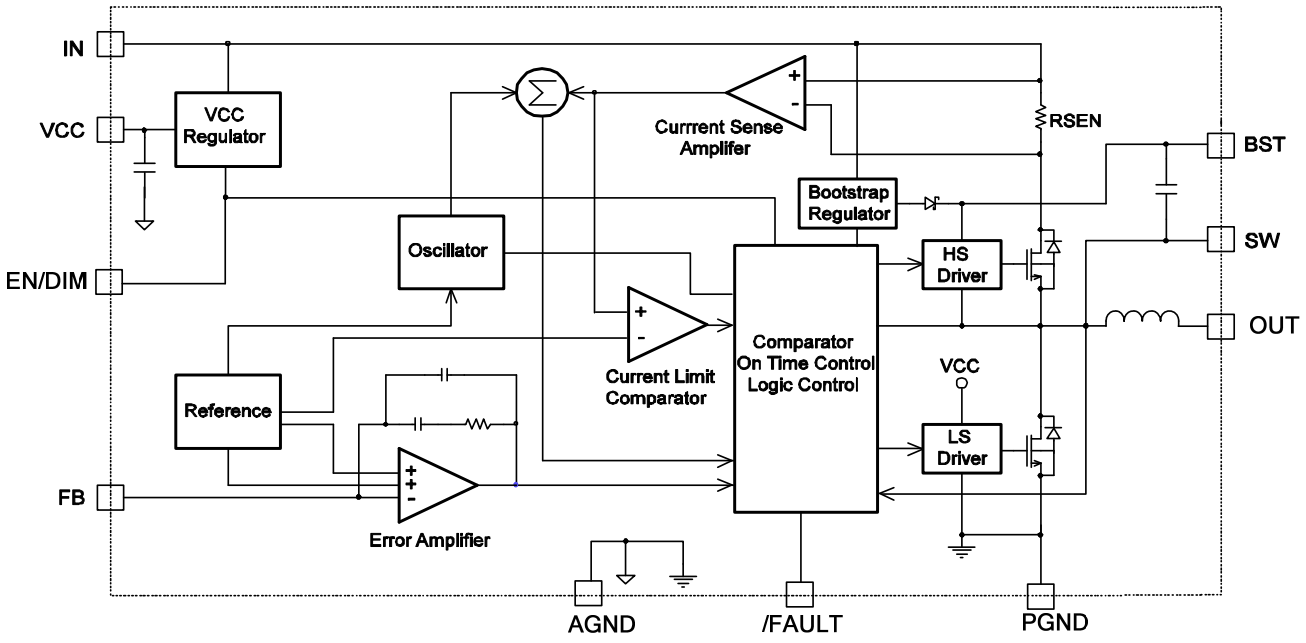


Figure 1: Functional Block Diagram

OPERATION

The MPM6010 is a high-frequency, synchronous, rectified, step-down, switch-mode, white LED driver with built-in power MOSFETs, integrated inductor, and two capacitors. The MPM6010 offers a very compact solution that achieves 1.5A of continuous output current with excellent load and line regulation over a 4V to 36V input supply range.

The MPM6010 operates in a fixed-frequency, peak-current-control mode to regulate the output current. An internal clock initiates a pulse-width modulation (PWM) cycle. The integrated high-side power MOSFET (HS-FET) turns on and remains on until its current reaches the value set by the COMP voltage (V_{COMP}). When the power switch is off, it remains off until the next clock cycle starts. If the current in the power MOSFET does not reach the current value set by V_{COMP} within 87% of one PWM period, the power MOSFET is forced off.

Internal Regulator

A 4.9V internal regulator powers most of the internal circuitries. This regulator takes V_{IN} as the input and operates in the full V_{IN} range. When V_{IN} exceeds 4.9V, the output of the regulator is in full regulation. When V_{IN} is less than 4.9V, the output decreases following V_{IN}. The MPM6010 integrates an internal decoupling capacitor, so there is no need to add an external VCC output capacitor.

CCM Operation

The MPM6010 uses continuous conduction mode (CCM) to ensure that the part works with fixed frequency from a no-load to full-load range. The advantage of CCM is the controllable frequency and lower output ripple at light load.

Frequency Foldback

The MPM6010 enters frequency foldback when the input voltage is higher than about 21V. The frequency decreases to half the nominal value and changes to 1.1MHz.

Frequency foldback also occurs during soft start and short-circuit protection.

Error Amplifier (EA)

The error amplifier compares the FB voltage to the internal 0.2V reference (V_{REF}) and outputs a current proportional to the difference between the two. This output current then charges or discharges the internal compensation network to form V_{COMP}, which controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 3.5V, while its falling threshold is about 3.1V.

Enable Control (EN/DIM)

EN/DIM is a control pin that turns the regulator on and off. Drive EN/DIM high to turn on the regulator; drive EN/DIM low to turn off the regulator. An internal resistor from EN/DIM to GND allows EN/DIM to be floated to shut down the MPM6010.

EN/DIM is clamped internally using a 6.5V series Zener diode (see Figure 2). Connecting EN/DIM through a pull-up resistor to V_{IN} limits the EN/DIM input current to less than 100μA.

For example, with 12V connected to V_{IN}, $R_{PULLUP} \geq (12V - 6.5V) \div 100\mu A = 55k\Omega$.

Connecting EN/DIM to a voltage source directly without a pull-up resistor requires limiting the amplitude of the voltage source to ≤6V to prevent damage to the Zener diode.

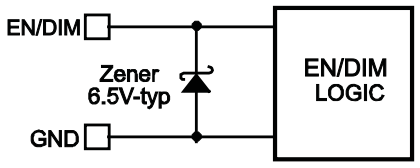


Figure 2: 6.5V Zener Diode Connection

Drive EN/DIM low for more than 25ms to shut down the IC.

PWM Dimming

Apply an external, 100Hz to 2kHz, PWM waveform to EN/DIM for PWM dimming. The average LED current is proportional to the PWM duty. The minimum amplitude of the PWM signal is 1.8V. If a dimming signal is applied before the chip starts up, the on time of the dimming signal must be longer than 2ms to ensure that the soft start is finished so the output current can be built. If the dimming signal is applied after the soft start is finished, the 2ms limit is not required.

Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (V_{SS}). When V_{SS} is lower than the internal reference (V_{REF}), V_{SS} overrides V_{REF}, so the error amplifier uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the error amplifier uses V_{REF} as the reference.

Fault Indicator (/FAULT)

The MPM6010 has fault indication (/FAULT). /FAULT is the open drain of a MOSFET and should be connected to VCC or another voltage source through a resistor (e.g. 100kΩ). /FAULT is pulled high during normal operation. LED short, open, or thermal shutdown pull /FAULT down to indicate a fault status.

Over-Current Protection (OCP)

The MPM6010 has cycle-by-cycle, peak-current-limit protection with valley-current detection. The inductor current is monitored during the HS-FET on state. If the inductor current exceeds the current limit value set by the COMP high-clamp voltage, the HS-FET turns off immediately. Then the low-side MOSFET (LS-FET) turns on to discharge the energy, and the inductor current decreases. The HS-FET remains off unless the inductor valley current is lower than a certain current threshold (the valley current limit), even though the internal clock pulses high. If the inductor current does not drop below the valley current limit when the internal clock pulses high, the HS-FET misses the clock, and the switching frequency decreases to half the nominal value.

Both the peak and valley current limits assist in keeping the inductor current from running away during an overload or short-circuit condition.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the die temperatures exceeds 170°C, the entire chip shuts down. When the temperature drops below its lower threshold (typically 140°C), the chip is enabled again.

Floating Driver and Bootstrap Charging

An internal bootstrap capacitor powers the floating power MOSFET driver. A dedicated internal regulator charges and regulates the bootstrap capacitor voltage to ~5V (see Figure 3). When the voltage between the BST and SW nodes drops below regulation, a PMOS pass transistor connected from V_{IN} to BST turns on. The charging current path is from V_{IN} to BST to SW. The external circuit should provide enough voltage headroom to facilitate charging. As long as V_{IN} is higher than SW significantly, the bootstrap capacitor remains charged. When the HS-FET is on, $V_{IN} \approx V_{SW}$, so the bootstrap capacitor cannot be charged. When the LS-FET is on, $V_{IN} - V_{SW}$ reaches its maximum for fast charging. When there is no inductor current, $V_{SW} = V_{OUT}$, so the difference between V_{IN} and V_{OUT} can charge the bootstrap capacitor. The floating driver has its own UVLO protection with a rising threshold of 2.2V and hysteresis of 150mV.

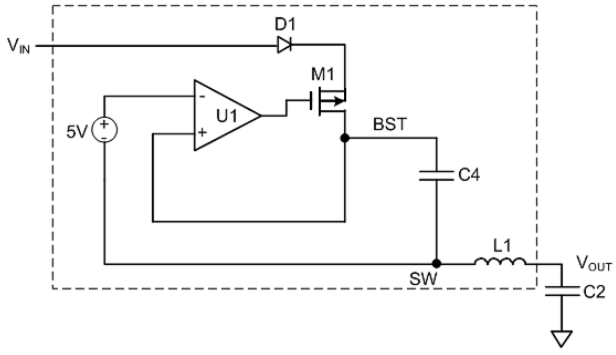


Figure 3: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both V_{IN} and EN/DIM exceed their thresholds, the chip starts up. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries. Three events can shut down the chip: V_{IN} low, EN/DIM low, and thermal shutdown. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

APPLICATION INFORMATION

Setting the Output Current

The output current is set by the external resistor (R_{FB}) (see Figure 4).

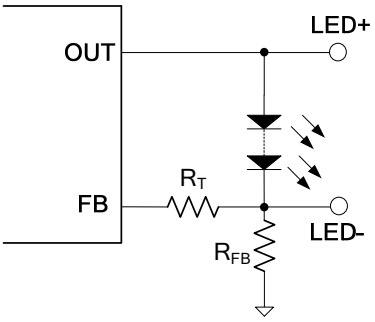


Figure 4: Feedback Network

The feedback voltage is 0.2V. Calculate I_{LED} with Equation (1):

$$I_{LED} = \frac{0.2V}{R_{FB}} \quad (1)$$

R_T is used to set the loop bandwidth. The lower R_T is, the higher the bandwidth. However, a high bandwidth may cause insufficient phase margin, resulting in loop instability. A proper value of R_T is needed to make a trade-off between bandwidth and phase margin. Table 1 lists the recommended feedback resistor and R_T values for common outputs with a 1- or 2-series LED.

Table 1: Resistor Selection for Common Outputs

I_{LED} (A)	R_{FB} (mΩ)	R_T (kΩ)
0.5	400 (1%)	200 (1%)
1	200 (1%)	150 (1%)
1.5	133 (1%)	100 (1%)

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, use a 4.7µF to 10µF capacitor. It is strongly recommended to use another lower-value capacitor (e.g. 0.1µF) in a small package (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to IN and GND as possible.

Since C_{IN} absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (2):

$$I_{CIN} = I_{LED} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (2)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (3):

$$I_{CIN} = \frac{I_{LED}}{2} \quad (3)$$

For simplification, choose an input capacitor with an RMS current rating greater than half the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality, ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated with Equation (4):

$$\Delta V_{IN} = \frac{I_{LED}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (5):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \cdot (1 - \frac{V_{OUT}}{V_{IN}}) \cdot (R_{ESR} + \frac{1}{8 f_{SW} \times C_{OUT}}) \quad (5)$$

Where L is the internal integrated inductor value (2.2µH), and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (7)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPM6010 can be optimized for a wide range of capacitance and ESR values.

V_{IN} UVLO Setting

The MPM6010 has an internal, fixed, under-voltage lockout (UVLO) threshold. The rising threshold is about 3.5V, while the falling threshold is about 3.1V. For applications that require a higher UVLO point, an external resistor divider can be added between IN and EN/DIM to achieve a higher equivalent UVLO threshold (see Figure 5).

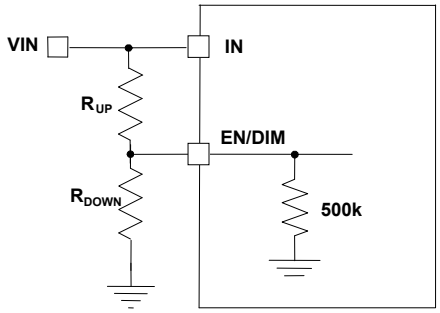


Figure 5: Adjustable UVLO Using EN/DIM Divider

The UVLO threshold can be calculated with Equation (8) and Equation (9):

$$INUV_{RISING} = (1 + \frac{R_{UP}}{500k // R_{DOWN}}) \times V_{EN\_RISING} \quad (8)$$

$$INUV_{FALLING} = (1 + \frac{R_{UP}}{500k // R_{DOWN}}) \times V_{EN\_FALLING} \quad (9)$$

Where V_{EN_RISING} = 1.45V, and $V_{EN\_FALLING}$ = 1V.

When choosing R_{UP}, ensure that it is large enough to limit the current flow into EN/DIM below 100μA.

External Bootstrap Diode

An external bootstrap diode can enhance the efficiency of the regulator when the duty cycle is high (>65%). A power supply between 2.5V and 5V can be used to power the external bootstrap diode. VCC or V_{OUT} is recommended for this power supply in the circuit (see Figure 6).

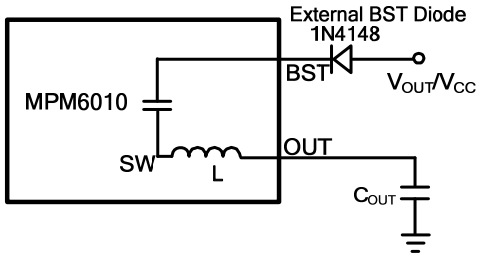


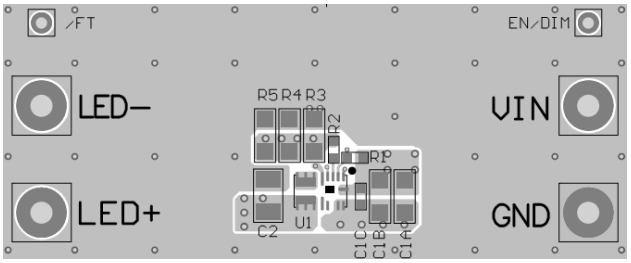
Figure 6: Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148.

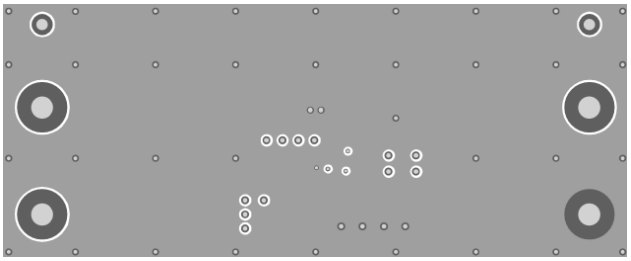
PCB Layout Guidelines [7]

Efficient PCB layout, especially of the input capacitor placement, is critical for stable operation. For best results, refer to Figure 7 and follow the guidelines below. A four-layer layout is strongly recommended to achieve better thermal performance.

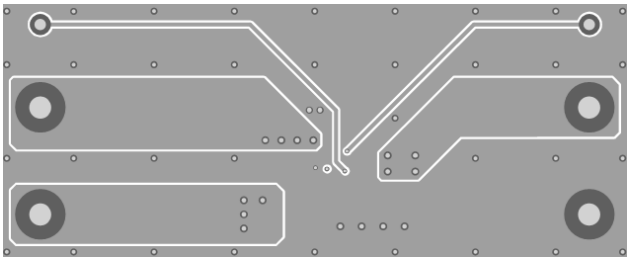
1. Use a large ground plane on PGND. If the bottom layer is a ground plane, add vias near PGND.
2. Ensure that the high-current paths at PGND and IN have short, direct, and wide traces.
3. Place the ceramic input capacitor, especially the small package (0603) input bypass capacitor as close to IN and PGND as possible to minimize high-frequency noise.
4. Keep the connection of the input capacitor and IN as short and wide as possible.
5. Place the feedback resistors close to the chip to ensure the trace which connects to FB is as short as possible.
6. Use multiple vias to connect the power planes to the internal layers.



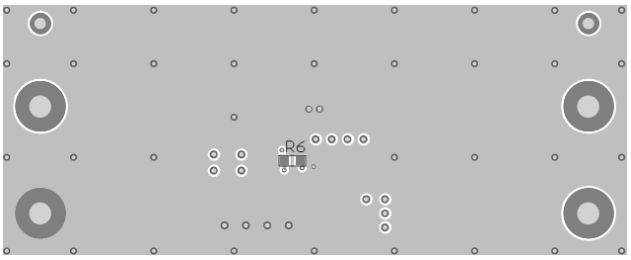
Top Layer



Inner Layer 1



Inner Layer 2



Bottom Layer

Figure 7: Recommended PCB Layout

NOTE:

7) The recommended layout is based on Figure 8.

TYPICAL APPLICATION CIRCUITS

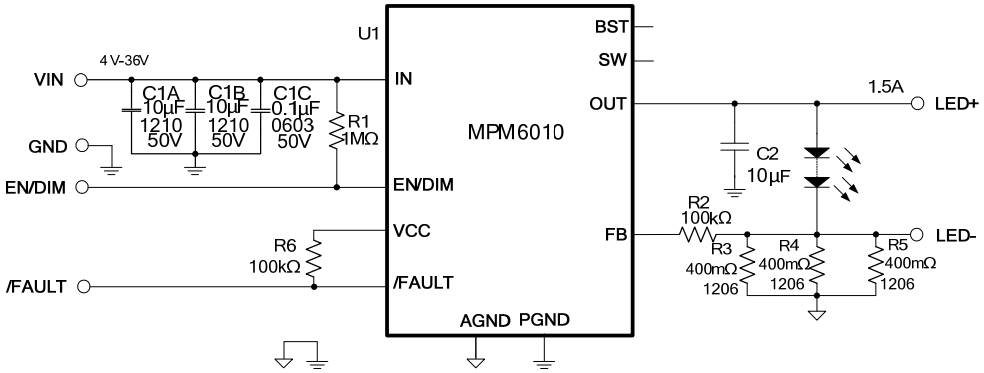


Figure 8: Typical Application Circuit for I_{LED} = 1.5A

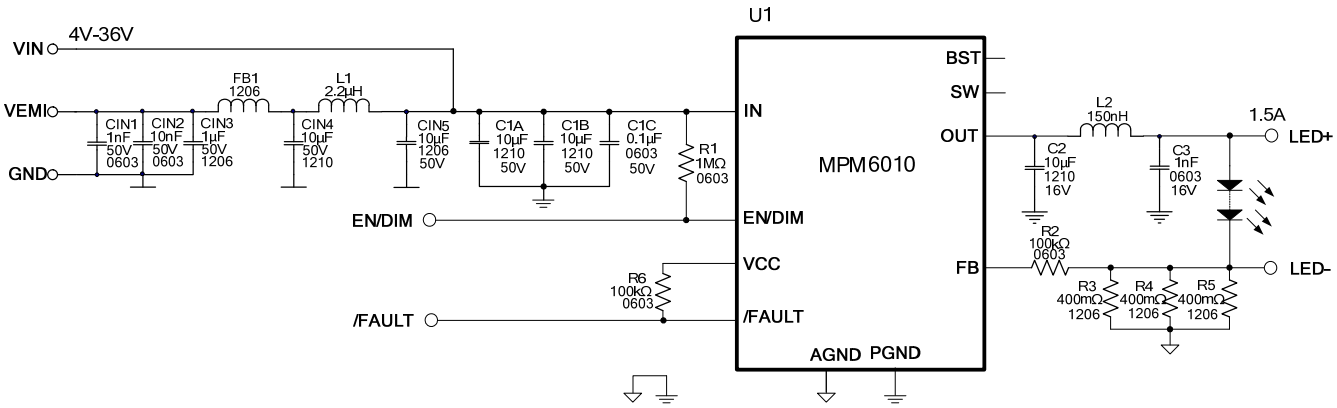
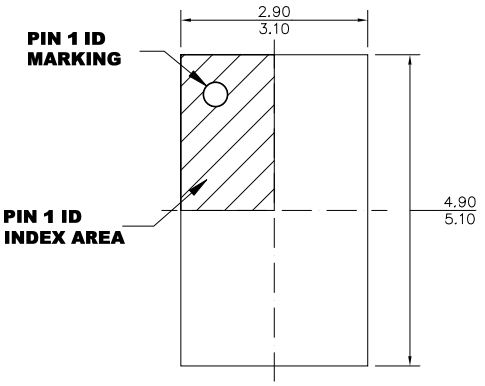


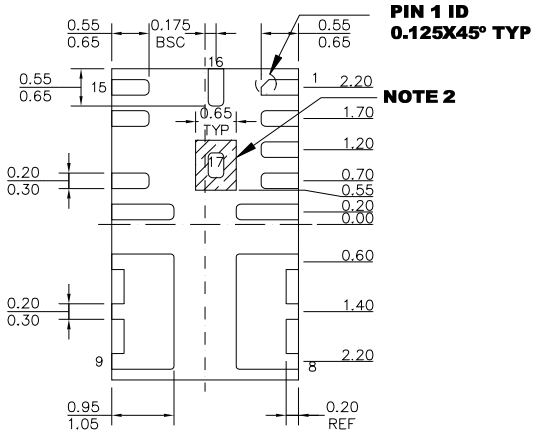
Figure 9: Application Circuit with EMI Filters for I_{LED} = 1.5A

PACKAGE INFORMATION

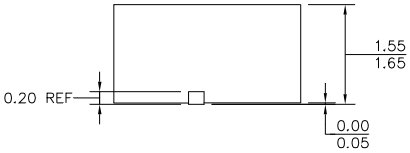
QFN-17 (3mmx5mmx1.6mm)
Non-Wettable Flank



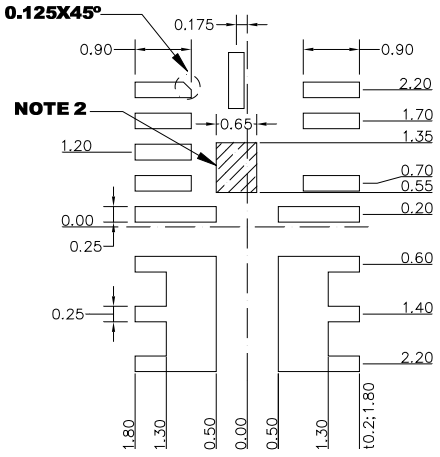
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) SHADED AREA IS THE KEEP-OUT ZONE. ANY PCB METAL TRACE AND VIA ARE NOT ALLOWED TO CONNECT TO THIS AREA ELECTRICALLY OR MECHANICALLY.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.