MPQ1530

Triple Output Step-Up Plus Linear Regulators for TFT Bias AEC-Q100 Qualified

DESCRIPTION

The MPQ1530 combines a triple output step-up converter with linear regulators to provide a complete DC/DC solution. It is designed to power TFT LCD panels from a regulated 3.3V or 5V supply.

This device integrates a 1.4MHz fixed-frequency step-up converter with positive and negative linear regulators. The step-up converter switch node drives two charge pumps, which supply powers to their respective linear regulators. The positive and negative linear regulator inputs can withstand up to 38V and down to -20V, respectively.

A single on/off control enables all 3 outputs. The outputs are internally sequenced at startup for ease of use. An internal soft-start prevents input overload at startup. Cycle-by-cycle current limiting reduces component stress.

The MPQ1530 is available in a tiny 3x3mm, 16-pin QFN package.

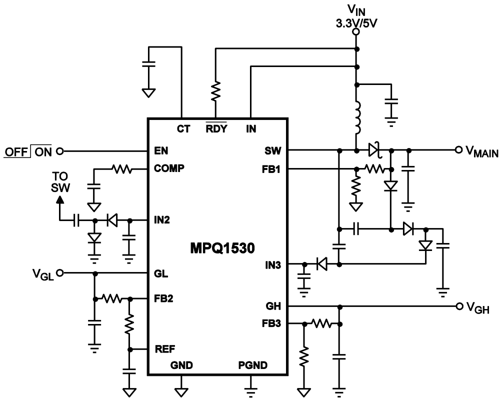
FEATURES

- Guaranteed Industrial/Automotive Temp Range Limits
- 2.7 to 5.5V Operating Input Range
- 2.8A Switch Current Limit
- 3 Outputs In a Single Package
    - Step-Up Converter up to 22V
    - Positive 20mA Linear Regulator
    - Negative 20mA Linear Regulator
- 250mΩ Internal Power MOSFET Switch
- Up to 95% Efficiency
- 1.4MHz Fixed Frequency
- Internal Power-On Sequencing
- Adjustable Soft-Start/Fault Timer
- Cycle-by-Cycle Over Current Protection
- Under Voltage Lockout
- Ready Flag
- 16-Pin QFN (3x3mm) Package
- Available in AEC-Q100 Qualified Grade 1

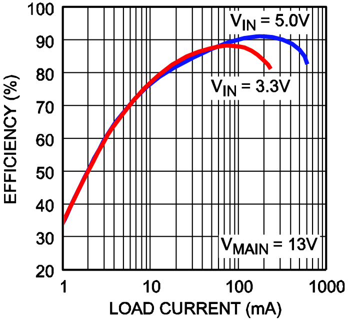
APPLICATIONS

- TFT LCD Displays
- Portable DVD Players
- Tablet PCs
- Car Navigation Displays

TYPICAL APPLICATION



Efficiency vs Load Current
(Step-Up Converter Only)



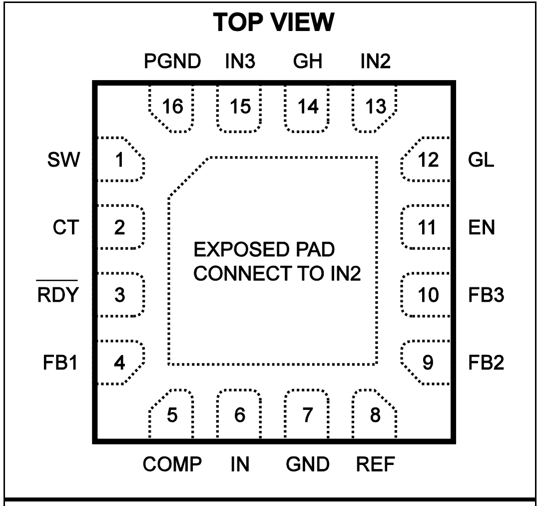
ORDERING INFORMATION

Part Number	Package	Top Marking
MPQ1530DQ*	QFN16 (3x3mm)	B8
MPQ1530DQ-AEC1**		

* For Tape & Reel, add suffix -Z (e.g. MPQ1530DQ-Z).
For RoHS Compliant Packaging, add suffix -LF (e.g. MPQ1530DQ-LF-Z)

** For Tape & Reel, add suffix -Z (e.g. MPQ1530DQ-AEC1-Z).
For RoHS Compliant Packaging, add suffix -LF (e.g. MPQ1530DQ-AEC1-LF-Z)

PACKAGE REFERENCE



QFN16

ABSOLUTE MAXIMUM RATINGS (1)

IN Supply Voltage	–0.3V to +6V
SW Voltage	–0.3V to +25V
IN2, GL Voltage	+0.3V to –25V
IN3, GH Voltage	–0.3V to +40V
IN2 to IN3 Voltage	–0.3V to +60V
All Other Pins	–0.3V to +6V

Continuous Power Dissipation (T_A = +25°C) (2)

QFN16 (3 x 3mm)	2.1W
Junction Temperature	125°C
Lead Temperature	260°C
Storage Temperature	–65°C to +150°C

ESD Susceptibility (3)

HBM (Human Body Mode)

- IN3: CLASS 1A;
- GH: CLASS 1B;
- GL: CLASS 1C;
- Other Pins: CLASS 2;

CDM (Charged Device Mode)

- All Pins: CLASS IV;

Recommended Operating Conditions (4)

Input Voltage	2.7V to 5.5V
Main Output Voltage	V_{IN} to 22V
IN2, GL Voltage	0V to –20V
IN3, GH Voltage	0V to 38V
Operating Junction Temp. (T_J)	-40°C to +125°C

Thermal Resistance (5)	θ_{JA}	θ_{JC}	
QFN16 (3 x 3mm)	60	12	°C/W

Notes:

1) Absolute maximum are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Devices are ESD sensitive. Handle with precaution.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on approximately 1” square of 1 oz copper.

ELECTRICAL CHARACTERISTICS (6)

V_{IN} = 5V, T_J = -40°C to +125°C, Typical value are at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Voltage Range	V_{IN}		2.7		5.5	V
IN Undervoltage Lockout Threshold	V_{UVLO}	IN Rising	2.25		2.65	V
IN Undervoltage Lockout Hysteresis				100		mV
IN Shutdown Current		$V_{EN} \leq 0.3V$		0.5	1	μA
IN Quiescent Current		V_{EN} > 2V, V_{FB1} = 1.4V		1.3	1.6	mA
EN Input High Voltage	$V_{EN\ HIGH}$	EN Rising	1.6			V
EN Input Low Voltage					0.3	V
EN Hysteresis				250		mV
EN Input Bias Current					1	μA
Oscillator						
Switching Frequency	f_{SW}		1	1.4		MHz
Maximum Duty Cycle	D_M		85	90		%
Soft Start Period		C_{CT} = 10nF		6		ms
Regulator #2 Turn-On/Turn-Off Delay				3		μs
		C_{CT} = 10nF		6		ms
Error Amplifier						
Error Amplifier Voltage Gain(6)	Av_{EA}			400		V/V
Error Amplifier Transconductance	Gm_{EA}			1000		μA/V
COMP Maximum Output Current				±100		μA
FB1, FB3 Regulation Voltage			1.22	1.25	1.28	V
FB2 Regulation Voltage			–25	0	+25	mV
FB1, FB3 Input Bias Current		V_{FB1} = V_{FB3} = 1.25V		±100		nA
FB2 Input Bias Current		V_{FB2} = 0V		±100		nA
Reference (REF)						
REF Regulation Voltage		I_{REF} = 50μA	1.22	1.25	1.28	V
REF Load Regulation		0μA < I_{REF} < 200μA		1	1.2	%
Output Switch (SW)						
SW On Resistance(6)		V_{IN} = 5V		250		mΩ
		V_{IN} = 3V		400		mΩ
SW Current Limit	I_{LIM}	T_J=+25°C	2.5	3.6		A
		T_J=-40°C to +125°C	2.2	3.6		
SW Leakage Current		V_{SW} = 22V		0.5	1	μA
GL Dropout Voltage (7)		V_{GL} = –10V, I_{GL} = –20mA		0.1	0.3	V
GH Dropout Voltage (7)		V_{GH} = 20V, I_{GH} = 20mA		0.45	1	V
GL Leakage Current		V_{IN2} = –15V, V_{GL} = GND			1	μA
GH Leakage Current		V_{IN3} = 25V, V_{GH} = GND			1	μA
Thermal Shutdown(6)				160		°C

Notes:

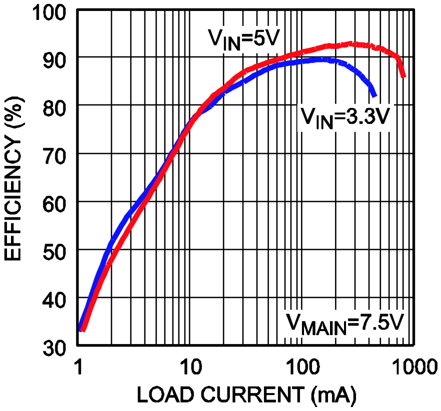
6) Not production tested.

7) Dropout Voltage is the input to output differential at which the circuit ceases to regulate against further reduction in input voltage.

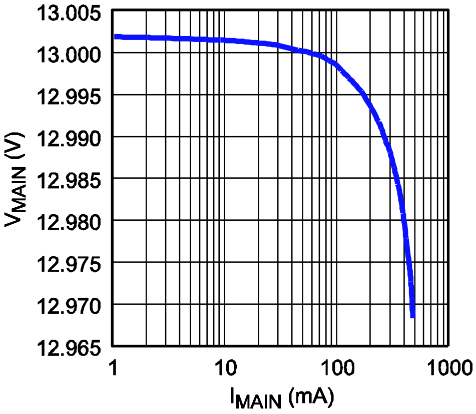
TYPICAL PERFORMANCE CHARACTERISTICS

Circuit of Figure 3, V_{IN} = 5V, V_{MAIN} = 13V, I_{MAIN} = 200mA, V_{GL} = -8.5V, I_{GL} = 10mA, V_{GH} = 27V, I_{GH} = 10mA, T_A = +25°C, unless otherwise noted.

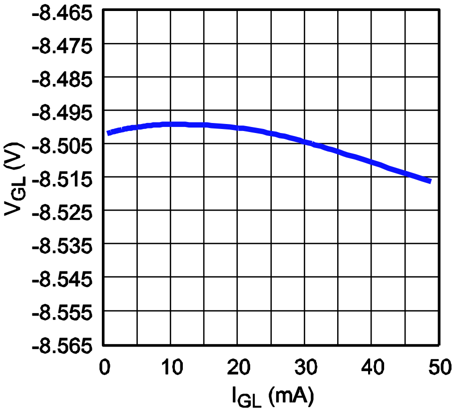
Efficiency vs Load Current
(Step-Up Converter Only)



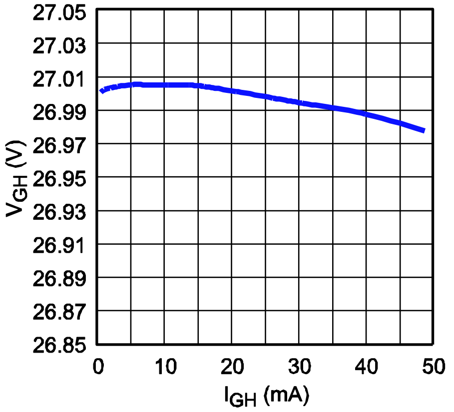
Step-Up Converter Load Regulation



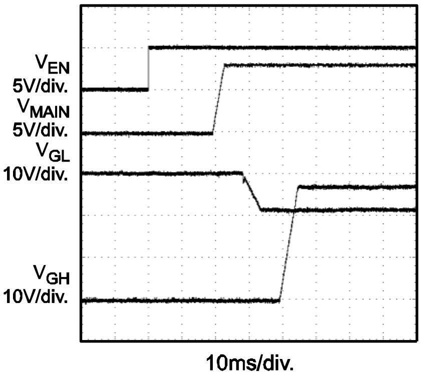
Negative Linear Regulator Load Regulation



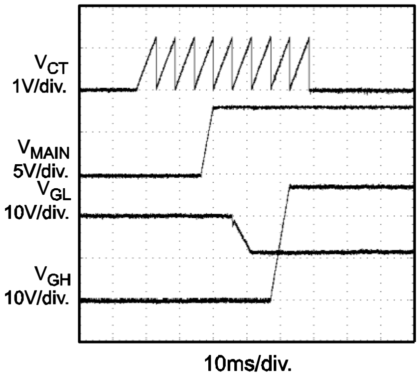
Positive Linear Regulator Load Regulation



Power-On Sequence



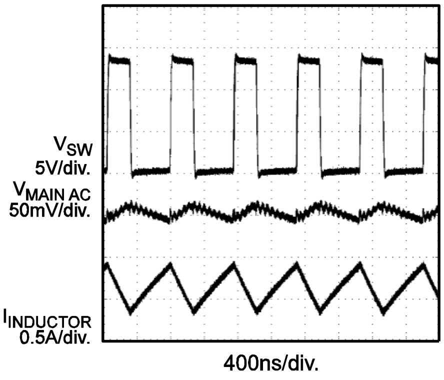
Power-On Sequence



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

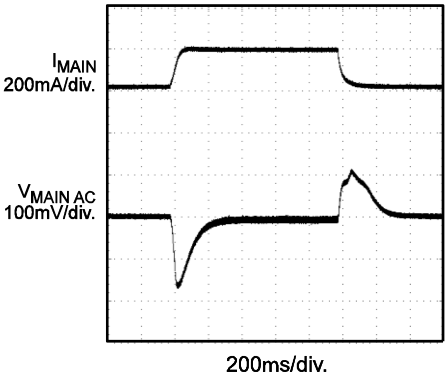
Circuit of Figure 3, V_{IN} = 5V, V_{MAIN} = 13V, I_{MAIN} = 200mA, V_{GL} = -8.5V, I_{GL} = 10mA, V_{GH} = 27V, I_{GH} = 10mA, T_A = +25°C, unless otherwise noted.

Normal Operation



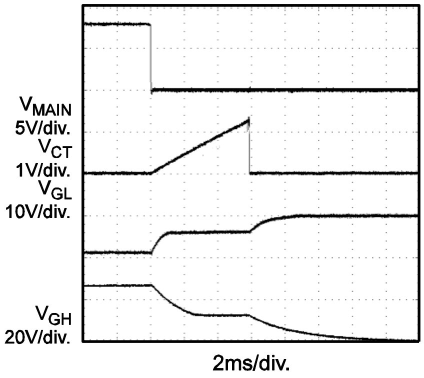
Load Transient on V_{MAIN}

I_{MAIN} = 20mA - 200mA Step

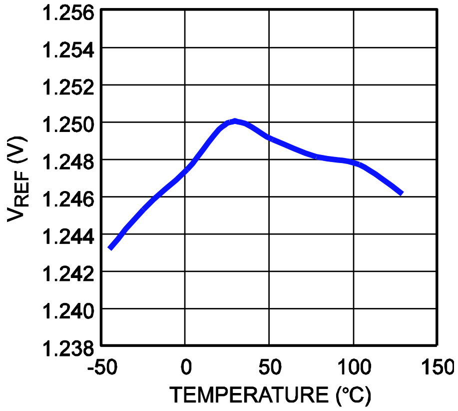


Fault Timer

V_{MAIN} Shorted to V_{IN}

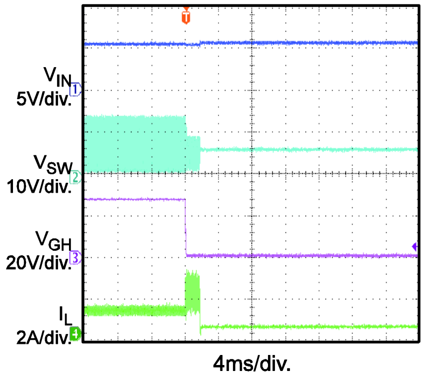


Reference Voltage vs Temperature

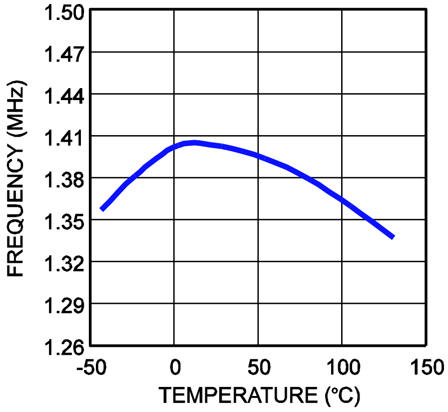


Short Protection for Main Output

V_{IN} =5.5V, I_{MAIN} =0.35A, I_{GH} =I_{GL}=20mA



Oscillator Frequency vs Temperature



PIN FUNCTIONS

QFN Pin #	Name	Description
1	SW	Step-Up Converter Power Switch Node. Connect an inductor between the input source and SW, and connect a rectifier from SW to the main output to complete the step-up converter. SW is the drain of the internal 250mΩ N-Channel MOSFET switch.
2	CT	Timing Capacitor for Power Supply Soft-Start and Power-On Sequencing. A capacitor from CT to GND controls the soft-start and sequencing turn-on delay periods. See Power-On Sequencing and Start Up Timing Diagram.
3	$\overline{\text{RDY}}$	Regulators Not Ready. During startup $\overline{\text{RDY}}$ will be left high. Once the turn-on sequence is complete, this pin will be pulled low if all FB voltages exceed 80% of their specified thresholds. After all regulators are turned-on, a fault in any regulator that causes the respective FB voltage to fall below 80% of its threshold will cause $\overline{\text{RDY}}$ to go high after approximately 15μs. If the fault persists for more than approximately 6ms (for C_{CT}=10nF), the entire chip will shut down. See Fault Sensing and Timer.
4	FB1	Step-Up Converter Feedback Input. FB1 is the inverting input of the internal error amplifier. Connect a resistive voltage divider from the output of the step-up converter to FB1 to set the step-up converter output voltage.
5	COMP	Step-Up Converter Compensation Node. COMP is the output of the error amplifier. Connect a series RC network to compensate the regulation control loop of the step-up converter.
6	IN	Internal Power Input. IN supplies the power to the MPQ1530. Bypass IN to PGND with a 10μF or greater capacitor.
7	GND	Signal Ground.
8	REF	Reference Output. REF is the 1.25V reference voltage output. Bypass REF to GND with a 0.1μF or greater capacitor. Connect REF to the low-side resistor of the negative linear regulator feedback string.
9	FB2	Negative Linear Regulator Feedback Input. Connect the FB2 feedback resistor string between GL and REF to set the negative linear regulator output voltage. FB2 regulation threshold is GND.
10	FB3	Positive Linear Regulator Feedback Input. Connect the FB3 feedback resistor string between GH and GND to set the positive linear regulator output voltage. FB3 regulation threshold is 1.25V.
11	EN	On/Off Control Input. Drive EN high to turn on the MPQ1530, drive EN low to turn it off. For automatic startup, connect EN to IN. Once the MPQ1530 is turned on, it sequences the outputs on (See Power-On Sequencing). When turned off, all outputs are immediately disabled.
12	GL	Negative Linear Regulator Output. GL is the output of the negative linear regulator. GL can supply up to 20mA to the load. Bypass GL to GND with a 1μF or greater, low-ESR, ceramic capacitor.
13	IN2	Negative Linear Regulator Input. IN2 is the input of the negative linear regulator. Drive IN2 with an inverting charge pump powered from SW. IN2 can go as low as -20V. For QFN package, connect the exposed pad to IN2 pin.
14	GH	Positive Linear Regulator Output. GH is the output of the positive linear regulator. GH can supply as much as 20mA to the load. Bypass GH to GND with a 1μF or greater, low-ESR, ceramic capacitor.
15	IN3	Positive Linear Regulator Input. IN3 is the input to the positive linear regulator. Drive IN3 with a doubling, tripling, or quadrupling charge pump from SW. IN3 voltage can go as high as 38V.
16	PGND	Power Ground. PGND is the source of the internal 250mΩ N-Channel MOSFET switch. Connect PGND to GND as close to the MPQ1530 as possible.
Pad	Exposed pad	No internal electrical connections. Solder it to the lowest potential (IN2 pin) plane to reduce thermal resistance.

BLOCK DIAGRAM

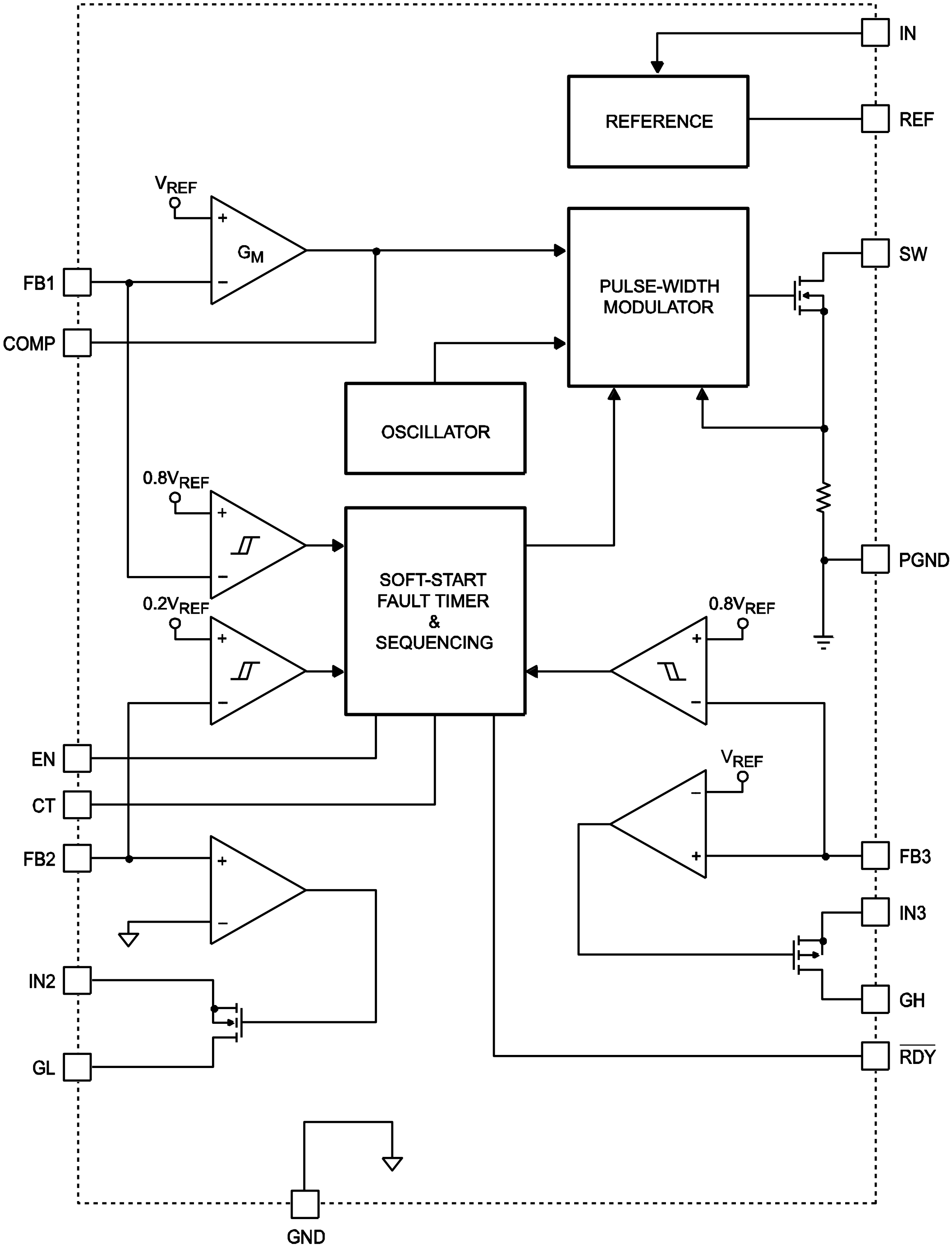


Figure 1—Functional Block Diagram

OPERATION

The MPQ1530 is a step-up converter with two integrated linear regulators to power TFT LCD panels. Typically the linear regulators are powered from charge-pumps driven from the switch node (SW). The user can set the positive charge-pump to be a doubler, tripler, or quadrupler to achieve the required linear regulator input voltage for the selected output voltage. Typically the negative charge-pump is configured as a 1x inverter.

Step-Up Converter

The step-up, fixed-frequency, 1.4MHz converter employs a current-mode control architecture that maximizes loop bandwidth to provide fast-transient responses needed for TFT LCD drivers. High switching frequency allows for smaller inductors and capacitors minimizing board space and thickness.

Linear Regulators

The positive linear regulator (GH) uses a P-Channel pass element to drop the input voltage down to the regulated output voltage. The feedback of the positive linear regulator is a conventional error amplifier with the regulation threshold at 1.25V.

The negative linear regulator (GL) uses a N-Channel pass element to raise the negative input voltage up to the regulated output voltage. The feedback threshold for the negative linear regulator is ground. The resistor string goes from REF (1.25V) to FB2 and from FB2 to GL to set the negative output voltage.

The difference between the voltage at IN3 and the voltage at IN2 is limited to 60V abs. max.

Fault Sensing and Timer

Each of the 3 outputs has an internal comparator that monitors its respective output voltage by measuring the voltage at its respective FB input. When any FB input indicates that the output voltage is below approximately 80% of the correct regulation voltage, the fault timer enables and the $\overline{\text{RDY}}$ pin goes high.

The fault timer uses the same CT capacitor as the soft-start sequencer. If any fault persists to the end of the fault timer (One CT cycle is 6ms for a 10nF capacitor), all outputs are disabled. Once the outputs are shut down due to the fault timer, the MPQ1530 must be re-enabled by either cycling EN or by cycling the input power.

If the fault persists for less than the fault timer period, $\overline{\text{RDY}}$ will be pulled low and the part will function as though no fault has occurred.

Power-On Sequencing and Soft-Start

The MPQ1530 automatically sequences its outputs at startup. When EN goes from low to high, or if EN is held high and the input voltage IN rises above the under-voltage lockout threshold, the outputs turn on in the following sequence:

1. Step-up Converter
2. Negative Linear Regulator (GL)
3. Positive Linear Regulator (GH)

Each output turns on with a soft-start voltage ramp. The soft-start ramp period is set by the timing capacitor connected between CT and GND. A 10nF capacitor at CT sets the soft-start ramp period to 6ms. The timing diagram is shown in Figure 2.

After the MPQ1530 is enabled, the power-on reset spans three periods of the CT ramp. First the step-up converter is powered up with reference to the CT ramp and allowed one period of the CT ramp to settle. Next the negative linear regulator (GL) is soft-started by ramping REF, which coincides with the CT ramp, and also allowed one CT ramp period to settle.

The positive linear regulator (GH) is then soft-started and allowed to settle in one period of CT ramp. Nine periods of the CT ramp have occurred since the chip enabled. If all outputs are in regulation (>80%), the CT will stop ramping and be held at ground.

The $\overline{RDY}$ pin will be pulled down to an active low. If any output remains below regulation (<80%) before and through the nine CT periods, $\overline{RDY}$ will remain high and CT will begin its fault timer pulse.

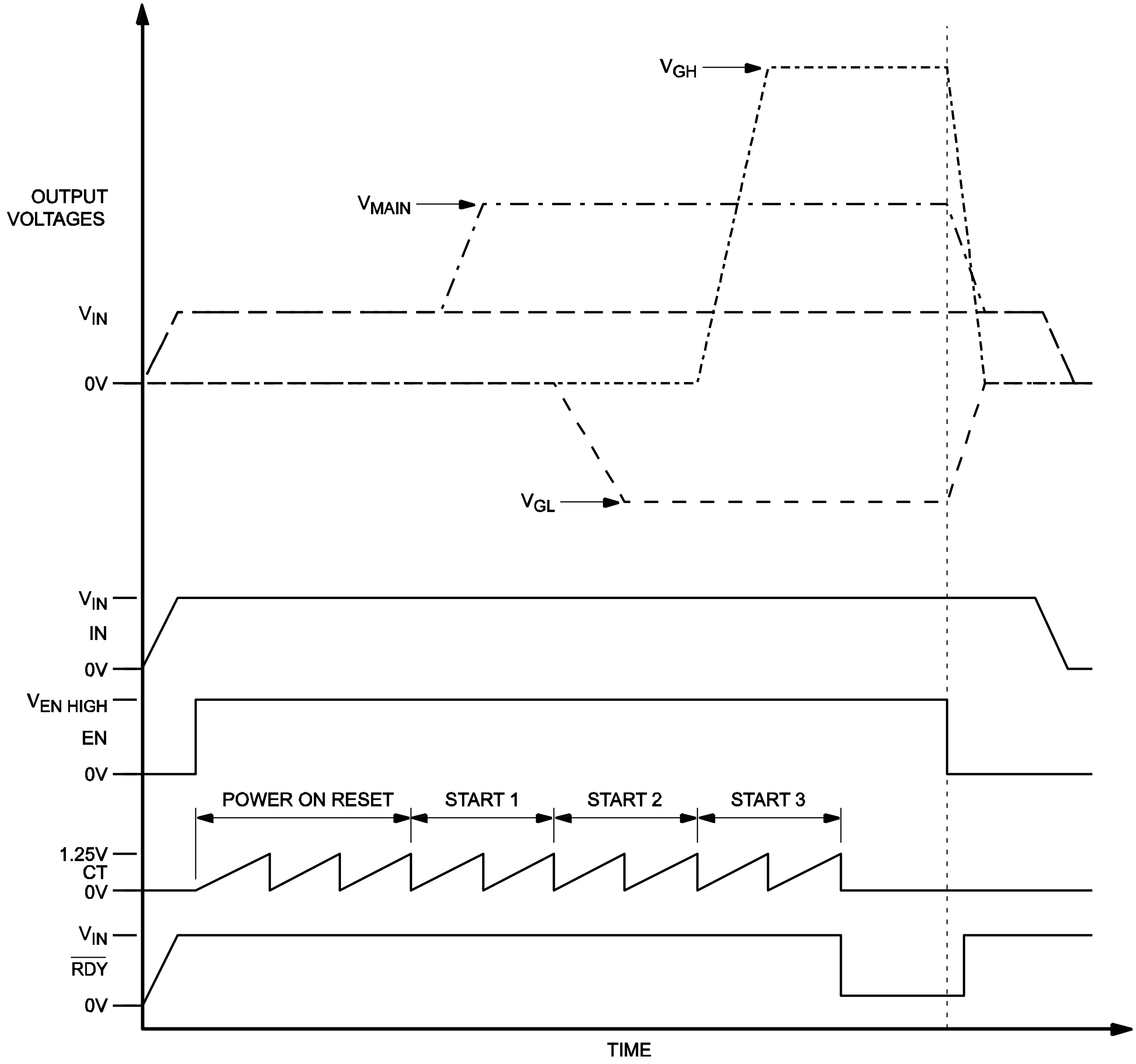


Figure 2—Startup Timing Diagram

APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltages

Set the output voltage on each output by selecting the resistive voltage divider ratio. The voltage divider drops the output voltage to the feedback threshold voltage. Use 10kΩ to 50kΩ for the low-side resistor R_L of the voltage divider.

For the step-up converter, determine the high-side resistor R_H by the equation:

$$R_H = \frac{V_{MAIN} - V_{FB1}}{\left(\frac{V_{FB1}}{R_L}\right)}$$

Where V_{MAIN} is the output voltage of the step-up converter.

For the positive charge-pump, determine the high-side resistor R_H by the equation:

$$R_H = \frac{V_{GH} - V_{FB3}}{\left(\frac{V_{FB3}}{R_L}\right)}$$

For the negative charge-pump, determine the high-side resistor R_H by the equation:

$$R_H = \frac{-V_{GL}}{\left(\frac{V_{REF}}{R_L}\right)}$$

Selecting the Inductor

The inductor is required to force the higher output voltage while being driven by the input voltage. A larger value inductor results in less ripple current that results in lower peak inductor current, reducing stress on the internal N-Channel switch. However, the larger value inductor has a larger physical size, higher series resistance, and/or lower saturation current.

A 4.7µH inductor is recommended for most applications. A good rule of thumb is to allow the peak-to-peak ripple current to be approximately 30-50% of the maximum input current. Make sure that the peak inductor current is below 75% of the current limit to prevent loss of regulation due to the current limit. Also make sure that the inductor does not saturate under the worst-case load transient and startup conditions.

Calculate the required inductance value by the equation:

$$L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f_{SW} \times \Delta I}$$

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{LOAD(MAX)}}{V_{IN} \times \eta}$$

$$\Delta I = (30\% - 50\%) I_{IN(MAX)}$$

Where $I_{LOAD(MAX)}$ is the maximum load current, ΔI is the peak-to-peak inductor ripple current, and η is efficiency.

Selecting the Input Capacitor

An input capacitor is required to supply the AC ripple current to the inductor, while limiting noise at the input source. A low ESR capacitor is required to keep the noise at the IC to a minimum. Since it absorbs the input switching current it requires an adequate ripple current rating. Use a capacitor with RMS current rating greater than the inductor ripple current (see selecting the Inductor to determine the inductor ripple current). One 10µF ceramic capacitor is used in the application circuit of Figure 3 because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance since the step-up converter typically runs directly from the output of another regulated supply. Typically, the input capacitance can be reduced below the value used in the typical application circuit.

To insure stable operation place the input capacitor as close to the IC as possible. Alternately a smaller high quality 0.1µF ceramic capacitor may be placed closer to the IC if the larger capacitor is placed further away.

Selecting the Rectifier Diodes

The MPQ1530's high switching frequency demands high-speed rectifiers. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. Typically, a 1A Schottky diode is recommended for the step-up converter. 100mA Schottky diodes such as Central Semiconductor CMPSH-3 are recommended for low current charge-pump circuits.

Selecting the Output Capacitor of the Step-Up Converter

The output capacitor is required to maintain the DC output voltage. Low ESR capacitors are preferred to keep the output voltage ripple to a minimum. The characteristics of the output capacitor also affect the stability of the regulation control system. A 10µF ceramic capacitor works well in most applications. In the case of ceramic capacitors, the impedance of the capacitor at the switching frequency is dominated by the capacitance, and so the output voltage ripple is mostly independent of the ESR. The output voltage ripple is estimated to be:

$$V_{RIPPLE} \cong \left(1-\frac{V_{IN}}{V_{MAIN}}\right)\times\frac{I_{LOAD}}{C2\times f_{SW}}$$

Where V_{RIPPLE} is the output ripple voltage, I_{LOAD} is the load current, and C2 is the capacitance of the output capacitor of the step-up converter.

Selecting the Number of Charge-Pump Stages

For highest efficiency, always choose the lowest number of charge-pump stages that meets the output requirement.

The number of positive charge-pump stages N_{POS} is given by:

$$N_{POS} = \frac{V_{GH} - V_{DROPOUT} - V_{MAIN}}{V_{MAIN} - 2V_D}$$

Where V_D is the forward voltage drop of the charge-pump diode, and $V_{DROPOUT}$ is the dropout margin for the linear regulator.

The number of negative charge-pump stages N_{NEG} is given by:

$$N_{NEG} = \frac{-V_{GL} + V_{DROPOUT}}{V_{MAIN} - 2V_D}$$

Use $V_{DROPOUT}$ = 1V for positive charge-pump and $V_{DROPOUT}$ = 0.3V for negative charge-pump.

Selecting the Flying Capacitor in Charge-Pump Stages

Increasing the flying capacitor C_X values increases the output current capability. A 0.1µF ceramic capacitor works well in most low current applications. The flying capacitor's voltage rating must exceed the following:

$$V_{CX} > N \times V_{MAIN}$$

Where N is the stage number in which the flying capacitor appears.

Step-Up Converter Compensation

The MPQ1530 uses current mode control which unlike voltage mode has only a single pole roll off due to the output filter. The DC gain (Av_{DC}) is equated from the product of current control to output gain ($Av_{CSCONTROL}$), error amplifier gain (Av_{EA}), and the feedback divider.

$$Av_{DC} = A_{CSCONTROL} \times Av_{EA} \times A_{FB1}$$

$$A_{CSCONTROL} = 4 \times \frac{V_{IN}}{I_{LOAD}}$$

$$A_{FB1} = \frac{V_{FB1}}{V_{MAIN}}$$

$$Av_{DC} = \frac{1600 \times V_{IN} \times V_{FB1}}{I_{LOAD} \times V_{MAIN}}$$

The output filter pole is given in hertz by:

$$f_{FILTERPOLE} = \frac{I_{LOAD}}{\pi \times V_{MAIN} \times C2}$$

The output filter zero is given in hertz by:

$$f_{FILTERZERO} = \frac{1}{2\pi \times R_{ESR} \times C2}$$

Where R_{ESR} is the output capacitor's equivalent series resistance.

With all boost regulators the right half plane zero (RHPZ) is given in hertz by:

$$f_{RHPZ} = \frac{\left(\frac{V_{IN}}{V_{MAIN}}\right)^2 \times V_{MAIN}}{2\pi \times I_{LOAD} \times L1}$$

Error Amplifier Compensation

To stabilize the feedback loop dynamics the error amplifier compensation is as follows:

$$f_{POLE1} \approx \frac{1}{2\pi \times 10^6 \times C3}$$

$$f_{ZERO1} \approx \frac{1}{2\pi \times R3 \times C3}$$

Where R3 and C3 are part of the compensation network in Figure 3. A 6.8kΩ and 10nF combination gives about 70° of phase margin and bandwidth of about 35kHz for most load conditions.

Linear Regulator Compensation

The positive and negative regulators are controlled by a transconductance amplifier and a pass transistor. The DC gain of either LDO is approximately 100dB with a slight dependency on load current. The output capacitor (C_{LDO}) and resistance load (R_{LOAD}) make-up the dominant pole.

$$f_{LDOPOLE1} = \frac{1}{2\pi \times R_{LOAD} \times C_{LDO}}$$

The pass transistor's internal pole is about 100Hz to 300Hz. To compensate for the two pole system and add more phase and gain margin, a capacitor network can be added in parallel with the high-side resistor.

For the positive linear regulator:

$$f_{POSPOLE1} = \frac{1}{2\pi \times R9 \| R8 \times C7}$$

$$f_{POSZERO1} = \frac{1}{2\pi \times R9 \times C7}$$

For the negative linear regulator:

$$f_{NEGPOLE1} = \frac{1}{2\pi \times R7 \| R5 \times C9}$$

$$f_{NEGZERO1} = \frac{1}{2\pi \times R7 \times C9}$$

$f_{POSPOLE1}$ and $f_{NEGPOLE1}$ are necessary to cancel out the zero created by the equivalent series resistance (R_{LDOESR}) of the output capacitor.

$$f_{LDOZERO} = \frac{1}{2\pi \times R_{LDOESR} \times C_{LDO}}$$

For the component values shown in Figure 3, a 330pF capacitor provides about 30° of phase margin and a bandwidth of approximately 90kHz on both regulators.

Layout Considerations

Careful PC board layout is important to minimize ground bounce and noise. First, place the main boost converter inductor, output diode and output capacitor as close to the SW and PGND pins as possible with wide traces. Then place ceramic bypass capacitors near IN, IN2 and IN3 pins to the PGND pin. Keep the charge-pump circuitry close to the IC with wide traces. Place all FB resistive dividers close to their respective FB pins. Separate GND and PGND areas and connect them at one point as close to the IC as possible. Avoid having sensitive traces near the SW node and high current lines. Refer to the MPQ1530 demo board for an example of proper board layout.

Design Specification

The below is a design example following the application guidelines for the specifications:

Table 1: Design Example Specification

Parameter	Symbol	Value	Units
Input Voltage	V_{IN}	3-5.5	V
Output Voltage 1	V_{MAIN}	+13	V
Output Current 1	I_{MAIN}	350	mA
Output Voltage 2	V_{GH}	+27	V
Output Current 2	I_{GH}	20	mA
Output Voltage 3	V_{GL}	-8.5	V
Output Current 3	I_{GL}	20	mA

Design Example

The detailed application schematic is shown in Figure 3. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheets.

TYPICAL APPLICATION CIRCUITS

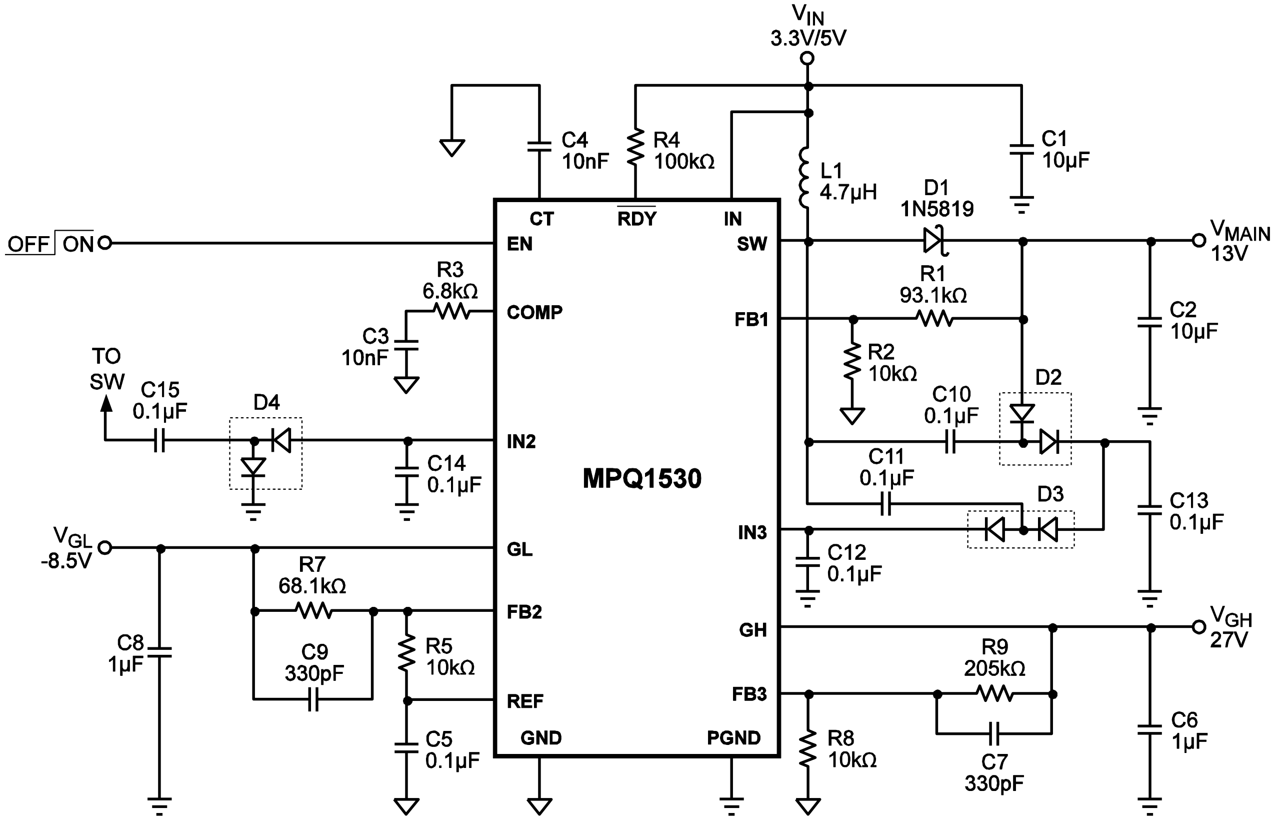


Figure 3—Triple Output Boost Application Circuit