MPQ18024

100V, 4A, High-Frequency, Half-Bridge Gate Driver AEC-Q100 Qualified

DESCRIPTION

The MPQ18024 is a high-frequency, 100V, half-bridge, N-channel power MOSFET driver. Its low-side and high-side driver channels are controlled independently and matched with less than 5ns of time delay. Under-voltage lockout (UVLO) on the high-side and low-side supplies force their outputs low in the case of an insufficient supply. The integrated bootstrap diode reduces the external component count.

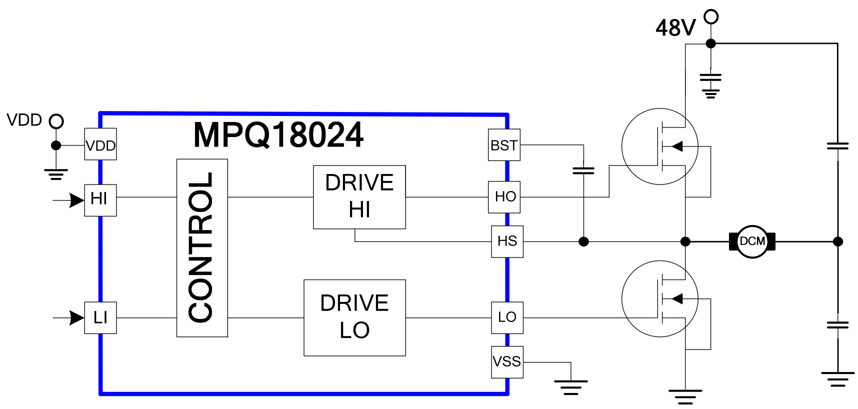
FEATURES

- Guaranteed Industrial / Automotive Temperature Range Limits
- Drives an N-Channel MOSFET Half-Bridge
- 100V V_{BST} Voltage Range
- On-Chip Bootstrap Diode
- Typical Propagation Delay of 20ns
- Gate Drive Matching of Less than 5ns
- Drives a 2.2nF Load with 15ns of Rise Time and 12ns of Fall Time at 12V VDD
- TTL-Compatible Input
- Quiescent Current of Less than 160µA
- UVLO for both High-Side and Low-Side
- Available in a SOIC-8E Package
- Available in AEC-Q100 Qualified Grade 1

APPLICATIONS

- Car DC/DC Power Systems
- Half-Bridge Motor Drivers

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MPQ18024HN-AEC1	SOIC-8 EP	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MPQ18024HN-AEC1–Z).

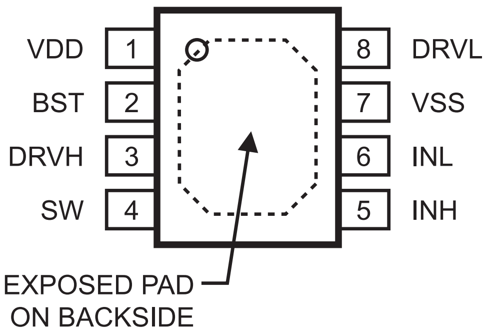
TOP MARKING

MP18024
LLLLLLLL
MPSYWW

MP18024: Part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE

TOP VIEW



SOIC-8 EP

PIN FUNCTIONS

Pin #	Name	Description
1	VDD	**Supply input.** VDD supplies power to all of the internal circuitries. Place a decoupling capacitor to ground close to VDD to ensure a stable and clean supply.
2	BST	**Bootstrap.** BST is the positive power supply for the internal floating high-side MOSFET driver. Connect a bypass capacitor between BST and SW.
3	DRVH	**Floating driver output.**
4	SW	**Switching node.**
5	INH	**Control signal input for the floating driver.**
6	INL	**Control signal input for the low side driver.**
7	VSS	**Chip ground.** Connect the exposed pad to VSS for proper thermal operation.
Exposed Pad		
8	DRVL	**Low-side driver output.**

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{DD}) .... -0.3V to 18V
SW voltage (V_{SW}) .... -5.0V to 110V
BST voltage (V_{BST}) .... -0.3V to 110V
BST to SW .... -0.3V to 18V
DRVH to SW .... -0.3V to (BST - SW) + 0.3V
DRVL to VSS ....-0.3V to (VDD + 0.3V)
All other pins ....-0.3V to (V_{DD} + 0.3V)
CDM rating (AEC-Q100-011C1)
All pins..Class C6
HBM rating (AEC-Q100-002)
BST, DRVH.......................................Class H1C
Other pins...Class H2
Continuous power dissipation (T_A = 25°C) (2)
.... 2.5W
Junction temperature .... 150°C
Lead temperature..................................... 260°C
Storage temperature...................-65°C to 150°C

Recommended Operating Conditions (3)

Supply voltage (V_{DD}) .... 9.0V to 16.0V
SW voltage (V_{SW}) ....
.... (-10V / <100ns) to 100V - VDD
SW slew rate .... <50V/ns
Operating junction temp. (T_J)......-40°C to 125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

SOIC-8 EP .... 50 ...... 12 ...°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{DD} = V_{BST} - V_{SW} = 12V, V_{SS} = V_{SW} = 0V, no load at DRVH and DRVL, T_J = -40°C to +125°C, typical values tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Currents						
VDD quiescent current	I_{DDQ}	INL = INH = 0		120	160	μA
VDD operating current	I_{DDO}	fsw = 500kHz		9		mA
Floating driver quiescent current	I_{BSTQ}	INL = INH = 0		70	100	μA
Floating driver operating current	I_{BSTO}	fsw = 500kHz		8.5		mA
Leakage current	I_{LK}	BST = SW = 100V		0.05	2.5	μA
Inputs						
INL/INH high				2.2	2.6	V
INL/INH low			1	1.5		V
INL/INH internal pull-down resistance	R_{IN}			185		kΩ
Under-Voltage Protection (UVP)						
VDD rising threshold	V_{DDR}		8.1	8.5	8.9	V
VDD hysteresis	V_{DDH}			0.5		V
(BST - SW) rising threshold	V_{BSTR}		6.8	7.4	8	V
(BST - SW) hysteresis	V_{BSTH}			0.55		V
Bootstrap Diode						
Bootstrap diode VF @ 100μA	V_{F1}			0.5		V
Bootstrap diode VF @ 100mA	V_{F2}			0.95		V
Bootstrap diode dynamic R	R_D	@ 100mA		2.3		Ω
Low-Side Gate Driver						
Low-level output voltage	V_{OLL}	I_O = 100mA		0.08		V
High-level output voltage to rail	V_{OHL}	I_O = -100mA		0.23		V
Peak pull-up current (5)	I_{OHL}	V_{DRVL} = 0V, V_{DD} = 12V		3		A
		V_{DRVL} = 0V, V_{DD} = 16V		4.7		A
Peak pull-down current (5)	I_{OLL}	V_{DRVL} = V_{DD} = 12V		4.5		A
		V_{DRVL} = V_{DD} = 16V		6		A
Floating Gate Driver						
Low-level output voltage	V_{OLH}	I_O = 100mA		0.08		V
High-level output voltage to rail	V_{OHH}	I_O = -100mA		0.23		V
Peak pull-up current (5)	I_{OHH}	V_{DRVH} = 0V, V_{DD} = 12V		2.6		A
		V_{DRVH} = 0V, V_{DD} = 16V		4		A
Peak pull-down current (5)	I_{OLH}	V_{DRVH} = V_{DD} = 12V		4.5		A
		V_{DRVH} = V_{DD} = 16V		5.9		A
Switching spec – low-side gate driver						
Turn-off propagation delay INL falling to DRVL falling	T_{DLFF}			20		ns
Turn-on propagation delay INL rising to DRVL rising	T_{DLRR}			20		
DRVL rise time		C_L = 2.2nF		15		ns
DRVL fall time		C_L = 2.2nF		9		ns

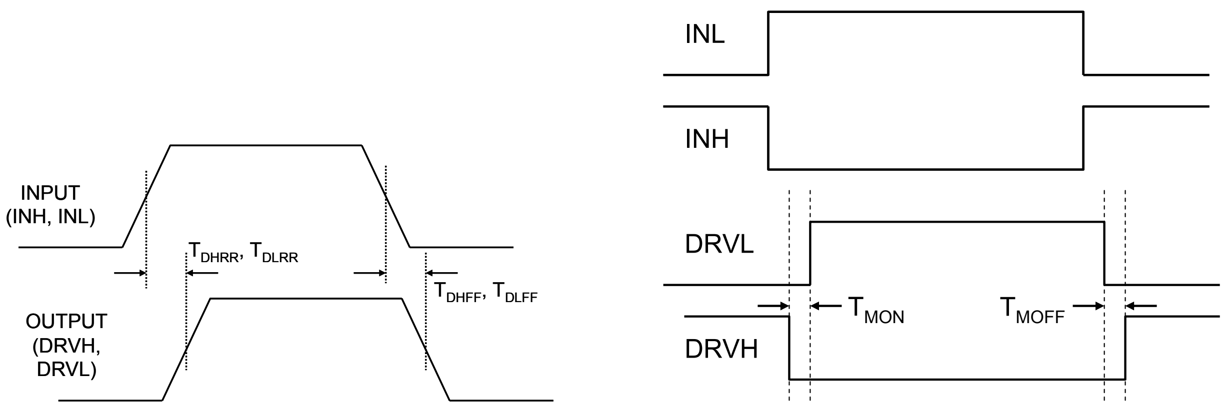
ELECTRICAL CHARACTERISTICS *(continued)*

V_{DD} = V_{BST} - V_{SW} = 12V, V_{SS} = V_{SW} = 0V, no load at DRVH and DRVL, T_J = -40°C to +125°C, typical values tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Switching Spec – Floating Gate Driver						
Turn-off propagation delay INL falling to DRVH falling	T_{DHFF}			20		ns
Turn-on propagation delay INL rising to DRVH rising	T_{DHRR}			20		ns
DRVH rise time		C_L = 2.2nF		15		ns
DRVH fall time		C_L = 2.2nF		12		ns
Switching Spec – Matching						
Floating driver turn-off to low-side drive turn-on (5)	T_{MON}			1	5	ns
Low-side driver turn-off to floating driver turn-on (5)	T_{MOFF}			1	5	ns
Minimum input pulse width that changes the output	T_{PW}				50 (5)	ns
Bootstrap diode turn-on or turn-off time	T_{BS}			10 (5)		ns
Thermal shutdown (5)				170		°C
Thermal shutdown hysteresis (5)				25		°C

NOTE:
5) Guaranteed by design.

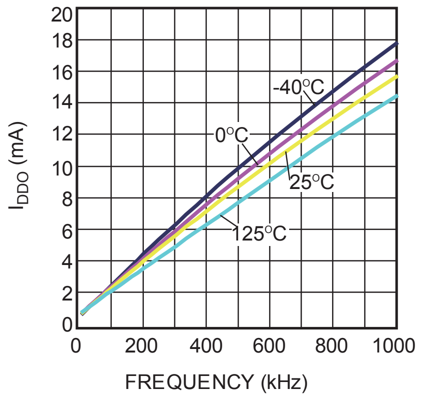
TIMING DIAGRAM



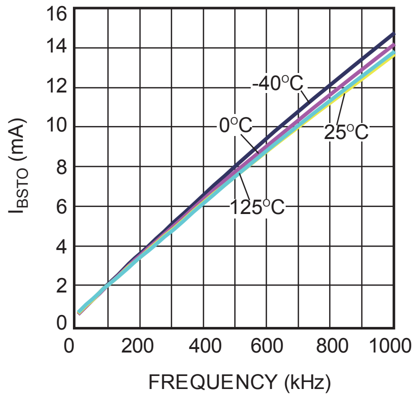
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 12V, V_{SS} = V_{SW} = 0V, T_A = +25°C, unless otherwise noted.

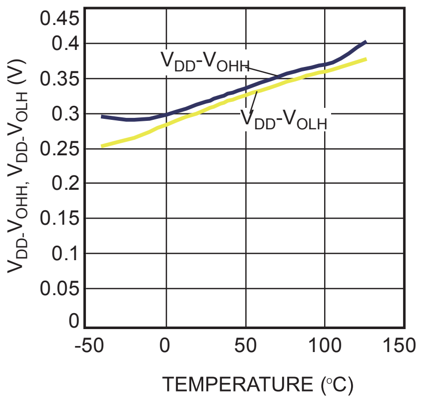
I_{DDO} Operation Current vs. Frequency



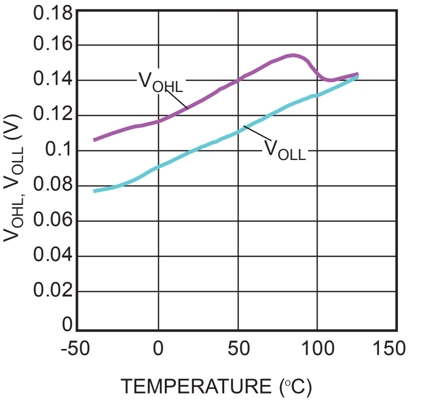
I_{BSTO} Operation Current vs. Frequency



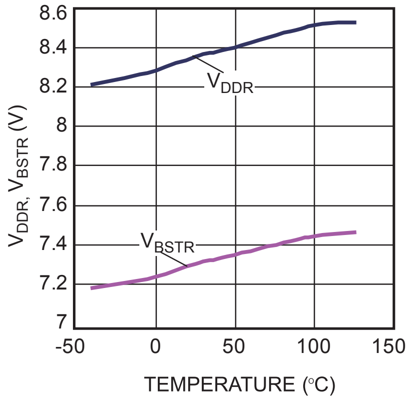
High-Level Output Voltage vs. Temperature



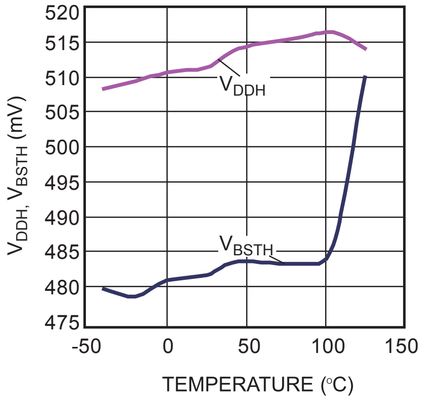
Low-Level Output Voltage vs. Temperature



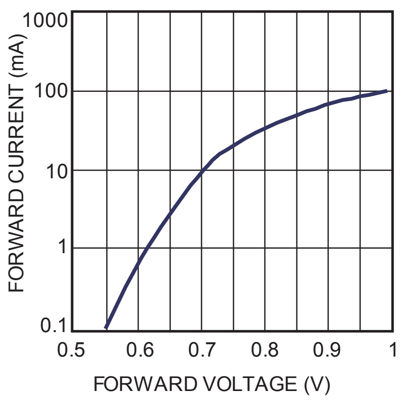
Under-Voltage Lockout Threshold vs. Temperature



Under-Voltage Lockout Hysteresis vs. Temperature

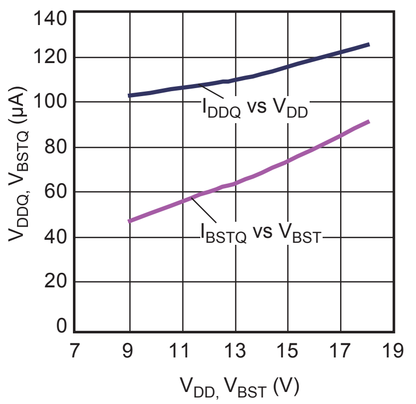


Bootstrap Diode I-V Characteristic

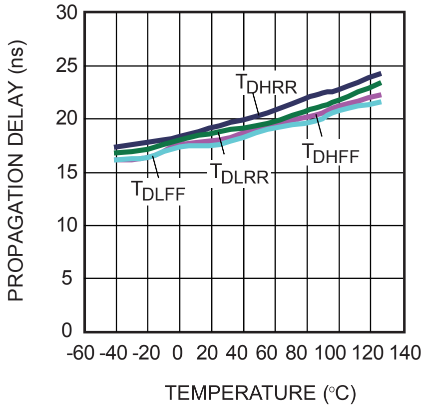


Quiescent Current vs. Voltage

INH=INL=0V



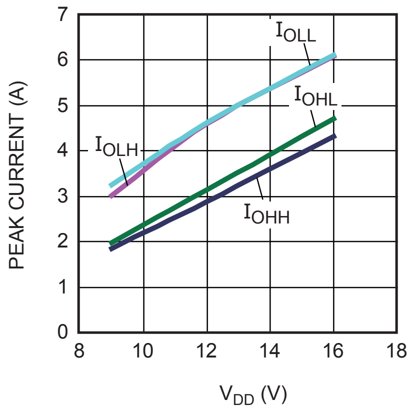
Propagation Delay vs. Temperature



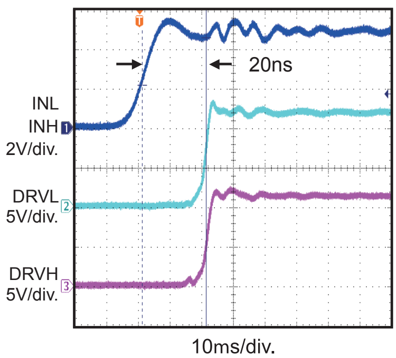
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{DD} = 12V, V_{SS} = V_{SW} = 0V, T_A = +25°C, unless otherwise noted.

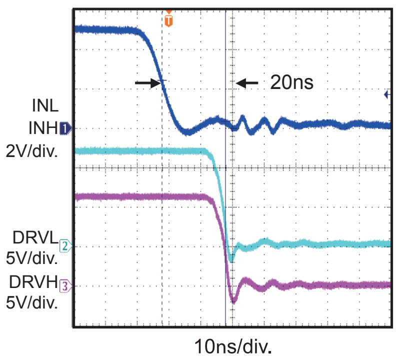
Peak Current vs. V_{DD} Voltage



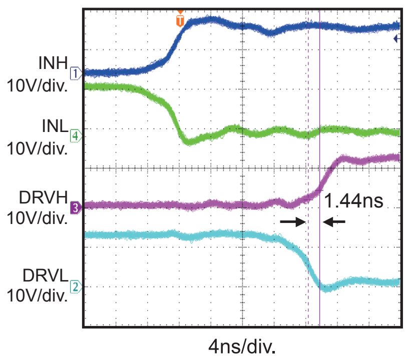
Turn-On Propagation Delay



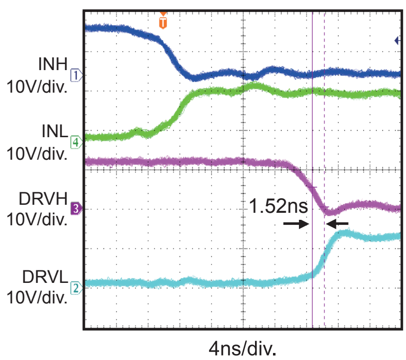
Turn-Off Propagation Delay



Gate Drive Matching T_{MOFF}

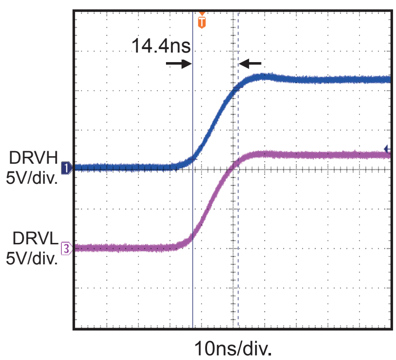


Gate Drive Matching T_{MON}



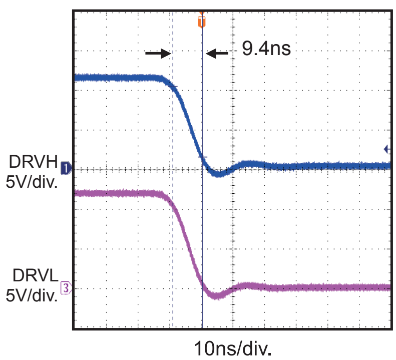
Drive Rise Time

2.2nF Load



Drive Fall Time

2.2nF Load



BLOCK DIAGRAM

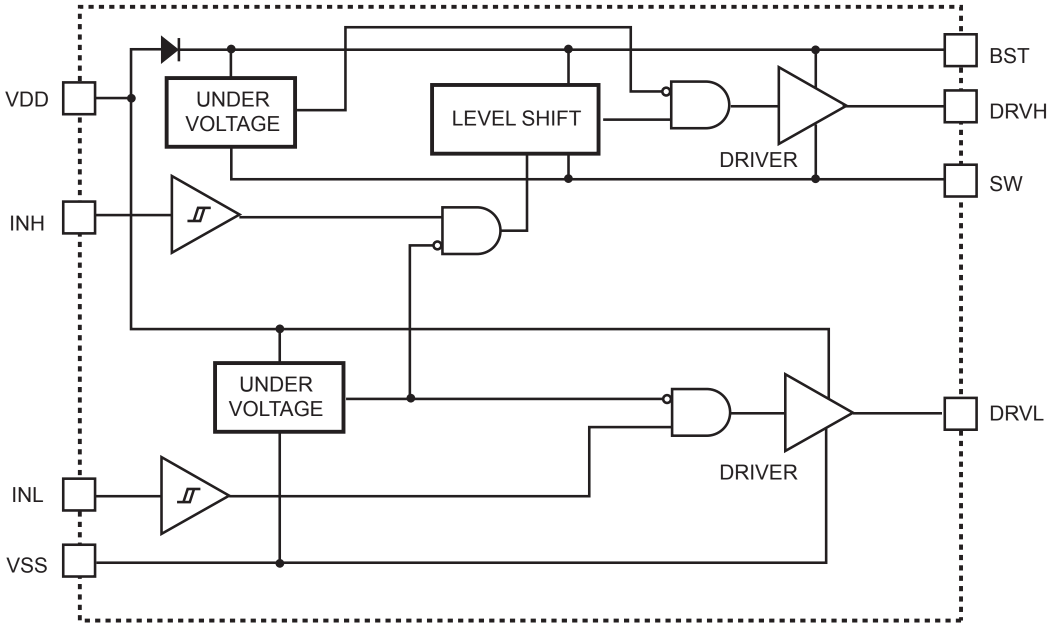


Figure 1: Functional Block Diagram

APPLICATION

The input signals of INH and INL can be controlled independently. If both INH and INL control the high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET) of the same bridge, shoot through can be prevented by setting a sufficient dead time between INH and INL low, and vice versa (see Figure 2). Dead time is defined as the time interval between INH low and INL low.

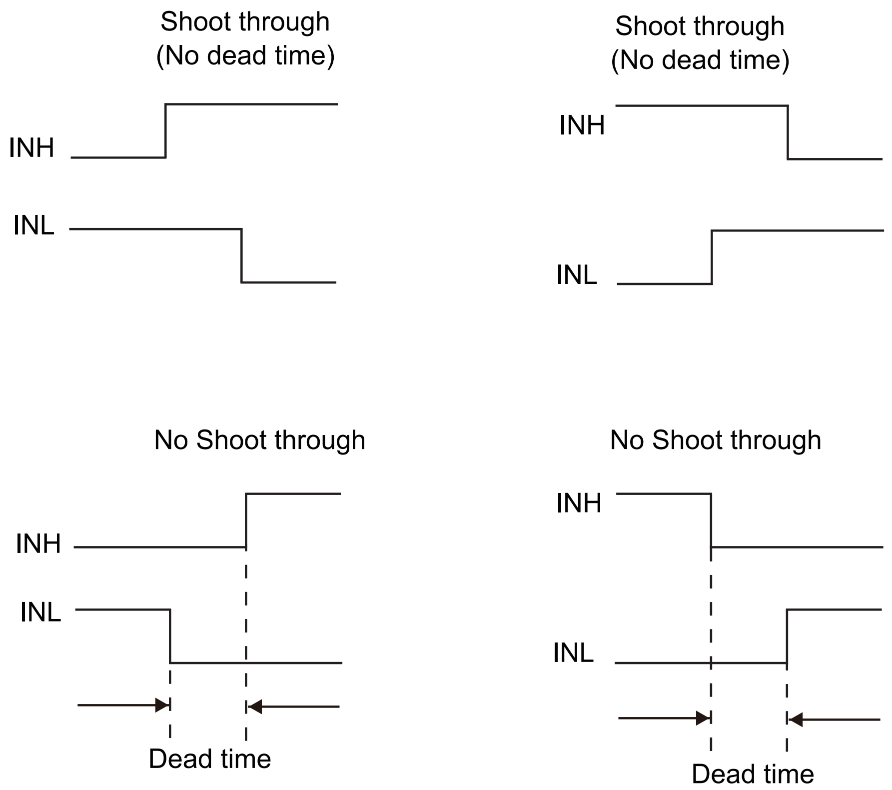


Figure 2: Shoot-Through Timing Diagram

REFERENCE DESIGN CIRCUITS

Half-Bridge Converter

The MPQ18024 drives the MOSFETs with alternating signals (with dead time) in a half-bridge converter topology. Because the pulse-width modulation (PWM) controller drives INH and INL with alternating signals, the input voltage can rise as high as 100V (see Figure 3 through Figure 5).

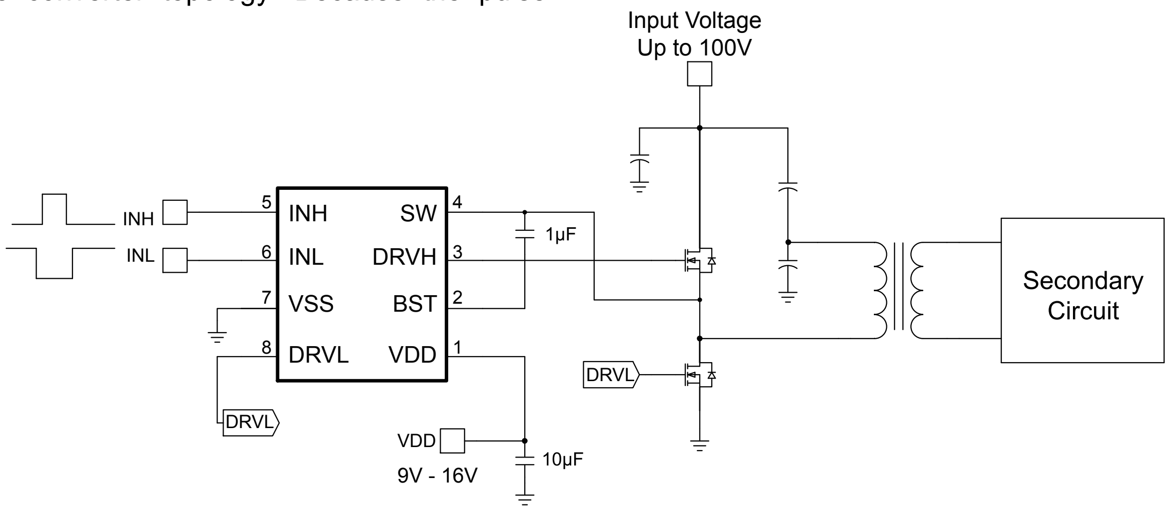


Figure 3: Half-Bridge Converter

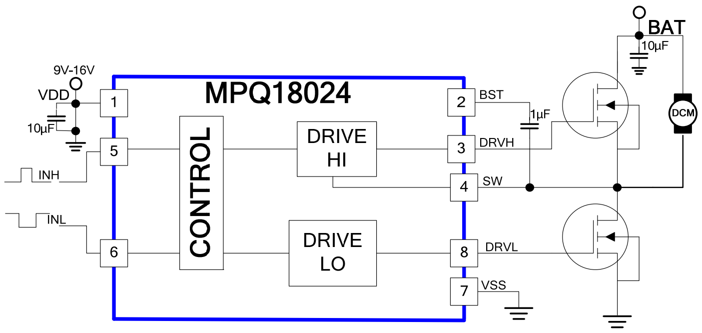


Figure 4: Half-Bridge for Unidirectional Motor

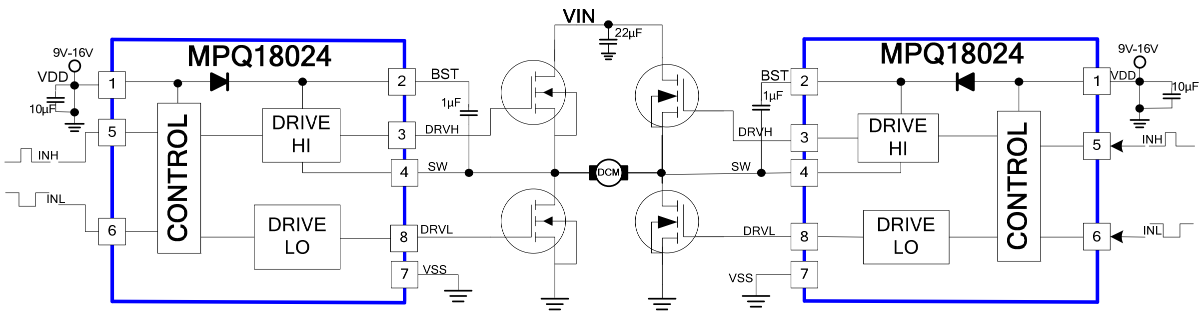


Figure 5: 2x MPQ18024 for One Bidirectional DC Motor