MPQ3324

8-Channel, 100mA/Ch, LED Driver with Separated PWM Analog Dimming and I²C Interface, AEC-Q100

DESCRIPTION

The MPQ3324 is an 8-channel WLED driver that operates from a wide 4V to 16V input voltage range. The MPQ3324 applies 8 internal current sources in each LED string terminal. The LED current of each channel is set by an external current-setting resistor. Each channel has a maximum 100mA current (while V_{IN} ≥ 4.5V).

The device integrates an I²C interface. There are 10 different I²C addresses that can be configured via an external resistor. This means the MPQ3324 can support up to 10 ICs that have been cascaded to drive an LED array. Each channel can be enabled or disabled through the I²C.

The MPQ3324 employs both separated PWM dimming and analog dimming for each LED channel, with a 12-bit PWM dimming resolution and 6-bit analog dimming for each channel. To optimize EMI and EMC performance, The LED current ramping rate and phase shift can be configured.

The MPQ3324 can output a refresh signal from the RFSH/FLT pin. The refresh signal frequency can be set via the I²C.

Integrated protections include open-load protection, short-load protection, and over-temperature protection (OTP). The fault indicator pulls to low if a protection is triggered. Meanwhile, the corresponding fault register is set.

The MPQ3324 is AEC-Q100 qualified, and is available in QFN-24 (4mmx4mm).

FEATURES

- Wide 4V to 16V Input Voltage Range
- 8 Channels, 100mA/Ch Maximum (V_{IN} ≥ 4.5V)
- LED Current Configured via External Resistor
- 6-Bit Analog Dimming for Each Channel
- 12-Bit PWM Dimming for Each Channel
- Selectable 220Hz, 250Hz, 280Hz, or 330Hz PWM Dimming Frequency
- Refresh Signal Output
- I²C Interface
- 10 Addresses Configurable via External Resistor
- Configurable LED Current Slew Rate
- 80μs Phase Shift
- Fault Indicator
- LED Open Protection
- LED Short Protection, Configurable Threshold
- Under-Voltage Lockout (UVLO)
- Over-Temperature Protection (OTP)
- ELV Directive II Compliant
- Available in a QFN-24 (4mmx4mm) Package with Wettable Flank
- AEC-Q100 Grade 1

APPLICATIONS

- Automotive Lights
- Automotive Displays
- Instruments Clusters
- General Industrial Displays

TYPICAL APPLICATION

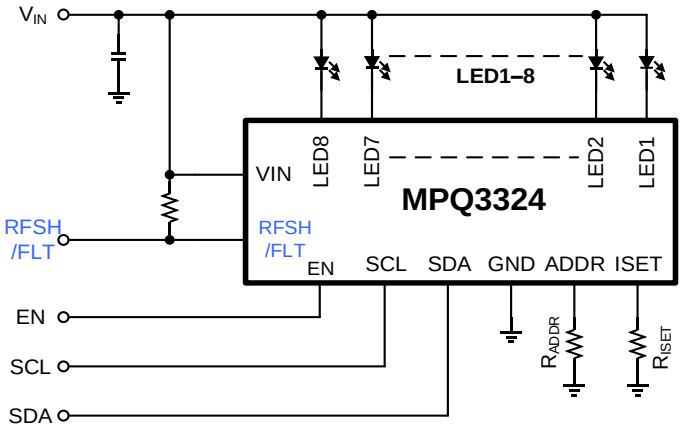


Figure 1: Typical Application Circuit

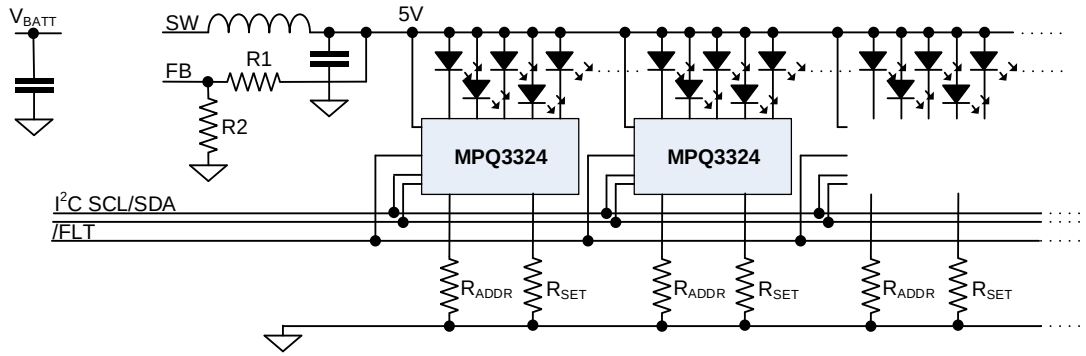


Figure 2: System Application Circuit

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ3324GRE-AEC1	QFN-24 (4mmx4mm)	*See Below*	*1*

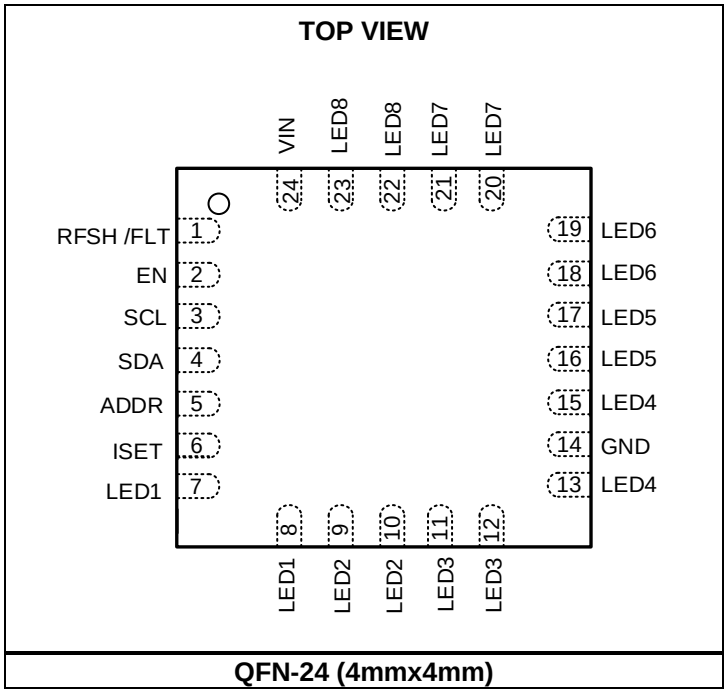
* For Tape & Reel, add suffix –Z (e.g. MPQ3324GRE-AEC1–Z).

TOP MARKING

MPSYWW
MP3324
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
MP3324: Part number
LLLLLL: Lot number
E: Wettable lead flank

PACKAGE REFERENCE



QFN-24 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	RFSH/FLT	**Refresh signal output or fault flag.** If the FLTEN bit is set to 0, the RFSH/FLT pin outputs a synchronized signal that is set by the FRFSH9:0 register. If the FLTEN bit is set to 1, RFSH/FLT is used to indicate fault conditions, and is pulled low if a fault occurs.
2	EN	**Enable control.** Pull EN low to disable the IC. Pull EN high to enable the IC.
3	SCL	**I²C interface clock input.**
4	SDA	**I²C interface data input.**
5	ADDR	**I²C address setting.** Configure the I²C addresses by attaching different resistors from ADDR to GND. ADDR sets the 4LSB of the I²C address. There are 10 configurable addresses.
6	ISET	**LED current setting.** Tie a current-setting resistor from ISET to ground to configure the current in each LED string.
7, 8	LED1	**LED channel 1 current input.** Connect the LED channel 1 cathode to this pin. Each channel has two LED1 pins, and both LED1 pins must be connected to LED channel 1 cathode.
9, 10	LED2	**LED channel 2 current input.** Connect the LED channel 2 cathode to this pin. Each channel has two LED2 pins, and both LED2 pins must be connected to LED channel 2 cathode.
11, 12	LED3	**LED channel 3 current input.** Connect the LED channel 3 cathode to this pin. Each channel has two LED3 pins, and both LED3 pins must be connected to LED channel 3 cathode.
13, 15	LED4	**LED channel 4 current input.** Connect the LED channel 4 cathode to this pin. Each channel has two LED4 pins, and both LED4 pins must be connected to LED channel 4 cathode.
14	GND	**Ground.**
16, 17	LED5	**LED channel 5 current input.** Connect the LED channel 5 cathode to this pin. Each channel has two LED5 pins, and both LED5 pins must be connected to LED channel 5 cathode.
18, 19	LED6	**LED channel 6 current input.** Connect the LED channel 6 cathode to this pin. Each channel has two LED6 pins, and both LED6 pins must be connected to LED channel 6 cathode.
20, 21	LED7	**LED channel 7 current input.** Connect the LED channel 7 cathode to this pin. Each channel has two LED7 pins, and both LED7 pins must be connected to LED channel 7 cathode.
22, 23	LED8	**LED channel 8 current input.** Connect the LED channel 8 cathode to this pin. Each channel has two LED8 pins, and both LED8 must be connected to LED channel 8 cathode.
24	VIN	**Power supply input.** VIN supplies power to the IC. Connect a capacitor from VIN to GND.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to +18V
V_{LED1} to V_{LED8}.....-0.5V to +18V
All other pins .....-0.3V to +5V
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C
Continuous power dissipation (T_A = 25°C) (2)
QFN-24 (4mmx4mm) 2.97W

ESD Ratings

Human body model (HBM) .....-2kV to +1.25kV
Charged device model (CDM) ..... ±2kV

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....4V to 16V
Operating junction temp (T_J).....-40°C to +150°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-24 (4mmx4mm) ……..…..42…….9.....°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, V_{EN} = 3.5V, T_J = -40°C to +125°C, typical value is at T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply Voltage						
Input voltage range	V_{IN}		4		16	V
Quiescent supply current	I_Q				4	mA
Shutdown supply current	I_{ST}	V_{EN} = 0V, V_{IN} = 16V			2	μA
Input UVLO threshold	V_{IN_UVLO}	Rising edge	3.45	3.7	3.95	V
		Falling edge	3.15	3.5	3.85	V
Enable						
EN rising threshold	V_{EN_ON}	EN rising	2.1			V
EN falling threshold	V_{EN_OFF}	EN falling			0.8	V
EN pull-down resistor	R_{EN}			1		MΩ
RFSH/FLT						
RFSH/FLT output frequency	f_{RFSH}	FRFSH9:0 = 0x1A9, FPWM2:0 = 01	285	300	315	Hz
RFSH/FLT pull-down resistor		FLTEN = 1, fault is triggered			100	Ω
LED Regulator						
ISET voltage	V_{ISET}	T_A = 25°C	1.174	1.2	1.226	V
LED current	I_{LED}	R_{ISET} = 20kΩ, ICHx5:0 = 0x3F	-3%	50	+3%	mA
		R_{ISET} = 20kΩ, ICHx5:0 = 0x3F, T_A = 25°C	-2%	50	+2%	mA
Current sink headroom	V_{LEDX}	I_{LED} = 40mA		150	210	mV
Dimming						
PWM frequency	f_{PWM}		230	245	260	Hz
PWM duty step	t_{PWM}	12-bit resolution, f_{PWM} = 250Hz		0.97		μs
Phase shift	t_{DELAY}	PS_EN = 1		80		μs
LED current step		I_{LED} = 50mA, analog dimming step		0.8		mA
LED current slew rate in PWM dimming		SLEW2:0 = 01, rising edge		5		μs
		SLEW1:0 = 11, rising edge		20		μs
Protection						
Short LED string protection threshold	V_{SLP}	STH1:0 = 01	2.75	3	3.25	V
Short LED string protection time	t_{SLP}	VLEDx > STH		4		ms
Short LED string protection hiccup time	t_{SLP_HICCUP}			1		ms
Short LED string protection hiccup detection time	t_{SLP_DET}			32		μs
Open LED string protection threshold	V_{LED_UV}			100	160	mV

ELECTRICAL CHARACTERISTICS

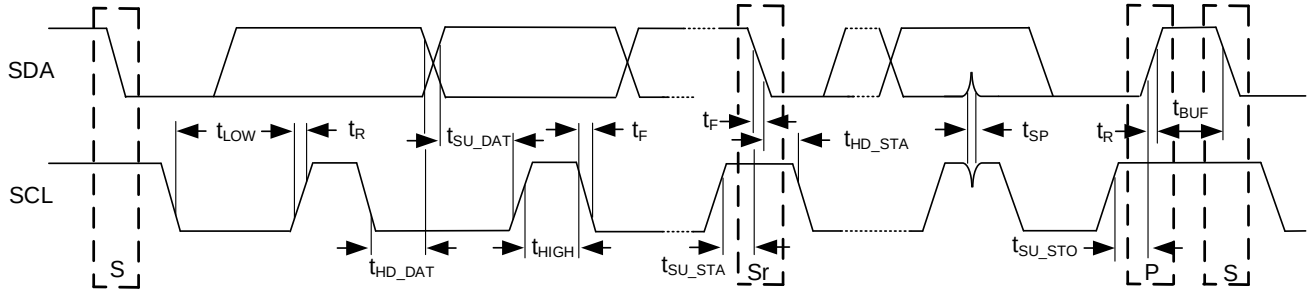
V_{IN} = 5V, V_{EN} = 3.5V, T_J = -40°C to +125°C, typical value is at T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Open LED string protection time	t_{LEDO}	VLEDx < 100mV		4		ms
Open LED string protection hiccup time	t_{SLP_HICCUP}			1		ms
Open LED string protection hiccup detection time	V_{SLP_DET}			32		µs
Thermal shutdown threshold (5)	T_{ST}			170		°C
Thermal shutdown hysteresis (5)	T_{ST_HYS}			20		°C
I²C Interface						
Input logic low	V_{IL}		0		0.4	V
Input logic high	V_{IH}		1.3			V
Output logic low	V_{OL}	I_{LOAD} = 3mA			0.4	V
SCL clock frequency	f_{SCL}				1200	kHz
SCL high time	t_{HIGH}		0.32			µs
SCL low time	t_{LOW}		0.12			µs
Data set-up time	t_{SU_DAT}		10			ns
Data hold time	t_{HD_DAT}		0		0.15	µs
Set-up time for repeated start	t_{SU_STA}		0.16			µs
Hold time for start	t_{HD_STA}		0.16			µs
Set-up time for stop condition	t_{SU_STO}		0.16			µs
SCL rising time after a repeated start condition and an acknowledge bit	t_{RCL1}		20		160	ns
SCL rising time	t_{RCL}		20		80	ns
SCL falling time	t_{FCL}		20		80	ns
SDA rising time	t_{RDA}		20		160	ns
SDA falling time	t_{FDA}		20		160	ns
Pulse width of suppressed spike	t_{SP}		0		10	ns
Capacitance bus for each bus line	C_B				400	pF

Notes:

5) Not tested in production. Guaranteed by characterization

I²C TIMING INTERFACE DIAGRAM



S = Start Condition
Sr = Repeated Start Condition
P = Stop Condition

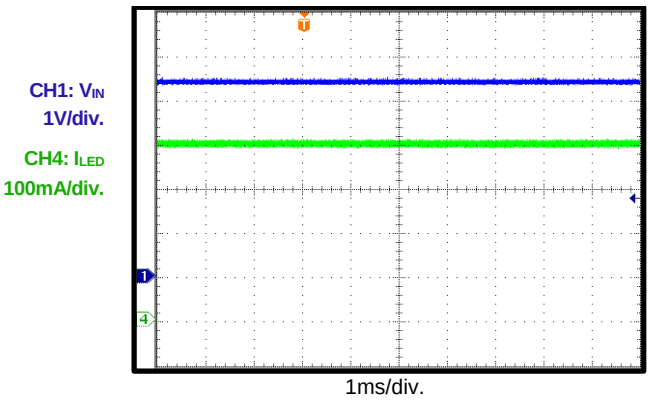
Figure 3: I²C Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

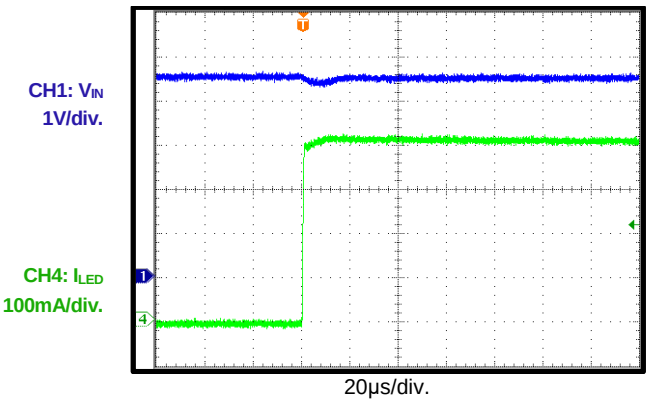
V_{IN} = 4.5V, LED = 8P/1S, I_{SET} = 50mA/string, T_A = 25°C, unless otherwise noted.

Steady State

V_{IN} = 4.5V, 8P/1S, 50mA/string

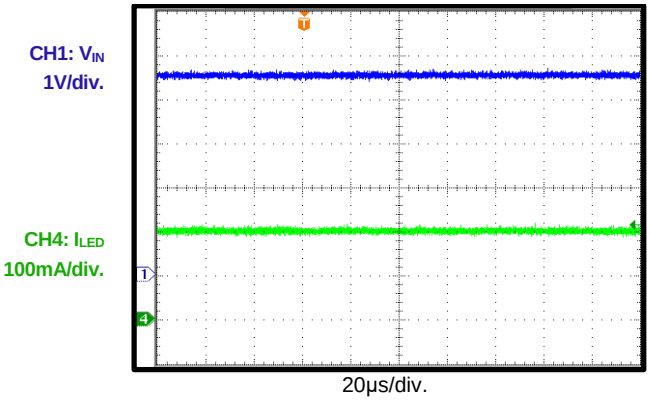


Start-Up through the EN Bit



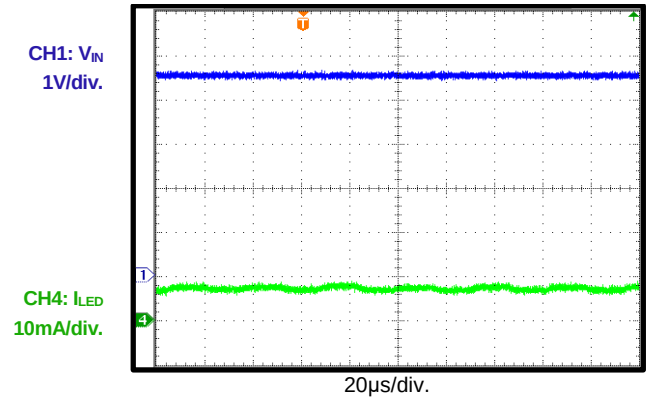
Analog Dimming

25mA/string



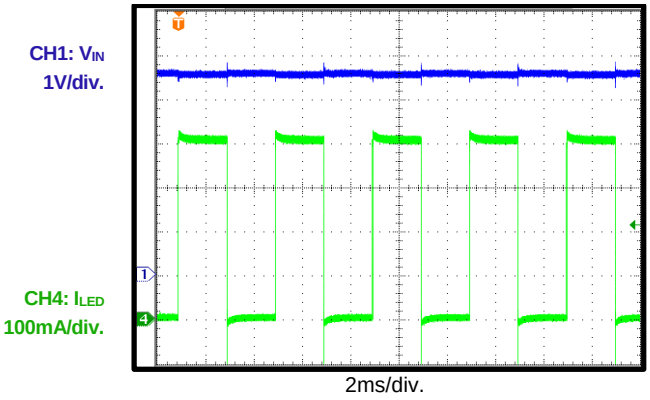
Analog Dimming

0.78mA/string



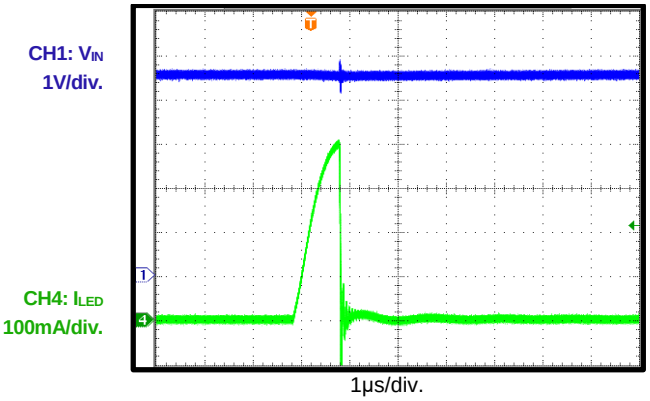
PWM Dimming

PWM duty = 50%



PWM Dimming

PWM duty = 0.024%

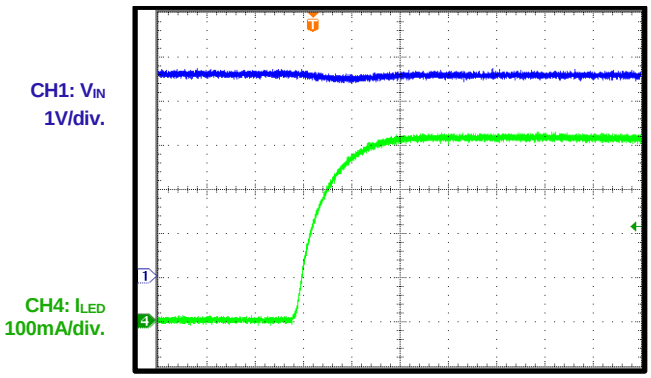


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 4.5V, LED = 8P/1S, I_{SET} = 50mA/string, T_A = 25°C, unless otherwise noted.

Slew Rate

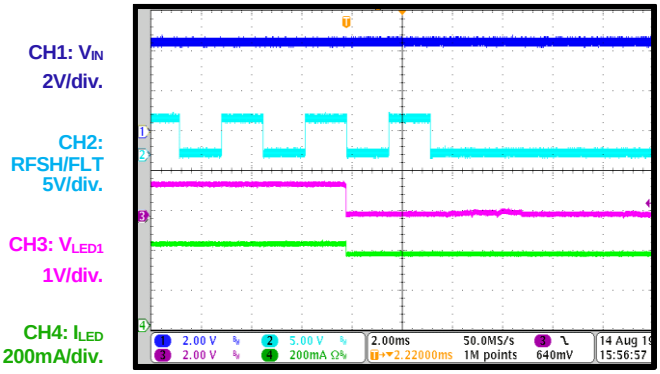
PWM dimming, slew rate = 5μs



10μs/div.

LED Open-Load Protection

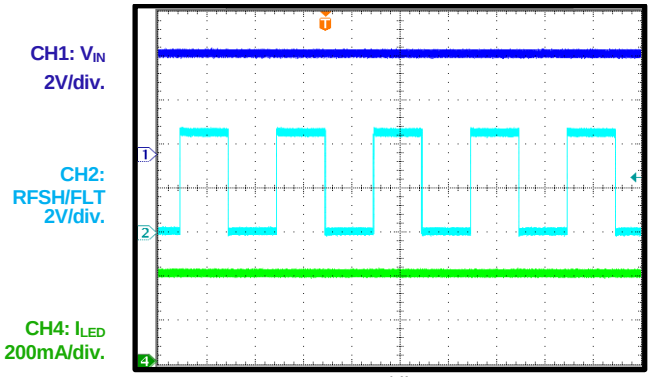
RFSH/FLT fault enabled



2ms/div.

Refresh Function

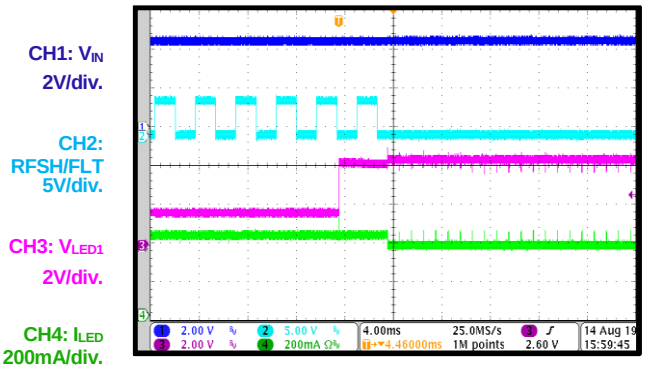
f_{PWM} = 250Hz, RFRSH = 1FF



2ms/div.

LED Short Protection

RFSH/FLT fault enable



4ms/div.

FUNCTIONAL BLOCK DIAGRAM

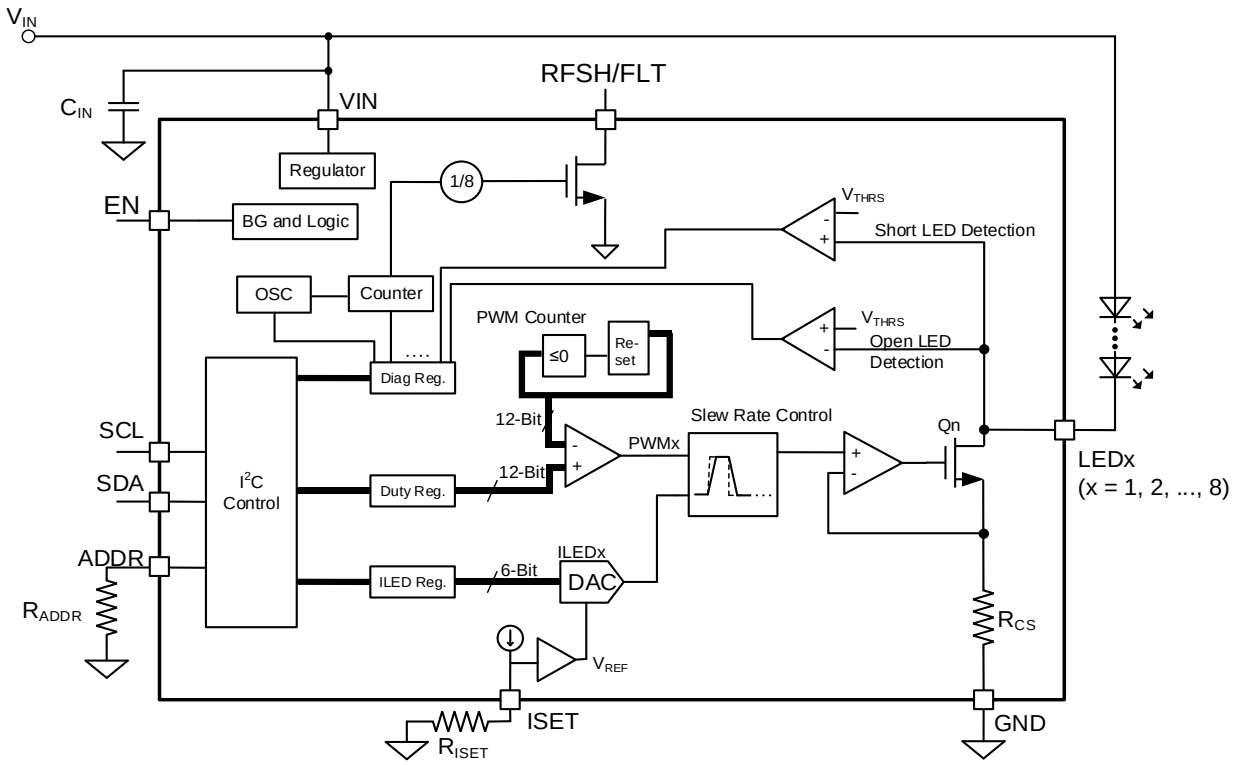


Figure 4: Functional Block Diagram

OPERATION

The MPQ3324 applies 8 internal current sources in each LED string terminal. The LED current of the channels are set via an external current-setting resistor. The maximum current is 100mA.

Enable and Start-Up

When the input voltage exceeds the under-voltage lockout (UVLO) threshold, and EN exceeds the rising threshold, the MPQ3324 operates in standby mode, and the I²C is active. After setting the I²C register, pull the EN bit high to start up the system. The start-up sequence is listed below:

1. VIN
2. EN
3. I²C setting
4. Set the EN bit

Channel Selection

Channels can be disabled by setting the corresponding CHxEN (e.g. x = 1, 2, ..., 8) bit low, or by connecting the channel to GND.

Dimming

Each channel has its own 6-bit analog dimming register and 12-bit PWM dimming register. The MPQ3324 can use analog dimming and PWM dimming for each channel.

In analog dimming, the LED current amplitude changes when the analog dimming register changes. Change the ICHx (e.g. x = 1, 2, ..., 8) bit to set analog dimming for the corresponding channel. The LED current (I_{LED}) can be estimated with Equation (1):

$$I_{LED} = \frac{ICHx}{63} \times ISET \quad (1)$$

Where ICHx sets the analog dimming code for the channel. If ICHx = 0, I_{LED} is 0A.

In PWM dimming, the LED current is a PWM waveform. The LED current amplitude stays the same, and the LED current duty varies with the PWM dimming register.

The PWM dimming duty is set by PWMx (e.g. x = 1, 2, ..., 8). The duty (D) can be calculated with Equation (2):

$$D = \frac{PWMx}{4095} \quad (2)$$

Where PWMx is the PWM dimming duty code for each corresponding channel. The duty changes only when the 8MSB of the PWM duty register is written. When PWMx = 0, the corresponding I_{LED} is 0A.

The PWM dimming frequency can be selected via register FPWM1:0. The potential frequencies are listed below:

- FPWM1:0 = 00: 220Hz
- FPWM1:0 = 01: 250Hz (default)
- FPWM1:0 = 10: 280Hz
- FPWM1:0 = 11: 330Hz

To avoid a glitch during normal operation, the following conditions must be met:

- Change the FPWM1:0 value only when the EN bit is set 0.
- Write the FPWM register and wait for a 10μs delay before writing to other registers.

Phase Shift

A channel-by-channel phase shift function can be implemented. This function is enabled by setting the PS_EN bit high.

When the phase shift function is enabled, the channel x + 1 (e.g. x = 1, 2, ..., 7) LED current rising edge is delayed for 80μs after channel x's LED current rising edge.

SYNC Output for the LCD Refresh Frequency

The fault indicator function can be enabled by the FLTEN bit.

If FLTEN = 0, the fault indicator function is disabled. RFSH/FLT maintains the output refresh signal, even if a protection is triggered.

If FLTEN = 1, the fault indicator function is enabled, and the RFSH/FLT pin is pulled low if a protection occurs. Table 1 shows the details of the RFSH/FLT pin's output status.

Table 1: RFSH/FLT Pin Output Status

FLTEN	RFSH/FLT Pin Output			
	FRFSH9:0 = 0x000		FRFSH9:0 = 0x001~0x3FF	
	No fault condition	Fault condition	No fault condition	Fault condition
1	Externally pulled high	Low	Rectangle signal	Low
0	Externally pulled high		Rectangle signal	

The refresh signal frequency is set by FRFSH9:0. If FRFSH9:0 = 0x000, then the RFSH/FLT pin outputs high. If FRFSH9:0 = 0x001~0x3FF, the RFSH/FLT pin outputs a rectangle signal. The refresh frequency can be calculated with Equation (3):

$$f_{REFRESH} = \frac{127500}{FRFSH9:0} \quad (3)$$

Note that if FPWM1:0 = 01, the PWM dimming frequency is 250Hz. If FRFSH9:0 = 0x000, the RFSH/FLT pin outputs high.

The refresh frequency is also related to the PWM dimming frequency, estimated with Equation (4):

$$f_{REFRESH} = \frac{127500}{FRFSH} \times \frac{f_{PWM}}{250} \ (Hz) \quad (4)$$

Where $f_{REFRESH}$ is the refresh frequency, FRFSH is the value of FRFSH9:0, and f_{PWM} is PWM dimming frequency set by register FPWM1:0 (it can be either 200Hz, 250Hz, 280Hz, or 330Hz).

For this equation, FRFSH9:0 > 0.

Note that all numbers in the equation have a decimal base, and that the refresh frequency does not change until the 8MSB are written.

The internal oscillator is divided by 8. As the clock refreshes the frequency generation, the FRFSH9:0 register sets the counter number (see Figure 5).

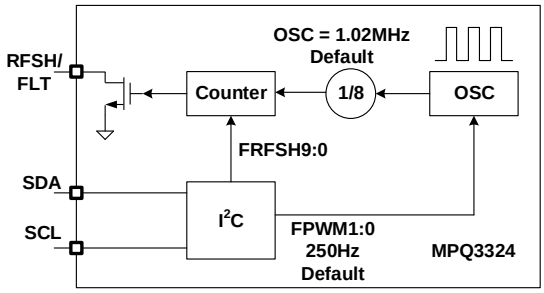


Figure 5: Refresh Frequency Generation

LED Current Slew Rate Control

Changing the LED current's rising/falling slew rate during PWM dimming can optimize EMI performance. The LED current rising/falling slew rate is controlled by SLEW1:0. The slew rate can be set to the values listed below:

- SLEW1:0 = 00: no slew rate
- SLEW1:0 = 01: 5μs
- SLEW1:0 = 10: 10μs
- SLEW1:0 = 11: 20μs

Protections

The MP3324 employs V_{IN} under-voltage lockout (UVLO), LED short protection, LED open-load protection, and thermal shutdown.

The RFSH/FLT pin is active low, open drain, and should be pulled high to an external voltage source. If a protection is triggered, the corresponding fault bit is set, and RFSH/FLT is pulled low.

In hiccup mode, the RFSH/FLT pin is pulled high once the fault condition is removed.

In latch-off mode, the RFSH/FLT pin is released if all of fault bits are read.

For LED open and short protection, hiccup mode or latch-up mode can be selected via the LATCH bit through the I²C.

If LATCH = 1, the MPQ3324 initiates latch-up mode if a fault is triggered. The fault channel stays off until VIN or EN is turned off and reset.

If LATCH = 0, the MPQ3324 operates in hiccup mode. In this mode, the fault channel tries to conduct for 32μs to detect if the fault is cleared. This process is repeated every 1ms. RFSH/FLT is released if fault condition is removed.

V_{IN} Under-Voltage Lockout (UVLO)

If the input voltage drops to the V_{IN} UVLO threshold, the IC stops working, and all I²C registers are reset.***LED Open-Load Protection***

If an LED open fault occurs, the LEDx (e.g. x = 1, 2, ..., 8) voltage drops. If the LEDx voltage drops below the protection threshold (about 100mV) for 4ms, LED open-load protection is triggered. Once this occurs, the fault channel turns off, the corresponding CHxO (x = 1, 2, ..., 8) open fault bit is set, and the RFSH/FLT pin is pulled low. The fault bit is reset when it is read, and the RFSH/FLT pin is pulled high.

LED Short Protection

If an LED short condition occurs, the VIN - VLEDx voltage drops. If the VLEDx (e.g. x = 1, 2, ..., 8) voltage exceeds the voltage set by STH for 4ms, LED short protection is triggered. Once this occurs, the short channel turns off, the corresponding CHxS fault bit is set, and RFSH/FLT pulls low.

The LED short protection threshold is configured by STH1:0, and can be set to the following values:

- STH1:0 = 00: 2V
- STH1:0 = 01: 3V
- STH1:0 = 10: 4V
- STH1:0 = 11: 5V

The fault bit is reset when it is read, and the RFSH/FLT pin is pulled high.

Over-Temperature Protection (OTP)

If the IC temperature exceeds 170°C, over-temperature protection (OTP) is triggered. All channels turn off, the RFSH/FLT pin is pulled low, and the FT_OTP bit is set. If the temperature drops by 20°C, the IC recovers, all channels turn on, and the part resumes normal operation.

I²C Interface Register

I²C Chip Address

The device's address is 0x30~0x39, and is configured by the ADDR resistor. The internal current source flows to the ADDR resistor, then the voltage of ADDR determines the I²C address. 10 different addresses can be configured through the ADDR resistor. Table 2 shows how the relationship between I²C address and resistor ratio the (R_{ADDR} / R_{ISET}).

Table 2: I²C Address Setting

R_{ADDR} / R_{ISET}	I²C Address (A3, A2, A1, A0)
<0.05	0000
>0.05, <0.15	0001
>0.15, <0.25	0010
>0.25, <0.35	0011
>0.35, <0.45	0100
>0.45, <0.55	0101
>0.55, <0.65	0110
>0.65, <0.75	0111
>0.75, <0.85	1000
>0.85, <0.95	1001

At start-up, the IC checks the I²C address first. This address remains the same during normal operation, unless the IC's power is reset.

After the start condition, the I²C-compatible master sends a 7-bit address followed by an 8th read (1) or write (0) bit. The 8th bit indicates the register address to/from which the data will be written/read (see Figure 6).

0	1	1	A3	A2	A1	A0	R/W

Figure 6: The I²C-Compatible Device Address

To avoid a glitch during normal operation, ensure that the following conditions are met:

- Change the FPWM1:0 value only when the EN bit is set to 0.
- Write the FPWM register and wait for a 10μs delay before writing other registers.

REGISTER MAP

Add	Default	D7	D6	D5	D4	D3	D2	D1	D0
00H	01	RESERVED						FPWM 1:0	
01H	00	FLTEN	LATCH	STH1:0		SLEW1:0		PS_EN	EN
02H	01	RESERVED					FT_OTP	FRFSH1:0	
03H	6A	FRFSH 9:2							
04H	FF	CH8EN	CH8EN	CH7EN	CH7EN	CH6EN	CH6EN	CH5EN	CH5EN
05H	FF	CH4EN	CH4EN	CH3EN	CH3EN	CH2EN	CH2EN	CH1EN	CH1EN
06H	00	RESERVED	CH8O	RESERVED	CH7O	RESERVED	CH6O	RESERVED	CH5O
07H	00	RESERVED	CH4O	RESERVED	CH3O	RESERVED	CH2O	RESERVED	CH1O
08H	00	RESERVED	CH8S	RESERVED	CH7S	RESERVED	CH6S	RESERVED	CH5S
09H	00	RESERVED	CH4S	RESERVED	CH3S	RESERVED	CH2S	RESERVED	CH1S
0AH	3F	RESERVED		ICH1 5:0					
0BH	0F	RESERVED				PWM1 3:0			
0CH	FF	PWM1 11:4							
0DH	3F	RESERVED		ICH1 5:0					
0EH	0F	RESERVED				PWM1 3:0			
0FH	FF	PWM1 11:4							
10H	3F	RESERVED		ICH2 5:0					
11H	0F	RESERVED				PWM2 3:0			
12H	FF	PWM2 11:4							
13H	3F	RESERVED		ICH2 5:0					
14H	0F	RESERVED				PWM2 3:0			
15H	FF	PWM2 11:4							
16H	3F	RESERVED		ICH3 5:0					
17H	0F	RESERVED				PWM3 3:0			
18H	FF	PWM3 11:4							
19H	3F	RESERVED		ICH3 5:0					
1AH	0F	RESERVED				PWM3 3:0			
1BH	FF	PWM3 11:4							

REGISTER MAP *(continued)*

Add	Default	D7	D6	D5	D4	D3	D2	D1	D0
1CH	3F	RESERVED		ICH4 5:0					
1DH	0F	RESERVED				PWM4 3:0			
1EH	FF	PWM4 11:4							
1FH	3F	RESERVED		ICH4 5:0					
20H	0F	RESERVED				PWM4 3:0			
21H	FF	PWM4 11:4							
22H	3F	RESERVED		ICH5 5:0					
23H	0F	RESERVED				PWM5 3:0			
24H	FF	PWM5 11:4							
25H	3F	RESERVED		ICH5 5:0					
26H	0F	RESERVED				PWM5 3:0			
27H	FF	PWM5 11:4							
28H	3F	RESERVED		ICH6 5:0					
29H	0F	RESERVED				PWM6 3:0			
2AH	FF	PWM6 11:4							
2BH	3F	RESERVED		ICH6 5:0					
2CH	0F	RESERVED				PWM6 3:0			
2DH	FF	PWM6 11:4							
2EH	3F	RESERVED		ICH7 5:0					
2FH	0F	RESERVED				PWM7 3:0			
30H	FF	PWM7 11:4							
31H	3F	RESERVED		ICH7 5:0					
32H	0F	RESERVED				PWM7 3:0			
33H	FF	PWM7 11:4							
34H	3F	RESERVED		ICH8 5:0					
35H	0F	RESERVED				PWM8 3:0			
36H	FF	PWM8 11:4							
37H	3F	RESERVED		ICH8 5:0					
38H	0F	RESERVED				PWM8 3:0			
39H	FF	PWM8 11:4							

PWM Dimming Frequency Setting

Addr: 0x00				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:2	RESERVED	R	000000	Reserved.
1:0	FPWM	R/W	01	Sets the PWM dimming frequency. 00: 220Hz 01: 250Hz 10: 280Hz 11: 330Hz To avoid a glitch during normal operation, ensure that the following conditions are met: • Change the FPWM1:0 value only when the EN bit is set to 0. • Write the FPWM register and wait for a 10µs delay before writing other registers.

Control

Addr: 0x01				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7	FLTEN	R/W	0	Enables the RFSH/FLT pin's fault indication. 0: Disabled. The RFSH/FLT pin refreshes the signal output 1: Enabled. The RFSH/FLT pin indicates if faults occurs
6	LATCH	R/W	1	Enables latch-off mode if a fault occurs. 0: Disabled. Faults trigger hiccup mode 1: Enabled. Faults trigger latch-up mode
5:4	S_TH1:0	R/W	00	Sets the LED short protection threshold. 00: 2V 01: 3V 10: 4V 11: 5V
3:2	SLEW1:0	R/W	00	Sets the LED current slew rate. 00: No slew rate 01: 5µs 10:10µs 11: 20µs
1	PS_EN	R/W	0	Enables the phase shift function. 0: Disabled 1: Enabled. The rising edge of channel x + 1 occurs 80µs after channel x (e.g. x = 1, 2, ..., 7).
0	EN	R/W	0	Enables the IC. 0: IC disabled 1: IC enabled

Refresh Frequency Setting and OTP Fault

Addr: 0x02				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:3	RESERVED	R	0	Reserved.
2	FT_OTP	R	0	Indicates if over-temperature protection (OTP) occurs. 0: No OTP fault has occurred 1: An OTP fault has occurred
1:0	FRFSH1:0	R/W	01	Sets the 2LSB of the refresh frequency. FRFSH 9:0 = 0x000: output a high-level voltage FRFSH 9:0 > 0: the frequency of the output pulse can be calculated with the following equation: $f_{REFRESH}=\frac{127500}{FRFSH}\times\frac{f_{PWM}}{250}$ (Hz) All numbers in the equation have a decimal base. The refresh frequency does not change until the 8MSB is written. The default refresh frequency is 300Hz.

Refresh Frequency Setting

Addr: 0x03				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:0	FRFSH9:2	R/W	6A	Sets the 8MSB of the refresh frequency. FRFSH 9:0 = 0x000: output high-level voltage FRFSH 9:0 > 0: the frequency of the output pulse can be calculated with the following equation: $f_{refresh}=\frac{127500}{FRFSH}\times\frac{f_{PWM}}{250}$ (Hz) All numbers in the equation have a decimal base. The refresh frequency does not change until the 8MSB is written. The default refresh frequency is 300Hz.

Channel Enable (Channel 5–8)

Addr: 0x04				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:6	CH8EN	R/W	11	Enables channel 8. 00: Disabled 11: Enabled
5:4	CH7EN	R/W	11	Enables channel 7. 00: Disabled 11: Enabled
3:2	CH6EN	R/W	11	Enables channel 6. 00: Disabled 11: Enabled

1:0	CH5EN	R/W	11	Enables channel 5. 00: Disabled 11: Enabled

Channel Enable (Channels 1–4)

Addr: 0x05				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:6	CH4EN	R/W	11	Enables channel 4. 00: Disabled 11: Enabled
5:4	CH3EN	R/W	11	Enables channel 3. 00: Disabled 11: Enabled
3:2	CH2EN	R/W	11	Enables channel 2. 00: Disabled 11: Enabled
1:0	CH1EN	R/W	11	Enables channel 1. 00: Disabled 11: Enabled

Channel Open Fault (Channels 5–8)

Addr: 0x06				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7	RESERVED	-	-	Reserved.
6	CH8O	R	0	Channel 8 open protection fault flag. 0: No open protection fault has occurred on channel 8 1: An open protection fault has occurred on channel 8
5	RESERVED	-	-	Reserved.
4	CH7O	R	0	Channel 7 open protection fault flag. 0: No open protection fault has occurred on channel 7 1: An open protection fault has occurred on channel 7
3	RESERVED	-	-	Reserved.
2	CH6O	R	0	Channel 6 open protection fault flag. 0: No open protection fault has occurred on channel 6 1: An open protection fault has occurred on channel 6
1	RESERVED	-	-	Reserved.
0	CH5O	R	0	Channel 5 open protection fault flag. 0: No open protection fault has occurred on channel 5 1: An open protection fault has occurred on channel 5

Channel Open Fault (Channels 1–4)

Addr: 0x07				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7	RESERVED	-	-	Reserved.
6	CH4O	R	0	Channel 4 open protection fault flag. 0: No open protection fault has occurred on channel 4 1: An open protection fault has occurred on channel 4
5	RESERVED	-	-	Reserved.
4	CH3O	R	0	Channel 3 open protection fault flag. 0: No open protection fault has occurred on channel 3 1: An open protection fault has occurred on channel 3
3	RESERVED	-	-	Reserved.
2	CH2O	R	0	Channel 2 open protection fault flag. 0: No open protection fault has occurred on channel 2 1: An open protection fault has occurred on channel 2
1	RESERVED	-	-	Reserved.
0	CH1O	R	0	Channel 1 open protection fault flag 0: No open protection fault has occurred on channel 1 1: An open protection fault has occurred on channel 1

Channel Short Fault (Channel 5-8)

Addr: 0x08				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7	RESERVED	-	-	Reserved.
6	CH8S	R	0	Channel 8 short protection fault flag 0: No short protection fault has occurred on channel 8 1: A short protection fault has occurred on channel 8
5	RESERVED	-	-	Reserved.
4	CH7S	R	0	Channel 7 short protection fault flag 0: No short protection fault has occurred on channel 7 1: A short protection fault has occurred on channel 7
3	RESERVED	-	-	Reserved.
2	CH6S	R	0	Channel 6 short protection fault flag 0: No short protection fault has occurred on channel 6 1: A short protection fault has occurred on channel 6
1	RESERVED	-	-	Reserved.
0	CH5S	R	0	Channel 5 short protection fault flag 0: No short protection fault has occurred on channel 5 1: A short protection fault has occurred on channel 5

Channel Short Fault (Channel 1-4)

Addr: 0x09				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7	RESERVED	-	-	Reserved.
6	CH4S	R	0	Channel 4 short protection fault flag 0: No short protection fault has occurred on channel 4 1: A short protection fault has occurred on channel 4
5	RESERVED	-	-	Reserved.
4	CH3S	R	0	Channel 3 short protection fault flag 0: No short protection fault has occurred on channel 3 1: A short protection fault has occurred on channel 3
3	RESERVED	-	-	Reserved.
2	CH2S	R	0	Channel 2 short protection fault flag 0: No short protection fault has occurred on channel 2 1: A short protection fault has occurred on channel 2
1	RESERVED	-	-	Reserved.
0	CH1S	R	0	Channel 1 short protection fault flag 0: No short protection fault has occurred on channel 1 1: A short protection fault has occurred on channel 1

Channel 1 LED Current Setting

Addr: 0x0A~0x0D				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:6	Reserved	R	00	Reserved.
5:0	ICH1 5:0	R/W	111111	Sets the channel 1 LED current for analog dimming, calculated with the following equation: $I_{LED} = \frac{Code}{63} \times ISET$

Channel 1 PWM Dimming Duty Setting (LSB)

Addr: 0x0B~0x0E				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:4	Reserved	R	0000	Reserved.
3:0	PWM1 3:0	R/W	1111	Sets the 4LSB for the channel 1 LED current PWM dimming duty. The dimming duty only changes once 8MSB is written.

Channel 1 PWM Dimming Duty Setting (MSB)

Addr: 0x0C~0F				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM1 11:4	R/W	11111111	Sets the 8MSB for the channel 1 LED current PWM dimming duty. The dimming duty only changes once 8MSB is written.

Channel 2 LED Current Setting

Addr: 0x10~13				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:6	Reserved	R	00	Reserved.
5:0	ICH2 5:0	R/W	111111	Sets the channel 2 LED current for analog dimming, calculated with the following equation: $I_{LED}=\frac{Code}{63}\times ISET$

Channel 2 PWM Dimming Duty Setting (LSB)

Addr: 0x11~14				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:4	Reserved	R	0000	Reserved.
3:0	PWM2 3:0	R/W	1111	Sets the 4LSB for the channel 2 LED current PWM dimming duty. The dimming duty only changes once 8MSB is written.

Channel 2 PWM Dimming Duty Setting (MSB)

Addr: 0x12~15				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM2 11:4	R/W	11111111	Sets the 8MSB for the channel 2 LED current PWM dimming duty. The dimming duty only changes once 8MSB is written.

Channel 3 LED Current Setting

Addr: 0x16~19				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:6	Reserved	R	00	Reserved.
5:0	ICH3 5:0	R/W	111111	Sets the channel 3 LED current for analog dimming, calculated with the following equation: $I_{LED}=\frac{Code}{63}\times ISET$

Channel 3 PWM Dimming Duty Setting (LSB)

Addr: 0x17~1A				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:4	Reserved	R	0000	Reserved.
3:0	PWM3 3:0	R/W	1111	Sets the 4LSB for the channel 3 LED current PWM dimming duty. The dimming duty only changes once 8MSB is written.

Channel 3 PWM Dimming Duty Setting (MSB)

Addr: 0x18~1B				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM3 11:4	R/W	11111111	Sets the 8MSB for the channel 3 LED current PWM dimming duty. The dimming duty only changes once 8MSB is written.

Channel 4 LED Current Setting

Addr: 0x1C~1F				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:6	Reserved	R	00	Reserved.
5:0	ICH4 5:0	R/W	111111	Sets the channel 4 LED current for analog dimming, calculated with the following equation: $I_{LED} = \frac{Code}{63} \times ISET$

Channel 4 PWM Dimming Duty Setting (LSB)

Addr: 0x1D~20				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:4	Reserved	R	0000	Reserved.
3:0	PWM4 3:0	R/W	1111	Sets the 4LSB for the channel 4 LED current PWM dimming duty. The dimming duty only changes once 8MSB is written.

Channel 4 PWM Dimming Duty Setting (MSB)

Addr: 0x1E~21				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM4 11:4	R/W	11111111	Sets the 8MSB for the channel 4 LED current PWM dimming duty. The dimming duty only changes once 8MSB is written.

Channel 5 LED Current Setting

Addr: 0x22~25				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:6	Reserved	R	00	Reserved
5:0	ICH5 5:0	R/W	111111	Sets the channel 5 LED current for analog dimming, calculated with the following equation: $I_{LED} = \frac{Code}{63} \times ISET$

Channel 5 PWM Dimming Duty Setting (LSB)

Addr: 0x23~26				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:4	Reserved	R	0000	Reserved
3:0	PWM5 3:0	R/W	1111	Sets the 4LSB for the channel 5 LED current PWM dimming duty. The dimming duty only changes once 8MSB is written.

Channel 5 PWM Dimming Duty Setting (MSB)

Addr: 0x24~27				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM5 11:4	R/W	11111111	Sets the 8MSB for the channel 5 LED current PWM dimming duty. The dimming duty only changes once 8MSB is written.

Channel 6 LED Current Setting

Addr: 0x28~2B				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:6	Reserved	R	00	Reserved
5:0	ICH6 5:0	R/W	111111	Sets the channel 6 LED current for analog dimming, calculated with the following equation: $I_{LED} = \frac{Code}{63} \times ISET$

Channel 6 PWM Dimming Duty Setting (LSB)

Addr: 0x29~2C				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:4	Reserved	R	0000	Reserved
3:0	PWM6 3:0	R/W	1111	Sets the 4LSB for the channel 6 LED current PWM dimming duty. The dimming duty only changes once 8MSB is written.

Channel 6 PWM Dimming Duty Setting (MSB)

Addr: 0x2A~2D				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM6 11:4	R/W	11111111	Sets the 8MSB for the channel 6 LED current PWM dimming duty. The dimming duty only changes once 8MSB is written.

Channel 7 LED Current Setting

Addr: 0x2E~31				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:6	Reserved	R	00	Reserved
5:0	ICH7 5:0	R/W	111111	Sets the channel 7 LED current for analog dimming, calculated with the following equation: $I_{LED} = \frac{Code}{63} \times ISET$

Channel 7 PWM Dimming Duty Setting (LSB)

Addr: 0x2F~32				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:4	Reserved	R	0000	Reserved
3:0	PWM7 3:0	R/W	1111	Sets the 4LSB for the channel 7 LED current PWM dimming duty. The dimming duty only changes once 8MSB is written.

Channel 7 PWM Dimming Duty Setting (MSB)

Addr: 0x30~33				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM7 11:4	R/W	11111111	Sets the 8MSB for the channel 7 LED current PWM dimming duty. The dimming duty only changes once 8MSB is written.

Channel 8 LED Current Setting

Addr: 0x34~37				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:6	Reserved	R	00	Reserved
5:0	ICH8 5:0	R/W	111111	Sets the channel 8 LED current for analog dimming, calculated with the following equation: $I_{LED} = \frac{Code}{63} \times ISET$

Channel 8 PWM Dimming Duty Setting Register (LSB)

Addr: 0x35~38				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:4	Reserved	R	0000	Reserved
3:0	PWM8 3:0	R/W	1111	Sets the 4LSB for the channel 8 LED current PWM dimming duty. The dimming duty only changes once 8MSB is written.

Channel 8 PWM Dimming Duty Setting Register (MSB)

Addr: 0x36~39				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM8 11:4	R/W	11111111	Sets the 8MSB for the channel 8 LED current PWM dimming duty. The dimming duty only changes once 8MSB is written.

APPLICATION INFORMATION

LED Current Setting

Connect a resistor from the ISET pin to GND to set the LED current for all 8 channels. The LED current (I_{LED}) can be calculated with Equation (5):

$$I_{LED}(mA)=\frac{500}{R_{ISET}(k\Omega)} \quad (5)$$

For a maximum I_{LED} (about 100mA), ensure that $V_{IN} \geq 4.5V$ to power the IC.

PCB Layout Guidelines

The traces from the LED anode to the LEDx pins must be wide enough to support the set current (up to 100mA) (see Figure 6).

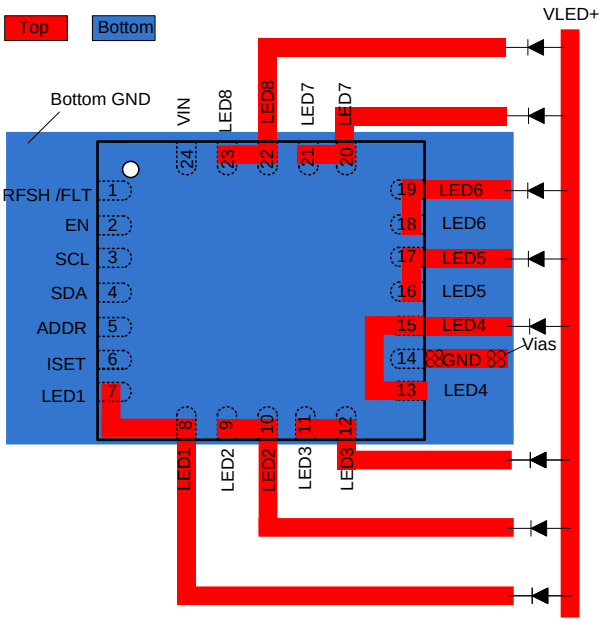


Figure 6: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

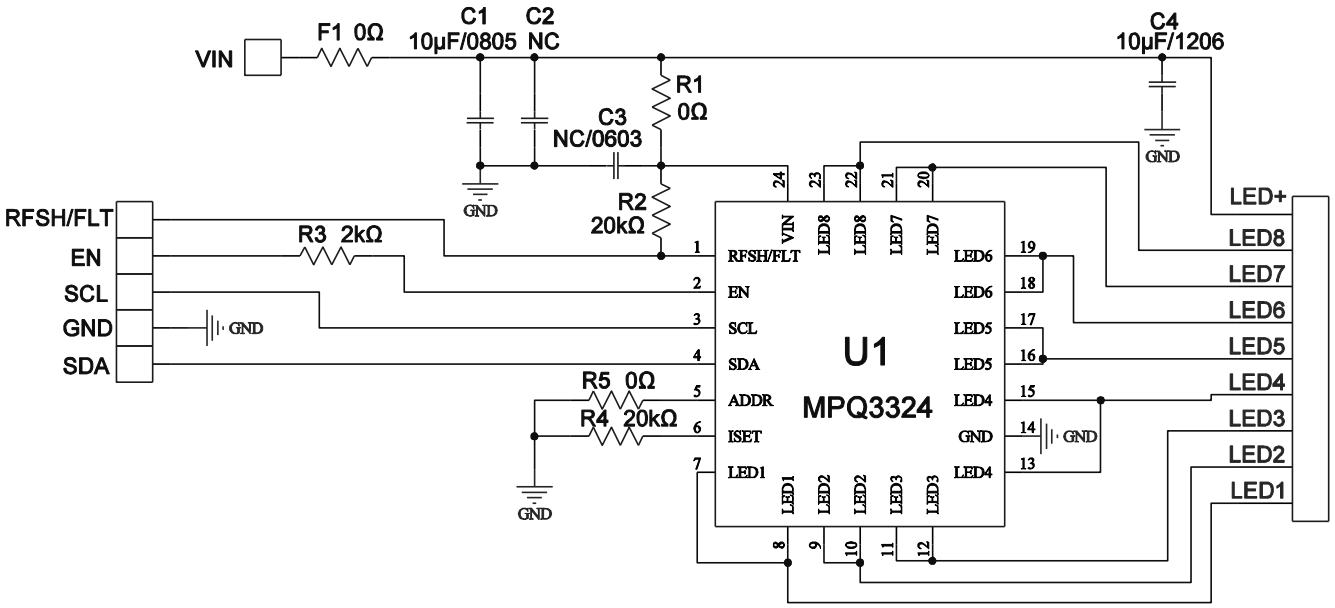


Figure 7: Typical Application Circuit

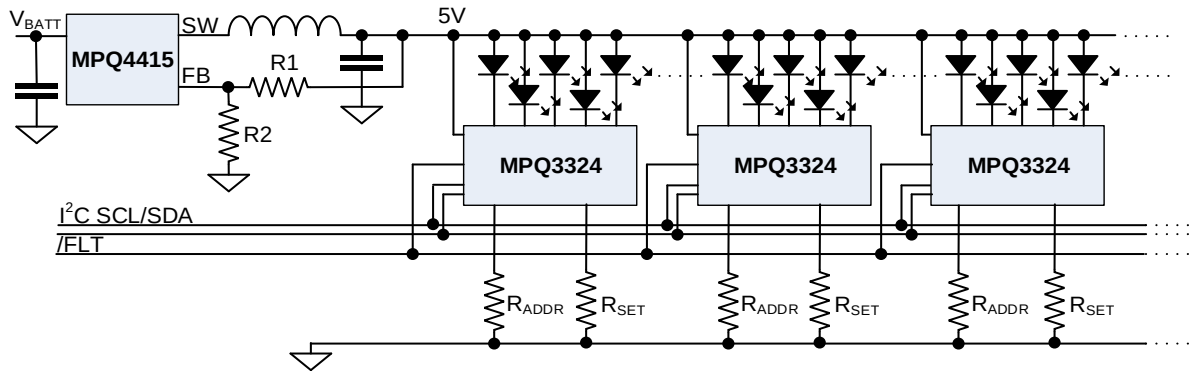
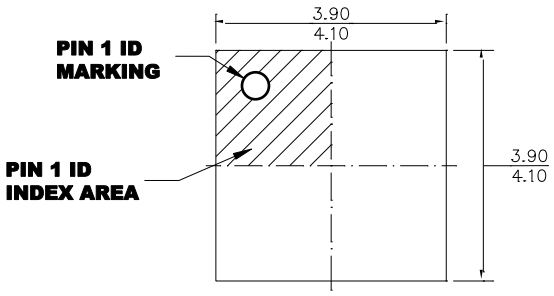


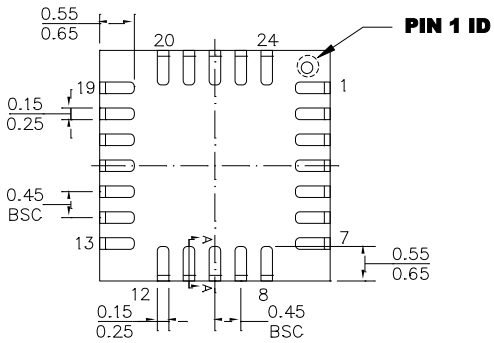
Figure 8: Typical System Application Circuit

PACKAGE INFORMATION

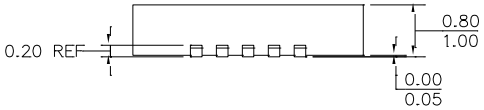
QFN-24 (4mmx4mm) Wettable Flank



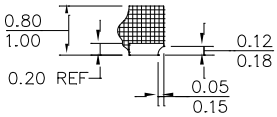
TOP VIEW



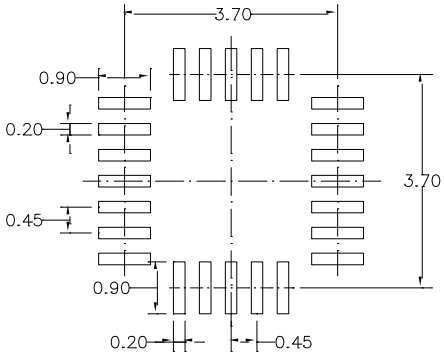
BOTTOM VIEW



SIDE VIEW



SECTION A-A

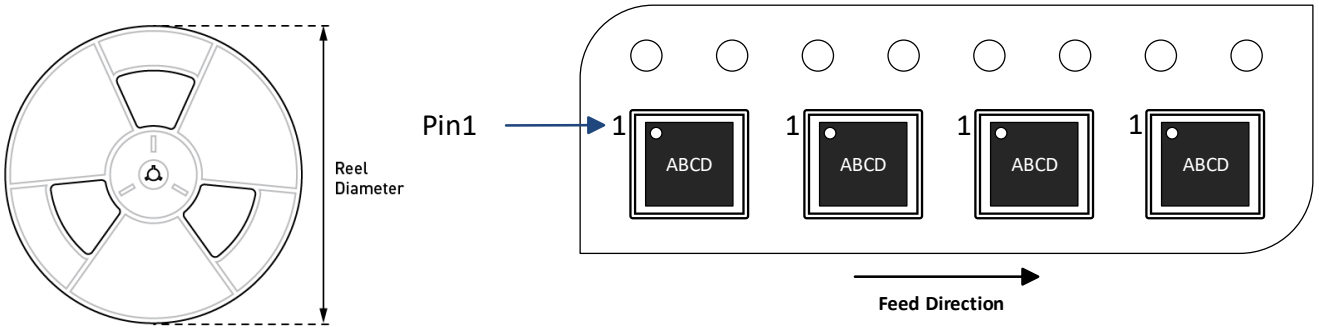


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tray	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ3324GRE-AEC1	QFN-24 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm