MPQ4210

40V, 100W Synchronous Buck-Boost Controller with I^{2}C and Current Monitor, AEC-Q100 Qualified

DESCRIPTION

The MPQ4210 is a synchronous, four-switch, buck-boost controller capable of regulating different output voltages with a wide input voltage range and high efficiency. It provides an I^{2}C interface, which supports V_{OUT} voltage programmability, V_{OUT} slew-rate control, and output constant current limit programmability, making the MPQ4210 suitable for USB power delivery (PD) design in USB Type-C power supplies.

The MPQ4210 uses valley current control in buck mode and peak current control in boost mode, providing fast load transient response and smooth buck-boost mode transient. The MPQ4210 provides forced continuous conduction mode (FCCM) and a programmable average current limit, which supports flexible designs for different applications.

It also features programmable over-current protection (OCP) mode, programmable over-voltage protection (OVP) mode, and programmable V_{IN} UVLO hysteresis.

The MPQ4210 is available in a QFN-27 (5mmx5mm) package.

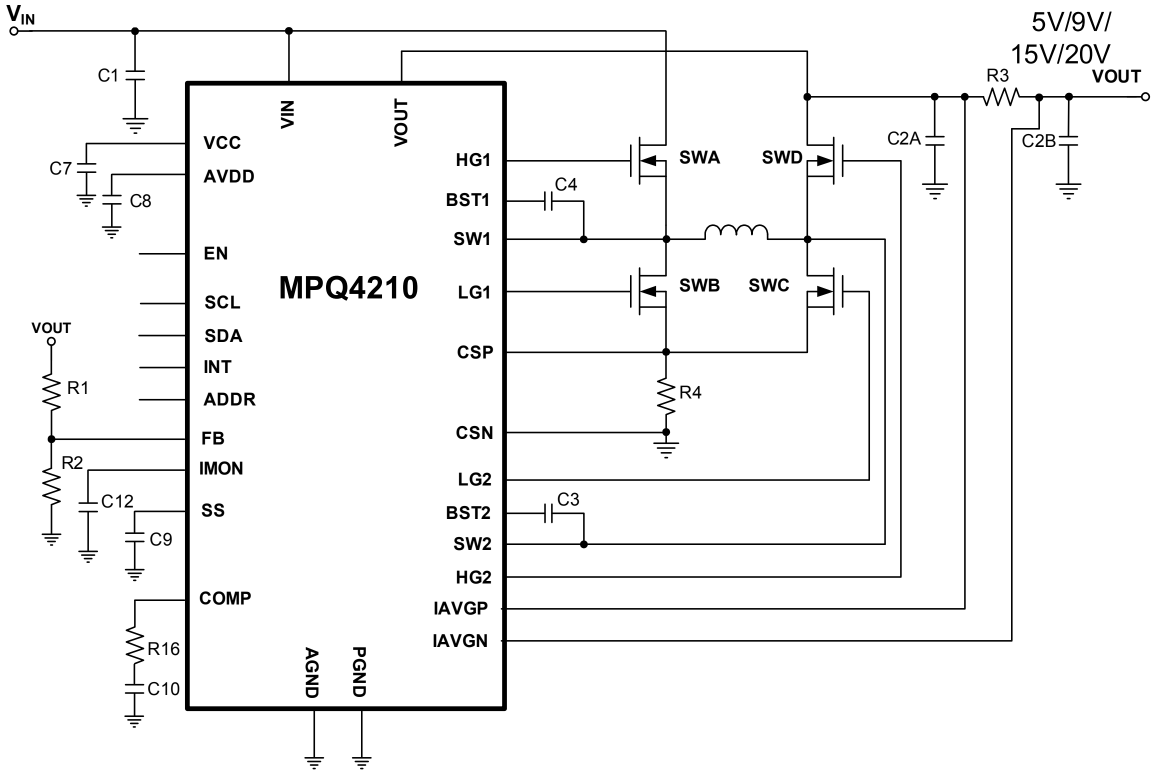
FEATURES

- 6V to 40V Start-Up Input Voltage Range
- 5V to 40V Operation Input Voltage Range
- Flexible I^{2}C Interface Control for:
  - 0.5V to 28V Output Voltage Range
  - 0.3V to 2.047V Reference Voltage Range with 1mV Step
  - Selectable V_{OUT} Slew Rate
  - Programmable Constant Current Limit
- Output Current Monitor Function (IMON)
- Programmable Soft-Start Time
- Switching Frequency Spread Spectrum for EMI Optimization
- Integrated V_{OUT} Discharge Function
- Selectable 200kHz, 300kHz, 400kHz, and 600kHz Switching Frequency
- Forced CCM Operation Mode
- Programmable V_{IN} UVLO Hysteresis
- OCP, SCP, and OVP
- Interrupt Indicator for OCP, OVP, and PNG
- Available in a QFN-27 (5mmx5mm) Package with Wettable Flank
- AEC-Q100 Qualified

APPLICATIONS

- USB Power Delivery
- Industrial PC Power Supplies
- Super-Capacitor Charging

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number	Package	Top Marking
MPQ4210GU-AEC1*	QFN-27 (5mmx5mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MPQ4210GU–AEC1-Z).

TOP MARKING

MPSYYWW
MP4210
LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP4210: Part number
LLLLLLL: Lot number

EVALUATION KIT EVKT-MPQ4210

EVKT-MPQ4210 Kit contents: (Items below can be ordered separately).

#	Part Number	Item	Quantity
1	EVQ4210-U-00B	MPQ4210GU Evaluation Board	1
2	EVKT-USBI2C-02-BAG	Includes USB to I2C Communication interface device, USB Cable, and Ribbon Cable	1

Order direct from MonolithicPower.com or our distributors.

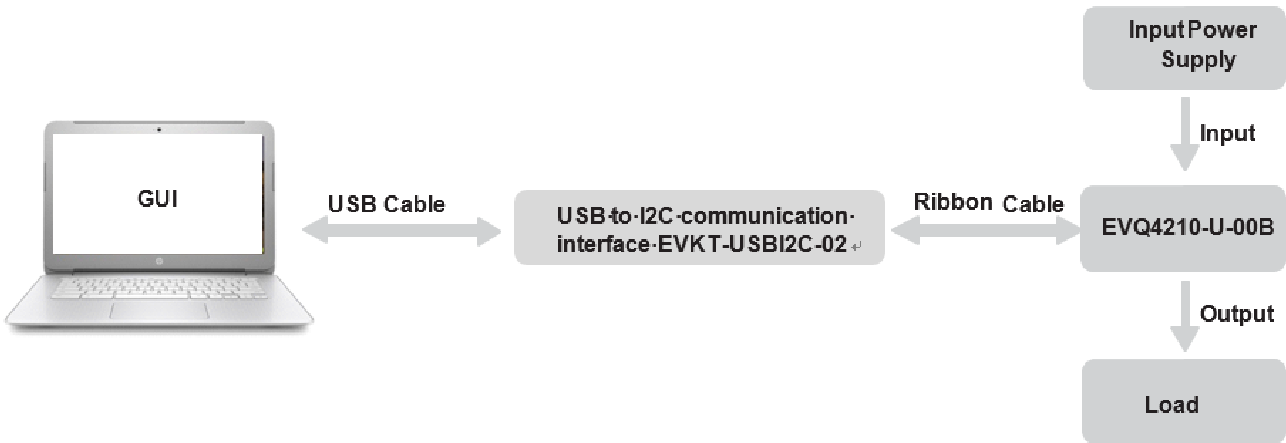
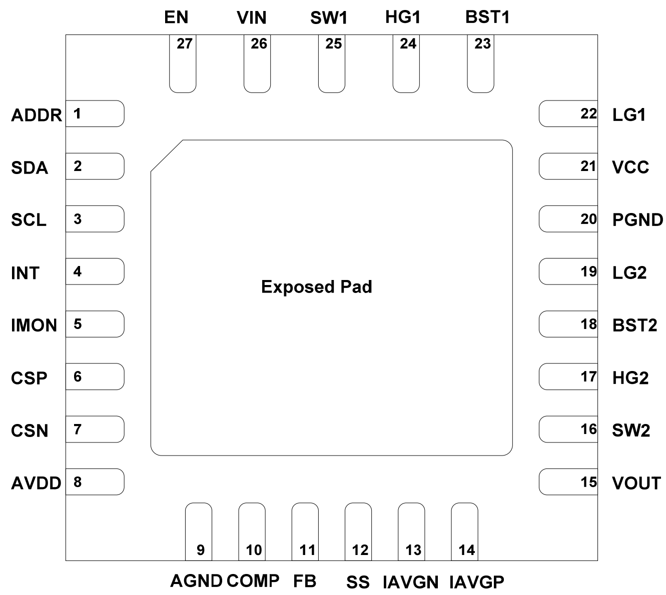


Figure A-1: EVKT-MPQ4210 Evaluation Kit Set-Up

PACKAGE REFERENCE



QFN-27 (5mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
1	ADDR	**I²C slave address set pin.**
2	SDA	**I²C data signal.**
3	SCL	**I²C clock signal.**
4	INT	**Interrupt for PNG, OCP, OTP and OVP events.** In default set-up, INT is masked off for response to a PNG event. It is an open-drain output, and is pulled low when an interrupt event occurs, recovering to open drain when the fault is cleared. INT is an open drain when the IC is not enabled.
5	IMON	**Current monitor output.** Represents the signal between IAVGP and IAVGN.
6	CSP	**Positive input of the switching current-sense signal.** Connect to the high side of the current-sense resistor.
7	CSN	**Negative input of the switching current-sense signal.** Connect to the low side of the current-sense resistor.
8	AVDD	**5V internal control circuit bias supply.** Decouple with a ≥2.2μF capacitor.
9	AGND	**Analog ground.**
10	COMP	**Internal error amplifier output pin.** Connect a capacitor and resistor in series to AGND for loop compensation.
11	FB	**VOUT voltage feedback pin.** Connect a resistor divider from VOUT to FB.
12	SS	**Soft-start set pin.** Sets the hiccup off-time period. Connect an external capacitor to SS.
13	IAVGN	**Negative terminal of average current limit sense input.** The IAVGN and IAVGP pins can only be used for the output current limit setting by connecting to the positive terminal of the output rail.

PIN FUNCTIONS *(continued)*

Pin #	Name	Description
14	IAVGP	**Positive terminal of average current limit sense input.** The IAVGN and IAVGP pins can only be used for the output current limit setting by connecting to the positive terminal of the output rail.
15	VOUT	**Voltage sense input.** Supplies power to VCC based on VCC power logic. Connect to the output capacitor.
16	SW2	**Boost switch node of the converter.** Connect to the source of SWD and the drain of SWC.
17	HG2	**Boost high-side MOSFET gate driver pin.** Connect directly to the gate of SWD.
18	BST2	**Bootstrap power pin for boost high-side MOSFET gate driver.** Connect one capacitor between BST2 and SW2. BST2 is supplied by VCC or BST1.
19	LG2	**Boost high-side MOSFET gate driver pin.** Connect directly to the gate of SWC.
20	PGND	**Power ground.** Gate-driving current return pin.
21	VCC	**Driver circuit and internal bias supply**. Powered by VIN or VOUT. Decouple with a ≥2.2µF ceramic capacitor as close to this pin as possible.
22	LG1	**Buck low-side MOSFET gate driver pin.** Connect directly to the gate of the SWB.
23	BST1	**Bootstrap power pin for buck high-side MOSFET gate driver.** Supplied by VCC or BST2. Connect one capacitor between BST1 and SW1.
24	HG1	**Buck high-side MOSFET gate driver pin.** Connect directly to the gate of SWA.
25	SW1	**Buck switch node of the converter.** Connect to the source of SWA and the drain of SWB.
26	VIN	**VIN power supply and voltage sense input.**
27	EN	**Chip enable control pin.** If not used, connect EN to the input source for automatic start-up. EN can also program VIN UVLO. Do not float this pin.
	Exposed Pad	**Connect to ground.**

ABSOLUTE MAXIMUM RATINGS [1]

VIN, EN .... -0.3V to +45V
VOUT, IAVGP, IAVGN .... -0.3V to +30V

VCC.. -0.3V to +8.5V
SW1, SW2 ....
.... -1V to +45V (-5V to +50V for <20ns)
LG1, LG2 ....
.... -0.3V to +10V (-2V to +11V for <20ns)
BST1, HG1........................ -0.3V to V_{SW1} + 8.5V
BST2, HG2........................ -0.3V to V_{SW2} + 8.5V
All other pins .... -0.3V to +6.5V
Continuous power dissipation [2] [5] 5W
Junction temperature .... 150°C
Lead temperature..................................... 260°C
Storage temperature .... -65°C to +150°C

Recommended Operating Conditions [3]

Start-up voltage (V_{ST})......................... 6V to 40V
Operation voltage (V_{IN}) [4] .... 5V to 40V
Output voltage (V_{OUT})...................... 0.5V to 28V
Operating junction temp (T_J).....-40°C to +125°C

Thermal Resistance	θ_{JA}	θ_{JC}	
EVQ4210-U-00B [5]	25	6	°C/W
JESD51-7 [6]	32	6	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Operation voltage after V_{OUT} is regulated to 5V or higher voltage, and the VCC load is smaller than 10mA.
5) Measured on EVQ4210-U-00B, 6-layer PCB, 2oz-1oz-1oz-1oz-1oz-2oz.
6) The value of θ_{JA} given in this table is only valid for comparison with other packages, and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 12V, V_{EN} = 2V, T_J = -40°C to 125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Operating VCC voltage	V_{CC}	V_{IN} = 6V or V_{OUT} = 6V, 0mA to 20mA on VCC	5.1	5.95	6	V
		V_{IN} = 12V or V_{OUT} = 12V, 0mA to 60mA on VCC	6.7	7.2	7.7	V
VIN UVLO (7)	$VIN_{UVLO\text{-}R}$	VIN rising	5	5.5	5.9	V
VCC UVLO (7)	$VCC_{UVLO\text{-}R}$	VCC falling	3.8	4.3	4.8	V
VCC power source change threshold	VIN_{TH_VCC}	V_{OUT} = 12V, ramp V_{IN} from 5V to 10V	8.1	8.8	9.5	V
	$VOUT_{TH\_VCC}$	V_{IN} = 12V, ramp V_{OUT} from 5V to 10V	8.1	8.8	9.5	V
AVDD voltage	V_{AVDD}	V_{IN} = 12V, 0mA to 5mA	4.7	5.2	5.6	V
Shutdown current	I_{SD}	V_{EN} = 0V, measured on VIN and VOUT pins			2	μA
		ENPWR bit = 0, V_{IN} = 12V, V_O = 0V, measured on VIN pin, V_{EN} = 2V	300	450	600	μA
Enable Control (EN Pin)						
EN turn-on threshold voltage	$V_{EN\text{-}ON}$	V_{EN} rising (switching)	1.25	1.35	1.45	V
EN high threshold voltage	$V_{EN\text{-}H}$	V_{EN} rising (micro-power)			1.1	V
EN low threshold voltage	$V_{EN\text{-}L}$	V_{EN} falling (micro-power)	0.4			V
EN turn-on hysteresis current	$I_{EN\text{-}HYS}$	EN > $V_{EN\text{-}ON}$, EN source current	3.2	4.7	6.2	μA
EN input current	I_{EN}	V_{EN} = 0V, 3.3V		0.01		μA
ENPWR turn-on delay (8)	T_{ENPWR_Delay}	From ENPWR = 1 to switching, C_{SS} = 47nF		1		ms
Feedback Control						
Reference voltage	V_{REF}	VREF bits = 7FFH, T_J = 25°C	-1%	2.047	1%	V
		VREF bits = 7FFH, T_J = -40°C to 125°C	-2%	2.047	2%	V
		VREF bits = 1F4H, T_J = 25°C	-2%	0.5	2%	V
		VREF bits = 1F4H, T_J = -40°C to 125°C	-3%	0.5	3%	V
FB input current	I_{FB}	V_{FB} = 0.52V			200	nA
Error amp transconductance	G_{EA}	V_{FB} = V_{REF} + 10mV, V_{COMP} = 2.5V		1220		μA/V
Comp to current sense gain (8)	G_{CS}	ΔV_{CS} / ΔV_{COMP}		200		mV/V
SS charge current	I_{CHG_SS}	During soft start and overload recovery	2	6	10	μA
SS discharge current	I_{DSG_SS}	After hiccup protection is triggered		1		μA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 12V, V_{EN} = 2V, T_J = -40°C to 125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VREF change slew-rate	T_{REF}	SR = 00	25	38	51	mV/ms
		SR = 11	130	150	170	mV/ms
Current Limit						
Buck valley current limit	I_{LIMIT_BUCK}		113	133	153	mV
Boost peak current limit	I_{LIMIT_BOOST}		130	150	170	mV
OCP hiccup threshold (8)	V_{TH_OCP}			60%		V_{REF}
Average constant current limit	I_{AV_LIMIT}	ILIM bits = 011, IAVGN = 12V, ramp IAVGP voltage up	39	45	51	mV
		ILIM bits = 111, IAVGN = 12V, ramp IAVGP voltage up	60	68	76	mV
CSP and CSN bias current	I_{CS_BIAS}	V_{CSP} = V_{CSN} = 0V		70		µA
IAVGP and IAVGN bias current	I_{AV_BIAS}	IAVGN = 5V IAVGN = 20V IAVGP - IAVGN = 40mV		55		µA
Switching Frequency						
Switching frequency	f_{SW}	f_{SW} bits = 10, V_{OUT} = 5V	300	400	500	kHz
		f_{SW} bits = 00 V_{OUT} = 5V	140	200	260	kHz
Frequency spread span (8)	f_{SS}	Dither bit = 1		±6%		f_{SW}
Frequency spread spectrum modulation frequency (8)	$f_{MODULATION}$	Dither bit = 1		2		kHz
Gate Driver						
Gate source current capability (8)	I_{HG_SO}	V_{CC} = 7.2V, 4.7nF load		0.7		A
	I_{LG_SO}			0.85		A
Gate sink current capability (8)	I_{HG_SI}	V_{CC} = 7.2V, 4.7nF load		1.6		A
	I_{LG_SI}			2		A
Low-side gate output high voltage	V_{LS_HIGH}		V_{CC}-0.05			V
Low-side gate output low voltage	V_{LS_LOW}				0.05	V
High-side gate output high voltage	V_{HS_HIGH}		V_{BST-SW}-0.05			V
High-side gate output low voltage	V_{HS_LOW}				0.05	V
Dead-time between high-side gate and low-side gate (8)	T_{DEAD}			30		ns
OVP Protection						
FB feedback OVP trigger threshold	V_{OVP_RISING}		119%	127%	135%	V_{REF}
FB feedback OVP recover threshold	$V_{OVP\_FALLING}$		104%	111%	118%	V_{REF}
Thermal Protection						
Thermal shutdown (8)	T_{SD}			150		°C
Thermal shutdown hysteresis (8)	T_{SD-HYS}			25		°C

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 12V, V_{EN} = 2V, T_J = -40°C to 125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

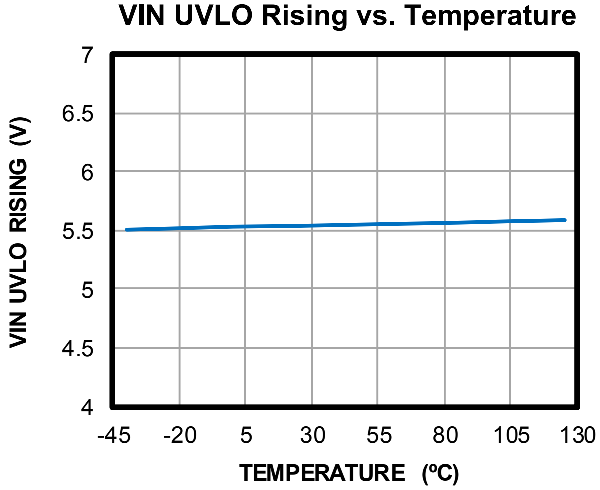
Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Good (INT Pin)						
Power good upper trip threshold	$PG_{H\_FALLING}$	PNG bit sets to 1, and INT pin pulls low	110%	117%	124%	V_{REF}
	PG_{H_RISING}	PNG bit resets to 0, and INT pin rises to high	101%	106.5%	112%	V_{REF}
Power good lower trip threshold	$PG_{L\_FALLING}$	PNG bit sets to 1, and INT pin pulls low	80%	85.5%	91%	V_{REF}
	PG_{L_RISING}	PNG bit resets to 0, and INT pin rises to high	85%	91%	97%	V_{REF}
Power good delay (INT response to PNG event)	PG_{DELAY}	Low to high		10		µs
		VOUT UV, high to low		2		µs
		VOUT OV, high to low		6.5		µs
INT sink current capability	I_{SINK_INT}	Sink 4mA		0.1	0.4	V
INT leakage current	I_{LKG_INT}	V_{INT} = 5V			1	µA
I²C Interface (400kHz)						
Input logic low voltage	V_{LI}	SCL, SDA			0.8	V
Input logic high voltage	V_{HI}	SCL, SDA	2			V
Logic input current	$I_{SCL\_SDA\_LKG}$	SCL/SDA = 5V	-1		1	µA
Output logic low voltage	V_{LO}	SDA, sink 4mA			0.4	V
ADDR Pin Setting Threshold						
Voltage threshold 1	ADDR1	Set I²C address 64H	0.51		0.68	AVDD
Voltage threshold 2	ADDR2	Set I²C address 66H	0.74			AVDD
Pin to GND pull-down resistor	R_{ADDR}	ADDR pin		2		MΩ
Current Monitor Function						
IMON output voltage gain	$GAIN_{IMON}$	+5mV IAVG sense voltage		18.8		V/V
IMON output voltage gain		+55mV IAVG sense voltage	16.92	18.8	20.68	V/V

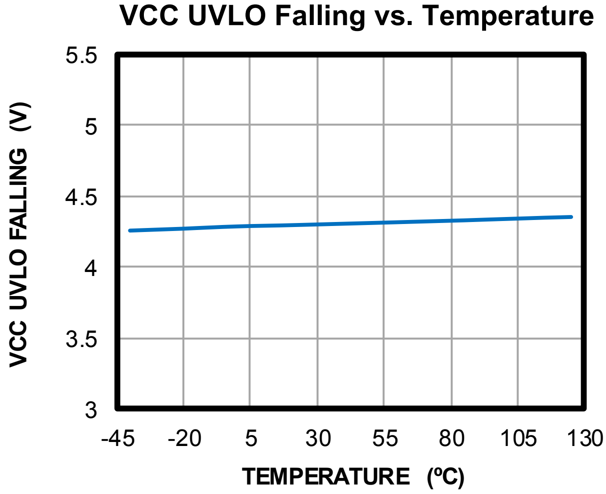
Notes:

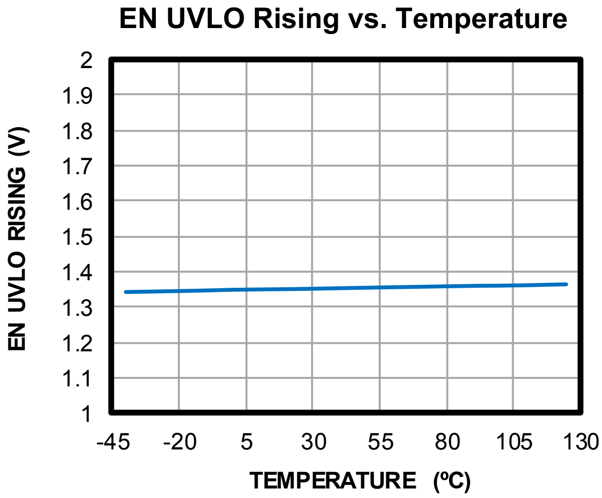
7) The MPQ4210 has a minimum start-up voltage of 6V, and VIN UVLO falling is lower than VCC UVLO falling.
8) Guaranteed by characterization.

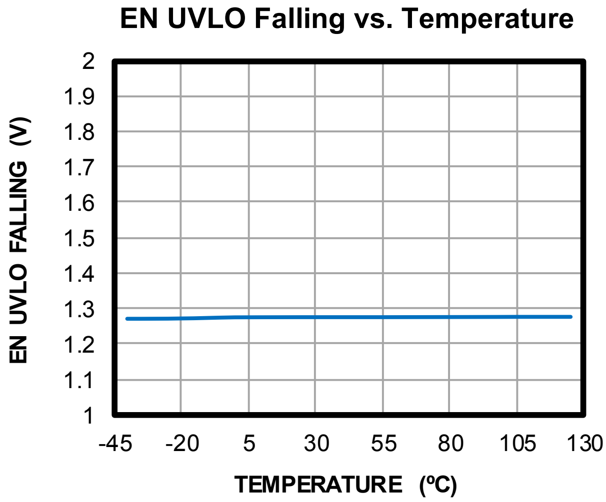
TYPICAL PERFORMANCE CHARACTERISTICS

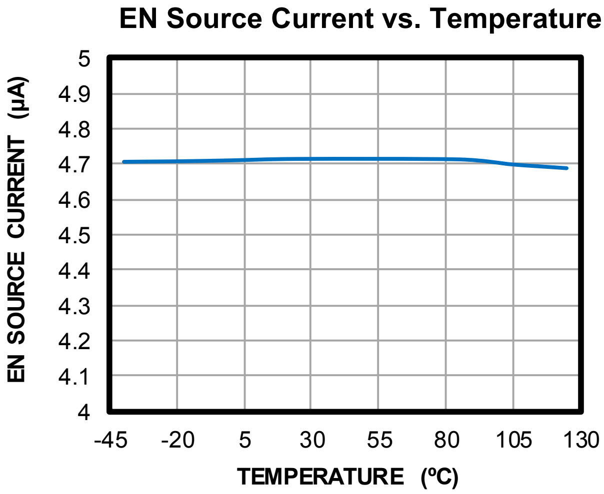
V_{IN} = 12V, V_{OUT} = 5V, L = 4.7μH, T_A = 25°C, unless otherwise noted.

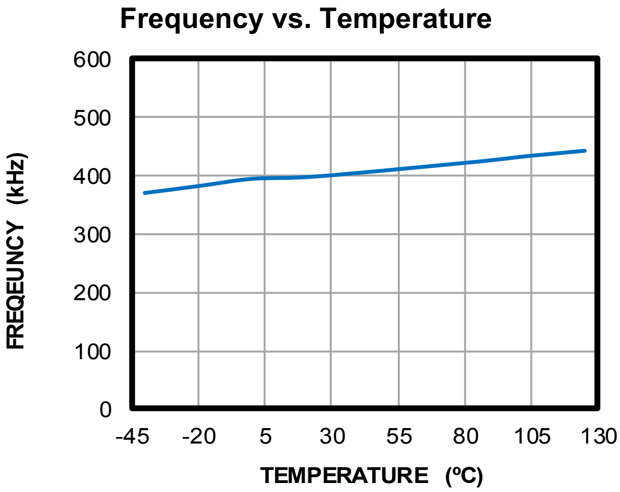








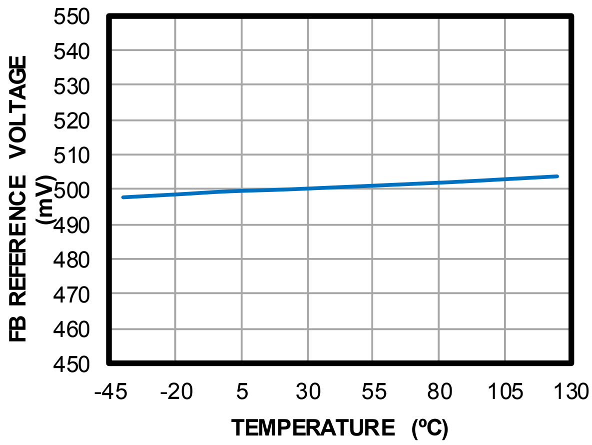




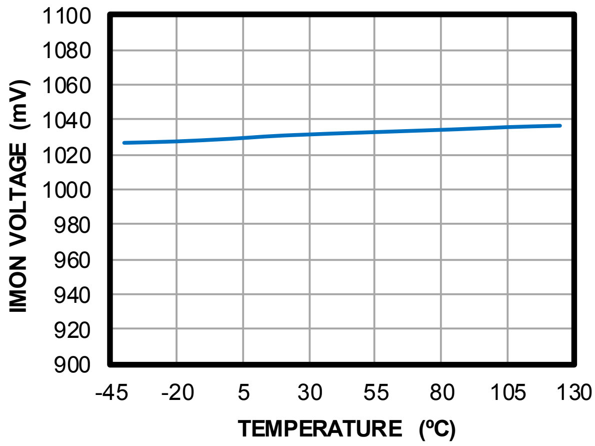
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

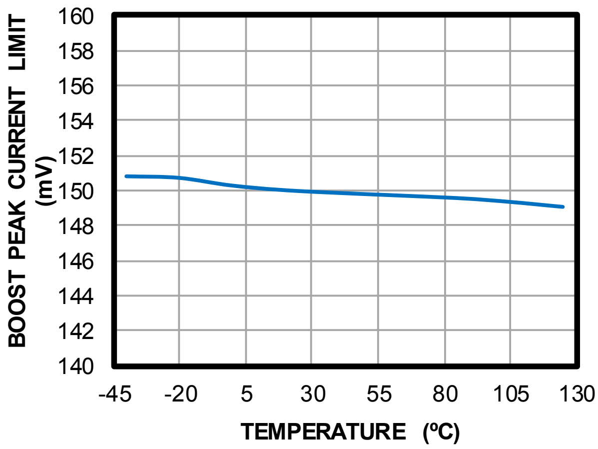
FB Reference Voltage vs. Temperature



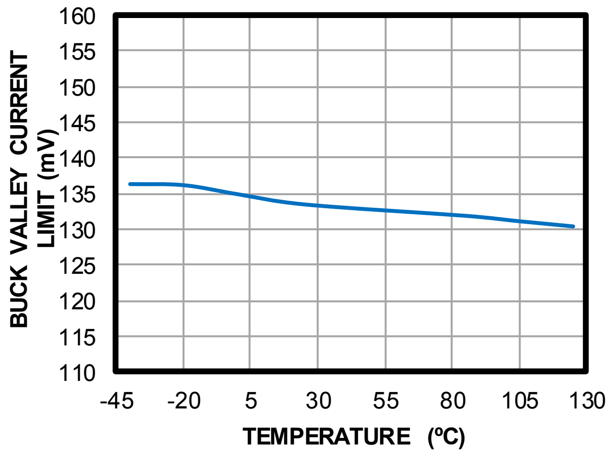
IMON Voltage vs. Temperature



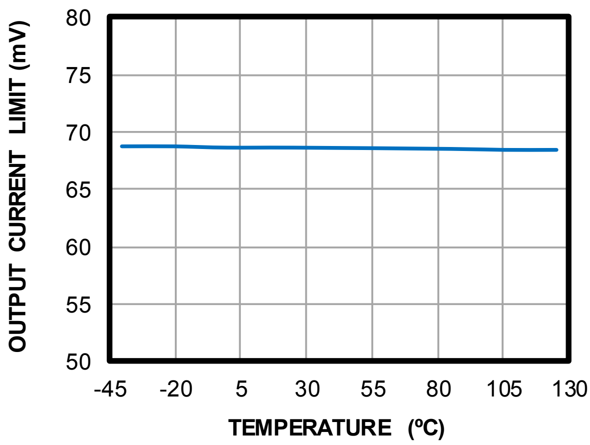
Boost Peak Current Limit vs. Temperature, I_{LIM} = 111b



Buck Valley Current Limit vs. Temperature, I_{LIM} = 111b



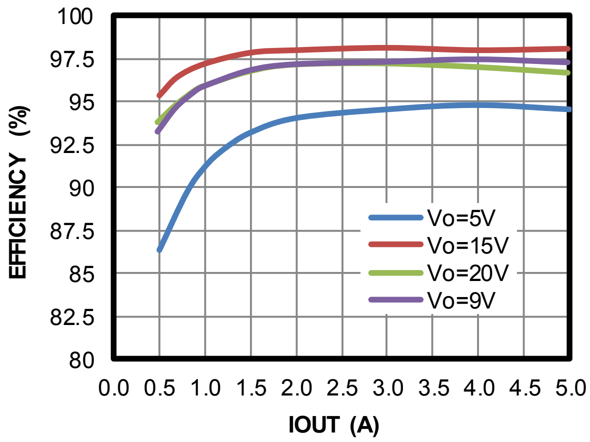
Output Current Limit vs. Temperature, I_{LIM} = 111b



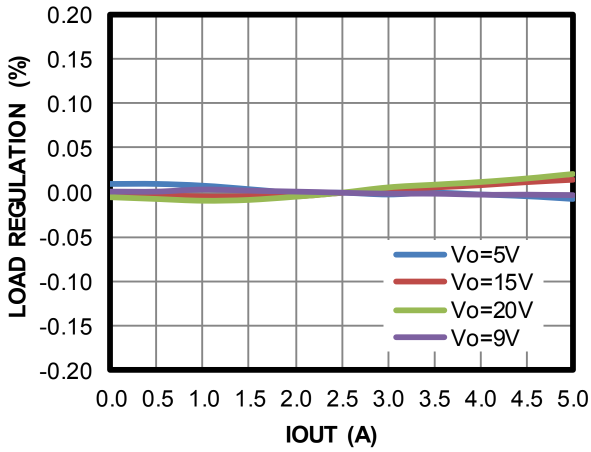
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

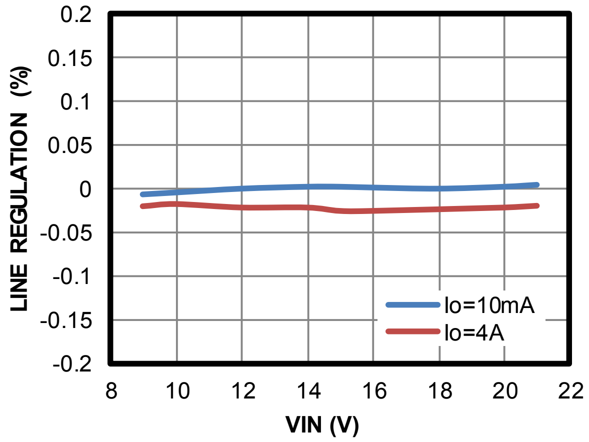
Efficiency vs. Load
V_{IN} = 12V



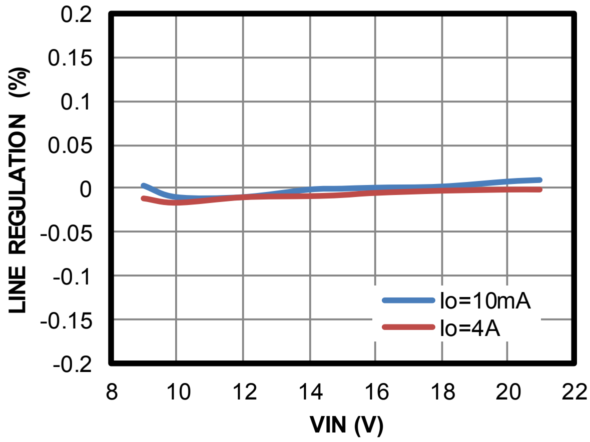
Load Regulation
V_{IN} = 12V



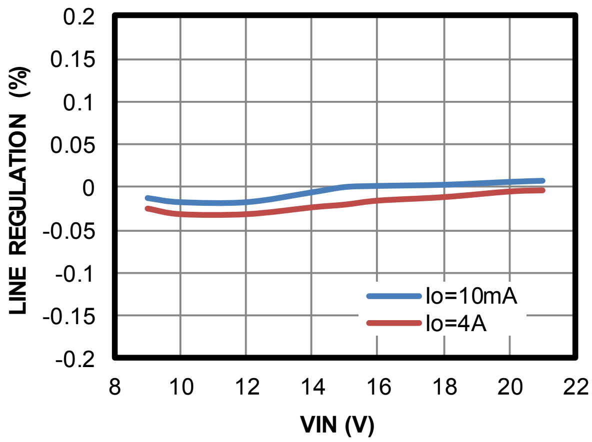
Line Regulation
V_{OUT} = 5V



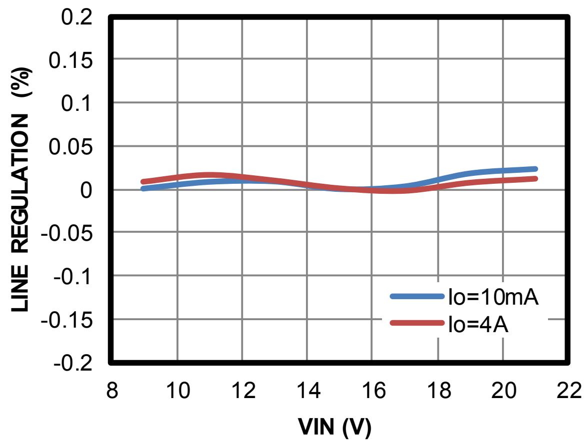
Line Regulation
V_{OUT} = 9V



Line Regulation
V_{OUT} = 15V



Line Regulation
V_{OUT} = 20V

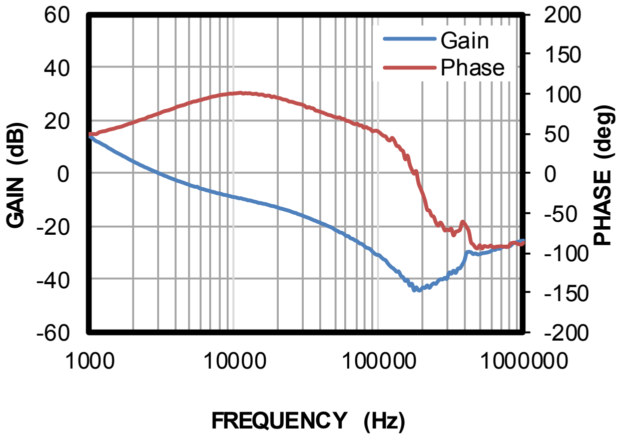


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

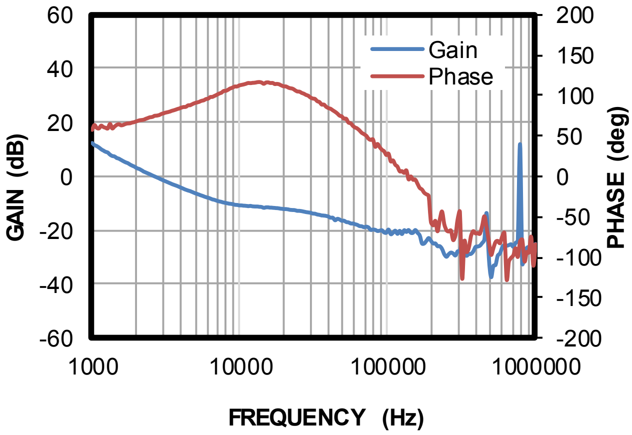
Bode Plot

V_{OUT} = 5V, I_{OUT} = 3A, BW = 3.06kHz, PM = 73.73deg



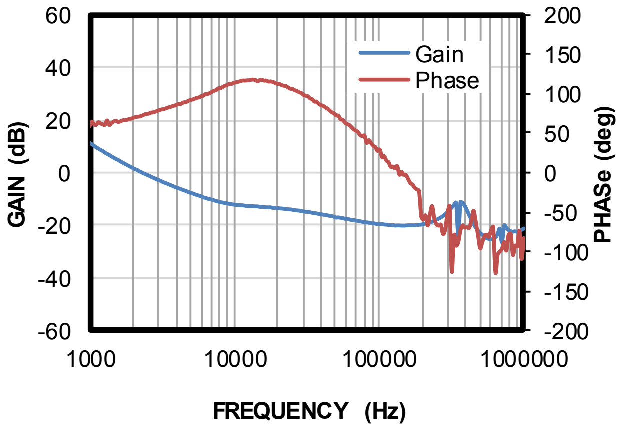
Bode Plot

V_{OUT} = 12V, I_{OUT} = 3A, BW = 2.64kHz, PM = 75deg



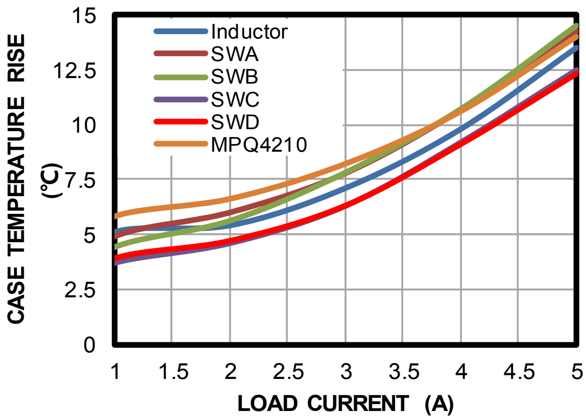
Bode Plot

V_{OUT} = 20V, I_{OUT} = 3A, BW = 2.3kHz, PM = 64.48deg



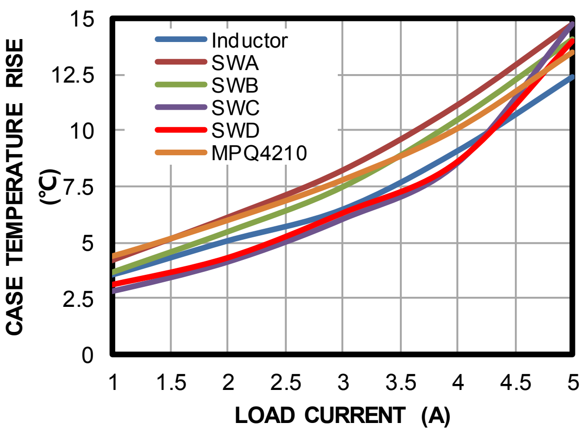
Thermal Rise

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 400kHz, based on EVQ4210-U-00B



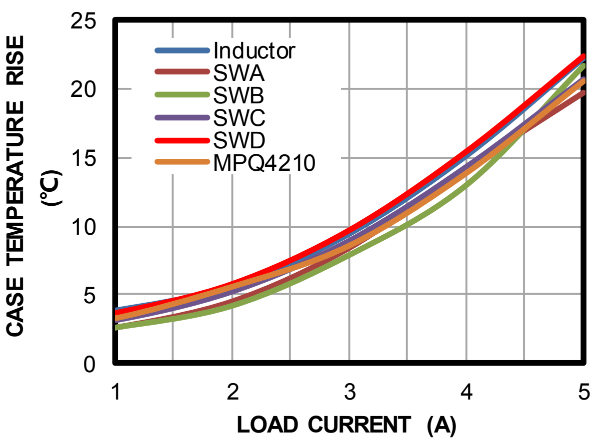
Thermal Rise

V_{IN} = 12V, V_{OUT} = 9V, f_{SW} = 400kHz, based on EVQ4210-U-00B



Thermal Rise

V_{IN} = 12V, V_{OUT} = 15V, f_{SW} = 400kHz, based on EVQ4210-U-00B

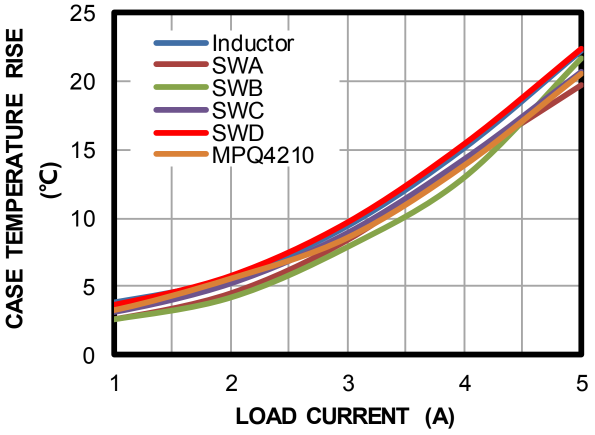


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

Thermal Rise

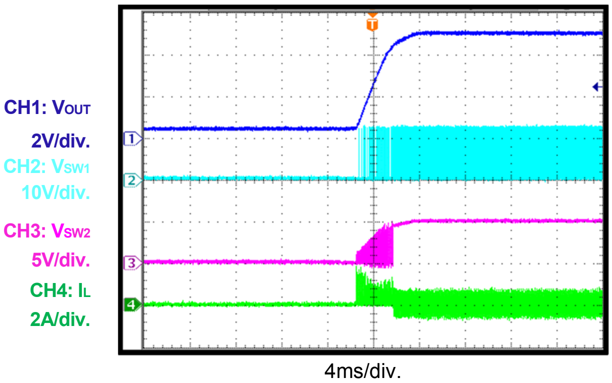
V_{IN} = 12V, V_{OUT} = 20V, f_{SW} = 400kHz, based on EVQ4210-U-00B



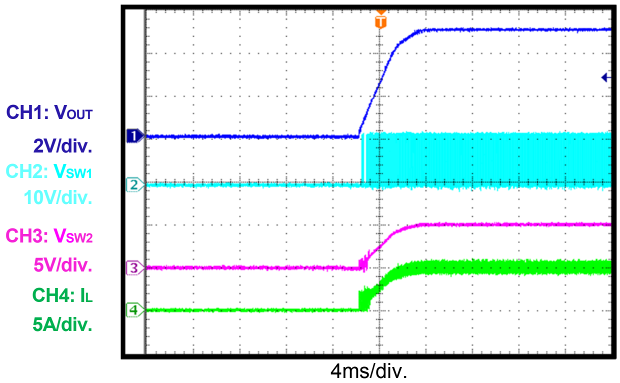
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

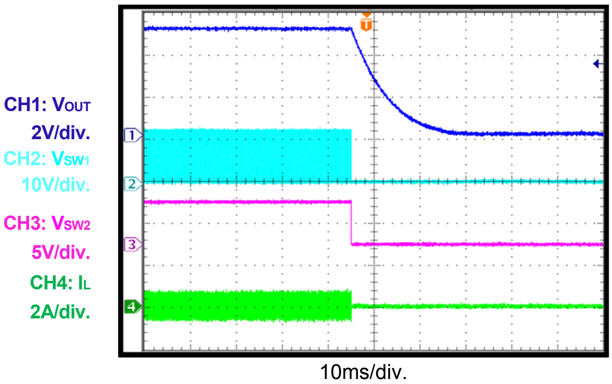
ENPWR Bit Enable through I²C Command, Load = 0A



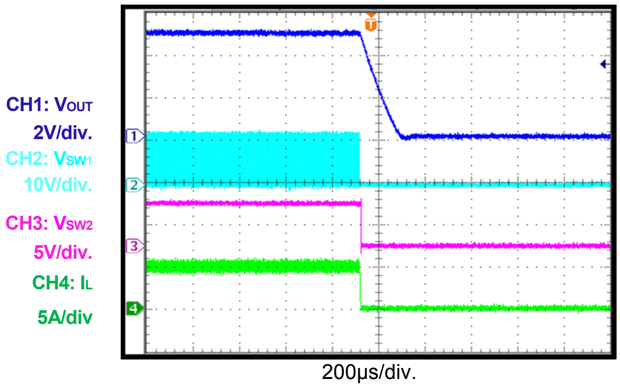
ENPWR Bit Enable through I²C Command, Load = 5A



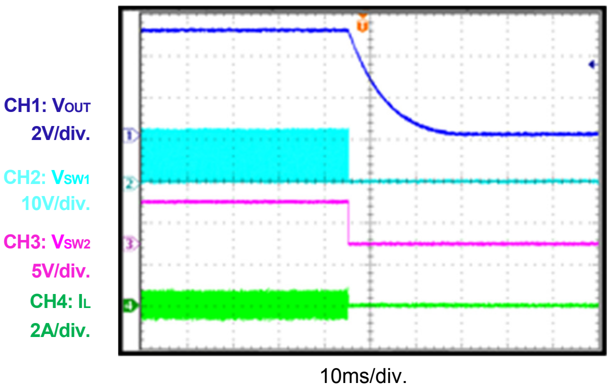
ENPWR Bit Disable through I²C Command, Load = 0A



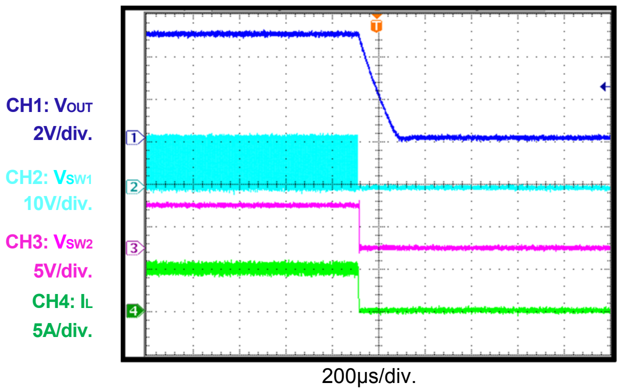
ENPWR Bit Disable through I²C Command, Load = 5A



EN Pin Disable, Load = 10mA



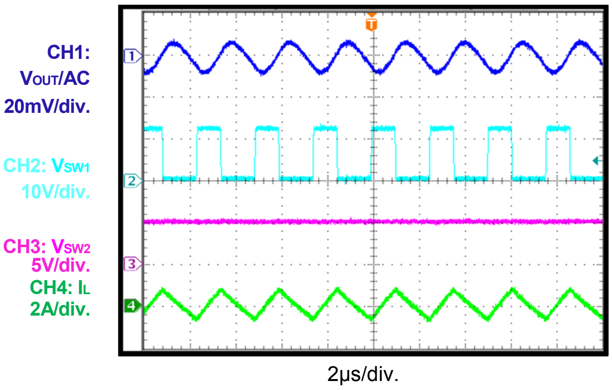
EN Pin Disable, Load = 5A



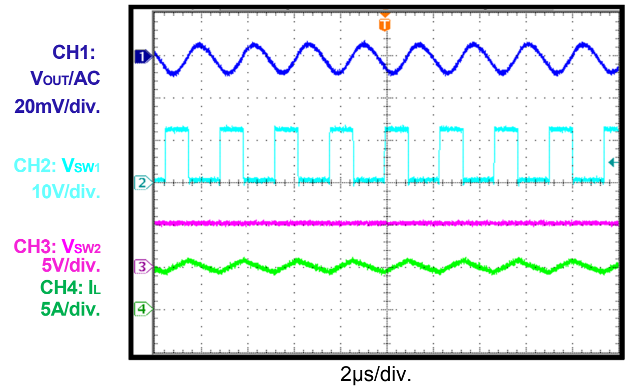
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7μH, T_A = 25°C, unless otherwise noted.

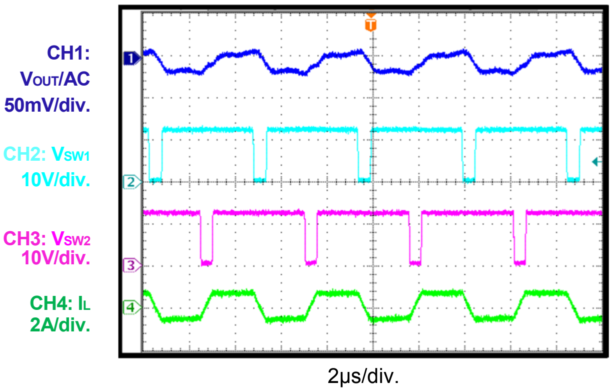
Steady State
V_{OUT} = 5V, load = 0A



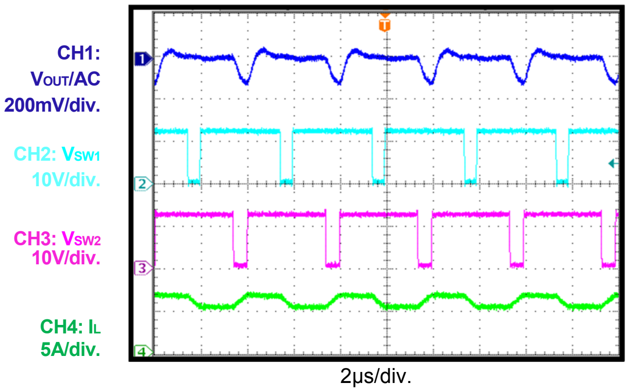
Steady State
V_{OUT} = 5V, load = 5A



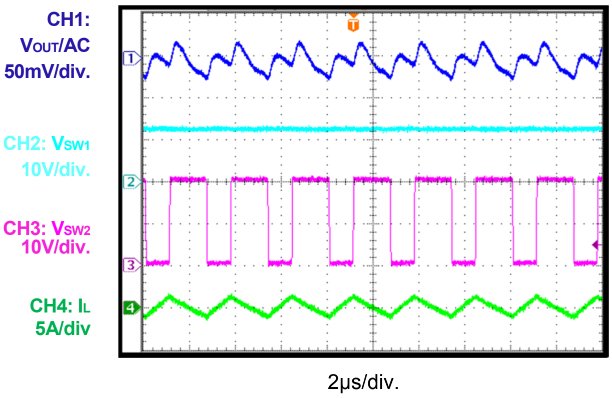
Steady State
V_{OUT} = 12V, BB_FSW = 1, load = 0A



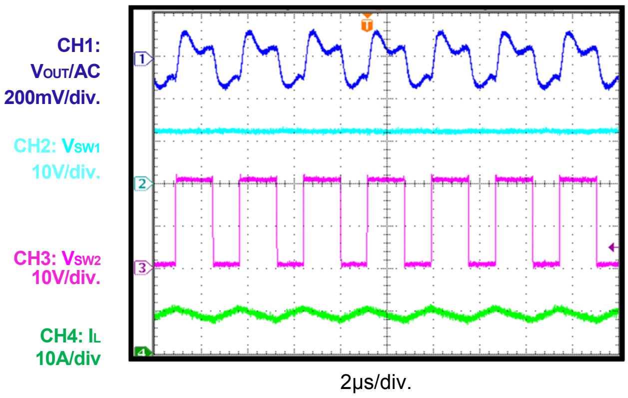
Steady State
V_{OUT} = 12V, BB_FSW = 1, load = 5A



Steady State
V_{OUT} = 20V, load = 0A



Steady State
V_{OUT} = 20V, load = 5A

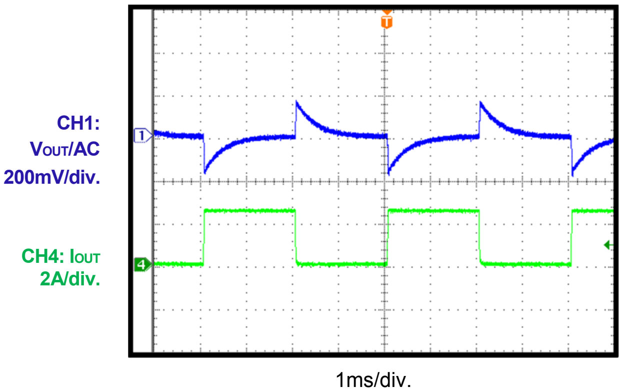


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

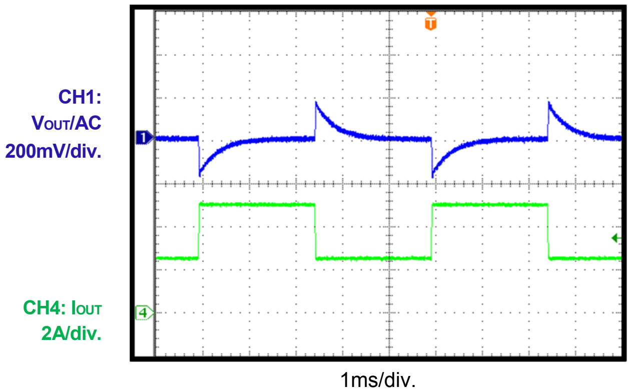
Load Transient

V_{IN} = 12V, V_{OUT} = 5V, load = 0A to 2.5A, 150mA/µs



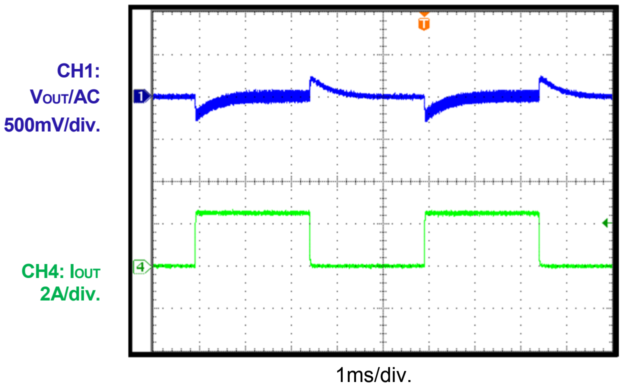
Load Transient

V_{IN} = 12V, V_{OUT} = 5V, load = 2.5A to 5A, 150mA/µs



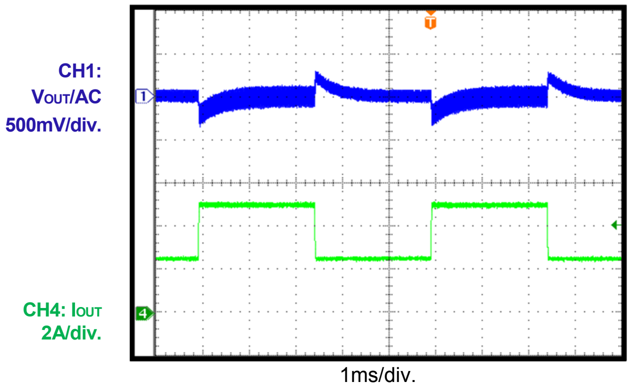
Load Transient

V_{IN} = 12V, V_{OUT} = 20V, load = 0A to 2.5A, 150mA/µs



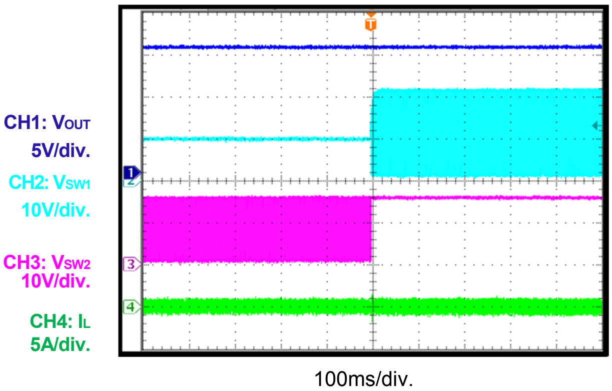
Load Transient

V_{IN} = 12V, V_{OUT} = 20V, load = 2.5A to 5A, 150mA/µs



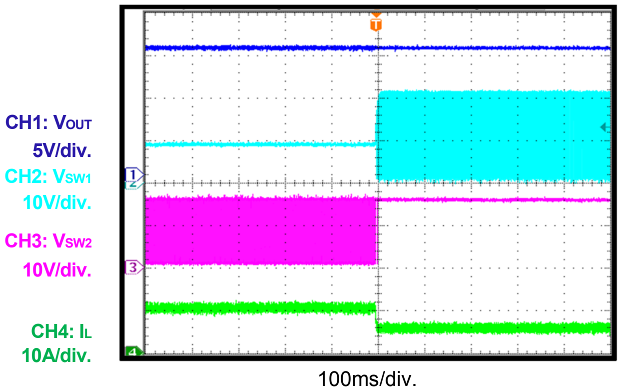
Input Voltage Transient

V_{IN} = 9V to 20V, V_{OUT} = 15V, load = 0A



Input Voltage Transient

V_{IN} = 9V to 20V, V_{OUT} = 15V, load = 5A

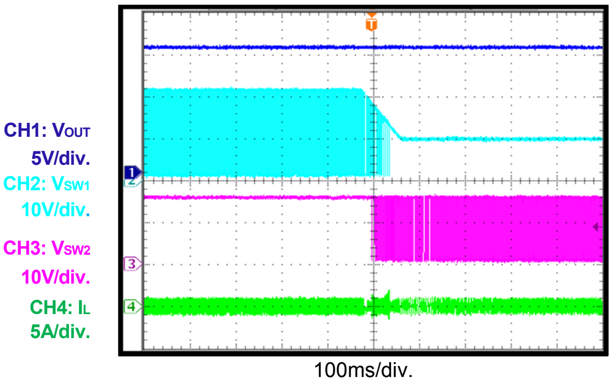


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

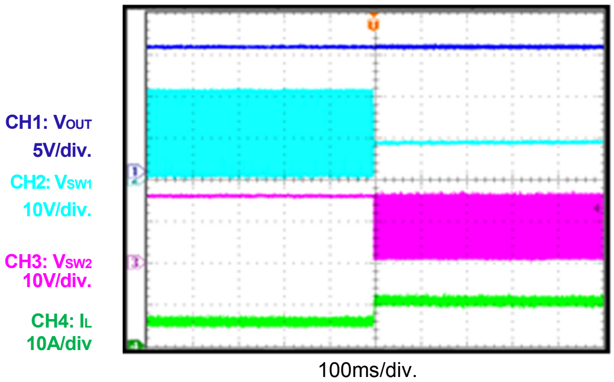
Input Voltage Transient

V_{IN} = 20V to 9V, V_{OUT} = 15V, load = 0A



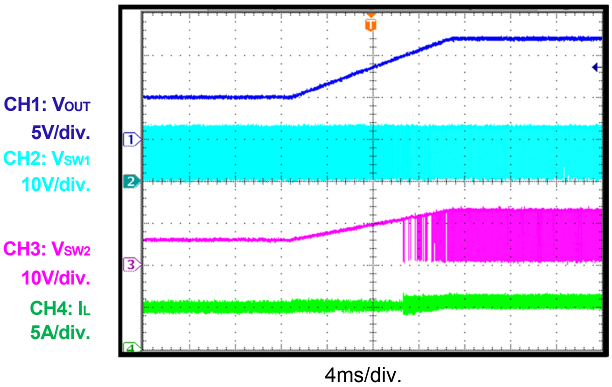
Input Voltage Transient

V_{IN} = 20V to 9V, V_{OUT} = 15V, load = 5A



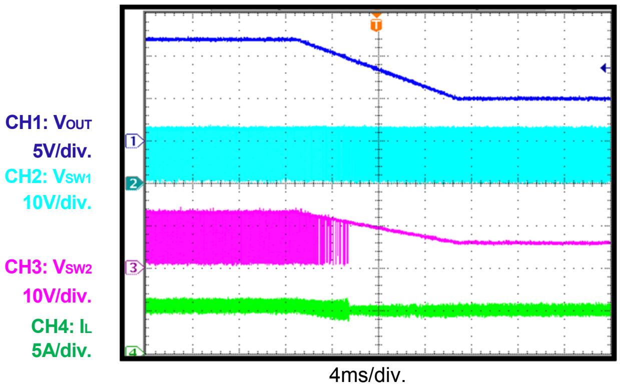
Output Voltage Transient

V_{OUT} = 5V to 12V, I_{OUT} = 5A



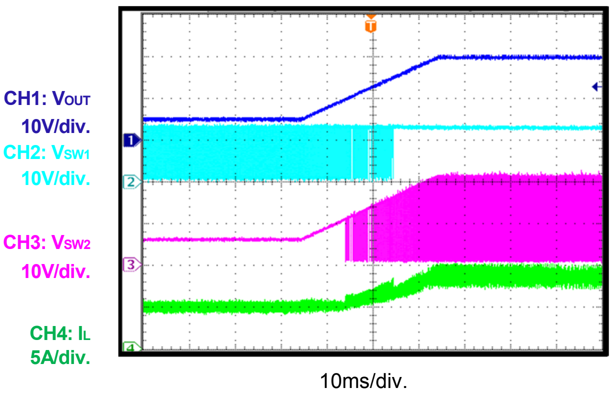
Output Voltage Transient

V_{OUT} = 12V to 5V, load = 5A



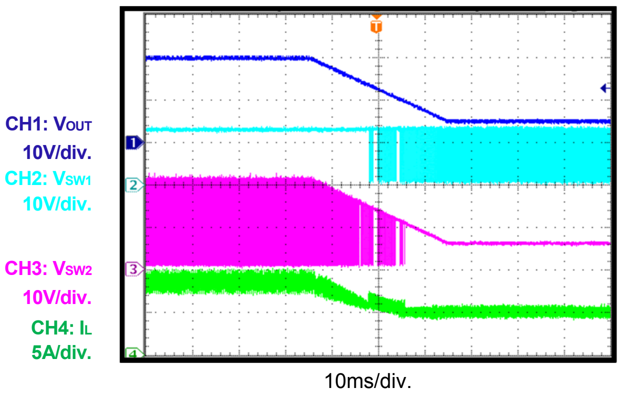
Output Voltage Transient

V_{OUT} = 5V to 20V, load = 5A



Output Voltage Transient

V_{OUT} = 20V to 5V, load = 5A

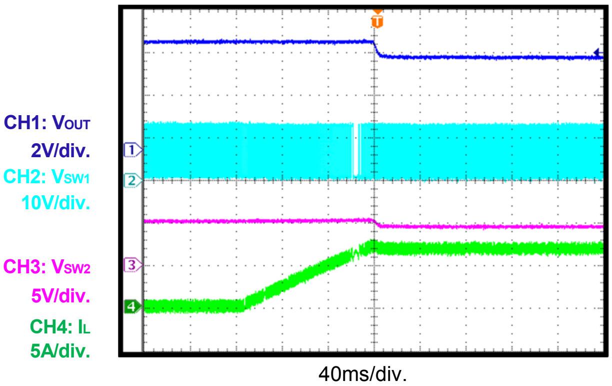


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

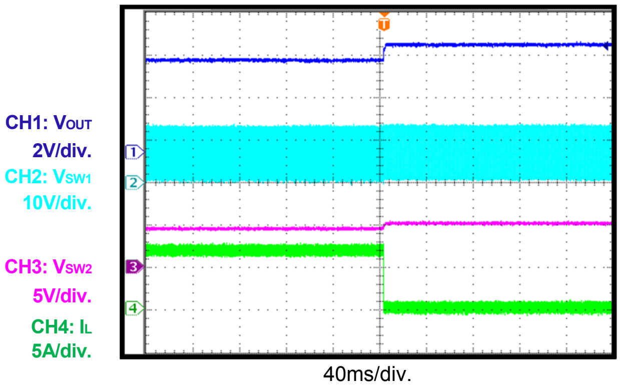
OCP Entry

Ramp up load current slowly



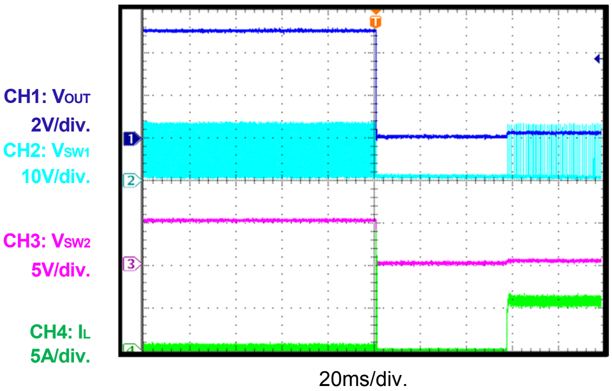
OCP Recovery

Remove load current



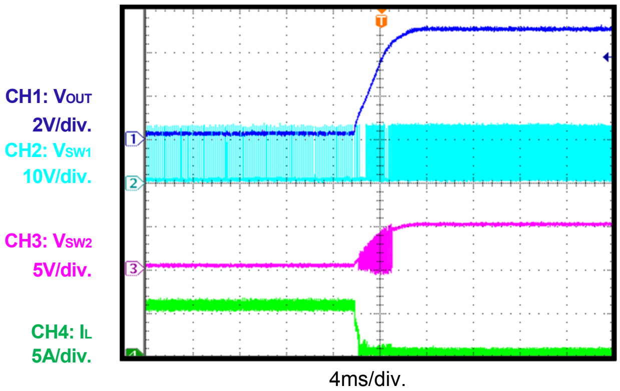
SCP Entry

Short output to ground, R_{CC} = 10mΩ



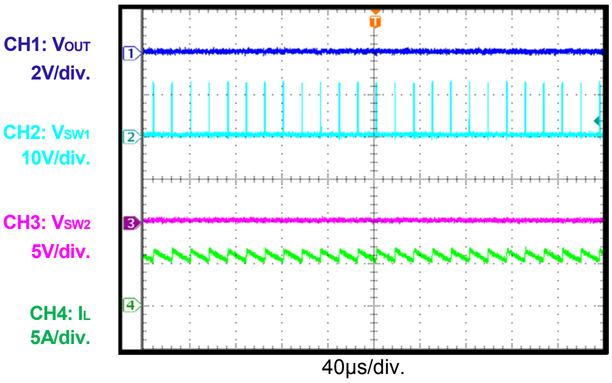
SCP Recovery

Remove short circuit, R_{CC} = 10mΩ



SCP Steady State

Short output to ground, R_{CC} = 10mΩ



FUNCTIONAL BLOCK DIAGRAM

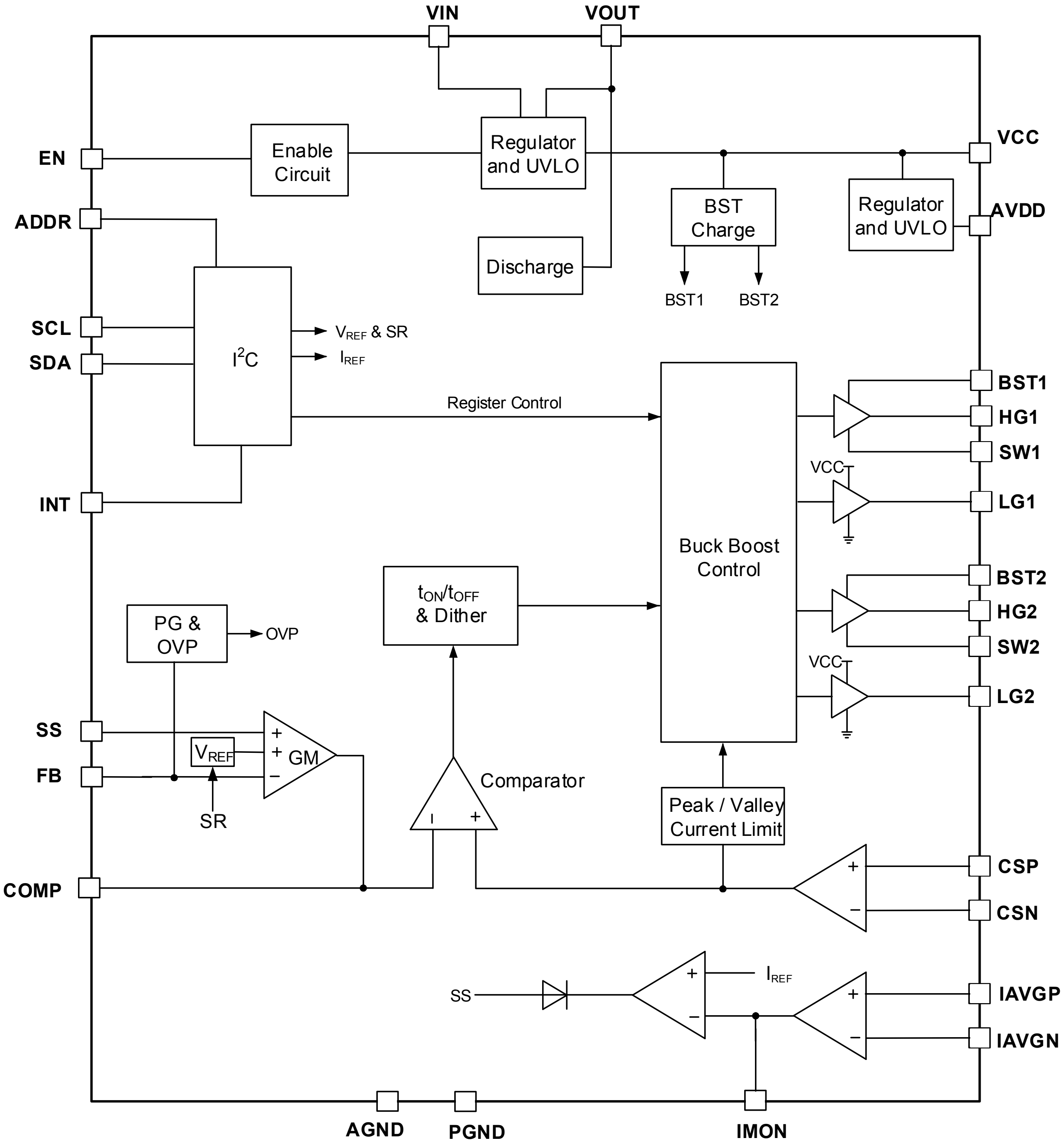


Figure 1: Functional Block Diagram

OPERATION

The MPQ4210 is a four-switch buck-boost controller. It works with fixed frequency in buck, boost, and buck-boost modes. One special buck-boost control strategy provides high efficiency over the device's full input range and smooth transient between different modes. Figure 1 shows the internal block diagram, and the following sections describe the MPQ4210's functions.

Buck-Boost Operation

The MPQ4210 can regulate output above, equal to, or below the input voltage. Based on the one-inductor, four-switch power structure (see Figure 2), it operates in buck mode, boost mode, or buck-boost mode with different V_{IN} inputs (see Figure 3).

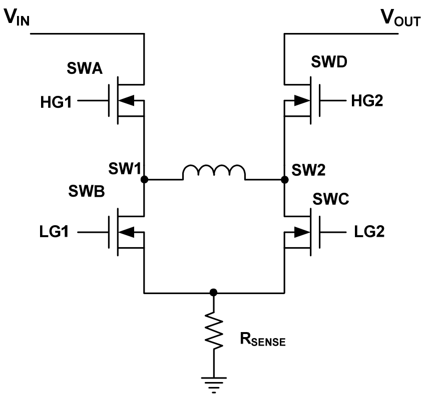


Figure 2: Buck-Boost Topology

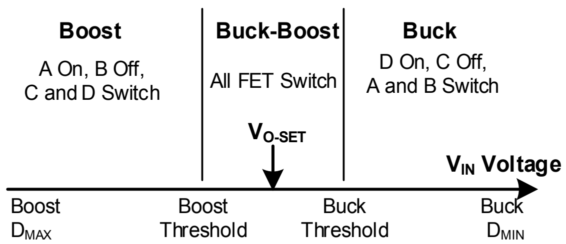


Figure 3: Buck-Boost Operation Range

Buck Mode (V_{IN} > V_{OUT})

When V_{IN} is significantly higher than V_{OUT}, the MPQ4210 works in buck mode. SWA and SWB switch during buck regulation; while SWC is off, SWD remains on to conduct the inductor current.

In each cycle of buck mode, SWA turns on when the FB voltage (V_{FB}) drops below the reference voltage (V_{REF}). After SWA turns off, SWB turns on to conduct the inductor current until it triggers the COMP control signal. By repeating operation in this way, the converter regulates the output voltage.

Boost Mode (V_{IN} < V_{OUT})

When V_{IN} is significantly lower than V_{OUT}, the MPQ4210 works in boost mode. In boost mode, SWC and SWD switch for the boost regulation. While SWB is off, SWA remains on to conduct the inductor current.

In each cycle of boost mode, SWC turns on to conduct the inductor current. When the inductor current rises and triggers the control signal on COMP, SWC turns off and SWD turns on for the current freewheel. Then SWC turns on and off repeatedly to regulate the output voltage in boost mode.

Buck-Boost Mode ($V_{IN} \approx V_{OUT}$)

When V_{IN} is close to V_{OUT}, the converter cannot provide enough energy to load in buck mode due to SWA's minimum off time, or the converter supplies too much power to load in boost mode due to SWC's minimum on time. In these conditions, the MPQ4210 adopts buck-boost control to regulate the output.

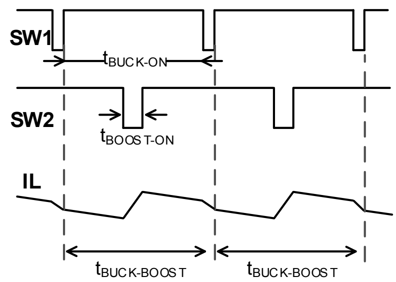


Figure 4: Buck-Boost Waveform

If V_{IN} is close to V_{OUT}, buck-boost mode engages, and one boost switching is inserted into each buck switching period. The MOSFET turn-on sequence is: SWA&SWD → SWA&SWC → SWA&SWD → SWB&SWD. Then the inductor current can meet the COMP voltage requirement, and supply enough current to output.

Power Supply

The MPQ4210's internal circuit is powered by 5.2V AVDD, while the gate drivers are powered by 7.2V VCC. VCC is regulated from V_{IN} and V_{OUT}, while AVDD is powered by VCC.

When V_{IN} power is supplied and EN is high, the MPQ4210 tries to regulate VCC at 7.2V, and at the same time AVDD is regulated to 5.2V. When AVDD rises above the UVLO voltage, the part starts switching if ENPWR is high, and regulates V_{OUT} by soft-start control. If V_{IN} and V_{OUT} are both above 8.8V, the MPQ4210 powers VCC from whichever is the lower voltage source to reduce power-loss. Otherwise, it powers VCC from the higher voltage power source of V_{IN} and V_{OUT} to get enough VCC voltage. VCC and BST have separate UVLO, which keeps the gate signal off. VCC and BST should have enough voltage to enable MPQ4210 switching, except for AVDD UVLO.

The MPQ4210 operates within a 6V to 40V input voltage range. When VCC is powered from VOUT after start-up, the part works until V_{IN} drops below 5V.

When the MPQ4210 is powered off by AVDD_UVLO or the EN signal, the I²C interface cannot respond to the host, and COMP is immediately pulled low. The VCC, AVDD, and BST voltages drop slowly with leakage, but all logic is off.

Start-Up

When the MPQ4210 is enabled, it starts switching with soft-start (SS) control. The SS circuit charges current to the SS pin and ramps the SS voltage up from 0V. It then feeds to the error amplifier to control output voltage. After the SS signal rises to the programmed reference voltage (set by VREF bits), soft start completes and closed-loop regulation starts. The SS voltage rises and clamps at 0.6V higher than V_{REF} in steady state, unless a protection is triggered.

Normally the MPQ4210 starts with buck switching after start-up because V_{OUT} is much lower than V_{IN}. If there is some bias voltage on V_{OUT}, the part will not switch until the SS signal rises above V_{FB}, which is proportional to the V_{OUT} bias voltage. During SS, the IC works in auto PFM mode. OVP and hiccup-OCP do not work during the SS period.

Enable (EN) and Programmable UVLO

The EN pin enables and disables the MPQ4210. When applying a voltage higher than the EN high threshold (>1.1V), the part starts up some of the internal circuits (micro-power mode). If the EN voltage exceeds the turn-on threshold (1.35V), the MPQ4210 enables all functions and starts switching operation. Switching operation is disabled when the EN voltage falls below its lower threshold (<1.28V).

If V_{EN} < 0.4V, the MPQ4210 completely shuts down. After shutdown, the part sinks a small amount of current from the input power (typically <1µA). EN is compatible with voltage up to 40V. For automatic start-up, connect EN directly to VIN. During EN shutdown, the I²C resets to its default value after a 200ms discharge time.

The MPQ4210 features a programmable UVLO hysteresis. When powering up, EN sources a 4.7µA current out of the EN pin (see Figure 5) once the EN voltage is higher than 1.35V. V_{IN} must decrease to overcome the current source and stop switching after the IC starts. The VIN start-and-stop switching threshold is determined with Equation (1) and Equation (2):

$$V_{IN\_ON}(V)=V_{EN\_ON}(V)\times(1+\frac{R_{TOP}}{R_{BOT}})=5.95V \quad (1)$$

$$V_{IN\_OFF}(V)=V_{EN\_OFF}(V)\times(1+\frac{R_{TOP}}{R_{BOT}})-4.7\mu A\times R_{TOP}(k\Omega)\div1000=5.16V \quad (2)$$

Where V_{EN_ON} is about 1.35V (typical), V_{EN_OFF} is about 1.28V.

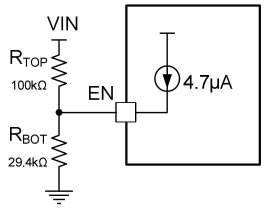


Figure 5: V_{IN} UVLO Program

Forced CCM Mode

The MPQ4210 works in forced continuous conduction mode (FCCM). Buck on time and boost off time are determined by an internal circuit to get fixed frequency, based on the V_{IN}/V_{OUT} ratio. When the load decreases, the average input current drops and the inductor current may go to negative from V_{OUT} to V_{IN} during the SWD on-period. This forces the inductor current to work in continuous mode with fixed frequency, producing a low V_{OUT} ripple.

Switching Current Limit

The MPQ4210 senses the low-side MOSFET current with the CSP and CSN pins. It provides the valley current limit in buck mode and peak current limit in boost mode for each cycle-by-cycle switch. In buck mode, the next period will not start before I_L drops to the valley current limit, so it may foldback the frequency when the valley current limit is triggered. The switching current limit can be programmed with an external sense resistor. The SWB and SWC current signal is blanked internally for about 180ns to enhance noise rejection.

When the cycle-by-cycle current limit is triggered, the interrupt OCP bit is set to 1; and if the OCP bit is not masked off, the INT is pulled low.

During over-current condition, the MPQ4210 runs in cycle-by-cycle current limit. It may also trigger hiccup protection or latch-off protection, depending on the OCP_MODE bit's setting. In hiccup mode, the IC turns off once FB drops below 60% of V_{REF} and triggers the switching current limit after SS period. It will attempt recovery after a fixed off time, programmed by SS capacitor discharge period. In latch-off mode, the IC turns off if FB falls below 60% of V_{REF}. Once the latch off protect is triggered, the chip doesn't recover until a new Vin power cycle, EN toggle or ENPWR bit toggle. If the hiccup and latch-off protections are disabled, the IC continues switching with a cycle-by-cycle current limit. The hiccup and latch-off protections are masked during the SS period.

Based on the cycle-by-cycle switching current limit, the MPQ4210 maximum input current can be calculated with Equation (3) in buck mode and Equation (4) in boost mode:

$$I_{INmax}(A)=\frac{Vo}{VIN}\times\eta\times\left(\frac{\text{Buck valley current limit(mV)}}{R_{sense}(m\Omega)}+\frac{VIN-Vo}{2\times L(\mu H)\times f(kHz)}\times\frac{Vo}{VIN}\times10^{3}\right)\quad(3)$$

$$I_{INmax}(A)=\frac{\text{Boost peak current limit(mV)}}{R_{sense}(m\Omega)}-\frac{VIN}{2\times L(\mu H)\times f(kHz)}\times\frac{Vo-VIN}{Vo}\times10^{3})\quad(4)$$

Where η is the efficiency, the buck valley current limit typical value is 133mV, the boost peak current limit typical value is 150mV, and R_{SENSE} is the cycle-by-cycle switching current limit sense resistor.

Average Current Limit

The IAVGP and IAVGN pins sense the output current in the MPQ4210. A sense resistor can be connected to the VOUT line for average output current limit control. Once the sensed signal is higher than the current limit reference voltage, one internal EA pulls down V_{SS}. Eventually, V_{SS} replaces V_{REF} to control COMP, and the inductor current is limited by COMP to transfer less energy to output. SS regulates output low until the average load current drops.

If the switching current is regulated by the average current limit, and it does not trigger cycle-by-cycle current limit, the MPQ4210 will not trigger hiccup or latch-off protection even if the average current limit is reached. This feature makes constant current charge possible in the MPQ4210. If only the average current limit is triggered, the interrupt OCP bit does not set to 1, and INT will not pull low.

It is recommended to add a 100Ω/220nF current sense filter (see Figure 13).

Overload and Short-Circuit Protection

When overload occurs, the MPQ4210 limits the output current by average current limit loop regulation. If average current limit loop is disabled, the cycle-by-cycle switching current limit works. In cycle-by-cycle current limit condition, if the IC works in boost mode and the SWC peak current is limited. If the IC works in buck mode, SWB remains on until I_L drops to the buck valley current limit level, and then the next cycle can kick in. Therefore, the inductor current can be controlled in all work modes.

Output Voltage Regulation

The MPQ4210 regulates V_{OUT} through FB pin feedback. V_{FB} is compared to the internal reference, which is between 300mV and 2.047V depending on the VREF register bit's setting. The EA output on COMP controls the inductor current to supply output voltage.

Switching Frequency and Frequency Spread Spectrum Function

The MPQ4210 programs switching frequency with a 2-bit FSW register. The frequency is selectable at 200kHz, 300kHz, 400kHz, and 600kHz. Typically, a 400kHz switching frequency is recommended.

The MPQ4210 has a frequency spread spectrum function. Set the Dither bit = 1 (0x02, D[4]) to enable this function. Set the Dither bit = 0 to disable the function. The purpose of the spread spectrum is to minimize the peak emissions at certain frequencies.

The MPQ4210 uses a 2kHz triangle wave to modulate the internal oscillator. The frequency span of the spread spectrum operation is ±6%.

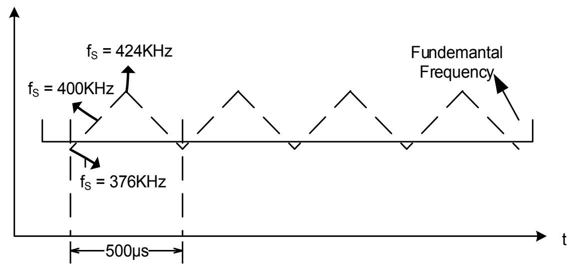


Figure 6: Frequency Spread Spectrum

The MPQ4210 frequency spread frequency can be enabled for a 200kHz, 300kHz, 400kHz, or 600kHz switching frequency.

Gate Driver and BST Power

The MPQ4210 provides four N-channel MOSFET gate drivers for the H-bridge MOSFETs (see Figure 2). Each driver is capable of sourcing and sinking current. In buck operation, LG1 and HG1 switch while HG2 remains on. In boost operation, LG2 and HG2 switch while HG1 remains on. LG1 and LG2 are powered by VCC power, while HG1 and HG2 are powered by BST1 and BST2 power.

Capacitors between BST1 to SW1 and BST2 to SW2 are necessary to supply the power, which can be from an internal diode from VCC or from charging each other.

Over-Voltage Protection

The MPQ4210 monitors FB. If V_{FB} exceeds 127% of V_{REF} and the OVP_MODE bits are 01, the IC discharges the V_{OUT} capacitor through one internal discharge resistor. It stops discharging when V_{FB} drops to 111% of the regulation voltage. If the OVP_MODE bits are 00, there is no logic to stop switching even if V_{FB} is higher than the OVP threshold. If the OVP_MODE bits are 10, the IC latches off when V_{OUT} rises to 127% of V_{REF}.

Interrupt (INT Pin)

The MPQ4210 has one interrupt pin for the following fault events: OCP, OVP, OTP, and PNG (V_{OUT} power not good) reporting.

When the switching peak cycle-by-cycle current limit (OCP), output over-voltage (FB OVP), or over-temperature protection (OTP) is triggered, the corresponding register bit sets to 1. At the same time, INT pulls low to indicate an interrupt signal, depending on the related Mask register setting.

INT is an open-drain output. When the MPQ4210 is disabled, INT is an open drain.

Slew-Rate Control and Output Discharge

The MPQ4210 sets the output voltage change slew-rate through internal SR bits. Four kinds of V_{REF} change (rising and falling) slew rate can be selected in different application requirement: 38mV/ms, 50mV/ms, 75mV/ms and 150mV/ms.

During voltage transient, the discharge function works when GO-BIT sets to 1. The discharge function is disabled automatically after GO_BIT resets to 0 (which means V_{REF} change completes). If V_{OUT} has not been discharged to the goal voltage when V_{REF} change completes due to too large of an output capacitor, the OVP discharge function or DISCHG bit can be used to continue discharging C_{OUT}.

The output discharge function is enabled in the following conditions:

1. GO_BIT set to 1. Discharge works until 20ms delay passes after GO_BIT resets to 0.
2. DISCHG bit set to 1.
3. OVP_MODE bits set to 01, and FB is 127% of V_{REF}.
4. ENPWR bit power off. Discharge works until 200ms delay passes.
5. EN pin off. Discharge works until 200ms delay passes.
6. If VIN_UVLO is triggered, but AVDD has residual voltage, the MPQ4210 discharges for 200ms. This discharge function may halt if the AVDD voltage drops.

Current Monitor Output

The MPQ4210 senses the average load current through one sense resistor, and outputs one voltage signal on the IMON pin. The signal is amplified from the IAVGP - IAVGN voltage difference. One small capacitor from IMON to AGND is recommended. The IMON output voltage can be calculated with Equation (5):

$$V_{IMON}(mV) = GAIN \times I_{OUT}(A) \times R_{sens}(m\Omega) \quad (5)$$

Typically, the IMON GAIN is 18. R_{sens} is the output current sense resistor.

Soft-Start Time Programmable (SS)

The MPQ4210 has a soft-start pin to program the soft-start time. The SS charge current is typically about 6μA. The soft-start time can be estimated with Equation (6):

$$T_{SS}(ms)=C_{SS}(nF)\times V_{REF}(V)\div Iss(\mu A) \qquad (6)$$

Typically, the I_{SS} charge current is about 6μA, C_{SS} = 47nF, and V_{REF} = 0.5V. The soft-start time is about 3.9ms.

Thermal Protection

The MPQ4210 integrates one temperature monitor circuit. If the junction temperature is higher than 150°C, the MPQ4210 shuts down. After the temperature drops below 125°C, the IC resumes operation. When OTP is triggered, INT is pulled low if it is not masked.

I²C Interface

The MPQ4210 integrates one I²C interface. The device address is defined as 1100xxxb, and the final one bit is R/W bit, which is 0 for a write command and 1 for a read command. It works as a slave and supports standard mode (100kbps) and fast mode (400kbps) communication. Table 1 shows I²C slave address selection.

Table 1: I²C Slave Address

Device Address	R_{TOP}	R_{BOT}
64H	68kΩ	100kΩ
66H	0	NC

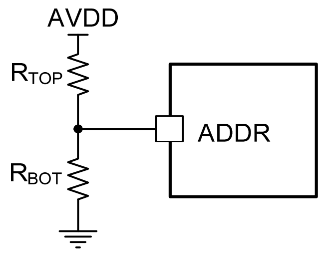


Figure 7: ADDR Set-Up

See the Register Description section on page 32 for details on I²C and register control functions.

I²C Transfer Data

Every byte put on the SDA line must be 8 bits long. Each byte must be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable (LOW) during the HIGH period of this clock pulse.

Figure 8 shows the format for data transfers. After the START condition (S), a slave address is sent. This address is 7 bits long, followed by an eighth data direction bit (R/W). A 0 indicates a transmission (WRITE), and a 1 indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address another slave without first generating a STOP condition.

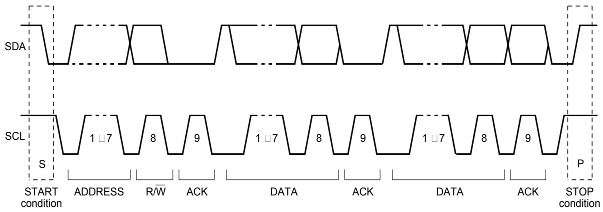
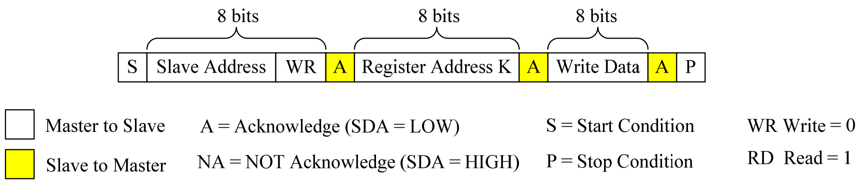


Figure 8: Complete Data Transfer

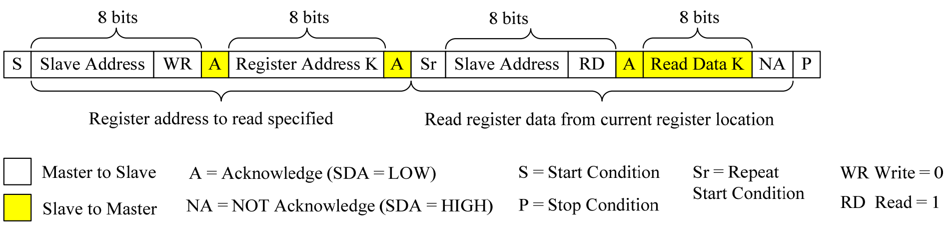
The MPQ4210 includes a full I²C slave controller. The I²C slave fully complies with the I²C specification requirements. It requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update.

After receiving each byte, the MPQ4210 acknowledges by pulling the SDA line low during the HIGH period of a single clock pulse. A valid I²C address selects the MPQ4210. The MPQ4210 then performs an update on the falling edge of the LSB byte.

Figure 9 shows an example of the I²C read and write command.



(a) I²C Write Example



(b) I²C Read Example

Figure 9: I²C Read and Write

APPLICATION INFORMATION

Output Voltage Setting

The default output voltage is set using a resistor divider to FB. The default reference voltage (V_{REF}) is 0.5V. The bottom resistor in the resistor divider is typically in the 1kΩ to 50kΩ range.

The top resistor in the feedback resistor divider is selected using Equation (7):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (7)$$

It is possible to use the I²C interface to select the FB V_{REF} and get another output voltage.

Inductor Selection

The inductor selection is based on the work mode. The inductance for the buck mode is calculated with Equation (8):

$$L_{Buck} = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

Where ΔI_L is the peak-to-peak inductor ripple current, and it is about 30% to 50% of the maximum load current.

In boost mode, the inductor selection is based on limiting ΔI_L to about 30% to 50% of the maximum input current. The target inductance for boost mode is calculated with Equation (9) and Equation (10):

$$L_{Boost} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times F_{SW} \times \Delta I_L} \quad (9)$$

$$I_{IN(max)} = \frac{V_{OUT} \times I_{LOAD(max)})}{V_{IN} \times \eta} \quad (10)$$

Where $I_{LOAD(max)}$ is the maximum load current, ΔI_L is the peak-to-peak ripple current (about 30% to 50% of the maximum input current), and η is the efficiency.

Choosing a larger inductance reduces the ripple current but also increases the size of the inductor and reduces the achievable bandwidth of the converter by moving the right half-plane zero to lower frequencies. The appropriate balance should be chosen based on the application requirements.

Input Capacitor Selection

In buck mode, the MPQ4210 has a discontinuous input current (boost mode is continuous), and requires a capacitor to supply the AC current during buck mode while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance, and should be placed as close to VIN as possible. Capacitors with X5R or X7R ceramic dielectrics are recommended because of their stable temperature characteristics. The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The buck mode input ripple current can be estimated with Equation (11):

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (11)$$

The worst-case condition in buck mode occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (12):

$$I_{CIN\_RMS} = \frac{I_{OUT}}{2} \quad (12)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the specification.

In buck mode, the input voltage ripple can be estimated with Equation (13):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

(13)

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (14):

$$\Delta V_{IN} = \frac{1}{4} \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (14)$$

Output Capacitor Selection

In boost mode, the output current is discontinuous, so C_{OUT} must be capable of reducing the output voltage ripple.

A higher capacitance value may be required to lower the output ripple and the transient response. Low-ESR capacitors, such as X5R or X7R ceramic capacitors, are recommended. If using ceramic capacitors, the capacitance dominates the impedance at the switching frequency, so the output voltage ripple is independent of the ESR. The output voltage ripple is estimated with Equation (15):

$$\Delta V_{OUT} = \frac{(1-\frac{V_{IN}}{V_{OUT}})\times I_{LOAD}}{C_{OUT}\times F_{SW}} \quad (15)$$

Where V_{RIPPLE} is the output ripple voltage, and C_{OUT} is the capacitance of the output capacitor.

If using hybrid, polymer, or low-ESR electrolytic capacitors, the ESR dominates the impedance at the switching frequency, so the output ripple is estimated using Equation (16):

$$\Delta V_{OUT} = \frac{(1-\frac{V_{IN}}{V_{OUT}})\times I_{LOAD}}{C_{OUT}\times F_{SW}} + \frac{I_{LOAD}\times R_{ESR}\times V_{OUT}}{V_{IN}} \quad (16)$$

Where R_{ESR} is the equivalent series resistance of the output capacitors.

For a 100W USB PD application, one 330μF electrolytic capacitor and four 10μF ceramic capacitors are recommended.

Choose output capacitors to satisfy the output ripple and load transient requirements of the design. Capacitance derating should be taken into consideration when designing high output voltage applications.

External MOSFET Selection

The MPQ4210 requires four external N-channel power MOSFETs. Figure 10 shows two for the top switches (switches A and D) and two for the bottom switches (switches B and C). In buck mode, SWA and SWB switch while SWD remains on. In boost mode, SWC and SWD switch while SWA remains on.

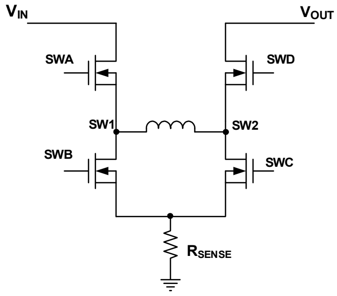


Figure 10: Buck-Boost Topology

The critical parameters of selecting a MOSFET are:

1. Maximum drain-to-source voltage, $V_{DS(MAX)}$

   The SWA and SWB need to withstand the maximum input voltage and the transient spikes at SW1 during switching. Therefore, it is recommended to select $V_{DS(MAX)}$ for SWA and SWB at 1.5 times the input voltage.

   The SWC and SWD see output voltage and transient spikes at SW2 during switching. Therefore, it is recommended to select SWC and SWD at ≥1.5 times the output voltage.

2. Maximum current, $I_{D(MAX)}$
3. V_{TH}: The driver voltages of the MPQ4210 are supplied by VCC. The gate plateau voltages of the MOSFETs should be smaller than the minimum VCC voltage of the converter, otherwise the MOSFETs may not fully enhance during start-up or overload conditions.
4. On resistance, $R_{DS(ON)}$
5. Total gate charge, Q_G

   For the MPQ4210, all switches Q_G should be smaller than 50nC (at 7.2V GATE condition). If there are two MOSFETs in parallel, each MOSFET Q_G need be smaller than 25nC.

MOSFET SWA

When the MPQ4210 works in boost mode, SWA is on consistently. Its conduction power loss can be calculated with Equation (17):

$$P_{C\_Loss(SWA)} = (I_o \times \frac{V_{OUT}}{V_{IN}})^2 \times R_{DSON(SWA)} \quad (17)$$

Assume that the MOSFET junction-to-ambient thermal resistance is 50°C/W (this is determined by the board power dissipation), and that the maximum acceptant temperature rise is 50°C, thus, the maximum power loss is 1W, shown with Equation (18):

$$P_{C\_Loss(SWA)} < 1W \quad (18)$$

Based on this equation, we can select the MOSFET R_{ON}.

When the MPQ4210 works in buck mode, the conduction and switching loss of SWA can be calculated with Equation (19) and Equation (20), respectively:

$$P_{C\_Loss(SWA)} = \frac{V_{OUT}}{V_{IN}} \times I_o^2 \times R_{DSON(SWA)} \quad (19)$$

$$P_{SW\_Loss(SWA)} = \frac{1}{2} V_{IN} \times I_{OUT} \times (t_{on} + t_{off}) \times F_{sw} \quad (20)$$

The switch on time (t_{on}) and the switch off time (t_{off}) are based on the MOSFET datasheet information (see Figure 11).

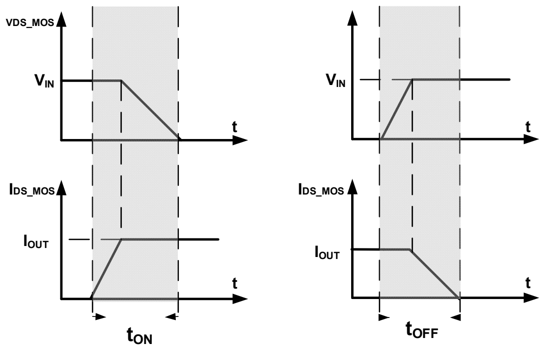


Figure 11: Switch On Time and Switch Off Time

MOSFET SWB

When MPQ4210 work in buck mode, its conduction loss can be calculated with Equation (21):

$$P_{C\_Loss(SWB)} = (1 - \frac{V_{OUT}}{V_{IN}}) \times I_o^2 \times R_{DSON(SWB)} \quad (21)$$

MOSFET SWC

When the MPQ4210 works in boost mode, SWB is always off. Its conduction loss in boost mode can be calculated with Equation (22):

$$P_{C\_Loss(SWC)} = (1 - \frac{V_{IN}}{V_{OUT}}) \times (I_o \times \frac{V_{OUT}}{V_{IN}})^2 \times R_{DSON(SWC)} \quad (22)$$

When the MPQ4210 works in boost mode, the SWC switching loss can be calculated with Equation (23):

$$P_{SW\_Loss(SWC)} = \frac{1}{2} \times V_{OUT} \times (I_{OUT} \times \frac{V_{OUT}}{V_{IN}}) \times (t_{on} + t_{off}) \times F_{sw} \quad (23)$$

MOSFET SWD

When the MPQ4210 works in buck mode, SWD is on consistently. Its power loss can be calculated with Equation (24):

$$P_{C\_Loss(SWD)} = I_o^2 \times R_{DSON(SWD)} \quad (24)$$

When the MPQ4210 works in boost mode, the SWD conduction loss can be calculated with Equation (25):

$$P_{C\_Loss(SWD)} = (\frac{V_{IN}}{V_{OUT}}) \times (I_o \times \frac{V_{OUT}}{V_{IN}})^2 \times R_{DSON(SWD)} \quad (25)$$

Dead time and the low-side MOSFET switching loss can be ignored.

Compensation Components

The COMP pin controls system stability and transient response. COMP is the output of the internal error amplifier. A series capacitor-resistor combination sets a pole-zero combination to control the control system's characteristics.

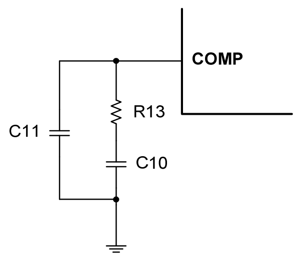


Figure 12: COMP External Compensation

The COMP external compensation sets one pole F_{P1} and one zero F_{Z1} (see Figure 12). These are determined by Equation (26) and Equation (27):

$$F_{P1} = \frac{1}{2\pi \times C11 \times R13} \quad (26)$$

$$F_{Z1} = \frac{1}{2\pi \times C10 \times R13} \quad (27)$$

When the MPQ4210 works in buck mode, the DC gain of the voltage feedback loop is calculated with Equation (28):

$$A_{VDC} = R_{LOAD} \times \frac{G_{CS}}{R_{SENSE}} \times A_{V-EA} \times \frac{V_{FB}}{V_{OUT}} \quad (28)$$

Where A_{V-EA} is the error-amplifier voltage gain (300V/V), G_{CS} is the COMP to current sense gain, R_{SENSE} is the current sense resistor, and R_{LOAD} is the load resistor value.

The system has two important poles: one is from the compensation capacitor (C10) and the output resistor of the error amplifier, and the other one is from the output capacitor and the load resistor. These poles can be calculated with Equation (29) and Equation (30), respectively:

$$F_{P2} = \frac{G_{EA}}{2\pi \times C10 \times A_{V-EA}} \quad (29)$$

$$F_{P3} = \frac{1}{2\pi \times C_{OUT} \times R_{LOAD}} \quad (30)$$

Where G_{EA} is the error-amplifier transconductance (1220μA/V), and C_{OUT} is the output capacitor.

The system may have another significant zero if the output capacitor has a large capacitance or a high ESR value. This zero can be located with Equation (31):

$$F_{ESR} = \frac{1}{2\pi \times C_{OUT} \times R_{ESR}} \quad (31)$$

When the MPQ4210 works in boost mode, the DC gain of the voltage feedback loop is calculated with Equation (32):

$$A_{VDC} = \frac{V_{IN} \times A_{V-EA} \times R_{LOAD} \times V_{FB} \times G_{CS} \times R13}{2 \times V_{OUT}^2 \times R_{SENSE}} \quad (32)$$

There is also a right-half-plane zero (F_{RHPZ}) that exists in boost mode. The frequency of the right half-plane zero is determined with Equation (33):

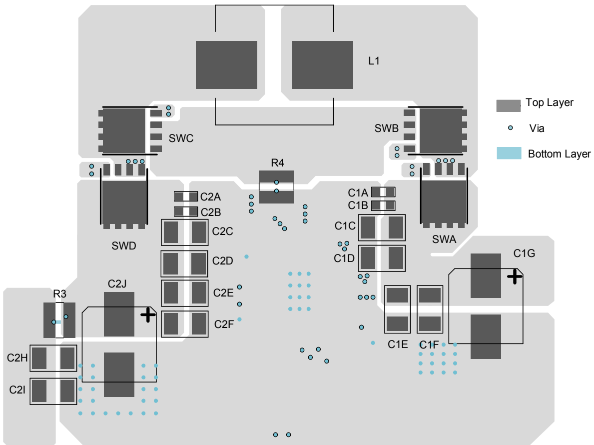
$$F_{RHPZ} = \frac{R_{LOAD}}{2 \times \pi \times L} \times \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \quad (33)$$

The right half-plane zero increases the gain and reduces the phase simultaneously, which results in a smaller phase and gain margin. The worst-case condition occurs when the input voltage is at its minimum and the output power is at its maximum.

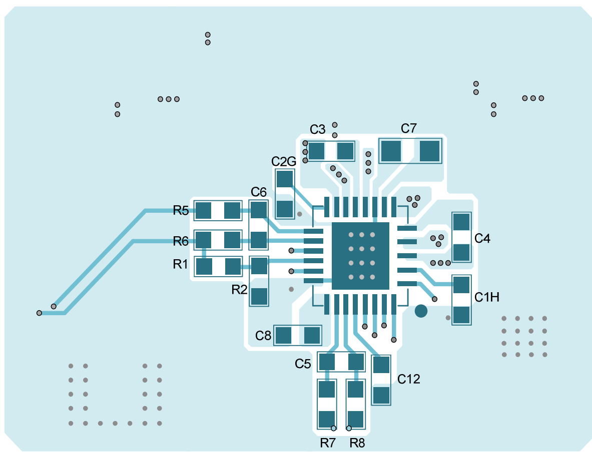
PCB Layout Guidelines

Efficient layout is a critical step in designing a buck-boost controller. Improper layout may result in reduced performance, EMI problems, resistive loss, and even system instability. For best results, refer to Figure 13 and follow the steps below:

1. In buck mode, place the input power loop — including the input filter capacitor (C_{IN}), the power MOSFETs (SWA and SWB), and the cycle-by-cycle current sense resistor (R4) — as close as possible.
2. In boost mode, place the output power loop — including the output filter capacitor (C_{OUT}), the power MOSFETs (SWC and SWD), and the cycle-by-cycle current sense resistor (R4) — as close as possible.
3. Use wide copper traces and power loop vias to help thermal dissipation.
4. Connect the exposed pad to GND, and place vias on the exposed pad for IC thermal dissipation.
5. Place small decoupling capacitors close to VIN, VOUT, and AGND.
6. Lay out the gate drive traces and return paths as directly as possible. Lay out the forward and return traces close together, either running side by side or on top of each other on adjacent layers, to minimize the inductance of the gate drive path.
7. Use Kelvin connections to R3 (for the average current sense) and R4 (for the cycle-by-cycle current), and run lines in parallel from the R3/R4 terminals to the IC pins. Avoid crossing noisy areas such as SW1 and SW2 or gate drive traces.
8. Place the filter capacitor for the current sense signal as close to the IC pins as possible.
9. Place the VCC and AVDD capacitors as close as possible to the VCC and AVDD pins.
10. Place the BST1 bootstrap capacitor close to the IC, and connect directly to the BST1 and SW1 pins.
11. Place the BST2 bootstrap capacitor close to the IC, and connect directly to the BST2 and SW2 pins.
12. The feedback loop should be far away from any noise source. Place the FB dividers (R1 and R2) as close as possible to the FB and AGND pins.
13. Separate the power and signal paths so that no power or switching current flows through the AGND connections. Connect the PGND and AGND traces near the PGND pin, near the VCC capacitor PGND connection, or near the PGND connection of the cycle by cycle current sense resistor (R4).



Top Layer



Bottom Layer

Figure 13: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

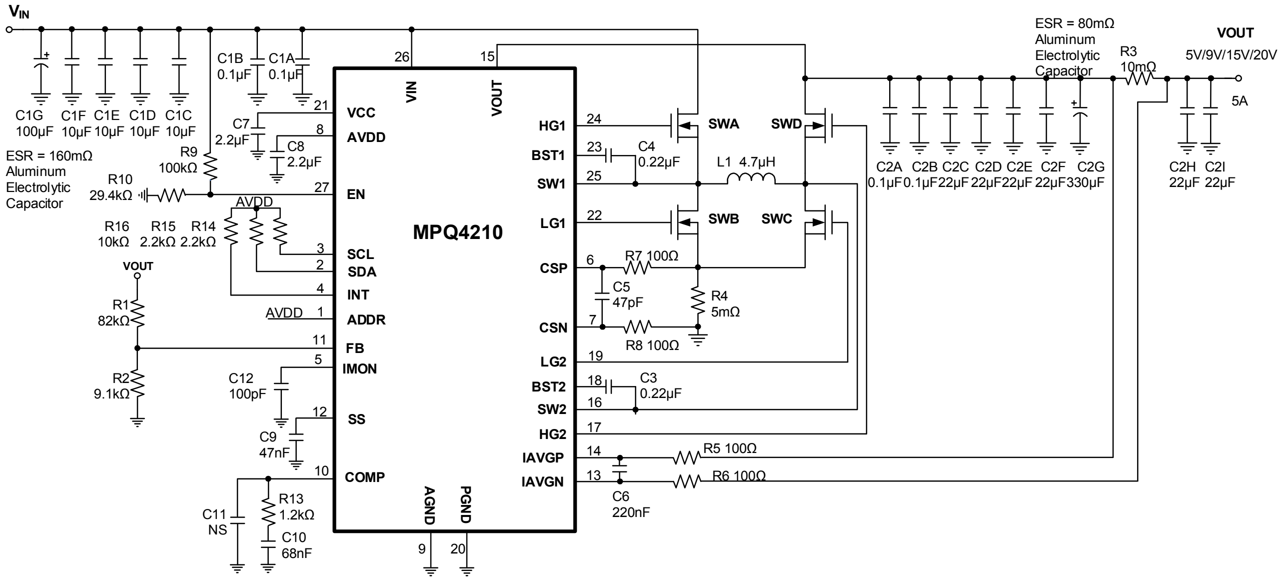


Figure 14: V_{IN} = 12V, V_{OUT} = 5V/9V/15V/20V for 100W USB PD

REGISER DESCRIPTION

Register Map

Address	Register	Type	D7	D6	D5	D4	D3	D2	D1	D0	Reset State
0x00	REF_LSB	R/W	-	-	-	-	-	VREF_L			0000 0100
0x01	REF_MSB	R/W	VREF_H								0011 1110
0x02	Control 1	R/W	SR		DISCHG	Dither	PNG_Latch	Reserved (9)	GO_BIT	ENPWR	0100 0000
0x03	Control 2	R/W	FSW		-	BB_FSW	OCP_MODE		OVP_MODE		1000 0101
0x04	ILIM	R/W	-	-	-	-	Reserved	ILIM			0000 1001
0x05	Interrupt status	R/W	-	-	-	OTP	-	OVP	OCP	PNG	0000 0000
0x06	Interrupt mask	R/W	-	-	-	M_OTP	-	M_OVP	M_OCP	M_PNG	0000 0001

Note:

9) This bit must be written to 1 before start-up.

Register Name: REF_LSB, 0x00, Read/Write

Name	Bits	Default Value	Description
VREF_L	D[2:0]	100	Feedback V_{REF} low 3 bits. LSB = 1mV.

Register Name: REF_MSB, 0x01, Read/Write

Name	Bits	Default Value	Description
VREF_H	D[7:0]	0011 1110	Feedback V_{REF} high 8 bits. LSB = 8mV.

See below for FB reference data format.

Name	VREF															
Format	Direct, unsigned binary integer															
Register Name	N/A					VREF_H D[7:0]								VREF_L D[2:0]		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	N/A					r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	N/A					Data bit high								Data bit low		
Default Value (0.5V)	N/A					500 integer										

Total 11 bits to set reference voltage. If V is an 11-bit, unsigned binary integer of VREF [10:0], then: V_{FB} (V) = V/1000.

Register Name: Control 1, 0x02, *Read/Write*

<table>
<tr><th>Name</th><th>Bits</th><th>Default Value</th><th colspan="2">Description</th></tr>
<tr><td rowspan="6">SR</td><td rowspan="6">D[7:6]</td><td rowspan="6">01</td><td colspan="2">Program the V_{REF} changing slew rate. This SR control only works after SS finishes. During the SS period, the V_{OUT} slew rate is controlled by SS.

V_{OUT} slew rate = V_{REF} slew rate × feedback ratio of (R1 + R2) / R2.</td></tr>
<tr><td>SR Bits Value</td><td>V_{REF} Slew Rate</td></tr>
<tr><td>00</td><td>38mV/ms</td></tr>
<tr><td>01</td><td>50mV/ms</td></tr>
<tr><td>10</td><td>75mV/ms</td></tr>
<tr><td>11</td><td>150mV/ms</td></tr>
<tr><td>DISCHG</td><td>D[5]</td><td>0</td><td colspan="2">Turn on or turn off the output-to-ground discharge path. Write DISCHG bit 1 to always turn on the internal discharge resistor. Write DISCHG bit 0 to turn off output discharge resistor. DISCHG bit function works even ENPWR bit is low.

This bit does not affect the output discharge behavior in the following cases:
1) V_{OUT} voltage changed by I^2C
2) ENPWR power off
3) EN pin power off
4) Output OVP (When OVP_MODE enables discharge)
5) VIN UVLO

When GO_BIT is set to 1, V_{OUT} discharges will automatically turn on. After GO_BIT resets to 0 with 20ms extra delay, the V_{OUT} discharge path turns off.

Normally, it is suggested to set the slew rate low so V_{OUT} can follow the V_{REF} change with this internal discharge current. If V_{OUT} cannot follow the V_{REF} change even with the discharge due to a large C_{OUT} capacitor, there is an additional 20ms discharge.</td></tr>
<tr><td>Dither</td><td>D[4]</td><td>0</td><td colspan="2">Frequency spread sprectrum enable bit.

Dither is enabled when this bit is 1, and disabled when this bit is 0.</td></tr>
<tr><td>PNG_Latch</td><td>D[3]</td><td>0</td><td colspan="2">PNG status bit reset control bit. Refer to PNG bit description on page 36.

0 = PNG bit status recovers to 0 once V_{OUT} returns to its normal voltage range

1 = PNG bit status latches to 1 once V_{OUT} exceeds the power good voltage range</td></tr>
<tr><td>Reserved</td><td>D[2]</td><td>0</td><td colspan="2">This bit must be set to 1 before the IC starts up.</td></tr>
</table>

GO_BIT	D[1]	0	V_{REF} change function enable bit. Set GO_BIT to 1 to enable the output change based on the VREF register. When the command completes (internal reference voltage steps to the goal of V_{REF}), GO_BIT auto-resets to 0. This prevents false operation of the VOUT scaling. Write the VREF registers (00h and 01h register) first, then write GO_BIT = 1. The reference and output voltage will change based on the new V_{REF}. GO_BIT resets to 0 when V_{REF} reaches a new level. The host reads GO_BIT to determine whether the V_{REF} scaling is finished or not. The V_{OUT} discharge path enables when GO_BIT is 1, no matter what the DISCHG bit is. This can help pull V_{OUT} from high to low in light-load condition. After GO_BIT resets to 0, the discharge continues and turn off after a 20ms delay. 0 = V_{OUT} cannot be changed 1 = V_{OUT} changes based on VREF registers. After V_{REF} reaches the new level set by the VREF bits, GO_BIT resets to 0 automatically
ENPWR	D[0]	0	The MPQ4210 power switching enable bit. 1 = Enables power switching 0 = Disables power switching, but other internal control circuits work ENPWR start-up sequence: Step 1: Set V_{REF} first, ENPWR = 0 Step 2: Set GO_BIT = 1 Step 3: Wait 200ms, then set ENPWR = 1 to start After ENPWER is set to 0 and a 200ms delay, the discharge function works.

Register Name: Control 2, 0x03, *Read/Write*

<table>
<tr><th>Name</th><th>Bits</th><th>Default Value</th><th colspan="5">Description</th></tr>
<tr><td rowspan="3">FSW</td><td rowspan="3">D[7:6]</td><td rowspan="3">10</td><td colspan="5">Switching frequency setting bit.
Writable during both ENPWR = 0 and ENPWR = 1 conditions. The switching frequency changes smoothly after I²C writes these bits.</td></tr>
<tr><td>FSW bits</td><td>00</td><td>01</td><td>10</td><td>11</td></tr>
<tr><td>Frequency</td><td>200kHz</td><td>300kHz</td><td>400kHz</td><td>600kHz</td></tr>
<tr><td>BB_FSW</td><td>D[4]</td><td>0</td><td colspan="5">Buck-boost region switching frequency set bit. See Figure 4.
1 = higher switching frequency in buck-boost region. The higher Buck-Boost switching frequency is 62.5% of the base switching frequency.
0 = lower switching frequency in buck-boost region. The lowers Buck-Boost switching frequency is 37.5% of the base switching frequency.</td></tr>
</table>

OCP_MODE	D[3:2]	01	Set OCP protection mode after triggering the cycle-by-cycle switching current limit (valley current limit in buck, or peak current limit in boost). 00 = No hiccup or latch-off protection. Inductor current is limited by cycle-by-cycle current limit 01 = Hiccup protection after triggering the switching current limit and FB < 60% of V_{REF}. Off-period is controlled by SS discharge 10 = Latch-off protection. Must re-power or re-enable for the IC to restart 11 = Reserved
OVP_MODE	D[1:0]	01	Set OVP protection mode after triggering the threshold at 127% of V_{REF}. 00 = No protection after OVP, V_{OUT} is regulated by COMP. No discharge after OVP 01 = Discharge V_{OUT} through an internal resistor and stop switching when V_{FB} exceeds 127% of V_{REF}. Recover when V_{FB} drops to 111% of V_{REF} 10 = Latch-off protection. No discharge after OVP 11 = Reserved

Register Name: ILIM, 0x04, *Read/Write*

<table>
<tr><th>Name</th><th>Bits</th><th>Default Value</th><th colspan="3">Description</th></tr>
<tr><td rowspan="10">ILIM</td><td rowspan="10">D[2:0]</td><td rowspan="10">001</td><td colspan="3">Average current limit. Can be used to program output current limit.</td></tr>
<tr><th>ILIM Bits</th><th>Current Limit Threshold</th><th>Current Limit with 10mΩ R_{SENSE}</th></tr>
<tr><td>000</td><td>27.9mV</td><td>2.79A</td></tr>
<tr><td>001</td><td>33.3mV</td><td>3.33A</td></tr>
<tr><td>010</td><td>39.3mV</td><td>3.93A</td></tr>
<tr><td>011</td><td>45.1mV</td><td>4.51A</td></tr>
<tr><td>100</td><td>51.2mV</td><td>5.12A</td></tr>
<tr><td>101</td><td>56.8mV</td><td>5.68A</td></tr>
<tr><td>110</td><td>62.8mV</td><td>6.28A</td></tr>
<tr><td>111</td><td>68.7mV</td><td>6.87A</td></tr>
</table>

Register Name: Interrupt Status, 0x05, *Read/Write*

<table>
<tr><th>Name</th><th>Bits</th><th>Default Value</th><th>Description</th><th>Reset Condition</th></tr>
<tr><td>OTP</td><td>D[4]</td><td>0</td><td>Over-temperature protection indication.
0: Normal state
1: Chip is in over-temperature protection state</td><td rowspan="3">This bit is latched once triggered.
Write 0xFF to this register to reset the interrupt status and INT's state.</td></tr>
<tr><td>OVP</td><td>D[2]</td><td>0</td><td>V_{OUT} OVP indicator.
0: Normal state
1: Chip is in over-temperature protection state</td></tr>
<tr><td>OCP</td><td>D[1]</td><td>0</td><td>Cycle-by-cycle switching current limit indication.
0: Normal state
1: Cycle-by-cycle current limit is triggered, V_{FB} < 60% of V_{REF}, and soft-start is finished</td></tr>
<tr><td>PNG</td><td>D[0]</td><td>0</td><td>V_{OUT} power not good indicator.
0: Normal state
1: Output power is not good. It indicates when V_{OUT} is out of both its upper and lower thresholds
The PNG_Latch bit controls the PNG reset behavior.</td><td>Related to PNG_Latch setting:
PNG_Latch = 0: This bit indicates instantaneous value. INT indicates instantaneous state
PNG_Latch = 1: This bit is latched once triggered. Write 0xFF to reset the interrupt status and INT's state</td></tr>
</table>

Register Name: Interrupt Mask, 0x06, *Read/Write*

Name	Bits	Default Value	Description
M_OTP	D[4]	0	Set M_OTP = 1 to mask off the OTP alert. M_OTP = 1 only masks INT's output. It is similar for other mask bits.
M_OVP	D[2]	0	OVP mask bit. Set 1 to mask off the OVP alert. M_OVP = 1 only masks INT's output.
M_OCP	D[1]	0	OCP mask bit. Set 1 to mask off the OCP alert. M_OCP = 1 only masks INT's output.
M_PNG	D[0]	1	PNG mask bit. Set 1 to mask off the PNG alert. M_PNG = 1 only masks INT's output.