MPQ4228-Q

3A, 36V, Step-Down Converter with 1-Channel USB Charging Port Supporting QC3.0 and Type-C 5V @ 3A DFP, AEC-Q100 Qualified

DESCRIPTION

The MPQ4228-Q integrates a monolithic, step-down, switch-mode converter with a single USB current-limit switch and Type-C 5V @ 3A mode configuration channel for USB port applications. It achieves 3A of output current across a wide input supply range, with excellent load and line regulation.

The output of the USB switch is current-limited. The USB port supports Quick Charge 3.0 (QC3.0) mode. It is backwards compatible with DCP schemes for battery charging specification (BC1.2), Apple 3A divider mode, and 1.2V/1.2V mode, without requiring outside user interaction. The USB port also supports USB Type-C 5V @ 3A DFP mode.

Fault protections include hiccup current limiting, output over-voltage protection (OVP), DP/DM/CC1/CC2 short to battery, and thermal shutdown (TSD).

The negative temperature coefficient (NTC) input monitors the external PCB or other components' temperature(s).

The MPQ4228-Q requires a minimal number of readily available, standard external components, and is available in a QFN-22 (4mmx4mm) package.

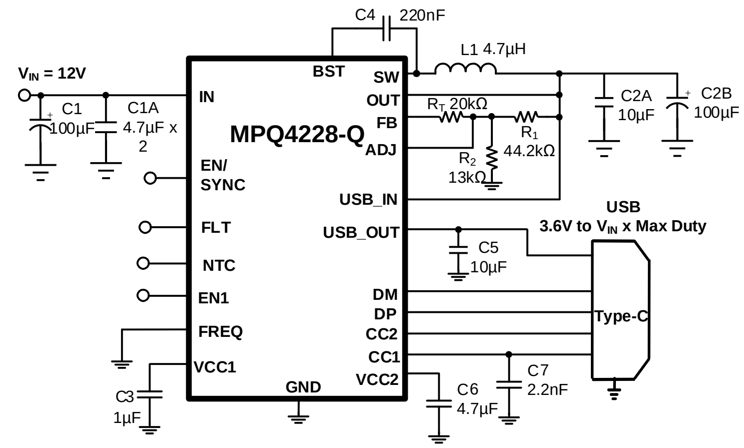
FEATURES

- DP/DM Support Quick Charge 3.0 Mode Class A
- Backwards Compatible with DCP Schemes: BC1.2 Short Mode, Apple 3A Divider Mode, 1.2V/1.2V Mode
- Supports USB Type-C 5V @ 3A DFP Mode
- NTC Over-Temperature Detection
- Passed Apple MFI Certification Test
- USB-IF Type-C Certified
- Independent USB On/Off Control Pin: EN1
- 145°C Internal Load-Shedding Entry Temperature
- USB_OUT, DP/DM, CC1/CC2 Pins Short-to-Battery Protection
- Wide 4.2V to 36V Continuous Operating Input Range
- Selectable Switching Frequency (420kHz or 2.2MHz with Spread Spectrum)
- 3A Output Continuous Current
- Integrated 20mΩ Low $R_{DS(ON)}$ MOSFET
- Line Drop Compensation
- Accurate 3.55A USB Current Limit
- EN Shutdown Discharge Function
- OCP, OVP, and OTP Fault Indication
- Frequency Sync from 200kHz to 2.2MHz
- Hiccup Current Limit for Buck and USB
- ±8kV IEC 61000-4-2 Contact Discharge ESD Rating for CC1 and CC2 Pins
- ±8kV IEC 61000-4-2 Contact Discharge ESD Rating with Small Resistor, Capacitor on DP and DM Pins
- ±15kV IEC 61000-4-2 Air Discharge ESD Rating for DP, DM, CC1 and CC2 Pins
- Available in a QFN-22 (4mmx4mm) Package with Wettable Flanks
- Available in AEC-Q100 Grade 1

APPLICATIONS

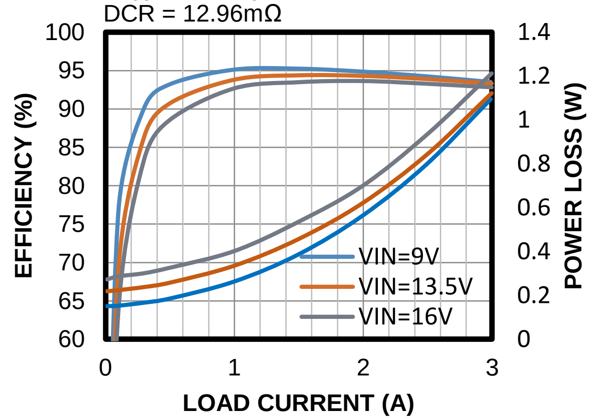
- Automotive USB QC3.0 Charging Ports
- Automotive USB Type-C Charging Ports

TYPICAL APPLICATION



Efficiency vs. Load Current vs. Power Loss

V_{BUS} = 5.1V, f_{SW} = 420kHz, L = 4.7µH, DCR = 12.96mΩ



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ4228GRE-Q-AEC1	QFN-22(4mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ4228GRE-Q-AEC1-Z).

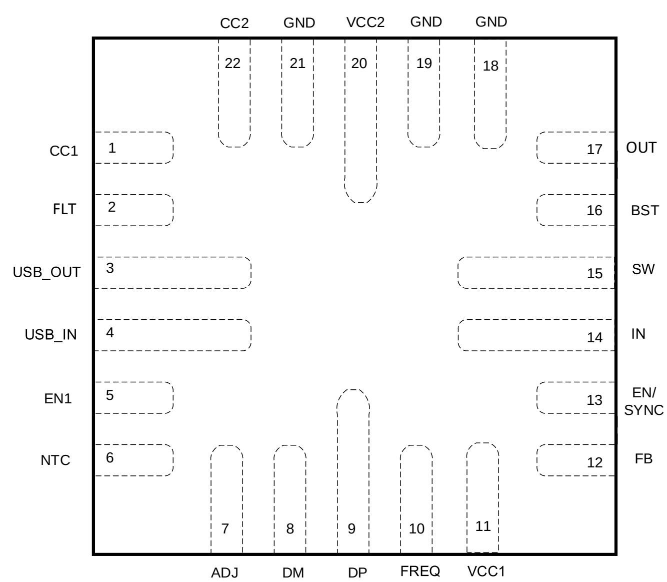
TOP MARKING

MPSYWW
MP4228
LLLLLL
QE

MPS: MPS prefix
Y: Year code
WW: Week code
MP4228: Part number
LLLLLL: Lot number
QE: Product suffix and package code

PACKAGE REFERENCE

TOP VIEW



QFN-22 (4mmx4mm) Wettable Flank

PIN FUNCTIONS

Pin #	Name	Description
1	CC1	**Configuration channel.** CC1 detects connections and configures the interface across the USB Type-C cables and connectors. Once a connection is established, CC1 or CC2 is reassigned to provide power over the VCONN pin of the plug.
2	FLT	**Fault indicator.** This pin indicates USB OCP/SCP, USB_IN OVP, DP/DM/CCx short to battery, and thermal shutdown. FLT is an open drain under normal conditions. FLT is pulled low during any of aforementioned fault conditions.
3	USB_OUT	**USB bus voltage output.**
4	USB_IN	**USB bus voltage input.**
5	EN1	**USB switch enable pin.** EN1 is active low pin. EN1 = 0, the USB is enabled, EN1 = 3.3V, USB is off. The buck output is still active when EN1 = 3.3V. By default, EN1 is pulled low by an internal 1MΩ resistor. EN1's maximum voltage is 4V.
6	NTC	**Thermistor input.** Connect a thermistor from NTC to VCC2, and a fixed resistor from NTC to GND. Put the thermistor near the USB connector or output capacitor for temperature monitoring. The MPQ4228-Q has a 1.5A load capability when NTC reaches the load-shedding threshold. If NTC reaches the thermal shutdown threshold, then the chip immediately turns off the USB output and the FLT pin is pulled low. By default, NTC is pulled low by an internal 1MΩ resistor. Connect NTC to GND or float NTC to disable the thermal sense function. NTC's maximum voltage is 4V.
7	ADJ	**Output voltage adjust.** This pin sinks a current from the DC/DC converter's FB pin to ground to regulate the step-down converter's output voltage (V_{OUT}).
8	DM	**D- data line to USB connector.** This pin's input and output are used for handshaking with portable devices.
9	DP	**D+ data line to USB connector.** This pin's input and output are used for handshaking with portable devices.
10	FREQ	**Frequency selection pin.** If FREQ = GND, then the frequency is 420kHz with frequency dithering (±10% dithering) and forced continuous conduction mode (FCCM). If FREQ = floating, then the frequency is 420kHz with frequency dithering (±10% dithering) and pulse-frequency modulation (PFM) mode. If FREQ = VCC, then the frequency is 2.2MHz with frequency dithering (±10% dithering) and FCCM.
11	VCC1	**Internal 5V LDO regulator output.** Decouple with a 1µF capacitor.
12	FB	**Feedback.** Connect to the tap of an external resistor divider from the output to GND, to set V_{OUT}. The frequency foldback comparator lowers the oscillator frequency when the FB voltage (V_{FB}) is below 400mV to prevent current limit runaway during a short circuit fault condition.
13	EN/SYNC	**On/off control input.** This pin is internally pulled to ground by a 500kΩ resistor. Apply an external CLK on this pin to sync the switching frequency (f_{SW}) to the external clock.
14	IN	**Supply voltage.** The MPQ4228-Q operates from a 4.2V to 36V input rail. Use C1 to decouple the input rail. Connect this pin to the input capacitor using a wide PCB trace.
15	SW	**Switch output.** Use a wide PCB trace to make the connection.
16	BST	**Bootstrap.** A 220nF capacitor is connected between SW and BST to form a floating supply across the high-side MOSFET (HS-FET) driver.
17	OUT	**Buck output.** Connect OUT to an external power supply ($5V \le V_{OUT} \le 20V$) or connect OUT to V_{OUT} to reduce power dissipation and increase efficiency. When connected to V_{OUT}, place a 10Ω RC filter and a 220nF RC filter from OUT to GND to absorb the voltage spike. Float OUT or connect to ground if not used.
18, 19, 21	GND	**Power ground.**
20	VCC2	**Internal 3.45V LDO regulator output.** Decouple with a 4.7µF capacitor.

PIN FUNCTIONS *(continued)*

Pin #	Name	Description
22	CC2	**Configuration channel.** CC2 detects connections and configures the interface across the USB Type-C cables and connectors. Once a connection is established, CC1 or CC2 is reassigned to provide power over the VCONN pin of the plug.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .... -0.4V to +40V
V_{SW} ....
-0.3V (-5V for <10ns) to V_{IN} + 0.3V (43V for <10ns)
V_{BST} ....V_{SW} + 5.5V
V_{USB_IN, USB_OUT} .... -0.3V to +24V
V_{CC1}, V_{CC2}, V_{DM}, V_{DP} .... -0.3V to +18V
V_{FLT} .... -0.3V to +6.5V
V_{NTC}, V_{EN1} .... -0.3V to +4V
V_{FREQ}, $V_{EN/SYNC}$ .... -0.3V to +5.5V (2)
All other pins.............................. -0.3V to +4.5V
Continuous power dissipation (T_A = 25°C) (3) (6)
QFN-22 (4mmx4mm)..............................3.47W
Junction temperature .... 150°C
Lead temperature .... 260°C
Storage temperature................-65°C to +150°C

ESD Ratings

DP/DM/CC1/CC2/USB_OUT (HBM)……….±8kV
All other pins (HBM)................................... ±2kV
DP/DM/CC1/CC2/USB_OUT (CDM)……...±2kV
All other pins (CDM) .... ±750V

Recommended Operating Conditions (5)

Operation input voltage range......... 4.2V to 36V
Output voltage range..... 3.6V - 12V or V_{IN} x D_{MAX}
Output current...3A
Operating junction temp (T_J).....-40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-22 (4mmx4mm)
EVQ4228-Q-RE-00A (6) .... 36 .... 5.... °C/W
JESD51-7 (7) .... 42 .... 9.... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) About the details of EN pin's ABS Max rating, see the EN/SYNC Control section on page 19.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101, AEC specification AEC-Q100-011. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. HBM with regard to GND.
5) The device is not guaranteed to function outside of its operating conditions.
6) Measured on 4-layer, 57.4mmx57.4mm PCB.
7) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JESD board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +150°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown supply current	I_{IN}	V_{EN} = 0V, T_J = 25°C			1	μA
		V_{EN} = 0V, T_J = -40°C to +150°C			8	
Buck quiescent supply current	$I_{Q\_CL\_VBUSDIS}$	CC pin floating, V_{FB} = 1V		0.75	1.1	mA
Overall quiescent supply current	I_Q	CC1 to ground with 5.1kΩ, V_{FB} = 1V		1	1.5	mA
EN rising threshold	V_{EN_RISING}		1.15	1.4	1.65	V
EN falling threshold	$V_{EN\_FALLING}$		1.05	1.25	1.45	V
EN input current	I_{EN1}	V_{EN} = 2V		4.5	6	μA
	I_{EN2}	V_{EN} = 0		0	0.2	
Thermal shutdown (8)	T_{STD}			165		°C
Thermal hysteresis (8)	T_{STD_HYS}			20		°C
VCC1 regulator voltage	V_{CC1}	I_{CC} = 0mA	4.8	5	5.2	V
VCC1 load regulation	V_{CC1_LOG}	I_{CC} = 5mA		1.5	4	%
VCC2 regulator voltage	V_{CC2}	I_{CC} = 0mA	3.15	3.45	3.75	V
Step-Down Converter						
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_RISING}$		3.5	3.7	3.9	V
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_FALLING}$		3.05	3.25	3.45	V
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$			50	90	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$			30	60	mΩ
Output discharge resistance	R_{DIS}			200		Ω
Feedback voltage	V_{FB}		776	792	808	mV
Feedback current	I_{FB}	V_{FB} = 820mV		10	100	nA
Sync frequency range	f_{SYNC}		0.2		2.4	MHz
Oscillator frequency	f_{SW1}	V_{FB} = 750mV, FREQ = floating	340	420	500	kHz
	f_{SW2} (8)	V_{FB} = 750mV, FREQ = VCC		2.2		MHz
Frequency spread spectrum Span	f_{SW3}	FREQ = GND, based on 420kHz		±10		%
	f_{SW4} (8)	FREQ = VCC, based on 2.2MHz		±10		%
Maximum duty cycle	D_{MAX}	Based on 420kHz	94.5	96		%
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 36V, T_J = 25°C			1	μA
		V_{EN} = 0V, V_{SW} = 36V, T_J = -40°C to +150°C			10	
High-side peak current limit	I_{LIMIT1}	T_J = -40°C to +150°C	7	10		A

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +150°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Low-side valley current limit (8)	I_{LIMIT2}			9		A
Low-side negative current limit (8)	I_{LSNEG}			-3		A
Minimum on time (8)	t_{ON_MIN}			60		ns
Output over-voltage protection (OVP)	V_{OVP1}		112	115	118	%
Output OVP recovery	V_{OVP1_R}			105		%
Soft-start time	t_{SS}	Output from 10% to 90%		1.5		ms
USB Switch						
UVLO rising threshold	V_{USB_UVR}		2.8	3.0	3.2	V
UVLO hysteresis threshold	V_{USB_UVHYS}			400		mV
EN1 logic high input	V_{EN1_H}	Turn off the USB output	2			V
EN1 logic low input	V_{EN1_L}	Turn on the USB output			0.4	V
Switch on resistance	$R_{DS(ON)\_SW}$			20	40	mΩ
Input discharge resistance	R_{DIS_USB}	Turn on during IN OVP		200		Ω
USB output voltage	V_{USB_OUT1}	Default	-2%	5.1	+2%	V
	V_{USB_OUT2}	QC 3.0, T_J = 25°C	-1.5%	9	+1.5%	V
	V_{USB_OUT3}	QC 3.0, T_J = 25°C, V_{IN} = 13.5V	-1.5%	12	+1.5%	V
USB input OVP rising threshold	V_{USB_OV}	V_{OUT} = 5V	5.62	5.82	6.02	V
V_{IN} input OVP recovery threshold	$V_{OV\_RECOVERY}$	V_{OUT} = 5V	5.32	5.52	5.72	V
Current limit	I_{LIMIT1}	V_{OUT} drops to 10%, Type-A/C mode, room temperature	3.20	3.55	3.9	A
USB_OUT soft-start time	t_{USB_SS}	V_{OUT} = 5V, from 10% to 90%		0.45		ms
V_{BUS} enter hiccup hold time	t_{HICP_ON}	V_{OUT} = 5V, OC, hiccup on time		2		ms
Hiccup mode off time	t_{HICP_OFF}	V_{OUT} = 5V, V_{BUS} connected to GND		2		sec
DM, DP pins OVP rising threshold	$V_{OV\_DM\_DP}$		3.75	4.0	4.25	V
DM, DP pins OVP hysteresis	$V_{OV\_DM\_DP\_HYS}$			100		mV

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +150°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Line drop compensation gain	G_{ADJ_SINK}	V_{OUT} = 5V, I_{OUT} = 3A		170	250	mV
FLT output low voltage	V_{FLT_L}	I_{SINK} = 1mA			0.15	V
FLT leakage current	V_{FLT_LKG}	6.5V pull-up voltage			1	µA
FLT deglitch time	t_{FLT_DEG}	Over-current		2		ms
NTC Temperature Sensing						
Load-shedding entry threshold	V_{LS_HIGH}	R_{DOWN} = 3kΩ, R_{UP} = 3kΩ (125°C)	0.47	0.5	0.53	V_{CC2}
Load-shedding exit threshold	V_{LS_LOW}	R_{DOWN} = 3kΩ, R_{UP} = 9.99kΩ (85°C)	0.21	0.24	0.27	V_{CC2}
Thermal shutdown entry threshold	V_{TSD_HIGH}	R_{DOWN} = 3kΩ, R_{UP} = 1.28kΩ (160°C)	0.63	0.7	0.73	V_{CC2}
Thermal shutdown exit threshold	V_{TSD_LOW}	R_{DOWN} = 3kΩ, R_{UP} = 2.07kΩ (140°C)	0.57	0.6	0.63	V_{CC2}
BC1.2 DCP Mode						
DP and DM short resistance	R_{DP/DM_SHORT}	V_{DP} = 0.8V, I_{DM} = 1mA, T_J = 25°C			40	Ω
		V_{DP} = 0.8V, I_{DM} = 1mA, T_J = -40°C to +150°C			50	Ω
3A Divider Mode						
DP output voltage	$V_{DP\_DIVIDER}$	V_{OUT} = 5V	2.5	2.7	2.85	V
DP output impedance	$R_{DP\_DIVIDER}$		20	26	32	kΩ
DM output voltage	$V_{DM\_DIVIDER}$	V_{OUT} = 5V		3.4		V
DM output impedance	$R_{DM\_DIVIDER}$			20		kΩ
1.2V/1.2V Mode						
DP/DM output voltage	$V_{DP/DM\_1.2V}$	V_{OUT} = 5V	1.1	1.2	1.3	V
DP/DM output impedance	$R_{DP/DM\_1.2V}$		200	300	400	kΩ
USB Type-C 5V @ 3A Mode – CC1, CC2						
CC resistor to disable Type-C mode	R_A	CC1 pin, for Type-C mode applications add a 2.2nF capacitor on CC1	95.3	97.6	100	kΩ
CC pull-up current to detect Type-A mode	I_{PLL}		8	10	12	µA
CC voltage to enable V_{CONN}	V_{RA}				0.75	V
CC voltage to enable V_{BUS}	V_{RD}	Room temperature	0.85		2.45	V
CC voltage at 5.1kΩ R_D	V_{CC_RD}	CC pin pull-down by 5.1kΩ, room temperature	1.31	1.683	2.04	V
CC detach threshold	V_{OPEN}		2.65			V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +150°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
CC voltage falling debounce timer	$t_{CC\_DEBOUNCE}$	V_{BUS} enable deglitch	100	150	200	ms
CC voltage rising debounce timer	$t_{PD\_DEBOUNCE}$	V_{BUS} disable deglitch	0	10	20	ms
V_{CONN} output power	P_{VCONN}	V_{CONN} comes from the buck output with some series resistance	1			W
V_{BUS} to ground impedance	R_{BUS}	Type-C detach, after output discharge turn-off	72.4			kΩ
Quick Charge 3.0 Mode						
DP/DM low voltage	V_{QC_LOW}		0.25	0.3	0.4	V
DP/DM high voltage	V_{QC_HIGH}		1.8	2	2.2	V
DP output impedance	R_{DP_QC}		300	400	1500	kΩ
DM output impedance	R_{DM_QC}		15	20	25	kΩ
DM low glitch time (8)	t_{GLITCH_DM}			10		ms
DP high glitch time	t_{GLITCH_DP}		800	1200	1600	ms
Output voltage change glitch time	$t_{GLITCH\_V\_CHANGE}$		20	40	60	ms
Bus voltage (V_{BUS}) step	$V_{BUS\_CONT\_STEP}$		150	200	250	mV
Time for V_{BUS} to discharge to 5V when DP < 0.6V (8)	t_{V_UNPLUG}				500	ms

Note:

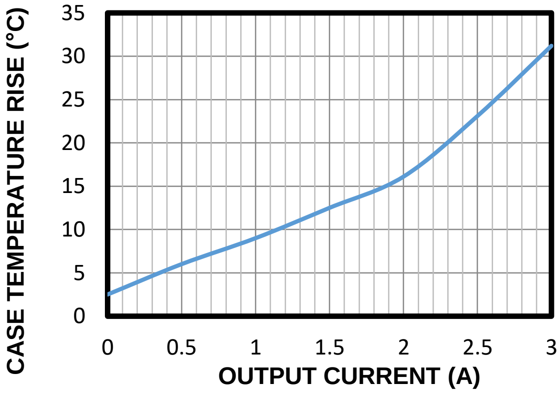
8) Guaranteed by engineering sample characterization.

TYPICAL CHARACTERISTICS

V_{IN} = 13.5V, V_{OUT} = 5.1V, L = 4.7µH, f_{SW} = 420kHz with spread spectrum, CC1 to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

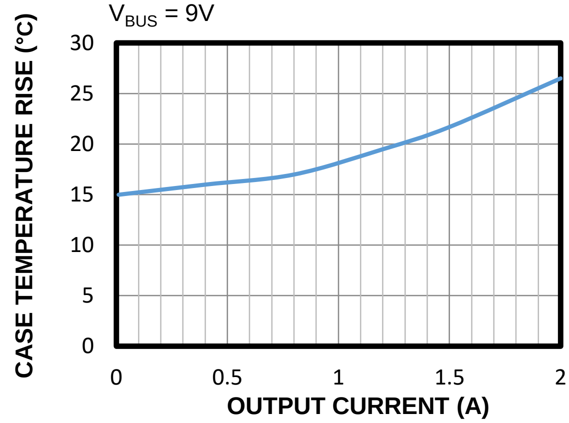
Case Temperature Rise vs. Output Current

V_{BUS} = 5.1V



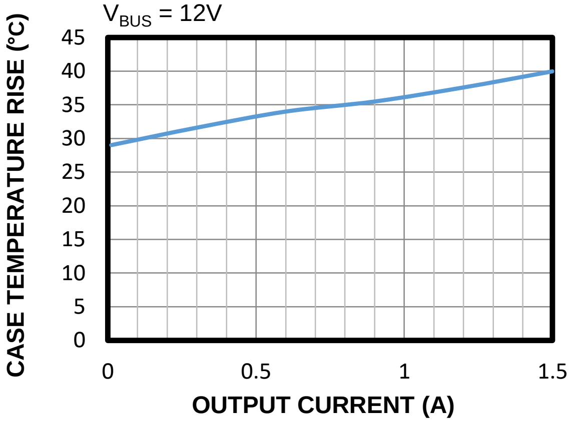
Case Temperature Rise vs. Output Current

V_{BUS} = 9V



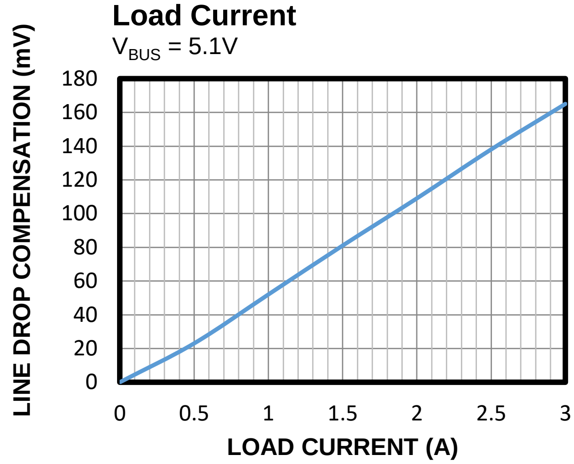
Case Temperature Rise vs. Output Current

V_{BUS} = 12V



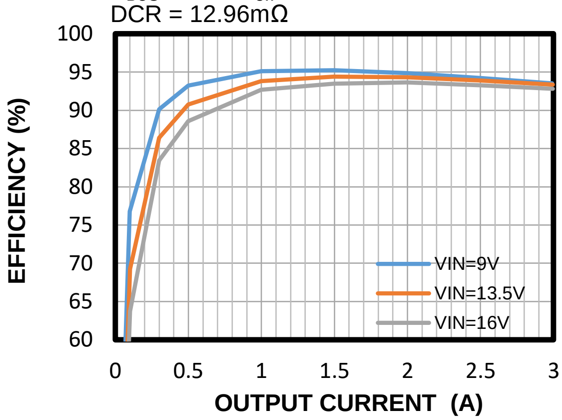
Line Drop Compensation vs. Load Current

V_{BUS} = 5.1V



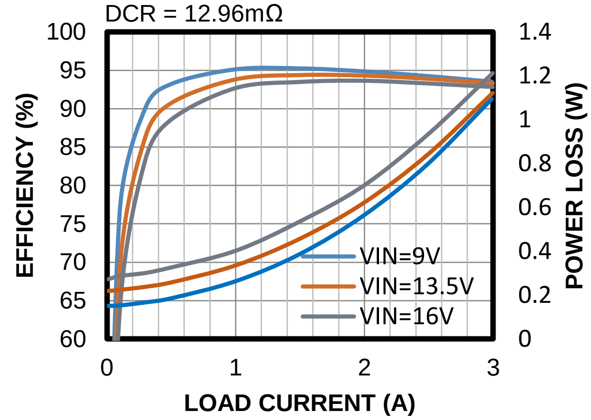
Efficiency vs. Load Current

V_{BUS} = 5.1V, f_{sw} = 420kHz, L = 4.7µH, DCR = 12.96mΩ



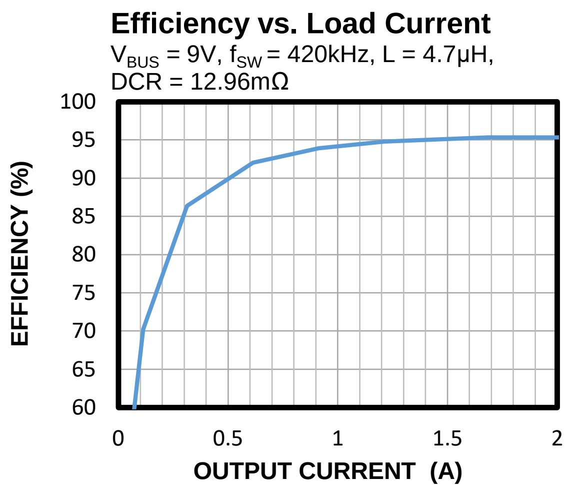
Efficiency vs. Load Current vs. Power Loss

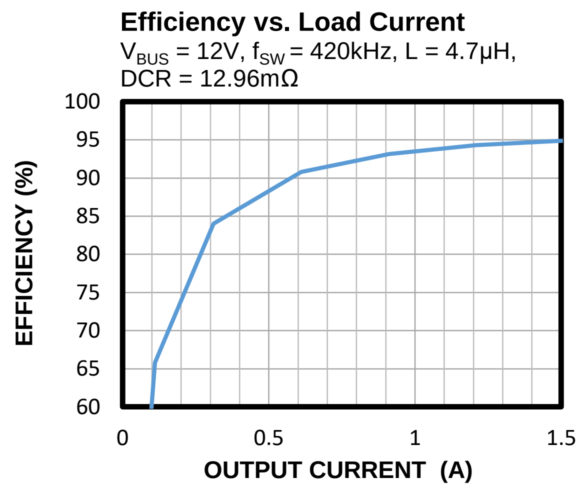
V_{BUS} = 5.1V, f_{sw} = 420kHz, L = 4.7µH, DCR = 12.96mΩ



TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 13.5V, V_{OUT} = 5.1V, L = 4.7µH, f_{SW} = 420kHz with spread spectrum, CC1 to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

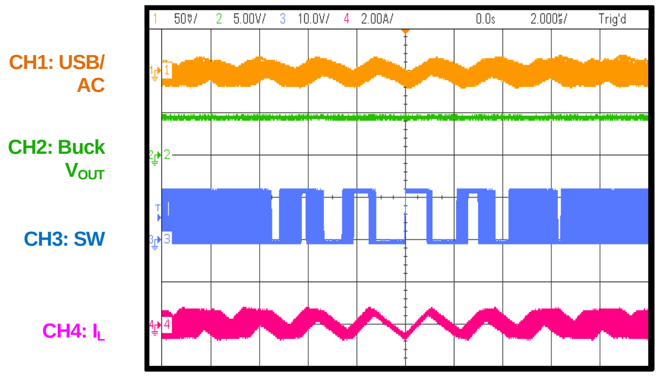




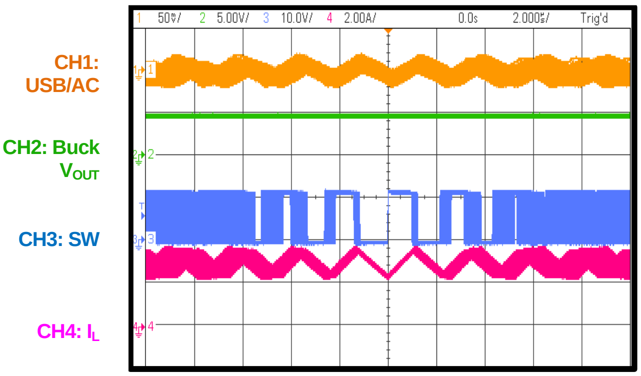
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 13.5V, V_{OUT} = 5.1V, L = 4.7µH, f_{SW} = 420kHz with spread spectrum, CC1 to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

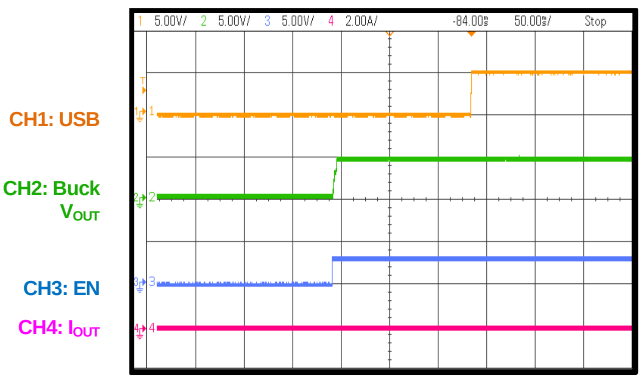
Steady State
Frequency spread spectrum is enabled,
I_{OUT} = 0A



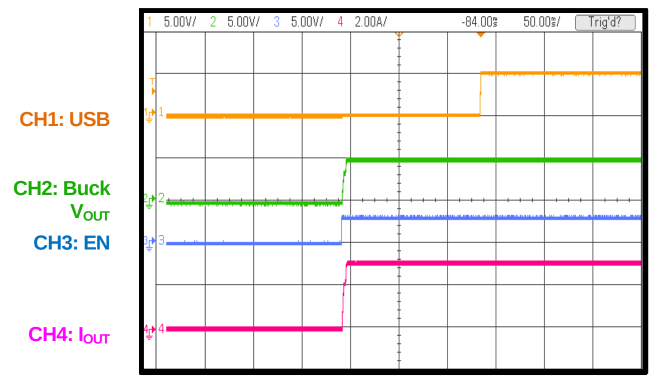
Steady State
Frequency spread spectrum is enabled,
I_{OUT} = 3A



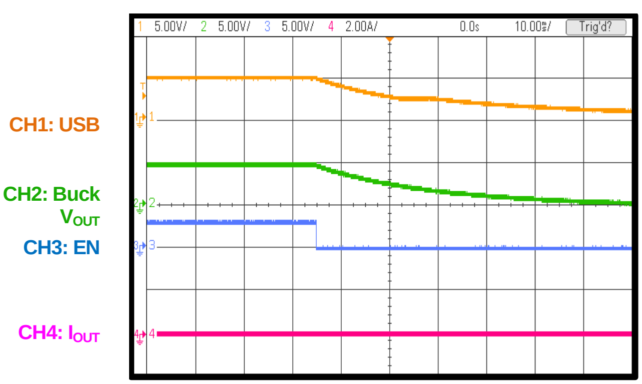
Start-Up through EN
I_{OUT} = 0A



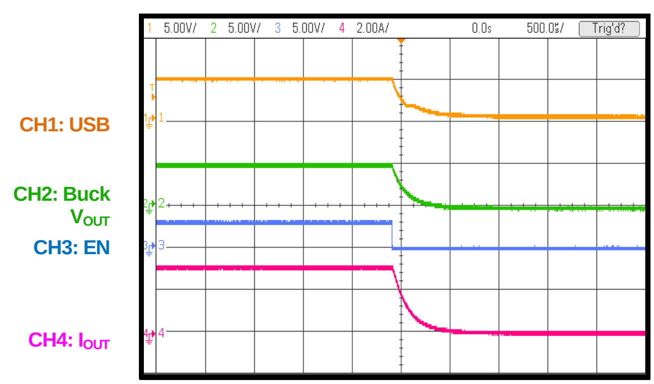
Start-Up through EN
I_{OUT} = 3A



Shutdown through EN
I_{OUT} = 0A



Shutdown through EN
I_{OUT} = 3A

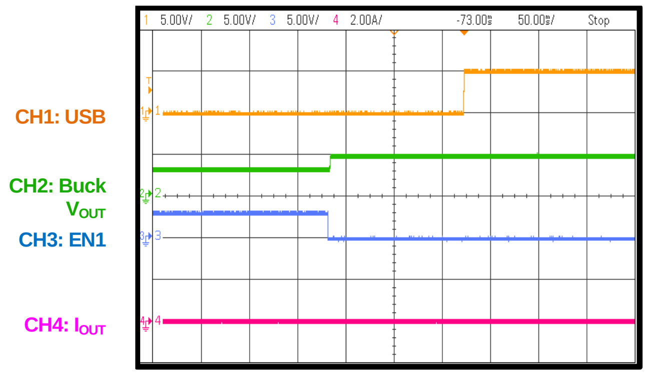


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 13.5V, V_{OUT} = 5.1V, L = 4.7µH, f_{SW} = 420kHz with spread spectrum, CC1 to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

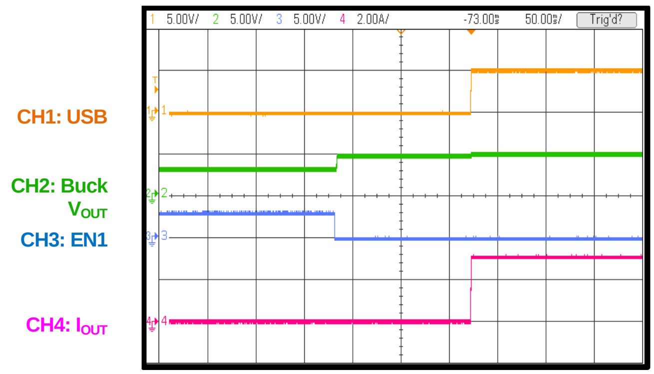
Start-Up through EN1

I_{OUT} = 0A



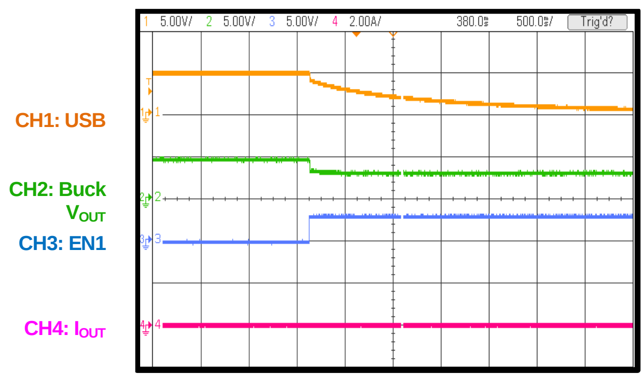
Start-Up through EN1

I_{OUT} = 3A



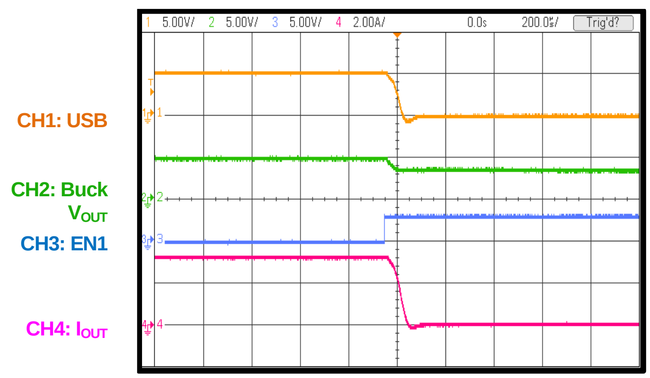
Shutdown through EN1

I_{OUT} = 0A



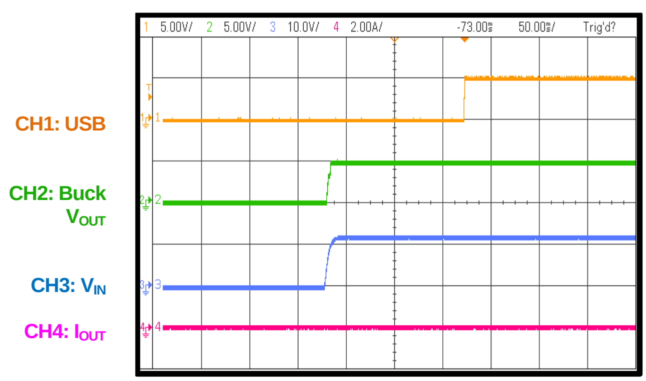
Shutdown through EN1

I_{OUT} = 3A



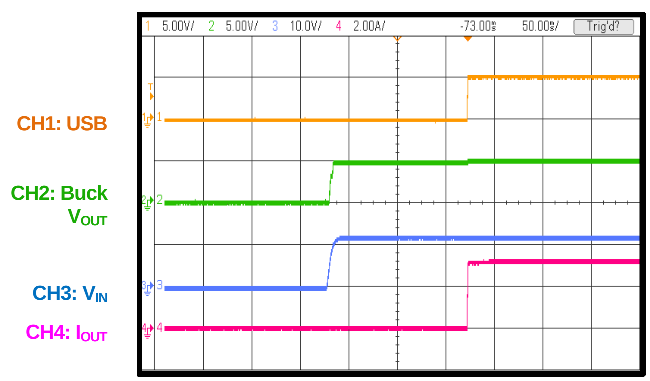
Start-Up through IN

I_{OUT} = 0A



Start-Up through IN

I_{OUT} = 3A

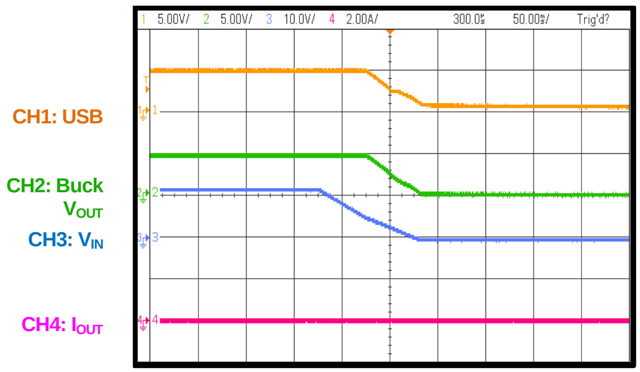


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 13.5V, V_{OUT} = 5.1V, L = 4.7µH, f_{SW} = 420kHz with spread spectrum, CC1 to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

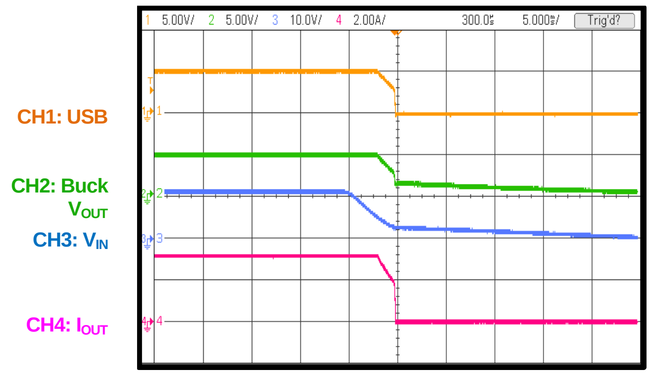
Shutdown through IN

I_{OUT} = 0A



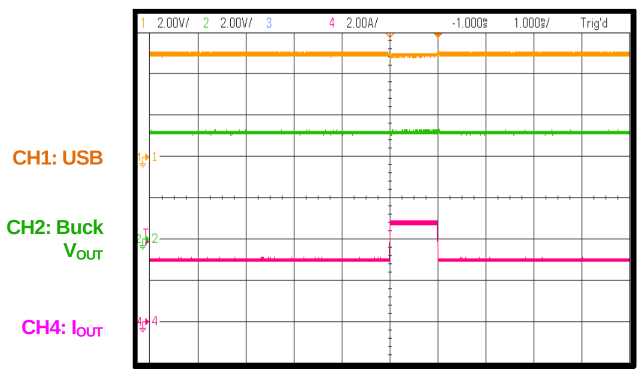
Shutdown through IN

I_{OUT} = 3A



MFI Over-Current Pulse Test

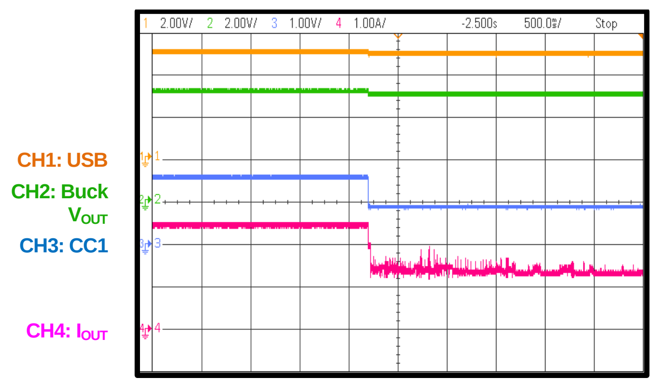
I_{OUT} = 3A to 4.8A, 1ms hold time



400µs/div.

Load-Shedding Entry

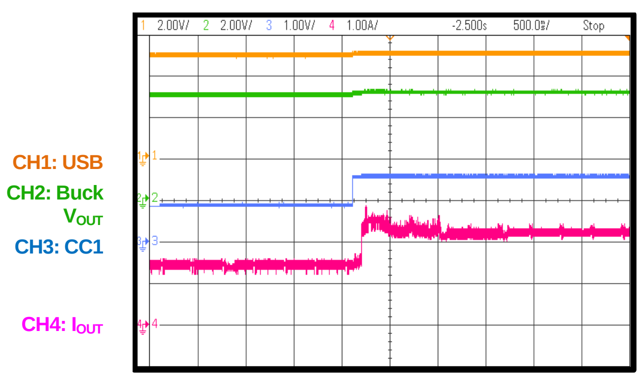
Connect to mobile phone during testing



10ms/div.

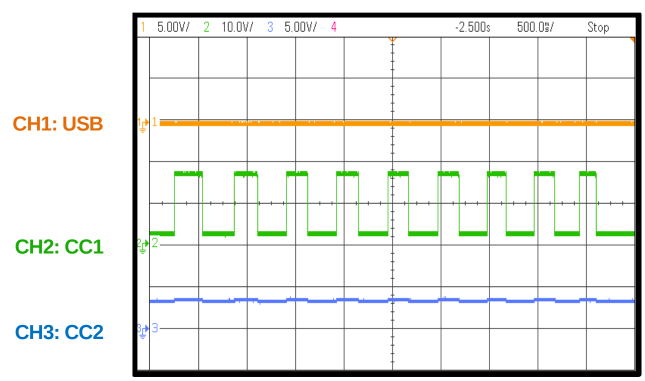
Load-Shedding Recovery

Connect to mobile phone during testing



CC1 Short to Battery

V_{BATT} = 18V, CC1 = CC2 = floating

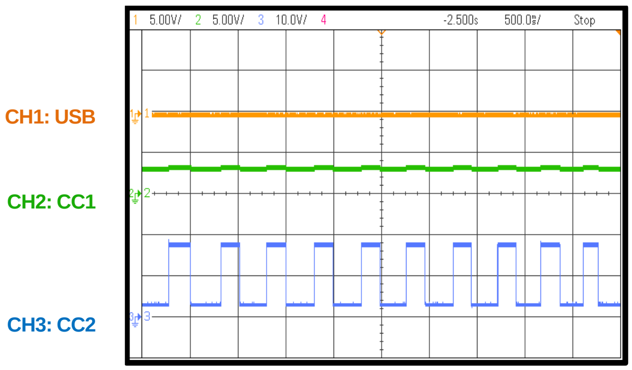


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 13.5V, V_{OUT} = 5.1V, L = 4.7µH, f_{SW} = 420kHz with spread spectrum, CC1 to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

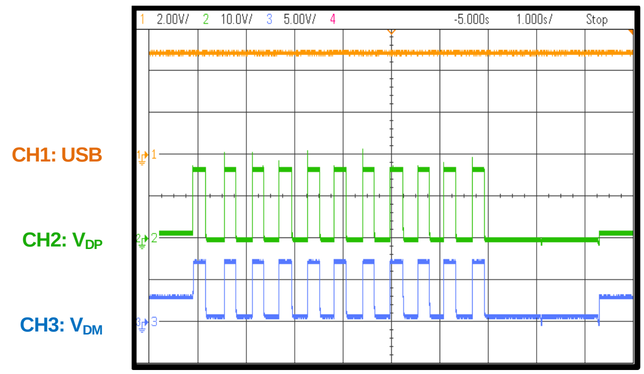
CC2 Short to Battery

V_{BATT} = 18V, CC1 = CC2 = floating



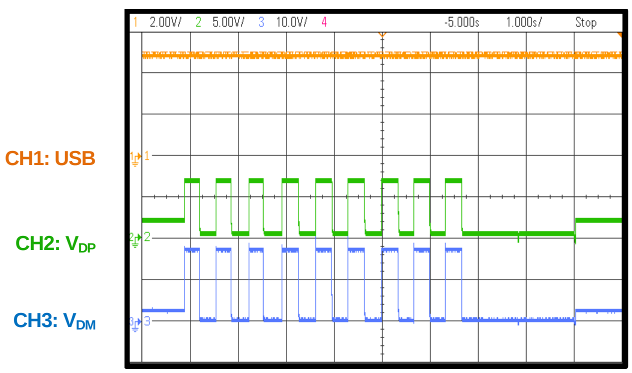
DP Short to Battery

V_{BATT} = 18V



DM Short to Battery

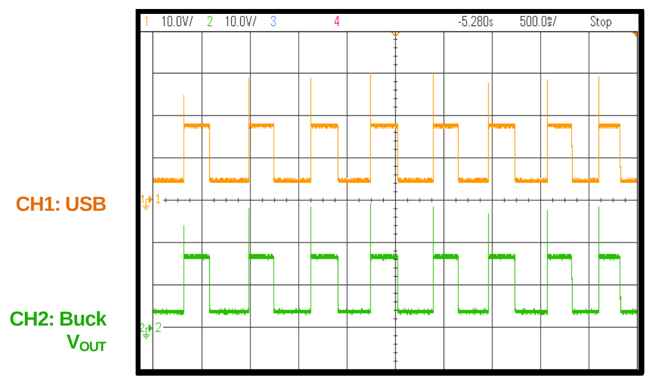
V_{BATT} = 18V



4ms/div.

USB_OUT Short to Battery

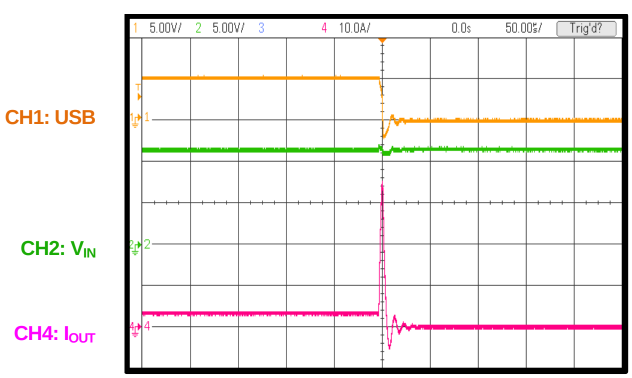
V_{BATT} = 18V, CC1 to ground with a 5.1kΩ resistor



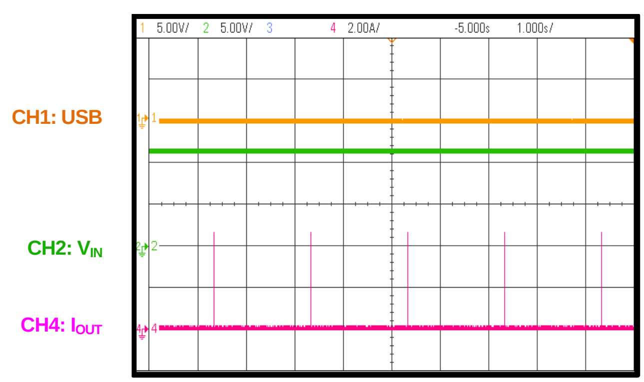
4ms/div.

USB_OUT Short-to-GND Entry

I_{OUT} = 3A



USB_OUT Short-to-GND Steady State

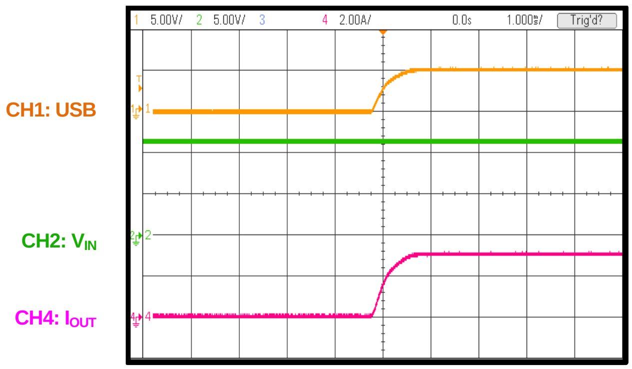


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 13.5V, V_{OUT} = 5.1V, L = 4.7µH, f_{SW} = 420kHz with spread spectrum, CC1 to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

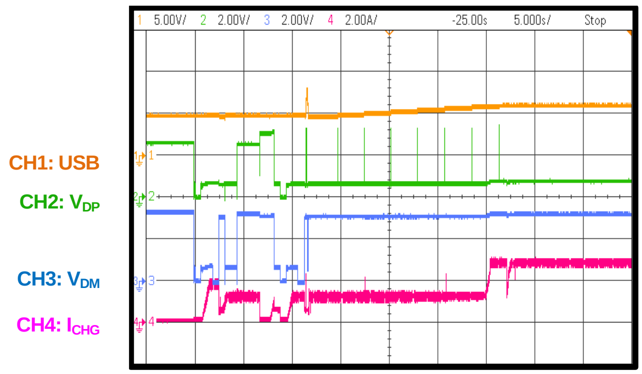
USB_OUT Short-to-GND Recovery

I_{OUT} = 3A



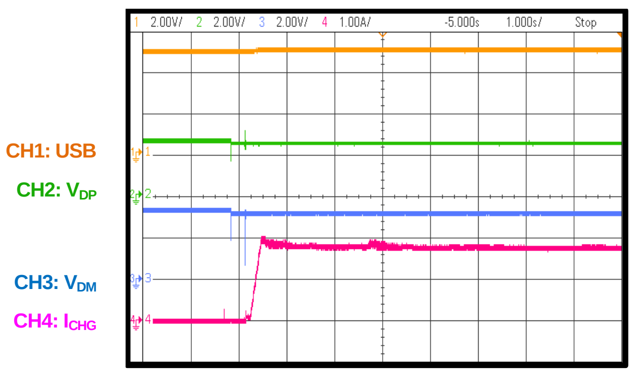
QC3.0 Device Charging Test

Mobile phone plug in



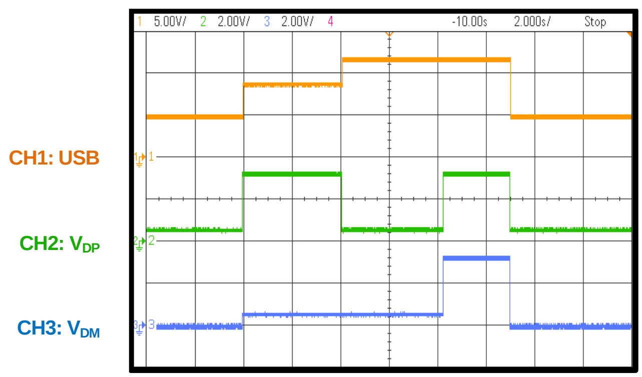
Apple Device Charging Test

Mobile phone plug in



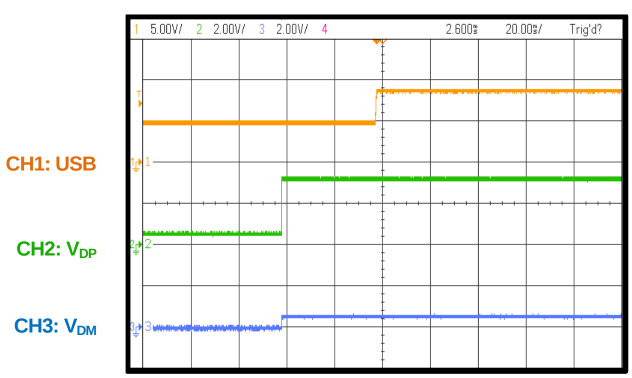
Voltage Mode Transition

5V to 9V to 12V to 5V



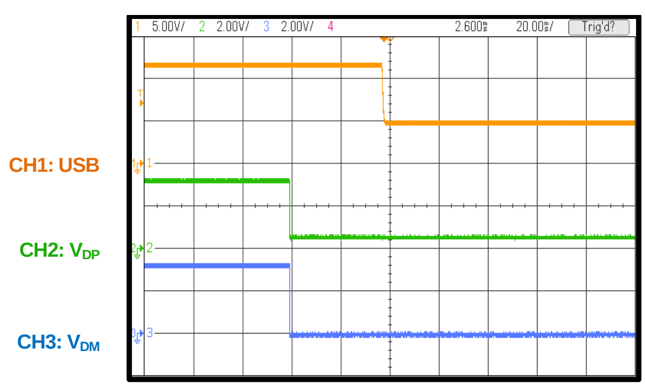
Voltage Mode Transition

5V to 9V, zoom in



Voltage Mode Transition

12V to 5V, zoom in

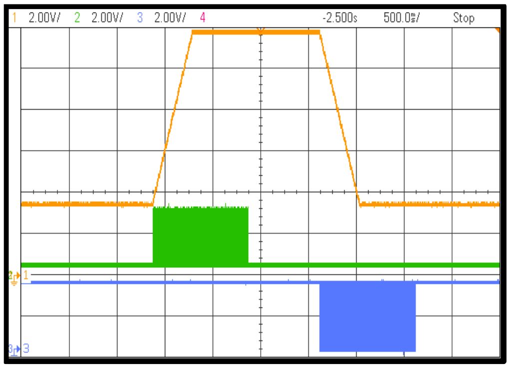


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 13.5V, V_{OUT} = 5.1V, L = 4.7µH, f_{SW} = 420kHz with spread spectrum, CC1 to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

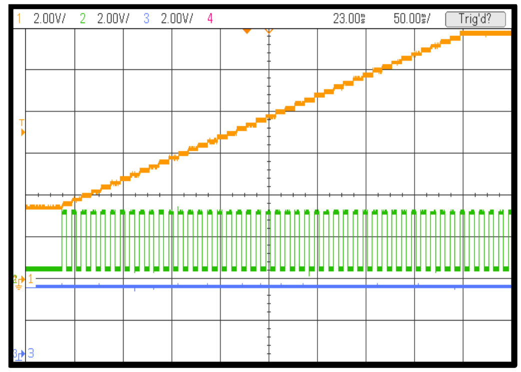
Adjusting V_{BUS} in Continuous Mode

3.6V to 12V to 3.6V



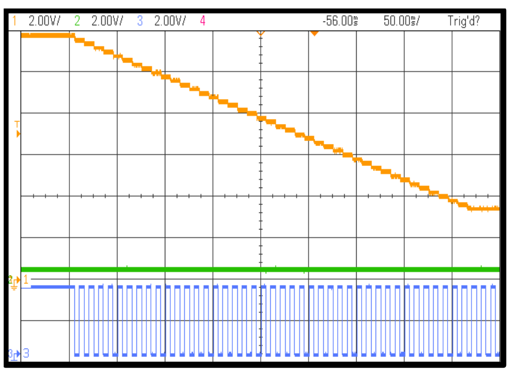
Adjusting V_{BUS} in Continuous Mode

3.6V to 12V, zoom in



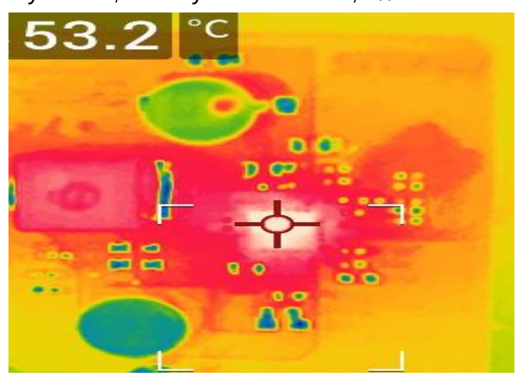
Adjusting V_{BUS} in Continuous Mode

12V to 3.6V, zoom in



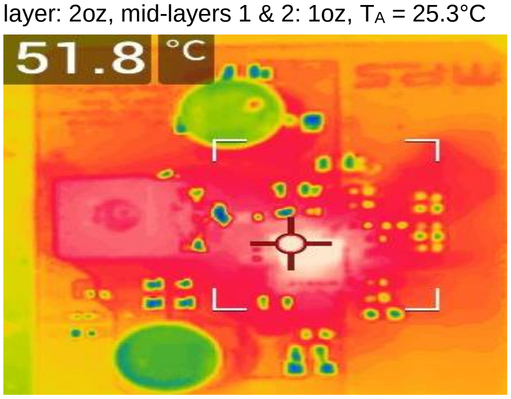
Case Thermal Test

V_{IN} = 13.5V, USB = 5.1V, I_{OUT} = 3A, measured on 4-layer PCB, 57.4mmx57.4mm, top/bottom layer: 2oz, mid-layers 1 & 2: 1oz, T_A = 22°C



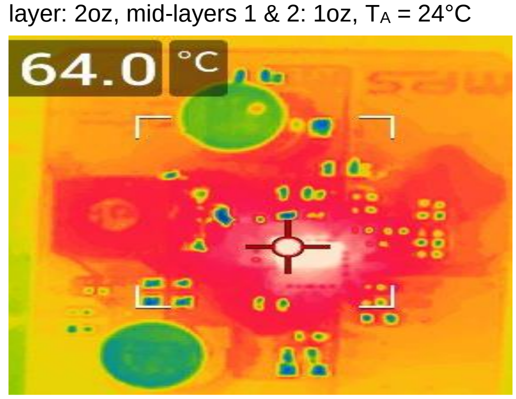
Case Thermal Test

V_{IN} = 13.5V, USB = 9V, I_{OUT} = 2A, measured on 4-layer PCB, 57.4mmx57.4mm, top/bottom layer: 2oz, mid-layers 1 & 2: 1oz, T_A = 25.3°C



Case Thermal Test

V_{IN} = 13.5V, USB = 12V, I_{OUT} = 1.5A, measured on 4-layer PCB, 57.4mmx57.4mm, top/bottom layer: 2oz, mid-layers 1 & 2: 1oz, T_A = 24°C



FUNCTIONAL BLOCK DIAGRAM

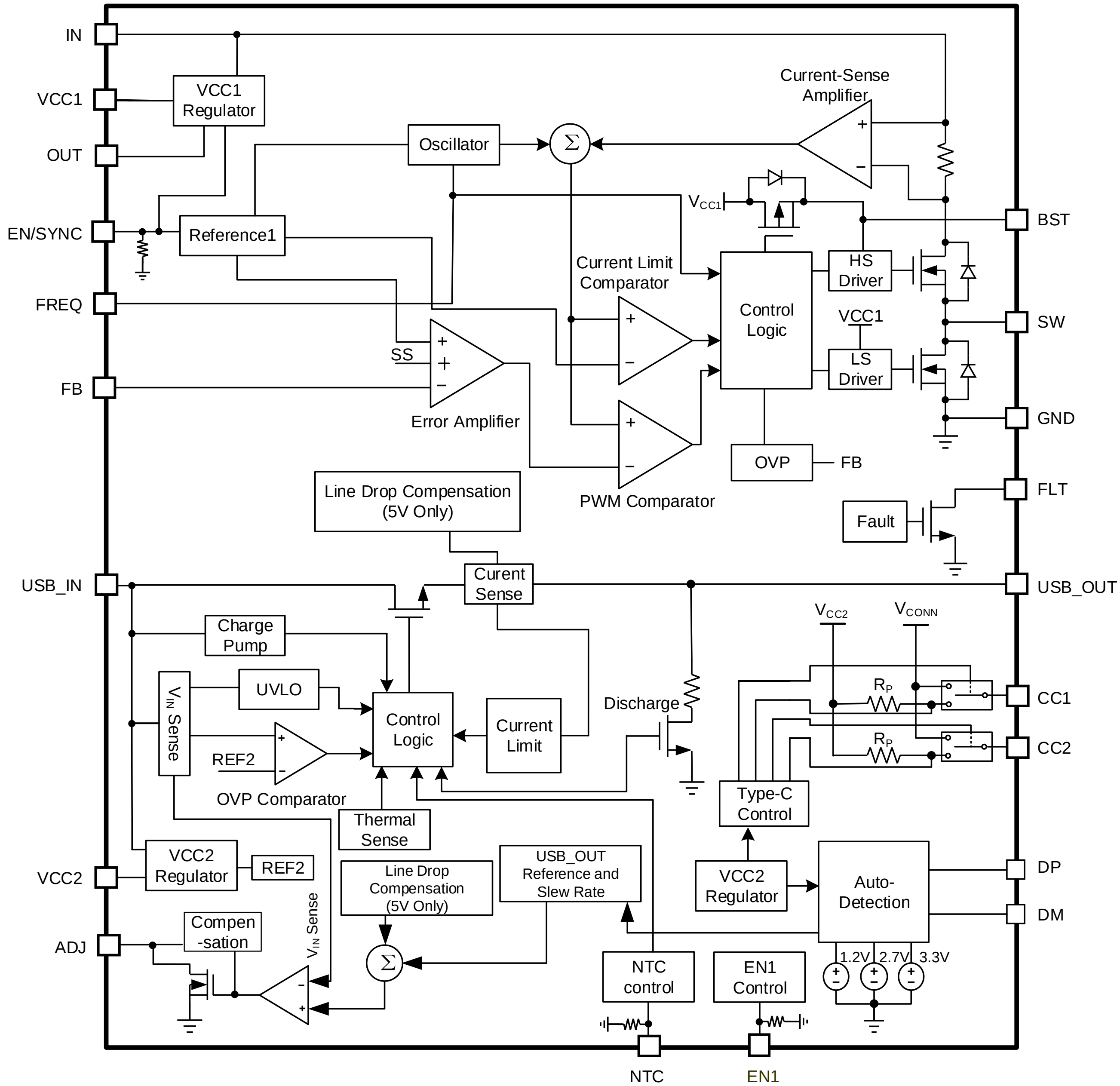


Figure 1: Functional Block Diagram

OPERATION

BUCK CONVERTER

The MPQ4228-Q integrates a monolithic synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs and a USB current-limit switch with charging-port auto detection. The converter offers a compact solution to achieve 3A of continuous output current (I_{OUT}) across a wide input supply range, with excellent load and line regulation.

The MPQ4228-Q operates with fixed-frequency, peak current mode control to regulate the output voltage (V_{OUT}). The internal clock initiates the PWM cycle, which turns on the integrated high-side MOSFET (HS-FET). The HS-FET remains on until its current reaches the value set by the COMP voltage (V_{COMP}). When the HS-FET is off, it remains off until the next clock cycle begins. If the duty cycle reaches 96% (420kHz switching frequency) in one PWM period, then the MOSFET current does not reach the COMP-set current value, and the MOSFET turns off. Under light loads, the converter enters PFM mode to achieve high efficiency.

Error Amplifier (EA)

The error amplifier (EA) compares the internal feedback voltage (V_{FB}) against the internal 0.8V reference voltage (V_{REF}) and outputs V_{COMP}. V_{COMP} controls the MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies control loop design.

Internal VCC1 Regulator

The 5V internal regulator powers most of the internal circuitries. This regulator can use either the buck converter's V_{OUT} or input voltage (V_{IN}) as the supply voltage. When V_{IN} is above 5V, the regulator's output is in full regulation. If V_{IN} is below 5V, the output decreases proportionately with V_{IN}. When V_{OUT} exceeds 4.75V, the VCC1 regulator is powered by V_{OUT} via the OUT pin to minimize low-dropout (LDO) power loss. VCC1 requires an external 0.22µF to 1µF ceramic decoupling capacitor.

EN/SYNC Control

EN/SYNC is a digital control pin that turns the regulator on and off. Drive EN high to turn the regulator on; drive EN low to turn it off. An internal 500kΩ resistor from EN/SYNC to GND allows EN/SYNC to be floated, which shuts down the chip.

The EN/SYNC pin is clamped internally with a 6.5V series Zener diode (see Figure 2). It is recommended to connect EN/SYNC to IN and GND with divider resistors. When selecting a pull-up resistor, it must be large enough to limit the current flow into EN/SYNC to less than 100µA. For example, if the EN/SYNC pull-up resistor is 100kΩ and the pull-down resistor is 36kΩ, then the IC starts up once V_{IN} exceeds 6V.

To connect the EN/SYNC pin directly to a voltage source without a pull-up resistor, limit the voltage amplitude to ≤5.5V to prevent damage to the Zener diode.

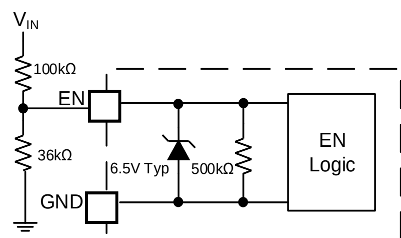


Figure 2: Zener Diode (6.5V Typical)

Connect a 200kHz to 2.2MHz external clock to synchronize the internal clock. Under external clock sync conditions, the MPQ4228-Q operates at a fixed frequency without spread spectrum. It is recommended to float the FREQ pin when synchronizing the switching frequency (f_{SW}) with an external clock.

The MPQ4228-Q's f_{SW} can be adjusted via the FREQ pin. When FREQ is pulled to GND, f_{SW} is 420kHz with spread spectrum (±10% dithering) and forced continuous conduction mode (FCCM). When FREQ is floating, f_{SW} is 420kHz with spread spectrum (±10% dithering) and pulse-frequency modulation (PFM) mode. When FREQ is pulled to VCC1, f_{SW} is 2.2MHz with spread spectrum (±10% dithering) and FCCM (see Table 1 on page 20).

Table 1: Switching Frequency Selection

FREQ Pin	Operation Mode	f_{SW}
GND	FCCM with spread spectrum	420kHz
Floating	PFM with spread spectrum	420kHz
VCC1	FCCM with spread spectrum	2.2MHz

Auto-PFM/PWM Mode (FREQ = Floating)

The MPQ4228-Q works in continuous conduction mode (CCM) mode under heavy loads. As the load decreases, the MPQ4228-Q first enters discontinuous conduction mode (DCM), and maintains a fixed frequency as long as the inductor current (I_L) approaches 0A. If the load is further decreased or there is no load that drops the inductor peak current below the AAM peak current threshold, then the MPQ4228-Q enters pulse-skip mode (PSM) to further improve the light-load efficiency.

Under very light loads or no load, V_{FB} decreases slowly and V_{COMP} ramps up until it reaches V_{AAM}. When the clock goes high, the HS-FET turns on and remains on until $V_{ILSENSE}$ reaches the value set by V_{COMP}. When V_{COMP} < V_{AAM}, the internal clock is blocked and the MPQ4228-Q skips some pulses; this operation is called pulse frequency modulation (PFM) mode. This control scheme improves efficiency by scaling down the frequency to reduce switching losses and gate driver losses.

As I_{OUT} increases from light-load conditions, V_{COMP} and f_{SW} also increase. If I_{OUT} exceeds the critical level set by V_{COMP}, then the MPQ4228-Q resumes fixed-frequency PWM control.

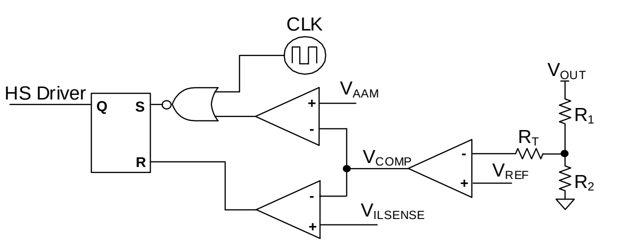


Figure 3: Auto-PFM/PWM Operation Control Logic

Forced Continuous Conduction Mode (FCCM) (FREQ = GND or VCC1)

The MPQ4228-Q works in forced continuous conduction mode (FCCM) under all conditions. The MPQ4228-Q operates with a fixed f_{SW}, regardless of whether it is operating under light-load or heavy-load conditions. The advantages of FCCM include a controllable frequency, smaller output ripple, and sufficient bootstrap charge time; however, it also has low efficiency under light-load conditions. The selected inductance must be such that it avoids triggering the low-side MOSFET's (LS-FET's) negative current limit (typically 3A from SW to GND). If the negative current limit is triggered, then the LS-FET turns off and the HS-FET turns on once the internal clock cycle begins.

Frequency Spread Spectrum

The purpose of frequency spread spectrum is to minimize the peak emissions at a specific frequency. The MPQ4228-Q uses a 4kHz triangle wave (125µs rising, 125µs falling) to modulate the internal oscillator. The spread spectrum operation frequency span is ±10% (see Figure 4).

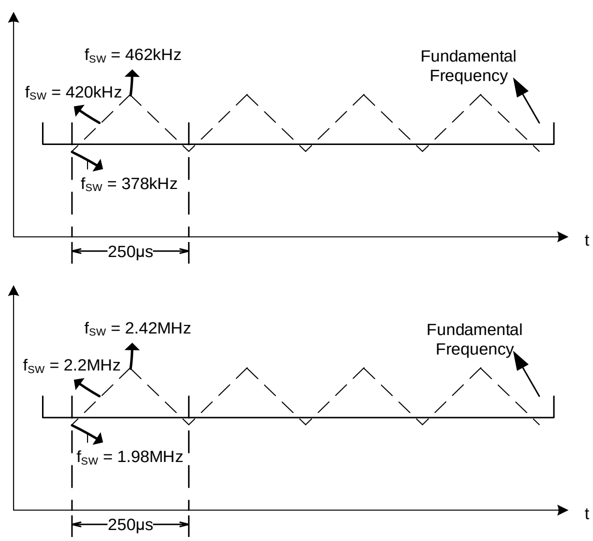


Figure 4: Frequency Spread Spectrum

Connect FREQ to GND or float it for a 420kHz f_{SW} with frequency spread spectrum. Connect FREQ to VCC1 for a 2.2MHz f_{SW} with frequency spread spectrum.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the MPQ4228-Q from operating at an insufficient supply voltage. The UVLO comparator monitors V_{IN}. The UVLO rising threshold is 3.7V, and its falling threshold is 3.25V.

Internal Soft Start (SS)

Soft start (SS) prevents the converter's V_{OUT} from overshooting during start-up. When the chip starts up, the internal circuitry generates a SS voltage (V_{SS}) that ramps up from 0V to 5V. When V_{SS} is below V_{REF}, the EA uses V_{SS} as the reference. When V_{SS} is above V_{REF}, the EA uses V_{REF} as the reference.

If the MPQ4228-Q's output is pre-biased to a certain voltage during start-up, then the IC disables the switching of both the HS-FET and LS-FET until the voltage on the internal SS capacitor (C_{SS}) exceeds the internal V_{FB}.

Buck Over-Current Protection (OCP)

The MPQ4228-Q has a cycle-by-cycle over-current (OC) limit when the inductor peak current exceeds the current-limit threshold and V_{FB} drops below the under-voltage (UV) threshold (typically 50% below V_{REF}). Once UV is triggered, the MPQ4228-Q enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground. This greatly reduces the average short-circuit current, alleviates thermal issues, and protects the regulator. Once the over-current condition is removed, the MPQ4228-Q exits hiccup mode and resumes normal operation.

Over-Voltage Protection (OVP)

The MPQ4228-Q detects an output over-voltage (OV) condition through the FB pin. When V_{OUT} exceeds 115% of the target voltage, the OVP comparator output goes high. The device stops switching and turns on the discharge resistor connected between OUT and ground until V_{OUT} falls below 105% of the target voltage.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. The UVLO rising threshold is 2.2V, with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by IN and VCC1 through D1, M1, C4, L1, and C2 (see Figure 5). The BST capacitor (C4) voltage is charged up quickly by VCC1 through M1. The 1µA input to BST current source also can charge C4 when the LS-FET is turned off.

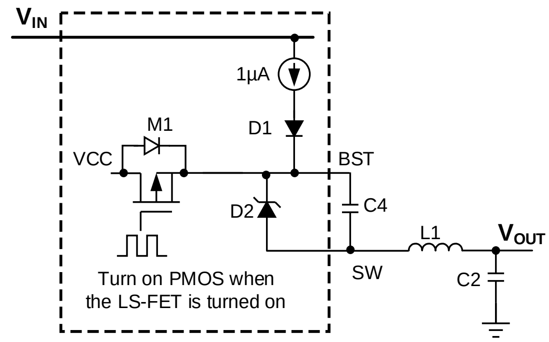


Figure 5: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both IN and EN exceed their respective thresholds, the chip is enabled. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Several events can shut down the chip: EN going low, V_{IN} going low, and thermal shutdown. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. Then V_{COMP} and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

Buck Output Discharge

The MPQ4228-Q includes an output discharge function that provides a resistive discharge path for the external output capacitor. Three scenarios can trigger the output to discharge:

1. V_{IN} falls beneath its UVLO threshold.
2. The part is turned off.
3. An output OV condition occurs.

If any of these scenarios occurs, then the discharge path turns off once V_{OUT} drops below 0.5V or the maximum 200ms timer completes, whichever occurs first.

USB CURRENT-LIMIT SWITCH

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at insufficient supply voltage. Once V_{IN} exceeds the USB SW UVLO threshold, there is a fixed delay time, and then the power MOSFET starts up with a controlled slew rate.

EN1 Function

The EN1 pin turns the USB switch on and off. EN1 is active low. When EN1 is pulled low, the USB is enabled; when EN1 is pulled high, the USB is disabled. By default, EN1 is pulled low by an internal 1MΩ resistor.

Pull EN1 high to disable the USB switch; pull EN1 low to enable it. The buck output is still active even when EN1 is high. The maximum EN1 voltage is 4V.

Internal Soft Start (SS)

The internal soft start (SS) prevents V_{OUT} from overshooting and from inrush current during start-up.

Line Drop Compensation

The MPQ4228-Q is capable of compensating a V_{OUT} drop, such as high impedance caused by a long trace, to maintain a fairly constant 5.1V load-side voltage. The line drop compensation is only active at V_{IN} = 5.1V. Line drop compensation functions through the ADJ pin.

At a 3A output current, the MPQ4228-Q increases the USB V_{IN} by 170mV (see Figure 6).

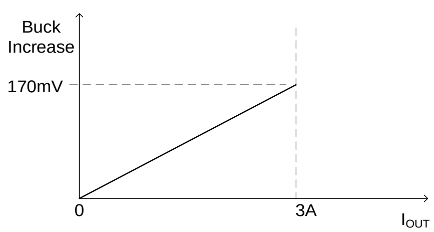


Figure 6: Line Drop Compensation

The voltage on the ADJ pin (V_{ADJ}) slowly sinks a controlled current, and the line drop compensation amplitude increases linearly as the load current increases.

Under no-load conditions, if the USB V_{IN} is below 5.1V, then ADJ pin sinks a current to regulate the upstream regulator's V_{OUT} to 5.1V. If the USB V_{IN} is above 5.1V, then the MPQ4228-Q stops regulating V_{IN}. To achieve a 3.6V to 12V V_{OUT} range, configure R1 and R2 to a default V_{OUT} below 3.6V. It is recommended to set buck V_{OUT} to 3.5V (i.e. R1 = 44.2kΩ, R2 = 13kΩ).

Figure 7 shows typical usage of the ADJ pin. The ADJ pin's sink current capability is 500μA. The feedback current through R1 must be below 500μA.

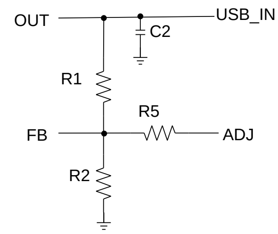


Figure 7: ADJ Configuration

Calculate R1 with Equation (1):

$$R1(k\Omega) > \frac{\Delta V(V)}{0.5} \quad (1)$$

Where ΔV is the output differential voltage value, which is determined by the QC3.0 max voltage minus the buck converter's voltage.

The ADJ sink current limits the maximum V_{OUT}, and inserting R5 between the FB pin and the ADJ pin can limits the maximum ADJ sink current. With R5, the maximum output voltage (V_{OUT_MAX}) can be calculated with Equation (2):

$$V_{OUT\_MAX}(V) = \frac{R1 + R2 // R5}{R2 // R5} \times V_{FB}(V) \quad (2)$$

After adding R5, the maximum ADJ sink current (I_{ADJ_MAX}) can be calculated with Equation (3):

$$I_{ADJ\_MAX}(\mu A) = \frac{V_{FB} - V_{ADJ\_OFFSET}(mV)}{R_5(k\Omega)} \quad (3)$$

Where V_{ADJ_OFFSET} is about 100mV.

USB Input Over-Voltage and Discharge

The MPQ4228-Q has a smart OVP threshold for different V_{OUT} values. The IC dynamically sets the OVP threshold to 115% of the V_{OUT} target value. A fast, accurate comparator monitors for any OV conditions on the input. If V_{IN} exceeds the threshold, the input-to-ground discharge path becomes active (the USB current-limit switch is still enabled). When V_{IN} falls below 5.52V, the IC exits OVP and resumes normal operation.

Output Discharge

When a USB Type-C device is unplugged, both discharge resistors (USB_IN and USB_OUT) remain active for 30ms, then turn off. After they turn off, the USB_IN-to-ground resistance and USB_OUT-to-ground resistance is very large (>72.4kΩ).

Over-Current Protection (OCP)

During normal operation, once the load current reaches the current-limit threshold, the MPQ4228-Q starts a 1.7ms counter. The device does not limit I_{OUT} within this 1.7ms period (see Figure 8).

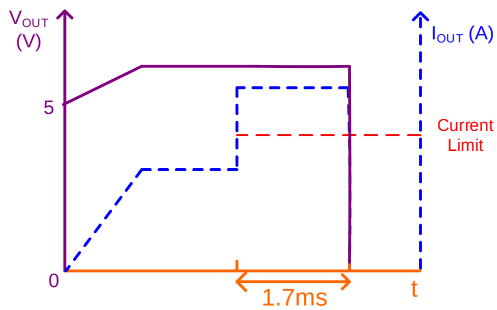


Figure 8: Over-Current Limit

If the over-current (OC) time exceeds the 1.7ms timer, the USB channel enters hiccup mode, with 2ms of on time and 2s of off time.

If the OC signal disappears during the 1.7ms period, then the MPQ4228-Q resets the counter.

If a short circuit occurs before start-up, the MPQ4228-Q enters constant current limit mode during SS. Once SS is complete, if the USB V_{OUT} remains low then the MPQ4228-Q enters hiccup mode.

In hiccup mode, the MPQ4228-Q turns off the power MOSFET. The hiccup signal resets the QC mode to 5V. ADJ changes V_{IN} to 5V. After 2s (the hiccup off-timer), the MPQ4228-Q restarts. If the OC condition remains, the MPQ4228-Q repeats this operation. If the OC condition has been removed, then the MPQ4482-Q resumes normal operation in 5V mode.

Short-Circuit Protection (SCP)

If the load current increases rapidly due to a short circuit, the current may significantly exceed the current limit threshold before the control loop can respond. If the current reaches an internal, secondary current limit level (about 10.5A), a fast turn-off circuit activates to turn off the MOSFET. This limits the peak current through the MOSFET to limit the V_{IN} drop. The typical fast-off response time is 300ns. Fast-off keeps the MOSFET turned off for 80µs. After this time elapses, the MOSFET turns on again. If the short-circuit condition is still present, then the USB current-limit switch treats it as an OC condition again and enters hiccup mode. If the silicon die temperature of the USB switch exceeds 165°C in the condition, the USB current-limit switch enters thermal shutdown. Once the short-circuit condition is removed, the MPQ4228-Q recovers automatically.

Short-to-Battery Protection

The MPQ4228-Q provides CC1, CC2, DP, DM, and USB_OUT short-to-battery protections when the IC is enabled and V_{BUS} is on. USB_OUT short-to-battery protection requires parallel a Schottky diode when V_{BUS} is off (see Figure 9).

During a USB output short-to-battery condition, the USB input triggers OVP, and the USB input discharge path turns on.

During a CC1/CC2 or DP/DM short-to-battery condition, the MPQ4228-Q can withstand high voltage on the internal components. The ESD breakdown voltage is significantly greater than the battery voltage.

A CC1, CC2 short-to-battery can easily occur when a Type-C port is connected with a cable but no sink (the device is unattached).

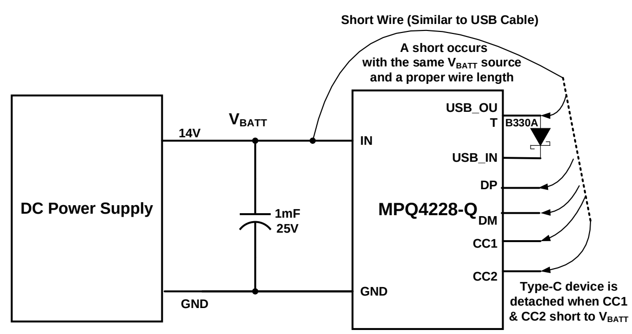


Figure 9: Short to Battery Set-Up

Fault Indication

FLT is the fault indication pin. FLT is an open drain during shutdown, start-up, and normal operation. It asserts (logic low) during USB over-current/short circuitry, USB_IN over-voltage, DP/DM/CC1/CC2 pin over-voltage (short to battery), and over-temperature conditions.

FLT asserts low until the fault condition is removed and the USB V_{OUT} goes back to high. There is a 2ms deglitch timer during an over-current (OC) condition to prevent a false FLT trigger. The FLT signal is not deglitched during over-voltage (OV) (short to battery) or over-temperature (OT) conditions.

Auto-Detection

The MPQ4228-Q's USB dedicated charging port (DCP) integrates an auto-detection function. This function recognizes most mainstream portable devices. It supports the following charging schemes:

- USB Battery Charging Specification BC1.2/ Chinese Telecommunications Industry Standard YD/T 1591-2009
- Apple 3A Divider Mode
- 1.2V/1.2V Mode
- USB Type-C 5V @ 3A Mode
- Quick Charge 3.0 Mode Class A

The auto-detection function is a state machine that supports all of the DCP charging schemes list above. The state machine starts in 3A divider mode. If a BC1.2 device is attached, the MPQ4228-Q exits the 3A divider mode and enters BC1.2 short mode. If the device supports QC2.0 or QC3.0, then the MPQ4228-Q enters quick charge mode. 1.2V/1.2V mode turns on in a time window when the MPQ4228-Q enters BC1.2 short mode. The MPQ4228-Q goes back to 3A divider mode when the downstream device releases a DP/DM line or is unplugged.

QC Mode Voltage Transition (Class A)

If the downstream device supports QC specifications, then the device can require a V_{OUT} above 5V by communicating with MPQ4228-Q's DP and DM pins (see Table 2). If a higher USB V_{BUS} is required, then the ADJ pin needs to be used to adjust the buck V_{OUT}. The ADJ pin is typically connected to the feedback (FB) pin of the upstream voltage converter. After the handshake, ADJ adjusts V_{OUT} to 9V to 12V or any other voltage step by step (200mV/step). In smart controller mode, only one ADJ pin can set a high voltage that meets QC specifications. The V_{OUT} transition is smooth, and does not have any voltage undershoot/overshoot. Figure 10 shows the mode transition.

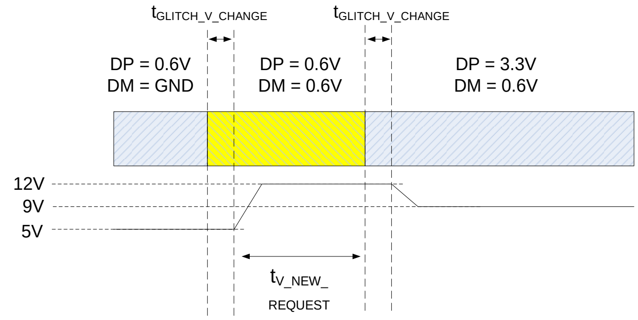


Figure 10: QC Mode Transition

Table 2 shows the QC mode definitions.

Table 2: QC Mode Definition

Portable Device		USB Bus Voltage
DP	DM	
0.6V	0.6V	12V
3.3V	0.6V	9V
0.6V	3.3V	3.6V to 12V (200mV steps) according to QC3.0
3.3V	3.3V	No action
0.6V	GND	5V

When the downstream device is removed, V_{OUT} automatically returns to its default 5V. The input to ground discharge resistor will help this procedure quickly.

USB Type-C Mode and V_{CONN}

For USB Type-C solutions, two pins on the connector (CC1 and CC2) are used to establish and manage the source-to-sink connection. The general concept for setting up a valid connection between a source and a sink is based on being able to detect terminations residing in the product being attached. To help define the functional behavior of CC1 and CC2, a pull-up (R_P) and pull-down (R_D = 5.1kΩ) termination model is used, based on a pull-up resistor and pull-down resistor (see Figure 11).

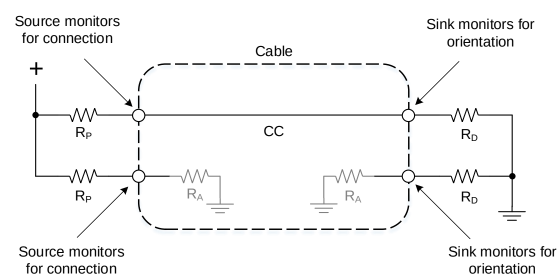


Figure 11: Current Source/Pull-Down CC Model

Initially, a source exposes independent R_P terminations on its CC1 and CC2 pins, and a sink exposes independent R_D terminations on its CC1 and CC2 pins. This source-to-sink circuit configuration represents a valid connection. To detect this, the source monitors CC1 and CC2 for a voltage below its unterminated voltage. R_P is a function of the pull-up termination voltage and the source's detection circuit. This indicates that a sink, a powered cable, or a sink connected via a powered cable has been attached (see Figure 12).

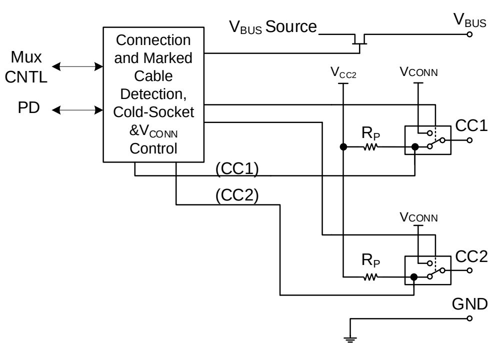


Figure 12: CC Pin Functional Block

Two special termination combinations on the CC pins (as seen by a source) are defined for directly attached accessory modes: R_A / R_A for audio adapter accessory mode, and R_D / R_D for debug accessory mode. V_{OUT} is disabled for both of these cases.

1. The source uses a FET to enable and disable power delivery across V_{BUS} (the source is disabled initially).
2. The source supplies pull-up resistors (R_P) on CC1 and CC2, and monitors both to detect a sink. The presence of an R_D pull-down resistor on either pin indicates that a sink is attached. The value of R_P indicates the initial USB Type-C current level supported by the host. The MPQ4228-Q default R_P is 4.7kΩ, which represents a 3A current level.
3. The source uses the CC pin pull-down characteristic to detect and determine which CC pin is intended to supply V_{CONN} (when R_A is detected).
4. Once a sink is detected, the source enables V_{BUS} and V_{CONN}.
5. The source can dynamically adjust the value of R_P to indicate a change in the available USB Type-C current to a sink. For example, at high temperatures, the MPQ4228-Q changes R_P to 12.7kΩ to indicate a 1.5A current capability.
6. The source monitors R_D continually to detect a sink detach event. When a detach event is detected, the source removes V_{BUS} and V_{CONN} and returns to step 2.

Disable Type-C Mode (Type-A Mode)

During initial start-up, the MPQ4228-Q sources a 10µA current (typical) for 50µs (typical) on the CC1 pin. To enter Type-A mode, use a 97.6kΩ CC1 resistor and a 0.976V CC1 voltage (V_{CC1}). V_{CC1} must be within the Type-A mode voltage detection range. The USB is latched at Type-A mode until power is recycled. Type-C mode is disabled, which means that the CC attach and detach logic is also disabled and that V_{BUS} is always enabled. The current limit also changes to Type-A specifications.

To trigger this mode, the external pull-down resistor should be 97.6kΩ. Do not connect extra capacitors on the CC1 pin.

Negative Temperature Coefficient (NTC) Thermistor and Load-Shedding

The MPQ4228-Q has a built-in NTC comparator that allows the external device's temperature to be sensed via the thermistor mounted near the device. This ensures a safe operating environment and prevents any smoke or fire from occurring due to an over-temperature (OT) condition.

Connect a resistor from NTC to GND. Connect the thermistor from NTC to VCC2.

If NTC is pulled to between 50% and 70% of V_{CC2} before IN starts up, then the MPQ4228-Q enters Type-C 1.5A mode. If NTC is pulled above 70% of V_{CC2}, then the MPQ4228-Q disables the USB output and FLT pin is kept low.

In normal operation, once the NTC voltage (V_{NTC}) exceeds 50% of V_{CC2}, the USB port's CC pin pull-up resistance (R_P) changes to 12.7kΩ to advertise its source capability (1.5A). The internal R_D detection threshold also changes to be between 0.4V and 1.6V, and the R_A detection threshold changes to <0.4V. The current limit does not change. The ADJ function remains operational even during the load-shedding period. The line drop compensation function is disabled when IC enters load-shedding.

When V_{NTC} falls to 24% of V_{CC2}, the USB Type-C current capability changes back to 3A (R_P = 4.7kΩ) and the MPQ4228-Q resumes normal operation (see Figure 13). Once V_{NTC} rises to 70% of V_{CC2}, the MPQ4228-Q turns off the USB switch and pulls FLT low. The USB switch turns on when V_{NTC} falls to 60% of V_{CC2}.

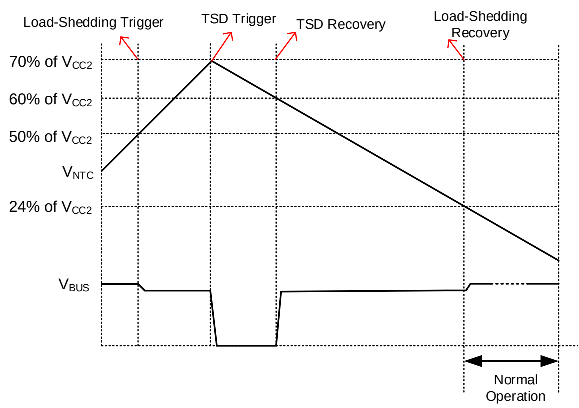


Figure 13: NTC Trigger and Recovery

Internal Load-Shedding vs. Temperature

The MPQ4228-Q also has an internal thermal sense function. The internal thermal sense function is works in conjunction with the NTC pin. If V_{NTC} > 50% of V_{CC2}, or the internal sensed temperature > 145°C, the IC enters load-shedding. Pull NTC pin low or float it to disable the NTC function.

When the sensed temperature exceeds 145°C, the USB port's CC pin pull-up resistance (R_P) changes to 12.7kΩ to advertise its source capability (1.5A). The internal R_D detection threshold changes to be between 0.4V and 1.6V, and the R_A detection threshold changes to <0.4V. The current limit does not change.

If the sensed temperature falls below 105°C and lasts for 16s, then the USB Type-C current capability changes back to 3A (R_P = 4.7kΩ). The line drop compensation function is disabled when the IC enters load-shedding.

Thermal Shutdown (TSD)

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the silicon die temperature of the USB switch exceeds 165°C, the USB current-limit switch shuts down. The CC pins' functional block and DP and DM pins' functional block remains active. Once the temperature falls below its lower threshold (typically 145°C), the USB current-limit switch is enabled and the IC resumes normal operation.

APPLICATION INFORMATION

Design Example for R1, R2, the ADJ Resistor, and the RT Resistors

R1, R2, and the ADJ resistor are limited by the ADJ sink capability and the maximum V_{OUT}.

The ADJ pin's sink current capability is 500µA. To achieve a 12V V_{OUT} during QC 3.0 mode and to limit the feedback current flowing through R1 to below 500µA, R1 should be calculated with Equation (1) (see page 22). ∆V is the output differential voltage value, which is determined by the QC3.0 max voltage minus the buck converter's voltage. If the buck converter's voltage is set to 3.5V, then R1 can be calculated with Equation (4):

$$R1(k\Omega) > \frac{\Delta V(V)}{0.5} = \frac{12-3.5}{0.5} = 17k\Omega \quad (4)$$

R1 should be greater than 17kΩ to provide an 8.5V buck V_{OUT} change (∆V). It is recommended to select R1 to be 44.2kΩ. Calculate R2 with Equation (5):

$$R2(k\Omega) = \frac{V_{FB} \times R1}{V_{BUCK} - V_{FB}} \quad (5)$$

For example, if V_{BUCK} = 3.5V, then R2 = 13kΩ.

When R1 and R2 have been determined, the ADJ current (I_{ADJ}) through R1 at 12V V_{OUT} can be calculated with Equation (6):

$$I_{ADJ}(\mu A) = \frac{\Delta V(mV)}{R_1(k\Omega)} = \frac{8500}{44.2} = 192\mu A \quad (6)$$

The maximum value of the ADJ resistor (R12) can be calculated with Equation (7):

$$R12(k\Omega) < \frac{V_{FB} - V_{ADJ\_OFFSET}(V)}{I_{ADJ}} = \frac{0.792-0.1}{0.192} = 3.6k\Omega \quad (7)$$

RT + R1 is used to set the loop bandwidth. The higher the value of RT + R1, the lower the bandwidth. To ensure the loop stability, it is recommended to limit the bandwidth to below 40kHz, based on the 420kHz default f_{SW}. For R1 = 44.2kΩ, RT can be ≥20kΩ.

Selecting the Inductor

For most applications, it is recommended to use an inductor with a DC current rating at least 25% above the maximum load current. Select an inductor with a small DC resistance for optimum efficiency. Calculate the inductance (L_1) with Equation (8):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (8)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current approximately 30% to 50% of the maximum load current. The maximum inductor peak current can be calculated with Equation (9):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (9)$$

Selecting Buck Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current while maintaining the DC input voltage. Use low-ESR capacitors for optimum performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For automotive applications, a 100µF electrolytic capacitor and two 4.7µF ceramic capacitors are recommended.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple-current rating. The input capacitor's RMS current (I_{C1}) can be estimated with Equation (10):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (10)$$

The worst-case condition occurs at $V_{IN} = 2 \times V_{OUT}$, calculated with Equation (11):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (11)$$

For simplification, choose an input capacitor with a RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using an electrolytic capacitor, place two additional, high-quality ceramic capacitors as close to IN as possible.

Estimate the input voltage ripple (ΔV_{IN}) caused by the capacitance with Equation (12):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (12)$$

Selecting the Buck Output Capacitor

The device requires an output capacitor (C2) to maintain the DC output voltage. Estimate the output voltage ripple (V_{OUT}) with Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (13)$$

Where L_1 is the inductance, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For an electrolytic capacitor, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (14):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (14)$$

The characteristics of the output capacitor affect the stability of the regulation system.

For applications, it is recommended to use a 100μF electrolytic capacitor with low ESR and a 10μF ceramic capacitor.

Setting V_{IN} Under-Voltage Lockout (UVLO)

The MPQ4228-Q has an internal, fixed under-voltage lockout (UVLO) threshold. The rising threshold is 3.7V, while the falling threshold is about 3.25V. If the application requires a higher UVLO point, the external resistor divider between EN/SYNC and IN can be used to achieve a higher equivalent UVLO threshold (see Figure 14).

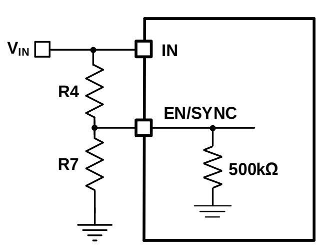


Figure 14: Adjustable UVLO Using the EN/SYNC Divider

The UVLO rising and falling thresholds can be calculated with Equation (15) and Equation (16), respectively:

$$V_{IN\_UVLO\_RISING} = \left(1 + \frac{R4}{500k\Omega // R7}\right) \times V_{EN\_RISING} \quad (15)$$

$$V_{IN\_UVLO\_FALLING} = \left(1 + \frac{R4}{500k\Omega // R7}\right) \times V_{EN\_FALLING} \quad (16)$$

Where V_{EN_RISING} is 1.4V, and $V_{EN\_FALLING}$ is 1.25V.

When selecting R4, ensure that it is large enough to limit the current flowing into EN/SYNC to below 100μA.

Enhanced ESD Protection for I/O Pins

High ESD levels should be considered for all USB I/O pins. The CC1 and CC2 pins satisfy the ±8kV IEC 61000-4-2 contact discharge ESD rating, and the ±15kV IEC 61000-4-2 air discharge ESD rating. The DP and DM pins can be configured to pass the ±8kV IEC 61000-4-2 contact discharge ESD rating and the ±15kV IEC 61000-4-2 air discharge ESD rating with a small resistor and capacitor (see Figure 15). The resistor must be at least 0603 in size, otherwise it might be damaged in ESD test.

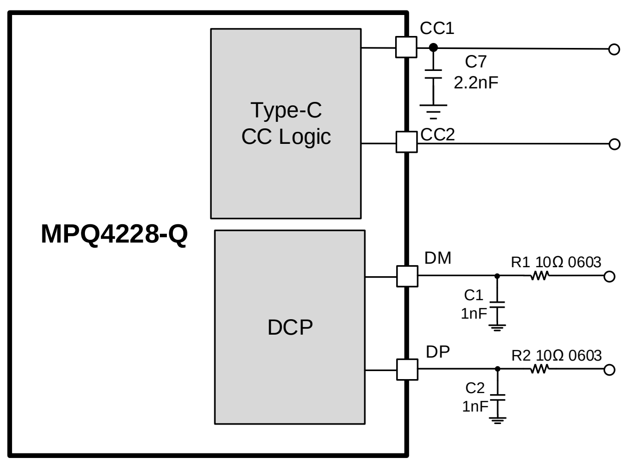


Figure 15: Recommended I/O Pins for Enhanced ESD

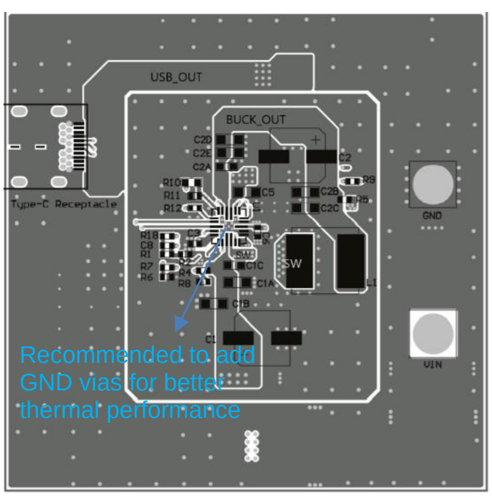
PCB Layout Guidelines (9)

Efficient PCB layout is critical for standard operation and thermal dissipation. A 4-layer PCB layout is recommended to achieve good thermal performance. For the best results, refer to Figure 16 and follow the guidelines below:

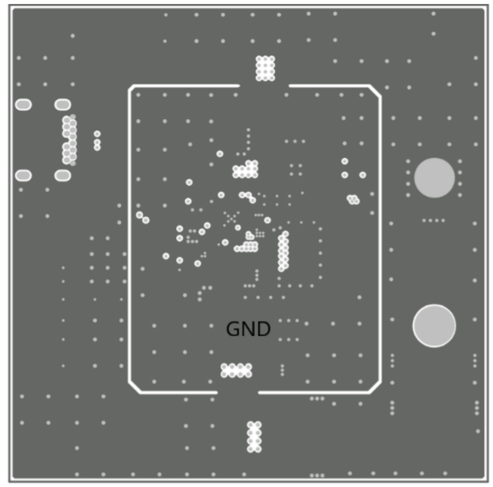
1. Place ceramic input capacitors as close to IN and GND as possible, especially the small package size (0603) input bypass capacitor.
2. Keep the connection between the input capacitor and IN as short and wide as possible.
3. Place the VCC1/2 capacitor as close to VCC1/2 and GND as possible.
4. Make the trace length from VCC1/2 to the capacitor to GND as short as possible. Use a large ground plane connected directly to GND.
5. If the bottom layer is a ground plane, add vias near GND.
6. Route SW and BST away from sensitive analog areas, such as FB.
7. Place the T-type feedback resistor close to the chip to ensure that the trace connected to FB is as short as possible.
8. Ensure that the SW area is small to reduce EMC radiated noise.

Notes:

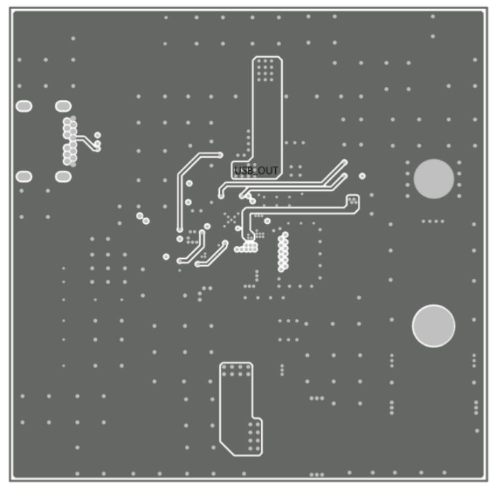
9) The recommended layout is based on the Typical Application Circuit (see Figure 17 on page 30).



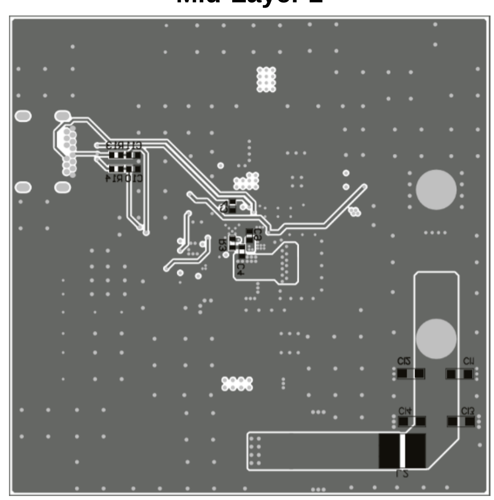
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 16: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

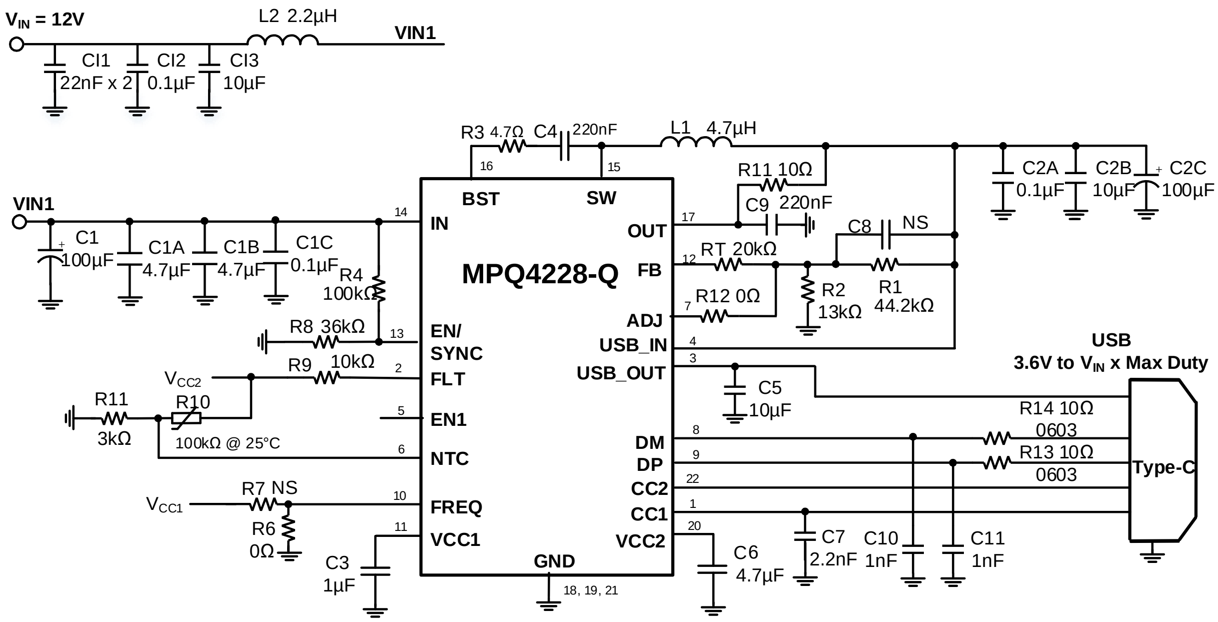


Figure 17: Typical Application Circuit (V_{IN} = 12V, USB Type-C 5V @ 3A DFP and QC3.0 Mode)

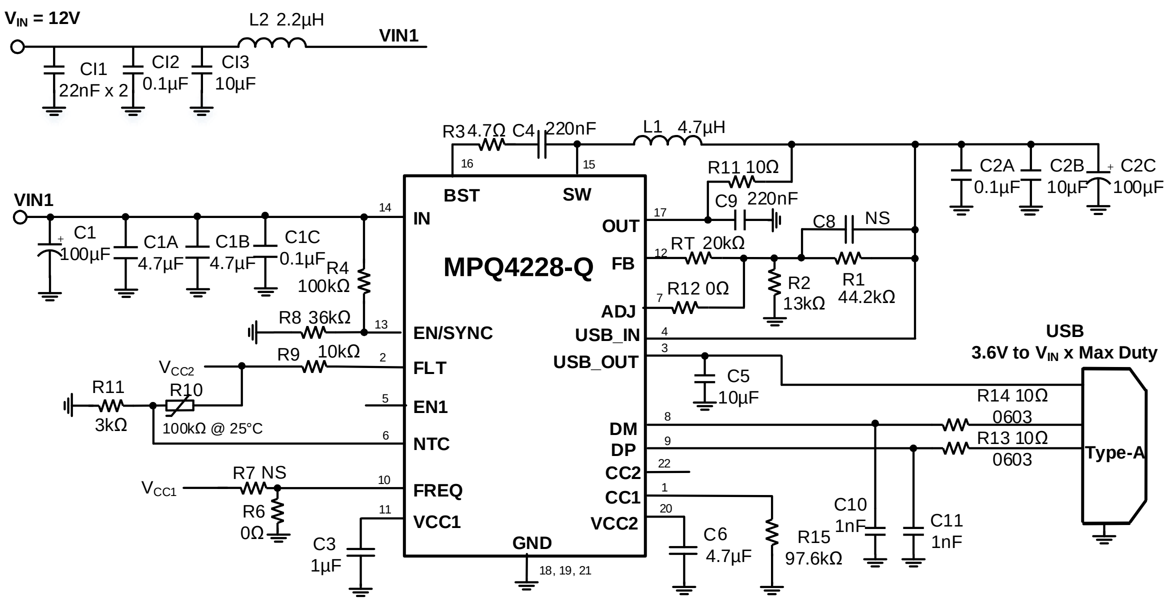
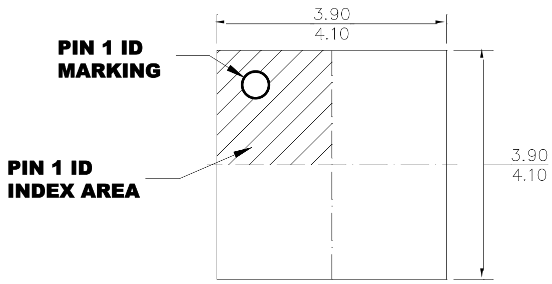


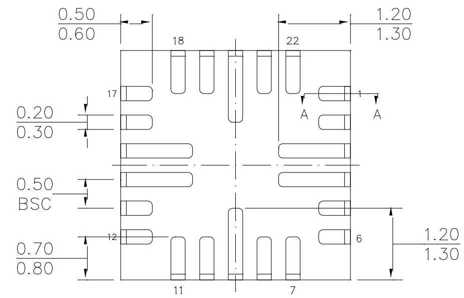
Figure 18: Typical Application Circuit (V_{IN} = 12V, USB Type-A Port and QC3.0 Mode)

PACKAGE INFORMATION

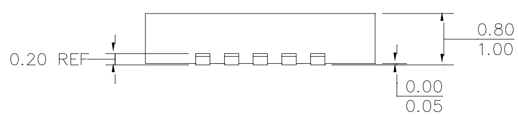
QFN-22 (4mmx4mm)



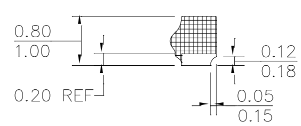
TOP VIEW



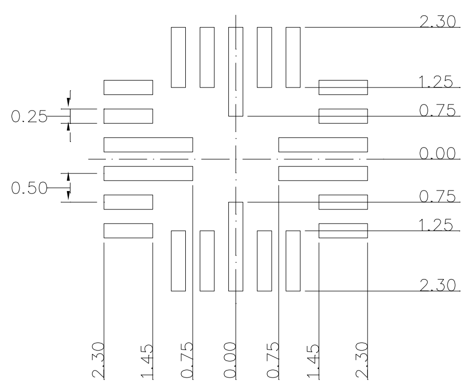
BOTTOM VIEW



SIDE VIEW



SECTION A-A

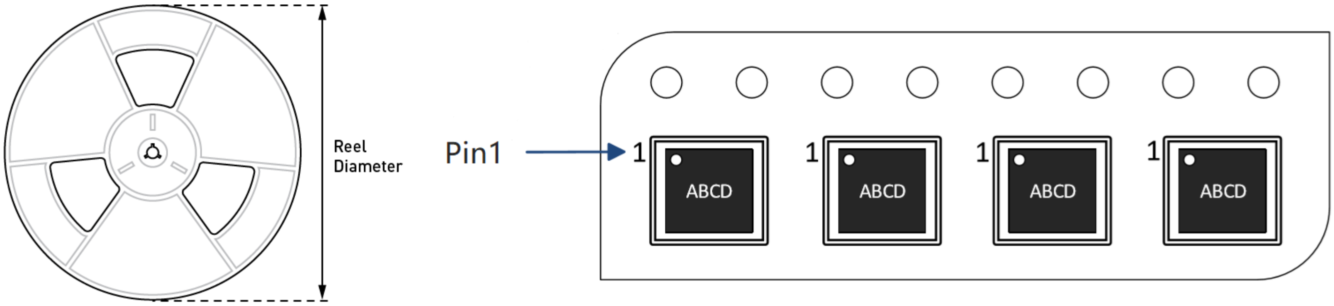


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity /Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4228GRE-Q-AEC1-Z	QFN-22 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm