



# MPQ4272

## 36V, 3A Dual Buck Converters with I<sup>2</sup>C Interface for Automotive Power Delivery, AEC-Q100

### DESCRIPTION

The MPQ4272 integrates dual-channel, monolithic step-down converters with an I<sup>2</sup>C interface. Each channel can deliver up to 3A of output current across a wide input supply range, with excellent load and line regulation.

The MPQ4272 is designed for USB charger applications with dual ports. Both channels can work with an external USB power deliver (PD) controller.

The I<sup>2</sup>C interface and one-time programmable (OTP) memory provide flexibility with configurable features.

Fault condition protections include current limiting, output over-voltage protection (OVP), and thermal shutdown (TSD).

The MPQ4272 requires a minimal number of readily available, standard external components. It is available in a QFN-21 (4mmx5mm) package.

### FEATURES

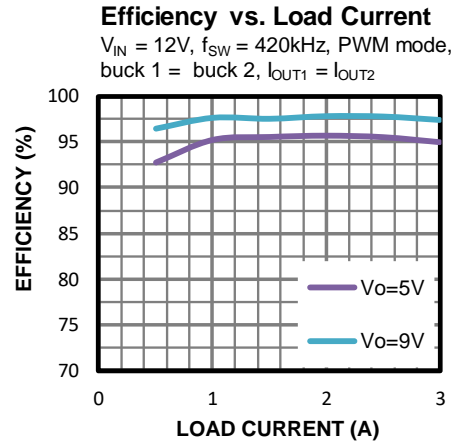
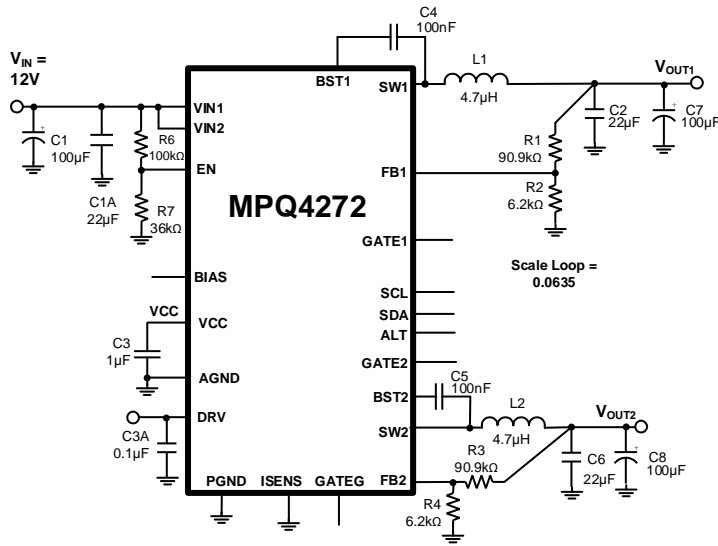
- Dual 3A or Shared 6A Buck Converter
- Supports USB PD 3.0
- Wide 4V to 36V Operating Input Voltage Range
- 1V to 21V Output Voltage Range with 12.6mV Resolution, V<sub>OUT</sub> Scale Loop = 0.0635
- Selectable 250kHz, 420kHz, 1.1MHz, or 2.1MHz Switching Frequency
- Frequency Spread Spectrum
- Low-Dropout Mode
- Line Drop Compensation
- Accurate Adjustable CC Output Current Limit (50mA/Step via the I<sup>2</sup>C)
- 22mΩ High-Side and 26mΩ Low-Side Low R<sub>DS(ON)</sub> Internal Buck Power MOSFETs
- I<sup>2</sup>C Interface and Over-Temperature Protection (OTP) with PMBus-Compatible Parameters:
  - PFM/PWM Mode, Current Limit, Output Voltage, Frequency Spread Spectrum, Phase Delay, and Line Drop Compensation
- V<sub>BUS</sub> Isolation N-Channel MOSFET Gate Driver
- Battery Short-to-Ground Protection
- Load-Shedding Alert
- EN Shutdown Active Discharge
- Available in a QFN-21 (4mmx5mm) Package with Wettable Flanks
- Available in AEC-Q100 Grade 1

### APPLICATIONS

- USB Power Delivery
- USB-Dedicated Charging Ports (DCP)
- Automotive DC/DC Supplies

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## TYPICAL APPLICATION



## ORDERING INFORMATION

| Part Number**         | Package          | Top Marking      | MSL Rating |
|-----------------------|------------------|------------------|------------|
| MPQ4272GVE-0000-AEC1* | QFN-21 (4mmx5mm) | <i>See Below</i> | 1          |
| MPQ4272GVE-0001-AEC1* |                  |                  |            |
| MPQ4272GVE-0011-AEC1* |                  |                  |            |
| MPQ4272GVE-xxxx-AEC1* |                  |                  |            |

\* For Tape & Reel, add suffix -Z (e.g. MPQ4272GVE-xxxx-AEC1-Z).

\*\* “xxxx” is the configuration code identifier for the register setting stored in the OTP. Each “x” can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number, even if ordering the “0000” code. MPQ4272GVE-0000 is the default version.

## TOP MARKING

**MPSYWW**  
**MP4272**  
**LLLLLL**  
**E**

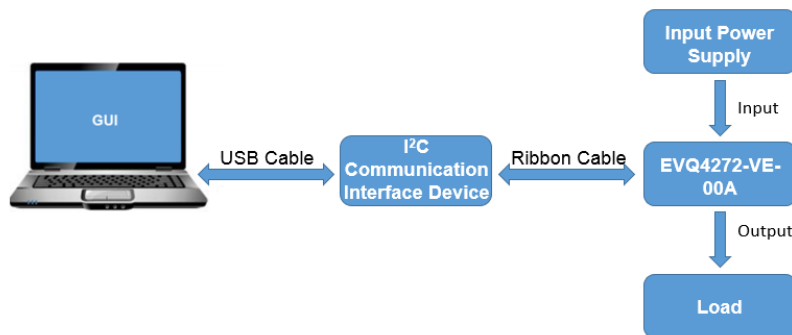
MPS: MPS prefix  
 Y: Year code  
 WW: Week code  
 MP4272: Part number  
 LLLLLL: Lot number  
 E: Wettable flank

## EVALUATION KIT EVKT-MPQ4272

EVKT-MPQ4272 kit contents (items below can be ordered separately):

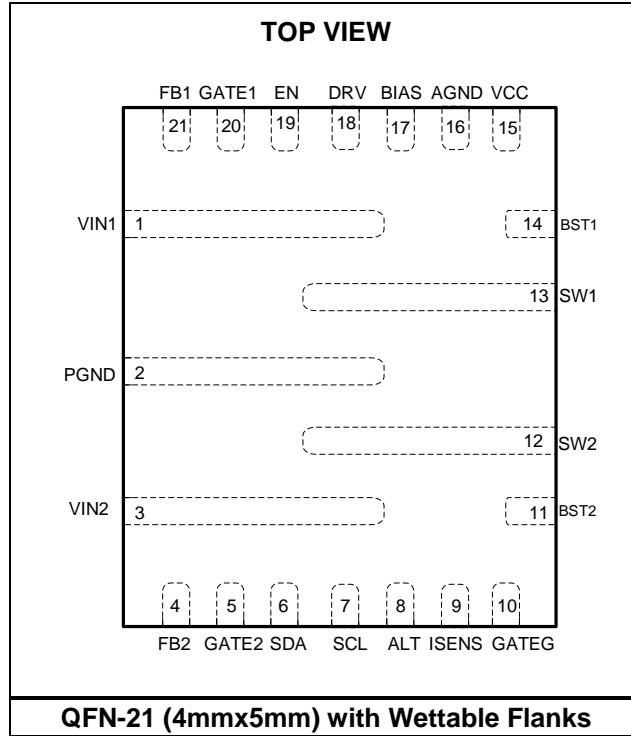
| # | Part Number          | Item  | Quantity |
|---|----------------------|---|----------|
| 1 | EVQ4272-VE-00A       | MPQ4272 evaluation board  | 1        |
| 2 | EVKT-USBI2C-02 bag   | Includes USB to I <sup>2</sup> C communication interface, one USB cable, and one ribbon cable | 1        |
| 3 | MPQ4272GVE-0000-AEC1 | IC with default configuration   | 2        |

**Order directly from [MonolithicPower.com](http://MonolithicPower.com) or our distributors.**



**Figure 1: EVKT-MPQ4272 Evaluation Kit Set-Up**

### PACKAGE REFERENCE



## PIN FUNCTIONS

| Pin # | Name  | Description   |
|-------|-------|---|
| 1     | VIN1  | <b>Supply voltage.</b> The MPQ4272 operates from a 4V to 36V input voltage. An input capacitor (C <sub>IN</sub> ) prevents large voltage spikes at the input. Place C <sub>IN</sub> as close to the IC as possible. VIN1 is the drain for channel 1's internal power device. VIN1 also provides the power supply for the entire chip. VIN1 and VIN2 should be connected together. |
| 2     | PGND  | <b>Power ground.</b> Reference ground of the first channel. PGND requires special considerations when designing the PCB layout. Connect PGND to GND with copper traces and vias.  |
| 3     | VIN2  | <b>Supply voltage.</b> The MPQ4272 operates from a 4V to 36V input voltage. C <sub>IN</sub> prevents large voltage spikes at the input. Place C <sub>IN</sub> as close to the IC as possible. VIN2 is the drain for channel 2's internal power device. VIN1 and VIN2 should be connected together.  |
| 4     | FB2   | <b>Feedback pin for buck 2.</b>   |
| 5     | GATE2 | <b>Gate driver.</b> Gate driver to turn on the isolation N-channel MOSFET on the V <sub>BUS</sub> line.   |
| 6     | SDA   | <b>I<sup>2</sup>C data line.</b>  |
| 7     | SCL   | <b>I<sup>2</sup>C clock signal input.</b>   |
| 8     | ALT   | <b>PMBus alert pin.</b> Open-drain output. Active low.  |
| 9     | ISENS | <b>Second current limit sense pin.</b>  |
| 10    | GATEG | <b>Gate drive pin to drive the external MOSFET.</b> The external MOSFET is used for ground short-to-battery protection.   |
| 11    | BST2  | <b>Bootstrap 2.</b> Connect a 0.1μF capacitor between the SW2 and BST2 pins to form a floating supply across the high-side switch driver.   |
| 12    | SW2   | <b>Switch 2 output.</b> Use a wide PCB trace to connect SW2 to the pad.   |
| 13    | SW1   | <b>Switch 1 output.</b> Use a wide PCB trace to connect SW1 to the pad.   |
| 14    | BST1  | <b>Bootstrap 1.</b> Connect a 0.1μF capacitor between the SW1 and BST1 pins to form a floating supply across the high-side switch driver.   |
| 15    | VCC   | <b>Internal 5V LDO regulator output.</b> Decouple VCC with a 1μF capacitor.   |
| 16    | AGND  | <b>Analog ground.</b> Connect AGND to PGND. AGND should also be connected to the VCC capacitor's ground node.   |
| 17    | BIAS  | <b>Bias input pin of internal VCC LDO.</b> Connect the BIAS pin to a 5V or 9V V <sub>OUT</sub> to improve system efficiency. Add an RC low-pass filter from output to the BIAS pin.   |
| 18    | DRV   | <b>LDO output.</b> 1mA load capability. The output voltage can be set by the I <sup>2</sup> C. Decouple DRV with a 0.1μF capacitor.   |
| 19    | EN    | <b>Enable control pin.</b> Apply a logic high voltage on this pin to enable the IC. Pull EN to logic low to disable the IC. The EN pin has an internal pull-down resistor.  |
| 20    | GATE1 | <b>Gate driver.</b> Gate driver to turn on the isolation N-channel MOSFET on the V <sub>BUS</sub> line.   |
| 21    | FB1   | <b>Feedback pin for buck 1.</b>   |

**ABSOLUTE MAXIMUM RATINGS** <sup>(1)</sup>

|  |   |
|--|---|
| Supply voltage ( $V_{IN1/2}$ )   | 40V                                     |
| $V_{SW1/2}$  | -0.3V (-5V for <10ns)                   |
|  | .....to $V_{IN} + 0.3V$ (43V for <10ns) |
| $V_{BST1/2}$   | $V_{SW1/2} + 5.5V$                      |
| $V_{BIAS}$ , $V_{GATE1/2}$ , $V_{ISENS}$                               | -0.3V to +30V                           |
| $V_{EN}$   | -0.3V to +10V <sup>(2)</sup>            |
| All other pins   | -0.3V to +5.5V                          |
| Continuous power dissipation ( $T_A = 25^\circ C$ ) <sup>(3) (6)</sup> |   |
| QFN-21 (4mmx5mm)   | 5.08W                                   |
| Junction temperature   | 150°C                                   |
| Lead temperature   | 260°C                                   |
| Storage temperature  | -65°C to +150°C                         |

**ESD Ratings** <sup>(4)</sup>

|                            |       |
|----------------------------|-------|
| Human body model (HBM)     | 2000V |
| Charged device model (CDM) | 750V  |

**Recommended Operating Conditions** <sup>(5)</sup>

|                                   |                                    |
|-----------------------------------|------------------------------------|
| Operation input voltage range     | 4V to 36V                          |
| Operation output voltage range    | .....                              |
|                                   | .....1V to $V_{IN} \times D_{MAX}$ |
| Output current                    | 3A for each channel                |
| Operating junction temp ( $T_J$ ) | -40°C to +150°C                    |

**Thermal Resistance**       $\theta_{JA}$        $\theta_{JC}$ 

|                                 |      |     |      |
|---------------------------------|------|-----|------|
| EVQ4272-VE-00A <sup>(6)</sup>   | 24.6 | 6.3 | °C/W |
| QFN-21 (4mmx5mm) <sup>(7)</sup> | 44   | 9   | °C/W |

**Notes:**

- 1) Exceeding these ratings may damage the device.
- 2) For details on the EN pin's absolute maximum rating, see the Enable (EN) Control section on page 17.
- 3) The maximum allowable power dissipation is a function of the maximum junction temperature,  $T_J$  (MAX), the junction-to-ambient thermal resistance,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 4) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101, AEC specification AEC-Q100-011. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. HBM with regard to GND.
- 5) The device is not guaranteed to function outside of its operating conditions. The PMBus  $V_{OUT}$  command does not support voltages exceeding 21V. If  $V_{OUT}$  must exceed 21V, a feedback resistor is required.
- 6) Measured on EVQ4272-VE-00A, 4-layer PCB, 55mmx55mm.
- 7) Measured on JESD51-7, 4-layer PCB. The value of  $\theta_{JA}$  given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

## ELECTRICAL CHARACTERISTICS

V<sub>IN</sub> = 12V, V<sub>EN</sub> = 5V, T<sub>J</sub> = -40°C to +125°C, typical value is tested at T<sub>J</sub> = 25°C, unless otherwise noted.

| Parameter   | Symbol                 | Condition   | Min   | Typ   | Max   | Units |
|---|------------------------|---|-------|-------|-------|-------|
| Shutdown supply current                                       | I <sub>Q_STD</sub>     | V <sub>EN</sub> = 0V, T <sub>J</sub> = 25°C                                   |       | 0.5   | 5     | μA    |
|   |                        | T <sub>J</sub> = -40°C to +125°C  |       | 0.5   | 30    | μA    |
| Quiescent supply current                                      | I <sub>Q</sub>         | No switching, both channels enabled   |       | 0.3   |       | mA    |
| EN rising threshold   | V <sub>EN_RISING</sub> |   | -5%   | 1.6   | +5%   | V     |
| EN hysteresis   | V <sub>EN_HYS</sub>    |   |       | 200   |       | mV    |
| EN pull-down resistor   | R <sub>EN</sub>        | V <sub>EN</sub> = 2V  |       | 2     |       | MΩ    |
| Thermal shutdown <sup>(8)</sup>                               | T <sub>STD</sub>       | OTP = 011b  |       | 170   |       | °C    |
| Thermal hysteresis <sup>(8)</sup>                             | T <sub>STD_HYS</sub>   |   |       | 20    |       | °C    |
| VCC regulator   | V <sub>CC</sub>        | I <sub>CC</sub> = 0mA to 50mA, T <sub>J</sub> = -40°C to +125°C               | 4.5   | 5.0   | 5.25  | V     |
| <b>Step-Down Converters (Ch1 and Ch2)</b>                     |                        |   |       |       |       |       |
| V <sub>IN</sub> under-voltage lockout (UVLO) rising threshold | V <sub>IN_UVLO</sub>   | Monitor VIN1 only   | 3.2   | 3.35  | 3.5   | V     |
| V <sub>IN</sub> UVLO threshold hysteresis                     | V <sub>UVLO_HYS</sub>  |   |       | 300   |       | mV    |
| HS-FET on resistance  | R <sub>DS(ON)_HS</sub> |   |       | 22    |       | mΩ    |
| LS-FET on resistance  | R <sub>DS(ON)_LS</sub> |   |       | 26    |       | mΩ    |
| FB reference voltage  | V <sub>FB0</sub>       | Set V <sub>OUT</sub> = 1.25V  | 0.092 | 0.1   | 0.108 | V     |
|   | V <sub>FB1</sub>       | Default, V <sub>OUT</sub> = 5V  | -2%   | 0.400 | +2%   | V     |
|   | V <sub>FB2</sub>       | Set V <sub>OUT</sub> = 9V   | -1.5% | 0.720 | +1.5% | V     |
|   | V <sub>FB3</sub>       | Set V <sub>OUT</sub> = 20V  | -1.5% | 1.600 | +1.5% | V     |
| Output over-voltage protection (OVP)                          | V <sub>OVP_F</sub>     |   | 114   | 120   | 125   | %     |
| Output OVP recovery   | V <sub>OVP_R</sub>     |   | 104   | 109   | 114   | %     |
| High-side current limit                                       | I <sub>HS_PEAK</sub>   |   |       | 13    |       | A     |
| Valley current limit  |                        | Falling edge  |       | 8     |       | A     |
| Low-side current limit  | I <sub>LS_SINK</sub>   |   |       | -3.6  | -2    | A     |
| Switch leakage  | SW <sub>LKG</sub>      | V <sub>EN</sub> = 0V, V <sub>SW</sub> = 36V, T <sub>J</sub> = 25°C            |       |       | 1     | μA    |
|   |                        | V <sub>EN</sub> = 0V, V <sub>SW</sub> = 36V, T <sub>J</sub> = -40°C to +150°C |       |       | 30    |       |
| Output CC current limit                                       | I <sub>LIMIT</sub>     | I <sup>2</sup> C set 1, T <sub>J</sub> = 0°C to 85°C, 420kHz                  | -5%   | 3.6   | +5%   | A     |
| Oscillator frequency  | f <sub>SW1</sub>       | I <sup>2</sup> C set 1  | -20%  | 250   | +20%  | kHz   |
|   | f <sub>SW2</sub>       | I <sup>2</sup> C set 2 (default)  | -20%  | 420   | +20%  |       |
|   | f <sub>SW3</sub>       | I <sup>2</sup> C set 3  | -20%  | 1100  | +20%  |       |
|   | f <sub>SW4</sub>       | I <sup>2</sup> C set 4  | -20%  | 2100  | +20%  |       |

## ELECTRICAL CHARACTERISTICS (continued)

V<sub>IN</sub> = 12V, V<sub>EN</sub> = 5V, T<sub>J</sub> = -40°C to +125°C, typical value is tested at T<sub>J</sub> = 25°C, unless otherwise noted.

| Parameter  | Symbol               | Condition  | Min  | Typ  | Max  | Units |
|--|----------------------|--|------|------|------|-------|
| Frequency dithering  |                      |  |      | ±12  |      | %     |
| Maximum duty cycle <sup>(8)</sup>                                | D <sub>MAX1</sub>    | FREQ = 420kHz  |      | 95   |      | %     |
|  | D <sub>MAX2</sub>    | In dropout mode  |      | 99   |      | %     |
| Minimum off time <sup>(8)</sup>                                  | t <sub>OFF_MIN</sub> |  |      | 100  |      | ns    |
| Minimum on time <sup>(8)</sup>                                   | t <sub>ON_MIN</sub>  |  |      | 80   |      | ns    |
| Soft-start time  | t <sub>SS</sub>      | Output from 10% to 90%, V <sub>OUT</sub> = 5V, constant slew rate for other V <sub>OUT</sub> |      | 0.8  |      | ms    |
| <b>Second Current Limit Sense</b>                                |                      |  |      |      |      |       |
| ISENS rising threshold   | I <sub>SENS_R</sub>  | The buck is disabled once triggered, gate 1 and gate 2 are off                               | 130  | 160  | 190  | mV    |
| ISENS falling threshold  | I <sub>SENS_F</sub>  |  | 70   | 100  | 130  | mV    |
| ISENS deglitch time <sup>(8)</sup>                               | t <sub>SENS</sub>    | Release edge   |      | 20   |      | µs    |
| ISENS pull-down current  | I <sub>SENS1</sub>   | V <sub>ISENS</sub> = 12V   |      | 17   |      | mA    |
|  | I <sub>SENS2</sub>   | V <sub>ISENS</sub> = 80mV  |      | 2.5  |      | mA    |
| GATEG pull-down resistance                                       | R <sub>GATEG</sub>   |  |      | 12   | 25   | Ω     |
| <b>GATE1, GATE2</b>  |                      |  |      |      |      |       |
| Output voltage   | V <sub>GATE1_2</sub> | V <sub>IN</sub> = 12V, V <sub>CC</sub> = 5V  | 16   | 17   | 18   | V     |
| Source current   | I <sub>GATE1_2</sub> |  | -30% | 21.5 | +30% | µA    |
| DRV voltage  | V <sub>DRV</sub>     |  | 5.7  | 5.95 | 6.2  | V     |
|  |                      | Load = 1mA   | 5.45 | 5.82 | 5.95 | V     |
| <b>I<sup>2</sup>C Interface Specifications (High-Speed Mode)</b> |                      |  |      |      |      |       |
| Alert pull-low resistance  |                      |  |      | 10   | 25   | Ω     |
| Alert leakage  |                      | Pull-up with 5V  |      |      | 1    | µA    |
| Input logic high   | V <sub>IH</sub>      | I <sup>2</sup> C pulled up to VDD (1.8V to 5V)   | 1.4  |      |      | V     |
| Input logic low  | V <sub>IL</sub>      |  |      |      | 0.45 | V     |
| Output voltage logic low   | V <sub>OUT_L</sub>   |  |      |      | 0.4  | V     |
| SCL clock frequency  | f <sub>SCL</sub>     |  |      | 400  |      | kHz   |
| SCL high time  | t <sub>HIGH</sub>    |  | 60   |      |      | ns    |



**ELECTRICAL CHARACTERISTICS (continued)**

$V_{IN} = 12V$ ,  $V_{EN} = 5V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , typical value is tested at  $T_J = 25^{\circ}C$ , unless otherwise noted.

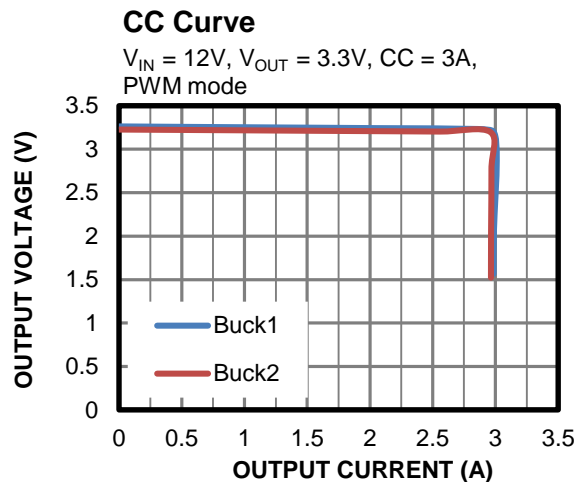
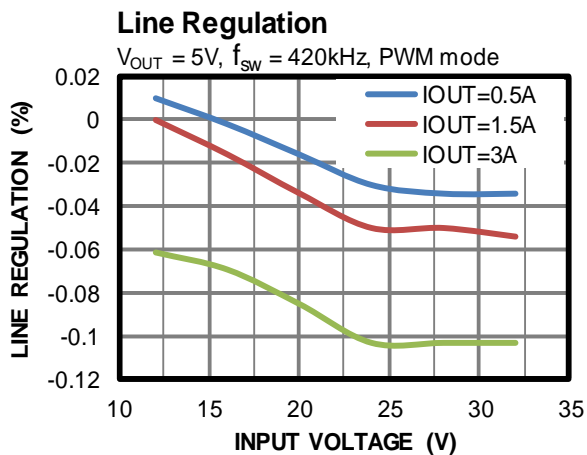
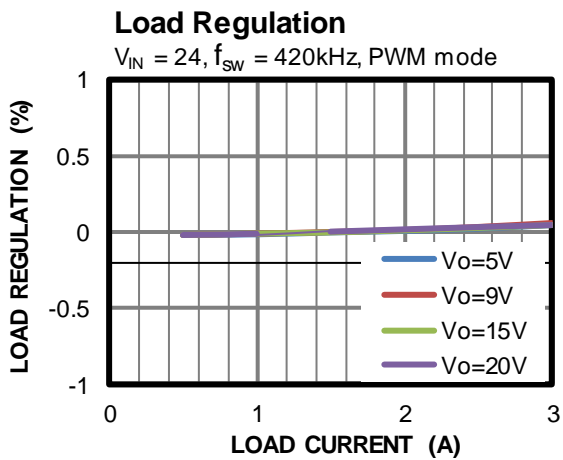
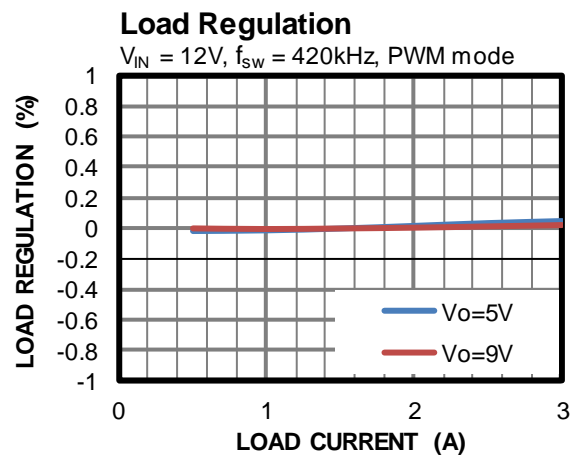
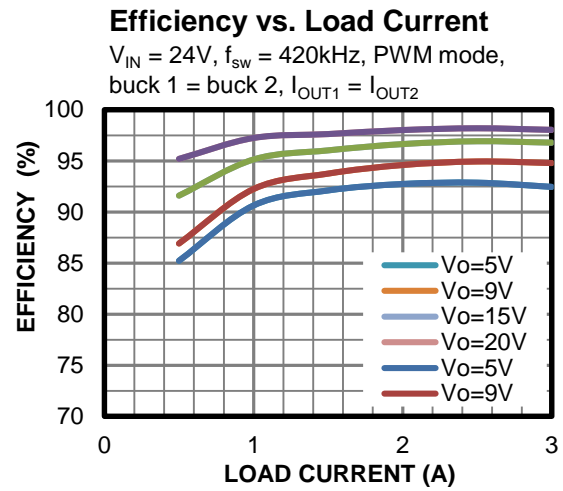
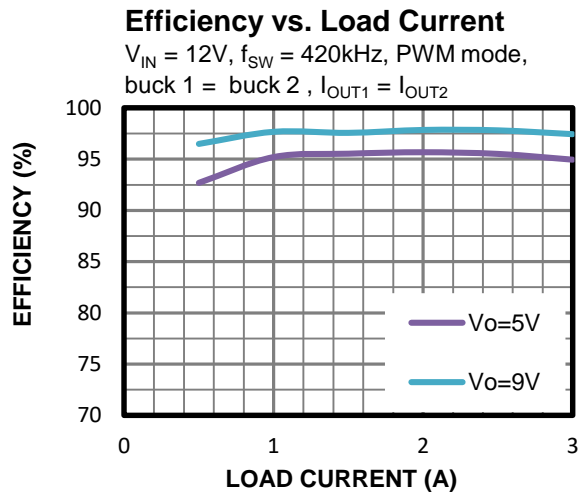
| Parameter  | Symbol        | Condition | Min | Typ | Max | Units |
|--|---------------|-----------|-----|-----|-----|-------|
| SCL low time                                     | $t_{LOW}$     |           | 160 |     |     | ns    |
| Data set-up time                                 | $t_{SU\_DAT}$ |           | 10  |     |     | ns    |
| Data hold time                                   | $t_{HD\_DAT}$ |           |     | 60  |     | ns    |
| Set-up time for repeated start condition         | $t_{SU\_STA}$ |           | 160 |     |     | ns    |
| Hold time for repeated start condition           | $t_{HD\_STA}$ |           | 160 |     |     | ns    |
| Bus free time between a start and stop condition | $t_{BUF}$     |           | 160 |     |     | ns    |
| Set-up time for stop condition                   | $t_{SU\_STO}$ |           | 160 |     |     | ns    |
| SCL and SDA rise time                            | $t_R$         |           | 10  |     | 300 | ns    |
| SCL and SDA fall time                            | $t_F$         |           | 10  |     | 300 | ns    |
| Pulse width of suppressed spike                  | $t_{SP}$      |           | 0   |     | 50  | ns    |
| Capacitance for each bus line                    | $C_B$         |           |     |     | 400 | pF    |

**Note:**

8) Guaranteed by characterization testing.

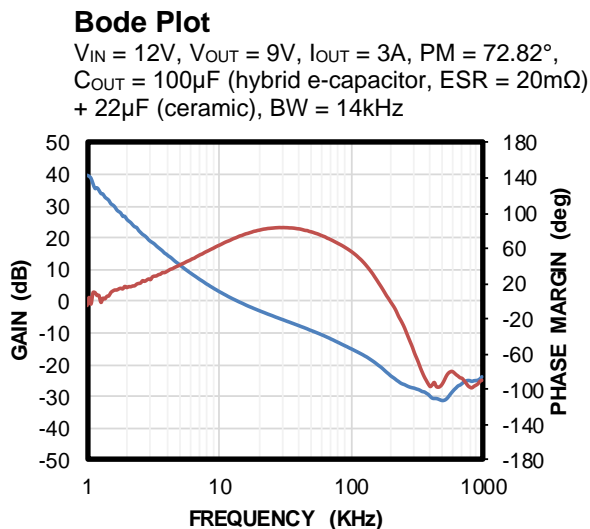
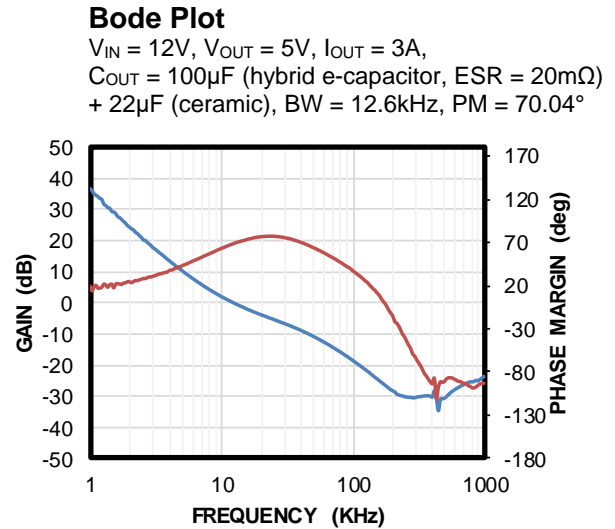
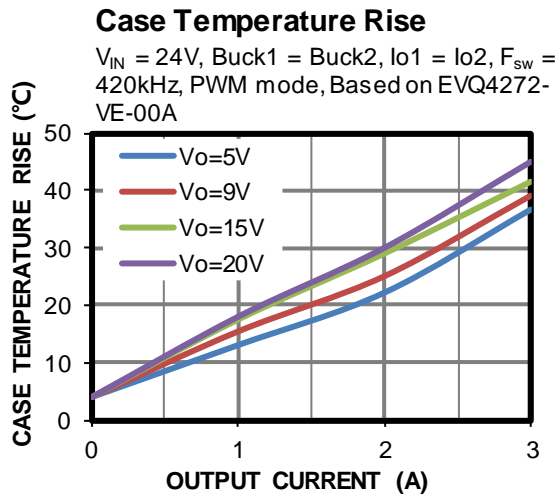
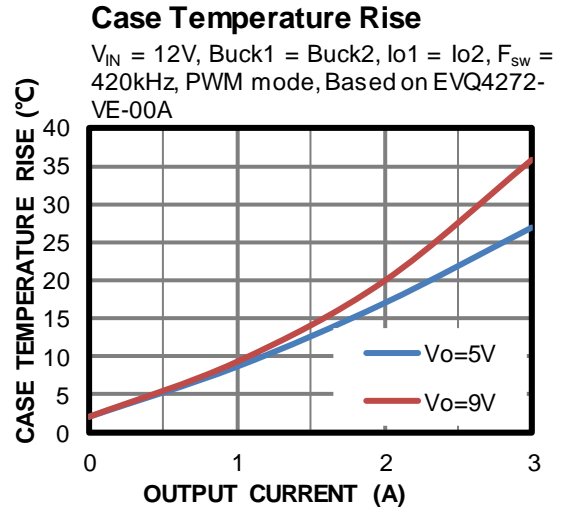
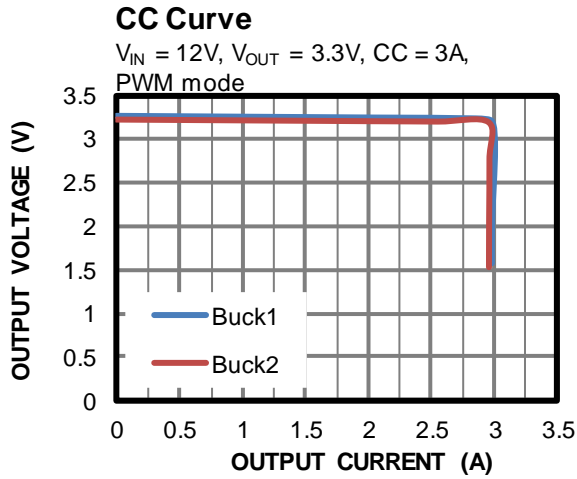
## TYPICAL CHARACTERISTICS

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 4.7\mu H$ ,  $f_{SW} = 420kHz$ , forced PWM mode,  $T_A = 25^\circ C$ , unless otherwise noted.



## TYPICAL CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 4.7\mu H$ ,  $f_{sw} = 420kHz$ , forced PWM mode,  $T_A = 25^\circ C$ , unless otherwise noted.

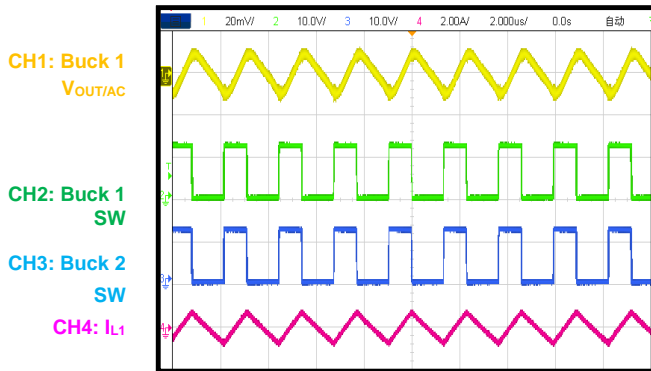


## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 4.7\mu H$ ,  $f_{SW} = 420kHz$ , forced PWM mode,  $T_A = 25^\circ C$ , unless otherwise noted.

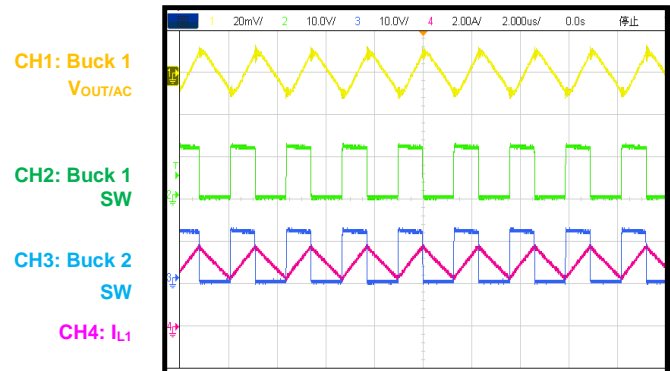
### Output Ripple

$V_{IN} = 12V$ , buck 1  $V_{OUT} =$  buck 2  $V_{OUT} = 5V$ ,  
 $I_{OUT1} = I_{OUT2} = 0A$ , PWM mode



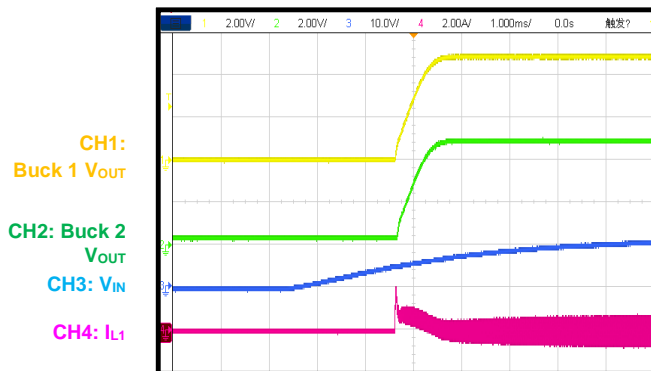
### Output Ripple

$V_{IN} = 12V$ , buck 1  $V_{OUT} =$  buck 2  $V_{OUT} = 5V$ ,  
 $I_{OUT1} = I_{OUT2} = 3A$ , PWM mode



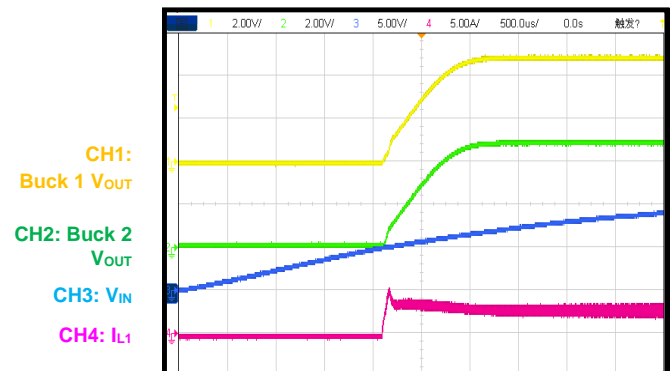
### Start-Up

$V_{IN} = 12V$ , buck 1  $V_{OUT} =$  buck 2  $V_{OUT} = 5V$ ,  
 $I_{OUT1} = I_{OUT2} = 0A$ , PWM mode



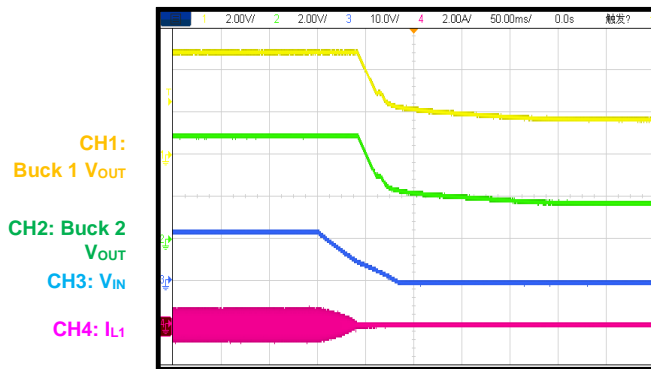
### Start-Up

$V_{IN} = 12V$ , buck 1  $V_{OUT} =$  buck 2  $V_{OUT} = 5V$ ,  
 $I_{OUT1} = I_{OUT2} = 3A$ , PWM mode



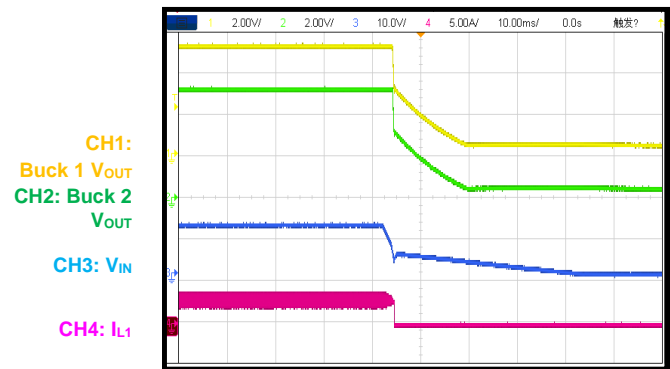
### Shutdown

$V_{IN} = 12V$ , buck 1  $V_{OUT} =$  buck 2  $V_{OUT} = 5V$ ,  
 $I_{OUT1} = I_{OUT2} = 0A$ , PWM mode



### Shutdown

$V_{IN} = 12V$ , buck 1  $V_{OUT} =$  buck 2  $V_{OUT} = 5V$ ,  
 $I_{OUT1} = I_{OUT2} = 3A$ , PWM mode

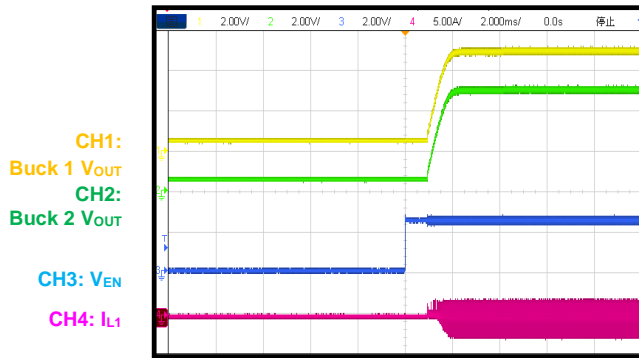


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 4.7\mu H$ ,  $f_{SW} = 420kHz$ , forced PWM mode,  $T_A = 25^\circ C$ , unless otherwise noted.

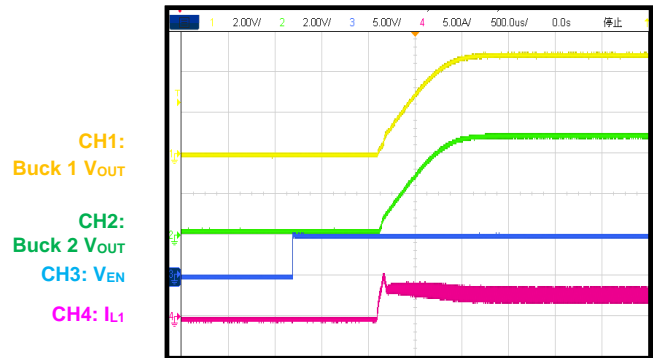
### Start-Up through EN

$V_{IN} = 12V$ , buck 1  $V_{OUT} =$  buck 2  $V_{OUT} = 5V$ ,  
 $I_{OUT1} = I_{OUT2} = 0A$ , PWM mode



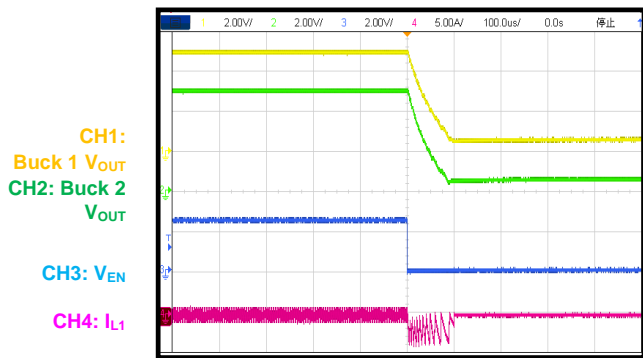
### Start-Up through EN

$V_{IN} = 12V$ , buck 1  $V_{OUT} =$  buck 2  $V_{OUT} = 5V$ ,  
 $I_{OUT1} = I_{OUT2} = 3A$ , PWM mode



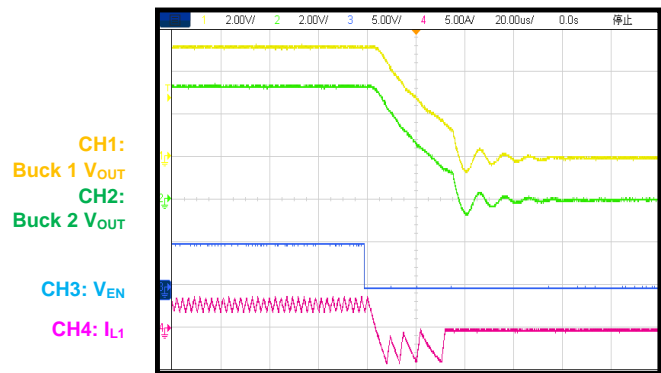
### Shutdown through EN

$V_{IN} = 12V$ , buck 1  $V_{OUT} =$  buck 2  $V_{OUT} = 5V$ ,  
 $I_{OUT1} = I_{OUT2} = 0A$ , PWM mode



### Shutdown through EN

$V_{IN} = 12V$ , buck 1  $V_{OUT} =$  buck 2  $V_{OUT} = 5V$ ,  
 $I_{OUT1} = I_{OUT2} = 3A$ , PWM mode



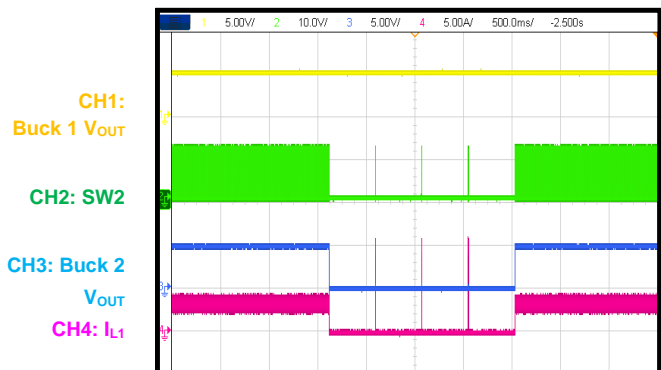
### Buck 1 $V_{OUT}$ Short-Circuit Protection Entry and Recovery

$V_{IN} = 12V$ , buck 1  $V_{OUT} = 5V$ ,  
buck 2  $V_{OUT} = 5V$ ,  $I_{OUT1} = I_{OUT2} = 3A$



### Buck 2 $V_{OUT}$ Short-Circuit Protection Entry and Recovery

$V_{IN} = 12V$ , buck 2  $V_{OUT} = 5V$ , buck 1  $V_{OUT} = 5V$ ,  
 $I_{OUT1} = I_{OUT2} = 3A$

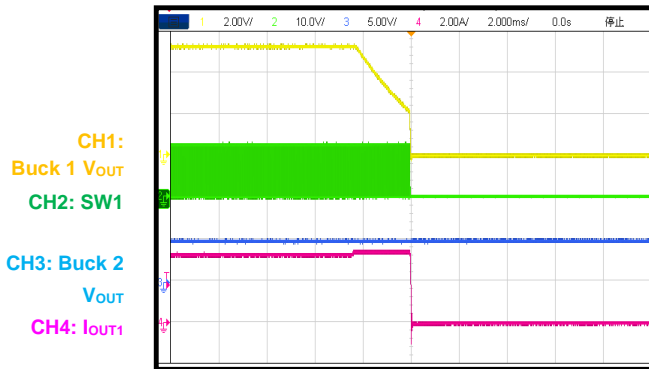


## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 4.7\mu H$ ,  $f_{SW} = 420kHz$ , forced PWM Mode,  $T_A = 25^\circ C$ , unless otherwise noted.

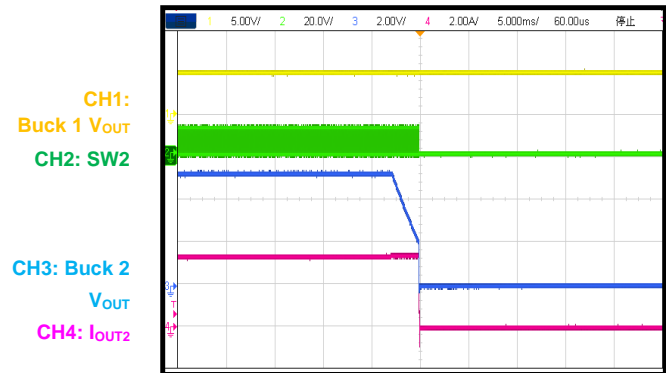
### Buck 1 $V_{OUT}$ OCP Test

$V_{IN} = 12V$ , buck 1  $V_{OUT} =$  buck 2  $V_{OUT} = 5V$ ,  
 $I_{OUT2} = 0A$ ,  $CL = 3.6A$ ,  $I_{OUT1}$  ramps up slowly



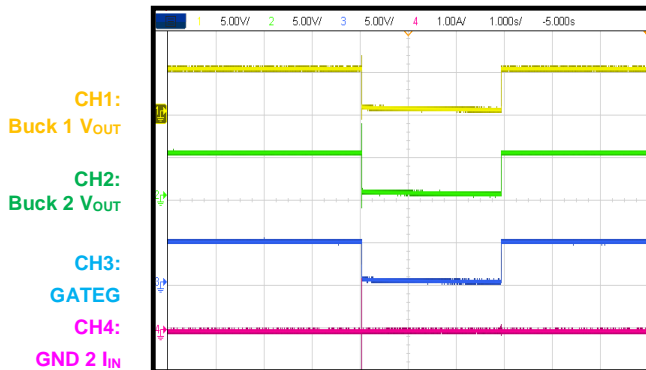
### Buck 2 $V_{OUT}$ OCP Test

$V_{IN} = 12V$ , buck 1  $V_{OUT} =$  buck 2  $V_{OUT} = 5V$ ,  
 $I_{OUT1} = 0A$ ,  $CL = 3.6A$ ,  $I_{OUT2}$  ramps up slowly



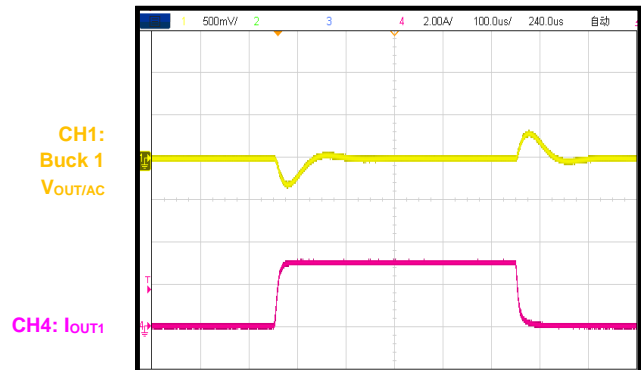
### GND2 Short-to-Battery Test

$V_{IN} = 12V$ , buck 1  $V_{OUT} =$  buck 2  $V_{OUT} = 5V$ ,  
 $I_{OUT1} = I_{OUT2} = 0A$



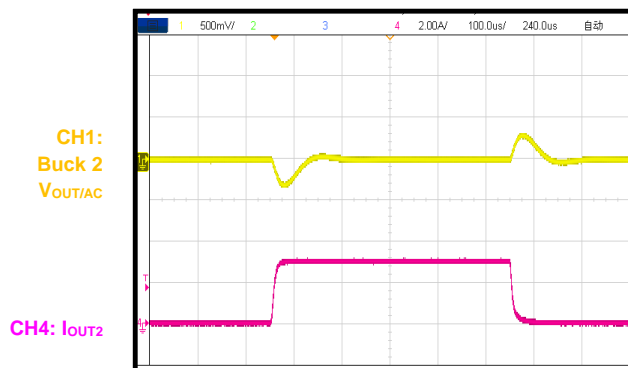
### Load Transient (Buck 1 $V_{OUT}$ )

$V_{IN} = 12V$ , buck 1  $V_{OUT} =$  buck 2  $V_{OUT} = 5V$ ,  
 $I_{OUT1} = 0A$  to  $3A$ , slew rate =  $2.5A/\mu s$



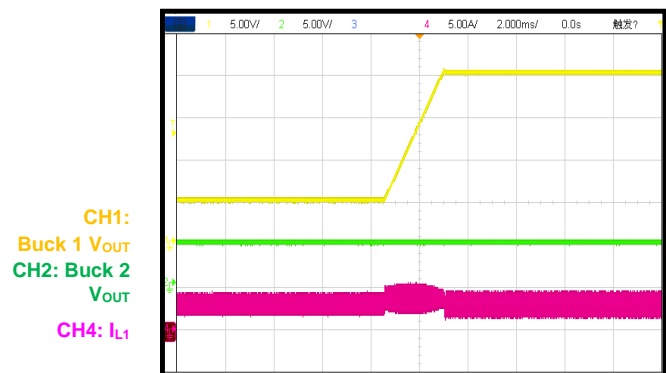
### Load Transient (Buck 2 $V_{OUT}$ )

$V_{IN} = 12V$ , buck 1  $V_{OUT} =$  buck 2  $V_{OUT} = 5V$ ,  
 $I_{OUT2} = 0A$  to  $3A$ , slew rate =  $2.5A/\mu s$



### Output Voltage Transition (Buck 1 $V_{OUT}$ Set via the I<sup>2</sup>C)

$V_{IN} = 24V$ , buck 2  $V_{OUT} = 5V$ ,  $I_{OUT1} = I_{OUT2} = 3A$ ,  
 buck 1  $V_{OUT} = 5V$  to  $20V$



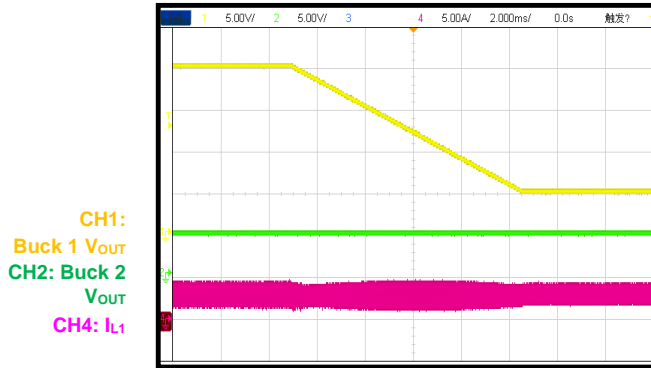
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 5V, L = 4.7μH, f<sub>sw</sub> = 420kHz, forced PWM mode, T<sub>A</sub> = 25°C, unless otherwise noted.

### Output Voltage Transition (Buck 1)

#### V<sub>OUT</sub> Set via the I<sup>2</sup>C

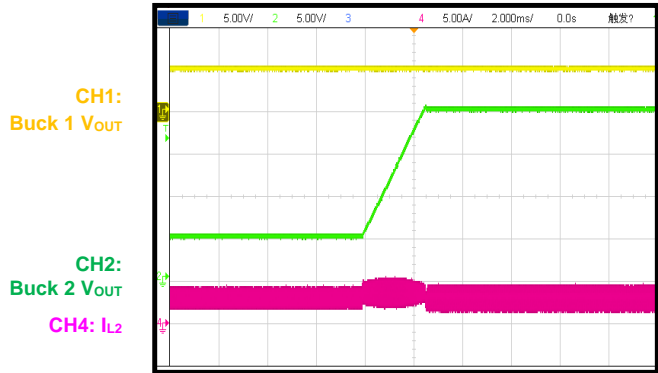
V<sub>IN</sub> = 24V, buck 2 V<sub>OUT</sub> = 5V,  
I<sub>OUT1</sub> = I<sub>OUT2</sub> = 3A, buck 1 V<sub>OUT</sub> = 20V to 5V



### Output Voltage Transition (Buck 2)

#### V<sub>OUT</sub> Set via the I<sup>2</sup>C

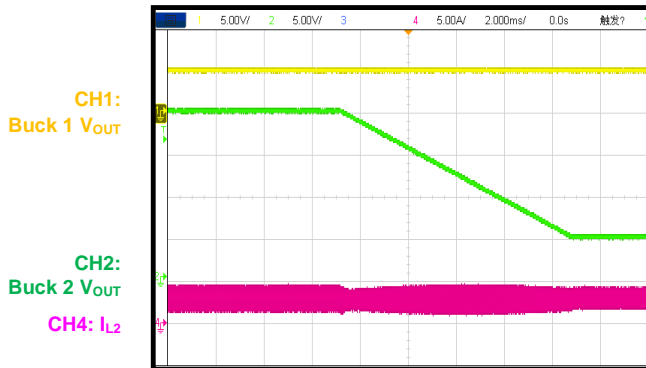
V<sub>IN</sub> = 24V, buck 1 V<sub>OUT</sub> = 5V, I<sub>OUT1</sub> = I<sub>OUT2</sub> = 3A,  
buck 2 V<sub>OUT</sub> = 5V to 20V



### Output Voltage Transition (Buck 2)

#### V<sub>OUT</sub> Set via the I<sup>2</sup>C

V<sub>IN</sub> = 24V, buck 1 V<sub>OUT</sub> = 5V, I<sub>OUT1</sub> = I<sub>OUT2</sub> =  
3A, buck 2 V<sub>OUT</sub> = 20V to 5V



## FUNCTIONAL BLOCK DIAGRAM

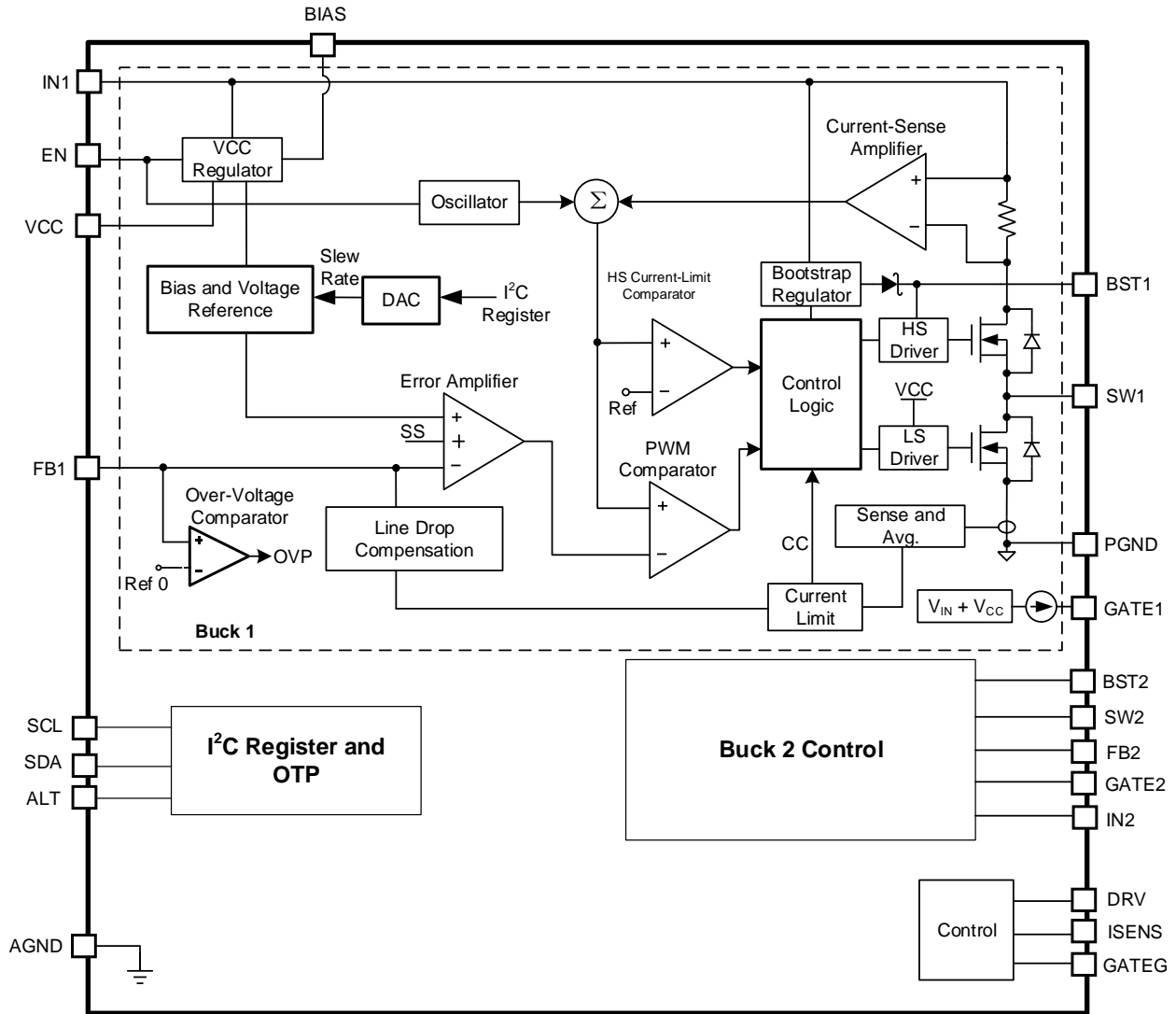


Figure 2: Functional Block Diagram



## OPERATION

### BUCK CONVERTER

The MPQ4272 integrates two dual-channel, monolithic, synchronous, rectified, step-down switch-mode converters with internal power MOSFETs. It offers a compact solution to achieve a dual 3A of continuous output current across a wide input supply range, with excellent load and line regulation.

Each step-down converter operates with fixed-frequency, peak current mode control to regulate the output voltage ( $V_{OUT}$ ). There is an internal oscillator that generates two phase-shift reference clocks. Each reference clock initiates the PWM cycle of each channel, which turns on the integrated high-side MOSFET (HS-FET). The HS-FET remains on until its current reaches the value set by the COMP voltage ( $V_{COMP}$ ). When the HS-FET turns off, it remains off until the next clock cycle begins.

### Error Amplifier (EA) of Each Channel

The error amplifier (EA) compares the internal feedback voltage ( $V_{FB}$ ) to the internal reference voltage ( $V_{REF}$ ) and outputs  $V_{COMP}$ .  $V_{COMP}$  controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies control loop design.

### BIAS and VCC Regulator

Most of the internal circuitries are powered by the internal VCC regulator. The MPQ4272 has two internal regulators (LDO1 and LDO2) (see Figure 3).

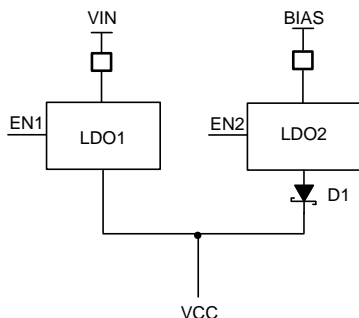


Figure 3: LDO Structure

LDO1 takes the  $V_{IN}$  input and operates across the full  $V_{IN}$  range. When  $V_{IN}$  exceeds 5V, the regulator output is in full regulation, and VCC is 5V. When  $V_{IN}$  drops below 5V, the output degrades.

The second regulator (LDO2) is powered by the BIAS pin. Connect the BIAS pin to an external power supply (>4.8V). LDO2 turns on when  $BIAS > 4.8V$ . Once LDO2 is enabled, LDO1 is disabled. For output applications equal to or exceeding 5V, connect BIAS to the output to improve efficiency. The diode (D1) between BIAS and the internal circuit is used for current reverse blocking. If the BIAS function is not used, connect the BIAS pin to GND.

VCC requires an external 1 $\mu$ F ceramic decoupling capacitor.

### Enable (EN) Control

The MPQ4272 offers enable (EN) control. The EN pin has two levels with different thresholds. At the first level,  $EN > 0.7V$ , and VCC is enabled. At the second level,  $EN > 1.6V$ , and the chip begins normal operation. EN is clamped internally using a 10V series Zener diode (see Figure 4). Use two resistor dividers to connect the EN pin to the  $V_{IN}$  supply and to GND. The EN rising threshold is 1.6V, so  $V_{IN}$  must exceed 6.05V to enable the circuit. Do not add a capacitor above 1nF on the EN pin.

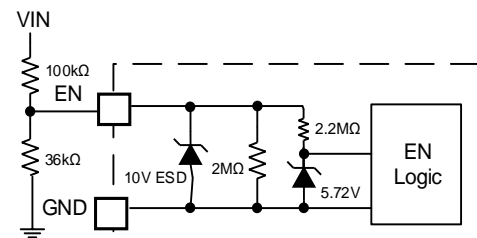


Figure 4: 10V Zener Diode Connection

It is recommended to connect a 100k $\Omega$  resistor between  $V_{IN}$  and EN, and a 36k $\Omega$  resistor between EN and GND. The  $V_{IN}$  start and stop switching thresholds can be calculated with Equation (1) and Equation (2), respectively:

$$V_{IN\_ON}(V) = V_{EN\_ON}(V) \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right) = 6.05V \quad (1)$$

$$V_{IN\_OFF}(V) = V_{EN\_OFF}(V) \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right) = 5.29V \quad (2)$$

The EN rising threshold is 1.6V, and the EN falling threshold is 1.4V. This means that the  $V_{IN}$  rising threshold is 6.05V, and the  $V_{IN}$  falling threshold is 5.29V.

If EN is connected directly to a voltage source without a pull-up resistor, limit the amplitude of the voltage source to  $\leq 6V$  to prevent damage to the Zener diode.

### Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the input voltage ( $V_{IN}$ ). The UVLO rising threshold is 3.35V, and its falling threshold is 3.05V.

### Internal Soft Start (SS)

Soft start (SS) prevents  $V_{OUT}$  from overshooting during start-up. When the chip starts up, the internal circuitry generates a SS voltage ( $V_{SS}$ ) that ramps up from 0V to 5V. When  $V_{SS}$  is below  $V_{REF}$ , the EA uses  $V_{SS}$  as the reference. When  $V_{SS}$  exceeds  $V_{REF}$ , the EA uses  $V_{REF}$  as the reference.

If the MPQ4272 output is pre-biased to a certain voltage during start-up, the IC disables the switching of both the HS-FET and low-side MOSFET (LS-FET) until the voltage on the internal SS capacitor exceeds the internal  $V_{FB}$ .

### Low-Dropout Mode

The MPQ4272 has a low-dropout function when  $V_{IN}$  is almost equal to  $V_{OUT}$ . After the minimum off time is triggered, the on time is extended and the switching frequency starts to decrease. When the maximum on time is triggered, the MPQ4272 works in maximum duty cycle operation (about 99.4%).

### Constant Current (CC) Mode Over-Current Protection (OCP)

The MPQ4272 senses the low-side current and uses this information to emulate the output current ( $I_{OUT}$ ) amplitude. If  $I_{OUT}$  exceeds the set current-limit threshold, the MPQ4272 enters constant current (CC) limit mode. In this mode, the current amplitude is limited.

As the load resistance drops,  $V_{OUT}$  also drops until  $V_{FB}$  falls below the under-voltage (UV) threshold. Once a UV condition is triggered, the MPQ4272 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead shorted to ground. This greatly reduces the average short-circuit current, alleviates thermal issues, and protects the regulator. The MPQ4272 exits hiccup mode once the over-

current (OC) condition is removed.

When  $V_{OUT}$  is set above 6.3V, the MPQ4272 hiccup UV threshold is about 2.4V. When  $V_{OUT}$  is set below 5.5V, the hiccup UV threshold is about 30% of the feedback reference value.

### Buck Output Over-Voltage Protection (OVP)

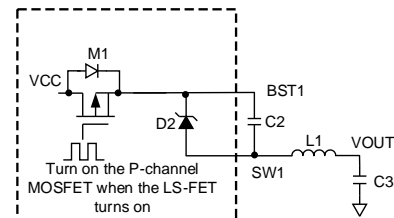
The MPQ4272 has output over-voltage protection (OVP). If  $V_{OUT}$  exceeds 120% of  $V_{REF}$ , the HS-FET stops turning on. The LS-FET turns on to discharge  $V_{OUT}$  until the low-side current reaches -3.6A. When the next internal clock starts, the LS-FET turns on again and repeats this process. Once  $V_{FB}$  drops to 109% of  $V_{REF}$ , the MPQ4272 resumes normal operation.

### Input Over-Voltage Protection (OVP)

The MPQ4272 has input over-voltage protection (OVP). If both output OVP and the input OVP fault rising threshold (about 39.5V) are triggered at the same time, the device stops switching. When  $V_{IN}$  falls below the input OVP fault falling threshold (about 37V), the device starts switching again. The MPQ4272 continues switching when the input OVP warning threshold is triggered. The input OVP warning rising threshold is about 37.5V, and the falling threshold is about 35V.

### Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. The UVLO rising threshold is 2.2V, with a hysteresis of 150mV. The BST1 capacitor voltage is regulated internally by VCC through D2, M1, and C2 (see Figure 5).



**Figure 5: Internal Bootstrap Charging Circuit**

### Start-Up and Shutdown

If both  $V_{IN1}$  and EN exceed their respective thresholds and I<sup>2</sup>C operation is set up, the chip is enabled.

The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Several events can shut down the chip: EN going low, VIN going low, an I<sup>2</sup>C operation off command, and thermal shutdown. During shutdown, the signaling path is blocked to avoid any fault triggering. Then V<sub>COMP</sub> and the internal supply rails are pulled down. The floating driver is not subject to this shutdown command.

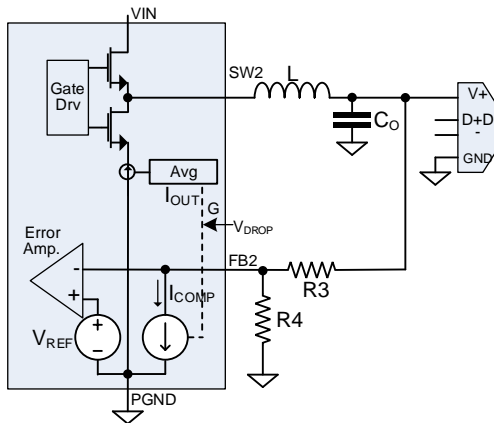
### EN Shutdown Discharge

When the EN pin is pulled low, the buck converter enters output discharge mode. Meanwhile, the internal soft-start capacitor starts to discharge. The discharge mode keeps working until the soft-start capacitor discharges to a very low level.

In this mode, the LS-FET turns on and remains on until the low-side current reaches the negative current limit (about -3.6A). Then the LS-FET turns off. It turns on again when the next clock cycle begins.

### Output Line Drop Compensation

The MPQ4272 is capable of compensating for a V<sub>OUT</sub> drop (e.g. high impedance caused by a long trace) to keep a fairly constant load-side voltage. The MPQ4272 uses the sensed load current through the LS-FET to sink a current (I<sub>COMP</sub>) at the FB pin (see Figure 6).



**Figure 6: Line Drop Compensation**

I<sub>COMP</sub> can be calculated with Equation (3):

$$I_{COMP} = G \times I_{OUT} \quad (3)$$

V<sub>OUT</sub> can be estimated with Equation (4):

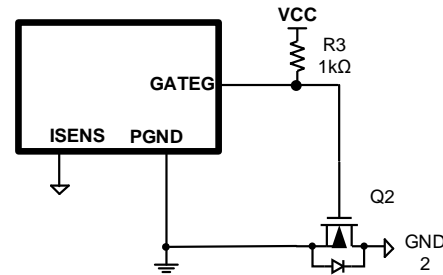
$$V_{OUT} = \left( \frac{R_3}{R_4} + 1 \right) \times V_{REF} + R_3 \times G \times I_{OUT} \quad (4)$$

The line drop compensation amplitude under certain output current conditions is equal to R<sub>3</sub> × G × I<sub>OUT</sub>.

The gain (G) is fixed internally, but it can be configured via the I<sup>2</sup>C. R<sub>3</sub> can be used to adjust the line drop compensation amplitude.

### Battery Short-to-Ground Protection Driver

The MPQ4272 integrates a battery short-to-ground protection driver (GATEG pin). When the output ground (GND 2) shorts to the battery, the I<sub>SENS</sub> pin's secondary current limit is triggered, the GATEG pin is pulled low, and Q2 turns off (see Figure 7).



**Figure 7: Battery Short-to-Ground Protection**

The secondary current limit threshold is equal to 160mV divided by the Q2 R<sub>DS(ON)</sub>. This can protect the GND current from ramping up when the car battery (B+) is falsely shorted to USB GND 2. Meanwhile, the buck output is disabled when secondary current limit is triggered.

If this protection is not required, short I<sub>SENS</sub> to PGND and float the GATEG pin.

Table 1 shows the different statuses for the GATEG pin.

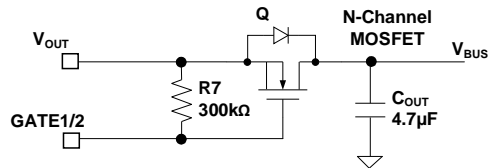
**Table 1: GATEG Pin Status**

| Condition                   | GATEG Status |
|-----------------------------|--------------|
| VIN < UVLO threshold        | Open drain   |
| EN < UVLO threshold         | Open drain   |
| Operation = off             | Open drain   |
| I <sub>SENS_R</sub> > 160mV | 0            |

### V<sub>BUS</sub> Isolation N-Channel MOSFET Driver

GATE1 and GATE2 source a weak 20μA pull-up current to turn on Q1 and Q2. This allows V<sub>BUS</sub> to turn on. The maximum GATE1 / GATE2 driving voltage is equal to V<sub>IN1</sub> + V<sub>CC</sub> (or 25V maximum) via an internal charge pump. A 300kΩ resistor (R7) or Zener diode is required to clamp the maximum Q1 V<sub>GS</sub> (see Figure 8). In this configuration, the reverse current is blocked during shutdown. When EN is commanded off via the I<sup>2</sup>C or the device shuts down through the EN pin, the V<sub>BUS</sub> voltage (V<sub>BUS</sub>) is discharged first before GATE1 and GATE2 turn off.

When the second current limit is triggered (I<sub>SENSE</sub> > 160mV), GATE1 and GATE2 also turn off.



**Figure 8: V<sub>BUS</sub> Isolation Schematic for GATE1 and GATE2**

### SYSTEM

#### Thermal Shutdown (TSD)

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the silicon die temperature exceeds 160°C, the entire chip shuts down. When the temperature falls below its lower threshold (about 140°C), the chip is enabled. The thermal shutdown (TSD) threshold can be configured via the I<sup>2</sup>C and OTP. The default value is 010b.

#### I<sup>2</sup>C Timing

The I<sup>2</sup>C is active once V<sub>IN</sub> and EN exceed their UVLO thresholds.

## PMBUS INTERFACE

### PMBus Serial Interface Description

The power management bus (PMBus) is an open-standard power management protocol that defines a means of communication with power conversion and other devices.

The PMBus is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the lines, a master device generates an SCL signal and device address, and arranges the communication sequence. This is based on I<sup>2</sup>C operation principles.

### Start and Stop Conditions

The start and stop conditions are signaled by the master device, which signifies the beginning and end of the PMBus transfer. A start command (S) is defined as the SDA signal transitioning from high to low while the SCL is high. A stop command (P) is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 9).

The master then generates the SCL clocks and transmits the device address and the read/write (R/W) direction bit on the SDA line. Data is transferred in 8-bit bytes by the SDA line. Each byte of data is followed by an acknowledge (ACK) bit.

### PMBus Update Sequence

The MPQ4272 requires a start condition, a valid PMBus address, a register address byte, and a data byte for a single data update. The device acknowledges that it has received each byte by pulling the SDA line low during the high period of a single clock pulse. A valid PMBus address selects the MPQ4272. The device performs an update on the falling edge of the LSB byte.

### PMBus Bus Message Format

Figure 10 shows the PMBus message format. The unshaded cells indicate that the bus host is actively driving the bus, and shaded cells indicate that the MPQ4272 is driving the bus. Additional components are defined below:

- S = Start condition
- Sr = Repeated start condition
- P = Stop condition
- R = Read bit
- $\bar{W}$  = Write bit
- A = Acknowledge bit (0)
- $\bar{A}$  = Acknowledge bit (1)

“A” represents the acknowledge (ACK) bit. The ACK bit is typically active low (logic 0) if the transmitted byte is received successfully by a device.

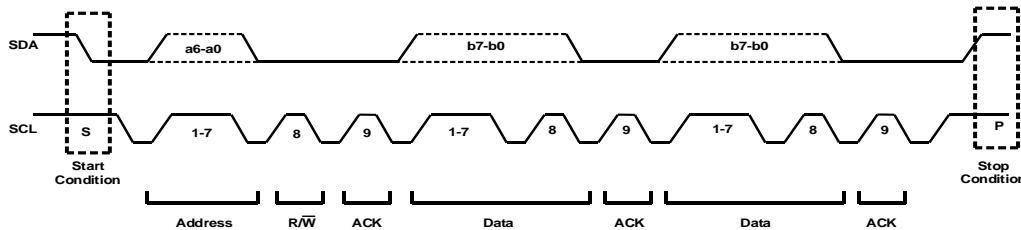
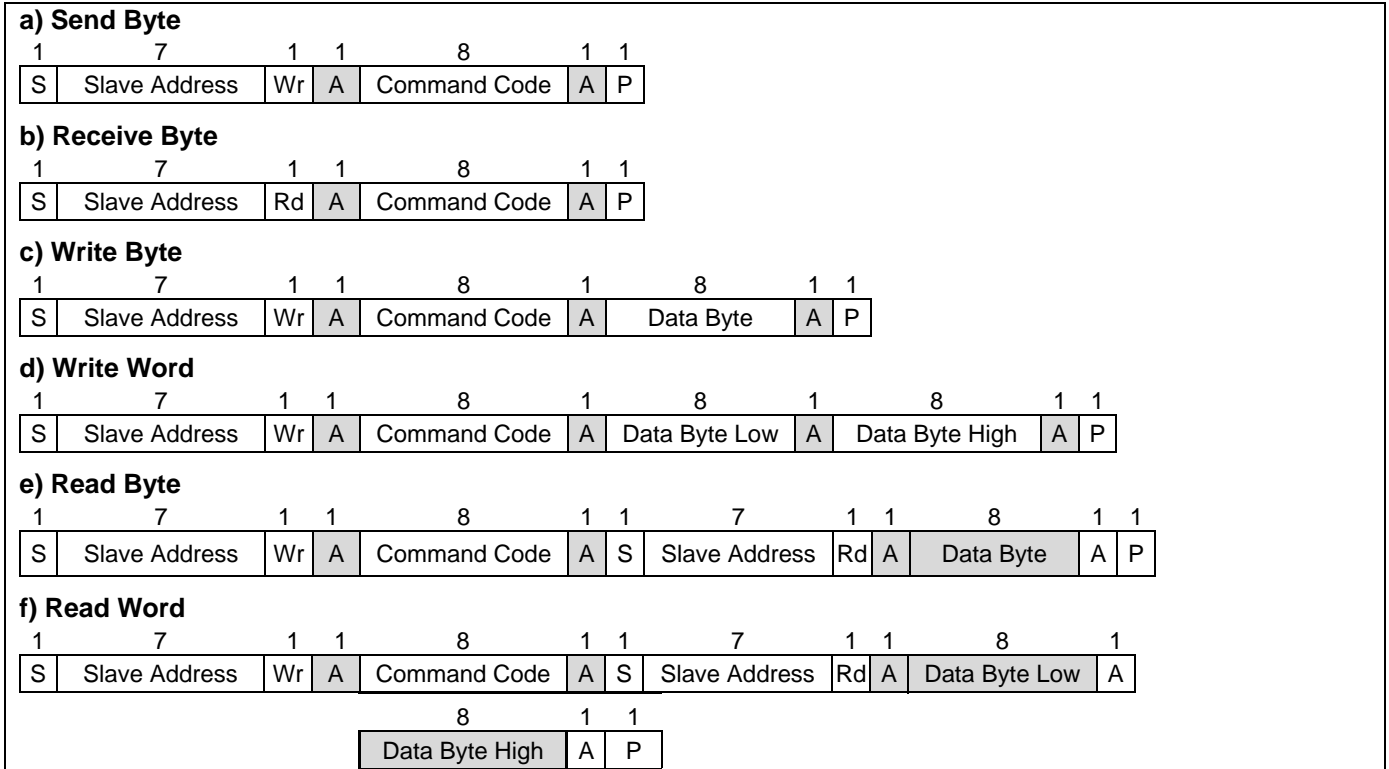


Figure 9: Data Transfer Over the PMBus


**Figure 10: PMBus Message Format**

## REGISTER DESCRIPTION

### I<sup>2</sup>C/PMBus Register

| CMD Name   | CMD Code | Description   | Type      | Data Format | Units | OTP | Default Value <sup>(9)</sup> |
|--|----------|---|-----------|-------------|-------|-----|------------------------------|
| PAGE (1 page). "0xFF" means the both buck converters are being controlled. | 0x00     | See the PAGE section on page 25                                     | R/W byte  | Reg         | -     | N   | 0                            |
| OPEARTION (Page 0 and Page 1)  | 0x01     | On/off  | R/W byte  | Reg         | -     | Y   | Off                          |
| CLEAR_FAULTS (1 page)  | 0x03     |   | Send byte | Reg         | -     | N   | -                            |
| WRITE_PROTECT (1 page)   | 0x10     |   | R/W byte  | Reg         | -     | N   | -                            |
| STORE_USER_ALL (1 page)  | 0x15     | Support 1 time OTP only   | Send byte | Reg         | -     | N   | -                            |
| RESTORE_USER_ALL (1 page)  | 0x16     |   | Send byte | Reg         | -     | N   | -                            |
| VOUT_MODE (1 page)   | 0x20     | Output voltage format and exponent (2 <sup>-10</sup> )              | R byte    | Reg         | -     | N   | 2 <sup>-10</sup><br>(0x16)   |
| VOUT_COMMAND (Page 0 and Page 1)   | 0x21     |   | R/W word  | Linear L16  | V     | Y   | 5V                           |
| VOUT_SCALE_LOOP (Page 0 and Page 1)  | 0x29     |   | R/W word  | Linear L11  | -     | Y   | 0.08                         |
| STATUS_BYTE (Page 0 and Page 1)  | 0x78     |   | R byte    | Reg         | -     | N   | -                            |
| STATUS_WORD (Page 0 and Page 1)  | 0x79     |   | R word    | Reg         | -     | N   | -                            |
| STATUS_VOUT (Page 0 and Page 1)  | 0x7A     |   | R byte    | Reg         | -     | N   | -                            |
| STATUS_INPUT (1 page)  | 0x7C     |   | R byte    | Reg         | -     | N   | -                            |
| STATUS_TEMPERATURE (1 page)  | 0x7D     |   | R byte    | Reg         | -     | N   | -                            |
| STATUS_CML (1 page)  | 0x7E     |   | R byte    | Reg         | -     | N   | -                            |
| MFR_Buck_CTRL1 (Page 0 and Page 1)   | 0xD0     | PWM/PFM, output discharge, hiccup timer, output OVP EN, phase delay | R/W byte  | Reg         | -     | Y   | -                            |
| MFR_Buck_CTRL2 (1 page)  | 0xD1     |   | R/W byte  | Reg         | -     | Y   | -                            |
| MFR_CURRENT_LIMIT (Page 0 and Page 1)                                      | 0xD2     | Sets the CC current limit continuously                              | R/W byte  | Reg         | -     | Y   | 3.6A                         |
| MFR_CTRL3 (1 page)   | 0xD3     | I <sup>2</sup> C address, OTP threshold                             | R/W byte  | Reg         | -     | Y   | -                            |
| MFR_CTRL4 (1 page)   | 0xD4     | Frequency, slew rate, OTP warning threshold                         | R/W byte  | Reg         | -     | Y   | -                            |
| MFR_CRC_ERROR_FLAG (1 page)  | 0xD5     | Set high when restoring OTP data CRC check error occurs             | R byte    | Reg         | -     | N   | 0                            |
| OTP_CONFIGURATION_CODE (1 page)  | 0xD6     | Represents the device   | R/W byte  | Reg         | -     | Y   | -                            |
| OTP_REVISION_NUMBER (1 page)   | 0xD7     | 1 byte is about 0x01  | R/W byte  | Reg         | -     | Y   | -                            |
| MFR_STATUS_MASK (1 page)   | 0xD8     | Masks the ALT pin indication  | R/W byte  | Reg         | -     | Y   | -                            |

**Note:**

9) All default register values are for the MPQ4272-0000 suffix.

## PMBUS COMMAND INTRODUCTION

### Data Format (Linear16 and Linear11)

Linear16 (L16) format is used for the  $V_{OUT}$  command (see Figure 11).

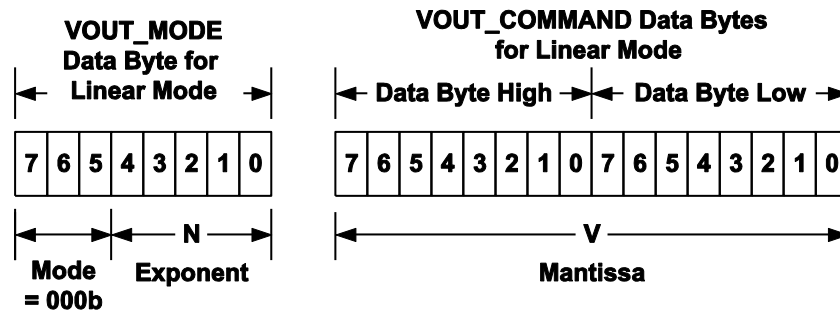


Figure 11: Linear16 Format

The Mode bits are set to 000b. The voltage (in V) can be calculated with Equation (5):

$$\text{Voltage} = V \times 2^N \quad (5)$$

Where Voltage is the parameter of interest (in V), V is a 16-bit unsigned binary integer, and N is a 5-bit two's complement binary integer.

Linear11 (L11) format is used for other commands, such as the  $V_{OUT}$  scale loop, output current, and temperature (see Figure 12).

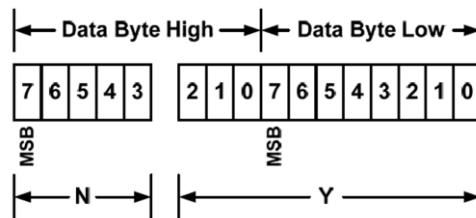


Figure 12: Linear11 Format

The relation between Y, N, and the real-world value (X) can be estimated with Equation (6):

$$X = Y \times 2^N \quad (6)$$

Where X is the real-world value, Y is an 11-bit two's complement integer, and N is 5-bit two's complement integer.

Devices that use the linear format must accept and be able to process any value of N.



## PAGE 0 and PAGE 1

### PAGE

The PAGE command provides the ability to configure, control, and monitor the device through only one physical address. Note that there are multiple outputs on one device.

| Bits[7:1] Value | Bit[0] Value | Description                          |
|-----------------|--------------|--------------------------------------|
| Reserved        | 0 (default)  | Buck 1 and output 1 are selected     |
| Reserved        | 1            | Buck 2 and output 2 are selected     |
| 0xFF            |              | Control both channels simultaneously |

In regards to Page 0 and Page 1 operation, the registers that only have one page can be read and written under Page 1 mode. For example, the CLEAR\_FAULT register only has one page, but it can be accessed and changed when PAGE is set to 0 or 1.

When PAGE is set to 0xFF, all buck 1 and buck 2 registers (including the MFR registers) are written to the same value when the I<sup>2</sup>C master sends a write command.

### OPERATION

The OPERATION command configures the operational state of the converter. Set OPERATION to 0x80 to enable the output. Set OPERATION to 0x00 or 0x40 to disable the output.

| Bits | Purpose   | Bit Value   | Description        |
|------|---|-------------|--------------------|
| 7    | On/off state. Note that the EN pin has a higher control priority than this bit. | 0 (default) | The output is off. |
|      |   | 1           | The output is on.  |
| 6:0  | Reserved.   |             |                    |

### CLEAR\_FAULTS

The CLEAR\_FAULTS command clears any fault bits that have been set. This command clears all bits in all status registers simultaneously. The device also releases its ALT signal output if the ALT signal is asserted.

If the device has latched off due to a fault protection, the CLEAR\_FAULTS command does not force the device to restart.

If the fault is still present when the bit is cleared, the fault bit is immediately set again, and the host is notified. This command is write-only. There is no data byte for this command.

### WRITE\_PROTECT

The WRITE\_PROTECT command controls writing to the PMBus device. The intent of this command is to provide protection against accidental changes. All supported commands may have their parameters read, regardless of the WRITE\_PROTECT settings.

| Data Byte Value | Description  |
|-----------------|--|
| 1000 0000       | Disable all writes except for the WRITE_PROTECT command.                                     |
| 0100 0000       | Disable all writes except for the WRITE_PROTECT, OPERATION, and PAGE commands.               |
| 0010 0000       | Disable all writes except for the WRITE_PROTECT, OPERATION, PAGE, and VOUT_COMMAND commands. |
| 0000 0000       | Enable writes to all commands. This is the default value.                                    |

### STORE\_USER\_ALL

The STORE\_USER\_ALL command instructs the PMBus device to copy the entire contents of the operating memory to the matching locations in the OTP (non-volatile user store memory). Any items in operating memory that do not have matching locations in the user store are ignored.

The STORE\_USER\_ALL command can be used while the device is operating. However, the device rejects the I<sup>2</sup>C write operation until the OTP program is finished. During this process, the I<sup>2</sup>C read command is still supported. While storing the user memory to the OTP, the device does a cyclic redundancy check (CRC) calculation, and stores the CRC result in a 1-byte OTP cell.

The output turns off first during this operation, then starts up again after the OTP program is finished.

This command has no data bytes. This command is write-only. Only the MPQ4272-0000 IC allows a one-time STORE\_USER\_ALL operation. Other suffix codes are already OTP-configured in the factory, so they do not support user configurations.

### RESTORE\_USER\_ALL

The RESTORE\_USER\_ALL command instructs the PMBus device to copy the entire contents of the OTP to the matching locations in the operating memory (I<sup>2</sup>C register). The values in the operating memory are overwritten by the value retrieved from the user store. Any items in user store that do not have matching locations in the operating memory are ignored.

The RESTORE\_USER\_ALL command can be used while the device is operating. However, the device rejects the I<sup>2</sup>C write operation until the OTP restoration process is finished. During this process, the I<sup>2</sup>C read command is still supported. While restoring OTP data to the user memory, the device does a CRC calculation and compares the calculated result to the stored CRC result in the OTP cell. The OTP value is restored to the operating memory only when the values match one other.

The output turns off first during this operation, then starts up again after the OTP program is finished.

This command is write-only. There is no data byte for this command.

### VOUT\_MODE

| Command       | VOUT_MODE       |   |   |   |   |   |   |   |
|---------------|-----------------|---|---|---|---|---|---|---|
| Format        | Unsigned binary |   |   |   |   |   |   |   |
| Bit           | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access        | R               | R | R | R | R | R | R | R |
| Function      | MODE            |   |   | N |   |   |   |   |
| Default Value | 0               | 0 | 0 | 1 | 0 | 1 | 1 | 0 |

The MPQ4272 only supports linear mode. Mode bits are set to 000b by default. N is set to a fixed value of -10.

### VOUT\_COMMAND

The VOUT\_COMMAND sets the output voltage ( $V_{OUT}$ ). It follows Linear16 data format.

| Command            | VOUT_COMMAND   |     |     |     |     |     |     |     |               |     |     |     |     |     |     |     |
|--------------------|----------------|-----|-----|-----|-----|-----|-----|-----|---------------|-----|-----|-----|-----|-----|-----|-----|
| Format             | Linear16       |     |     |     |     |     |     |     |               |     |     |     |     |     |     |     |
| Bit                | 15             | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7             | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access             | R/W            | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W           | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function           | Data byte high |     |     |     |     |     |     |     | Data byte low |     |     |     |     |     |     |     |
| Default Value (5V) | 5120 decimal   |     |     |     |     |     |     |     |               |     |     |     |     |     |     |     |

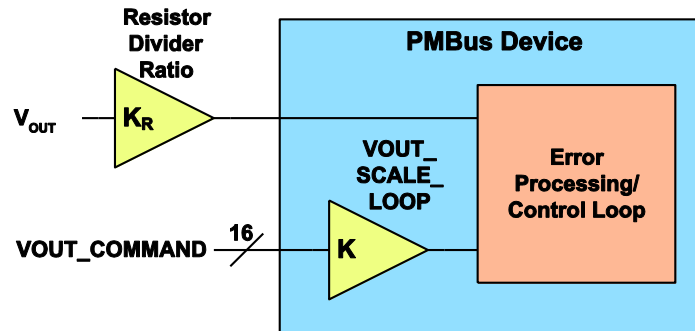
$V_{OUT}$  (in V) can be calculated with Equation (7):

$$V_{OUT} = V \times 2^{-10} \tag{7}$$

Where V is a 16-bit unsigned binary integer of  $V_{OUT\_COMMAND}$ , bits[15:0].

The actual  $V_{OUT}$  resolution or minimum step is 0.8mV/K, where K is the value set by  $V_{OUT\_SCALE\_LOOP}$ . For example, if the feedback resistor ratio ( $V_{OUT} / V_{FB}$ ) equals 12.5, then  $K = 1/12.5 = 0.08$ . The real  $V_{OUT\_COMMAND}$  resolution is 10mV (see Figure 13).

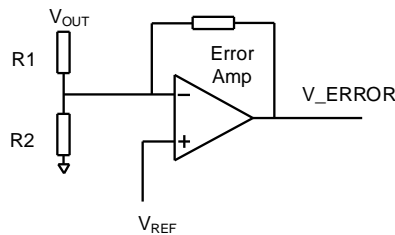
The internal reference voltage is equal to  $V_{OUT} \times K$ . The internal reference voltage ranges between 0.1V and 1.63V, with a 0.8mV step.



**Figure 13: Resistor Divider Ratio**

### V<sub>OUT\_SCALE\_LOOP</sub>

$V_{OUT}$  is typically sensed through a resistor divider (see Figure 14). The resistor divider reduces or scales  $V_{OUT}$  so that when  $V_{OUT}$  is correct, the value supplied to the control circuit is equal to  $V_{REF}$ . This command has 2 data bytes encoded in linear format. It functions similarly to the  $V_{OUT\_COMMAND}$  data format, and its value is unitless.



**Figure 14: Output Voltage Sense**

| Command              | V <sub>OUT_SCALE_LOOP</sub>  |    |    |    |    |                |     |     |     |     |                                     |     |     |     |     |     |
|----------------------|------------------------------|----|----|----|----|----------------|-----|-----|-----|-----|-------------------------------------|-----|-----|-----|-----|-----|
| Format               | Linear11                     |    |    |    |    |                |     |     |     |     |                                     |     |     |     |     |     |
| Bit                  | 15                           | 14 | 13 | 12 | 11 | 10             | 9   | 8   | 7   | 6   | 5                                   | 4   | 3   | 2   | 1   | 0   |
| Access               | R                            | R  | R  | R  | R  | R/W            | R/W | R/W | R/W | R/W | R/W                                 | R/W | R/W | R/W | R/W | R/W |
| Function             | N                            |    |    |    |    | Data byte high |     |     |     |     | Data byte low                       |     |     |     |     |     |
| Default Value (0.08) | -10 decimal,<br>10110 binary |    |    |    |    |                |     |     |     |     | 82 decimal,<br>000 0101 0010 binary |     |     |     |     |     |

$V_{OUT\_SCALE\_LOOP}$  is determined by  $V_{FB} / V_{OUT}$  or  $R2 / (R1 + R2)$ , calculated with Equation (8):

$$V_{OUT\_SCALE\_LOOP} = X \times 2^{-10} \tag{8}$$

Where X is an 11-bit, unsigned binary integer of VOUT\_SCALE\_LOOP, bits[10:0]. The default value is 0.08.

In real applications, the user should always set VOUT\_SCALE\_LOOP value equal to the external R2 / (R1 + R2) value. To select VOUT\_SCALE\_LOOP, follow the steps below:

1. Confirm the maximum V<sub>OUT</sub>. The MPQ4272's maximum FB reference voltage is 1.638V. Once the maximum V<sub>OUT</sub> is confirmed, there is a minimum feedback ratio value:  $(R1 + R2) / R2_{MIN} = VOUT\_MAX / 1.638$ .
2. Confirm the minimum V<sub>OUT</sub> change resolution. The MPQ4272's minimum FB reference voltage resolution is 0.8mV. The V<sub>OUT</sub> change resolution is equal to  $0.8mV \times (R1 + R2) / R2$ . This means that the maximum feedback ratio  $(R1 + R2) / R2_{MAX} = VOUT_{MIN\_DVS\_STEP} / 0.8$ .
3. Choose a proper R2 / (R1 + R2) value that meets the requirements from step 1 and step 2.
4. Set the VOUT\_SCALE\_LOOP value according to step 3.

For example, in USB PD applications, a 3.3V to 21V output with a 20mV resolution is required for 60W PPS APDO. To obtain the required values, follow the steps below:

1.  $(R1 + R2) / R2_{MIN} = 21V / 1.638V = 12.82$
2.  $(R1 + R2) / R2_{MAX} = 20mV / 0.8mV = 25$
3. Choose  $(R1 + R2) / R2 = 15.7$ . Note that this value can be set to any value between 12.82 and 25.
4. VOUT\_SCALE\_LOOP = 0.0635 according to step 3. In real USB PD applications, set R1 to 93.1kΩ and R2 to 6.2kΩ for a higher V<sub>OUT</sub> to meet MFI certification requirements.

## STATUS\_BYTE

The STATUS\_BYTE command returns 1 byte of information with a summary of the most critical faults. The STATUS\_BYTE message content is described in greater detail below.

| Bit | Bit Name          | Description   |
|-----|-------------------|---|
| 7   | BUSY              | A fault is detected because the device is busy and unable to respond.   |
| 6   | OFF               | This bit is asserted if the unit is not providing power to the output, regardless of the reason (e.g. the device is not enabled). This bit is a non-latch protection. It automatically updates its status without a CLEAR_FAULTS command. |
| 5   | VOUT_OV_FAULT     | An output over-voltage (OV) fault has occurred.   |
| 4   | IOUT_OC_FAULT     | An output over-current (OC) fault has occurred. If the device reaches the CC current limit or enters hiccup mode, this bit is set.  |
| 3   | VIN_UV_FAULT      | An input under-voltage (UV) fault has occurred.   |
| 2   | TEMPERATURE       | A temperature fault or warning has occurred.  |
| 1   | CML               | A communications, memory, or logic fault has occurred (e.g. over-temperature protection or a CRC error).  |
| 0   | NONE_OF_THE_ABOVE | A fault or warning not listed in bits[7:1] has occurred.  |

## STATUS\_WORD

The STATUS\_WORD command returns 2 bytes of information with a summary of the MPQ4272's fault conditions. Based on the information in these bytes, the host can get more information by reading the appropriate status registers.

The low byte of the STATUS\_WORD is the same register as the STATUS\_BYTE command.

| Byte | Bits    | Bit Name   | Description   |
|------|---------|--|---|
| Low  | 7:0     | -  | See the STATUS_BYTE register on page 28.  |
| High | 7       | VOUT   | A V <sub>OUT</sub> fault or warning has occurred.   |
|      | 6       | IOUT/POUT  | An I <sub>OUT</sub> condition has occurred. If the device reaches the CC current limit or enters hiccup mode, this bit is set.  |
|      | 5       | INPUT  | A V <sub>IN</sub> fault or warning has occurred.  |
|      | 4       | OC_EXIT  | This bit indicates if I <sub>OUT</sub> exits the CC current limit. If I <sub>OUT</sub> changes from CC (before entering hiccup mode) to non-CC mode, this bit is set high. Recovery from hiccup mode does not set this bit. Send a CLEAR_FAULTS command to reset this bit.  |
|      | 3       | PG_STATUS#   | If the POWER_GOOD signal is present, this bit is ineffective. This bit is a non-latch protection. It automatically updates its status without a CLEAR_FAULTS command.<br>If V <sub>OUT</sub> < 80% of the set-up value, this bit is set to indicate that V <sub>OUT</sub> is not good. When V <sub>OUT</sub> > 90% of the set-up value, this bit is cleared, and V <sub>OUT</sub> is power good. The PG signal rising edge is about 80%, and the falling edge is about 90%. |
|      | 2       | RESERVED   | Reserved.   |
|      | 1       | OTHER  | A bit in the STATUS_OTHER register is set.  |
| 0    | UNKNOWN | A fault type not listed in bits[15:1] of the STATUS_WORD register has been detected. |   |

Most bits remain set, but there are two exceptions: the OFF and PG\_STATUS# bits. These bits always reflect the current state of the device and the POWER\_GOOD signal (if present).

## STATUS\_VOUT

The STATUS\_VOUT command returns 1 byte of data to indicate whether a fault or warning has occurred.

| Bits | Bit Name        | Description                                  |
|------|-----------------|--|
| 7    | VOUT_OV_FAULT   | Output over-voltage (OV) fault indicator.    |
| 6    | VOUT_OV_WARNING | Output OV warning indicator.                 |
| 5    | VOUT_UV_WARNING | Output under-voltage (UV) warning indicator. |
| 4    | VOUT_UV_FAULT   | Output UV fault indicator.                   |
| 3:0  | RESERVED        | Reserved.                                    |

### STATUS\_INPUT

The STATUS\_INPUT command returns 1 byte of data to indicate whether a fault or warning has occurred. This command is only one page.

| Bit | Bit Name       | Description                                 |
|-----|----------------|---|
| 7   | VIN_OV_FAULT   | Input over-voltage (OV) fault indicator.    |
| 6   | VIN_OV_WARNING | Input OV warning indicator.                 |
| 5   | VIN_UV_WARNING | Input under-voltage (UV) warning indicator. |
| 4   | VIN_UV_FAULT   | Input UV fault indicator.                   |
| 3   | RESERVED       | Reserved.                                   |
| 2   | RESERVED       | Reserved.                                   |
| 1   | RESERVED       | Reserved.                                   |
| 0   | RESERVED       | Reserved.                                   |

### STATUS\_TEMPERATURE

The STATUS\_TEMPERATURE command returns 1 byte of data to indicate whether a fault or warning has occurred. This command is only one page.

| Bits | Bit Name        | Description  |
|------|-----------------|--|
| 7    | OT_FAULT        | Over-temperature (OT) fault indicator. This bit has the same OTP threshold that is set by MFR_OT_FAULT_LIMIT.                          |
| 6    | OT_WARNING      | Over-temperature (OT) warning indicator. See the I <sup>2</sup> C register section (OT_WARNING_THRESHOLD) on page 33 for more details. |
| 5    | UT_WARNING      | Under-temperature warning indicator. The under-temperature warning threshold is -20°C, with a 10°C hysteresis.                         |
| 4    | UT_FAULT        | Under-temperature fault indicator. The under-temperature fault threshold is -40°C, with a 10°C hysteresis.                             |
| 3    | OT_WARNING_EXIT | The OT_WARNING falling edge sets this bit high. There is a 20°C hysteresis.  |
| 2:0  | RESERVED        | Reserved.  |

## MFR COMMAND DESCRIPTION

### I<sup>2</sup>C Register Map

| Name                   | REG (0x) | R/W | D[7]  | D[6]                        | D[5]        | D[4]          | D[3]                 | D[2]                | D[1]         | D[0]      |
|------------------------|----------|-----|---|-----------------------------|-------------|---------------|----------------------|---------------------|--------------|-----------|
| MFR_BUCK_CTRL1         | D0       | R/W | DROPOUT_EN  | LINE_DROP_COMPENSATION_GAIN |             | OUTPUT_OVP_EN | HICCUP_TIMER         | OUTPUT_DISCHARGE_EN | PFM/PWM_MODE |           |
| MFR_BUCK_CTRL2         | D1       | R/W | GATE1_2_EN  | -                           | PHASE_DELAY | -             | DRV_VOLTAGE          | DITHER_ENABLE       |              |           |
| MFR_CURRENT_LIMIT      | D2       | R/W | CONSTANT_CURRENT_LIMIT (1A to 6.4A/50mA Step)             |                             |             |               |                      |                     |              |           |
| MFR_CTRL3              | D3       | R/W | I <sup>2</sup> C_ADDRESS (A5:A1)                          |                             |             |               | OTP_THRESHOLD        |                     |              |           |
| MFR_CTRL4              | D4       | R/W | FREQ (250kHz, 420kHz, 1.1MHz, or 2.1MHz)                  |                             | SLEW_RATE   | -             | OT_WARNING_THRESHOLD |                     |              |           |
| MFR_CRC_ERROR_FLAG     | D5       | R   | -   |                             |             |               |                      |                     |              | CRC_ERROR |
| OTP_CONFIGURATION_CODE | D6       | R/W | Represents the device. 0x08.                              |                             |             |               |                      |                     |              |           |
| OTP_REVISION_NUMBER    | D7       | R/W | Product suffix (e.g. 0x01)                                |                             |             |               |                      |                     |              |           |
| MFR_STATUS_MASK        | D8       | R/W | Mask the ALT pin indication when a fault or event occurs. |                             |             |               |                      |                     |              |           |

### I<sup>2</sup>C Slave Address

The default I<sup>2</sup>C slave address is 61h.

| I <sup>2</sup> C Address A7:A1        |                               |
|---------------------------------------|-------------------------------|
| Binary                                | Hex                           |
| 1100 001 (default)                    | 61h                           |
| I <sup>2</sup> C-adjustable for A5:A1 | Set by MFR_CTRL3_D, bits[7:3] |

### MFR\_BUCK\_CTRL1

Address: 0xD0

Reset value: Set by the OTP

Type: Read and write

Pages: 2 pages

| Bits   | Bit Name                    | Description   |
|--------|-----------------------------|---|
| D[7]   | DROPOUT_EN                  | 0: No dropout mode<br>1: Enable dropout mode when V <sub>IN</sub> is almost equal to V <sub>OUT</sub> (default)   |
| D[6:4] | LINE_DROP_COMPENSATION_GAIN | 000: 0.<br>001: 0.5μA/A<br>010: 1μA/A (default for buck 1 and buck 2)<br>011: 2μA/A<br>100: 4μA/A<br>101: 8μA/A   |
| D[3]   | OUTPUT_OVP_EN               | Enables output over-voltage protection (OVP). The default value is 1.<br>0: Output OVP is disabled<br>1: Output OVP is enabled                                    |
| D[2]   | HICCUP_TIMER                | Controls the buck over-current protection (OCP) hiccup timer control. The default value is 0.<br>0: The hiccup timer is 500ms<br>1: The hiccup timer is 2 seconds |

|      |                     |  |
|------|---------------------|--|
| D[1] | OUTPUT_DISCHARGE_EN | Enables the output discharge function. It is an active discharge. The LS-FET turns on to discharge the output until it reaches the negative current limit. The LS-FET turns on again when a new clock cycle starts. This discharge function is operational until the soft-start signal drops to zero. The default value is 1.<br><br>0: Disable the output discharge function<br>1: Enable the output discharge function |
| D[0] | PFM/PWM_MODE        | Sets the buck to work in auto-PFM/PWM mode or forced PWM mode. The default value is 1.<br><br>0: Auto-PFM/PWM mode<br>1: Forced PWM mode   |

### MFR\_BUCK\_CTRL2

Address: 0xD1

Reset value: Set by the OTP

Type: Read and write

Pages: Only 1 page

| Bits   | Name          | Description   |
|--------|---------------|---|
| D[7]   | GATE1_2_EN    | 0: Disable the GATE1 and GATE2 output for a lower I <sub>Q</sub><br>1: Enable the GATE1 and GATE2 output function (default)   |
| D[5:4] | PHASE_DELAY   | Selects the buck switching clock's phase delay (from buck 1 to buck 2). The default value is 10.<br><br>00: 0° phase delay<br>01: 90° phase delay<br>10: 180° phase delay<br>11: 270° phase delay |
| D[2:1] | DRV_VOLTAGE   | Sets the DRV pin output voltage. The default value is 01.<br><br>00: 5.5V<br>01: 6V<br>10: 6.2V<br>11: 6.5V   |
| D[0]   | DITHER_ENABLE | 0: No dither (default)<br>1: Enable frequency spread spectrum   |

### MFR\_CURRENT\_LIMIT

Address: 0xD2

Reset value: Set by the OTP

Type: Read and write

Page: 2 pages

This command sets the buck output constant current (CC) limit threshold.

| Name                 | IOUT_LIM                        |     |     |     |     |     |     |     |
|----------------------|---------------------------------|-----|-----|-----|-----|-----|-----|-----|
| Format               | Direct, unsigned binary integer |     |     |     |     |     |     |     |
| Bit                  | 7                               | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access               | R/W                             | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default Value (3.6A) | 72 integer                      |     |     |     |     |     |     |     |

The real-world IOUT\_OC (in A) can be calculated with Equation (9):

$$IOUT\_OC (A) = IOUT\_LIM \times 0.05 \tag{9}$$

Where IOUT\_LIM is an 8-bit unsigned binary integer of IOUT\_LIM, bitsD[7:0].



The IOOUT\_OC resolution or minimum step is 50mA. The minimum current limit value of IOOUT\_OC is 1A, and the maximum value is 6.4A. The device is not guaranteed to operate outside this setting range.

### MFR\_CTRL3

Address: 0xD3

Reset value: Set by the OTP

Type: Read and write

Page: Only 1 page

Sets the thermal shutdown trigger threshold.

| Bits   | Bit Name                 | Description  |
|--------|--------------------------|--|
| D[7:3] | I <sup>2</sup> C_ADDRESS | Sets the I <sup>2</sup> C slave address A5:A1 bit. The default value is 00001.   |
| D[2:0] | OTP_THRESHOLD            | Sets the over-temperature (OT) threshold. The default value is 010.<br>000: 140°C<br>001: 150°C<br>010: 160°C<br>011: 170°C<br>100~111: Reserved |

### MFR\_CTRL4

Address: 0xD4

Reset value: Set by the OTP

Type: Read and write

Page: Only 1 page

Sets the thermal warning trigger threshold.

| Bits   | Bit Name             | Description   |
|--------|----------------------|---|
| D[7:6] | FREQ                 | Sets the buck switching frequency. The default value is 01.<br>00: 250kHz<br>01: 420kHz<br>10: 1.1MHz<br>11: 2.1MHz   |
| D[5:4] | SLEW_RATE            | Sets the adjustable V <sub>REF</sub> slew rate. The default is 10 (V <sub>OUT_SLEW_RATE</sub> = V <sub>REF_SLEW_RATE</sub> x Feedback Ratio).<br>00: 0.08mv/μs V <sub>REF</sub> rising slew rate; 0.02mv/μs V <sub>REF</sub> falling slew rate<br>01: 0.16mv/μs V <sub>REF</sub> rising slew rate; 0.04mv/μs V <sub>REF</sub> falling slew rate<br>10: 0.4mv/μs V <sub>REF</sub> rising slew rate; 0.1mv/μs V <sub>REF</sub> falling slew rate<br>11: 0.8mv/μs V <sub>REF</sub> rising slew rate; 0.2mv/μs V <sub>REF</sub> falling slew rate |
| D[2:0] | OT_WARNING_THRESHOLD | Sets the over-temperature (OT) warning threshold. There is a 20°C hysteresis for recovery. The default value is 100.<br>000: 80°C<br>001: 90°C<br>010: 100°C<br>011: 110°C<br>100: 120°C<br>101: 130°C<br>110: 140°C<br>111: 150°C  |

**MFR\_CRC\_ERROR\_FLAG**

Address: 0xD5

Reset value: Set by the OTP

Type: Read-only

Page: Only 1 page

| Bit  | Bit Name       | Description  |
|------|----------------|--|
| D[0] | CRC_ERROR_FLAG | If a CRC error occurs while restoring the OTP memory to the I <sup>2</sup> C, this bit is set to 1.<br>If a CRC error occurs, the OTP data is discarded, and the system uses the default I <sup>2</sup> C or OTP register value. |

**MFR\_STATUS\_MASK**

Address: 0xD8

Reset value: Set by the OTP

Type: Read and write

Page: 2 pages

This register can only mask off the ALT pin behavior; the STATUS register still indicates each event.

| Bit | Bit Name        | Description   |
|-----|-----------------|---|
| 7   | VOUT_MSK        | 0: No mask (default)<br>1: Mask enabled   |
| 6   | IOUT/POUT_MSK   | 0: No mask. This bit masks IOUT_OC_FAULT, IOUT/POUT, and OC_EXIT (default)<br>1: Mask enabled   |
| 5   | INPUT_MSK       | 0: No mask<br>1: Mask enabled (default)   |
| 4   | TEMP_MSK        | Temperature-related mask bit.<br>0: No mask (default)<br>1: Mask enabled  |
| 3   | PG_STATUS#_MSK  | High-level PG mask off control bit.<br>0: No mask (default)<br>1: Mask enabled  |
| 2   | PG_ALT_EDGE_MSK | 0: No mask. The ALT pin indicates both the PG_STATUS# rising and falling edges (default)<br>1: Mask enabled. The ALT pin only indicates the PG_STATUS# falling edge, which means V <sub>OUT</sub> has gone from a suboptimal to a good transition |
| 1   | BUSY_FAULT_MASK | 0: No mask (default)<br>1: Mask enabled   |
| 0   | CML_FAULT_MASK  | 0: No mask (default)<br>1: Mask enabled   |

## APPLICATION INFORMATION

### COMPONENT SELECTION

#### Selecting the Inductor

For most applications, use an inductor with a DC current rating at least 25% greater than the maximum load current. Select an inductor with a small DC resistance for optimal efficiency. The inductor value can be calculated with Equation (10):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (10)$$

Where  $\Delta I_L$  is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be estimated with Equation (11):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (11)$$

If  $V_{IN}$  is 24V and  $V_{OUT}$  is 20V, choose L to be 8 $\mu$ H. For automotive input and PD applications, choose the inductor ripple current to be approximately 30% to 50% of the maximum load current (see Table 1). It is recommended to use a fully shielded inductor to improve EMI performance.

**Table 1: Recommended L for Different  $f_{sw}$  Values ( $D_{MAX}$  at  $\Delta I_L = 30\%$  to  $50\%$  of  $I_{O\_MAX}$ )**

| $V_{IN} / V_{OUT}$<br>(below)                        | $f_{sw} =$<br>250kHz | $f_{sw} =$<br>420kHz | $f_{sw} =$<br>1.1MHz | $f_{sw} =$<br>2.1MHz |
|--|----------------------|----------------------|----------------------|----------------------|
| $V_{IN} = 12V$<br>Buck1/2 =<br>5V<br>$I_{OUT} = 3A$  | 8.2 $\mu$ H          | 4.7 $\mu$ H          | 2.2 $\mu$ H          | 1 $\mu$ H            |
| $V_{IN} = 24V$<br>Buck1/2 =<br>20V<br>$I_{OUT} = 3A$ | 10 $\mu$ H           | 8.2 $\mu$ H          | 2.2 $\mu$ H          | 1 $\mu$ H            |

#### Selecting the Buck Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current while maintaining the DC input voltage. Use low-ESR capacitors for optimum performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For CLA applications, a 100 $\mu$ F electrolytic capacitor and two 10 $\mu$ F ceramic capacitors are recommended.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple-current rating. The RMS current in the input capacitor can be calculated with Equation (12):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (12)$$

The worst-case condition occurs at  $V_{IN} = 2V_{OUT}$ , estimated with Equation (13):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (13)$$

For simplification, choose an input capacitor with a RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using an electrolytic capacitor, place two additional high-quality ceramic capacitors as close to IN as possible. Estimate the input voltage ripple caused by the capacitance with Equation (14):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (14)$$

#### Selecting Buck Output Capacitor

The device requires an output capacitor (C2) to maintain the DC output voltage. Calculate the output voltage ripple with Equation (15):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (15)$$

Where  $L_1$  the inductor value, and  $R_{ESR}$  is the equivalent series resistance (ESR) value of the output capacitor.

For an electrolytic capacitor, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (16):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (16)$$

The MPQ4272-UC's loop compensation is optimized for ceramic output capacitors.

Generally, 4pcs 22 $\mu$ F ceramic output capacitors are recommended for good loop stability and transient response. The bandwidth is about 1/10 of the switching frequency, with a phase margin exceeding 45°.

For polymer capacitor designs, the ESR zero frequency must exceed the internal, high-

frequency compensation pole. It is recommended for the ESR to be below or equal to  $1 / (2 \times \pi \times C_{OUT} \times f_{SW})$ . Table 2 lists the recommended C<sub>IN</sub> and C<sub>OUT</sub> values for different output power ratings.

**Table 2: Recommended C<sub>IN</sub> and C<sub>OUT</sub> Values for Different Output Power Ratings at f<sub>sw</sub> = 420kHz**

| Maximum Output  | Input Capacitor  | Output Capacitor   |
|---|--|--|
| <b>V<sub>IN</sub> = 12V</b><br><b>Buck1/2 = 5V/9V,</b><br><b>I<sub>OUT</sub> = 3A</b>                         | <b>4 x 22<math>\mu</math>F + 2 x 0.1<math>\mu</math>F</b>                        | <b>4 x 22<math>\mu</math>F + 0.1<math>\mu</math>F</b>                    |
|   | 22 $\mu$ F: Ceramic capacitor, 25V   | 22 $\mu$ F: Ceramic capacitor, 25V                                       |
|   | 100nF: Ceramic capacitor, 25V  | 100nF: Ceramic capacitor, 10V  |
| <b>V<sub>IN</sub> = 24V</b><br><b>Buck1/2 = 5V, 9V,</b><br><b>15V, or 20V,</b><br><b>I<sub>OUT</sub> = 3A</b> | <b>100<math>\mu</math>F + 3 x 10<math>\mu</math>F + 2 x 0.1<math>\mu</math>F</b> | <b>100<math>\mu</math>F + 22<math>\mu</math>F + 4.7<math>\mu</math>F</b> |
|   | 100 $\mu$ F: Electrolytic capacitor, 35V   | 100 $\mu$ F: Electrolytic capacitor, ESR < 50m $\Omega$ , 25V            |
|   | 10 $\mu$ F: Ceramic capacitor, 35V   | 22 $\mu$ F: Ceramic capacitor, 25V                                       |
|   | 100nF: Ceramic capacitor, 50V  | 4.7 $\mu$ F: Ceramic capacitor, 25V                                      |

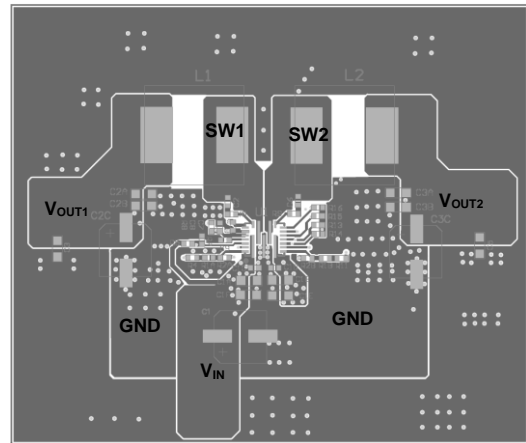
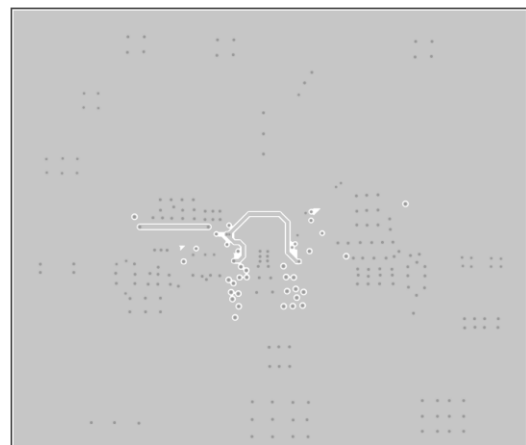
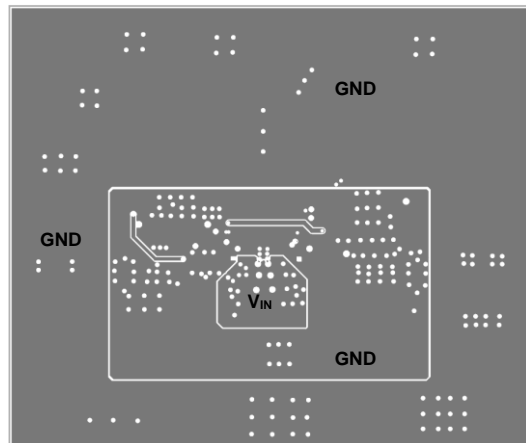
**PCB Layout Guidelines** <sup>(10)</sup>

Efficient PCB layout is critical for standard operation and thermal dissipation. For the best results, refer to Figure 15 and follow the guidelines below:

1. Use short, direct, and wide traces to connect the output nodes.
2. Place vias to GND after the output filter if required.
3. Use a large copper plane for PGND. Add multiple vias to improve thermal dissipation.
4. Connect AGND to PGND.
5. To improve EMI performance, place ceramic input decoupling capacitors as close as possible to VIN1, VIN2, and PGND.
6. Add two 0.1µF ceramic capacitors close to the VIN1 and VIN2 pins, respectively.
7. Place the input filter on the bottom layer to improve EMI performance.
8. Place the VCC decoupling capacitor as close to VCC as possible.

**Note:**

- 10) The recommended layout is based on the typical application circuit (see Figure 16 on page 38).


**Top Layer**

**Mid-Layer 1**

**Bottom Layer**
**Figure 15: Recommended PCB Layout**

## TYPICAL APPLICATION CIRCUITS

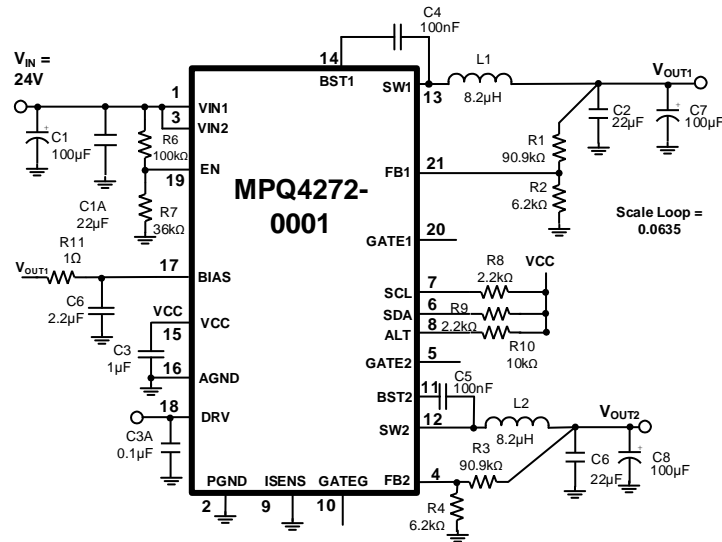


Figure 16:  $V_{IN} = 24V$ ,  $V_{OUT1} = V_{OUT2} = 3.3V$  to  $21V$  (Default Off)

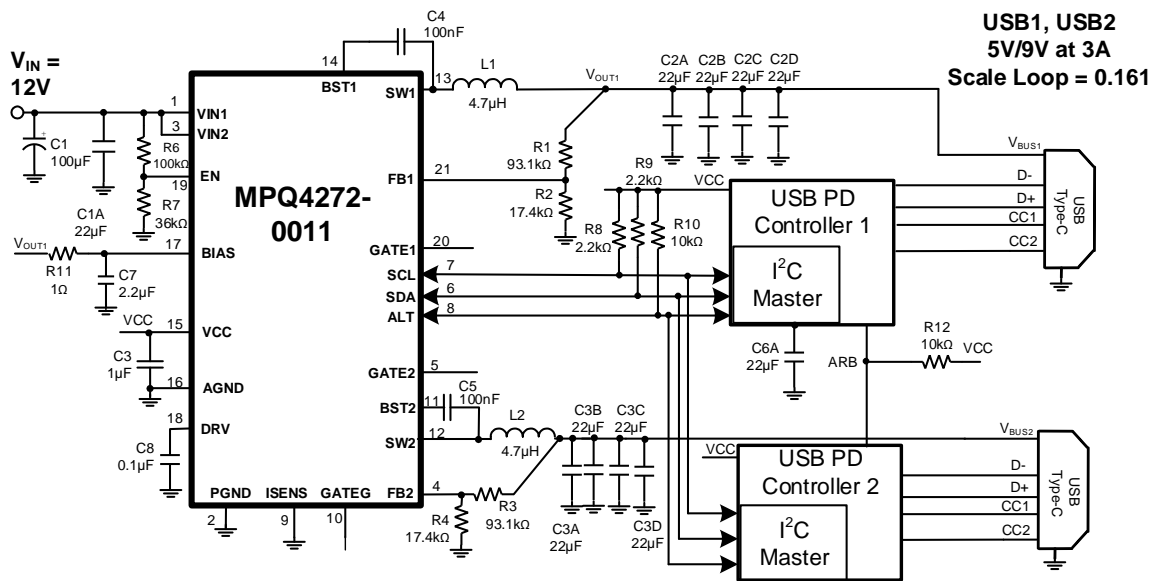


Figure 17:  $V_{IN} = 12V$ ,  $USB1 = 5V/9V$  at  $3A$ ,  $USB2 = 5V/9V$  at  $3A$

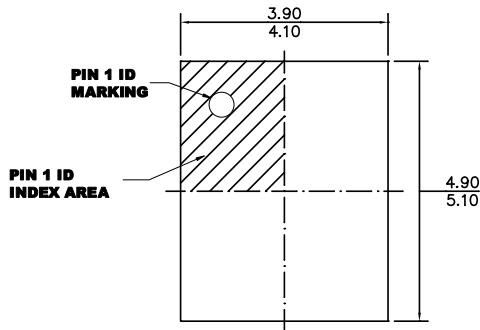
**OTP REGISTER VALUE SELECTED TABLE BY DEFAULT (MPQ4272-0001)**

| OTP Items                                     | Description  | Default Value  |
|---|--|--|
| GATE1_2_EN                                    | Enables/disables   | Disabled   |
| I <sup>2</sup> C address                      | Sets the I <sup>2</sup> C slave address, bits[A5~A1]                   | 61h  |
| FREQ  | Sets the buck switching frequency                                      | 420kHz   |
| Slew rate                                     | Sets the adjustable V <sub>REF</sub> slew rate                         | 0.4mv/μs V <sub>REF</sub> rising slew rate;<br>0.1mv/μs V <sub>REF</sub> falling slew rate |
| Dither enable                                 | Enables/disables frequency spread spectrum                             | Disabled   |
| DRV voltage                                   | Driver pin V <sub>OUT</sub> (LDO output)                               | 6V   |
| Phase delay                                   | Selects the buck switching clock's phase delay (from buck 1 to buck 2) | 0° phase delay   |
| Over-temperature protection threshold         | Thermal shutdown protection (TSD) threshold                            | 170°C  |
| Over-temperature protection warning threshold | Thermal warning threshold  | 150°C  |
| OTP configuration code                        | OTP configuration code (defined by MPS)                                | 0x01   |

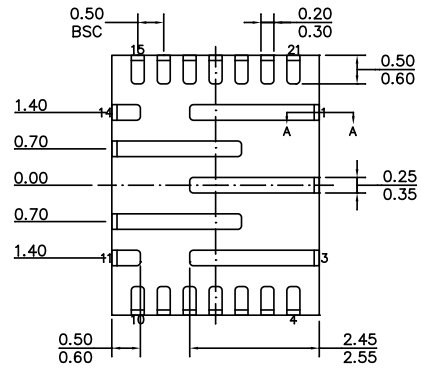
| OTP Items                               | Description   | CH1 Default Value | CH2 Default Value |
|---|---|-------------------|-------------------|
| OPERATION                               | MPQ4272 default is on or off                          | Off               | Off               |
| V <sub>OUT</sub>                        | Output voltage  | 5V                | 5V                |
| V <sub>OUT</sub> scale loop             | 1 / (V <sub>OUT</sub> feedback ratio)                 | 0.0635            | 0.0635            |
| EN OVP                                  | Enables/disables output over-voltage protection (OVP) | Enabled           | Enabled           |
| Hiccup timer                            | Over-current protection (OCP) off timer               | 500ms             | 500ms             |
| Output discharge EN                     | Enables/disables                                      | Enabled           | Enabled           |
| Dropout EN                              | Frequency decreases in dropout mode                   | Enabled           | Enabled           |
| PFM/PWM mode                            | Auto-PFM/PWM or forced PWM mode                       | Forced PWM mode   | Forced PWM mode   |
| Current limit                           | Output current limit                                  | 3.6A              | 3.6A              |
| Line drop compensation gain             | μA/A  | 0μA/A             | 0μA/A             |
| V <sub>OUT</sub> mask                   | Mask or no mask for the ALT pin indication            | Masked            | Masked            |
| I <sub>OUT</sub> /P <sub>OUT</sub> mask |   | Not masked        | Not masked        |
| Input mask                              |   | Masked            | Masked            |
| Temperature mask                        |   | Not masked        | Not masked        |
| PG_STATUS mask                          |   | Masked            | Masked            |
| PG_ALT_EDGE mask                        |   | Masked            | Masked            |
| Other mask                              |   | Masked            | Masked            |

## PACKAGE INFORMATION

### QFN-21 (4mmx5mm) with Wettable Flanks



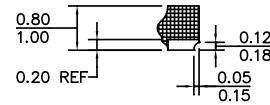
**TOP VIEW**



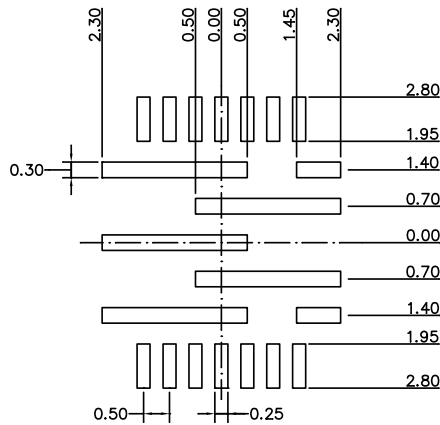
**BOTTOM VIEW**



**SIDE VIEW**



**SECTION A-A**



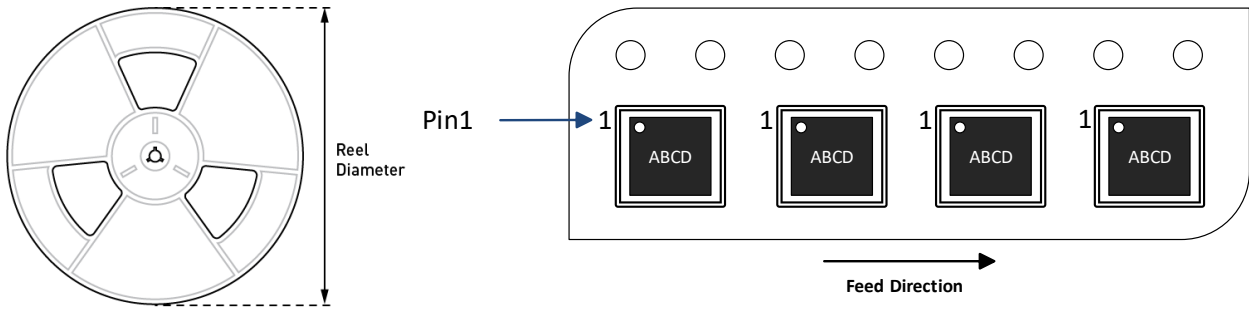
**RECOMMENDED LAND PATTERN**

#### NOTE:

- 1) LAND PATTERNS OF PINS 1, 2, AND 3, AND PINS 12 AND 13 HAVE THE SAME LENGTH AND WIDTH.
- 2) ALL DIMENSIONS ARE IN MILLIMETERS.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.



### CARRIER INFORMATION



| Part Number            | Package Description | Quantity/ Reel | Quantity/ Tube | Quantity/ Tray | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|------------------------|---------------------|----------------|----------------|----------------|---------------|--------------------|--------------------|
| MPQ4272GVE-xxxx-AEC1-Z | QFN-21 (4mmx5mm)    | 5000           | N/A            | N/A            | 13in          | 12mm               | 8mm                |