MPQ4317

45V, 7A, Low I_Q, Synchronous Step-Down Converter with Frequency Spread Spectrum, AEC-Q100 Qualified

DESCRIPTION

The MPQ4317 is a configurable-frequency, synchronous, step-down switching regulator with integrated internal high-side and low-side power MOSFETs. It provides up to 7A of highly efficient output current (I_{OUT}) with current mode control for fast loop response.

The wide 3.3V to 45V input voltage (V_{IN}) range accommodates a variety of step-down applications in automotive input environment. A 1.7µA shutdown mode quiescent current allows use in battery-powered applications.

High power conversion efficiency across a wide load range is achieved by scaling down the switching frequency (f_{SW}) under light-load conditions to reduce switching and gate driver losses.

An open-drain power good signal indicates whether the output is within 95% to 105% of its nominal voltage.

Frequency foldback helps prevent inductor current (I_L) runaway during start-up. Thermal shutdown provides reliable, fault-tolerant operation. High duty cycle and low-dropout mode are provided for automotive cold-crank conditions.

The MPQ4317 is available in a QFN-20 (4mmx4mm) package.

MPQ4317 FAMILY VERSIONS

Part Number	Output Current	Package Options
MPQ4312	2A	QFN-20 (4mmx4mm) WF (1)
MPQ4313	3A	
MPQ4314	4A	
MPQ4315	5A	
MPQ4316	6A	
MPQ4317	7A	

Note:

1) WF means wettable flank.

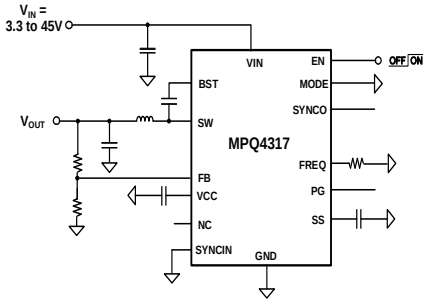
FEATURES

- Wide 3.3V to 45V Operating V_{IN} Range
- 7A Continuous Output Current (I_{OUT})
- 1.7µA Low Shutdown Supply Current
- 18µA Sleep Mode Quiescent Current
- Internal 48mΩ High-Side MOSFET (HS-FET) and 20mΩ Low-Side MOSFET (LS-FET)
- 350kHz to 1000kHz Configurable Switching Frequency (f_{SW}) for Car Battery Applications
- Can Be Synchronized to an External Clock
- Out-of-Phase Synchronized Clock Output
- Fixed Output Options: 3.3V, 5V
- Frequency Spread Spectrum (FSS) for Low EMI
- Symmetric V_{IN} for Low EMI
- Power Good (PG) Output
- External Soft Start (SS)
- 100ns Minimum On Time
- Selectable Advanced Asynchronous Modulation (AAM) Mode or Forced Continuous Conduction Mode (FCCM)
- Low-Dropout Mode
- Over-Current Protection (OCP) with Hiccup Mode
- Available in a QFN-20 (4mmx4mm) Package
- Available in a Wettable Flank Package
- Available in AEC-Q100 Grade 1

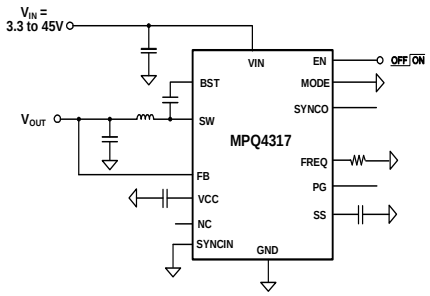
APPLICATIONS

- Automotive Infotainment
- Automotive Clusters
- Advanced Driver Assistance Systems (ADAS)
- Industrial Power Systems

TYPICAL APPLICATION



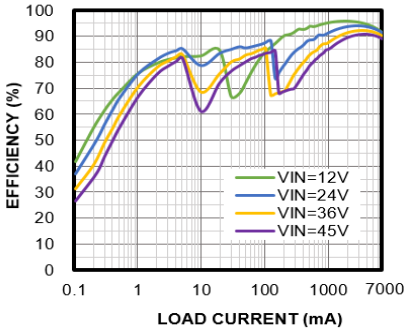
Adjustable-Output Version



Fixed-Output Version

Efficiency vs. Load Current

V_{OUT} = 5V, f_{SW} = 470kHz, L = 4.7µH (DCR = 15mΩ), AAM



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ4317GRE-AEC1***	QFN-20 (4mmx4mm)	*See Below*	1
MPQ4317GRE-33-AEC1***			
MPQ4317GRE-5-AEC1***			

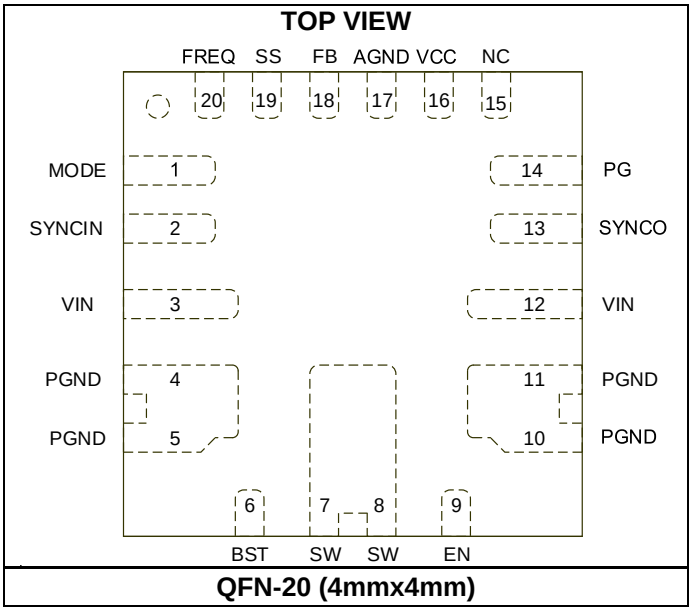
* For Tape & Reel, add suffix -Z (e.g. MPQ4317GRE-AEC1-Z).
** Moisture Sensitivity Level Rating.
*** Wettable Flank.

TOP MARKING

MPSYWW
MP4317
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
MP4317: Part number
LLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-20 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	MODE	**AAM or FCCM selection pin.** Pull this pin high to make the part operate in forced continuous conduction mode (FCCM). Pull it low to make it operate in advanced asynchronous modulation (AAM) mode under light-load conditions. Do not leave this pin floating.
2	SYNCIN	**SYNC input.** Apply a 350kHz to 1000kHz clock signal to this pin to synchronize the internal oscillator frequency to the external clock. This pin is internally high impedance. Do not float this pin under any circumstances. If used, ensure that the external sync clock has adequate pull-up and pull-down capability. It is recommended to place a ≤51kΩ resistor between the pin and GND in case the external sync clock pull-down capability is not strong enough or the pin enters a high-impedance state.
3, 12	VIN	**Input supply.** VIN supplies power to all of the internal control circuitry and the power MOSFET connected to SW. It is recommended to place a decoupling capacitor connected to ground and close to VIN to minimize switching spikes.
4, 5, 10, 11	PGND	**Power ground.**
6	BST	**Bootstrap.** BST is the positive power supply for the high-side MOSFET (HS-FET) driver connected to SW. Connect a bypass capacitor between BST and SW. See the Application Information section on page 33 to determine the size of this capacitor.
7, 8	SW	**Switch node.** SW is the output of the internal power MOSFET.
9	EN	**Enable.** Pull this pin above 1V to turn the MPQ4317 on; pull it below 0.85V to turn the chip off.
13	SYNCO	**SYNC output.** This pin outputs a clock signal that is 180° out-of-phase with the internal oscillator signal or opposite the clock signal applied at the SYNCIN pin. Float this pin if not used.
14	PG	**Power good indicator.** This pin has an open-drain output, and a pull-up resistor to power source is required if this pin is used. If the output voltage (V_{OUT}) is within 95% to 105% of the nominal voltage, this pin goes high. If V_{OUT} is above 106.5% or below 93% of the nominal voltage, it goes low.
15	NC	**Not connected.** Float this pin.
16	VCC	**Bias supply.** This pin supplies 4.9V to the internal control circuitry and gate drivers. Place a decoupling capacitor to ground close to this pin. See the Application Information section on page 33 to determine the size of this capacitor.
17	AGND	**Analog ground.**
18	FB	**Feedback input.** For the adjustable-output version of the MPQ4317, connect FB to the center point of the external resistor divider from the output to AGND to set V_{OUT}. The feedback (FB) threshold voltage is 0.815V. Place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces. For the fixed-output version, connect the FB pin directly to the output.
19	SS	**Soft start input.** Place a capacitor from SS to GND to set the soft-start time. The MPQ4317 sources 13µA from SS to the soft-start capacitor (C_{SS}) at start-up. As the SS voltage (V_{SS}) rises, the FB threshold voltage increases to limit inrush current during start-up.
20	FREQ	**Switching frequency program.** Connect a resistor from this pin to ground to set the switching frequency (f_{SW}). See the f_{SW} vs. R_{FREQ} curve in the Typical Performance Characteristics (TPC) section on page 15 to set the frequency.

ABSOLUTE MAXIMUM RATINGS (2)

VIN, EN .....-0.3V to +50V
SW ..... -0.3V to $V_{IN(MAX)}$ + 0.3V
BST ..... V_{SW} + 5.5V
All other pins .....-0.3V to +5.5V
Continuous power dissipation (T_A = 25°C) (3) (5)
QFN-20 (4mmx4mm) 5.4W
Operating junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

Electrostatic Discharge (ESD) Rating

Human body model (HBM) .....±2kV
Charged device model (CDM) ..... ±750V

Recommended Operating Conditions

Supply voltage (V_{IN}) .....3.3V to 45V
Output voltage (V_{OUT}) ..... 0.815V to 0.95 x V_{IN}
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-20 (4mmx4mm)		
JESD51-7 (4)	44	9 °C/W
EVQ4317-R-00A (5)	23	2.5 °C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
5) Measured on an MPS standard EVB: 9cmx9cm, 2oz. copper thickness, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IN} under-voltage lockout (UVLO) rising threshold	IN_{UVLO_RISING}		2.8	3.0	3.2	V
V_{IN} UVLO falling threshold	$IN_{UVLO\_FALLING}$		2. 5	2.7	2.9	V
V_{IN} UVLO hysteresis	IN_{UVLO_HYS}			280		mV
VCC voltage	V_{CC}	I_{VCC} = 0A	4.6	4.9	5.2	V
VCC regulation		I_{VCC} = 30mA		1	4	%
VCC current limit	I_{LIMIT_VCC}	V_{CC} = 4V	100			mA
V_{IN} quiescent current	I_Q	FB = 0.85V, no load, (sleep mode)		18	26	µA
V_{IN} quiescent current (switching) (6)	I_{Q_ACTIVE}	MODE = GND (AAM), switching, no load, R_{FB_UP} = 1MΩ, R_{FB_DOWN} = 324kΩ		20		µA
		MODE = HIGH (FCCM), switching, f_{SW} = 2MHz, no load		40		mA
		MODE = HIGH(FCCM), switching, f_{SW} = 470kHz, no load		9.5		mA
V_{IN} shutdown current	I_{SHDN}	EN = 0V		1.7	3.5	µA
FB reference voltage	V_{FB}	V_{IN} = 3.3V to 45V, T_J = 25°C	807	815	823	mV
		V_{IN} = 3.3V to 45V	799	815	831	mV
Output voltage accuracy of MPQ4317-33	V_{OUT}	T_J = 25°C	3234	3300	3366	mV
			3201	3300	3399	mV
Output voltage accuracy of MPQ4317-5	V_{OUT}	T_J = 25°C	4900	5000	5100	mV
			4850	5000	5150	mV
FB current	I_{FB}	V_{FB} = 0.85V, adjustable-output version	-50	0	+50	nA
Switching frequency	f_{SW}	R_{FREQ} = 62kΩ	420	470	520	kHz
		R_{FREQ} = 26.1kΩ	820	1000	1180	
Minimum on time (6)	t_{ON_MIN}			100		ns
Minimum off time (6)	t_{OFF_MIN}			80		ns
SYNCIN voltage rising threshold	V_{SYNC_RISING}		1.8			V
SYNCIN voltage falling threshold	$V_{SYNC\_FALLING}$				0.4	V
SYNCIN clock range	f_{SYNC}	External clock	350		1000	kHz
SYNCO high voltage	V_{SYNCO_HIGH}	I_{SYNCO} = -1mA	3.3	4.5		V
SYNCO low voltage	V_{SYNCO_LOW}	I_{SYNCO} = 1mA			0.4	V
SYNCO phase shift		Tested under SYNCIN		180		deg
High-side (HS) current limit	I_{LIMIT}	Duty cycle = 30%	10	13	16	A
Low-side (LS) valley current limit	I_{LIMIT_VALLEY}		8	10	12	A

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Zero-current detection (ZCD) current	I_{ZCD}	AAM	-0.15	0.1	+0.35	A
LS reverse current limit	$I_{LIMIT\_REVERSE}$	FCCM	2.0	4.5	7.0	A
Switch leakage current	I_{SW_LKG}			0.01	1	µA
HS-FET on resistance	R_{ON_HS}	V_{BST} - V_{SW} = 5V		48	80	mΩ
LS-FET on resistance	R_{ON_LS}	V_{CC} = 5V		20	40	mΩ
Soft-start current	I_{SS}	V_{SS} = 0V	8	13	19	µA
EN rising threshold	V_{EN_RISING}		0.8	1.0	1.2	V
EN falling threshold	$V_{EN\_FALLING}$		0.65	0.85	1.05	V
EN hysteresis voltage	V_{EN_HYS}			190		mV
MODE rising threshold	V_{MODE_RISING}		1.8			V
MODE falling threshold	$V_{MODE\_FALLING}$				0.4	V
PG rising threshold (V_{FB} / V_{REF})	PG_{RISING}	V_{FB} rising	92%	95%	98%	V_{REF}
		V_{FB} falling	102%	105%	108%	
PG falling threshold (V_{FB} / V_{REF})	$PG_{FALLING}$	V_{FB} falling	90.5%	93.5%	96.5%	
		V_{FB} rising	103.5%	106.5%	109.5%	
PG output voltage low	V_{PG_LOW}	I_{SINK} = 1mA		0.1	0.3	V
PG rising delay	$t_{PG\_R\_DELAY}$			35		µs
PG falling delay	$t_{PG\_F\_DELAY}$			35		µs
Thermal shutdown (6)	T_{SD}			170		°C
Thermal shutdown hysteresis (6)	T_{SD_HYS}			20		°C

Note:

6) Derived from bench characterization. Not tested in production.

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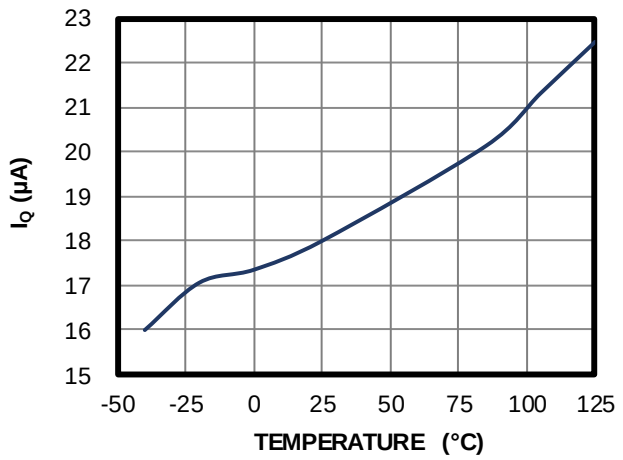
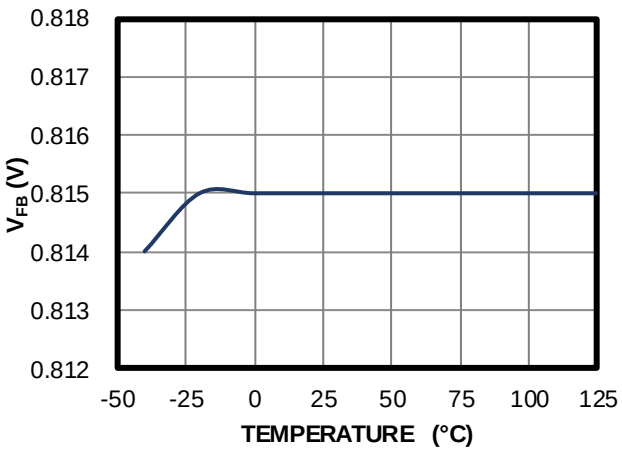
TYPICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

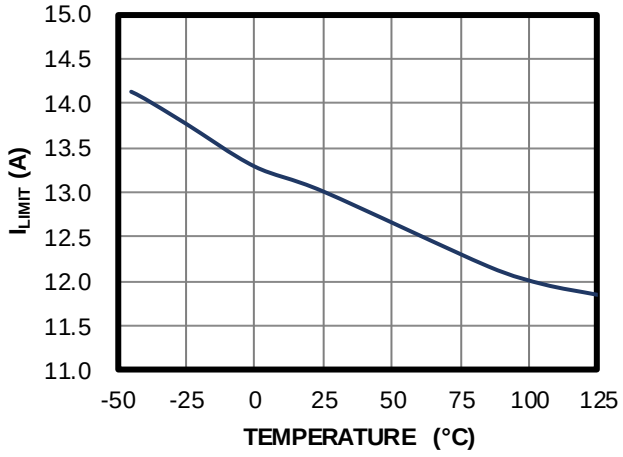
I_Q vs. Temperature



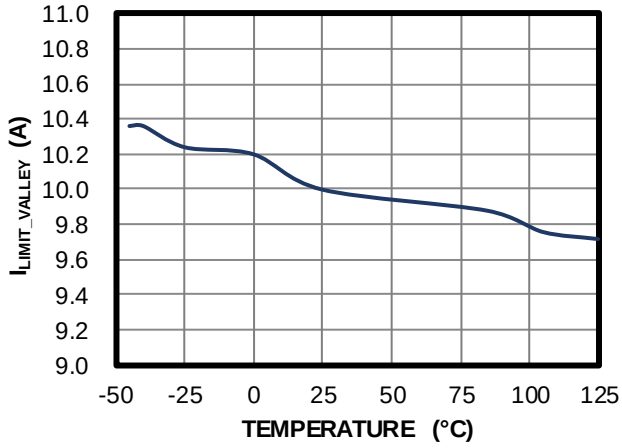
V_{FB} vs. Temperature



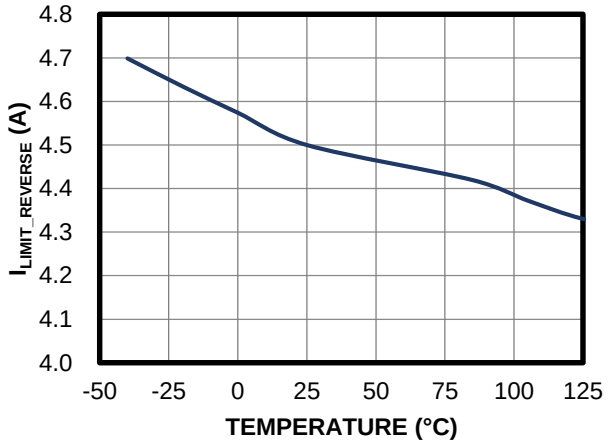
I_{LIMIT} vs. Temperature



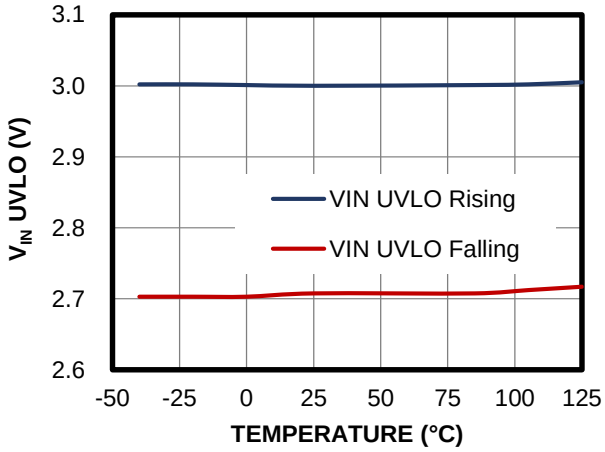
Valley Current Limit vs. Temperature



Reverse Current Limit vs. Temperature



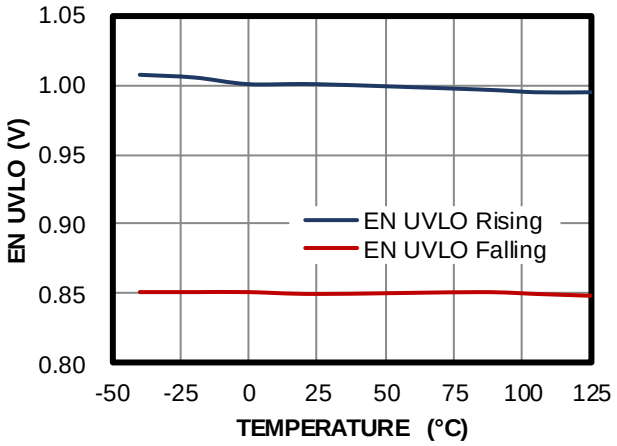
V_{IN} UVLO vs. Temperature



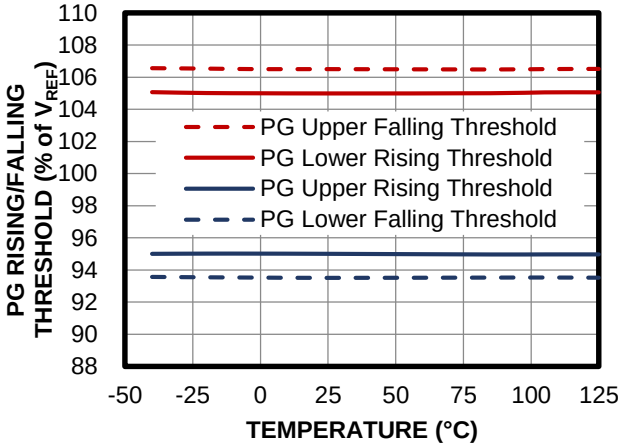
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

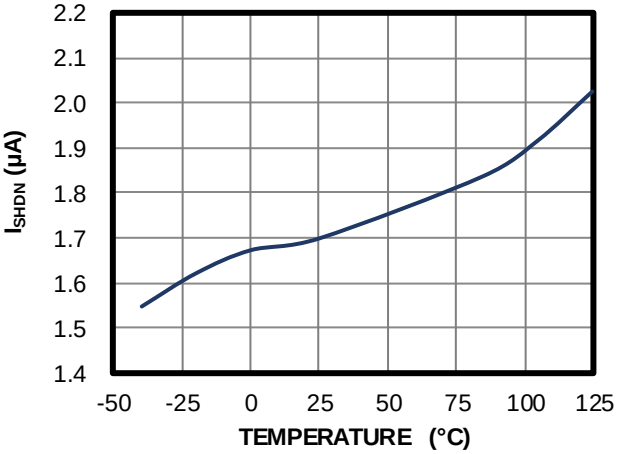
EN UVLO Threshold vs. Temperature



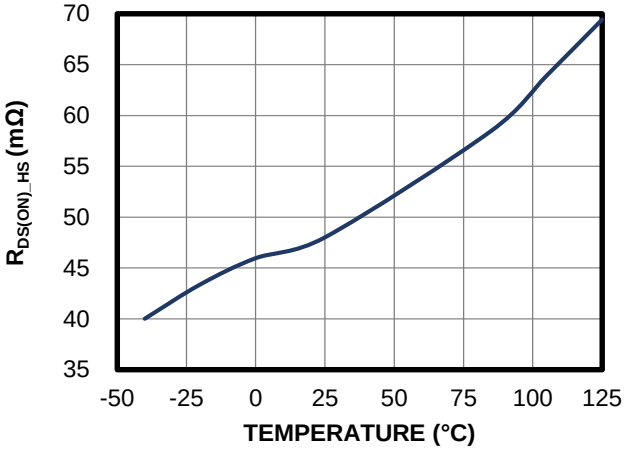
PG Rising/Falling Threshold vs. Temperature



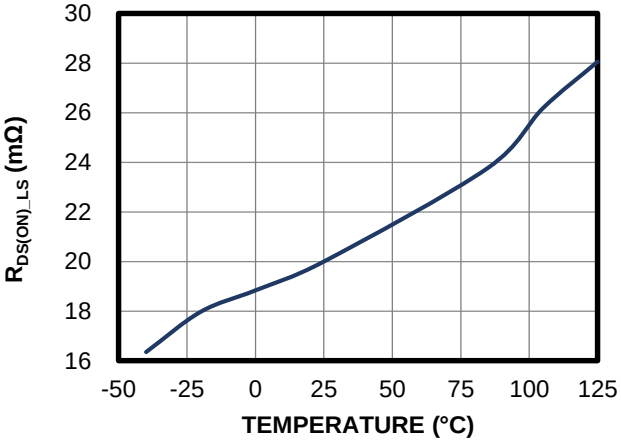
Shutdown Current vs. Temperature



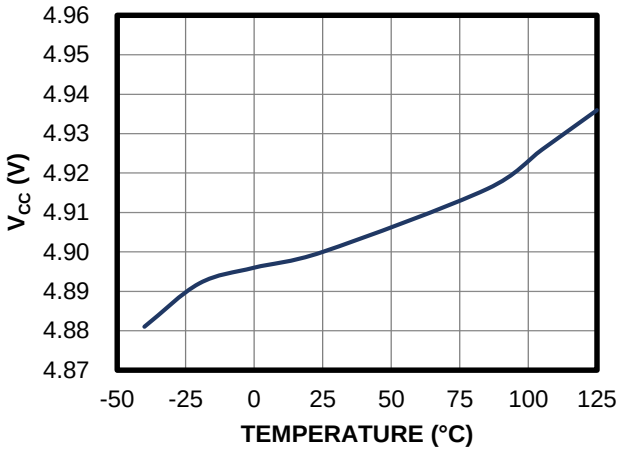
$R_{DS(ON)\_HS}$ vs. Temperature



$R_{DS(ON)\_LS}$ vs. Temperature



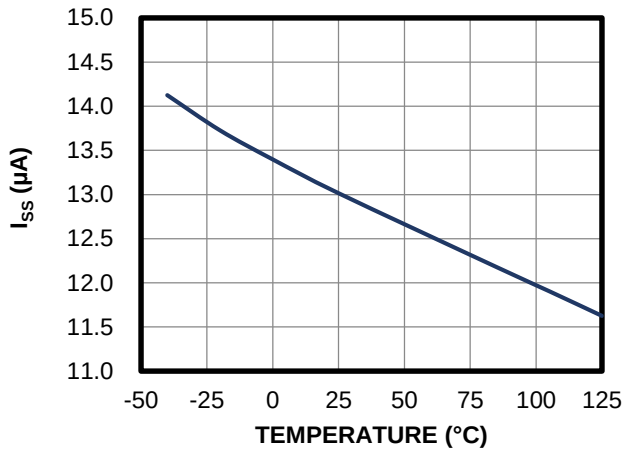
V_{CC} vs. Temperature



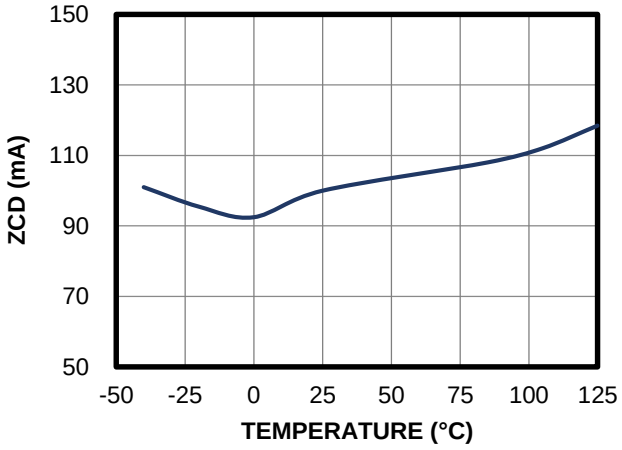
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Soft-Start Current vs. Temperature

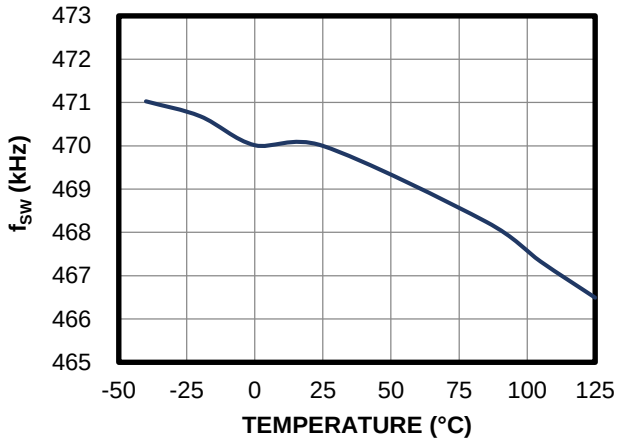


ZCD vs. Temperature



f_{SW} vs. Temperature

R_{FREQ} = 62kΩ

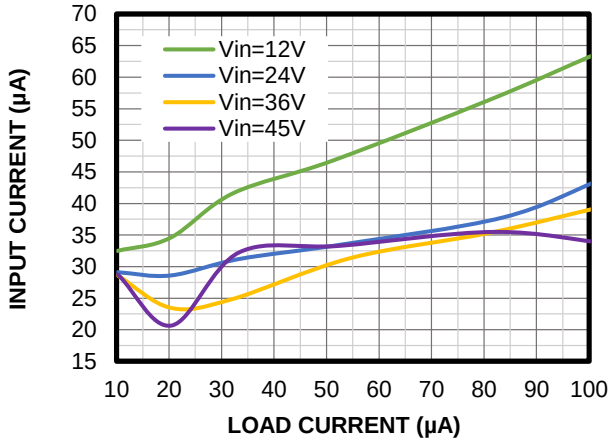


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH (7), f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

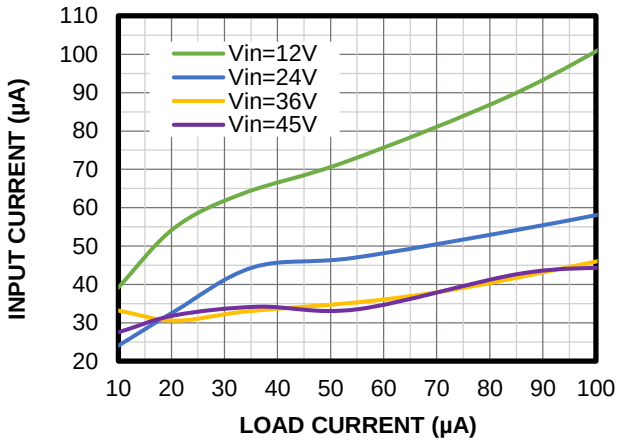
Input Current vs. Load Current

AAM, V_{OUT} = 3.3V



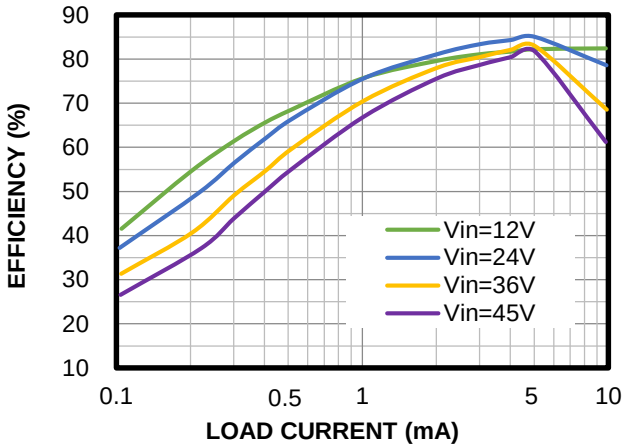
Input Current vs. Load Current

AAM, V_{OUT} = 5V



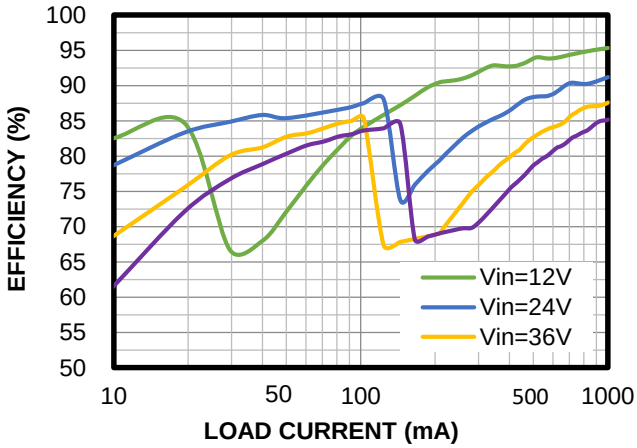
Efficiency vs. Load Current

AAM, V_{OUT} = 3.3V



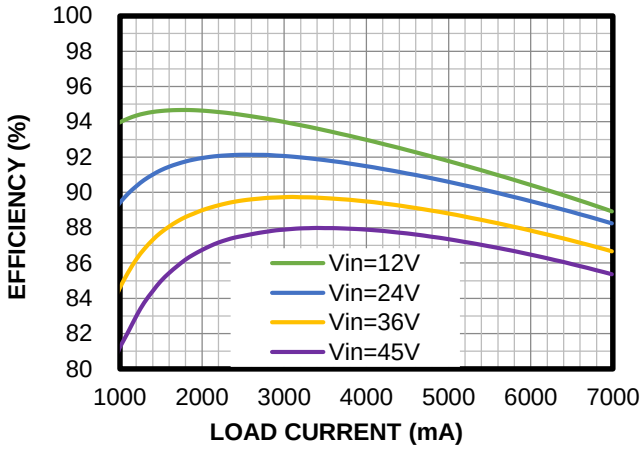
Efficiency vs. Load Current

AAM, V_{OUT} = 3.3V



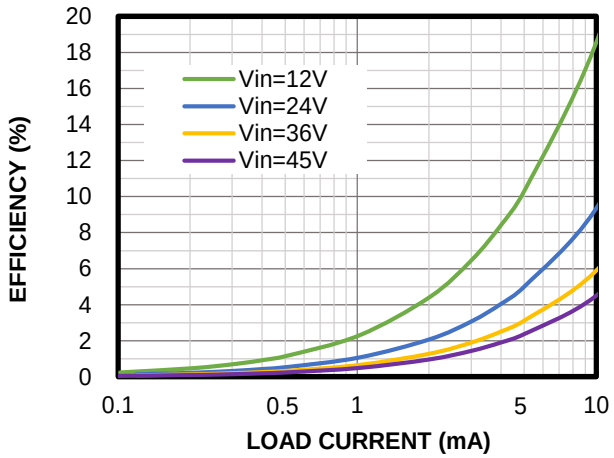
Efficiency vs. Load Current

AAM, V_{OUT} = 3.3V



Efficiency vs. Load Current

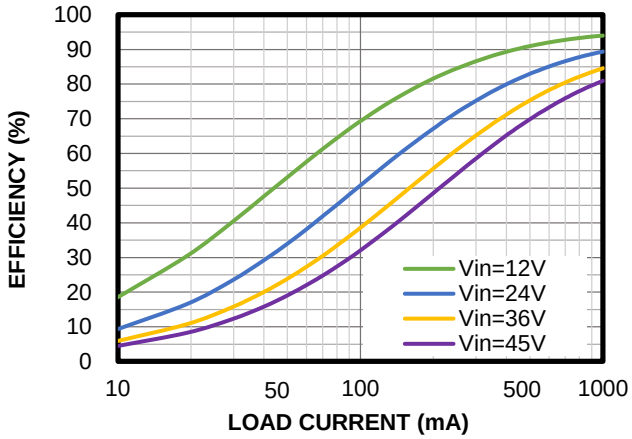
FCCM, V_{OUT} = 3.3V



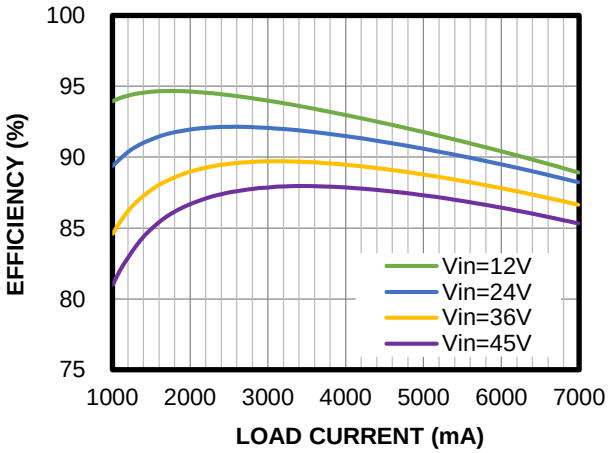
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH (7), f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

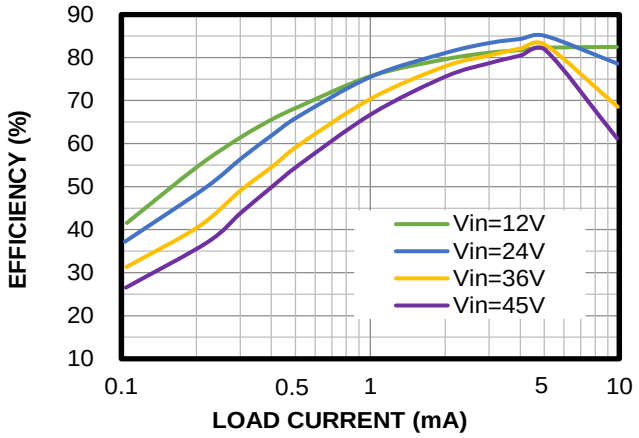
Efficiency vs. Load Current
FCCM, V_{OUT} = 3.3V



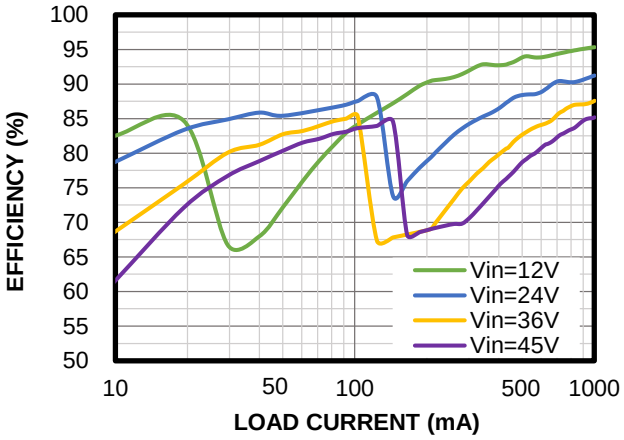
Efficiency vs. Load Current
FCCM, V_{OUT} = 3.3V



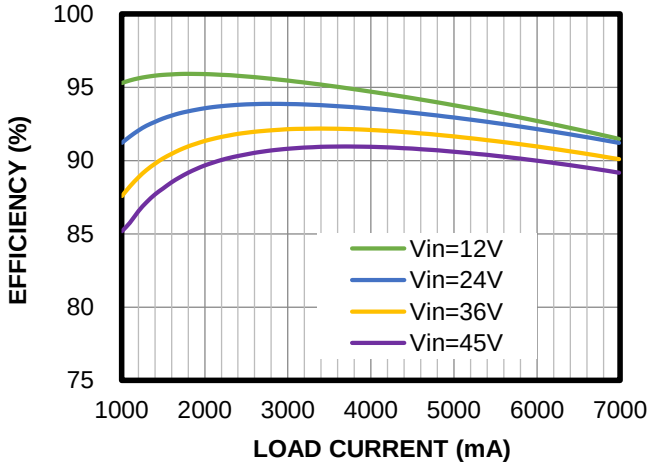
Efficiency vs. Load Current
AAM, V_{OUT} = 5V



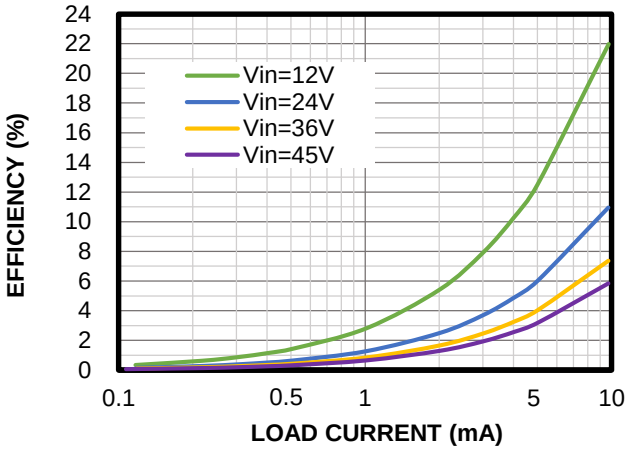
Efficiency vs. Load Current
AAM, V_{OUT} = 5V



Efficiency vs. Load Current
AAM, V_{OUT} = 5V



Efficiency vs. Load Current
FCCM, V_{OUT} = 5V

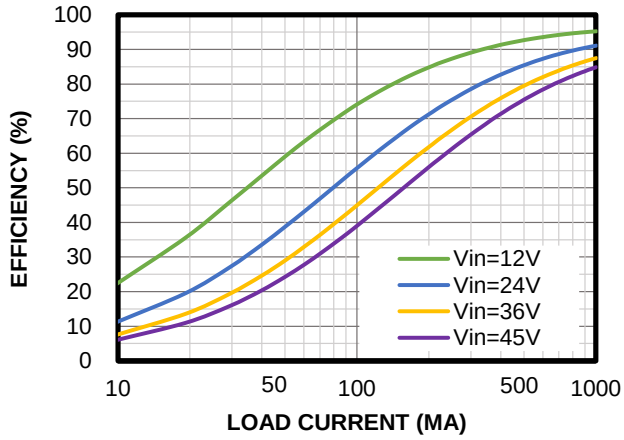


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH (7), f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

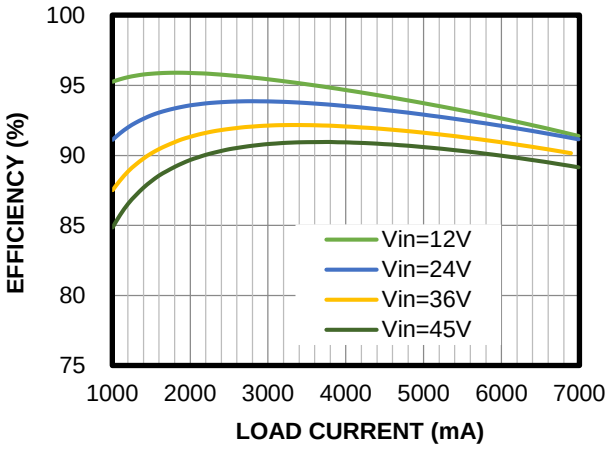
Efficiency vs. Load Current

FCCM, V_{OUT} = 5V



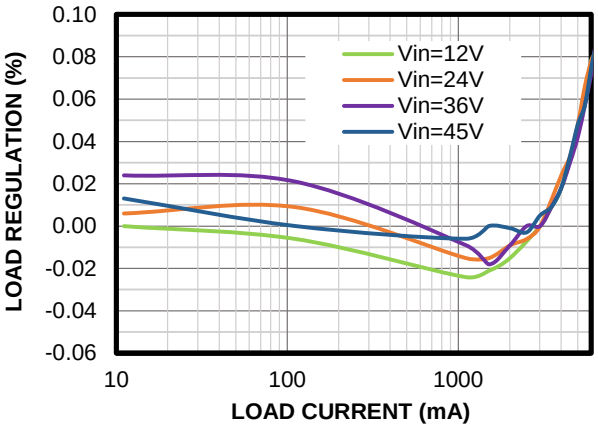
Efficiency vs. Load Current

FCCM, V_{OUT} = 5V



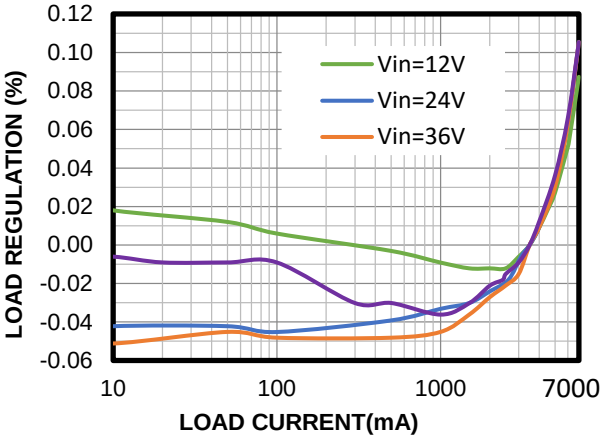
Load Regulation

AAM, V_{OUT} = 3.3V



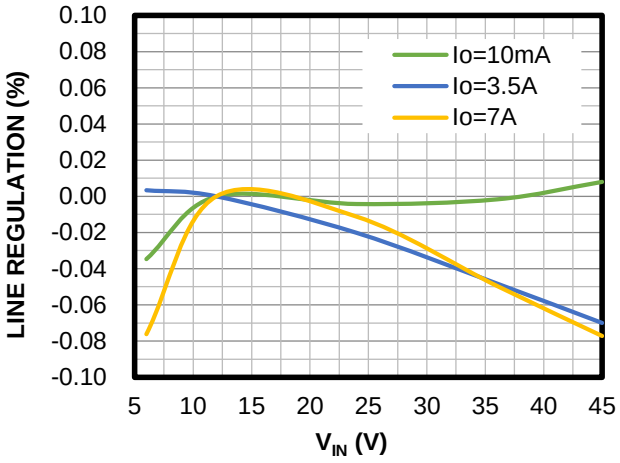
Load Regulation

FCCM, V_{OUT} = 3.3V



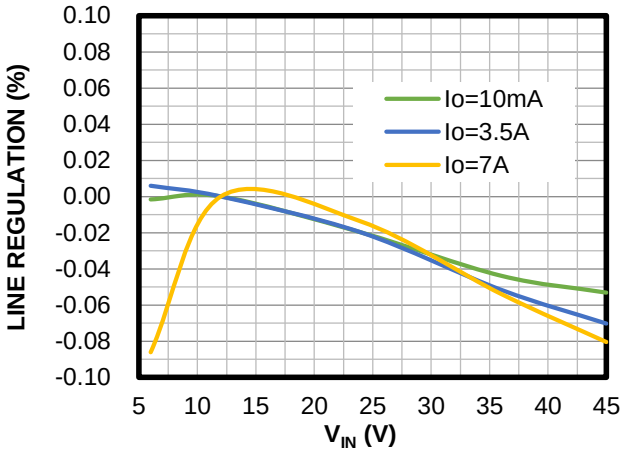
Line Regulation

AAM, V_{OUT} = 3.3V



Line Regulation

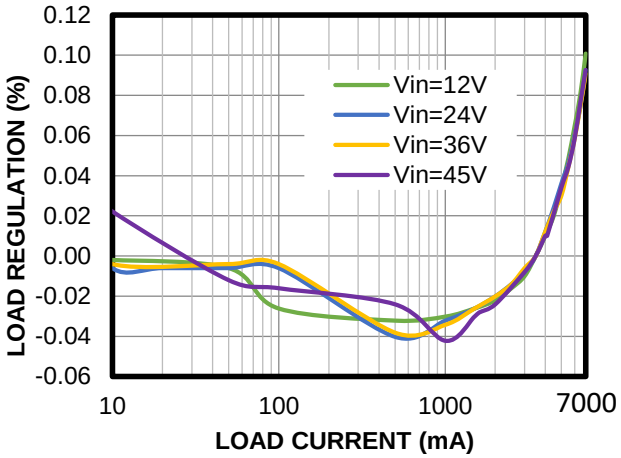
FCCM, V_{OUT} = 3.3V



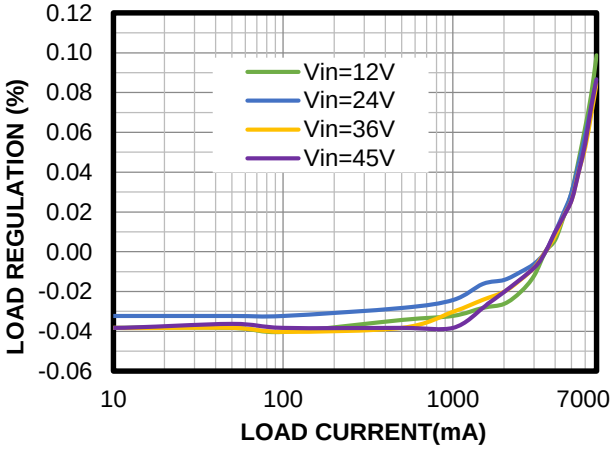
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH [7], f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

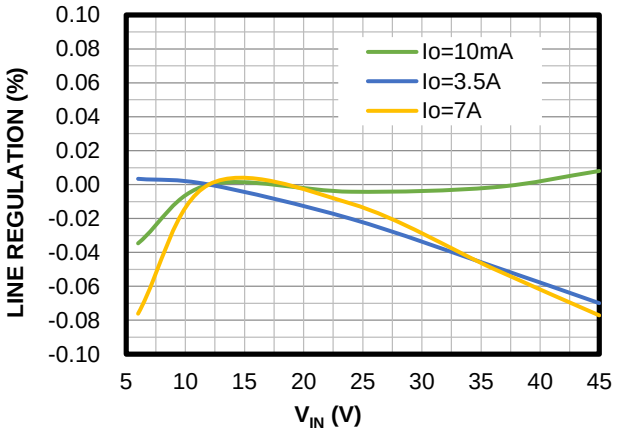
Load Regulation
AAM, V_{OUT} = 5V



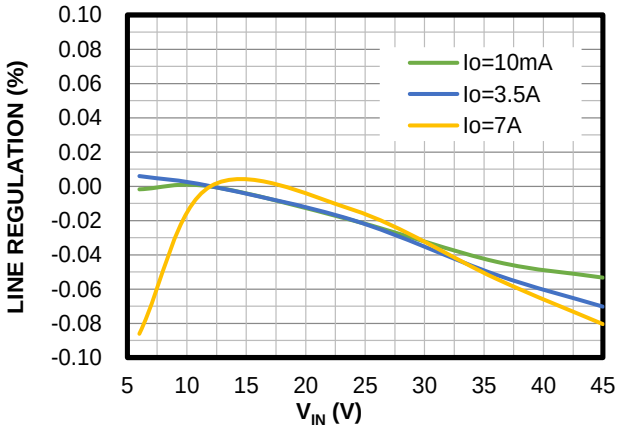
Load Regulation
FCCM, V_{OUT} = 5V



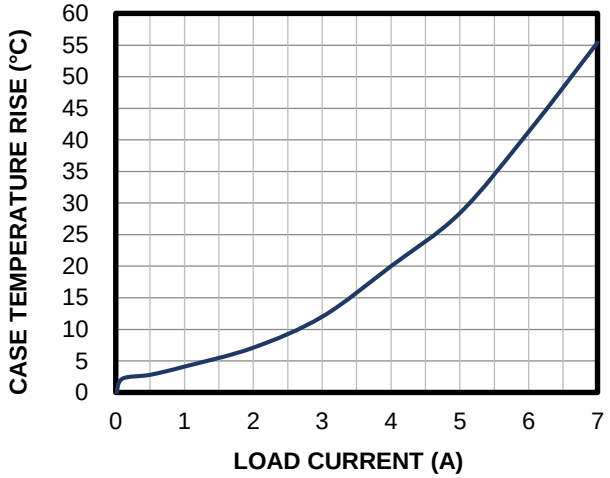
Line Regulation
AAM, V_{OUT} = 5V



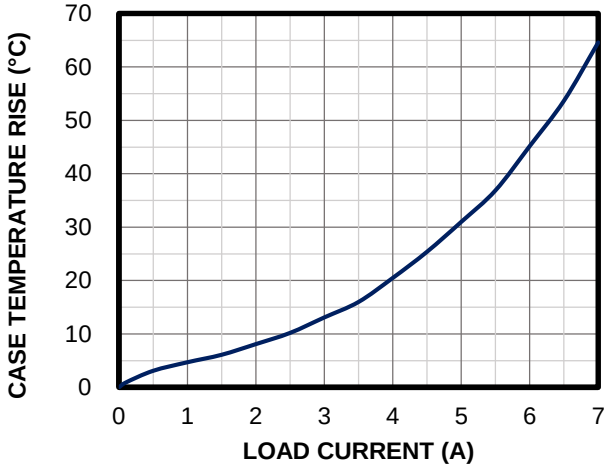
Line Regulation
FCCM, V_{OUT} = 5V



Case Temperature Rise
V_{OUT} = 3.3V



Case Temperature Rise
V_{OUT} = 5V

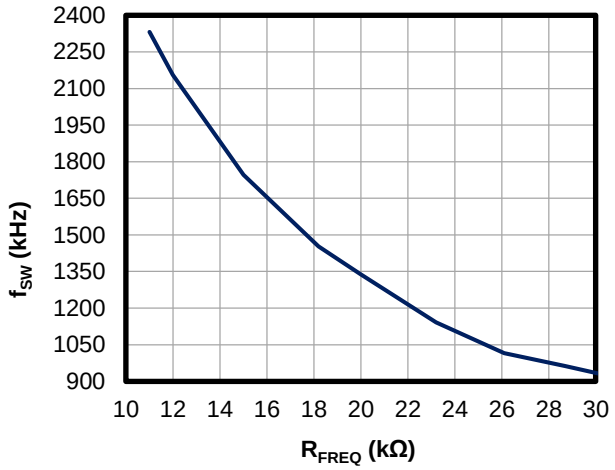


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH (7), f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

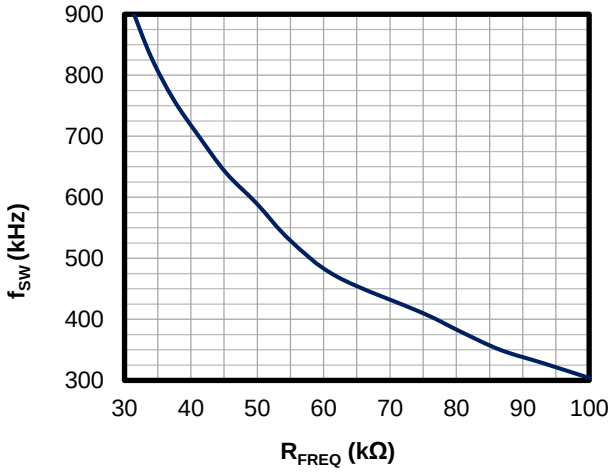
f_{SW} vs. R_{FREQ}

R_{FREQ} = 10kΩ to 30kΩ

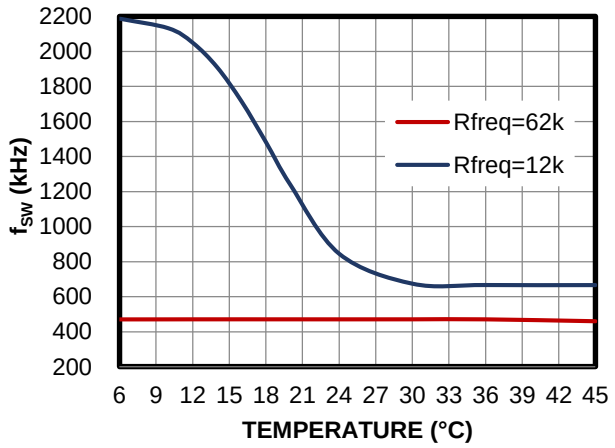


f_{SW} vs. R_{FREQ}

R_{FREQ} = 30kΩ to 100kΩ

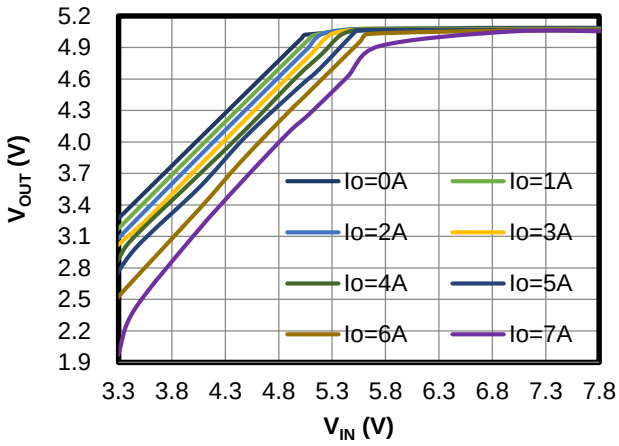


f_{SW} vs. V_{IN}



Low-Dropout Mode

V_{OUT} = 5V

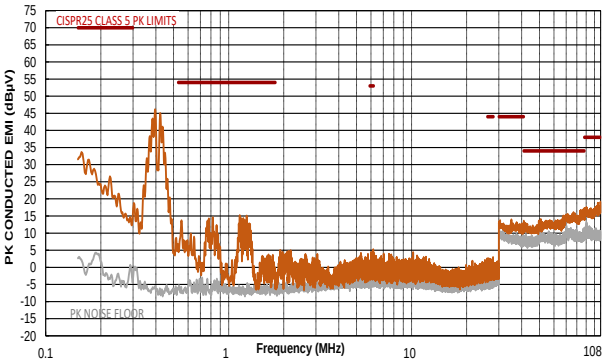


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 7A, L = 4.7µH (7), f_{SW} = 410kHz, T_A = 25°C, unless otherwise noted.(8)

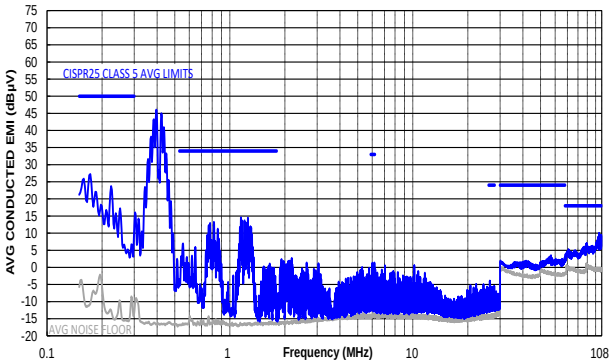
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



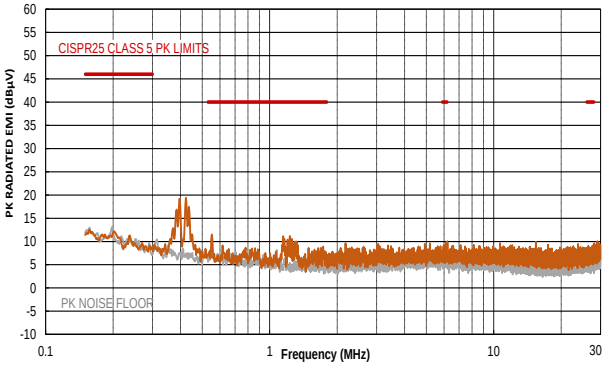
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



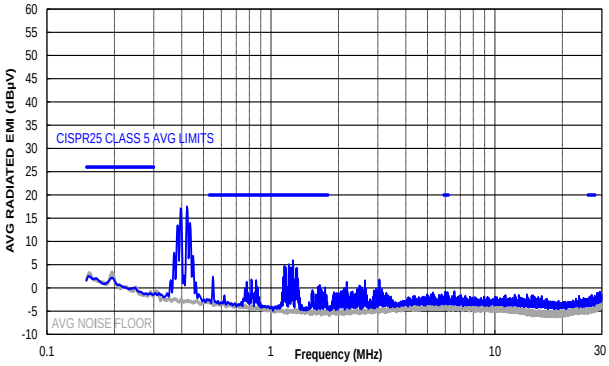
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



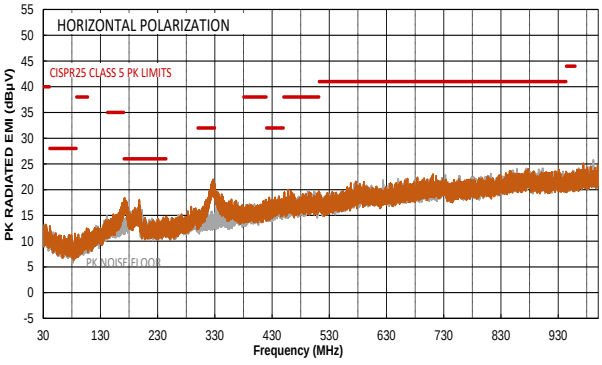
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



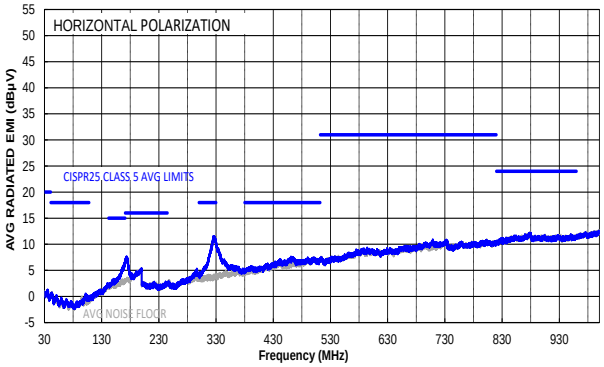
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz

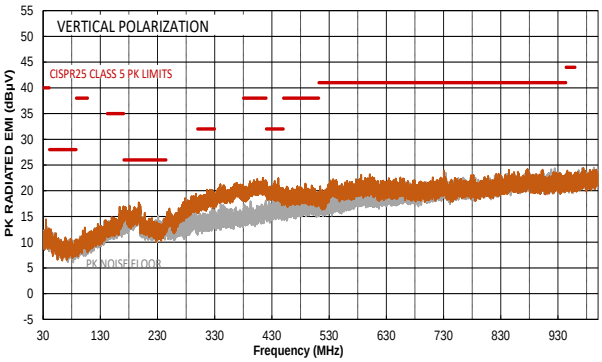


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 7A, L = 4.7µH (7), f_{SW} = 410kHz, T_A = 25°C, unless otherwise noted.(8)

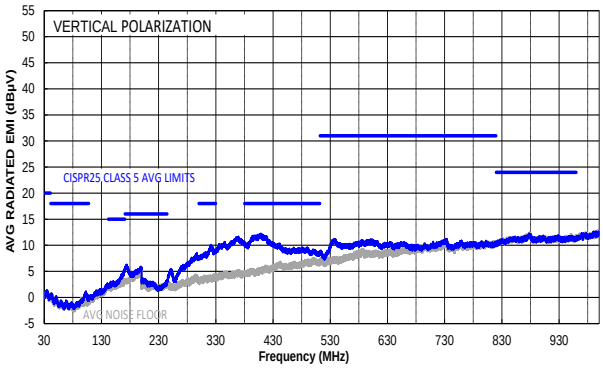
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



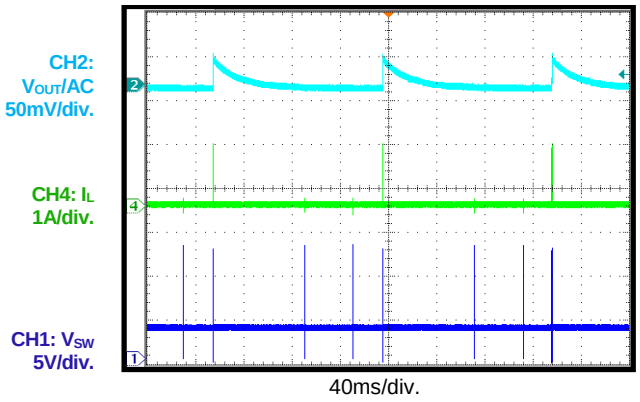
Note:

7) Inductor part number: XAL6060-472MEC. DCR = 15mΩ.
8) The EMC test results are based on the application circuit with EMI filters (see Figure 12).

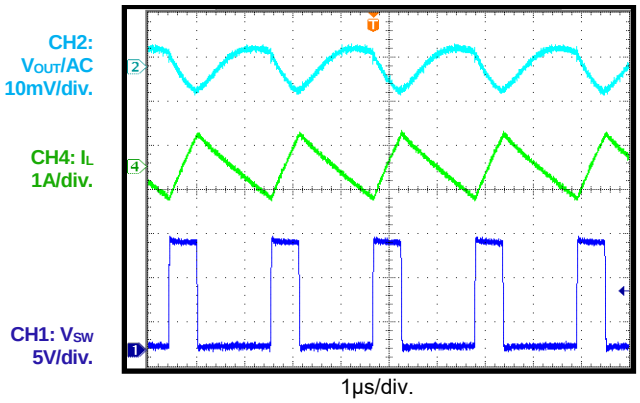
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

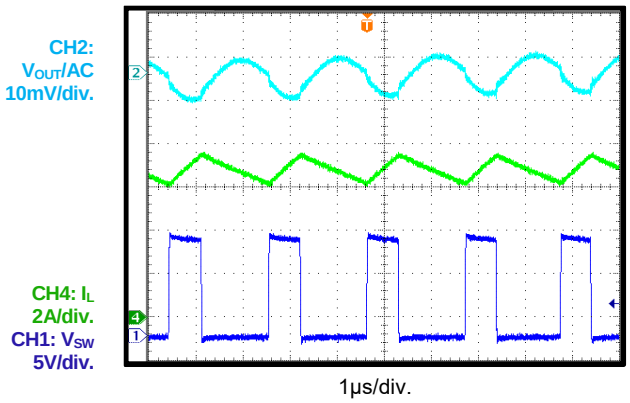
Steady State
I_{OUT} = 0A, AAM



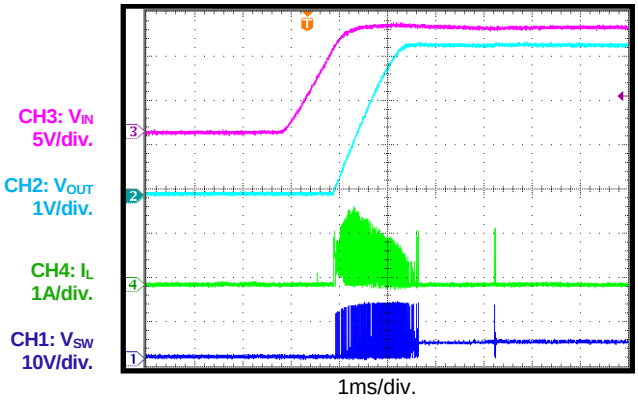
Steady State
I_{OUT} = 0A, FCCM



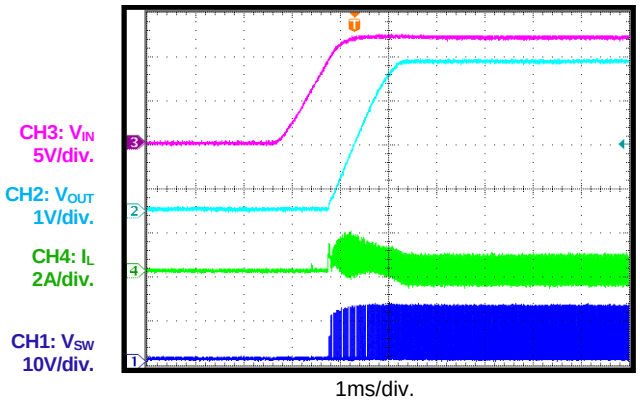
Steady State
I_{OUT} = 7A



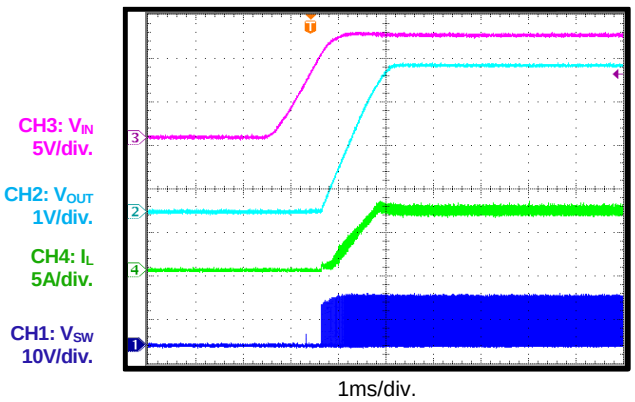
Start-Up through VIN
I_{OUT} = 0A, AAM



Start-Up through VIN
I_{OUT} = 0A, FCCM



Start-Up through VIN
I_{OUT} = 7A

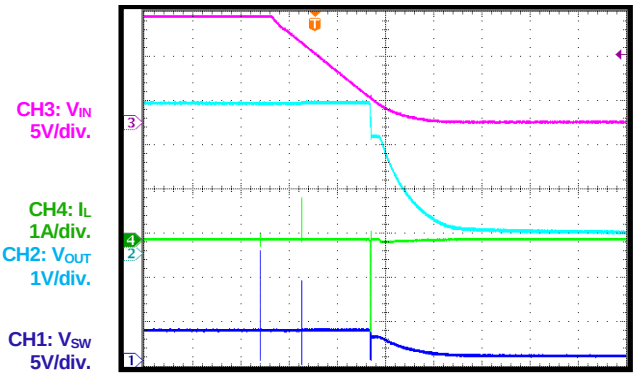


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

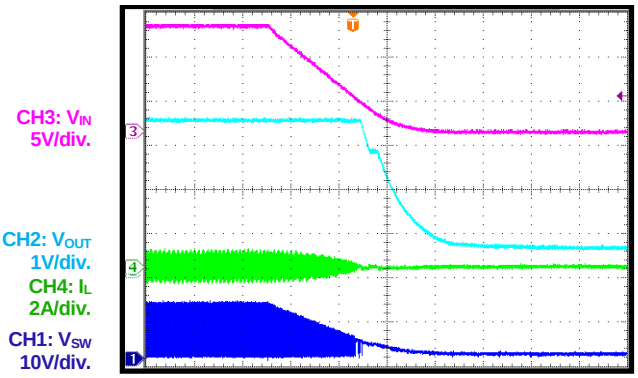
Shutdown through VIN

I_{OUT} = 0A, AAM



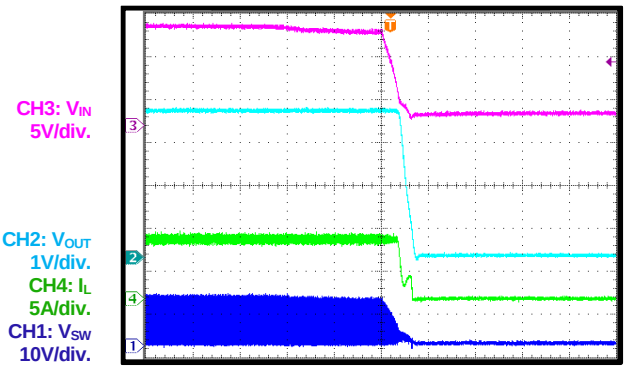
Shutdown through VIN

I_{OUT} = 0A, FCCM



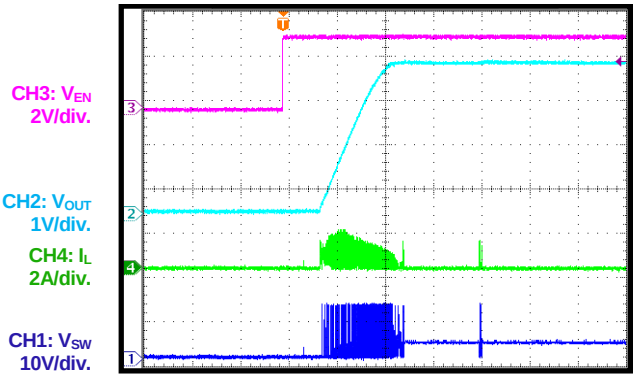
Shutdown through VIN

I_{OUT} = 7A



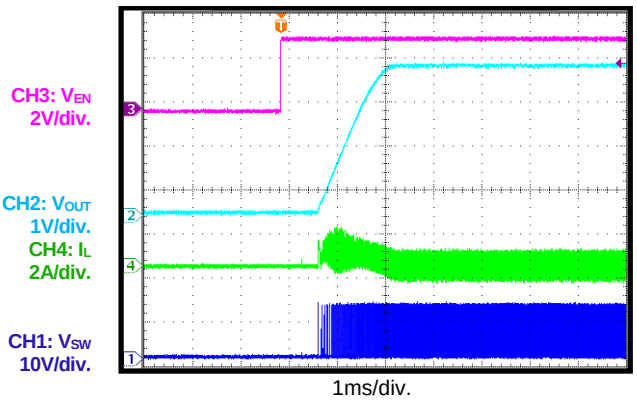
Start-Up through EN

I_{OUT} = 0A, AAM



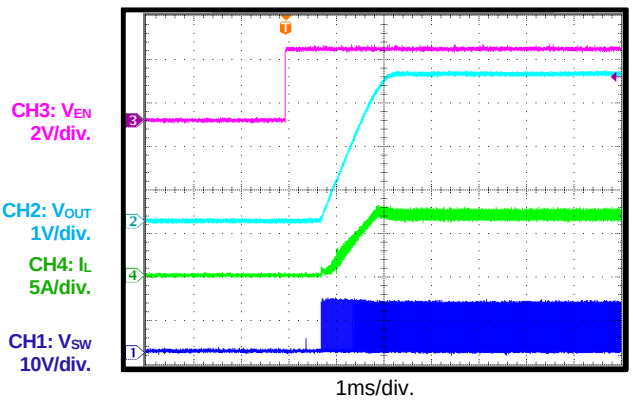
Start-Up through EN

I_{OUT} = 0A, FCCM



Start-Up through EN

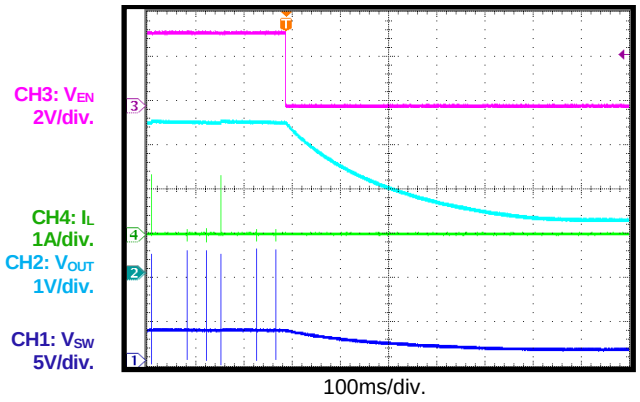
I_{OUT} = 7A



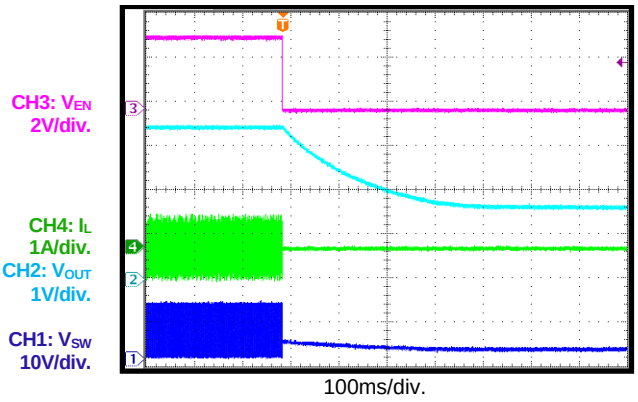
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

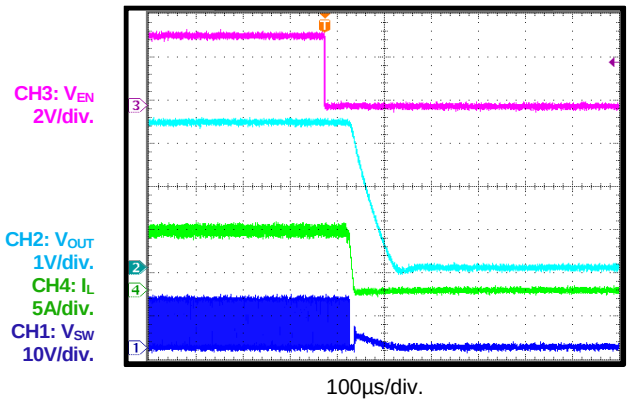
Shutdown through EN
I_{OUT} = 0A, AAM



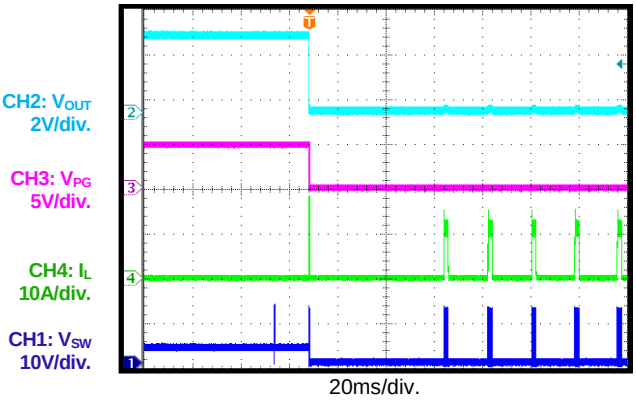
Shutdown through EN
I_{OUT} = 0A, FCCM



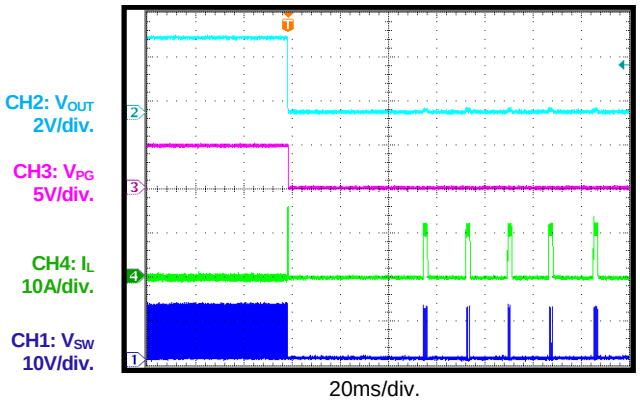
Shutdown through EN
I_{OUT} = 7A



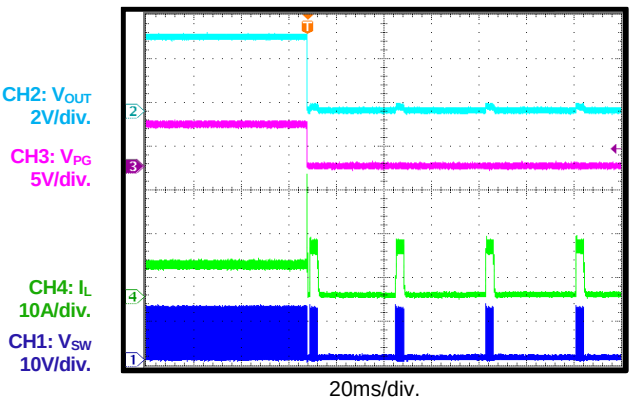
SCP Entry
I_{OUT} = 0A, AAM



SCP Entry
I_{OUT} = 0A, FCCM



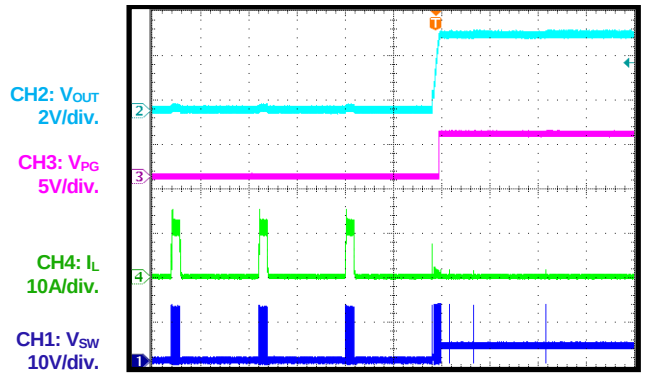
SCP Entry
I_{OUT} = 7A



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

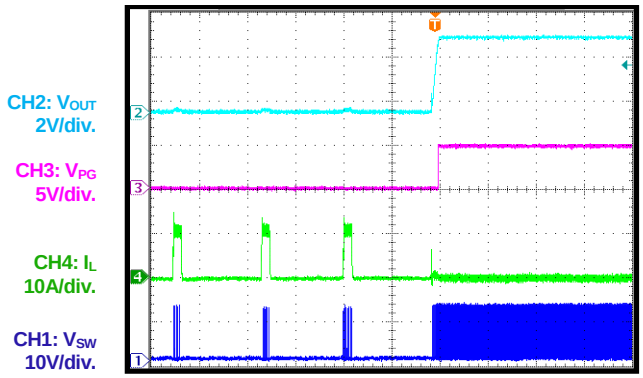
V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

SCP Recovery
I_{OUT} = 0A, AAM



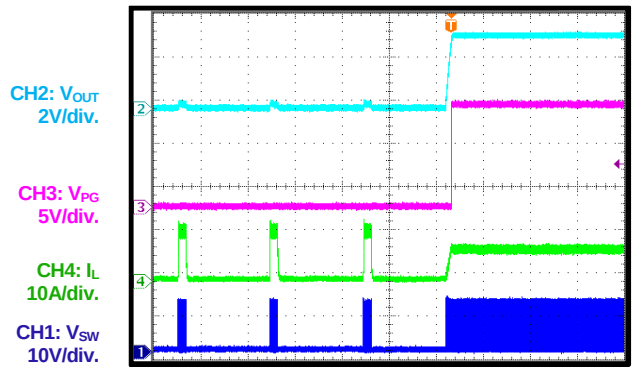
10ms/div.

SCP Recovery
I_{OUT} = 0A, FCCM



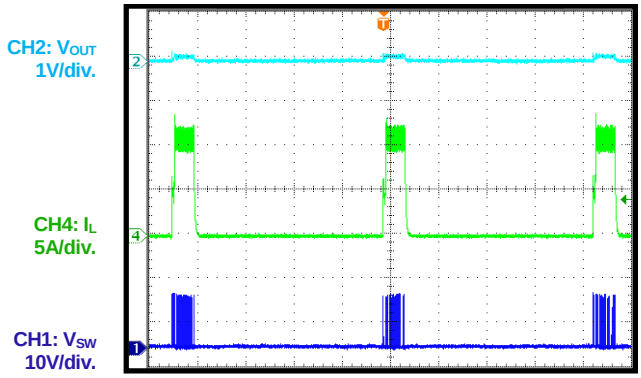
10ms/div.

SCP Recovery
I_{OUT} = 7A



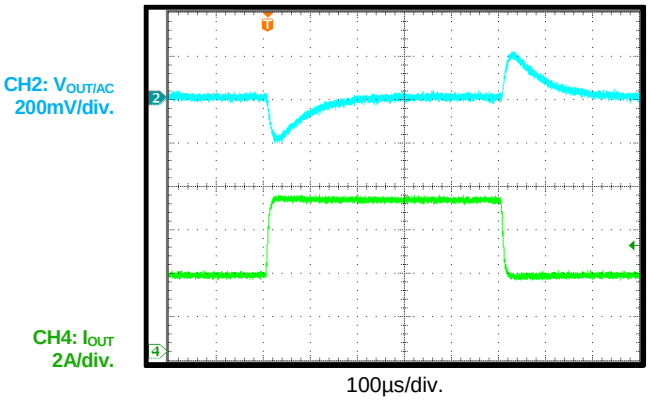
10ms/div.

SCP Steady State



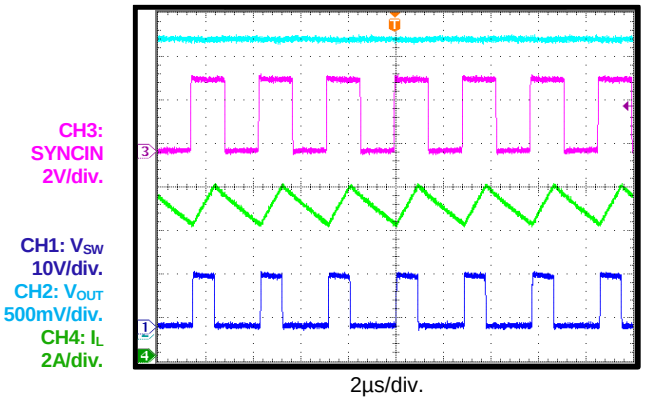
4ms/div.

Load Transient
I_{OUT} = 3.5A to 7A, 1.6A/µs



100µs/div.

SYNCIN Operation
I_{OUT} = 7A, SYNC frequency = 350kHz



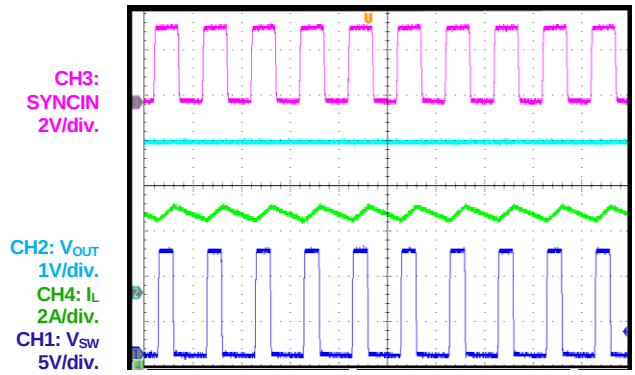
2µs/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

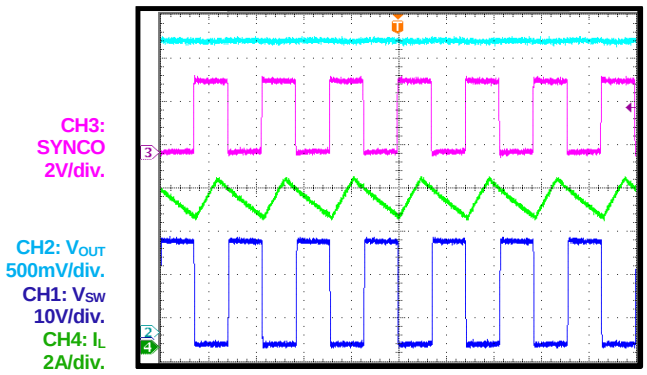
SYNCIN Operation

I_{OUT} = 7A, SYNC frequency = 1000kHz



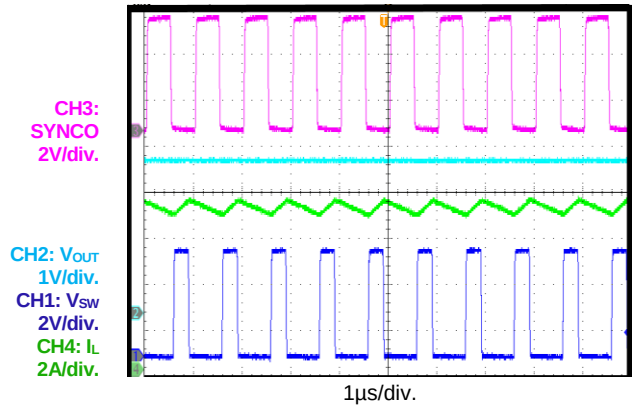
SYNCO Operation

I_{OUT} = 7A, SYNC frequency = 350kHz



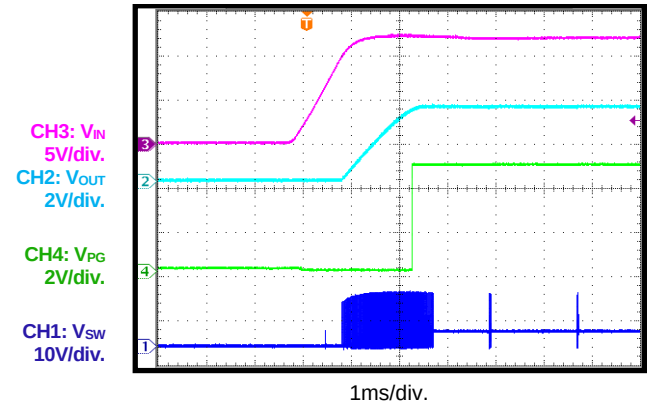
SYNCO Operation

I_{OUT} = 7A, SYNC frequency = 1000kHz



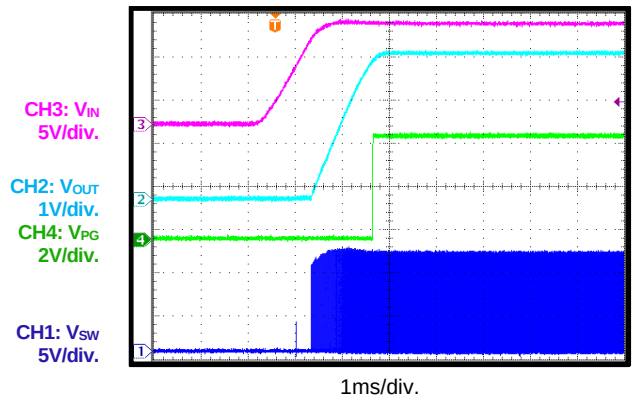
PG in Start-Up through VIN

I_{OUT} = 0A



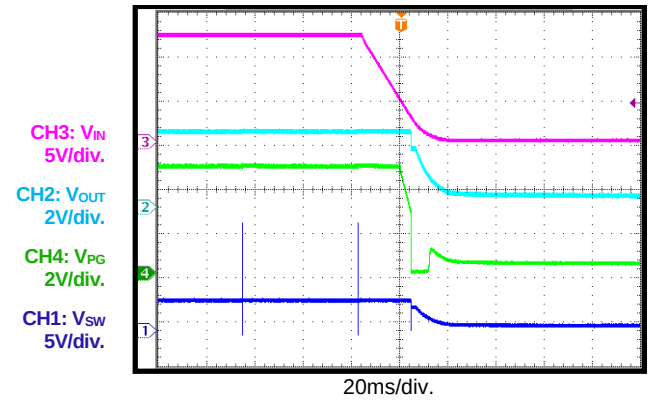
PG in Start-Up through VIN

I_{OUT} = 7A



PG in Shutdown through VIN

I_{OUT} = 0A

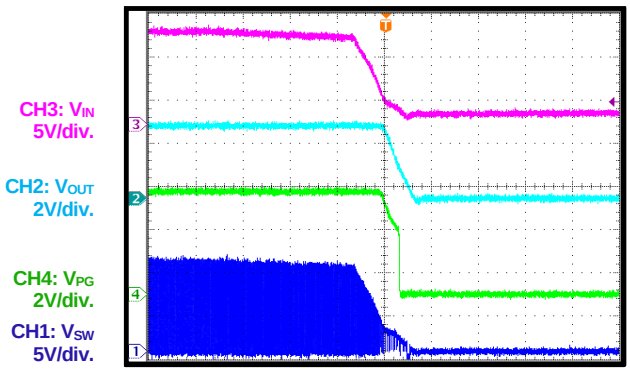


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

PG in Shutdown through VIN

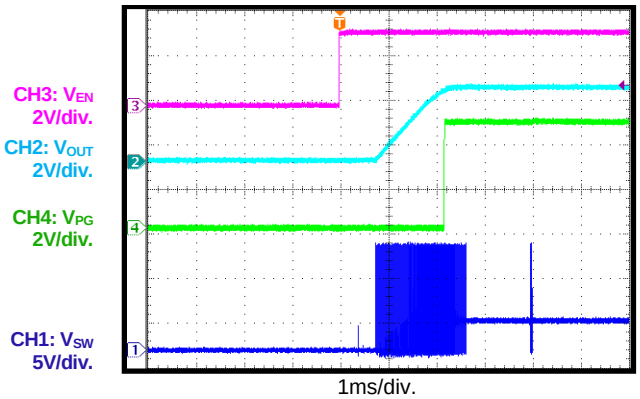
I_{OUT} = 7A



20ms/div.

PG in Start-Up through EN

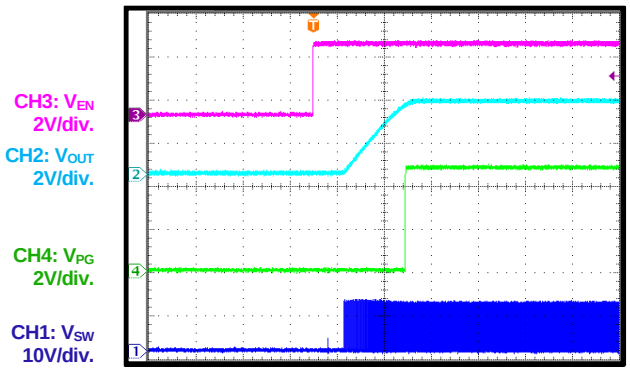
I_{OUT} = 0A



1ms/div.

PG in Start-Up through EN

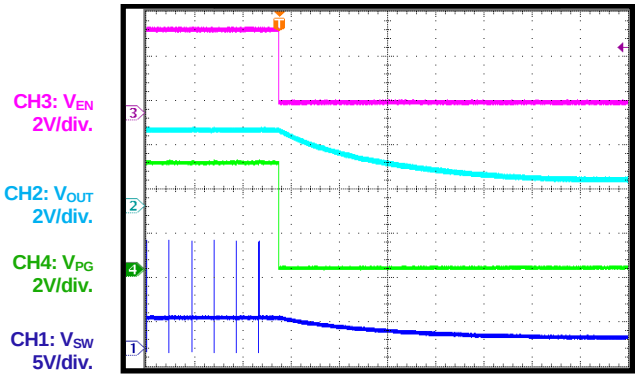
I_{OUT} = 7A



1ms/div.

PG in Shutdown through EN

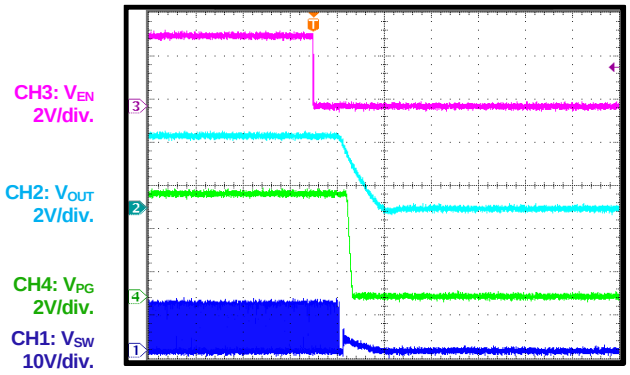
I_{OUT} = 0A



100ms/div.

PG in Shutdown through EN

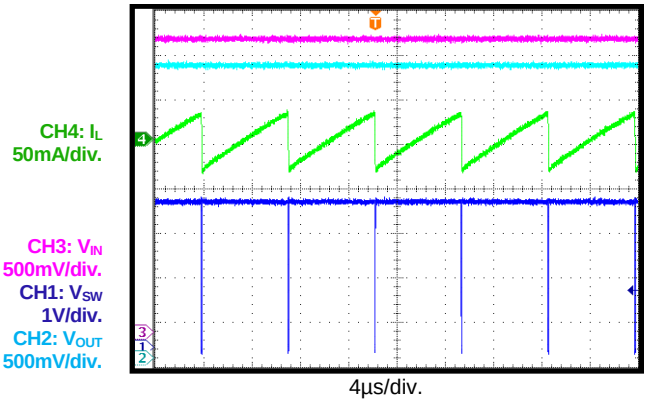
I_{OUT} = 7A



1ms/div.

Low-Dropout Mode

V_{IN} = 3.3V, V_{OUT} set to 3.3V, I_{OUT} = 0A



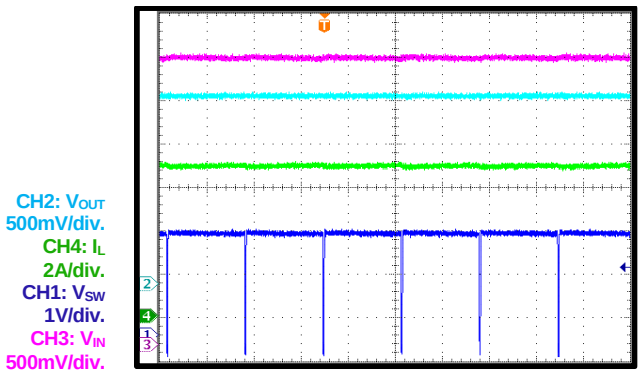
4µs/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

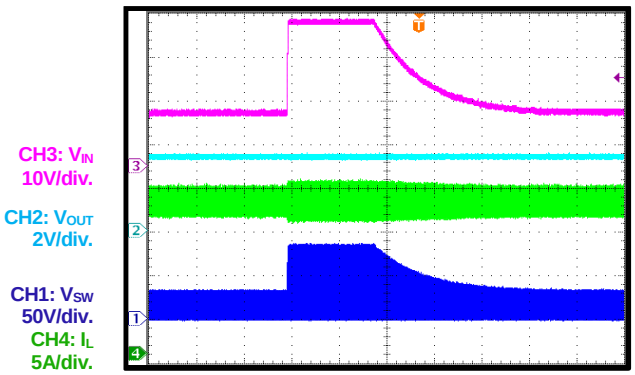
Low-Dropout Mode

V_{IN} = 3.3V, V_{OUT} set to 3.3V, I_{OUT} = 7A



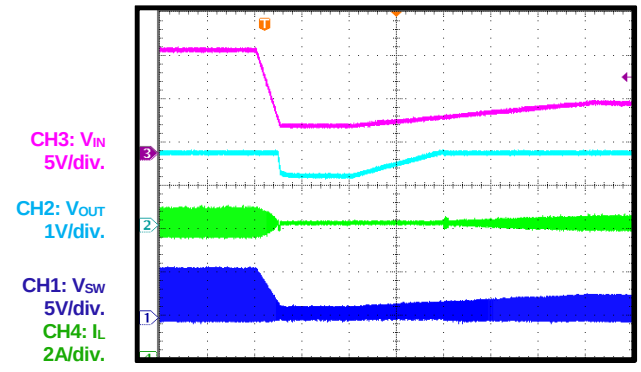
Load Dump

V_{IN} = 12V to 36V, I_{OUT} = 7A



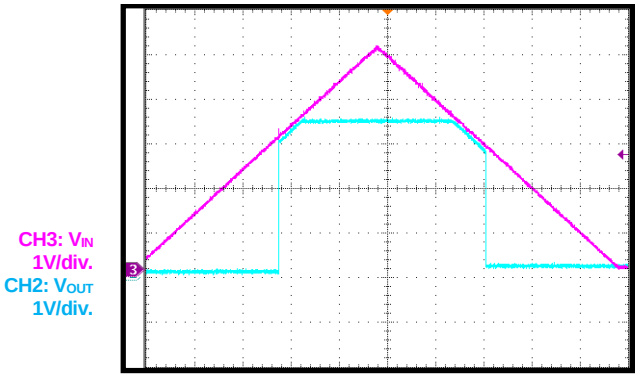
Cold Crank

V_{IN} = 12V to 3.3V to 5V, I_{OUT} = 7A



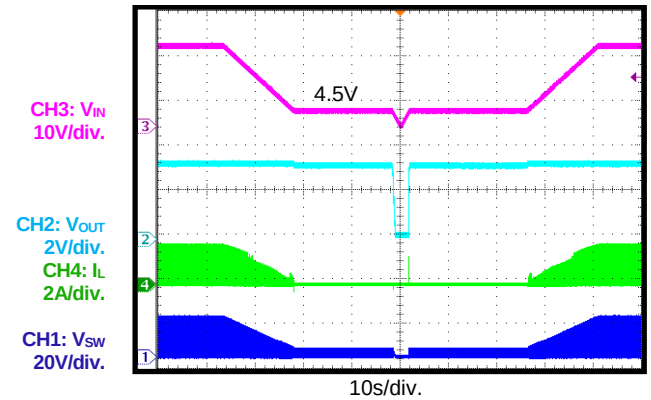
V_{IN} Ramp Up and Down

I_{OUT} = 0.1A



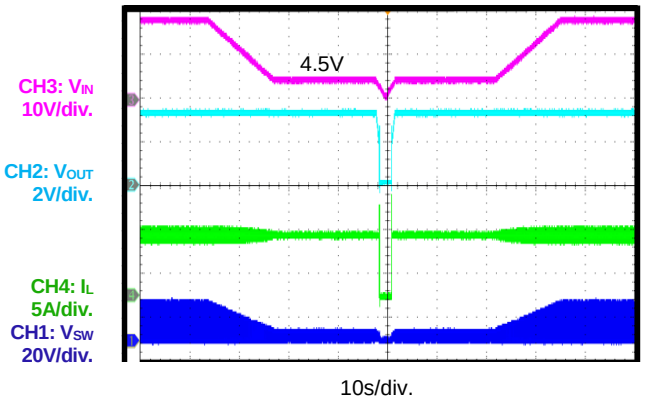
V_{IN} Ramp Down and Up

I_{OUT} = 1mA



V_{IN} Ramp Down and Up

I_{OUT} = 7A



FUNCTIONAL BLOCK DIAGRAM

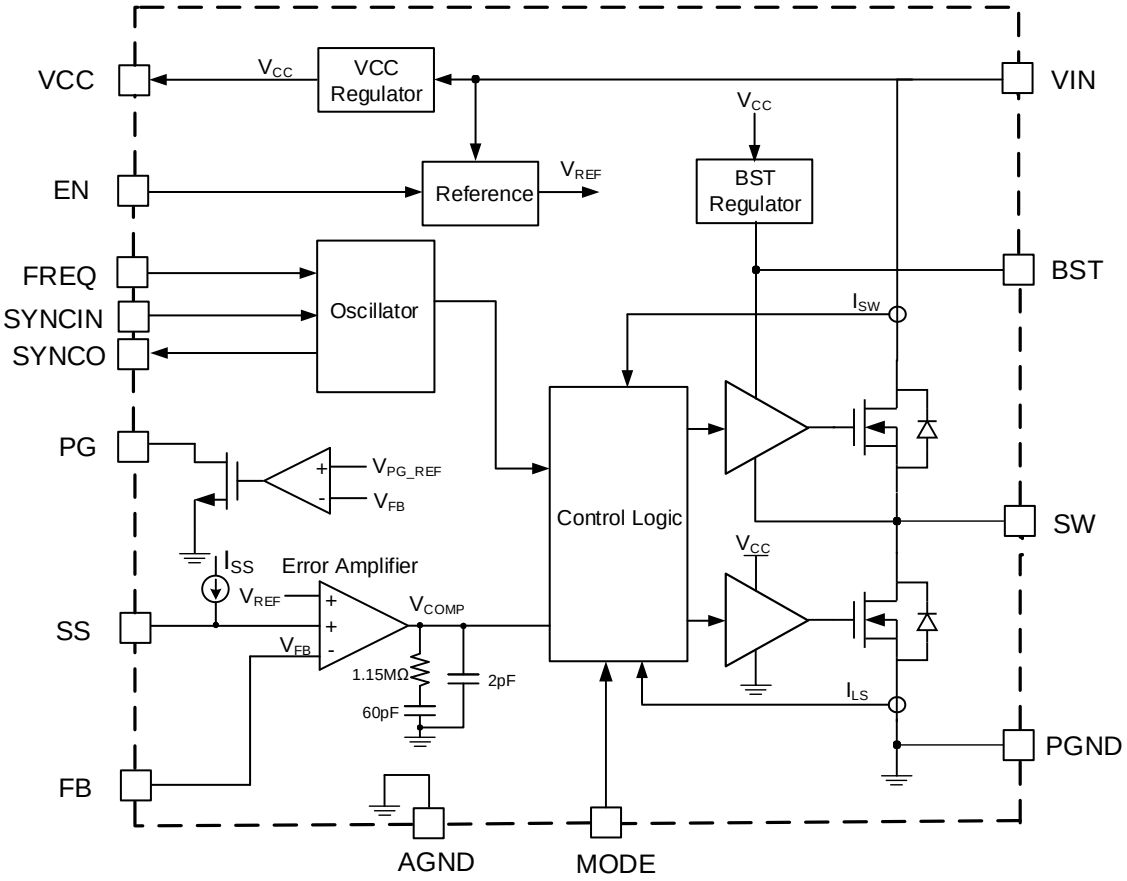


Figure 1: Functional Block Diagram (Adjustable-Output Version)

FUNCTION BLOCK DIAGRAM *(continued)*

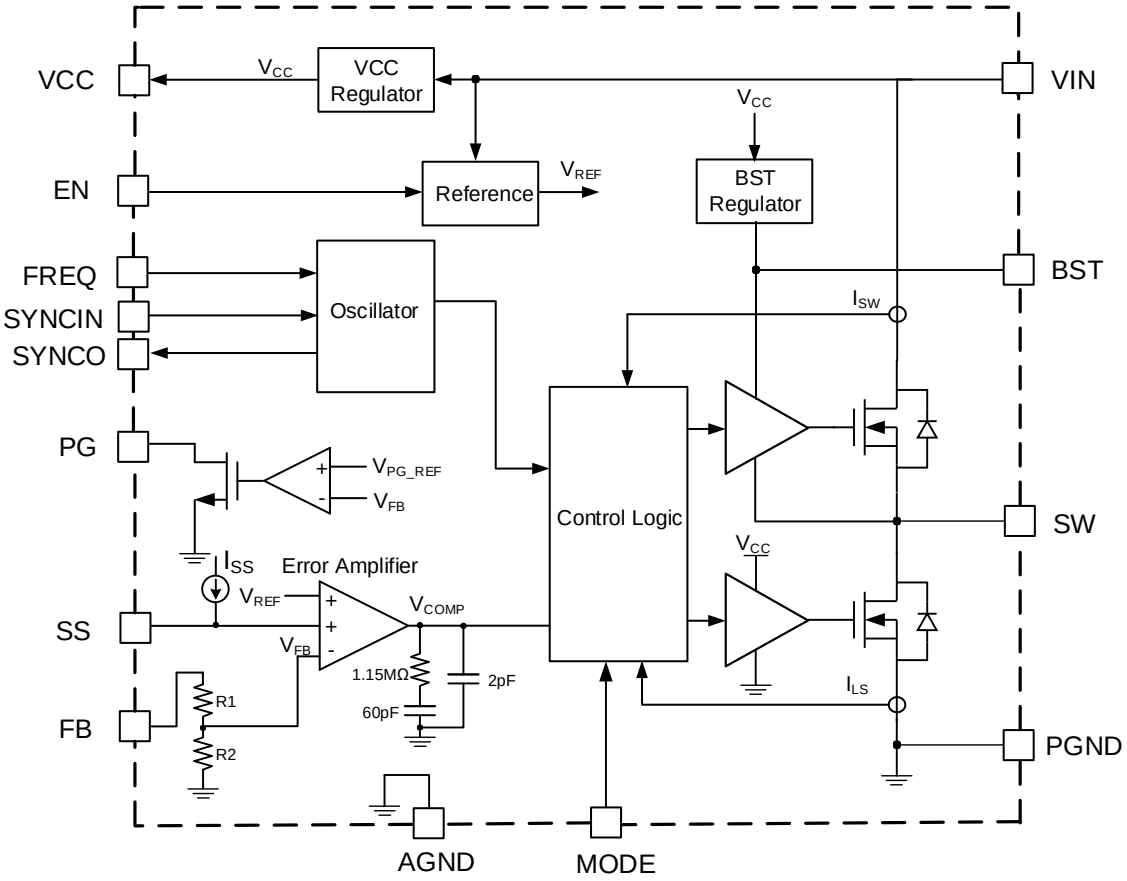


Figure 2: Functional Block Diagram (Fixed-Output Version)

TIMING SEQUENCE DIAGRAM

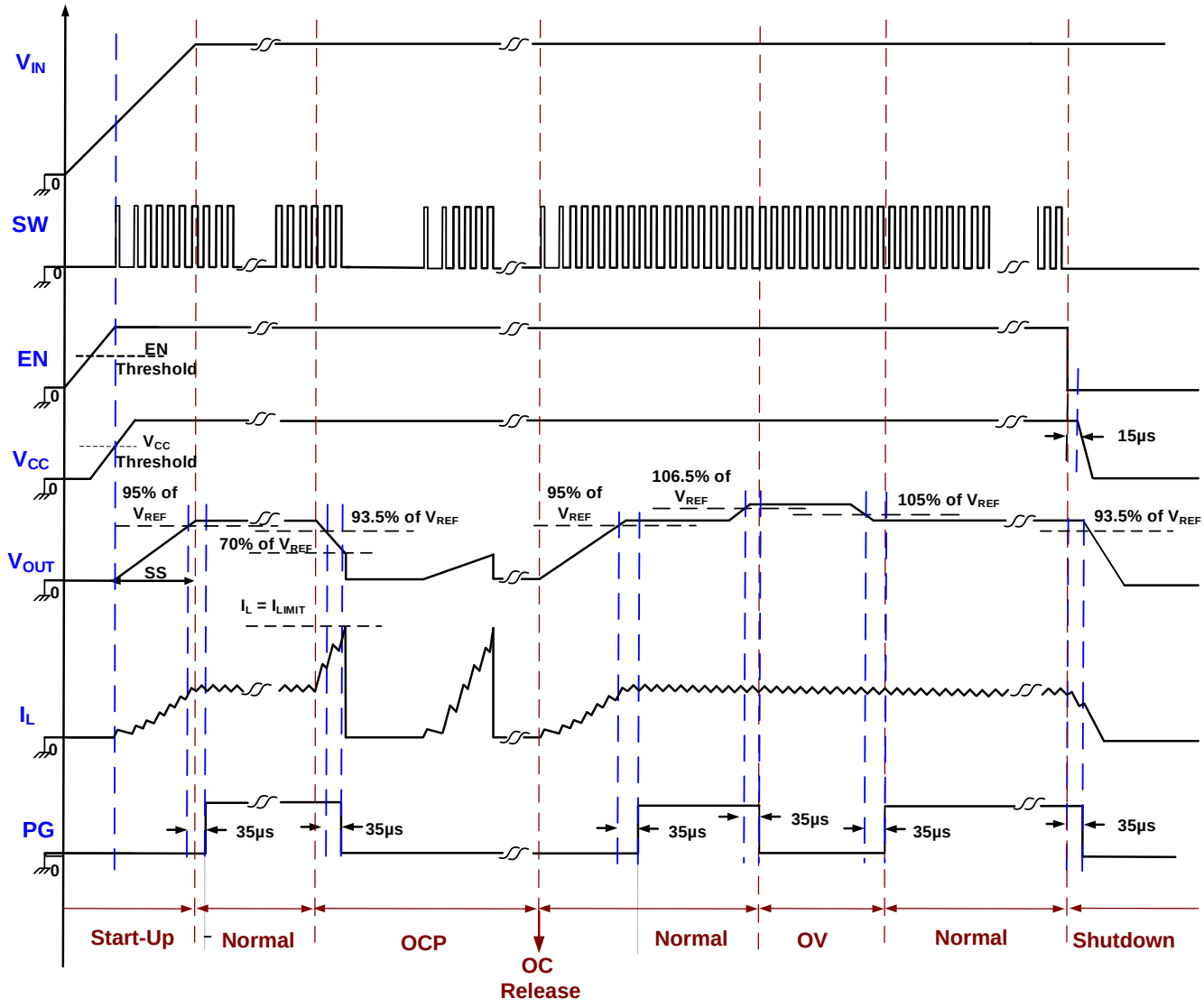


Figure 3: Timing Sequence Diagram

OPERATION

The MPQ4317 is a synchronous, step-down switching regulator with integrated internal high-side and low-side power MOSFETs (HS-FETs and LS-FETs, respectively). It provides 7A of highly efficient output current (I_{OUT}) with current mode control.

It also features wide input voltage (V_{IN}) range, programmable switching frequency (f_{SW}), external soft start (SS), and precision current limit. Its very low operational quiescent current (I_Q) makes it well suited for battery-powered applications.

Pulse-Width Modulation (PWM) Control

At moderate to high output currents, the MPQ4317 operates in a fixed-frequency, peak current control mode to regulate the output voltage (V_{OUT}). A pulse-width modulation (PWM) cycle is initiated by the internal clock. At the rising edge of the clock, the HS-FET turns on and remains on until its current reaches the value set by the internal COMP voltage (V_{COMP}). Once the HS-FET is on, it remains on for at least 100ns.

When the HS-FET is off, the LS-FET turns on immediately and remains on until the next cycle starts. Once the LS-FET is on, it remains on for at least 80ns before next cycle starts.

If the current in the HS-FET does not reach the COMP set current value within one PWM period, then the HS-FET remains on, saving a shutdown operation. If the on time lasts about 10µs, the HS-FET is forced off even though V_{COMP} is not reached.

Light-Load Operation

Under light-load conditions, the MPQ4317 can operate in two different modes by setting the MODE pin to a different status (see Figure 4).

When the MODE pin is pulled above 1.8V, the MPQ4317 works in forced continuous conduction mode (FCCM). The part works with a fixed frequency across the no-load to full-load range in this mode. The advantage of FCCM is the controllable frequency and lower output ripple at light loads.

When the MODE pin is pulled below 0.4V, the MPQ4317 works in advanced asynchronous modulation (AAM) mode. AAM is intended to optimize efficiency during light-load and no-load conditions.

When AAM is enabled, the MPQ4317 first enters non-synchronous operation for as long as the inductor current (I_L) approaches 0A at light loads. If the load decreases further or there is no load that makes V_{COMP} decrease to the set value, then the MPQ4317 enters AAM. In AAM, the internal clock resets every time V_{COMP} crosses over the set value; the crossover time is taken as benchmark of the next clock. When the load increases and V_{COMP} exceeds the set value, the MPQ4317 operates in discontinuous conduction mode (DCM) or CCM, which has a constant switching frequency.

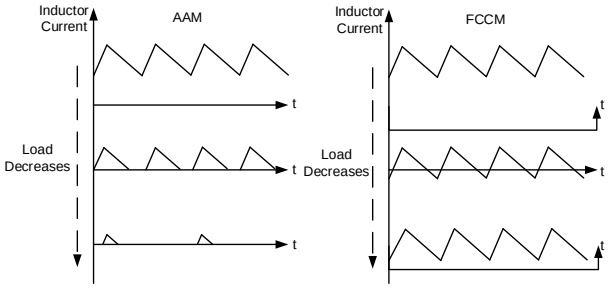


Figure 4: AAM Mode and FCCM

Error Amplifier (EA)

The error amplifier (EA) compares the FB voltage (V_{FB}) with the internal reference voltage (V_{REF}, typically 0.815V) and outputs a current proportional to the difference between the two. I_{OUT} is then used to charge the compensation network to form V_{COMP}, which is used to control the MOSFET current.

During operation, the minimum V_{COMP} is clamped to 0.9V, and the maximum V_{COMP} is clamped to 2.0V. COMP is internally pulled down to GND in shutdown mode.

Internal VCC Regulator

Most of the internal circuitry is powered by the internal, 4.9V VCC regulator. This regulator takes V_{IN} as the input and operates across the full V_{IN} range. When V_{IN} is above 4.9V, the VCC voltage (V_{CC}) is in full regulation. When V_{IN} is below 4.9V, V_{CC} degrades.

Bootstrap Charging

The bootstrap capacitor (C_{BST}) is charged and regulated to about 5V by the dedicated internal bootstrap regulator. When the voltage between the BST and SW nodes falls below its regulation, a PMOS pass transistor connected from VCC to BST turns on to charge C_{BST}. External circuitry

should provide enough voltage headroom to facilitate the charging. When the HS-FET is on, the BST voltage (V_{BST}) exceeds V_{CC}, so C_{BST} cannot be charged.

At higher duty cycles, the time period available for bootstrap charging is shorter, so C_{BST} may not be sufficiently charged. If the external circuit does not have sufficient voltage and time to charge C_{BST}, additional external circuitry can be used to ensure V_{BST} is within its normal operation range.

Low-Dropout Mode and BST Refresh

To improve dropout, the MPQ4317 is designed to operate at close to 100% duty cycle as long as the BST-to-SW-pin voltage is above 2.5V. If the voltage from the BST pin to the SW pin drops below 2.5V, the HS-FET turns off using the under-voltage lockout (UVLO) circuit, which allows the LS-FET to conduct and refresh the charge on C_{BST}. In DCM or pulse-skip mode (PSM), the LS-FET is forced on to refresh V_{BST}.

Since the supply current sourced from C_{BST} is low, the HS-FET can remain on for more switching cycles than are required to refresh the capacitor, thus making the switching regulator's duty cycle high.

The effective duty cycle during the regulator's dropout period is mainly influenced by the voltage drops across the power MOSFET, the inductor resistance, the low-side diode, and the PCB resistance.

Enable (EN) Control

EN is a digital control pin that turns the regulator on and off. The MPQ4317 can be enabled by two methods, described below:

The first is to enable the part via the external logic H/L signal. When EN is pulled below its falling threshold voltage (0.85V), the chip is put into the lowest shutdown current mode. Force this pin above the EN rising threshold voltage (1V) to turn on the part.

The second is the configurable V_{IN} under-voltage lockout (UVLO) threshold. With a high enough V_{IN}, the chip can be enabled and disabled via the EN pin. With the internal current source, this circuit can generate a programmable V_{IN} UVLO and hysteresis (see Figure 5).

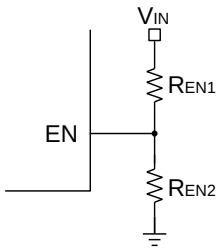


Figure 5: Enable Divider Circuit

Frequency Programmable and Fold back

The MPQ4317's oscillating frequency can be configured either by an external resistor (R_{FREQ}) from the FREQ pin to ground, or by a logic level SYNC signal.

To get the expected f_{SW}, select the corresponding R_{FREQ} value using the f_{SW} vs. R_{FREQ} curve (see the Typical Performance Characteristics section on page 15). Note that f_{SW} will fold back at high input voltages to avoid the minimum on time being triggered and V_{OUT} going out of regulation. The recommended f_{SW} for car battery applications is 350kHz to 1000kHz. Table 1 lists recommended R_{FREQ} values for common frequencies. Higher frequencies may be supported for the applications that do not have a critical limit on f_{SW} or have a relatively low, stable V_{IN}.

Table 1: Recommended R_{FREQ} for Given f_{SW}

R_{FREQ} (kΩ)	f_{SW} (kHz)
86.6	350
80.6	380
75	410
62	470
59	500
54.9	530
49.9	590
45.3	640
41.2	700
37.4	760
34	830
30.9	910
28.7	960
26.1	1000

Frequency Spread Spectrum (FSS)

The MPQ4317 uses a 12kHz modulation frequency with a 128-steps triangular profile to spread the internal oscillator frequency across a 20% (±10%) window. The steps are fixed, and independent of the setting oscillator frequency to optimize the frequency spread spectrum (FSS) performance (see Figure 6 on page 30).

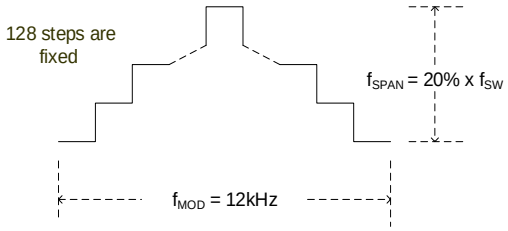


Figure 6: Spread Spectrum Scheme

Side bands are created by modulating f_{SW} with the triangle modulation waveform. The emission power of the fundamental f_{SW} and its harmonics is distributed into smaller pieces. Thus, the peak EMI noise is reduced significantly.

Soft Start (SS)

The MPQ4317 implements soft start (SS) to prevent the converter's V_{OUT} from overshooting during start-up.

When the SS period starts, an internal current source begins charging the external soft-start capacitor (C_{SS}). When the soft-start voltage (V_{SS}) is below the internal V_{REF}, V_{SS} overrides V_{REF} and the EA uses V_{SS} as the reference. When V_{SS} is above V_{REF}, V_{REF} regains control. C_{SS} can be calculated with Equation (1):

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} = 13.5 \times t_{SS}(ms) \quad (1)$$

The SS pin can be used for tracking and sequencing.

Pre-Biased Start-Up

if V_{FB} > V_{SS} - 150mV at start-up, the output has pre-biased voltage. Neither the HS-FET or LS-FET turn on until V_{SS} exceeds V_{FB}.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from thermally running away. When the silicon die temperature exceeds its upper threshold, the power MOSFETs shut down. When the temperature returns to below its lower threshold, the chip is enabled and resumes normal operation.

Current Comparator and Current Limit

The power MOSFET current is accurately sensed via a current-sense MOSFET. It is then fed to the high-speed current comparator for current mode control. The current comparator takes this sensed current as one of its inputs. When the HS-FET is on, the comparator is blanked until the end of the turn-on transition to dodge the sample inductor current noise. Then the comparator compares the MOSFET current with V_{COMP}. When the sensed current is above V_{COMP}, the comparator outputs low to turn off the HS-FET. The internal power MOSFET's maximum current is internally limited cycle by cycle.

Hiccup Protection

When the output is shorted to ground, V_{OUT} drops below 70% of its nominal output, which causes the IC to shut down momentarily and begin discharging C_{SS}. Once C_{SS} is fully discharged, the IC restarts with a full SS. This hiccup process repeats until the fault is removed.

Start-Up and Shutdown

If both VIN and EN exceeds their appropriate thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

While the internal supply rail is up, an internal timer keeps the power MOSFET off for about 50µs to blank any start-up glitches. When the SS block is enabled, it first holds its output low to ensure the remaining circuitries are ready, and then slowly ramps up.

Three events can shut down the chip: EN low, V_{IN} low, thermal shutdown. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

Power Good (PG) Output

The MPQ4317 includes an open-drain power good (PG) output that indicates whether the V_{OUT} is within its normal range. If using this function, a pull-up resistor connected to the power source is required. If V_{OUT} is within 95% to 105% of the nominal voltage, PG goes high. If V_{OUT} is above 106.5% or below 93.5% of the nominal voltage, PG goes low.

SYNCIN and SYNCO

f_{SW} can be synced to the rising edge of the clock signal applied at SYNCIN. The recommended SYNCIN frequency range is 350kHz to 1000kHz. Ensure that the SYNCIN off time is shorter than the internal oscillator period; otherwise, the

internal clock will turn on the HS-FET before the rising edge of SYNCIN. There is no other limit on the pulse width of SYNCIN, but there is always parasitic capacitance of the pad. So if the pulse width is too short, a clear rising and falling edge may not be seen due to the parasitic capacitance. A pulse longer than 100ns is recommended in applications.

When applying SYNCIN in AAM, drive SYNCIN below its specified threshold (0.4V) or leave SYNCIN floating before the MPQ4317 starts up to enter AAM. An external SYNCIN clock can also be added. To avoid SYNCIN floating when using this function through an external clock, connect a resistor to GND. Given SYNCIN's drive capability, the resistor is recommended to be between 10kΩ and 51kΩ.

The SYNCO pin provides a default 180° phase-shifted clock to the internal oscillator. If there is no external SYNCIN clock, SYNCO can provide a 180° phase-shifted clock compared with the internal clock. If there is an external SYNCIN clock, SYNCO provides a 180° phase-shifted clock compared with the external SYNCIN clock.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider connected to FB sets V_{OUT} (see Figure 7).

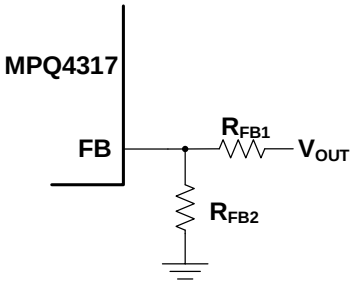


Figure 7: Feedback Network

Calculate R_{FB2} with Equation (2):

$$R_{FB2} = \frac{R_{FB1}}{\frac{V_{OUT}}{0.815V} - 1} \quad (2)$$

Table 2 lists the recommended feedback resistor values for common output voltages.

Table 2: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)
3.3	100 (1%)	32.4 (1%)
5	100 (1%)	19.6 (1%)

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, use a 4.7µF to 10µF capacitor. It is strongly recommended to use another, lower-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and GND as possible.

Since C_{IN} absorbs the input switching current, it requires an adequate ripple current rating. The RMS current (I_{CIN}) in the input capacitor can be estimated with Equation (3):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (3)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (4):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (4)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low-ESR capacitors to keep the output voltage ripple low. The output voltage ripple (ΔV_{OUT}) can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 f_{SW} \times C_{OUT}}) \quad (6)$$

Where L is the inductance, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple (ΔV_{OUT}) can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output voltage ripple (ΔV_{OUT}) can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (8)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ4317 can be optimized for a wide range of capacitances and ESR values.

Selecting the Inductor

A 1µH to 10µH inductor with a DC current rating at least 25% greater than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage; however, it also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductor value is to allow the inductor ripple current to be approximately 30% of the maximum load current. The inductance (L) can then be calculated with Equation (9):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current (I_{LP}) can be calculated with Equation (10):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

V_{IN} UVLO Setting

The MPQ4317 has an internal, fixed under-voltage lockout (UVLO) threshold. The rising threshold is 3V, while the falling threshold is about 2.7V. For the applications that require a higher UVLO point, an external resistor divider between VIN and EN can be used to achieve a higher equivalent UVLO threshold (see Figure 8).

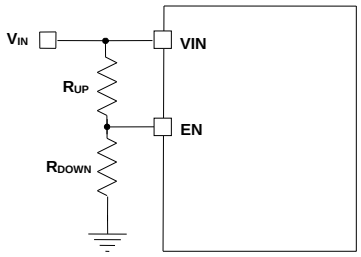


Figure 8: Adjustable UVLO Using EN Divider

The UVLO rising and falling thresholds can be calculated with Equation (11) and Equation (12), respectively:

$$IN_{UVLO\_RISING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN\_RISING} \quad (11)$$

$$IN_{UVLO\_FALLING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN\_FALLING} \quad (12)$$

Where V_{EN_RISING} is 1V, and $V_{EN\_FALLING}$ is 0.85V.

External BST Diode and Resistor

An external BST diode can enhance the efficiency of the regulator when the duty cycle is high. A 2.5V to 5V power supply can be used to power the external bootstrap diode. VCC or V_{OUT} is recommended to be this power supply in the circuit (see Figure 9).

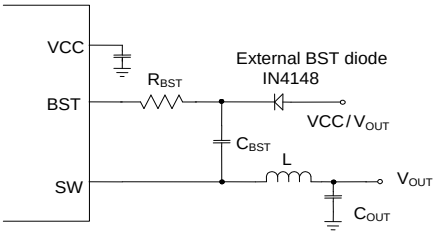


Figure 9: Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the recommended C_{BST} value is 0.1µF to 1µF. A resistor in series with the BST capacitor (R_{BST}) can reduce the SW rising rate and voltage spikes. This helps enhance EMI performance and reduce voltage stress at a high V_{IN}. A higher resistance is better for SW spike reduction, but compromises efficiency. As a tradeoff between EMI and efficiency, a ≤20Ω R_{BST} is recommended.

Selecting the VCC Capacitor

The VCC capacitor should be 10 times greater than the boost capacitor. A VCC capacitor above 68µF (nominal) is not recommended.

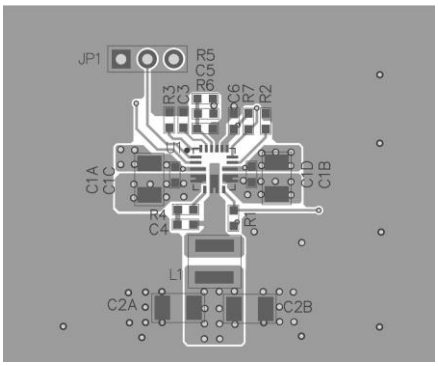
PCB Layout Guidelines [9]

Efficient PCB layout is critical for stable operation. A 4-layer layout is strongly recommended to achieve better thermal performance. For best results, refer to Figure 10 and follow the guidelines below:

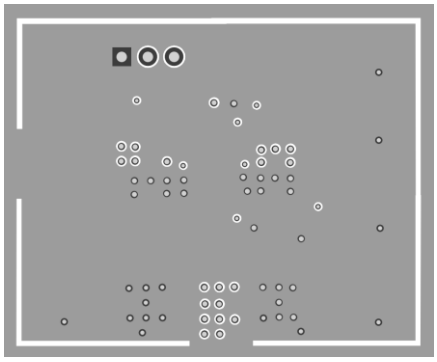
1. Place symmetric input capacitors as close to VIN and GND as possible.
2. Use a large ground plane to connect directly to PGND.
3. If the bottom layer is a ground plane, add vias near PGND.
4. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
5. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to minimize high-frequency noise.
6. Keep the connection between the input capacitor and VIN as short and wide as possible.
7. Place the VCC capacitor as close to VCC and GND as possible.
8. Route SW and BST away from sensitive analog areas, such as FB.
9. Place the feedback resistors close to the chip to ensure that the trace that connects to FB is as short as possible.
10. Use multiple vias to connect the power planes to the internal layers.

Note:

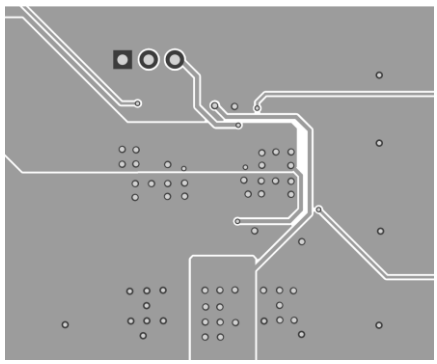
9) The recommended PCB layout is based on Figure 11 .



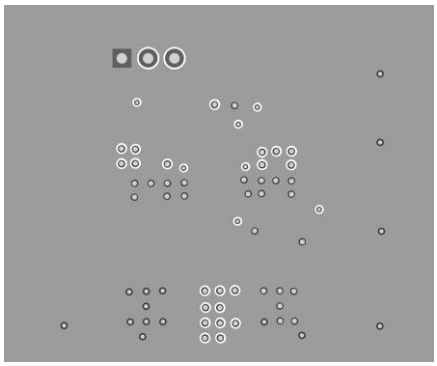
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 10: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

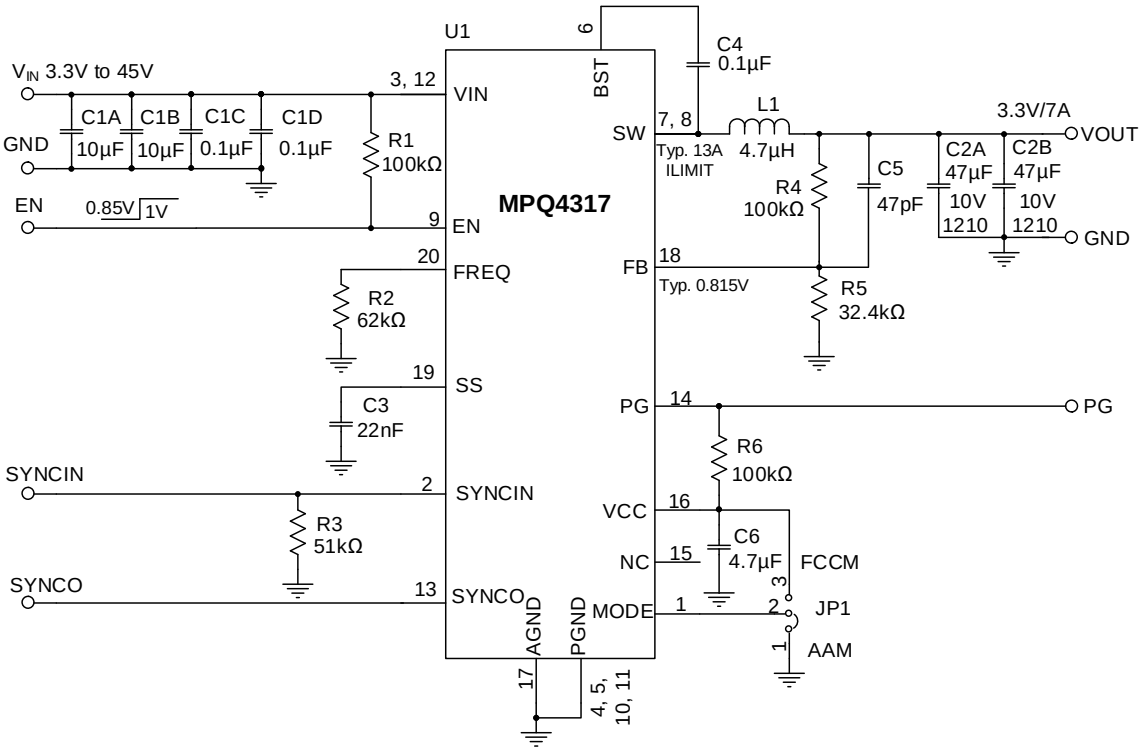


Figure 11: Typical Application Circuit (V_{OUT} = 3.3V, f_{SW} = 470kHz)

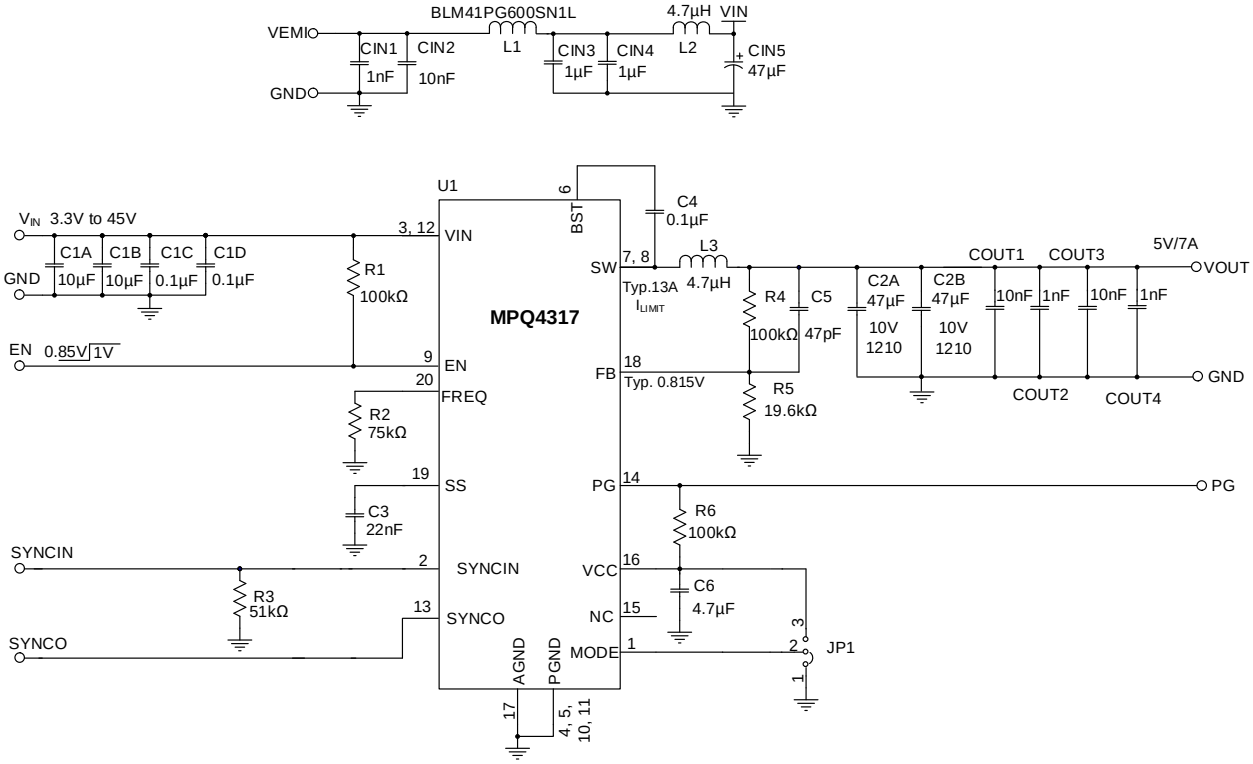


Figure 12: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 410kHz with EMI Filters)

TYPICAL APPLICATION CIRCUITS *(continued)*

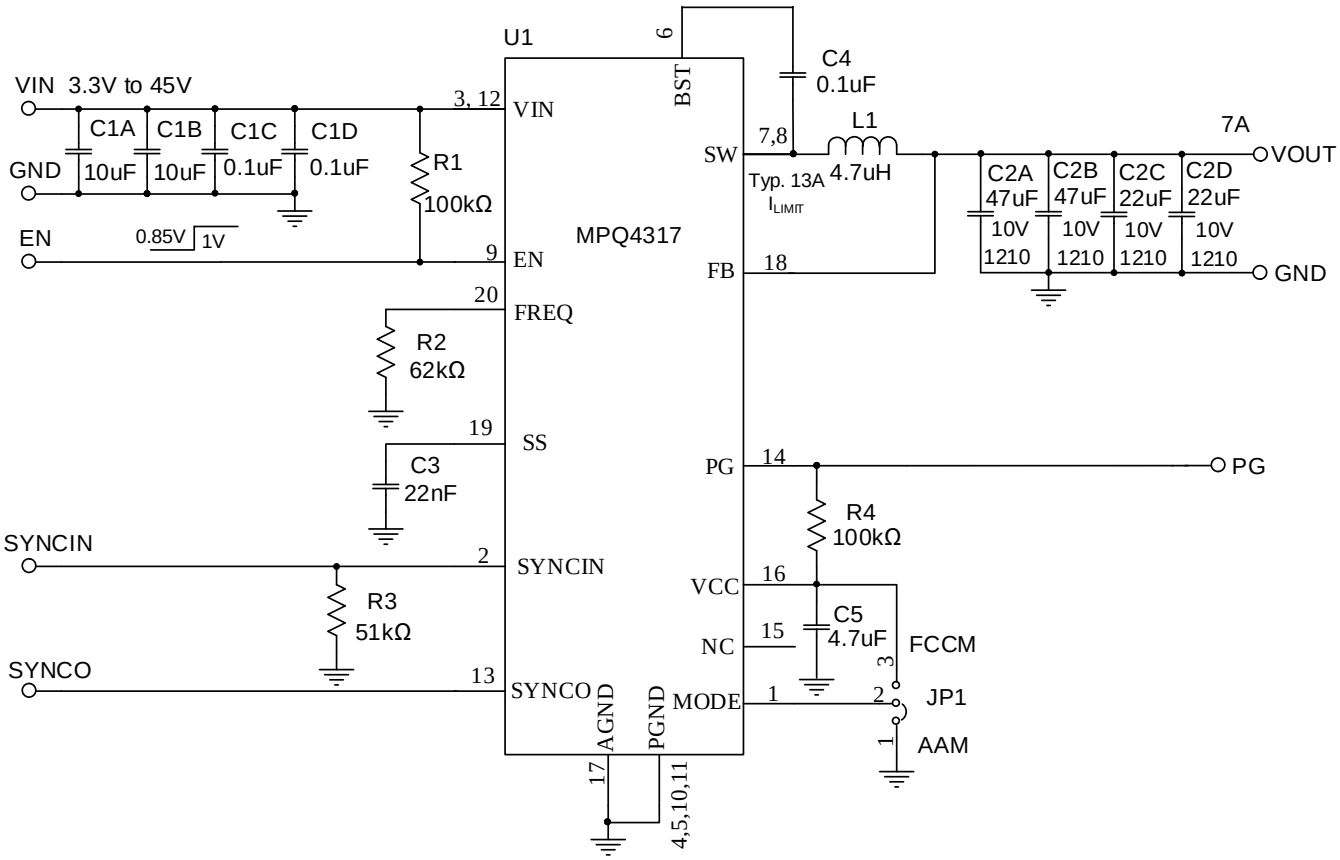
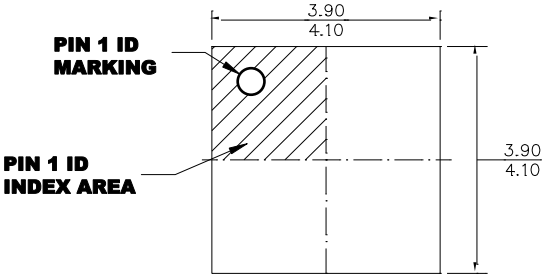


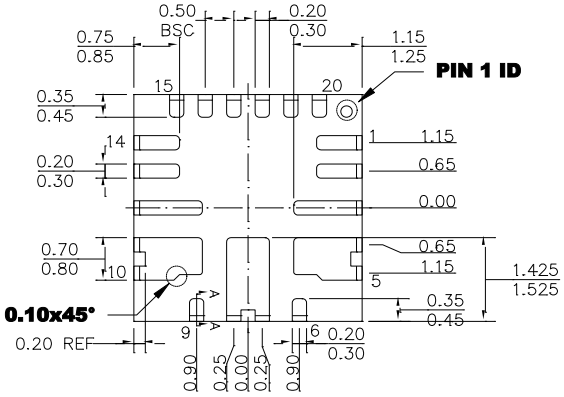
Figure 13: Typical Application Circuit (f_{SW} = 470kHz, Fixed Output)

PACKAGE INFORMATION

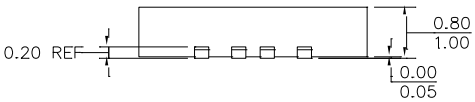
QFN-20 (4mmx4mm)
Wettable Flank



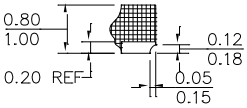
TOP VIEW



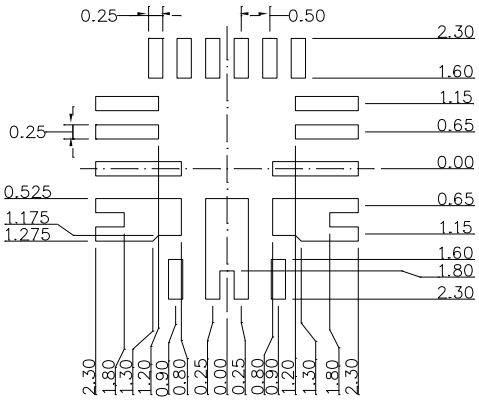
BOTTOM VIEW



SIDE VIEW



SECTION A-A

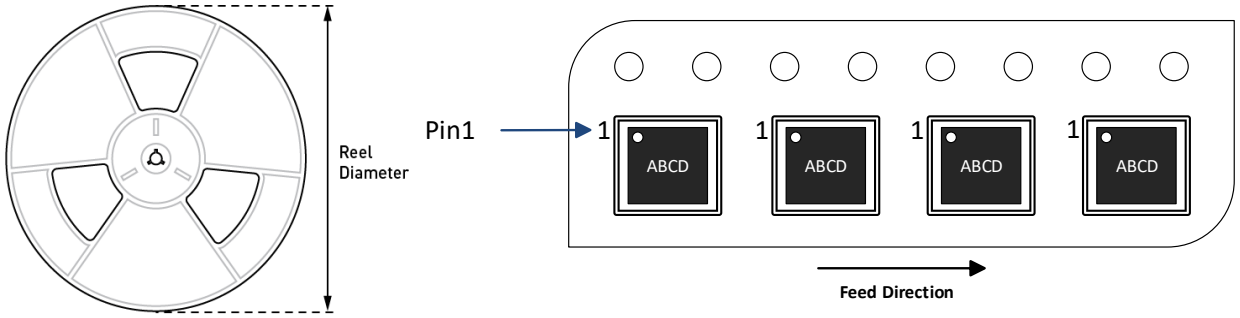


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube (10)	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4317GRE-AEC1-Z	QFN-20 (4mmx4mm)	5000	N/A	13in	12mm	8mm
MPQ4317GRE-33-AEC1-Z						
MPQ4317GRE-5-AEC1-Z						

Note:

10) N/A indicates “not available” in tubes. For 500-piece tape & reel prototype quantities, please contact the factory. (The order code for a 500-piece partial reel order is “-P”. Tape & reel dimensions are the same as the full reel.)