MPQ4415A

1.5A, 36V, 2.2MHz, High-Efficiency, Synchronous, Step-Down Converter AEC-Q100 Qualified

DESCRIPTION

The MPQ4415A is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. The MPQ4415A offers a very compact solution that achieves 1.5A of continuous output current with excellent load and line regulation over a wide input supply range. The MPQ4415A uses synchronous mode operation for higher efficiency over the output current load range.

Current mode operation provides fast transient response and eases loop stabilization.

Full protection features include over-current protection (OCP) and thermal shutdown.

The MPQ4415A requires a minimal number of readily available, standard, external components and is available in a space-saving QFN-13 (2.5mmx3mm) package.

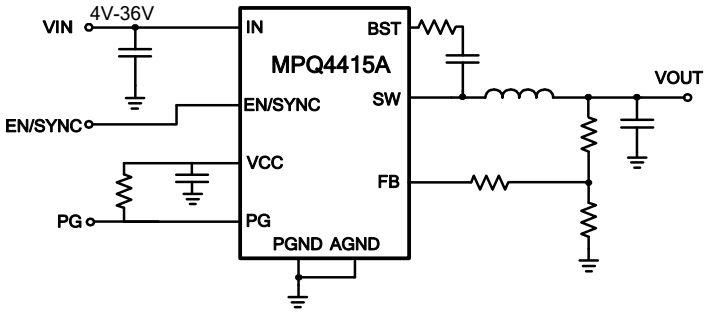
FEATURES

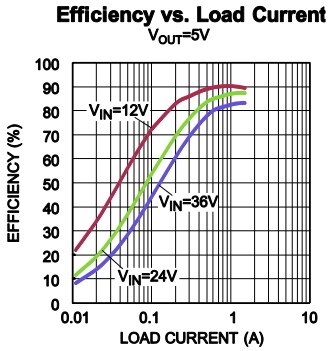
- Wide 4V to 36V Operating Input Range
- 1.5A Continuous Load Current
- 90mΩ/50mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- High-Efficiency Synchronous Mode Operation
- Default 2.2MHz Switching Frequency
- 450kHz to 2.2MHz Frequency Sync
- Forced Continuous Conduction Mode (CCM)
- Internal Soft Start (SS)
- Power Good (PG) Indicator
- Over-Current Protection (OCP) with Valley-Current Detection and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- CISPR25 Class 5 Compliant
- Available in a QFN-13 (2.5mmx3mm) Package
- Available in a Wettable Flank Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Automotive
- Industrial Control Systems
- Medical and Imaging Equipment
- Telecom Applications
- Distributed Power Systems

TYPICAL APPLICATION



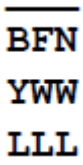


ORDERING INFORMATION

Part Number*	Package	Top Marking
MPQ4415AGQB**	QFN-13 (2.5mmx3mm)	*See Below*
MPQ4415AGQB-AEC1**		
MPQ4415AGQBE-AEC1***	QFN-13 (2.5mmx3mm)	*See Below*

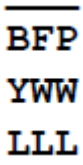
* For Tape & Reel, add suffix –Z (e.g. MPQ4415AGQB-Z)
*** wettable flank

TOP MARKING (MPQ4415AGQB&MPQ4415AGQB-AEC1)



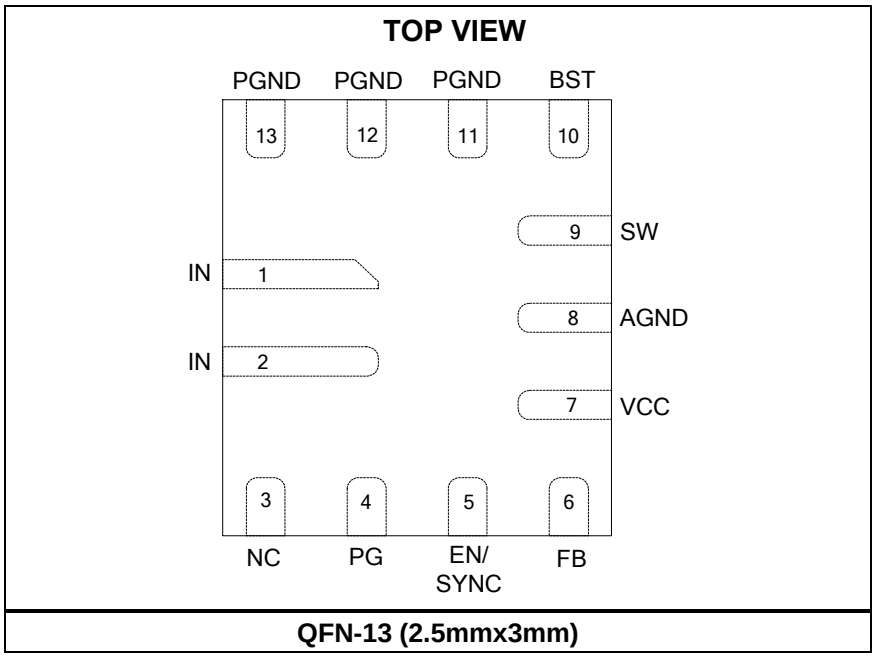
BFN: Product code of MPQ4415AGQB and MPQ4415AGQB-AEC1
Y: Year code
WW : Week code
LLL: Lot number

TOP MARKING (MPQ4415AGQBE-AEC1)



BFP: Product code of MPQ4415AGQBE-AEC1
Y: Year code
WW : Week code
LLL: Lot number

PACKAGE REFERENCE



QFN-13 (2.5mmx3mm)

PIN FUNCTIONS

Package Pin #	Name	Description
1, 2	IN	**Supply voltage.** IN supplies power for the internal MOSFET and regulator. The MPQ4415A operates from a 4V to 36V input rail. A low ESR and low inductance capacitor is required to decouple the input rail. Place the input capacitor very close to IN and connect it with wide PCB traces and multiple vias.
3	NC	**No connection.** Do not connect.
4	PG	**Power good indicator.** The output of PG is an open drain and goes high if the output voltage exceeds 88% of the nominal voltage.
5	EN/SYNC	**Enable/synchronize.** Pull EN/SYNC high to enable the MPQ4415A. Float EN/SYNC or connect EN/SYNC to ground to disable the MPQ4415A. If an external sync clock is applied to EN/SYNC, the internal clock follows the sync frequency.
6	FB	**Feedback.** Connect FB to the tap of an external resistor divider from the output to AGND to set the output voltage. The frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 400mV to prevent current limit runaway during a short-circuit fault. Place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces.
7	VCC	**Internal bias supply.** Decouple VCC with a 0.1μF - 0.22μF capacitor. The capacitance should be no more than 0.22μF.
8	AGND	**Analog ground.** AGND is the reference ground of the logic circuit. AGND is connected to PGND internally. There is no need to add external connections to PGND.
9	SW	**Switch output.** Connect SW using a wide PCB trace.
10	BST	**Bootstrap.** A capacitor connected between SW and BST is required to form a floating supply across the high-side switch driver. A 20Ω resistor placed between the SW and BST capacitor is strongly recommended to reduce SW voltage spikes.
11, 12, 13	PGND	**Power ground.** PGND is the reference ground of the power device and requires careful consideration during PCB layout. For best results, connect PGND with copper pours and vias.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to 40V
Switch voltage (V_{SW}) .....-0.3V to V_{IN} + 0.3V
BST voltage (V_{BST}) ..... V_{SW} + 6V
All other pins ..... -0.3V to 6V (2)
Continuous power dissipation (T_A = +25°C) (3)
QFN-13 (2.5mmx3mm) 2.08W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to 150°C

Recommended Operating Conditions

Supply voltage (V_{IN}) .....4V to 36V
Output voltage (V_{OUT}) .....0.8V to V_{IN}*D_{MAX}
Operating junction temp. (T_J). .. -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-13 (2.5mmx3mm)	60	13	°C/W

NOTES:

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) For details on EN/SYNC's ABS max rating, please refer to the Enable/SYNC section on page 12.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, unless otherwise noted, typical values are at T_J = +25°C.

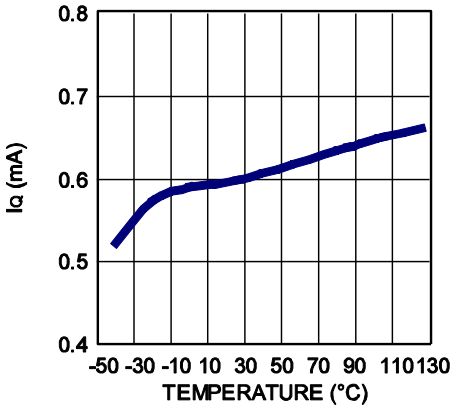
Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{SHDN}	V_{EN} = 0V			8	μA
Supply current (quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 1V, no switching		0.6	0.8	mA
HS switch on resistance	R_{ON_HS}	V_{BST-SW} = 5V		90	155	mΩ
LS switch on resistance	R_{ON_LS}	V_{CC} = 5V		50	105	mΩ
Switch leakage	I_{SW_LKG}	V_{EN} = 0V, V_{SW} = 12V			1	μA
Current limit (5)	I_{LIMIT}	20% duty cycle	2.4	4.0	6.0	A
Low-side valley current limit			1.7	2.5	3.5	A
Reverse current limit				1.2		A
Oscillator frequency	f_{SW}	V_{FB} = 700mV	1800	2200	2600	kHz
Foldback frequency during soft start (5)	f_{FB}	V_{FB} = 200mV		0.2		f_{SW}
Maximum duty cycle	D_{MAX}	V_{FB} = 700mV		85		%
Minimum on time (5)	t_{ON_MIN}			46		ns
Synchronous frequency range	f_{SYNC}		450		2200	kHz
Feedback voltage	V_{FB}	T_J = +25°C	795	807	819	mV
		T_J = -40°C to +125°C	790	807	824	mV
Feedback current	I_{FB}	V_{FB} = 820mV		10	50	nA
EN/SYNC rising threshold	V_{EN_RISING}		1.1	1.45	1.8	V
EN/SYNC falling threshold	$V_{EN\_FALLING}$		0.7	1	1.3	V
EN/SYNC threshold hysteresis	V_{EN_HYS}			450		mV
EN/SYNC input current	I_{EN}	V_{EN} = 2V		5	10	μA
		V_{EN} = 0V		0	0.2	μA
EN turn off delay				3		μs
V_{IN} under-voltage lockout threshold rising	$INUV_{RISING}$		3	3.5	3.8	V
V_{IN} under-voltage lockout threshold hysteresis	$INUV_{HYS}$			330		mV
PG rising threshold	PG_{Vth_RISING}	As a percentage of V_{FB}	83	88	93	%
PG falling threshold	$PG_{Vth\_FALLING}$	As a percentage of V_{FB}	78	83	88	%
PG threshold hysteresis	PG_{Vth_HYS}	As a percentage of V_{FB}		5		%
PG rising delay	PG_{TD_RISING}		30	90	160	μs
PG falling delay	$PG_{TD\_FALLING}$		30	55	95	μs
PG sink current capability	V_{PG}	Sink 4mA			0.4	V
PG leakage current	I_{PG_LKG}			10	100	nA
VCC regulator	V_{CC}	I_{CC} = 0mA	4.6	4.9	5.2	V
VCC load regulation		I_{CC} = 5mA		1.5	4	%
Soft-start time	t_{SS}	V_{OUT} from 10% to 90%	0.45	1.5	3	ms
Thermal shutdown (5)				170		°C
Thermal hysteresis (5)				30		°C

NOTE:

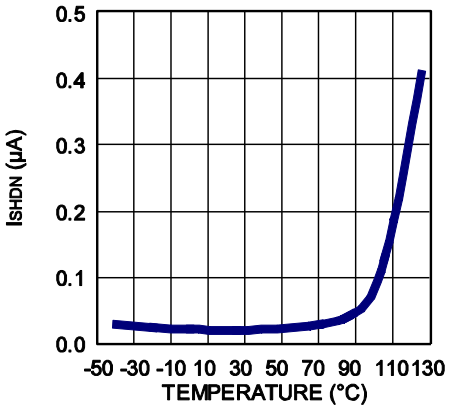
5) Not tested in production and guaranteed by design and characterization.

TYPICAL CHARACTERISTICS

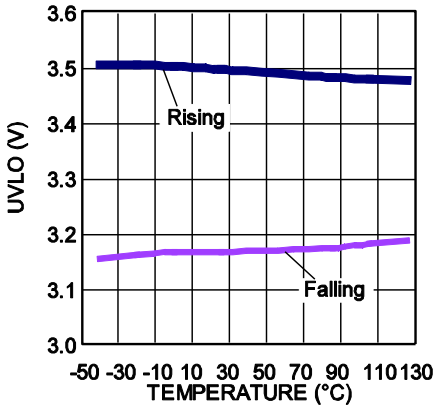
Quiescent Current vs. Temperature



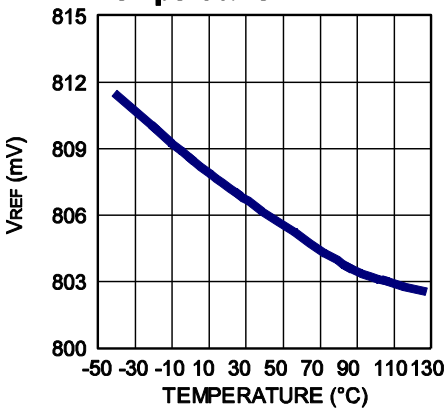
Shutdown Current vs. Temperature



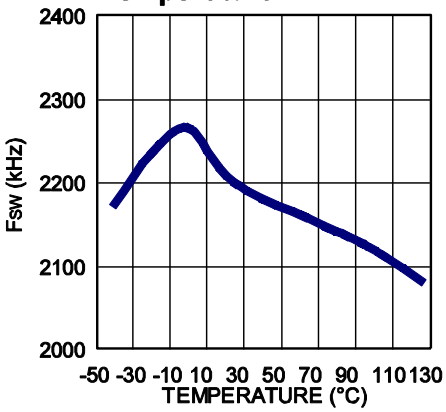
VIN UVLO Threshold vs. Temperature



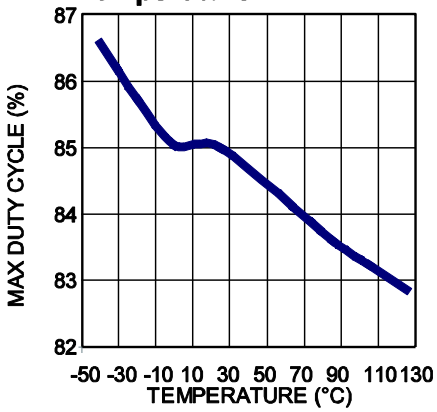
Feedback Reference vs. Temperature



Switching Frequency vs. Temperature



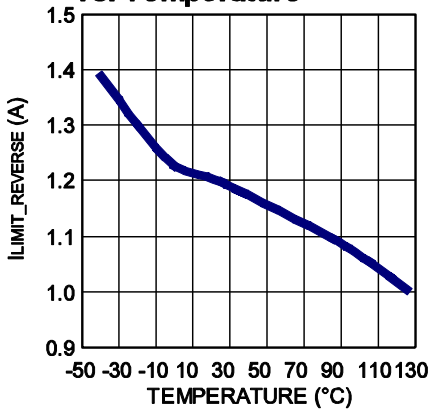
Max Duty Cycle vs. Temperature



Current Limit vs. Temperature

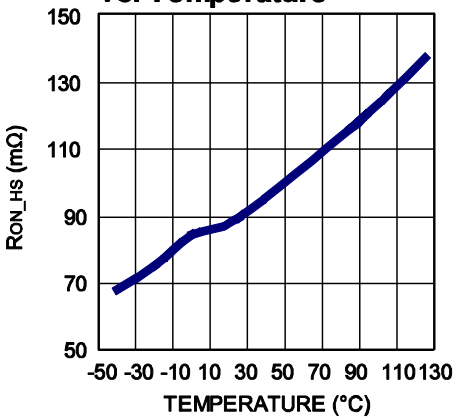
Valley Current Limit vs. Temperature

Reverse Current Limit vs. Temperature

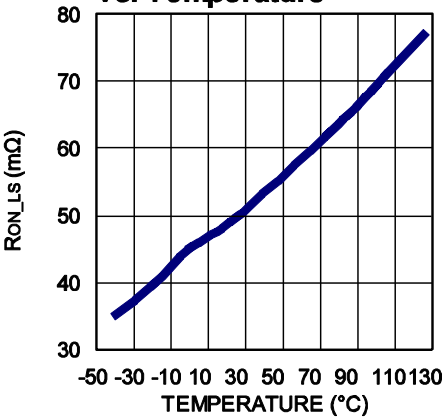


TYPICAL CHARACTERISTICS *(continued)*

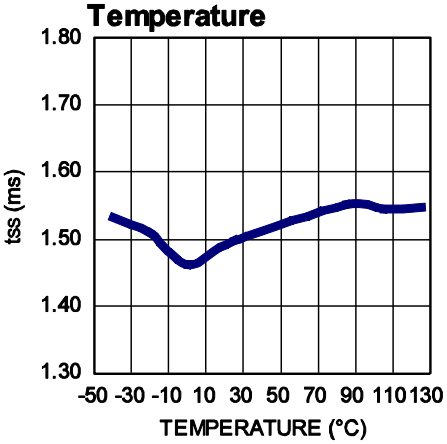
HS-FET On Resistance vs. Temperature



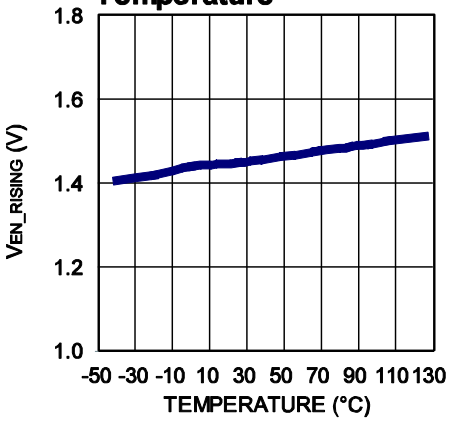
LS-FET On Resistance vs. Temperature



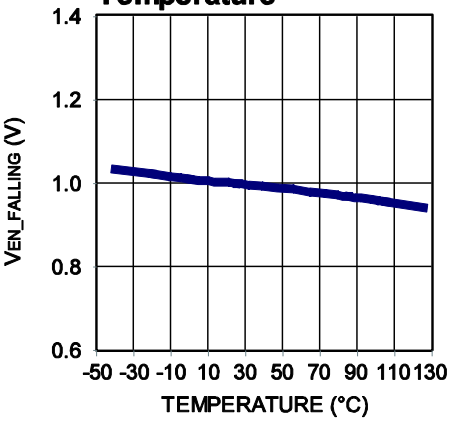
Soft-Start Time vs. Temperature



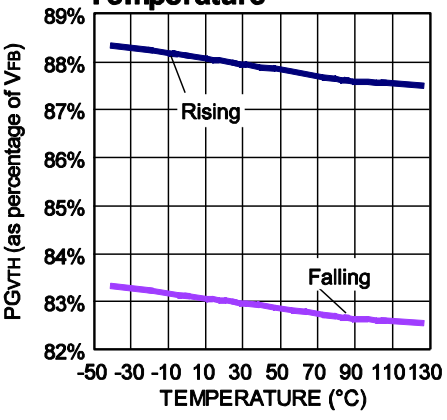
EN Rising Threshold vs. Temperature



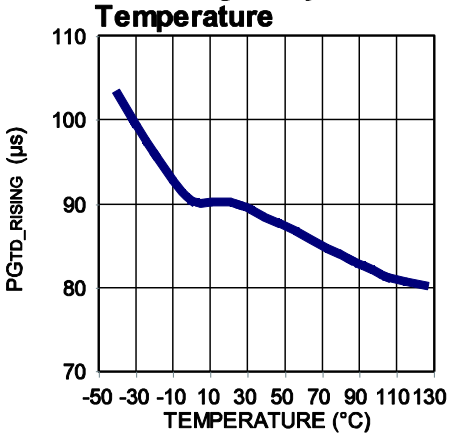
EN Falling Threshold vs. Temperature



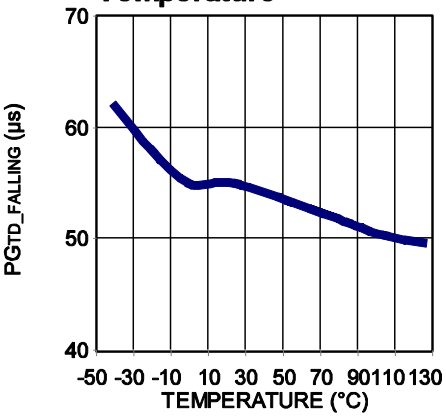
PG Threshold vs. Temperature



PG Rising Delay vs. Temperature



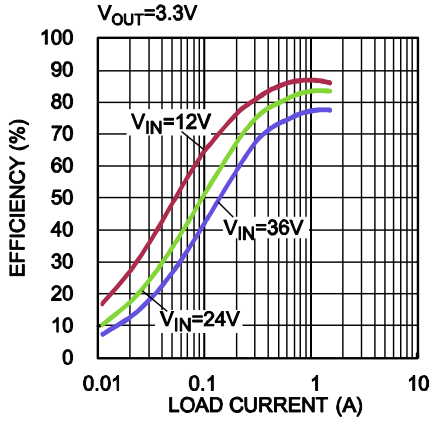
PG Falling Delay vs. Temperature



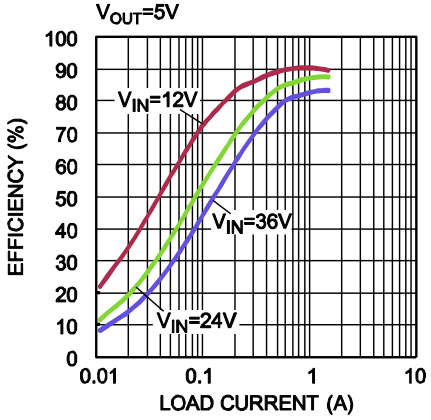
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 2.2µH, F_{SW} = 2.2MHz, T_A = +25°C, unless otherwise noted.

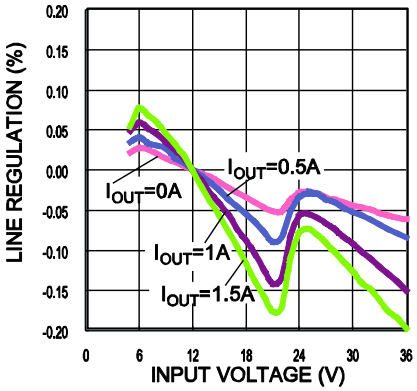
Efficiency vs. Load Current
V_{OUT}=3.3V



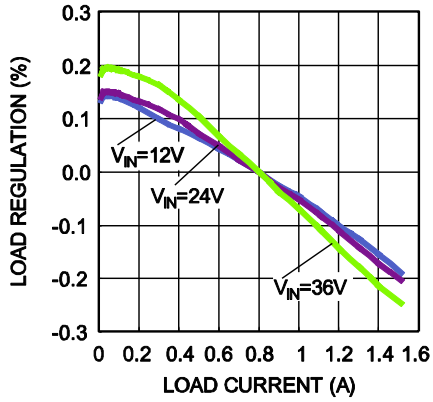
Efficiency vs. Load Current
V_{OUT}=5V



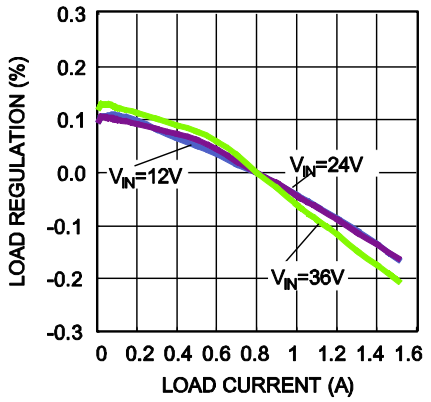
Line Regulation (6)
V_{OUT}=3.3V



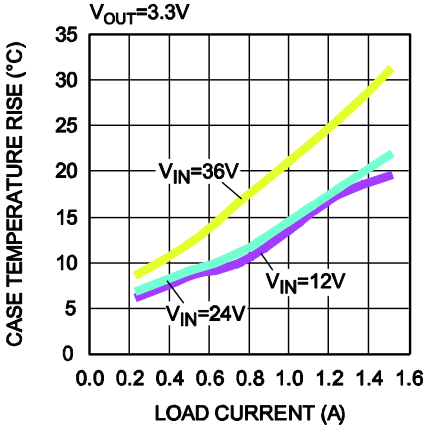
Load Regulation (6)
V_{OUT}=3.3V



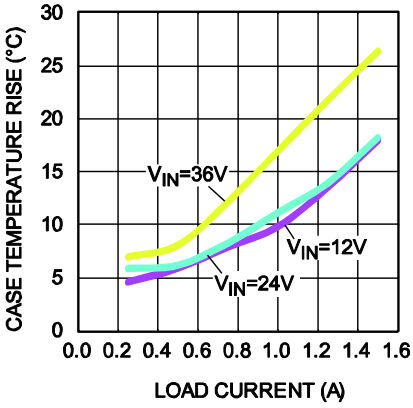
Load Regulation (6)
V_{OUT}=5V



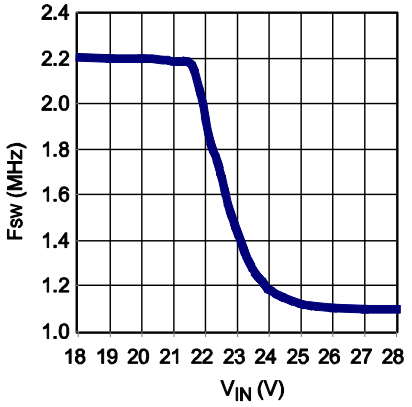
Case Temperature Rise vs. Load Current
V_{OUT}=3.3V



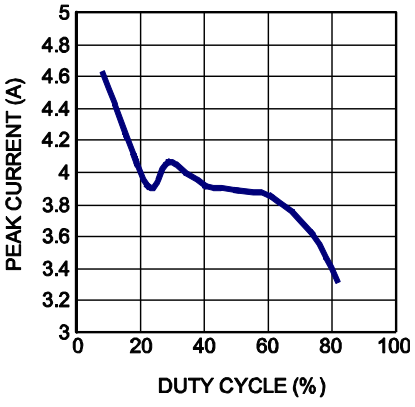
Case Temperature Rise vs. Load Current
V_{OUT}=5V



Frequency vs. V_{IN}



Peak Current vs. Duty Cycle



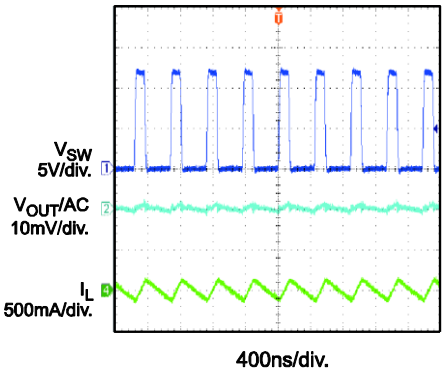
NOTES:

6) The load/line regulation diagrams do not take the feedback voltage accuracy into account.

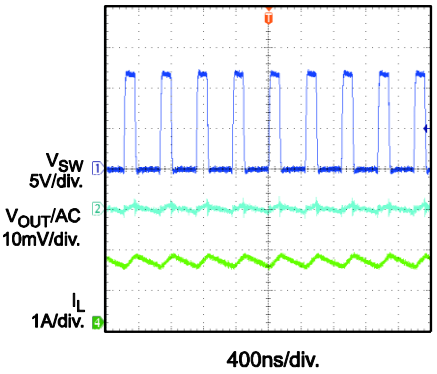
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 2.2µH, F_{SW} = 2.2MHz, T_A = +25°C, unless otherwise noted.

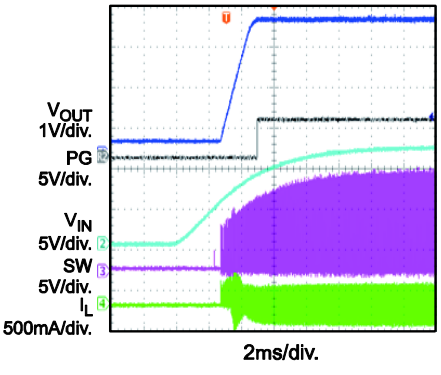
Steady State
I_{OUT}=0A



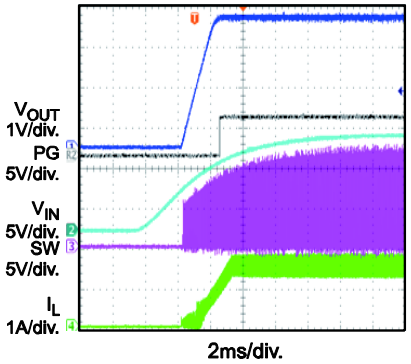
Steady State
I_{OUT}=1.5A



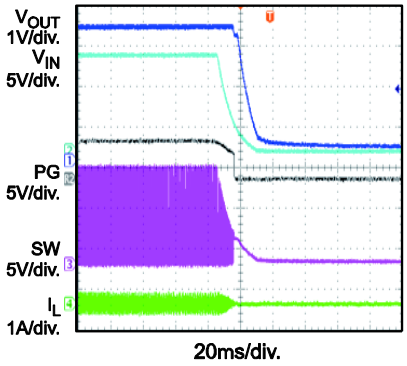
Start-Up through Input Voltage
I_{OUT}=0A



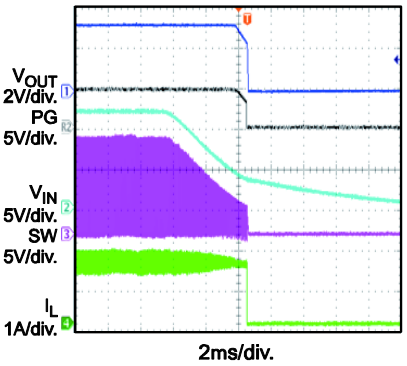
Start-Up through Input Voltage
I_{OUT}=1.5A



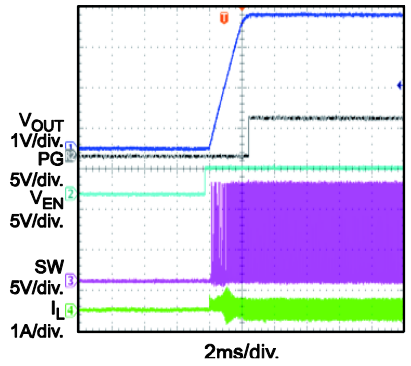
Shutdown through Input Voltage
I_{OUT} = 0A



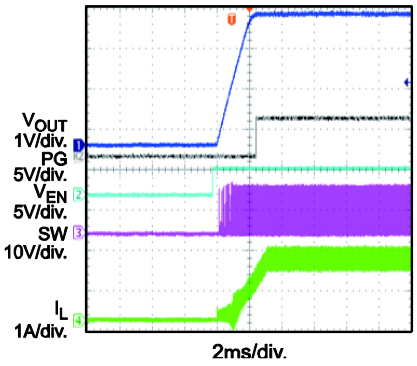
Shutdown through Input Voltage
I_{OUT}=1.5A



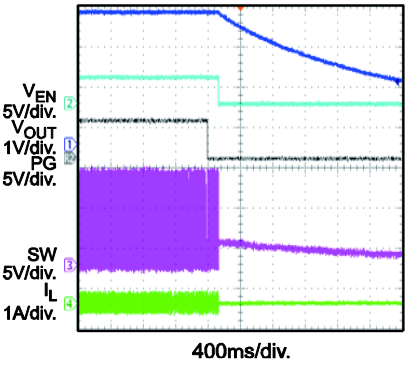
Start-Up through Enable
I_{OUT} = 0A



Start-Up through Enable
I_{OUT}=1.5A



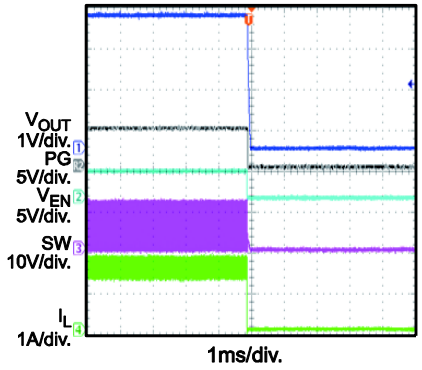
Shutdown through Enable
I_{OUT} = 0A



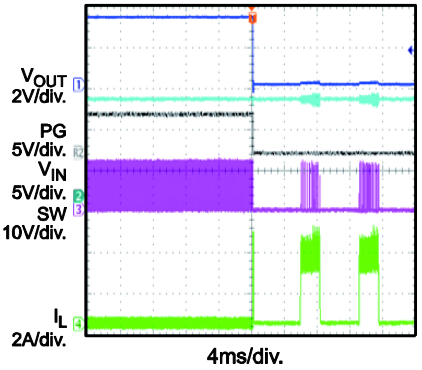
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 2.2µH, F_{SW} = 2.2MHz, T_A = +25°C, unless otherwise noted.

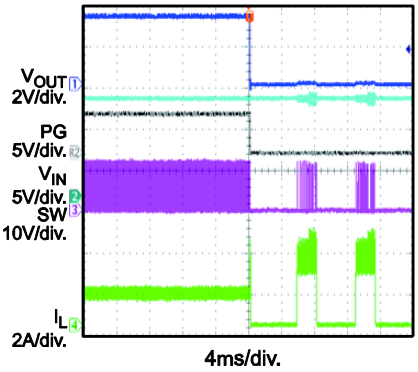
Shutdown through Enable
I_{OUT} = 1.5A



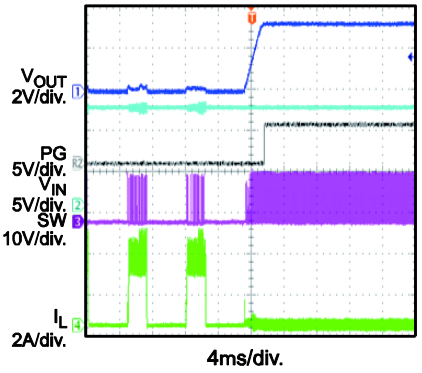
SCP Entry
I_{OUT} = 0A



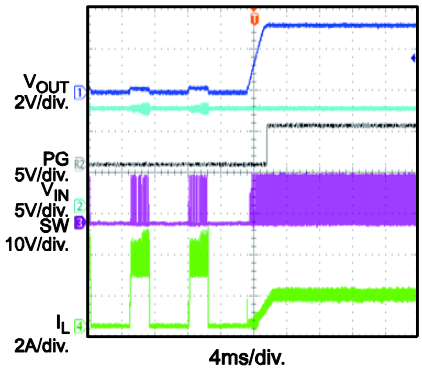
SCP Entry
I_{OUT} = 1.5A



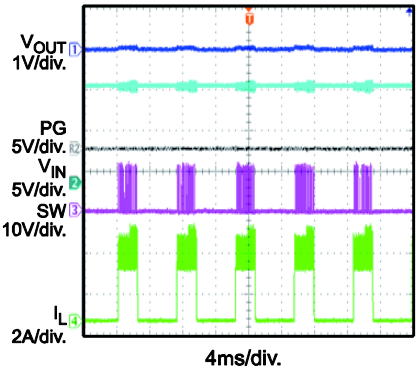
SCP Recovery
I_{OUT} = 0A



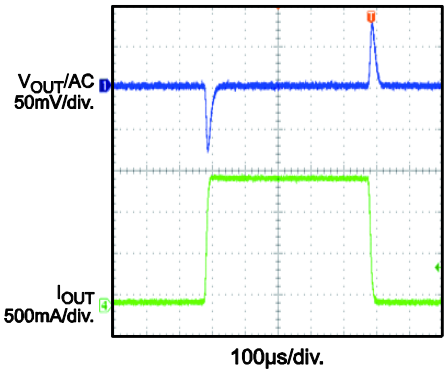
SCP Recovery
I_{OUT} = 1.5A



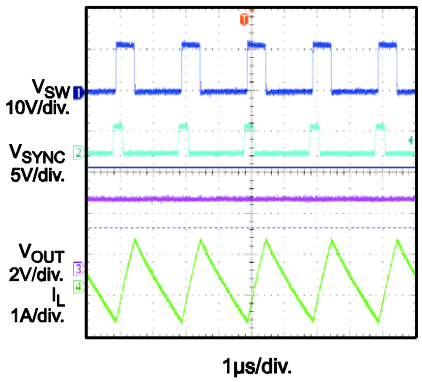
SCP Steady State



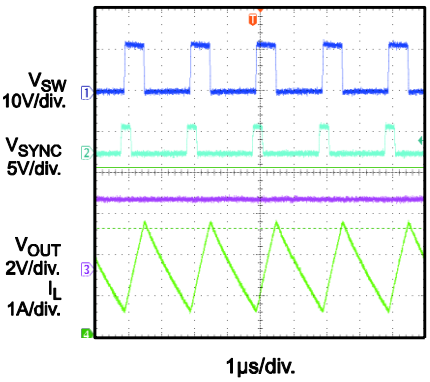
Load Transient
I_{OUT} = 0A-1.5A



SYNC Operation
f_{SYNC}=500kHz, D=15%, I_{OUT}=0A



SYNC Operation
f_{SYNC}=500kHz, D=15%, I_{OUT}=1.5A



BLOCK DIAGRAM

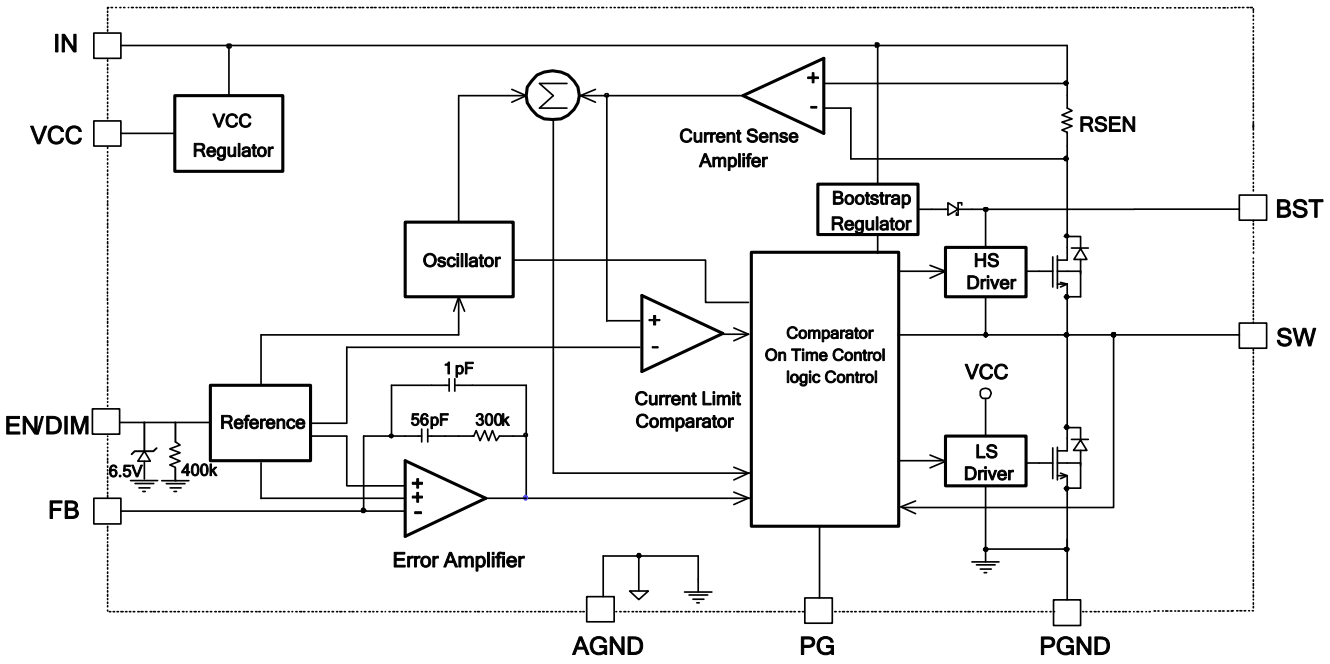


Figure 1: Functional Block Diagram

OPERATION

The MPQ4415A is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. The MPQ4415A offers a very compact solution that achieves 1.5A of continuous output current with excellent load and line regulation over a 4V to 36V input supply range.

The MPQ4415A operates in a fixed frequency, peak-current-control mode to regulate the output voltage. An internal clock initiates a pulse-width modulation (PWM) cycle. The integrated high-side power MOSFET (HS-FET) turns on and remains on until the current reaches the value set by the COMP voltage (V_{COMP}). When the power switch is off, it remains off until the next clock cycle begins. If the current in the power MOSFET does not reach the value set by V_{COMP} within 85% of one PWM period, the power MOSFET is forced off.

Internal Regulator

A 4.9V internal regulator powers most of the internal circuitries. This regulator takes V_{IN} as the input and operates in the full V_{IN} range. When V_{IN} exceeds 4.9V, the output of the regulator is in full regulation. When V_{IN} falls below 4.9V, the output decreases following V_{IN}. A 0.1µF decoupling ceramic capacitor is required at VCC.

Continuous Conduction Mode (CCM) Operation

The MPQ4415A uses continuous conduction modulation (CCM) mode to ensure that the part works with a fixed frequency from a no load to a full load range. The advantage of CCM is the controllable frequency and lower output ripple at light load.

Frequency Foldback

The MPQ4415A enters frequency foldback when the input voltage is higher than about 21V. The frequency decreases to half the nominal value and changes to 1.1MHz.

Frequency foldback also occurs during soft-start and short-circuit protection.

Error Amplifier (EA)

The error amplifier (EA) compares the FB voltage to the internal 0.807V reference (V_{REF}) and outputs a current proportional to the difference between the two. This output current then charges or discharges the internal compensation network to form V_{COMP}, which controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 3.5V with a 330mV hysteresis.

Enable/SYNC

EN/SYNC is a control pin that turns the regulator on and off. Drive EN/SYNC high to turn on the regulator; drive EN/SYNC low to turn off the regulator. An internal 400kΩ resistor from EN/SYNC to GND allows EN/SYNC to be floated to shut down the chip.

EN/SYNC is clamped internally using a 6.5V series Zener diode (see Figure 2). Connecting the EN/SYNC input through a pull-up resistor to the voltage on V_{IN} limits the EN input current to less than 100µA. For example, with 12V connected to V_{IN}, $R_{PULLUP} \geq (12V - 6.5V) \div 100\mu A = 55k\Omega$.

Connecting EN/SYNC to a voltage source directly without a pull-up resistor requires limiting the amplitude of the voltage source to ≤6V to prevent damage to the Zener diode.

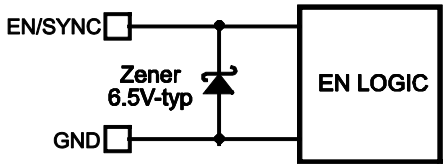


Figure 2: 6.5V Zener Diode Connection

Connect an external clock with a range of 450kHz to 2.2MHz to synchronize the internal clock rising edge to the external clock rising edge. The pulse width of the external clock signal should be below 350ns; the off time of the external clock signal should be below 1.9µs.

Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (V_{SS}). When V_{SS} is lower than the internal reference (V_{REF}), V_{SS} overrides V_{REF}, so the error amplifier uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the error amplifier uses V_{REF} as the reference. The SS time is set to 1.5ms internally.

Power Good (PG)

The MPQ4415A has a power good (PG) indicator. PG is the open drain of a MOSFET and should be connected to VCC or another voltage source through a resistor (e.g.: 100kΩ). In the presence of an input voltage, the MOSFET turns on, and PG is pulled low before SS is ready. After V_{FB} reaches 88% x V_{REF}, PG is pulled high after a typical 90μs delay. When V_{FB} drops to 83% x V_{REF}, PG is pulled low. PG is also pulled low if thermal shutdown occurs or EN/SYNC is pulled low.

Over-Current Protection (OCP) and Hiccup

The MPQ4415A has cycle-by-cycle peak current limit protection and valley current detection protection. The inductor current is monitored during the HS-FET on state. If the inductor current exceeds the current limit value set by the COMP high-clamp voltage, the HS-FET turns off immediately. Then the low-side MOSFET (LS-FET) turns on to discharge the energy, and the inductor current decreases. The HS-FET remains off unless the inductor valley current is lower than a certain current threshold (the valley current limit), even though the internal clock pulses high. If the inductor current does not drop below the valley current limit when the internal clock pulses high, the HS-FET misses the clock, and the switching frequency decreases to half the nominal value. Both the peak and valley current limits assist in keeping the inductor current from running away during an overload or short-circuit condition.

If the output voltage drops below the under-voltage (UV) threshold (typically 50% below the reference), the peak current limit is kicked simultaneously, then the MPQ4415A enters hiccup mode to restart the part periodically. This protection mode is useful when the output is dead-shorted to ground and reduces the average short-circuit current greatly to alleviate thermal issues and protect the regulator. The MPQ4415A exits hiccup mode once the over-current condition is removed.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the die temperature exceeds 170°C, the entire chip shuts down. When the temperature drops below its lower threshold (typically 140°C), the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. The floating driver has its own UVLO protection with a rising threshold of 2.2V and hysteresis of 150mV. A dedicated internal regulator charges and regulates the bootstrap capacitor voltage to ~5V (see Figure 3). When the voltage between the BST and SW nodes drops below regulation, a PMOS pass transistor connected from V_{IN} to BST turns on. The charging current path is from V_{IN} to BST and then to SW. The external circuit should provide enough voltage headroom to facilitate charging. As long as V_{IN} is significantly higher than SW, the bootstrap capacitor remains charged. When the HS-FET is on, $V_{IN} \approx V_{SW}$, the bootstrap capacitor cannot be charged. When the LS-FET is on, $V_{IN} - V_{SW}$ reaches its maximum for fast charging. When there is no inductor current, $V_{SW} = V_{OUT}$, the difference between V_{IN} and V_{OUT} can charge the bootstrap capacitor. A 20Ω resistor placed between the SW and BST capacitor is strongly recommended to reduce SW voltage spikes.

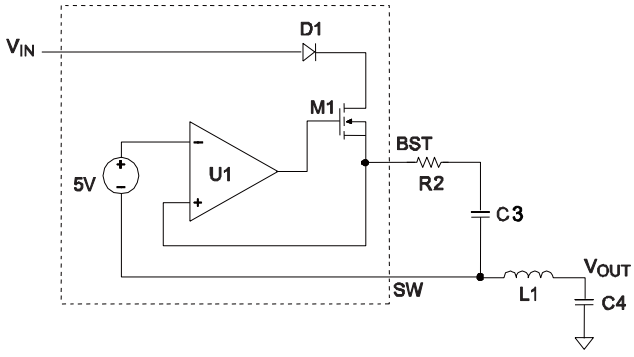


Figure 3: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both V_{IN} and EN/SYNC exceed their thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: V_{IN} low, EN/SYNC low, and thermal shutdown. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider connected to FB sets the output voltage (see Figure 4). The feedback resistor (R1) also sets the feedback loop bandwidth with the internal compensation capacitor. Choose R_{FB1} to be around 40kΩ when $V_{OUT} \geq 1V$. R_{FB2} can then be calculated with Equation (1):

$$R_{FB2} = \frac{R_{FB1}}{\frac{V_{OUT}}{0.807V} - 1} \quad (1)$$

The T-type network is highly recommended when V_{OUT} is low (see Figure 4).

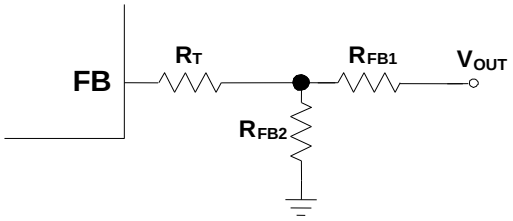


Figure 4: T-Type Feedback Network

$R_T + R_{FB1}$ is used to set the loop bandwidth. The lower $R_T + R_{FB1}$ is, the higher the bandwidth. However, a high bandwidth may cause an insufficient phase margin, resulting in loop instability. Therefore, a proper R_T value is required to make a trade-off between the bandwidth and phase margin. Table 1 lists the recommended feedback resistor and R_T values for common output voltages.

Table 1: Resistor Selection for Common Output

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)	R_T (kΩ)
3.3	41.2 (1%)	13 (1%)	20 (1%)
5	41.2 (1%)	7.68 (1%)	20 (1%)

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, use a 4.7µF to 10µF capacitor. It is strongly recommended to use another lower value capacitor (e.g.: 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to IN and GND as possible.

Since C_{IN} absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (2):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (2)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (3):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (3)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g.: 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by the capacitance can be estimated with Equation (4):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Use ceramic, tantalum, or low ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (5):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \cdot (1 - \frac{V_{OUT}}{V_{IN}}) \cdot (R_{ESR} + \frac{1}{8 f_{SW} \times C_{OUT}}) \quad (5)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (7)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ4415A can be optimized for a wide range of capacitance and ESR values.

Selecting the Inductor

A 1µH to 10µH inductor with a DC current rating at least 25% higher than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductor value is to allow the inductor ripple current to be approximately 30% of the maximum load current. The inductance value can then be calculated with Equation (8):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_{L}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (9):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

V_{IN} UVLO Setting

The MPQ4415A has an internal, fixed, under-voltage lockout (UVLO) threshold. The rising threshold is 3.5V, while the falling threshold is about 3.17V. For applications that require a higher UVLO point, an external resistor divider between IN and EN/SYNC can be used to achieve a higher equivalent UVLO threshold (see Figure 5).

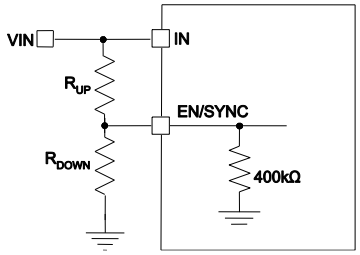


Figure 5: Adjustable UVLO using EN Divider

The UVLO threshold can be calculated with Equation (10) and Equation (11):

$$INUV_{RISING} = (1 + \frac{R_{UP}}{\frac{400k * R_{DOWN}}{400k + R_{DOWN}}}) \times V_{EN\_RISING} \quad (10)$$

$$INUV_{FALLING} = (1 + \frac{R_{UP}}{\frac{400k * R_{DOWN}}{400k + R_{DOWN}}}) \times V_{EN\_FALLING} \quad (11)$$

Where V_{EN_RISING} = 1.45V, and $V_{EN\_FALLING}$ = 1V.

When choosing R_{UP}, ensure that it is large enough to limit the current flowing into EN/SYNC below 100µA.

BST Resistor and External BST Diode

A 20Ω resistor in series with the BST capacitor is recommended to reduce SW voltage spikes. A higher resistance is better for SW spike reduction, but also compromises efficiency.

An external BST diode can enhance the efficiency of the regulator when the duty cycle is high (>65%). A power supply between 2.5V and 5V can be used to power the external bootstrap diode. VCC or V_{OUT} is recommended for this power supply in the circuit (see Figure 6).

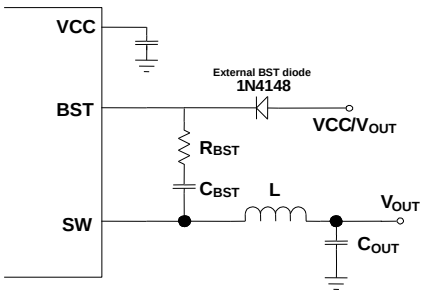


Figure 6: Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the recommended BST capacitor value is 0.1µF to 1µF.

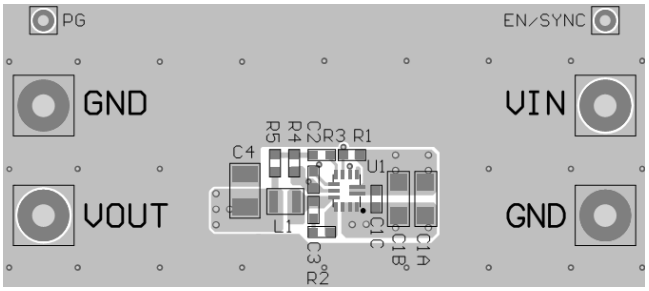
PCB Layout Guidelines [7]

Efficient PCB layout, especially regarding input capacitor placement, is critical for stable operation. A four-layer layout is strongly recommended to achieve better thermal performance. For best results, refer to Figure 7 and follow the guidelines below.

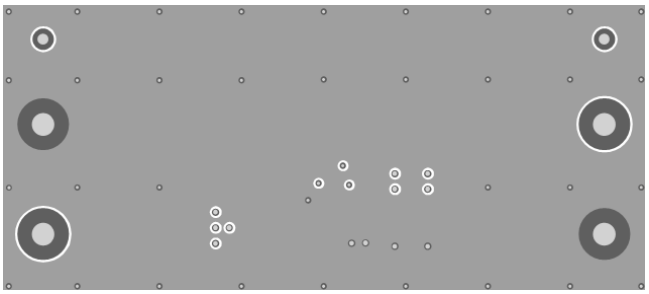
1. Use a large ground plane to connect directly to PGND. If the bottom layer is a ground plane, add vias near PGND.
2. Ensure that the high-current paths at GND and IN have short, direct, and wide traces.
3. Place the ceramic input capacitor, especially the small-sized input bypass capacitor (0603), as close to IN and PGND as possible to minimize high-frequency noise.
4. Keep the connection of the input capacitor and IN as short and wide as possible.
5. Place the VCC capacitor to VCC and AGND as close as possible.
6. Route SW and BST away from sensitive analog areas such as FB.
7. Place the feedback resistors close to the chip to ensure that the trace connecting to FB is as short as possible.
8. Use multiple vias to connect the power planes to internal layers.

NOTE:

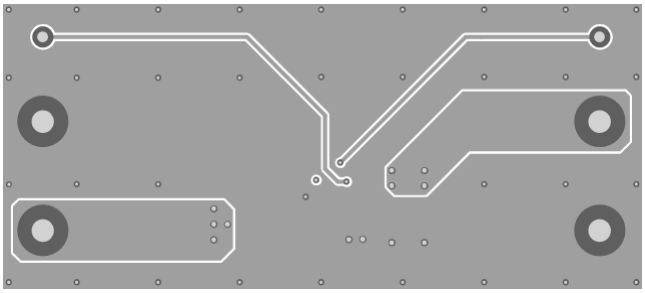
7) The recommended layout is based on Figure 7.



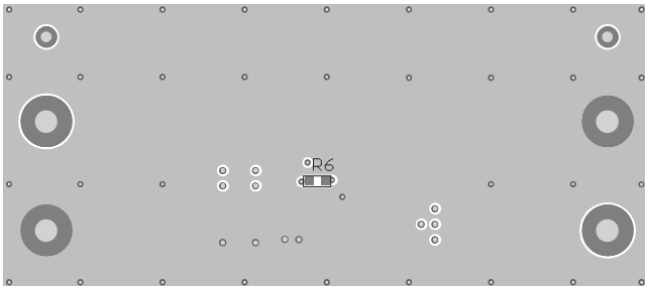
Top Layer



Inner Layer 1



Inner Layer 2



Bottom Layer

Figure 7: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

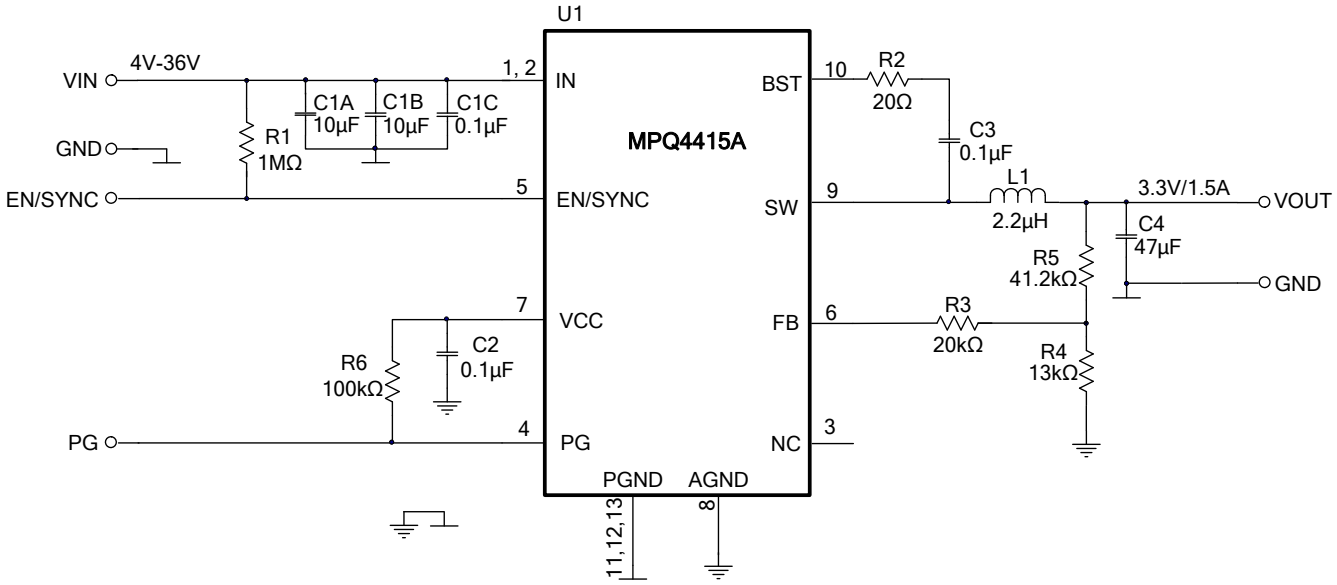


Figure 8: V_{OUT} = 3.3V, I_{OUT} = 1.5A

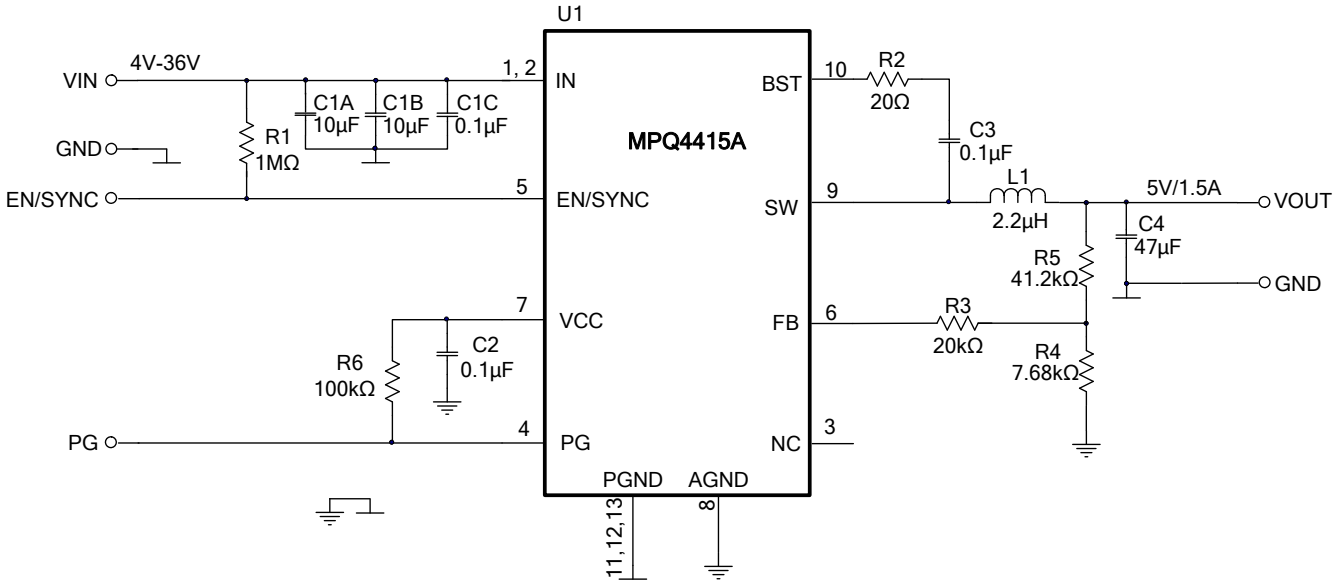


Figure 9: V_{OUT} = 5V, I_{OUT} = 1.5A

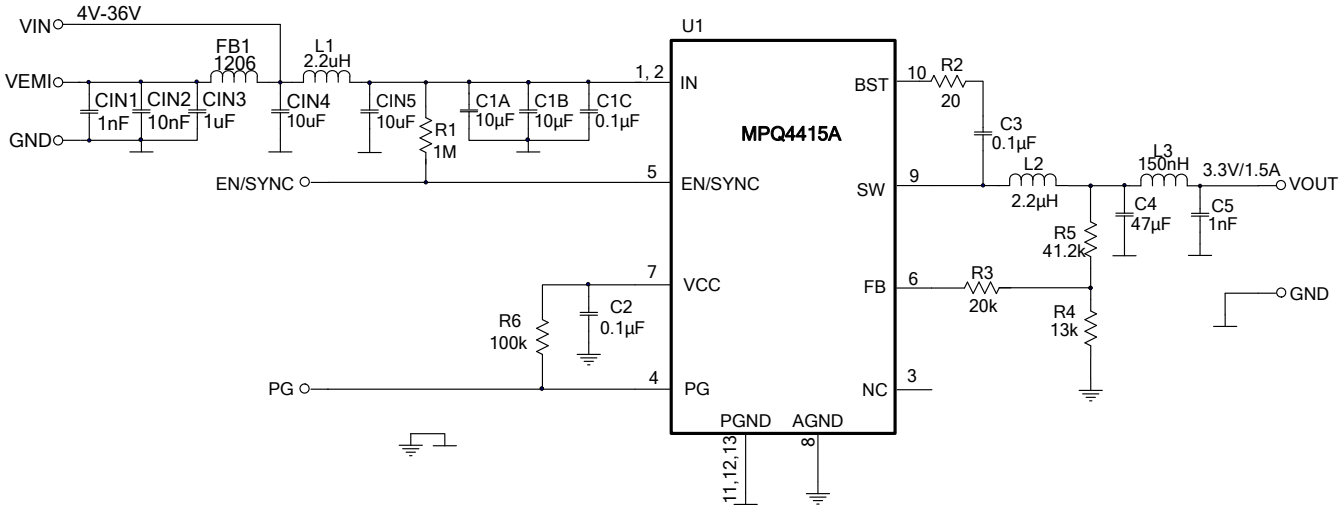
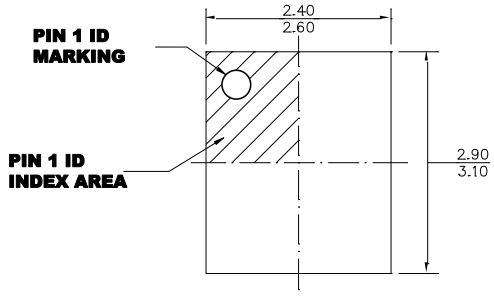


Figure 10: V_{OUT} = 3.3V, I_{OUT} = 1.5A, with EMI Filters

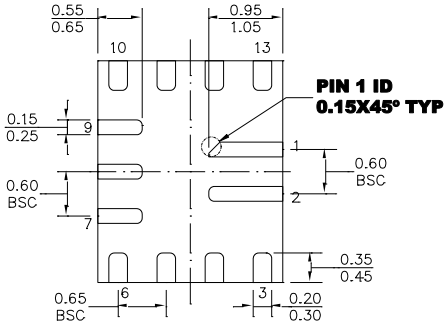
PACKAGE INFORMATION

QFN-13 (2.5mmx3mm)

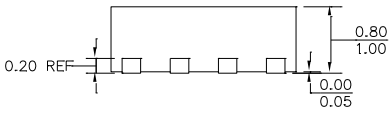
Non-Wettable Flank



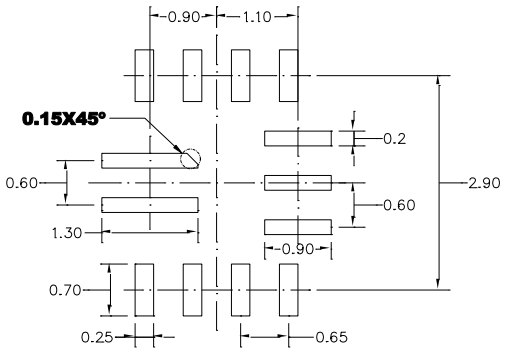
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.