



# MPQ4425B

High-Efficiency, 1.5A, 36V, 400kHz,  
Synchronous, Step-Down, LED Driver,  
AEC-Q100 Qualified

## DESCRIPTION

The MPQ4425B is a high-frequency, synchronous, rectified, step-down, switch-mode white LED driver with built-in power MOSFETs. It offers a compact solution to achieve a 1.5A of continuous output current with excellent load and line regulation over a wide input supply range. Synchronous mode operation ensures high efficiency, while current mode operation provides fast transient responses and eases loop stabilization. Additional features include over-current protection (OCP) and thermal shutdown (TSD).

This device requires a minimal number of readily available, external components, and is available in space-saving QFN-13 (2.5mmx3mm) and TSOT23-8 packages.

## FEATURES

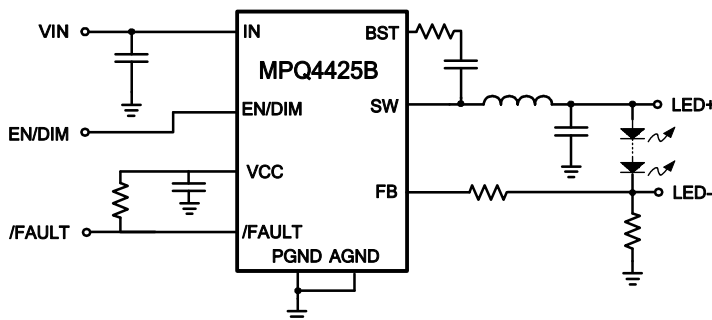
- Wide 4V to 36V Operating Input Range
- 85mΩ/50mΩ Low  $R_{DS(ON)}$  Internal Power MOSFETs
- High-Efficiency Synchronous Mode Operation
- Default 400kHz Switching Frequency
- PWM Dimming (Min 100Hz Dimming Frequency)
- Forced CCM Mode
- 0.2V Reference Voltage
- Internal Soft Start
- Fault Indication for LED Short, Open, and Thermal Shutdown
- Over-Current Protection (OCP) with Valley-Current Detection
- Thermal Shutdown
- CISPR25 Class 5 Compliant
- Available in QFN-13 (2.5mmx3mm) and TSOT23-8 Packages
- Available in AEC-Q100 Grade 1

## APPLICATIONS

- Automotive LED Lighting

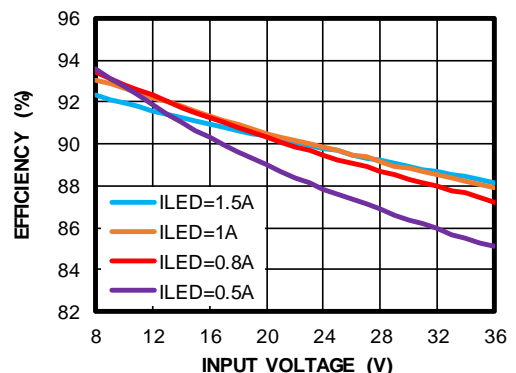
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## TYPICAL APPLICATION



### Efficiency vs. Input Voltage

$V_{LED} = 6.4V$



### ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ4425BGJ-AEC1***	TSOT23-8	<i>See Below</i>	<i>Level 1</i>
MPQ4425BGQB-AEC1	QFN-13 (2.5mmx3.0mm)		
MPQ4425BGQBE-AEC1****	QFN-13 (2.5mmx3.0mm)		

\* For Tape & Reel, add suffix -Z (e.g. MPQ4425BGJ-AEC1-Z).

\*\* Moisture Sensitivity Level Rating

\*\*\* Under Qualification

\*\*\*\*Wettable Flank

### TOP MARKING (MPQ4425BGJ-AEC1)

**| BHQY**

BHQ: Product code of MPQ4425BGJ-AEC1

Y: Year code

### TOP MARKING (MPQ4425BGQB-AEC1)

**—  
BFM  
YWW  
LLL**

BFM: Product code of MPQ4425BGQB-AEC1

Y: Year code

WW: Week code

LLL: Lot number

### TOP MARKING (MPQ4425BGQBE-AEC1)

**—  
BFQ  
YWW  
LLL**

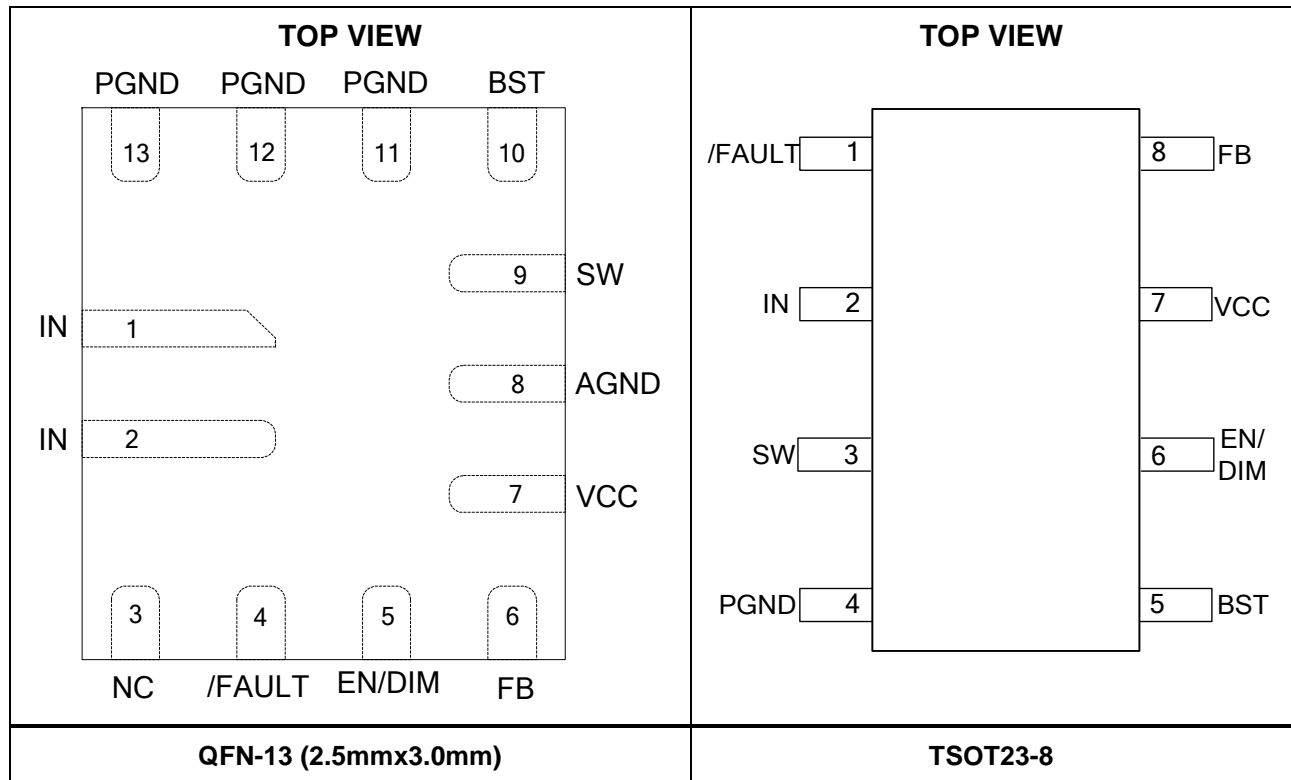
BFQ: Product code of MPQ4425BGQBE-AEC1

Y: Year code

WW: Week code

LLL: Lot number

## PACKAGE REFERENCE



## PIN FUNCTIONS

QFN-13 Pin #	TSOT23-8 Pin #	Name	Description
1, 2	2	IN	<b>Supply voltage.</b> The MPQ4425B operates from a 4V to 36V input rail. C <sub>IN</sub> is required to decouple the input rail. Connect using a wide PCB trace.
3		NC	<b>Do not connect.</b>
4	1	/FAULT	<b>Fault indicator.</b> Open-drain output. Pulled low during LED short circuit, open circuit, or thermal shutdown.
5	6	EN/DIM	<b>Enable/dimming control.</b> Pull EN high to enable the device. Apply a 100Hz to 2kHz external clock to the EN/DIM pin for PWM dimming.
6	8	FB	<b>LED current feedback input.</b>
7	7	VCC	<b>Internal bias supply.</b> Decouple VCC with a 0.1μF to 0.22μF capacitor. The capacitance should not exceed 0.22μF.
8		AGND	<b>Analog ground.</b> Reference ground of the logic circuit. AGND is connected to PGND internally. It is not necessary to externally connect AGND and PGND, but it is recommended for improved ground connection.
9	3	SW	<b>Switch output.</b> Connect using a wide PCB trace.
10	5	BST	<b>Bootstrap.</b> Requires a capacitor connected between the SW and BST pins to form a floating supply across the high-side switch driver. A 20Ω resistor placed between the SW and BST capacitors is strongly recommended to reduce SW spike voltage.
11, 12, 13	4	PGND	<b>Power ground.</b> PGND is the reference ground of the power device, and requires careful consideration during PCB layout. For optimal results, connect PGND with copper pours and vias.

**ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>**

Supply voltage ( $V_{IN}$ ) .....	-0.3V to +40V
Switch voltage ( $V_{SW}$ ) .....	-0.3V to $V_{IN} + 0.3V$
BST voltage ( $V_{BST}$ ) .....	$V_{SW} + 6V$
All other pins .....	-0.3V to +6V <sup>(2)</sup>
Continuous power dissipation ( $T_A = 25^\circ C$ ) <sup>(3)</sup>	
QFN-13 (2.5mmx3mm) .....	2.08W
TSOT23-8 .....	1.25W
Junction temperature .....	150°C
Lead temperature .....	260°C
Storage temperature .....	-65°C to +150°C

**Electrostatic Discharge (ESD)**

HBM (human body model) .....	±2kV
CDM (charged device model) .....	±750V

**Recommended Operating Conditions**

Supply voltage ( $V_{IN}$ ) .....	4V to 36V
LED current ( $I_{LED}$ ) .....	Up to 1.5A
Operating junction temp ( $T_J$ ) <sup>(4)</sup>	
.....	-40°C to +125°C

<b>Thermal Resistance</b>	<b><math>\theta_{JA}</math></b>	<b><math>\theta_{JC}</math></b>
<i>QFN-13 (2.5mmx3mm)</i>		
JESD51-7 <sup>(5)</sup> .....	60 .....	13 ... °C/W
EVQ4425B-QB-00A <sup>(6)</sup> .....	42 .....	2.5 .. °C/W
<i>TSOT23-8</i>		
JESD51-7 <sup>(5)</sup> .....	100 .....	55 ... °C/W
EVQ4425B-J-00A <sup>(6)</sup> .....	45 .....	3 ... °C/W

**Notes:**

- 1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
- 2) For details on the EN/DIM pin's ABS MAX ratings, see the Enable Control section on page 16.
- 3) The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J$  (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation causes excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 4) Operation of the device at a junction temperature up to 150°C is possible; contact MPS for details.
- 5) Measured on JESD51-7, 4-layer PCB. The value of  $\theta_{JA}$  given in this table is only valid for comparison with other packages and can't be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
- 6) Measure on MPS standard EVB of MPQ4425B, 4-layer PCB, 64mmx64mm.

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 12V$ ,  $V_{EN} = 2V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ ,  $T_J = 25^{\circ}C$ , unless otherwise noted.

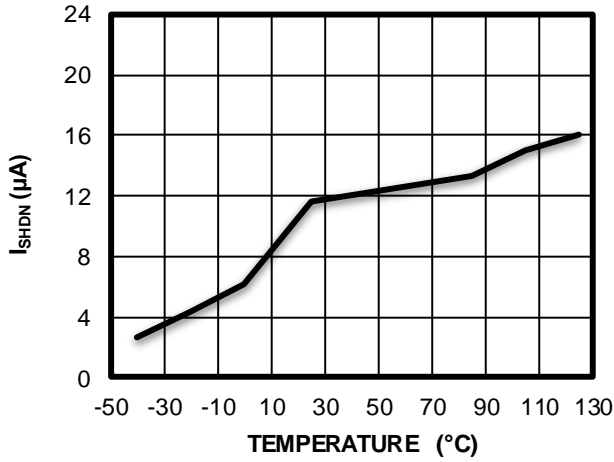
Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	$I_{IN}$	$V_{EN} = 0V$		12		$\mu A$
Supply current (quiescent)	$I_Q$	$V_{EN} = 2V$ , $V_{FB} = 1V$ , no switching		0.6	1	mA
HS switch on resistance	$HS_{RDS-ON}$	$V_{BST-SW} = 5V$		85	150	m $\Omega$
LS switch on resistance	$LS_{RDS-ON}$	$V_{CC} = 5V$		50	105	m $\Omega$
Switch leakage	$SW_{LKG}$	$V_{EN} = 0V$ , $V_{SW} = 12V$			2	$\mu A$
Current limit <sup>(7)</sup>	$I_{LIMIT}$	Under 40% duty cycle	3.6	5.7	7.8	A
Reverse current limit				3.5		A
Oscillator frequency	$f_{SW}$	$V_{FB} = 100mV$	300	400	500	kHz
Maximum duty cycle	$D_{MAX}$	$V_{FB} = 100mV$	92	95		%
Minimum on time <sup>(7)</sup>	$t_{ON\_MIN}$			46		ns
Feedback voltage	$V_{FB}$	$T_J = 25^{\circ}C$	192	200	208	mV
		$T_J = -40^{\circ}C$ to $+125^{\circ}C$	184	200	216	
Feedback current	$I_{FB}$	$V_{FB} = 250mV$		30	100	nA
EN rising threshold	$V_{EN\_RISING}$		1.1	1.45	1.8	V
EN falling threshold	$V_{EN\_FALLING}$		0.7	1	1.3	V
EN threshold hysteresis	$V_{EN\_HYS}$			450		mV
EN input current	$I_{EN}$	$V_{EN} = 2V$		5	10	$\mu A$
		$V_{EN} = 0$		0	0.2	$\mu A$
EN turn-off delay	$EN_{td-off}$		10	25	50	ms
VIN under-voltage lockout rising threshold	$INUV_{Vth}$		3.2	3.5	3.8	V
VIN under-voltage lockout falling threshold			2.8	3.1	3.5	V
VIN under-voltage lockout threshold hysteresis	$INUV_{HYS}$			400		mV
Over-voltage detection (/FAULT pulled low)	$FT_{Vth-Hi}$			140%		$V_{FB}$
Over-voltage detection hysteresis				20%		$V_{FB}$
/FAULT delay	$FT_{Td}$			10		$\mu s$
/FAULT sink current capability	$V_{FT}$	Sink 4mA			0.4	V
/FAULT leakage current	$I_{FT-LEAK}$				100	nA
VCC regulator	$V_{CC}$	$I_{CC} = 0mA$	4.6	4.9	5.2	V
VCC load regulation		$I_{CC} = 5mA$		1.5	4	%
Soft-start time <sup>(7)</sup>	$t_{SS}$	$I_{LED} = 1.5A$ , $L = 6.8\mu H$ , load = 2 series LED, $I_{LED}$ from 10% to 90%		0.9		ms
Thermal shutdown <sup>(7)</sup>			150	170		$^{\circ}C$
Thermal hysteresis <sup>(7)</sup>				30		$^{\circ}C$

**Note:**

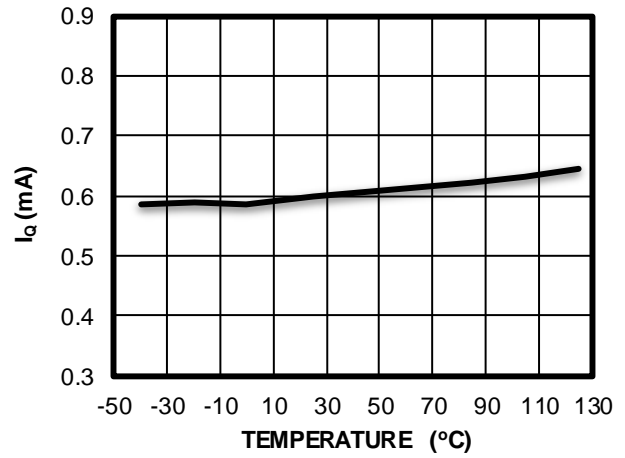
7) Derived from bench characterization. Not tested in production.

## TYPICAL CHARACTERISTICS

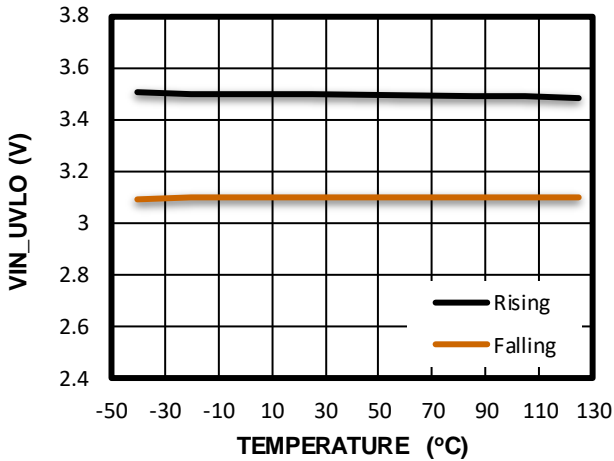
Shutdown Current vs. Temperature



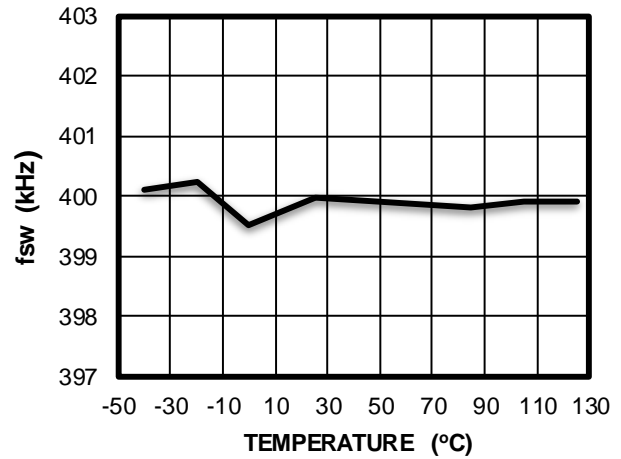
Quiescent Current vs. Temperature



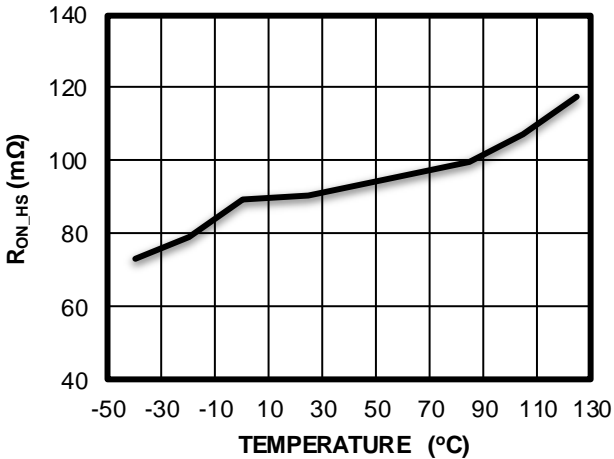
VIN UVLO Threshold vs. Temperature



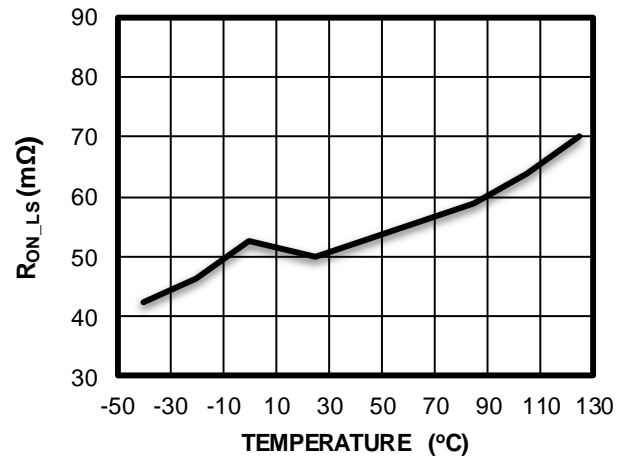
Switching Frequency vs. Temperature

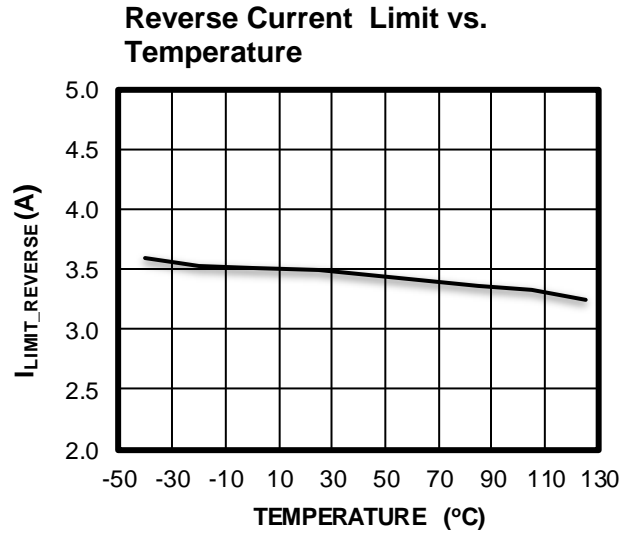
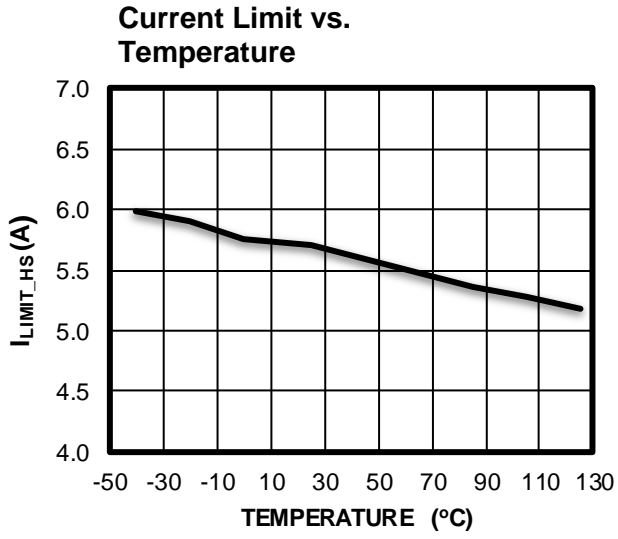


HS-FET On Resistance vs. Temperature



LS-FET On Resistance vs. Temperature

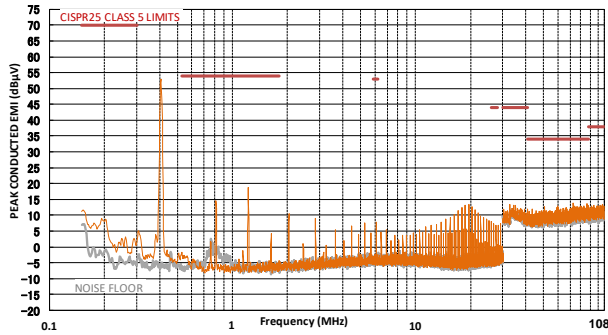


**TYPICAL CHARACTERISTICS (continued)**


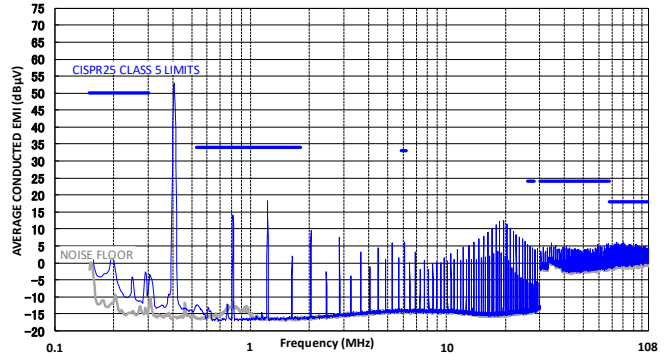
## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 12V$ ,  $V_{LED+} - V_{LED-} = 2 \times 3.2V$  @  $I_{LED} = 1.5A$ ,  $L = 10\mu H$ ,  $f_{sw} = 400kHz$ , with EMI filters,  $T_A = 25^\circ C$ , unless otherwise noted.

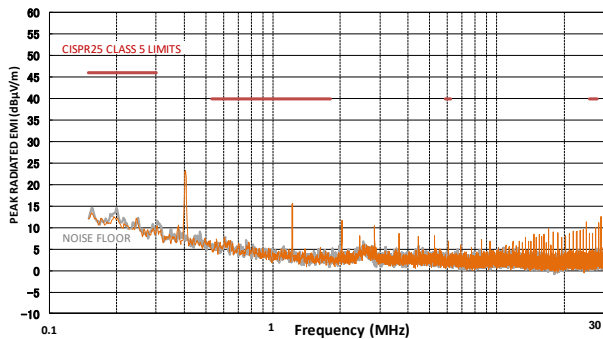
**CISPR25 Class 5 Peak Conducted Emissions**  
150kHz to 108MHz



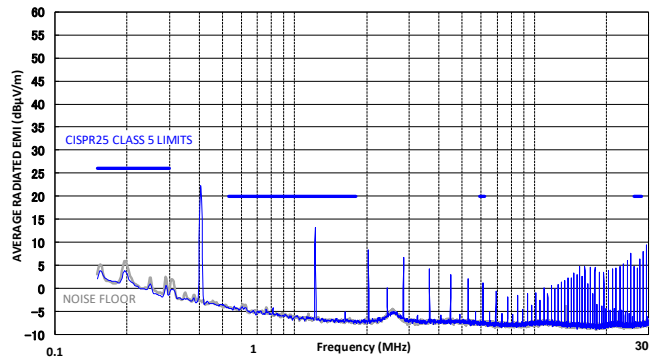
**CISPR25 Class 5 Average Conducted Emissions**  
150kHz to 108MHz



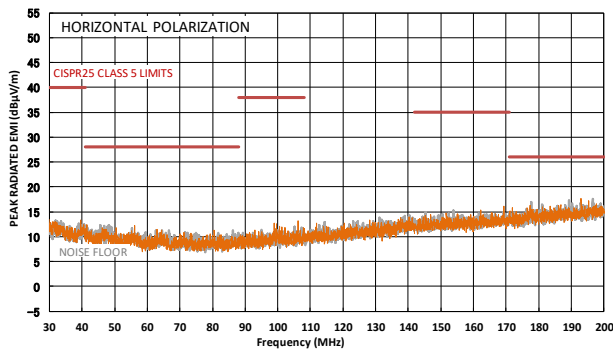
**CISPR25 Class 5 Peak Radiated Emissions**  
150kHz to 30MHz



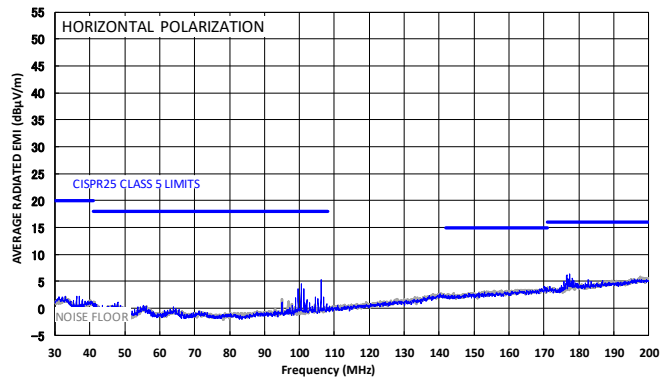
**CISPR25 Class 5 Average Radiated Emissions**  
150kHz to 30MHz



**CISPR25 Class 5 Peak Radiated Emissions**  
Horizontal, 30MHz to 200MHz



**CISPR25 Class 5 Average Radiated Emissions**  
Horizontal, 30MHz to 200MHz



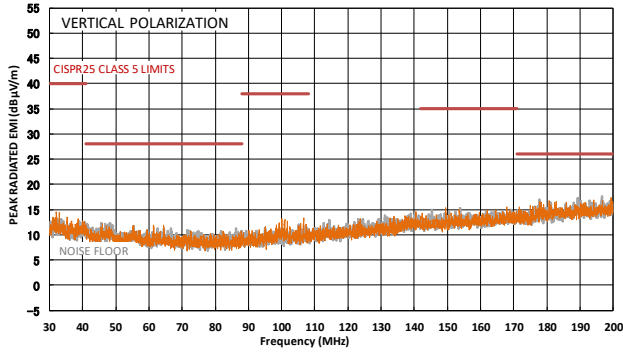


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 12V$ ,  $V_{LED+} - V_{LED-} = 2 \times 3.2V$  @  $I_{LED} = 1.5A$ ,  $L = 10\mu H$ ,  $f_{sw} = 400kHz$ , with EMI filters,  $T_A = 25^\circ C$ , unless otherwise noted.

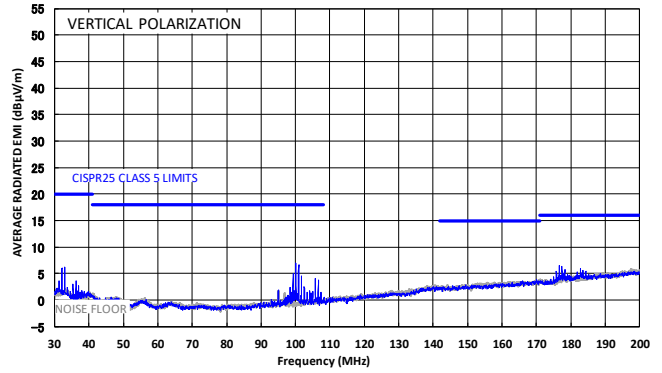
### CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 200MHz



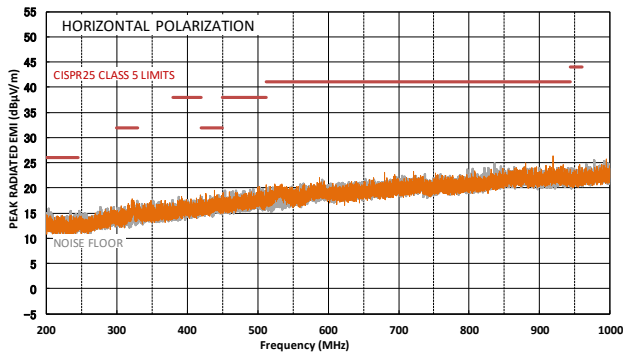
### CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 200MHz



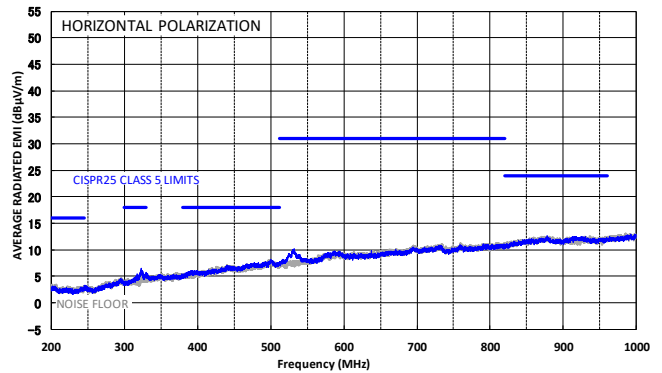
### CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 200MHz to 1GHz



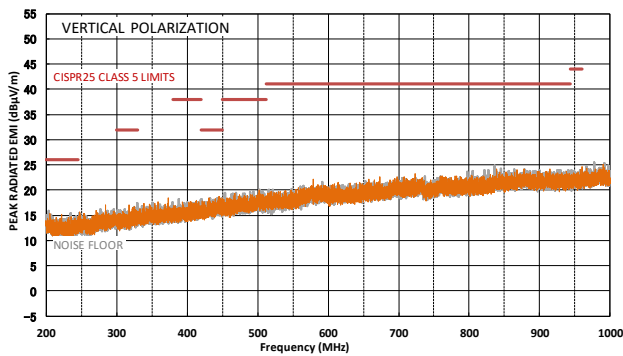
### CISPR25 Class 5 Average Radiated Emissions

Horizontal, 200MHz to 1GHz



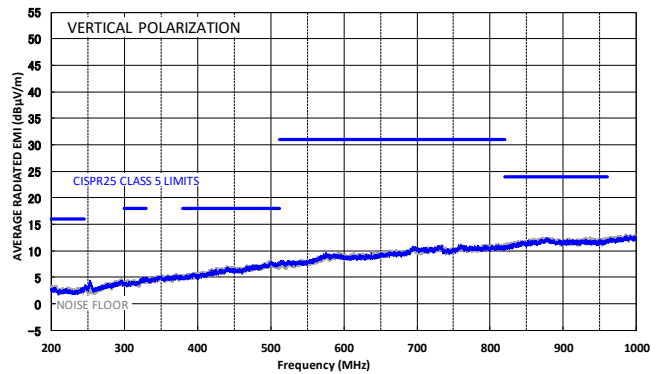
### CISPR25 Class 5 Peak Radiated Emissions

Vertical, 200MHz to 1GHz



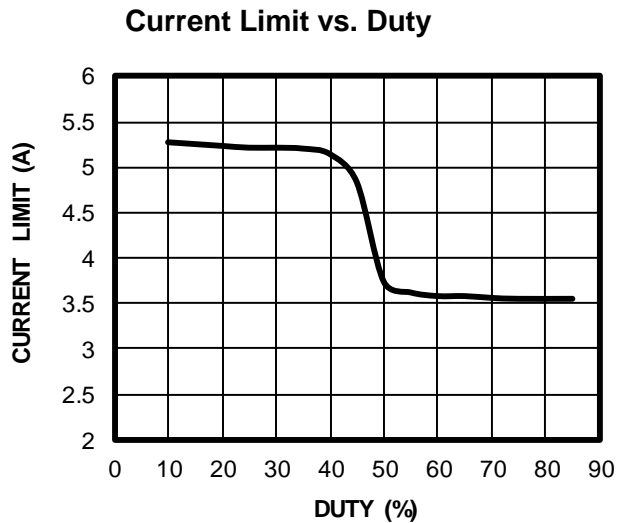
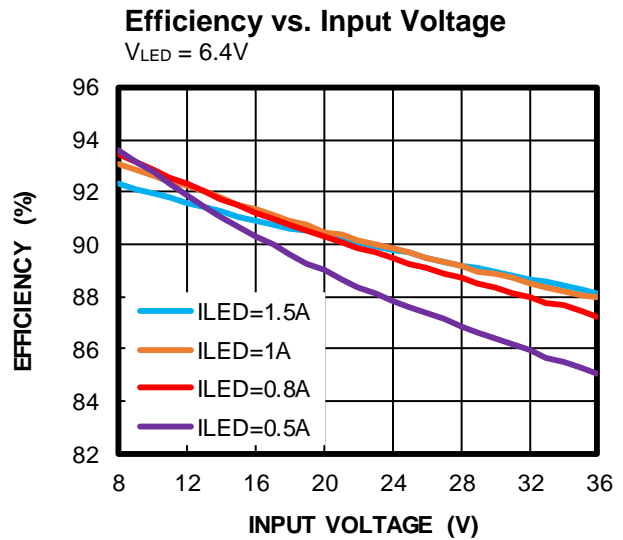
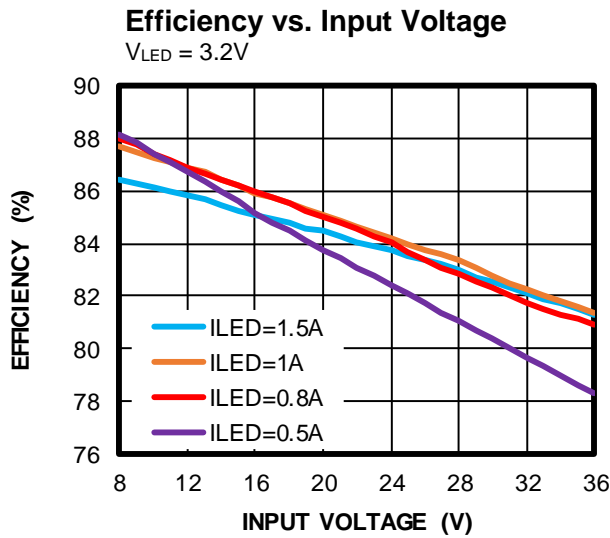
### CISPR25 Class 5 Average Radiated Emissions

Vertical, 200MHz to 1GHz



### TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 12V$ ,  $V_{LED+} - V_{LED-} = 2 \times 3.2V$  @  $I_{LED} = 1.5A$ ,  $L = 10\mu H$ ,  $f_{SW} = 400kHz$ , with EMI filters,  $T_A = 25^\circ C$ , unless otherwise noted.



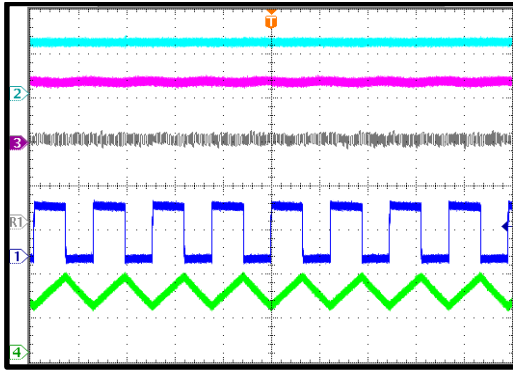
**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

$V_{IN} = 12V$ ,  $V_{LED+} - V_{LED-} = 2 \times 3.2V$  @  $I_{LED} = 1.5A$ ,  $L = 10\mu H$ ,  $f_{sw} = 400kHz$ , with EMI filters,  $T_A = 25^\circ C$ , unless otherwise noted.

**Steady State**
 $I_{LED} = 1.5A$ 

CH2:  $V_{OUT}$   
 5V/div.  
 CH3:  $I_{LED}$   
 1A/div.

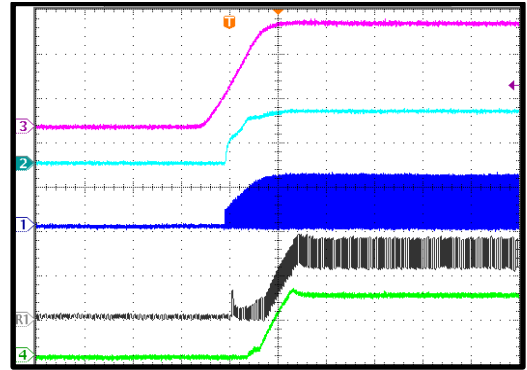
R1:  $V_{FAULT}$   
 2V/div.  
 CH1:  $V_{SW}$   
 10V/div.  
 CH4:  $I_L$   
 1A/div.


 2 $\mu s$ /div.

**Start-Up through  $V_{IN}$** 
 $I_{LED} = 1.5A$ 

CH3:  $V_{IN}$   
 5V/div.  
 CH2:  $V_{OUT}$   
 5V/div.

CH1:  $V_{SW}$   
 10V/div.  
 R1:  $I_L$   
 1A/div.  
 CH4:  $I_{LED}$   
 1A/div.

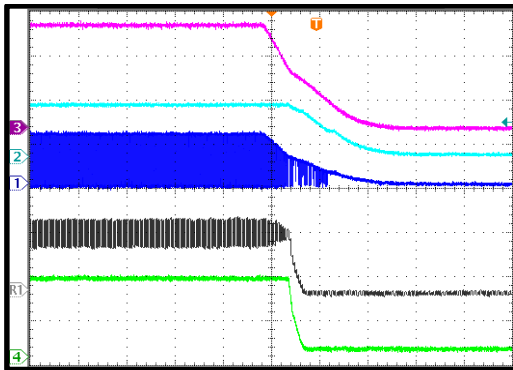


1ms/div.

**Shutdown through  $V_{IN}$** 
 $I_{LED} = 1.5A$ 

CH3:  $V_{IN}$   
 5V/div.  
 CH2:  $V_{OUT}$   
 5V/div.

CH1:  $V_{SW}$   
 10V/div.  
 R1:  $I_L$   
 1A/div.  
 CH4:  $I_{LED}$   
 1A/div.

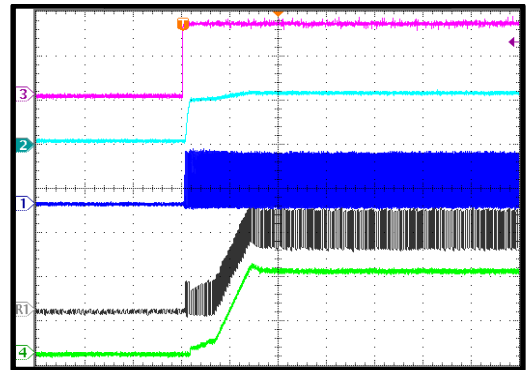


10ms/div.

**Start-Up through EN**
 $I_{LED} = 1.5A$ 

CH3:  $V_{ENDIM}$   
 2V/div.  
 CH2:  $V_{OUT}$   
 5V/div.

CH1:  $V_{SW}$   
 10V/div.  
 R1:  $I_L$   
 1A/div.  
 CH4:  $I_{LED}$   
 1A/div.

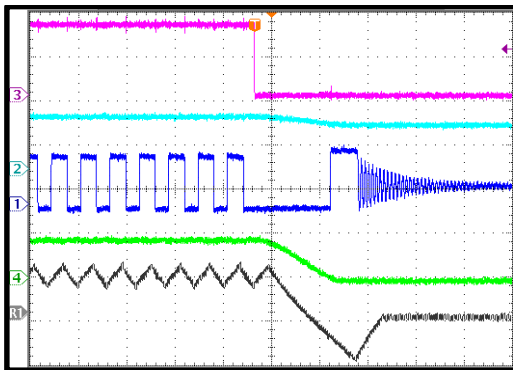


1ms/div.

**Shutdown through EN**
 $I_{LED} = 1.5A$ 

CH3:  $V_{ENDIM}$   
 2V/div.  
 CH2:  $V_{OUT}$   
 5V/div.

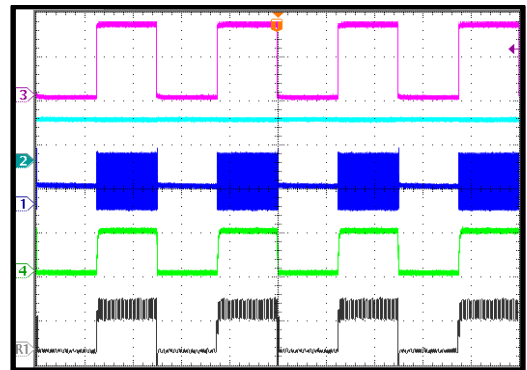
CH1:  $V_{SW}$   
 10V/div.  
 CH4:  $I_{LED}$   
 2A/div.  
 R1:  $I_L$   
 1A/div.


 4 $\mu s$ /div.

**PWM Dimming**
 $F_{PWM} = 200Hz$ 

CH3:  $V_{ENDIM}$   
 2V/div.  
 CH2:  $V_{FAULT}$   
 5V/div.

CH1:  $V_{SW}$   
 10V/div.  
 CH4:  $I_{LED}$   
 2A/div.  
 R1:  $I_L$   
 2A/div.



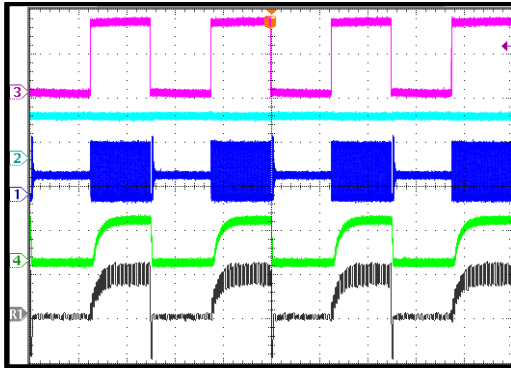
2ms/div.

**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

$V_{IN} = 12V$ ,  $V_{LED+} - V_{LED-} = 2 \times 3.2V$  @  $I_{LED} = 1.5A$ ,  $L = 10\mu H$ ,  $f_{sw} = 400kHz$ , with EMI filters,  $T_A = 25^\circ C$ , unless otherwise noted.

**PWM Dimming**
 $F_{PWM} = 2kHz$ 

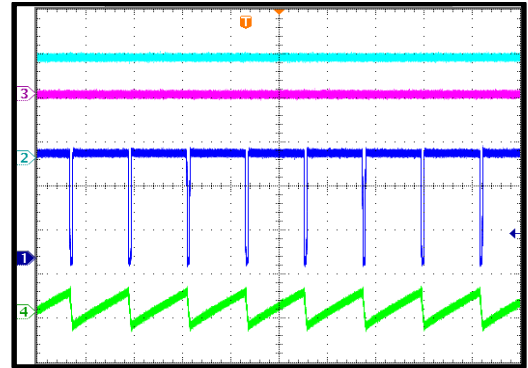
CH3:  $V_{ENDIM}$   
 2V/div.  
 CH2:  $V_{FAULT}$   
 5V/div.  
 CH1:  $V_{SW}$   
 10V/div.  
 CH4:  $I_{LED}$   
 2A/div.  
 R1:  $I_L$   
 2A/div.



200µs/div.

**LED Open Steady State**

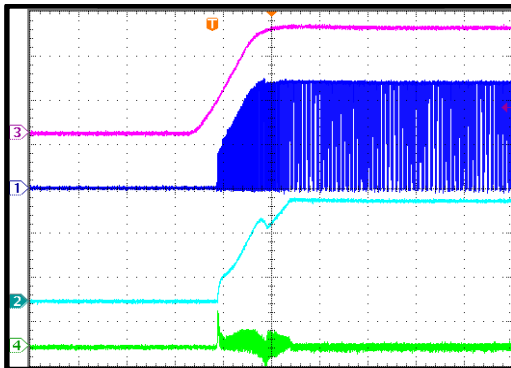
CH3:  $V_{FAULT}$   
 2V/div.  
 CH2:  $V_{OUT}$   
 5V/div.  
 CH1:  $V_{SW}$   
 5V/div.  
 CH4:  $I_L$   
 200mA/div.



2µs/div.

**LED Open Input Power-On**

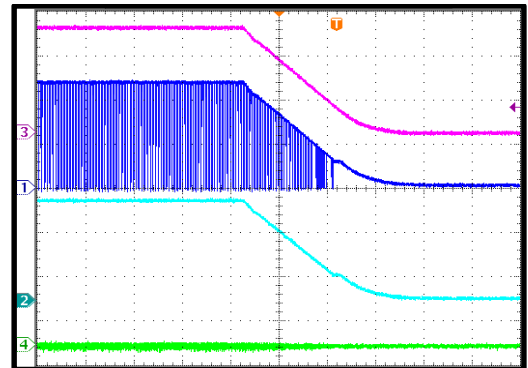
CH3:  $V_{IN}$   
 5V/div.  
 CH1:  $V_{SW}$   
 5V/div.  
 CH2:  $V_{OUT}$   
 5V/div.  
 CH4:  $I_L$   
 1A/div.



1ms/div.

**LED Open Input Power-Off**

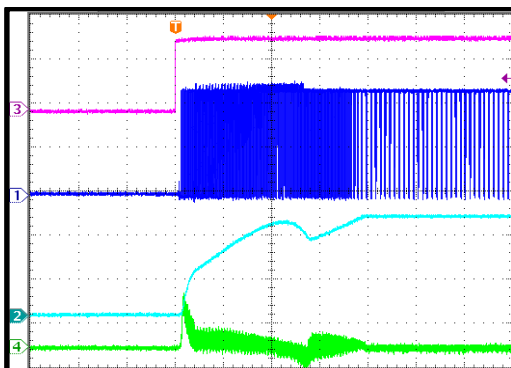
CH3:  $V_{IN}$   
 5V/div.  
 CH1:  $V_{SW}$   
 5V/div.  
 CH2:  $V_{OUT}$   
 5V/div.  
 CH4:  $I_L$   
 1A/div.



10ms/div.

**LED Open EN On**

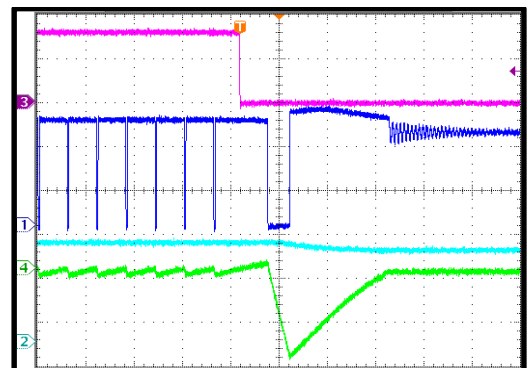
CH3:  $V_{ENDIM}$   
 2V/div.  
 CH1:  $V_{SW}$   
 5V/div.  
 CH2:  $V_{OUT}$   
 5V/div.  
 CH4:  $I_L$   
 1A/div.



400µs/div.

**LED Open EN Off**

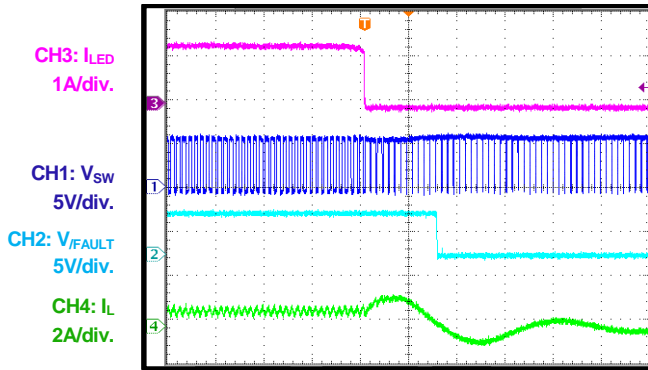
CH3:  $V_{ENDIM}$   
 2V/div.  
 CH1:  $V_{SW}$   
 5V/div.  
 CH4:  $I_L$   
 1A/div.  
 CH2:  $V_{OUT}$   
 5V/div.



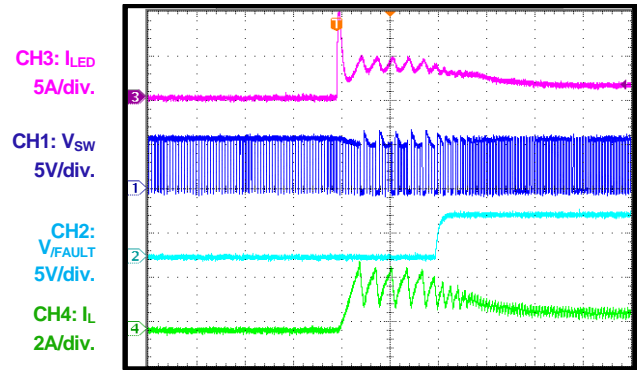
4µs/div.

**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

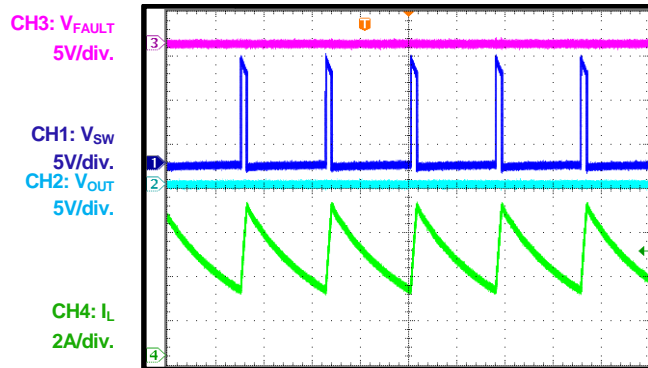
$V_{IN} = 12V$ ,  $V_{LED+} - V_{LED-} = 2 \times 3.2V$  @  $I_{LED} = 1.5A$ ,  $L = 10\mu H$ ,  $f_{sw} = 400kHz$ , with EMI filters,  $T_A = 25^\circ C$ , unless otherwise noted.

**LED Open Entry**
 $I_{LED} = 1.5A$ 


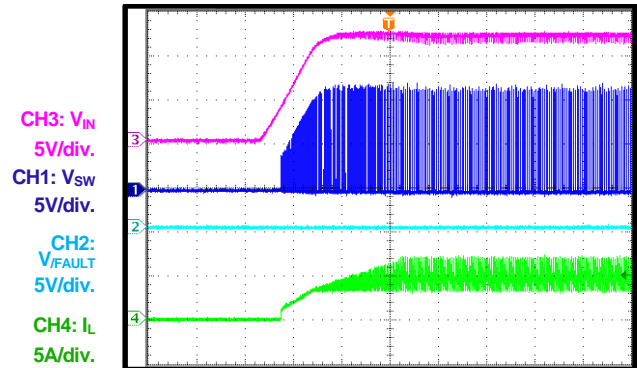
20µs/div.

**LED Open Recovery**
 $I_{LED} = 1.5A$ 


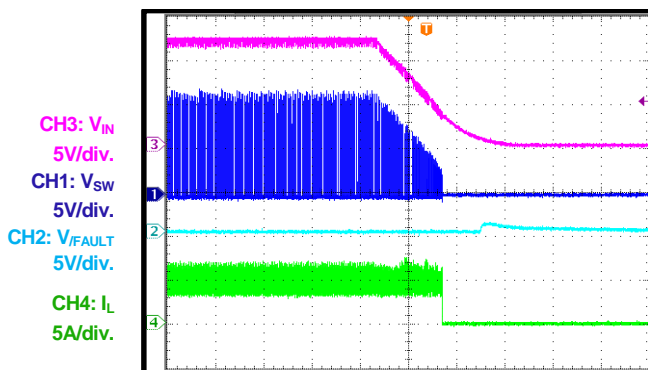
40µs/div.

**LED + Short to GND Steady State**


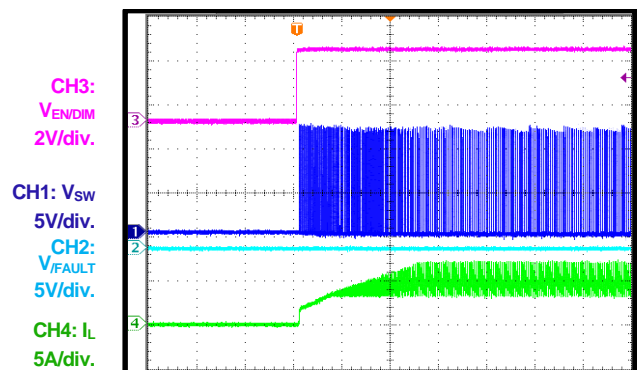
10µs/div.

**LED + Short to GND Input Power-On**


1ms/div.

**LED + Short to GND Input Power-Off**


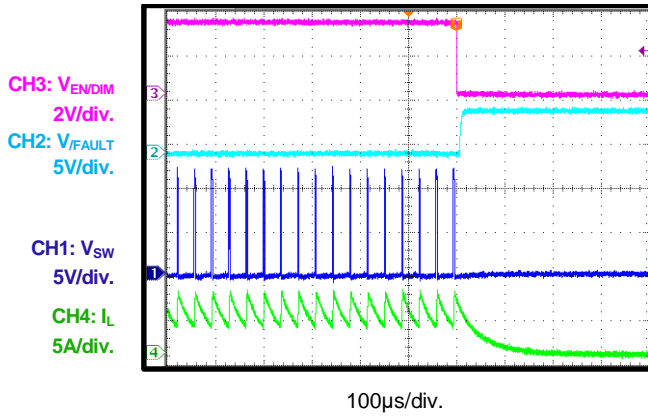
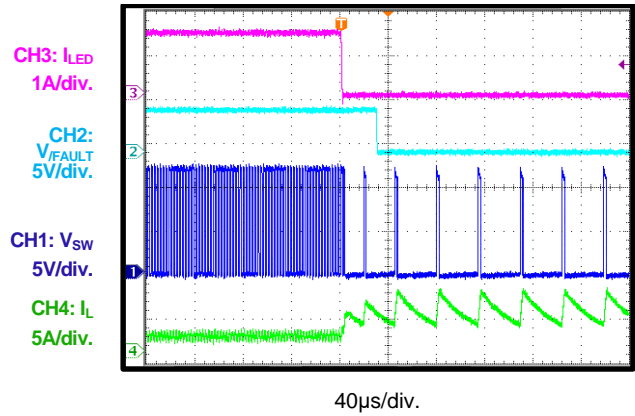
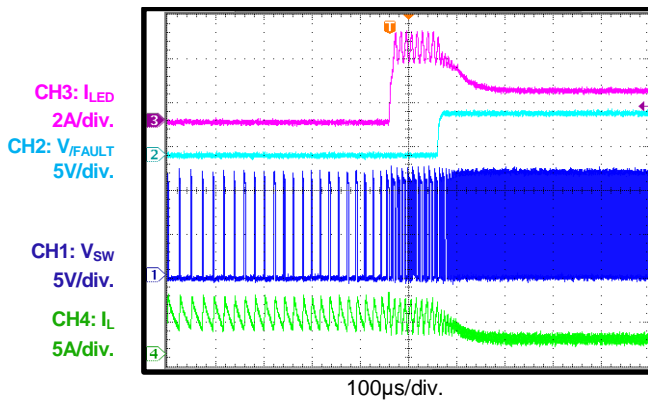
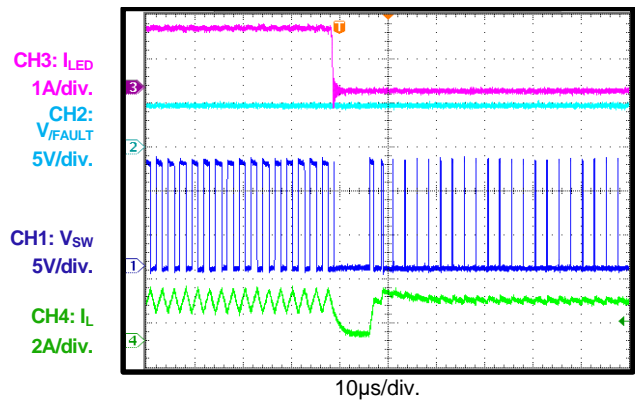
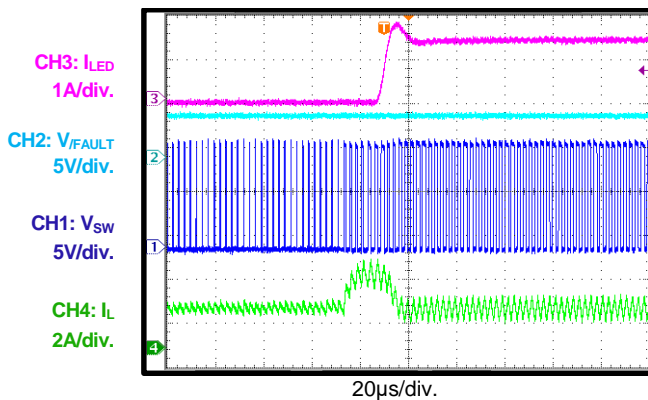
10ms/div.

**LED + Short to GND En On**


1ms/div.

**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

$V_{IN} = 12V$ ,  $V_{LED+} - V_{LED-} = 2 \times 3.2V$  @  $I_{LED} = 1.5A$ ,  $L = 10\mu H$ ,  $f_{sw} = 400kHz$ , with EMI filters,  $T_A = 25^\circ C$ , unless otherwise noted.

**LED + Short to GND En Off**

**LED + Short to GND Entry**
 $I_{LED} = 1.5A$ 

**LED + Short to GND Recovery**
 $I_{LED} = 1.5A$ 

**LED + Short to LED- Entry**
 $I_{LED} = 1.5A$ 

**LED + Short to LED- Recovery**
 $I_{LED} = 1.5A$ 


### FUNCTIONAL BLOCK DIAGRAM

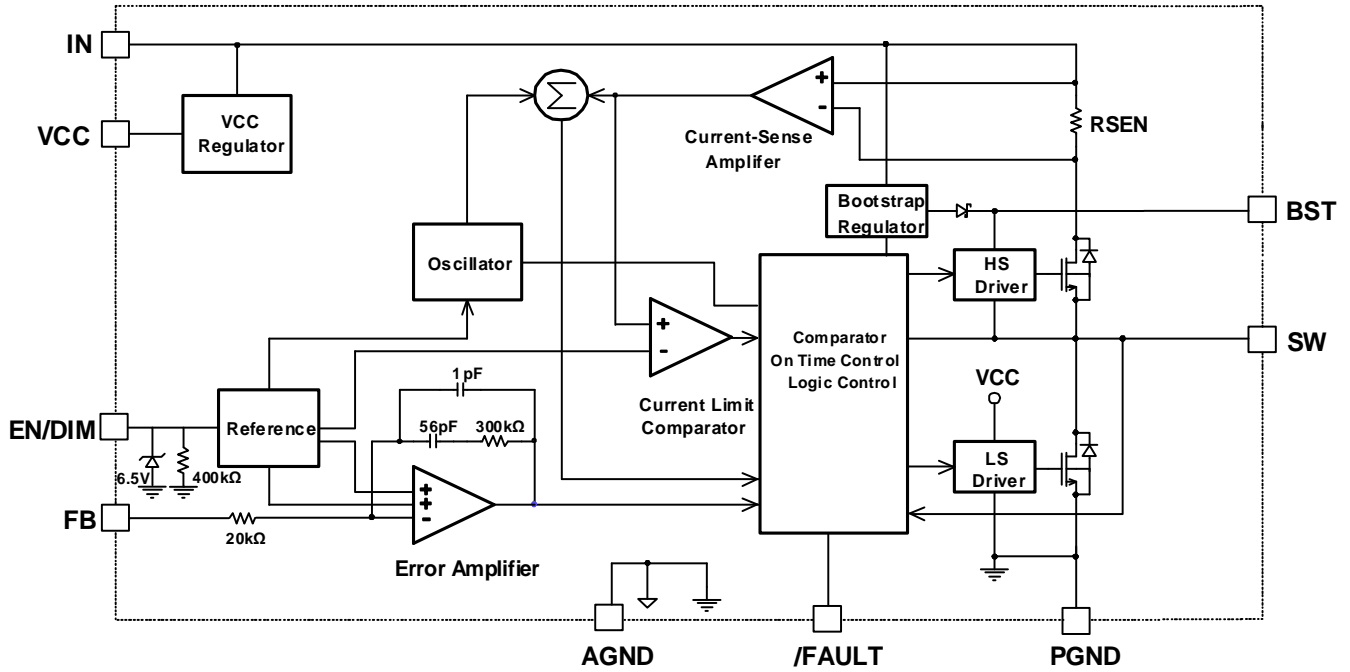


Figure 1: Functional Block Diagram

## OPERATION

The MPQ4425B is a high-frequency, synchronous, rectified, step-down, switch-mode white LED driver with built-in power MOSFETs. It offers a compact solution to achieve 1.5A of continuous output current with excellent load and line regulation over a 4V to 36V input supply range.

The device operates in a fixed-frequency, peak current control mode to regulate the output current. An internal clock initiates a PWM cycle. The integrated high-side power MOSFET turns on and remains on until its current reaches the value set by the COMP voltage ( $V_{COMP}$ ). When the power switch is off, it remains off until the next clock cycle starts. If the power MOSFET's current does not reach the value set by  $V_{COMP}$  within 95% of one PWM period, the power MOSFET turns off.

### Internal Regulator

The 4.9V internal regulator powers most of the internal circuitries. This regulator takes the  $V_{IN}$  input and operates in the full  $V_{IN}$  range. When  $V_{IN}$  exceeds 4.9V, the regulator's output is in full regulation. When  $V_{IN}$  falls below 4.9V, the output decreases following  $V_{IN}$ . A 0.1 $\mu$ F decoupling ceramic capacitor is required at the pin.

### CCM Operation

Continuous conduction mode (CCM) ensures that the part works with a fixed frequency from a no-load to a full-load range. An advantage of CCM is its controllable frequency and lower output ripple at light load.

### Frequency Foldback

Frequency foldback initiates during soft start and short-circuit protection.

### Error Amplifier (EA)

The error amplifier compares the FB pin voltage to the internal 0.2V reference ( $V_{REF}$ ), and outputs a current proportional to the difference between the two values. This output current charges or discharges the internal compensation network to form  $V_{COMP}$ , which controls the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

### Enable Control (EN)

EN/DIM is a control pin that turns the regulator on and off. Drive EN/DIM high to turn on the regulator; drive EN/DIM low to turn it off. An internal resistor from EN/DIM to GND allows EN/DIM to be floated and shut down the chip.

EN/DIM is clamped internally using a 6.5V series Zener diode (see Figure 2). Connecting the EN/DIM input through a pull-up resistor to the voltage on  $V_{IN}$  limits the EN input current below 100 $\mu$ A. For example, with 12V connected to  $V_{IN}$ ,  $R_{PULLUP} \geq (12V - 6.5V) \div 100\mu A = 55k\Omega$ .

Directly connecting EN/DIM to a voltage source without a pull-up resistor requires limiting the amplitude of the voltage source to  $\leq 6V$  to prevent damage to the Zener diode.

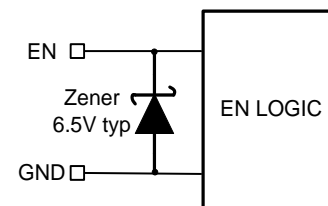


Figure 2: 6.5V Zener Diode Connection

If EN/DIM is driven low for longer than 25ms, the IC shuts down.

### PWM Dimming

Apply an external 100Hz to 2kHz PWM waveform to the EN/DIM pin for PWM dimming. The average LED current is proportional to the PWM duty. The minimum amplitude of the PWM signal is 1.8V. If a dimming signal is applied before the chip starts up, the dimming signal's on time must be longer than 2ms to ensure soft start finishes and the output current can be built. If a dimming signal is applied after soft start finishes, the 2ms time limit is not required.

### Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the output voltage of the internal regulator ( $V_{CC}$ ).



### Internal Soft Start (SS)

The soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage ( $V_{SS}$ ). When  $V_{SS}$  is below the internal reference ( $V_{REF}$ ),  $V_{SS}$  overrides  $V_{REF}$ , and the error amplifier uses  $V_{SS}$  as the reference. When  $V_{SS}$  exceeds  $V_{REF}$ , the error amplifier uses  $V_{REF}$  as the reference.

### Fault Indicator

The MPQ4425B has fault indication. The /FAULT pin is the open drain of a MOSFET. It should be connected to VCC or another voltage source through a resistor (e.g. 100k $\Omega$ ). The /FAULT pin is pulled high at normal operation, but during LED short circuit, open circuit, or thermal shutdown, it is pulled down to indicate a fault status.

### Over-Current Protection (OCP)

The device has cycle-by-cycle, peak current limit protection with valley-current detection. The inductor current is monitored during the high-side MOSFET (HS-FET) on state. If the inductor current exceeds the current limit value set by the COMP high-clamp voltage, the HS-FET turns off. The low-side MOSFET (LS-FET) turns on to discharge the energy, and the inductor current decreases.

Even though the internal clock pulses high, the HS-FET remains off unless the inductor valley current falls below a certain current threshold (the valley current limit). If the inductor current does not drop below the valley current limit when the internal clock pulses high, the HS-FET misses the clock, and the switching frequency decreases to half the nominal value. The peak and valley current limits keep the inductor current from running away during an overload or short-circuit condition.

### Thermal Shutdown (TSD)

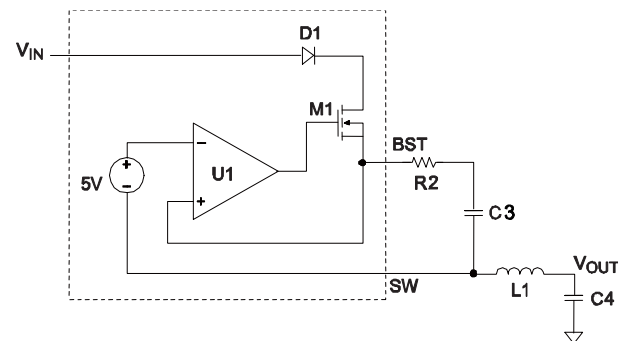
Thermal shutdown prevents the chip from operating at high temperatures. When the die temperature exceeds 170°C, the entire chip shuts down. When the temperature drops below its lower threshold (typically 140°C), the chip turns on.

### Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection, with a rising threshold of 2.2V and hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by  $V_{IN}$  through D1, M1, C3, L1, and C4 (see Figure 3).

If  $V_{IN} - V_{SW}$  exceeds 5V, U1 regulates M1 to maintain a 5V BST voltage across C4. As long as  $V_{IN}$  is sufficiently higher than SW, the bootstrap capacitor can be charged.

When the HS-FET is on,  $V_{IN} \approx V_{SW}$ , so the bootstrap capacitor cannot be charged. When the LS-FET is on,  $V_{IN} - V_{SW}$  reaches its maximum for fast charging. When there is no inductor current,  $V_{SW} = V_{OUT}$ , so the difference between  $V_{IN}$  and  $V_{OUT}$  can charge the bootstrap capacitor. It is recommended to place a 20 $\Omega$  resistor between the SW and BST capacitors to reduce SW spike voltage.



**Figure 3: Internal Bootstrap Charging Circuit**

### Start-Up and Shutdown

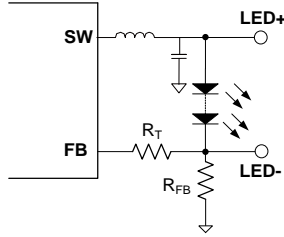
If  $V_{IN}$  and EN exceed their thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip:  $V_{IN}$  low, EN low, and thermal shutdown. During the shutdown procedure, the signaling path is first blocked to avoid any fault triggering.  $V_{COMP}$  and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

## APPLICATION INFORMATION

### Setting the Output Current

The output current is set by the external resistor  $R_{FB}$  (see Figure 4).



**Figure 4: Feedback Network**

When the feedback reference voltage is 0.2V,  $I_{LED}$  can be calculated with Equation (1):

$$I_{LED} = \frac{0.2V}{R_{FB}} \quad (1)$$

$R_T$  sets the loop bandwidth, and a lower  $R_T$  correlates with a higher bandwidth. However, a high bandwidth may lead to an insufficient phase margin, resulting in an unstable loop. An optimal  $R_T$  value is required to make a tradeoff between the bandwidth and phase margin. Table 1 lists the recommended feedback resistor and  $R_T$  values for common output with a 1 or 2 series LED.

**Table 1: Resistor Selection for Common Output**

$I_{LED}$ (A)	$R_{FB}$ (m $\Omega$ )	$R_T$ (k $\Omega$ )
0.5	400 (1%)	200
1	200 (1%)	150
1.5	133 (1%)	100

### Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and it requires a capacitor to supply the AC current to the converter to maintain the DC input voltage. For optimal performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are recommended due to their low ESR and small temperature coefficients.

For most applications, use a 4.7 $\mu$ F to 10 $\mu$ F capacitor. It is recommended to use another, lower-value capacitor (e.g. 0.1 $\mu$ F) with a small package size (0603) to absorb high-frequency switching noise. Place the secondary capacitor as close to the IN and GND pins as possible.

Since  $C_{IN}$  absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (2):

$$I_{CIN} = I_{LED} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (2)$$

The worst-case condition occurs at  $V_{IN} = 2V_{OUT}$ , calculated with Equation (3):

$$I_{CIN} = \frac{I_{LED}}{2} \quad (3)$$

Choose an input capacitor with an RMS current rating greater than half the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1 $\mu$ F) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (4):

$$\Delta V_{IN} = \frac{I_{LED}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (4)$$

### Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. Use low-ESR capacitors to maintain low output voltage ripple. The output voltage ripple can be estimated with Equation (5):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8f_{SW} \times C_{OUT}}\right) \quad (5)$$

Where L is the inductor value, and  $R_{ESR}$  is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency. The capacitance causes the majority of the output voltage ripple.

The output voltage ripple can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (7)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ4425B can be optimized for a wide range of capacitance and ESR values.

### Selecting the Inductor

For most applications, a 4.7µH to 22µH inductor with a DC current rating at least 25% higher than the maximum load current is recommended. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage. However, inductors with a larger value inductor also have a larger physical size, higher series resistance, and lower saturation current. To determine the inductor value, set the inductor ripple current to about 30% of the maximum load current. The inductance value can be then be calculated with Equation (8):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

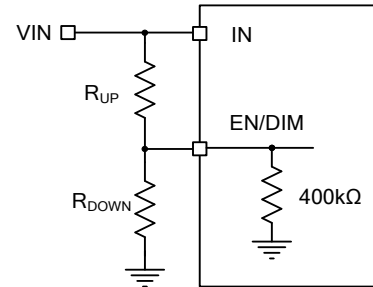
Where  $\Delta I_L$  is the peak-to-peak inductor ripple current.

Make the inductor ripple current about 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (9):

$$I_{LP} = I_{LED} + \frac{V_{OUT}}{2f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

### V<sub>IN</sub> UVLO Setting

The MPQ4425B has an internal, fixed under-voltage lockout (UVLO) threshold. The rising threshold is about 3.5V, while the falling threshold is about 3.1V. If the application requires a higher UVLO point, place an external resistor divider between the IN and EN/DIM pins to raise the equivalent UVLO threshold (see Figure 5).



**Figure 5: Adjustable UVLO using EN divider**

The UVLO threshold can be calculated with Equation (10) and Equation (11):

$$INUV_{RISING} = \left(1 + \frac{R_{UP}}{400k\Omega/R_{DOWN}}\right) \times V_{EN\_RISING} \quad (10)$$

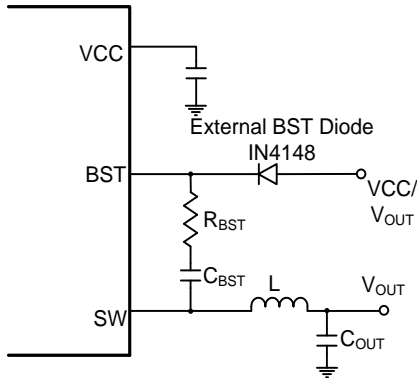
$$INUV_{FALLING} = \left(1 + \frac{R_{UP}}{400k\Omega/R_{DOWN}}\right) \times V_{EN\_FALLING} \quad (11)$$

Where  $V_{EN\_RISING} = 1.45V$ ,  $V_{EN\_FALLING} = 1V$ . When choosing  $R_{UP}$ , ensure it is high enough to limit the current flow into the EN/DIM pin to less than 100µA.

### BST Resistor and External BST Diode

A 20Ω resistor is recommended in series with the BST capacitor to reduce the SW spike voltage. Higher resistance improves SW spike reduction, but compromises efficiency.

An external BST diode enhances the regulator's efficiency when the duty cycle is high (>65%). A power supply (typically VCC or V<sub>OUT</sub>) between 2.5V and 5V can power the external bootstrap diode (see Figure 6).



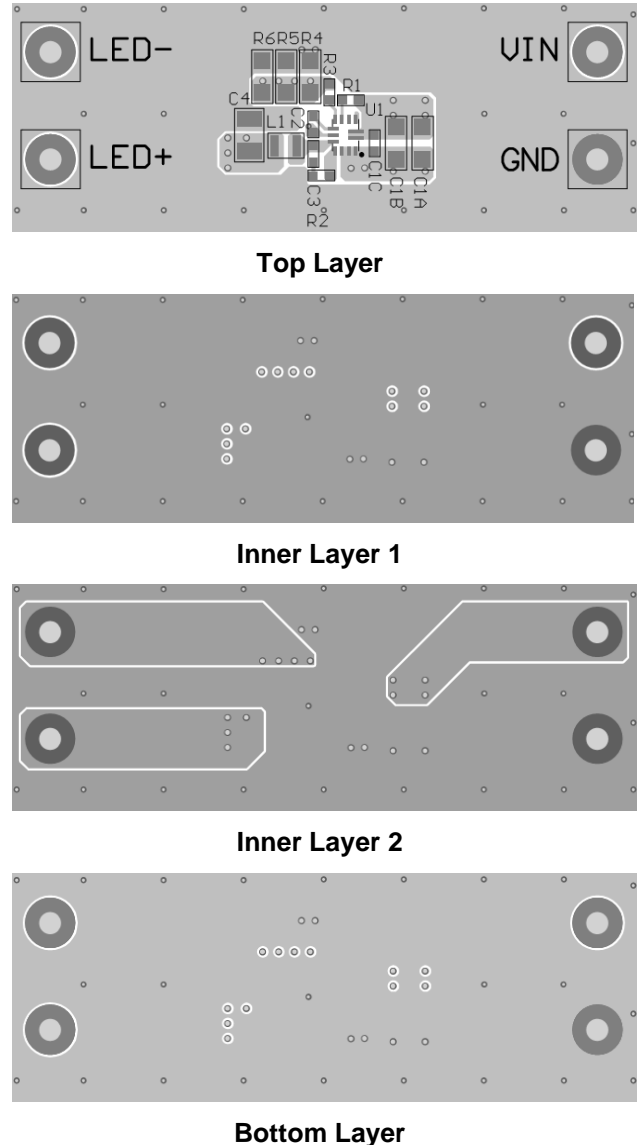
**Figure 6: Optional External Bootstrap Diode to Enhance Efficiency**

The recommended external BST diode is IN4148, and the recommended BST capacitor value is 0.1 $\mu$ F to 1 $\mu$ F.

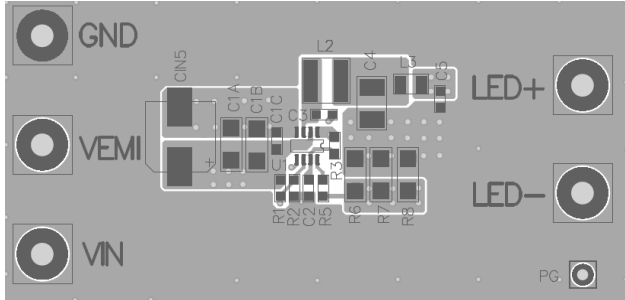
### PCB Layout Guidelines

Efficient PCB layout is critical for stable operation, especially for input capacitor placement. For better thermal performance, a 4-layer layout is recommended. For best results, refer to Figure 7 and Figure 8. and follow the guidelines below: <sup>(8)</sup> <sup>(9)</sup>

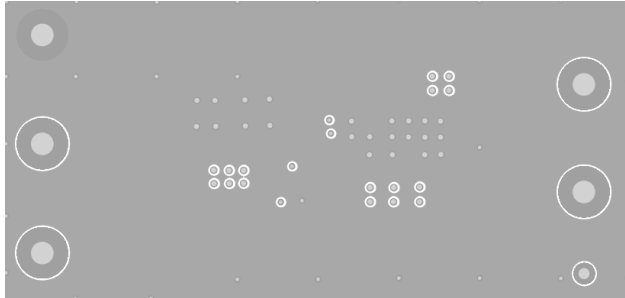
1. Connect directly to PGND using a large ground plane. If the bottom layer is a ground plane, add vias near PGND.
2. Ensure that the high-current paths at PGND and IN have short, direct, and wide traces.
3. Place the ceramic input capacitor, especially the small package (0603) input bypass capacitor, as close to the IN and PGND pins as possible to minimize high-frequency noise.
4. Keep the connection between the input capacitor and IN as short and wide as possible.
5. Place the VCC capacitor as close as possible to the VCC and GND pins.
6. Route SW and BST away from sensitive analog areas, such as FB.
7. Place the feedback resistors close to the chip to keep the trace connecting to the FB pin as short as possible.
8. Use multiple vias to connect the power planes to internal layers.



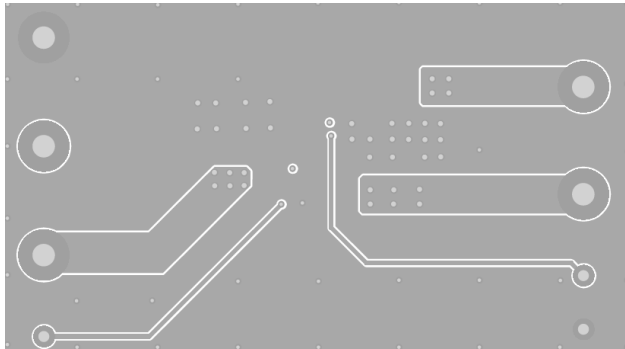
**Figure 7: Recommended PCB Layout for QFN Package <sup>(8)</sup>**



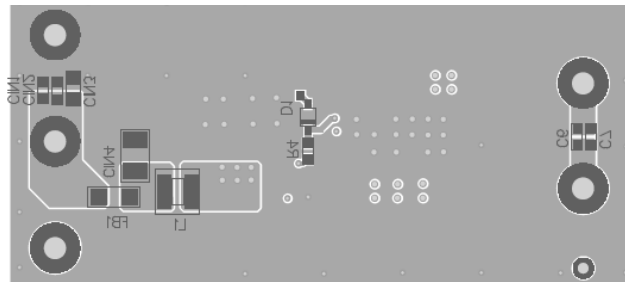
Top Layer



Inner Layer 1



Inner Layer 2



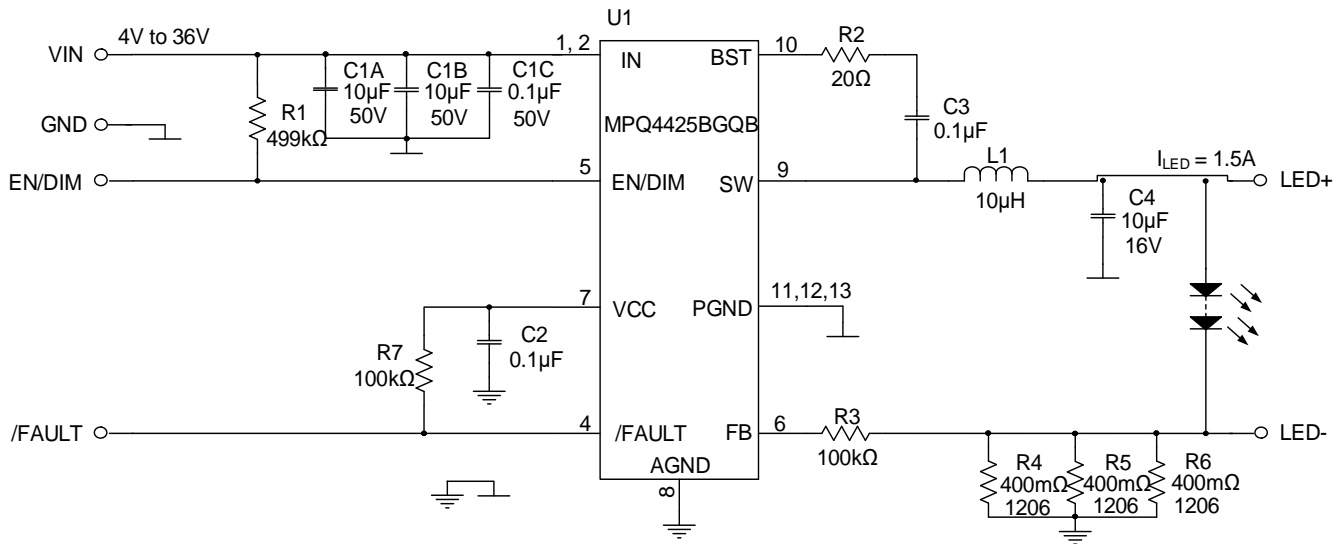
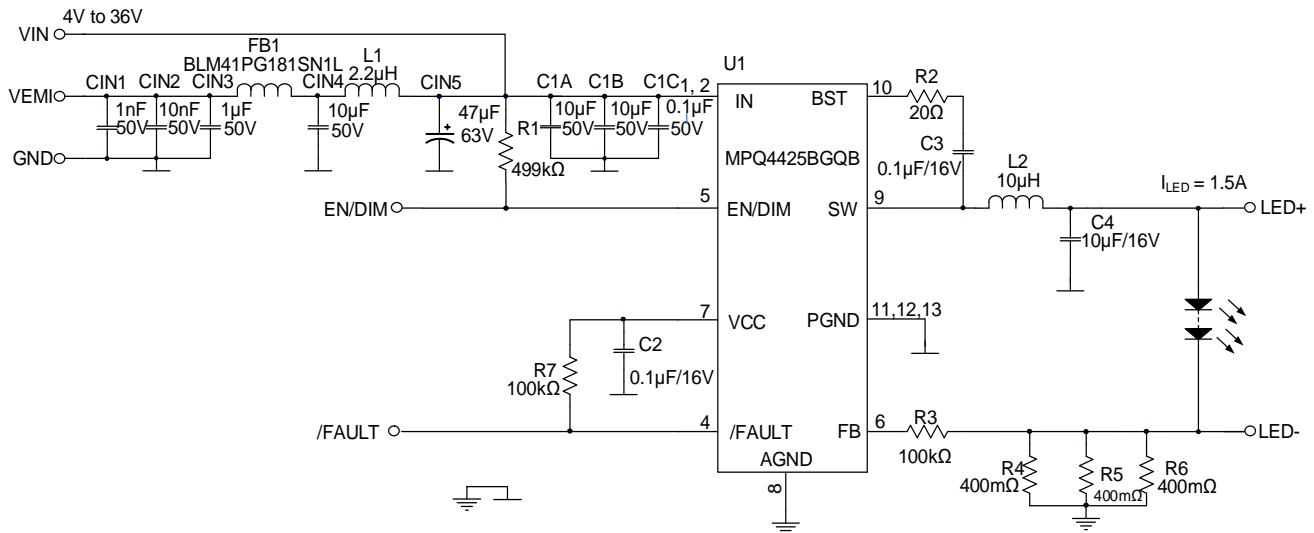
Bottom Layer

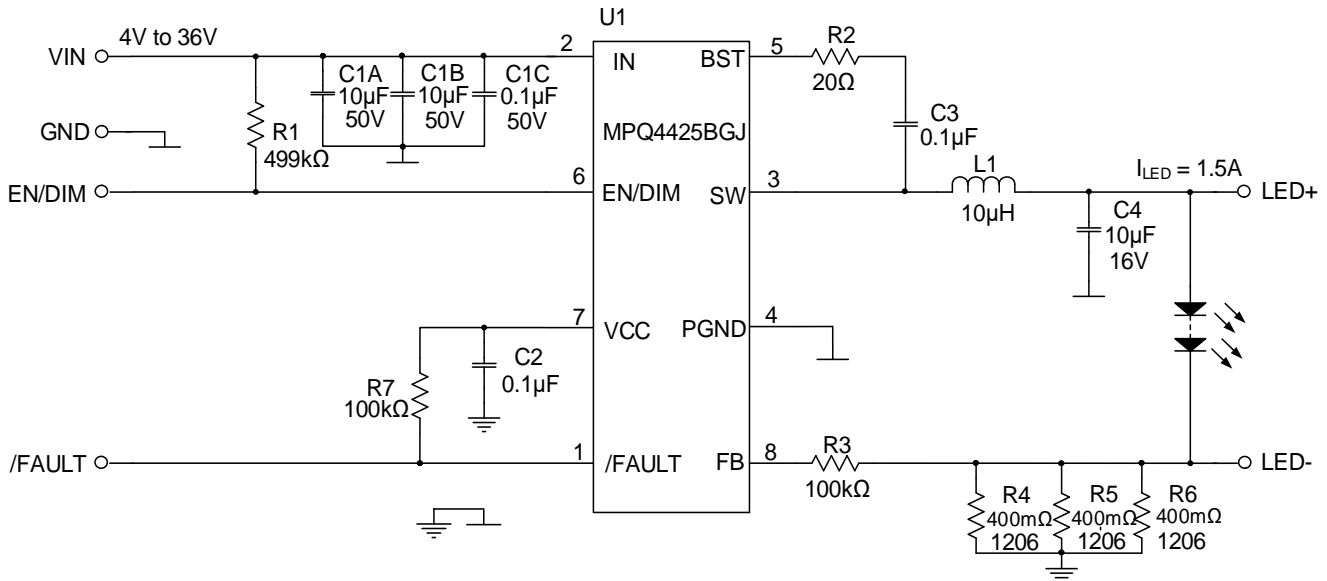
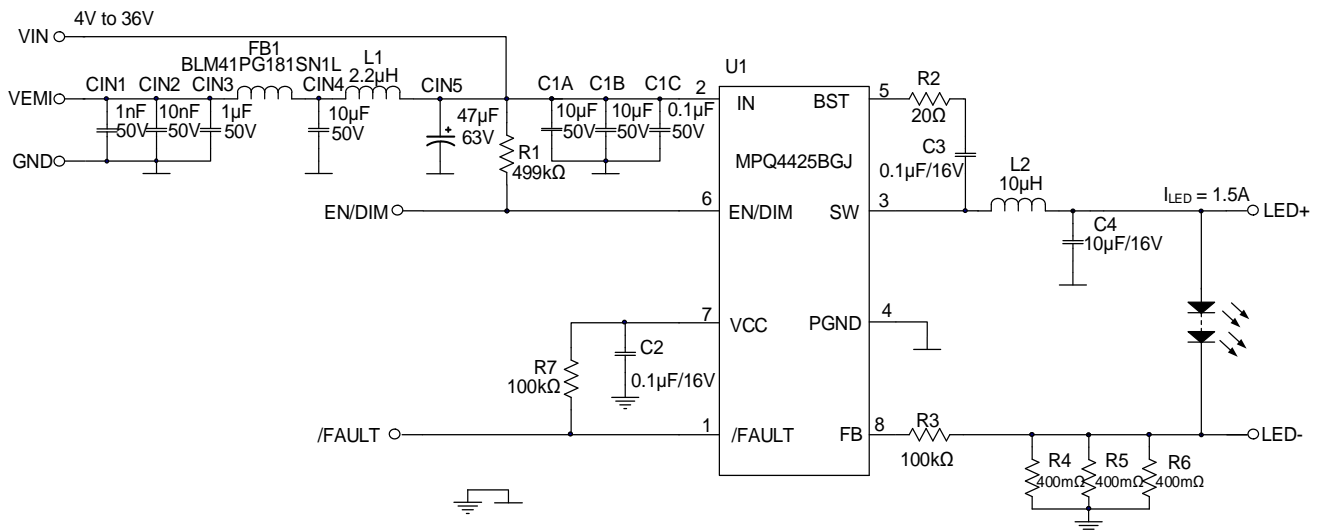
Figure 8: Recommended PCB Layout for TSOT23-8 Package <sup>(9)</sup>

Notes:

- 8) The recommended layout is based on Figure 9.
- 9) The recommended layout is based on Figure 12.

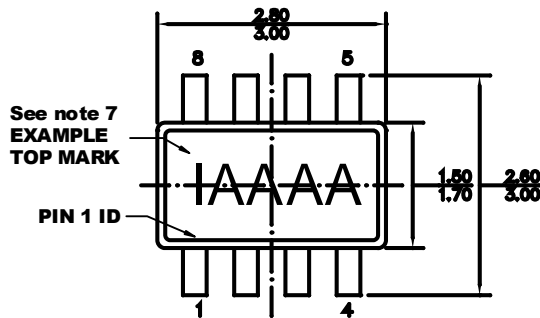
## TYPICAL APPLICATION CIRCUITS


 Figure 9:  $I_{LED} = 1.5A$  Application Circuit of QFN-13 Package

 Figure 10:  $I_{LED} = 1.5A$  Application Circuit of QFN-13 with EMI Filters

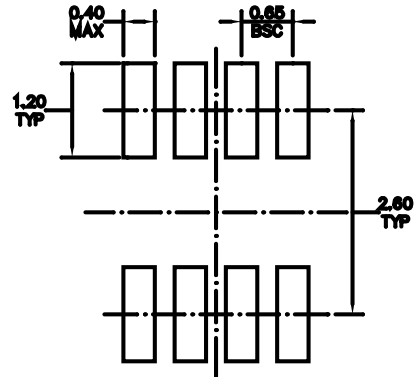
**TYPICAL APPLICATION CIRCUITS (continued)**

**Figure 11:  $I_{LED} = 1.5A$  Application Circuit with TSOT23-8 Package**

**Figure 12:  $I_{LED} = 1.5A$  Application Circuit of TSOT23-8 with EMI Filters**

## PACKAGE INFORMATION

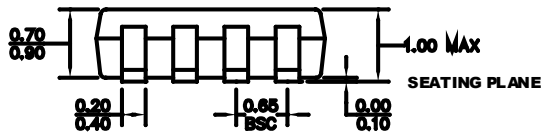
### TSOT23-8



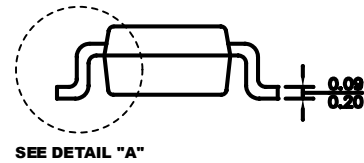
**TOP VIEW**



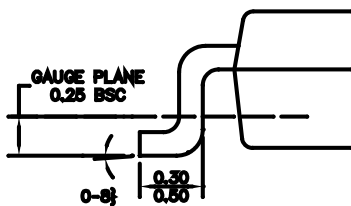
**RECOMMENDED LAND PATTERN**



**FRONT VIEW**



**SIDE VIEW**



**DETAIL "A"**

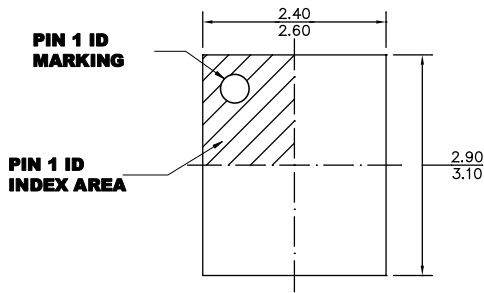
### NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHOULD BE 0.10 MILLIMETERS MAX.
- 5) JEDEC REFERENCE IS MO-193, VARIATION BA.
- 6) DRAWING IS NOT TO SCALE.
- 7) PIN 1 IS THE LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT (SEE EXAMPLE TOP MARK).

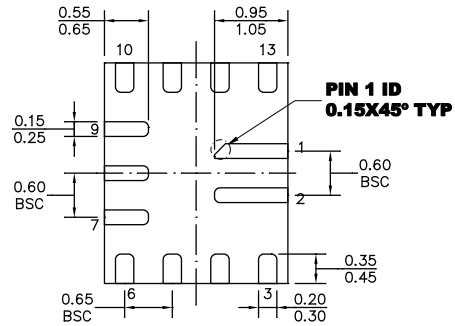


PACKAGE INFORMATION (continued)

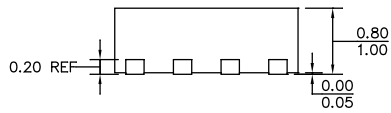
QFN-13 (2.5mmx3mm)



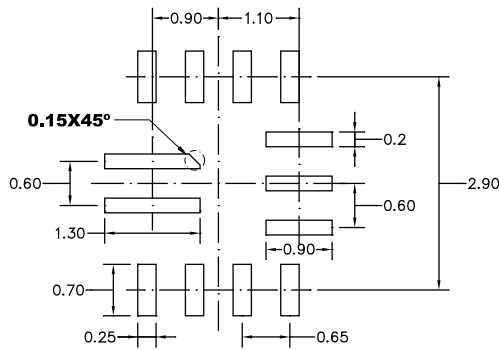
**TOP VIEW**



**BOTTOM VIEW**



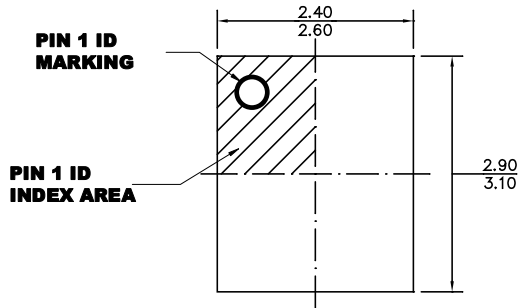
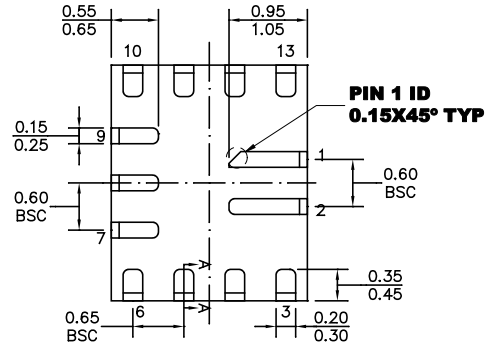
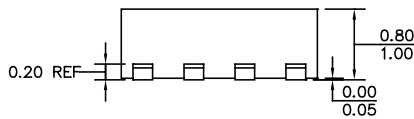
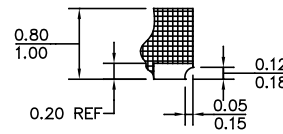
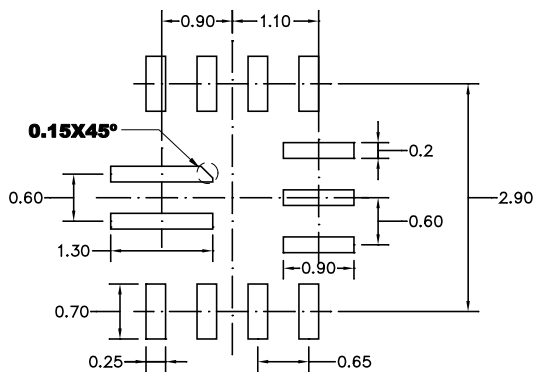
**SIDE VIEW**



**RECOMMENDED LAND PATTERN**

**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) LEAD COPLANARITY SHOULD BE 0.10 MILLIMETERS MAX.
- 3) JEDEC REFERENCE IS MO-220.
- 4) DRAWING IS NOT TO SCALE.

**PACKAGE INFORMATION (continued)**
**QFN-13 (2.5mmx3mm)**
**Wettable Flank**

**TOP VIEW**

**BOTTOM VIEW**

**SIDE VIEW**

**SECTION A-A**

**RECOMMENDED LAND PATTERN**
**NOTE:**

- 1) THE LEAD SIDE IS WETTABLE.
- 2) ALL DIMENSIONS ARE IN MILLIMETERS.
- 3) LEAD COPLANARITY SHOULD BE 0.08 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.