MPQ4436/4436A

45V, 6A, Low I_Q, Synchronous Step-Down Converter, AEC-Q100 Qualified

DESCRIPTION

The MPQ4436/4436A is a frequency programmable, synchronous, step-down switching regulator with integrated internal high-side and low-side power MOSFETs. It provides 6A (or less) of highly efficient output, with current mode control for fast loop response.

The wide 3.3V to 45V input range accommodates a variety of step-down applications in an automotive input environment. A 1.7µA shutdown mode quiescent current allows the part to be used in battery-powered applications.

High power conversion efficiency over a wide load range is achieved by scaling down the switching frequency in light-load conditions to reduce the switching and gate driving losses.

An open-drain power good signal indicates that the output is within 93% to 106% of its nominal voltage.

Frequency foldback helps prevent inductor current runaway during start-up. Thermal shutdown provides reliable, fault-tolerant operation.

High-duty cycle and low dropout mode are provided for the automotive cold crank condition.

The MPQ4436/4436A is available in a QFN-20 (4mmx4mm) package.

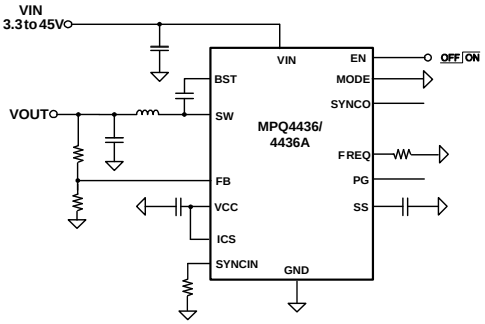
FEATURES

- Wide 3.3V to 45V Operating Voltage Range
- 6A Continuous Output Current
- 1.7µA Low Shutdown Supply Current
- 18µA Sleep Mode Quiescent Current
- Internal 48mΩ High-Side and 20mΩ Low-Side MOSFET
- 350kHz to 1000kHz Programmable Switching Frequency for Car Battery Applications
- Synchronize to External Clock
- Multi-Phase Capability
- Out-of-Phase Synchronized Clock Output
- Frequency Spread Spectrum (FSS) Option for Low EMI
  MPQ4436: Non-FSS version
  MPQ4436A: FSS version
- Symmetric V_{IN} for Low EMI
- Power Good Output
- External Soft Start
- 100ns Minimum On Time
- Selectable Advanced Asynchronous Mode (AAM) or Forced Continuous Conduction Mode (FCCM)
- Low Dropout Mode
- Hiccup Over-Current Protection
- Available in a QFN-20 (4mmx4mm) Package
- Available in a Wettable Flank Package
- Available in AEC-Q100 Grade-1

APPLICATIONS

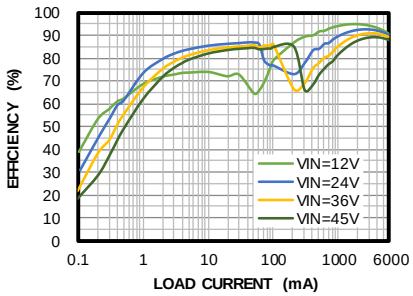
- Automotive Infotainment
- Automotive Clusters
- Advanced Driver Assistance Systems
- Industrial Power Systems

TYPICAL APPLICATION



Efficiency vs. Load Current

V_{OUT}=3.3V, F_{SW}=470kHz, L=3.3µH, AAM



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ4436GRE	QFN-20 (4mmx4mm)	*See Below*	1
MPQ4436GRE-AEC1	QFN-20 (4mmx4mm)	*See Below*	1
MPQ4436AGRE	QFN-20 (4mmx4mm)	*See Below*	1
MPQ4436AGRE-AEC1	QFN-20 (4mmx4mm)	*See Below*	1

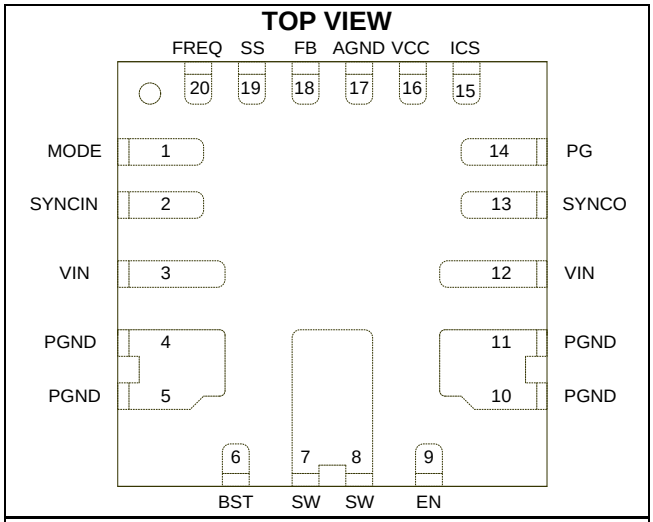
* For Tape & Reel, add suffix -Z (e.g. MPQ4436GRE-AEC1-Z).
**Moisture Sensitivity Level Rating

TOP MARKING

MPSYWW
MP4436
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
MP4436: Part number
LLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-20 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	MODE	**AAM or FCCM select pin.** Pull high to put the part in FCCM, and pull low for AAM at light load. Do not leave it floating.
2	SYNCIN	**SYNC input.** Connect a 51kΩ resistor between SYNCIN and GND. Apply a 350kHz to 1000kHz clock signal to this pin to synchronize the internal oscillator frequency to the external clock. This pin is also used for multi-phase operation. Connect this pin to GND if not used; do not float it.
3, 12	VIN	**Input supply.** VIN supplies power to all the internal control circuitry and the power switch connected to SW. It is recommended to place a decoupling capacitor to ground close to VIN to minimize switching spikes.
4, 5, 10, 11	PGND	**Power ground.**
6	BST	**Bootstrap.** BST is the positive power supply for the high-side MOSFET driver connected to SW. Connect a bypass capacitor between BST and SW. Check the application section to calculate the size of this capacitor.
7, 8	SW	**Switch node.** SW is the output of the internal power switch.
9	EN	**Enable.** Pull this pin below the specified threshold (0.85V) to shut down the chip. Pull it up above the specified threshold (1V) to enable the chip.
13	SYNCO	**SYNC output.** Output a clock signal 180° out-of-phase with the internal oscillator signal or opposite to the clock signal applied at SYNCIN pin. Leave floating if not used.
14	PG	**Power good indicator.** The output of PG is an open drain. A pull-up resistor to the power source is needed if PG is used. It goes high if the output voltage is within 93% to 106% of the nominal voltage; and goes low if the output voltage is above 107.5% or below 91% of the nominal voltage.
15	ICS	**Current sharing pin.** In a multi-phase application, connect the ICS pin of the ICs in parallel to improve the current sharing between different phases. Do not float this pin; connect it to VCC pin or VOUT that is at least 3V in a single-phase application.
16	VCC	**Bias supply.** This supplies power to the internal control circuit and gate drivers. A decoupling capacitor to ground is required close to this pin. Check the application section to calculate the size of this capacitor.
17	AGND	**Analog ground.**
18	FB	**Feedback input.** Connect FB to the center point of the external resistor divider from the output to AGND to set the output voltage. The feedback threshold voltage is 0.815V. Place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces.
19	SS	**Soft start input.** Place a capacitor from SS to GND to set the soft-start period. The MPQ4436/4436A sources 6μA from SS to the soft-start capacitor at start-up. As the SS voltage rises, the feedback threshold voltage increases to limit inrush current during start-up.
20	FREQ	**Switching frequency program.** Connect a resistor from this pin to ground to set the switching frequency. Follow the f_{SW} vs. R_{FREQ} curve in the Typical Performance Characteristics (TPC) section on page 14 to set the frequency.

ABSOLUTE MAXIMUM RATINGS (1)

VIN, EN ..... -0.3V to +50V
SW .....-0.3V to $V_{IN\ (MAX)}$ + 0.3V
BST ..... V_{SW} + 6V
All other pins..... -0.3V to +6V
Continuous power dissipation (T_A = 25°C) (2)
QFN-20 (4mmx4mm).....2.84W
Operating junction temperature.....+150°C
Lead temperature .....+260°C
Storage temperature..... -65°C to +150°C

ESD Rating

Human-body model (HBM) ..... ±2kV
Charged-device model (CDM) ..... ±750V

Recommended Operating Conditions

Supply voltage (V_{IN}) ..... 3.3V to 45V
Operating junction temp (T_J) .... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-20 (4mmx4mm)
JESD51-7 (3).....44.....9....°C/W
EVQ4436-R-00A(4).....23.....2.5..°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7, 4-layer PCB.
4) Measured on EVQ4436-R-00A, 9cmx9cm, 4-Layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VIN UVLO rising threshold	IN_{UVLO_RISING}		2.8	3.0	3.2	V
VIN UVLO falling threshold	$IN_{UVLO\_FALLING}$		2.45	2.65	2.85	V
VIN UVLO hysteresis	IN_{UVLO_HYS}			250		mV
VCC voltage	V_{CC}	I_{VCC} = 0A	4.6	4.9	5.2	V
VCC regulation		I_{VCC} = 30mA		1	4	%
VCC current limit	I_{LIMIT_VCC}	V_{CC} = 4V	100			mA
VIN quiescent current	I_Q	FB = 0.85V, no load, (sleep mode)		18	26	µA
VIN quiescent current (switching) (5)	I_{Q_ACTIVE}	MODE = GND (AAM), switching, no load, R_{FB_Up} = 1MΩ, R_{FB_Down} = 316kΩ		20		µA
		MODE = high (FCCM), switching, f_{SW} = 2MHz, no load		40		mA
		MODE = high (FCCM), switching, f_{SW} = 470kHz, no load		9.5		mA
VIN shutdown current	I_{SHDN}	EN = 0V		1.7	2.5	µA
FB voltage	V_{FB}	VIN = 3.3V to 45V, T_J = 25°C	0.807	0.815	0.823	V
		VIN = 3.3V to 45V	0.799	0.815	0.831	V
FB current	I_{FB}	V_{FB} = 0.85V	-50	0	50	nA
Switching frequency	f_{SW}	R_{FREQ} = 62kΩ	420	470	520	kHz
Minimum on time (5)	t_{ON_MIN}			100		ns
Minimum off time (5)	t_{OFF_MIN}			80		ns
SYNCIN voltage rising threshold	V_{SYNC_RISING}		1.8			V
SYNCIN voltage falling threshold	$V_{SYNC\_FALLING}$				0.4	V
SYNCIN clock range	f_{SYNC}	External clock	350		1000	kHz
SYNCO high voltage	V_{SYNCO_HIGH}	I_{SYNCO} = -1mA	3.3	4.5		V
SYNCO low voltage	V_{SYNCO_LOW}	I_{SYNCO} = 1mA			0.4	V
SYNCO phase shift		Tested on SYNCIN		180		Deg
HS current limit	I_{LIMIT}	Duty cycle = 30%	10	13	16	A
LS valley current limit	I_{LIMIT_VALLEY}		8	10	12	A
ZCD current	I_{ZCD}	AAM	-0.15	0.1	0.35	A
LS reverse current limit	$I_{LIMIT\_REVERSE}$	FCCM	2	4.5	6.5	A

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Switch leakage current	I_{SW_LKG}			0.01	1	µA
HS switch on resistance	R_{ON_HS}	V_{BST} - V_{SW} = 5V		48	80	mΩ
LS switch on resistance	R_{ON_LS}	V_{CC} = 5V		20	40	mΩ
Soft-start current	I_{SS}	V_{SS} = 0V	4	6	8	µA
EN rising threshold	V_{EN_RISING}		0.8	1	1.2	V
EN falling threshold	$V_{EN\_FALLING}$		0.65	0.85	1.05	V
EN hysteresis voltage	V_{EN_HYS}			180		mV
MODE rising threshold	V_{MODE_RISING}		1.8			V
MODE falling threshold	$V_{MODE\_FALLING}$				0.4	V
PG rising threshold (V_{FB} / V_{REF})	PG_{RISING}	V_{FB} rising	88.5%	93%	97.5%	V_{REF}
		V_{FB} falling	101.5%	106%	110.5%	
PG falling threshold (V_{FB} / V_{REF})	$PG_{FALLING}$	V_{FB} falling	86.5%	91%	95.5%	
		V_{FB} rising	103%	107.5%	112%	
PG output voltage low	V_{PG_LOW}	I_{SINK} = 1mA		0.1	0.3	V
PG rising delay	$t_{PG\_R\_DELAY}$			30		µs
PG falling delay	$t_{PG\_F\_DELAY}$			30		µs
Thermal shutdown (5)	t_{SD}			170		°C
Thermal shutdown hysteresis (5)	t_{SD_HYS}			20		°C

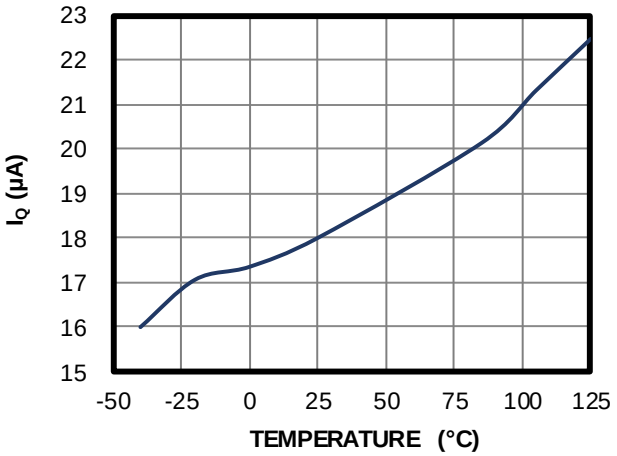
Note:

5) Derived from bench characterization, not tested in production.

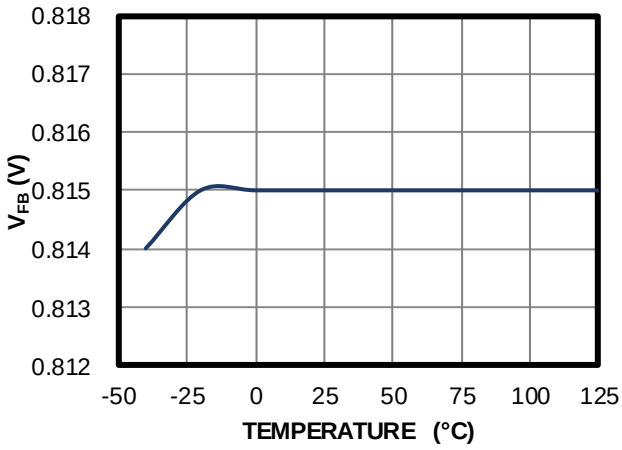
TYPICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

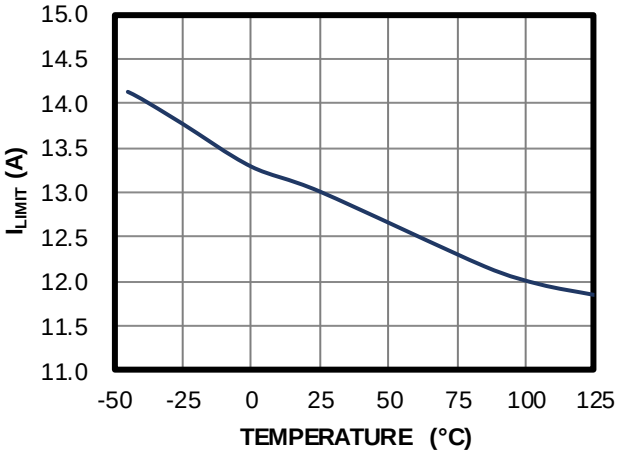
I_Q vs. Temperature



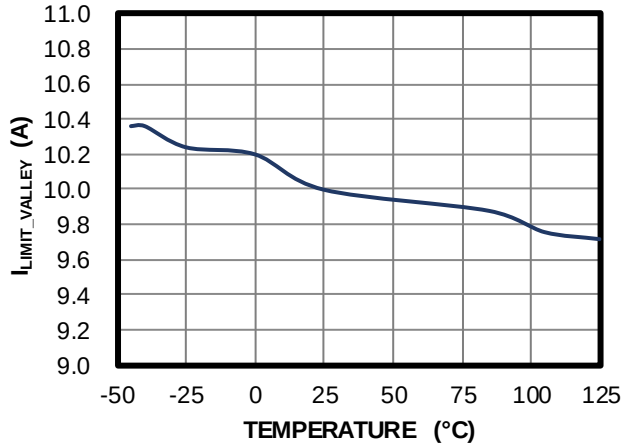
V_{FB} vs. Temperature



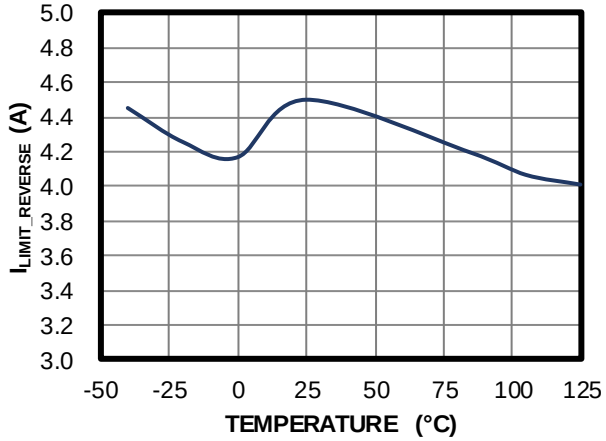
I_{LIMIT} vs. Temperature



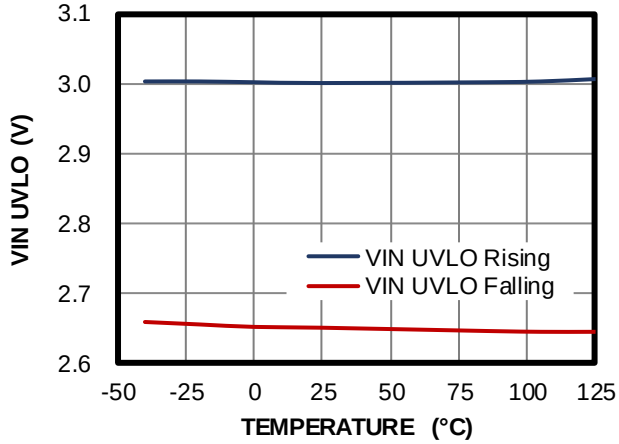
Valley Current Limit vs. Temperature



Reverse Current Limit vs. Temperature



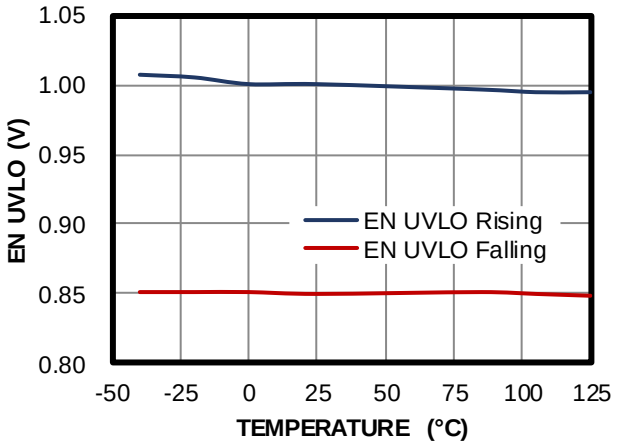
VIN UVLO Threshold vs. Temperature



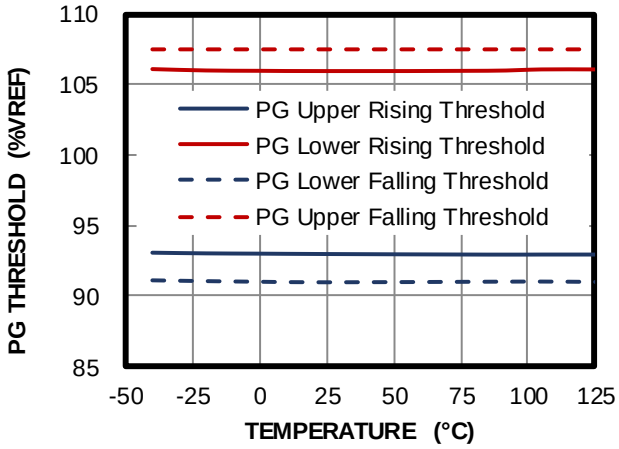
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

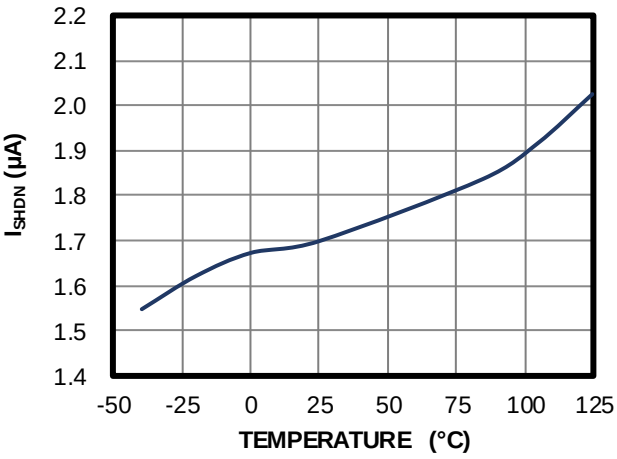
EN UVLO Threshold vs. Temperature



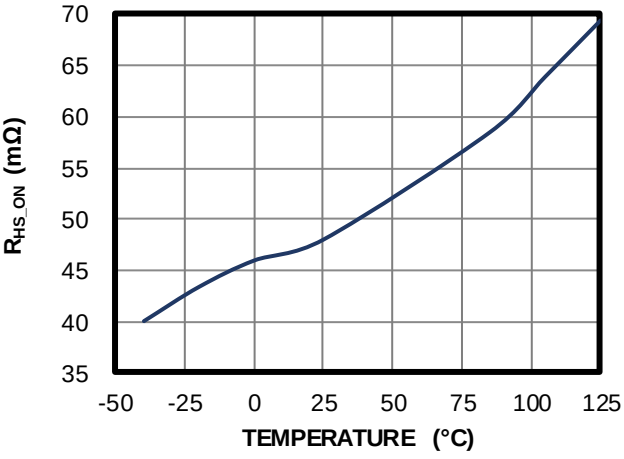
PG Rising/Falling Threshold vs. Temperature



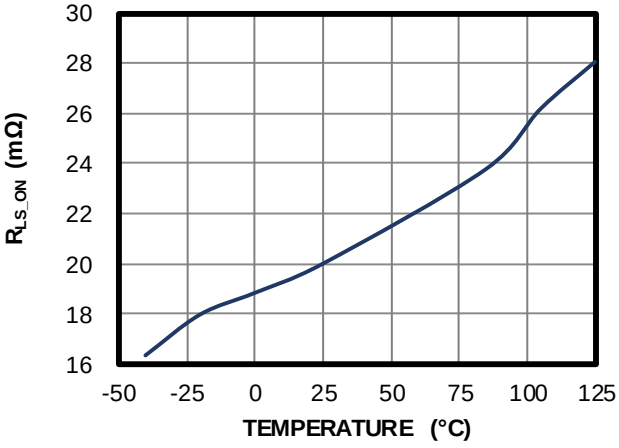
V_{IN} Shutdown Current vs. Temperature



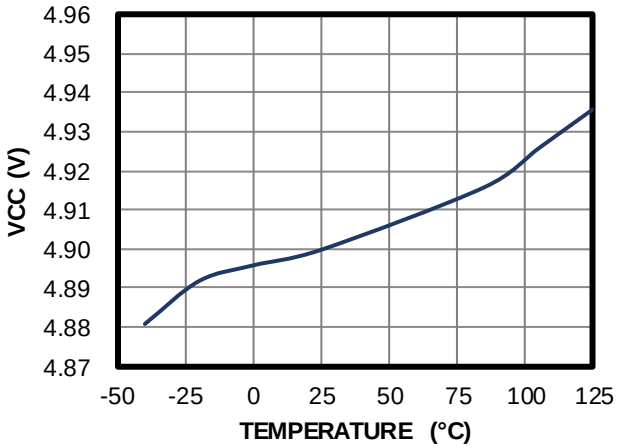
R_{HS_ON} vs. Temperature



R_{LS_ON} vs. Temperature



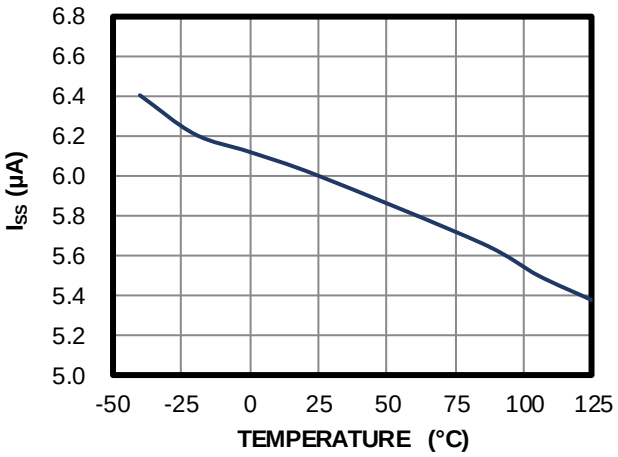
VCC vs. Temperature



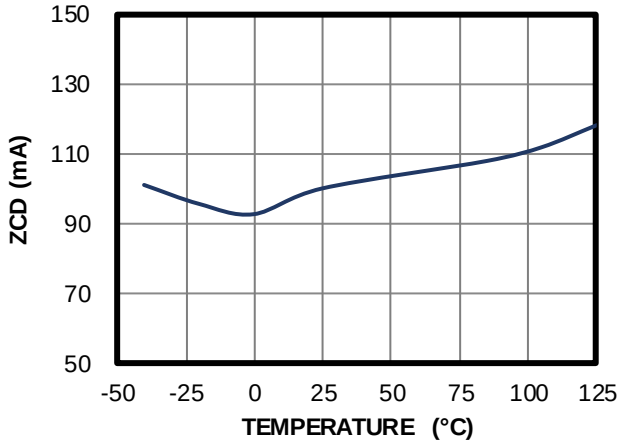
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Soft-Start Current vs. Temperature

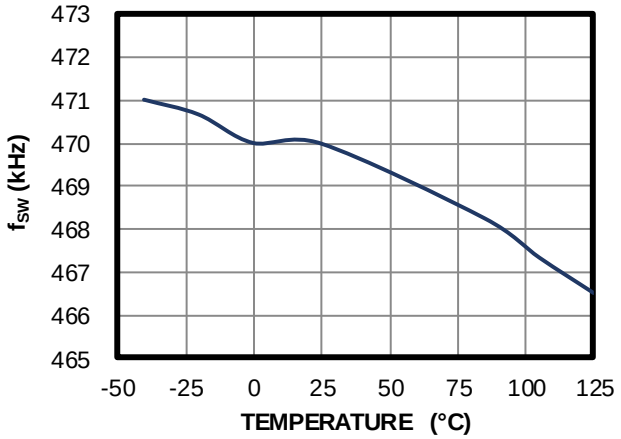


ZCD vs. Temperature



f_{SW} vs. Temperature

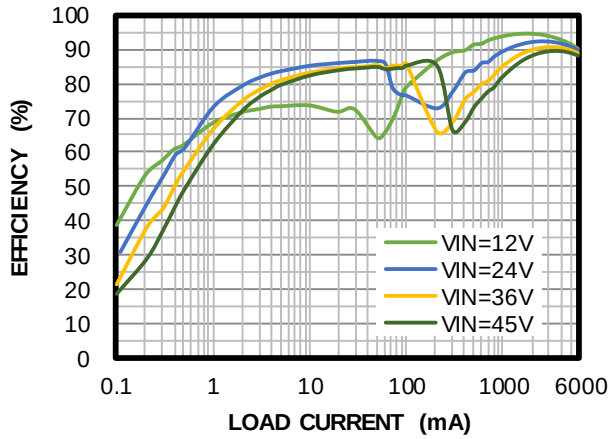
R_{FREQ} = 62kΩ



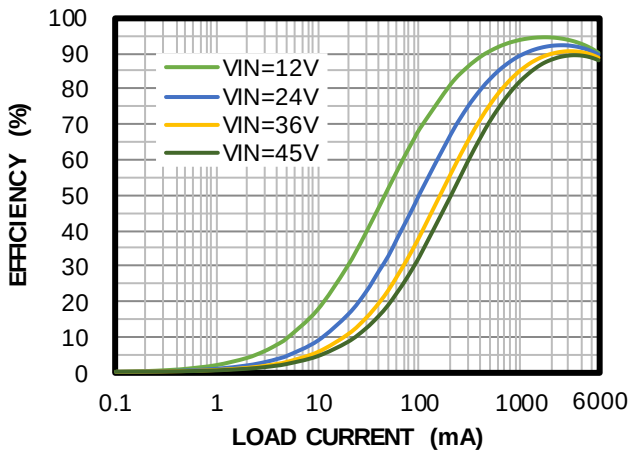
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

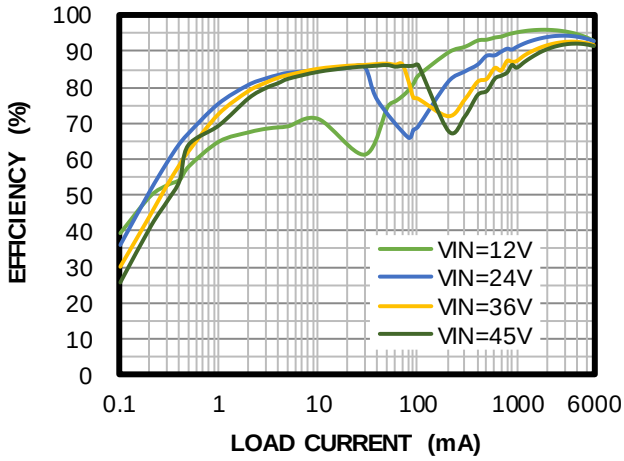
Efficiency vs. Load Current
AAM, L=3.3µH



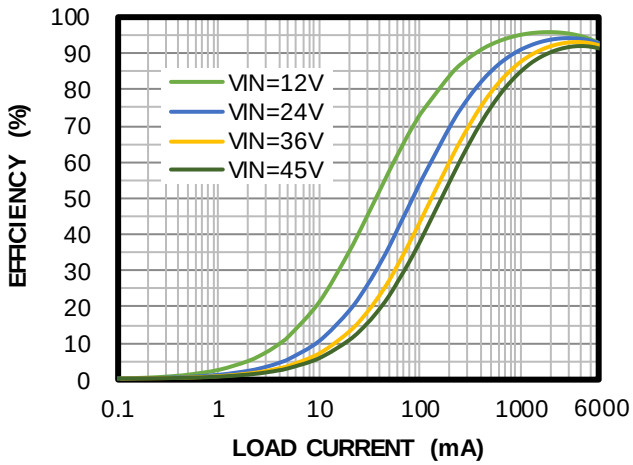
Efficiency vs. Load Current
FCCM, L=3.3µH



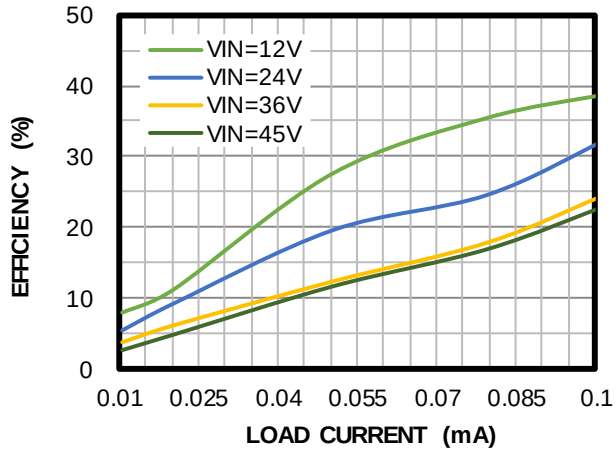
Efficiency vs. Load Current
AAM, V_{OUT} = 5V, L=3.3µH



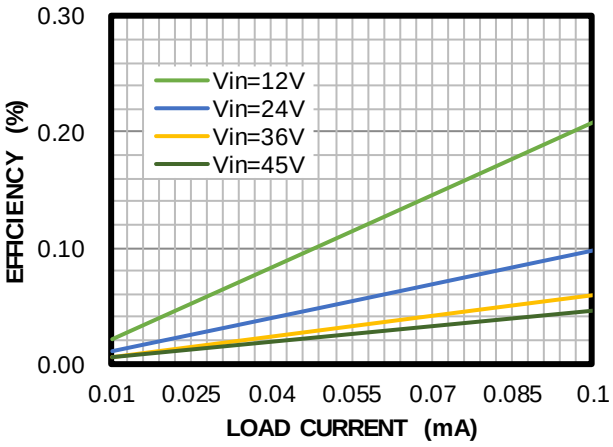
Efficiency vs. Load Current
FCCM, V_{OUT} = 5V, L=3.3µH



Efficiency vs. Load Current
(Extreme light load) AAM, L=3.3µH



Efficiency vs. Load Current
(Extreme light load) FCCM, L=3.3µH

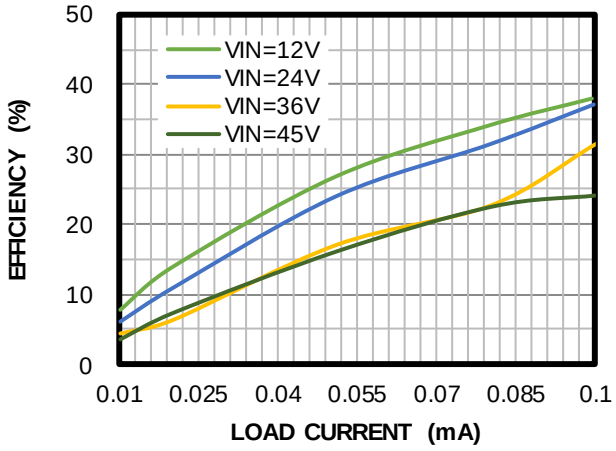


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

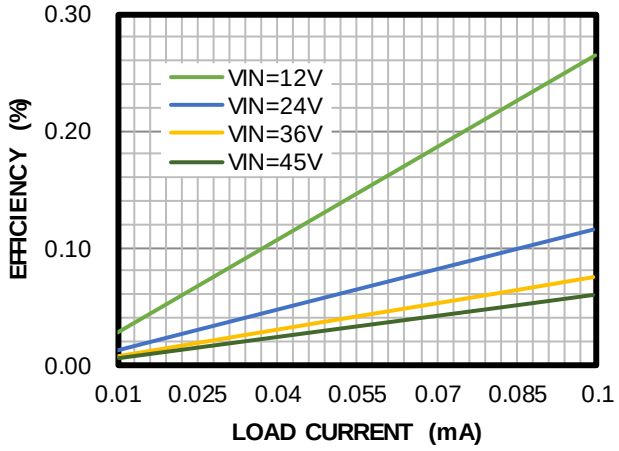
Efficiency vs. Load Current

(Extreme light load) AAM, V_{OUT} = 5V, L=3.3µH



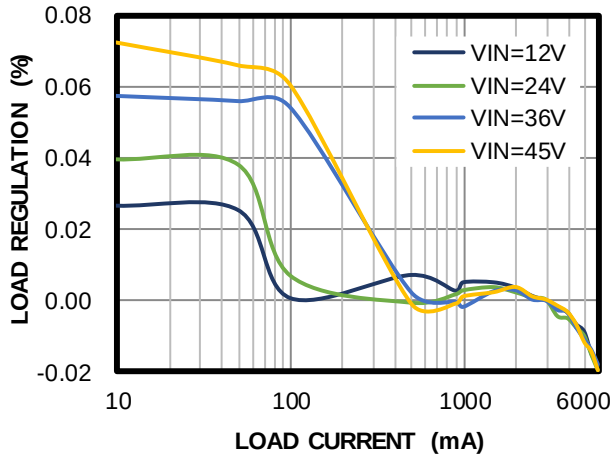
Efficiency vs. Load Current

(Extreme light load) FCCM, V_{OUT} = 5V, L=3.3µH



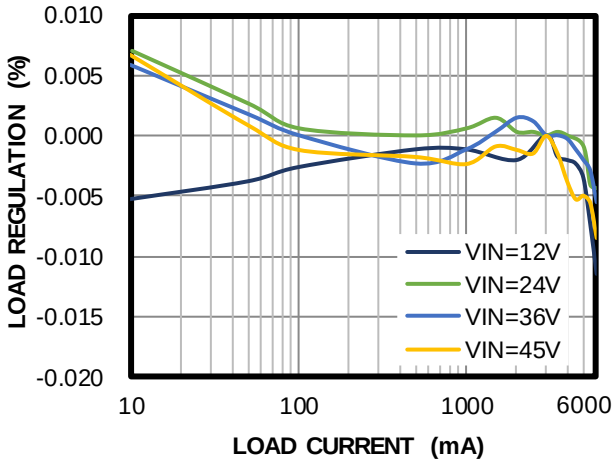
Load Regulation

AAM



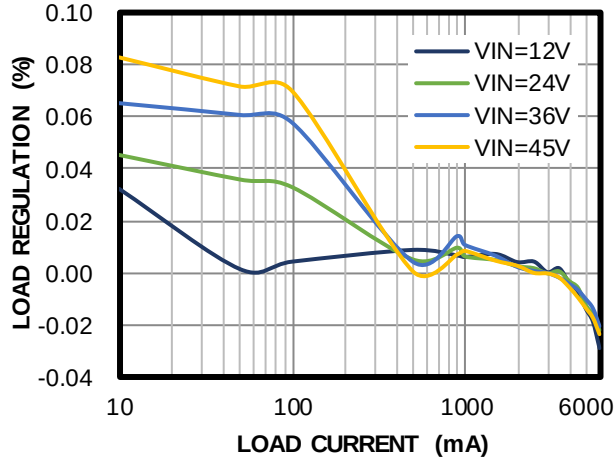
Load Regulation

FCCM



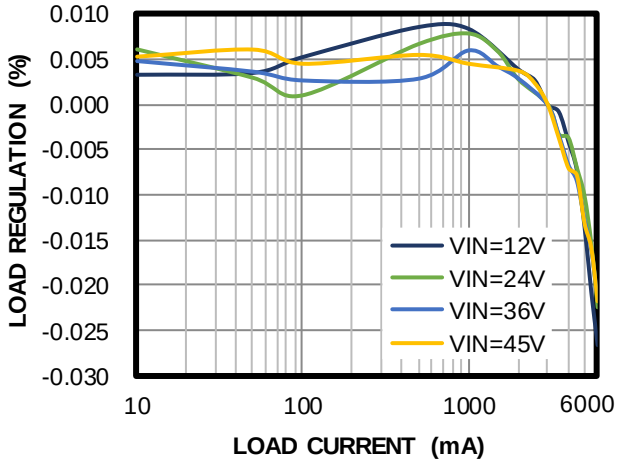
Load Regulation

AAM, V_{OUT} = 5V



Load Regulation

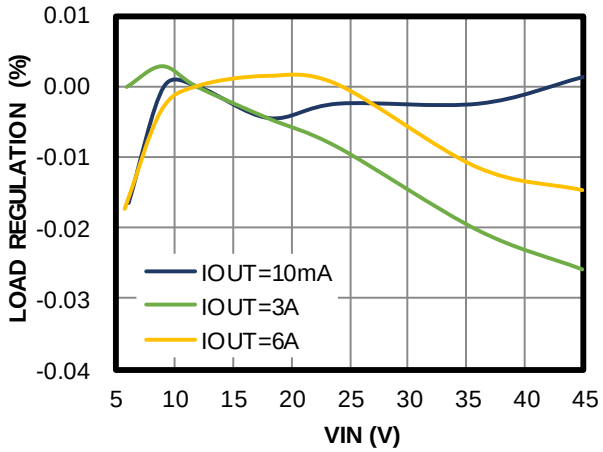
FCCM, V_{OUT} = 5V



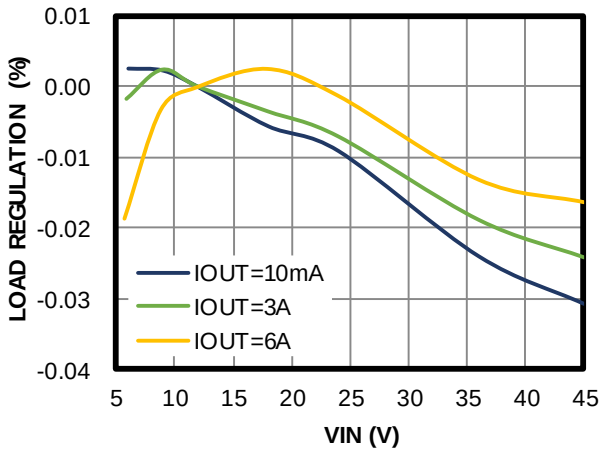
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

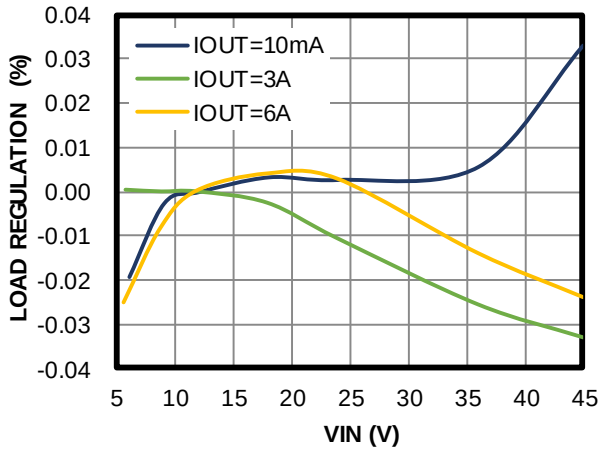
Line Regulation
AAM



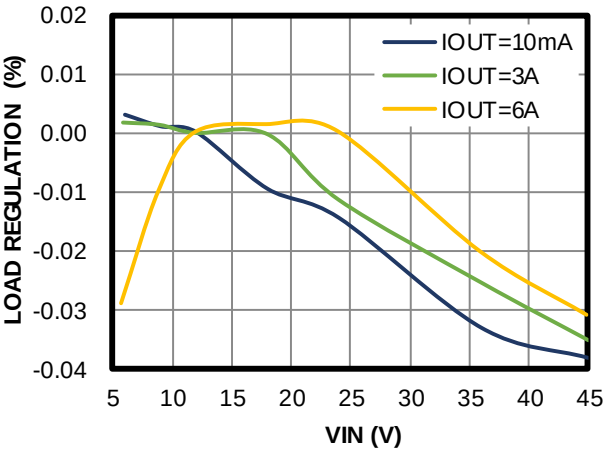
Line Regulation
FCCM



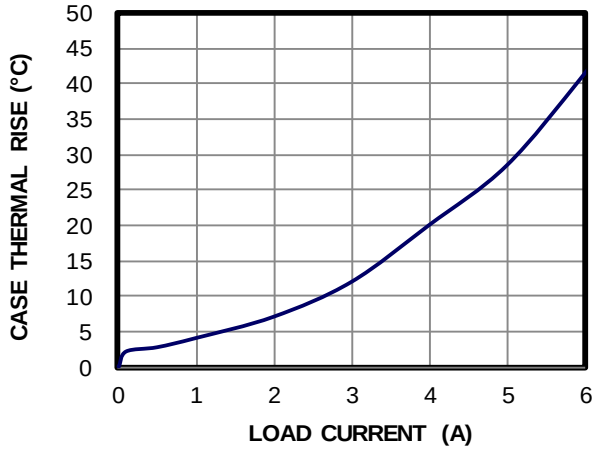
Line Regulation
AAM, V_{OUT} = 5V



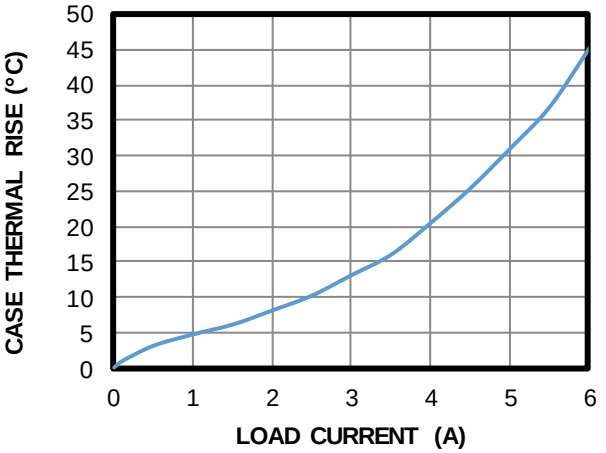
Line Regulation
FCCM, V_{OUT} = 5V



Case Thermal Rise
V_{OUT} = 3.3V



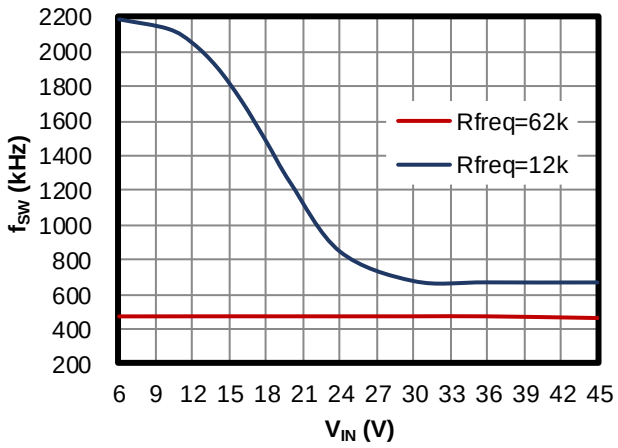
Case Thermal Rise
V_{OUT} = 5V



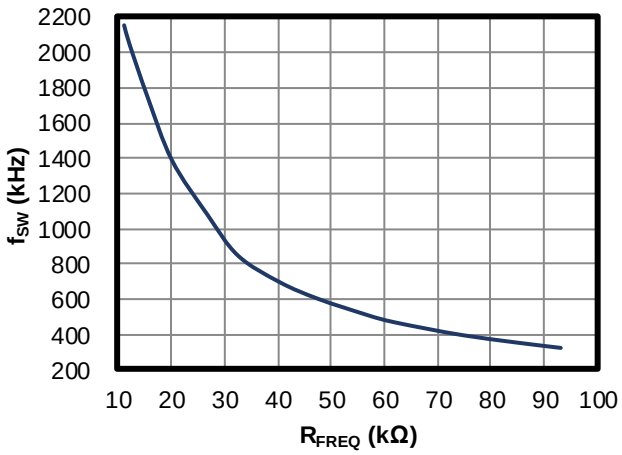
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

f_{SW} vs. V_{IN}

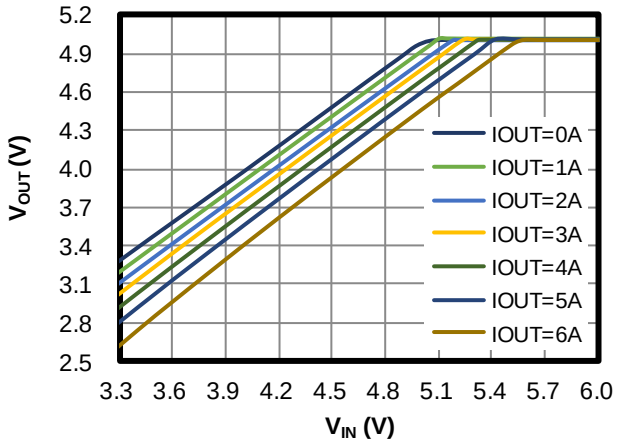


f_{SW} vs. R_{FREQ}



Low Dropout

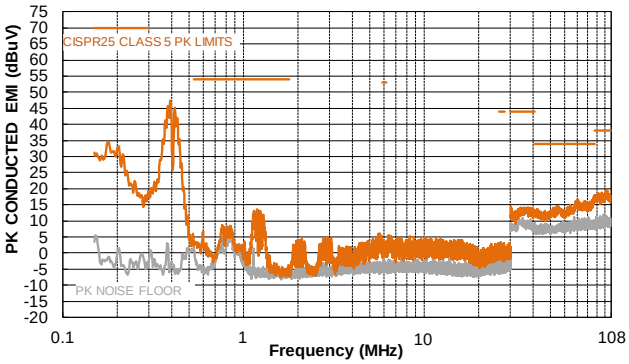
V_{OUT} = 5V



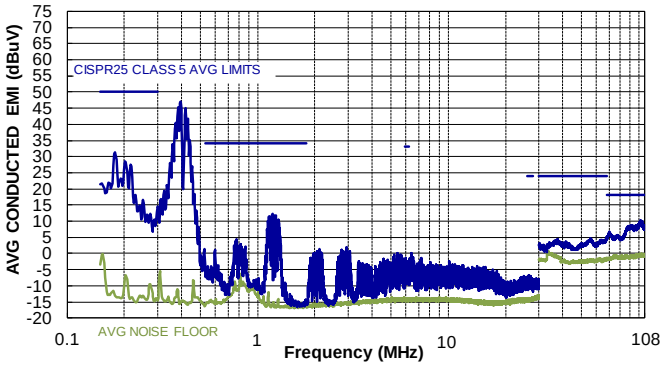
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 6A, L = 4.7µH, f_{SW} = 410kHz, T_A = 25°C, with FSS (MPQ4436A only), unless otherwise note. (6)

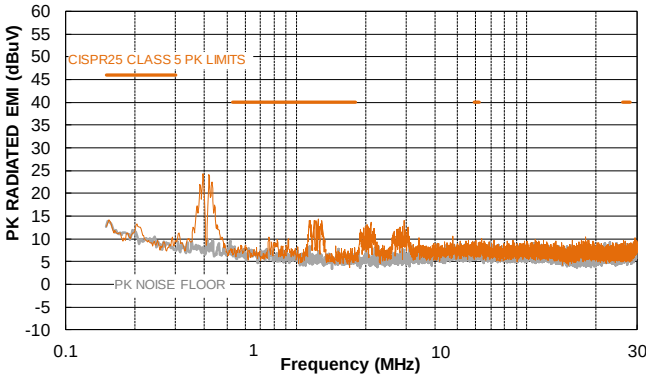
CISPR25 Class 5 Peak Conducted Emissions
150kHz to 108MHz



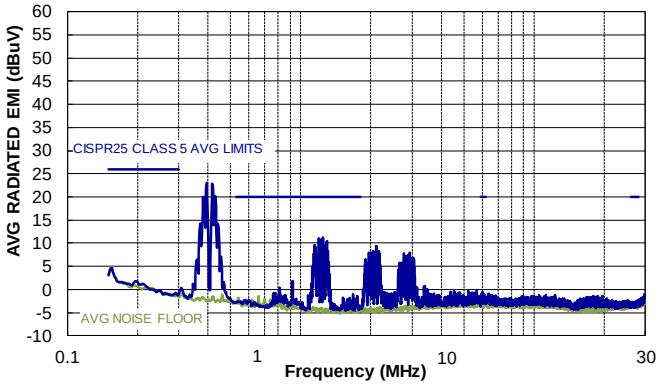
CISPR25 Class 5 Average Conducted Emissions
150kHz to 108MHz



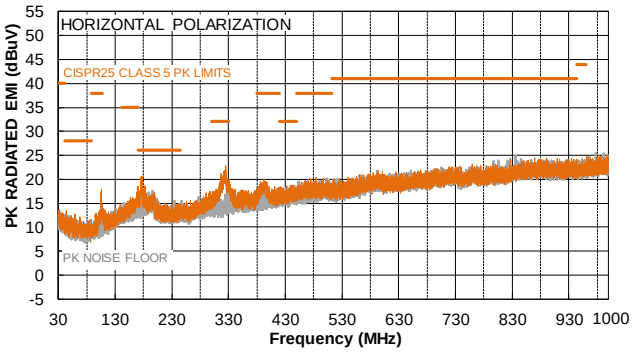
CISPR25 Class 5 Peak Radiated Emissions
150kHz to 30MHz



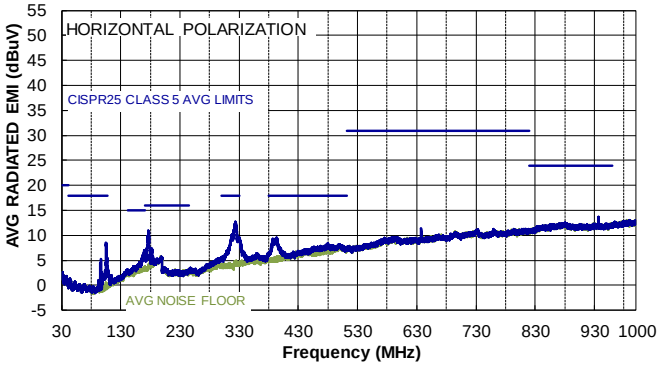
CISPR25 Class 5 Average Radiated Emissions
150kHz to 30MHz



CISPR25 Class 5 Peak Radiated Horizontal
30MHz to 1GHz



CISPR25 Class 5 Average Radiated Horizontal
30MHz to 1GHz

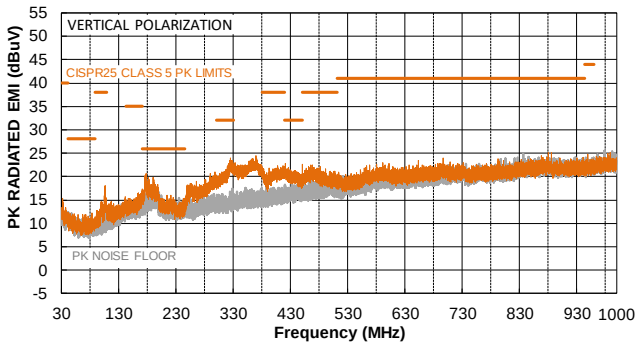


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 6A, L = 4.7µH, f_{SW} = 410kHz, T_A = 25°C, with FSS (MPQ4436A only), unless otherwise noted. (6)

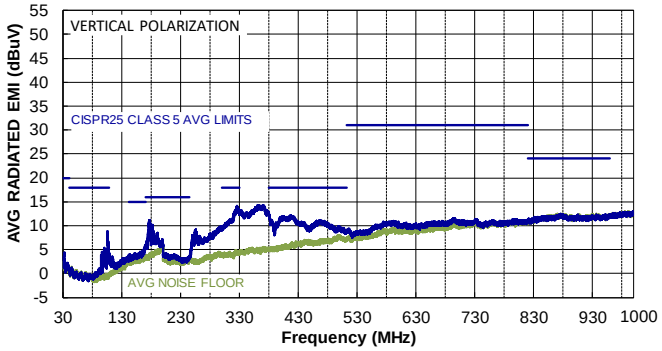
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



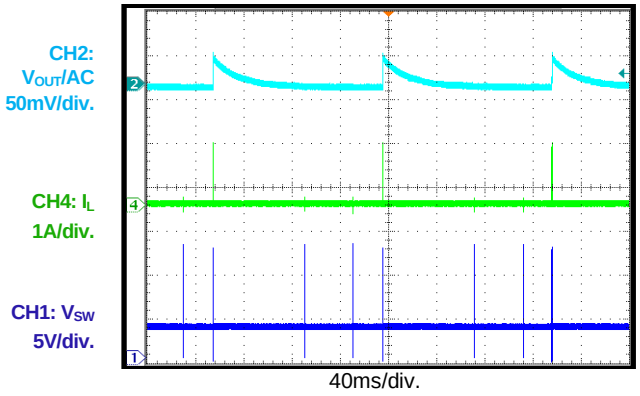
Note:

6) The EMC test results are based on the application circuit with EMI filters (see Figure 13).

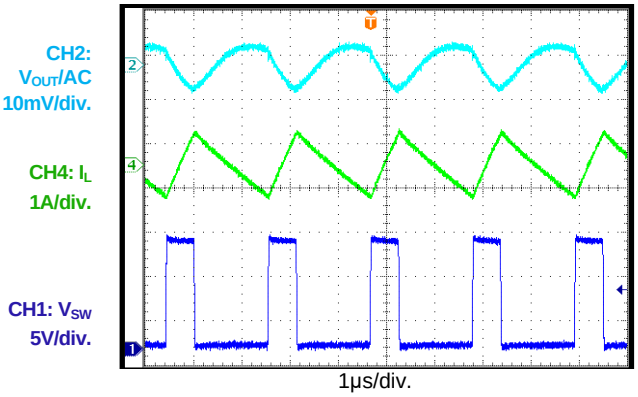
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

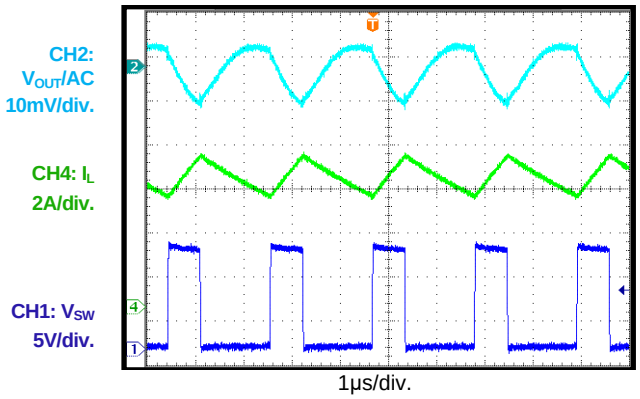
Steady State
I_{OUT} = 0A, AAM



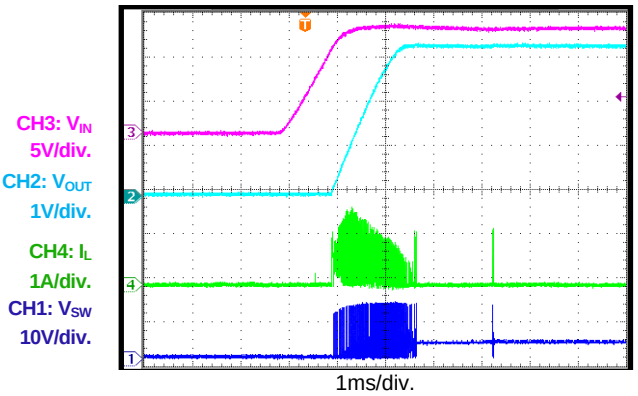
Steady State
I_{OUT} = 0A, FCCM



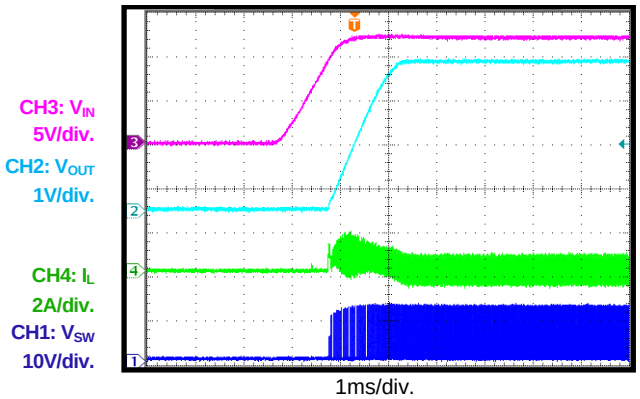
Steady State
I_{OUT} = 6A



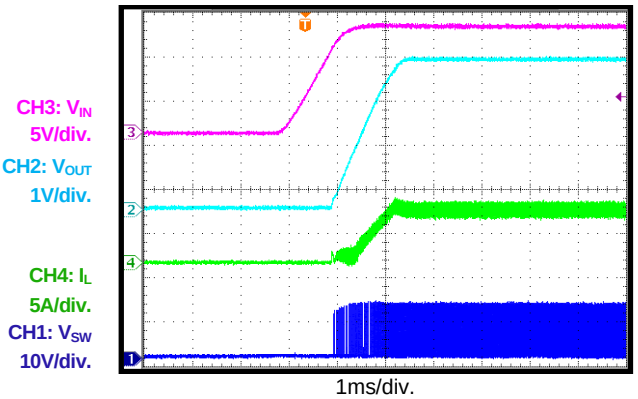
Start-Up through V_{IN}
I_{OUT} = 0A, AAM



Start-Up through V_{IN}
I_{OUT} = 0A, FCCM



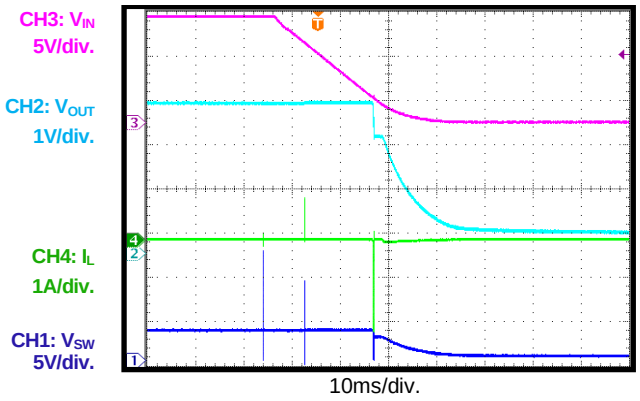
Start-Up through V_{IN}
I_{OUT} = 6A



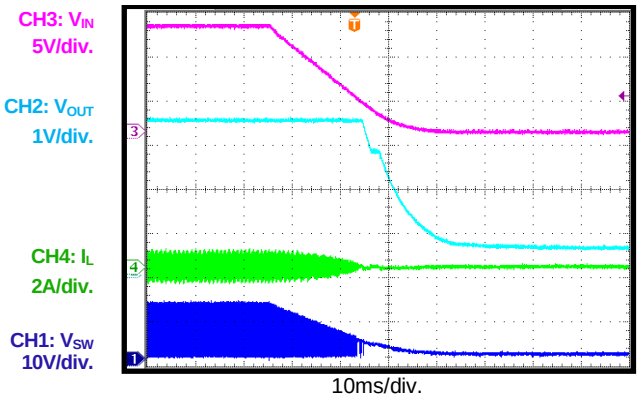
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

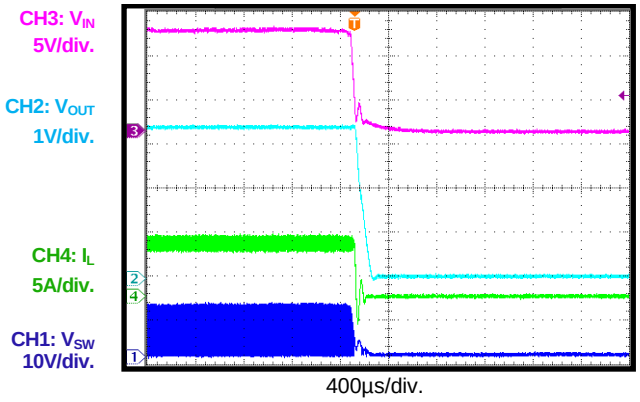
Shutdown through V_{IN}
I_{OUT} = 0A, AAM



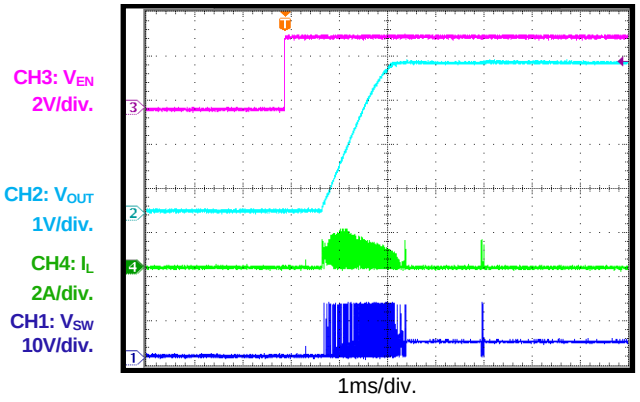
Shutdown through V_{IN}
I_{OUT} = 0A, FCCM



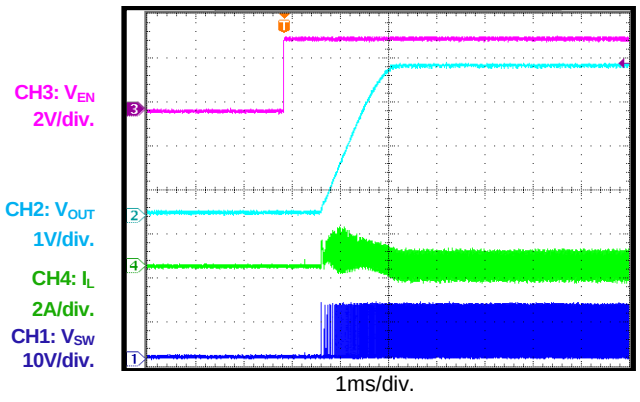
Shutdown through V_{IN}
I_{OUT} = 6A



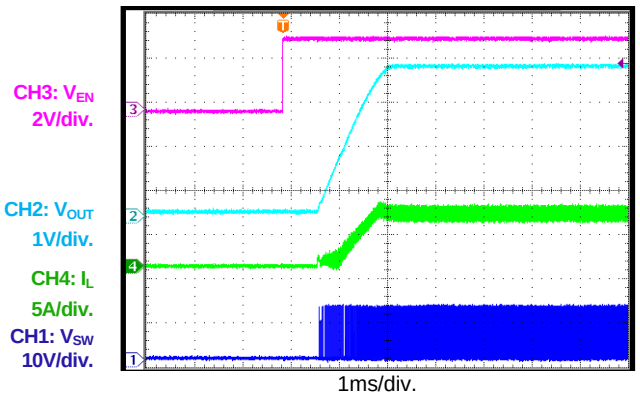
Start-Up through EN
I_{OUT} = 0A, AAM



Start-Up through EN
I_{OUT} = 0A, FCCM



Start-Up through EN
I_{OUT} = 6A

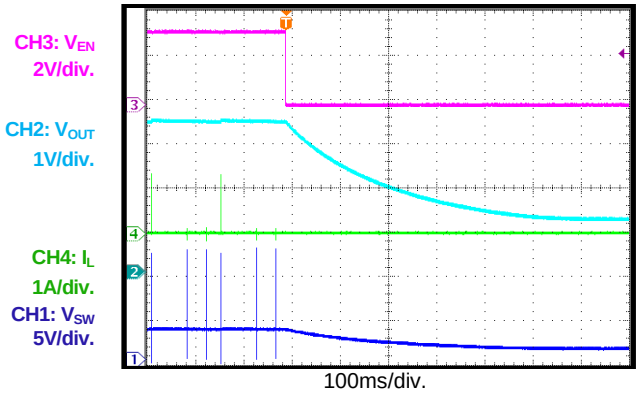


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

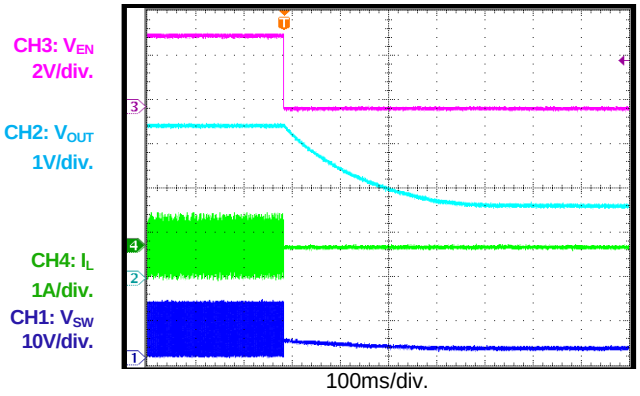
Shutdown through EN

I_{OUT} = 0A, AAM



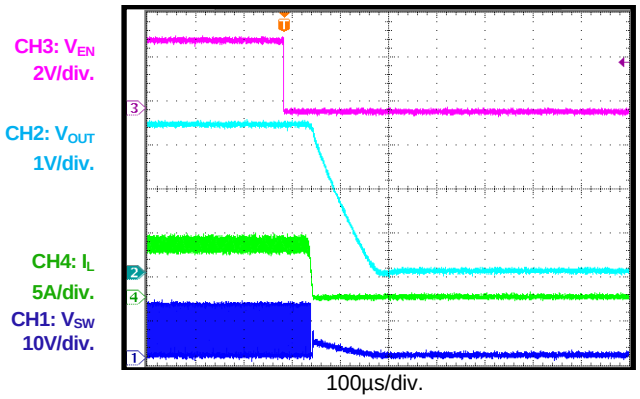
Shutdown through EN

I_{OUT} = 0A, FCCM



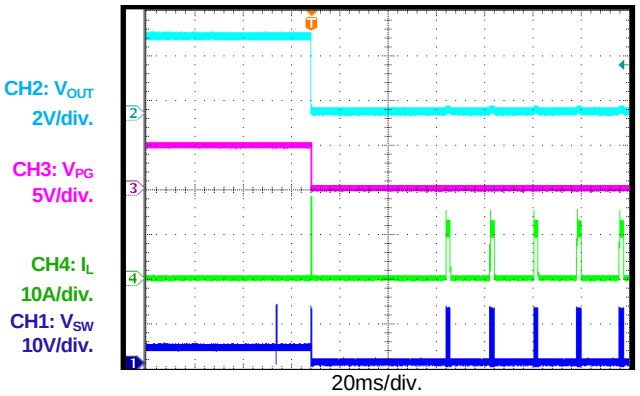
Shutdown through EN

I_{OUT} = 6A



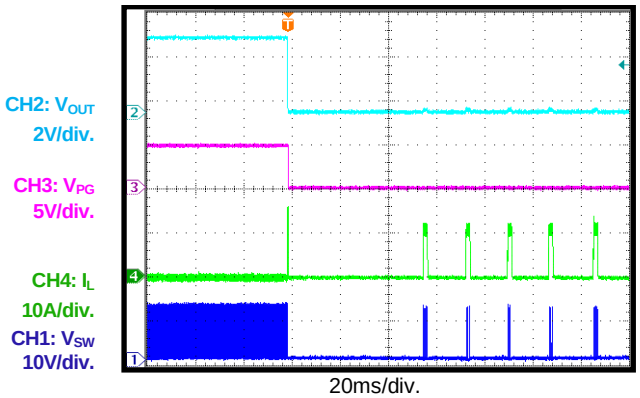
SCP Entry

I_{OUT} = 0A, AAM



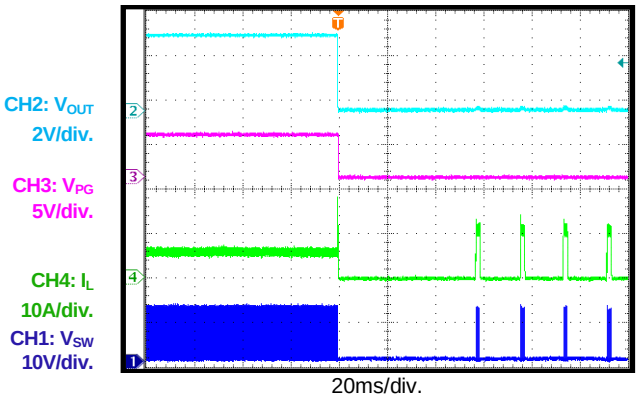
SCP Entry

I_{OUT} = 0A, FCCM



SCP Entry

I_{OUT} = 6A

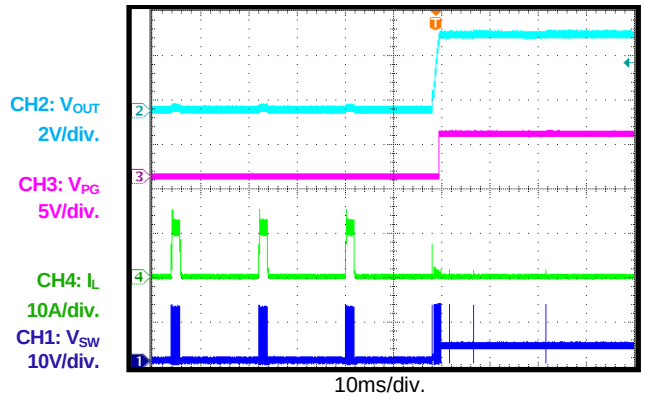


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

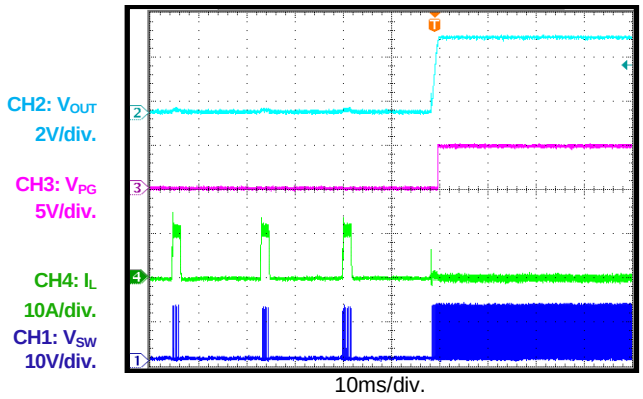
SCP Recovery

I_{OUT} = 0A, AAM



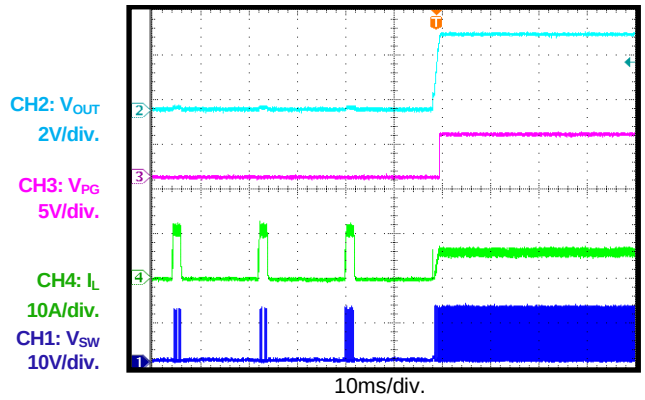
SCP Recovery

I_{OUT} = 0A, FCCM

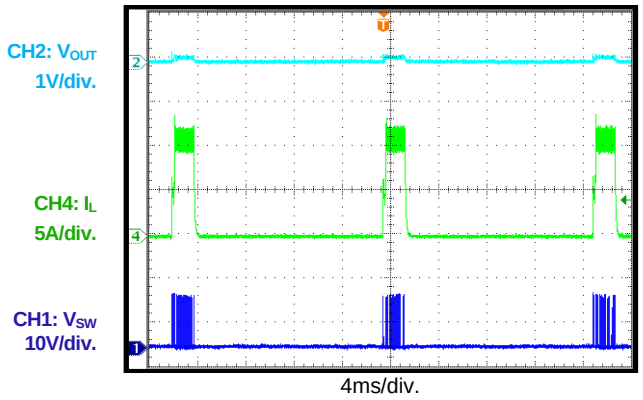


SCP Recovery

I_{OUT} = 6A

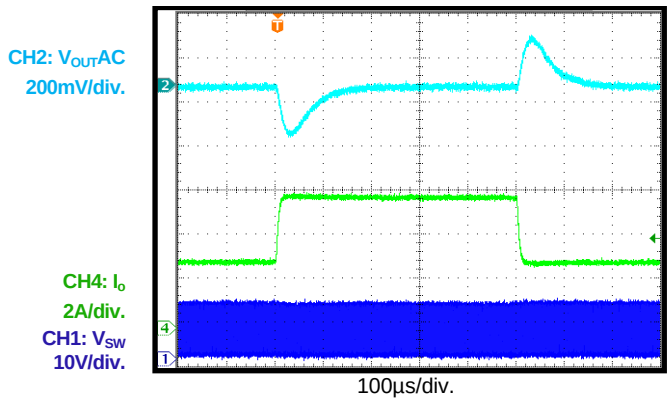


SCP Steady State



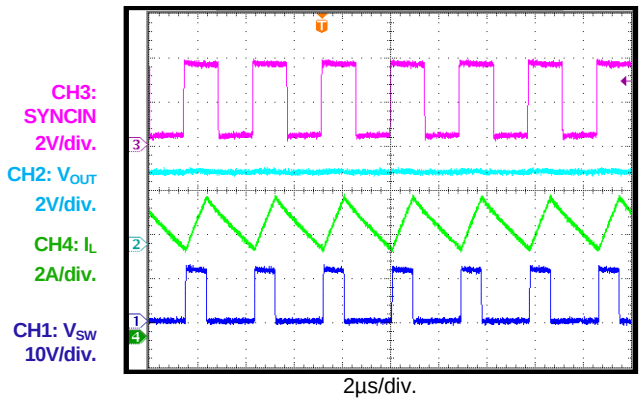
Load Transient

I_{OUT} = 3A to 6A, 1.6A/µs



SYNCIN Operation

I_{OUT} = 6A, SYNC frequency = 350kHz

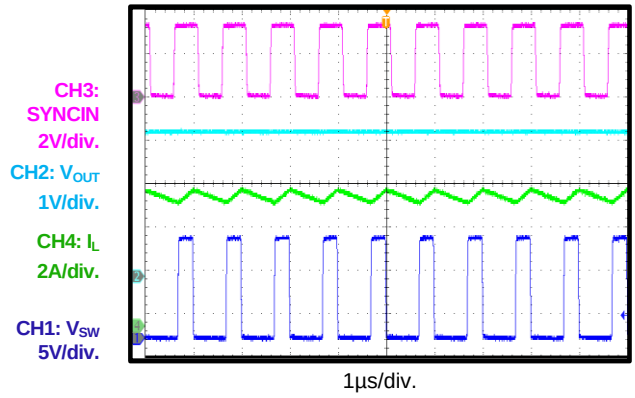


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

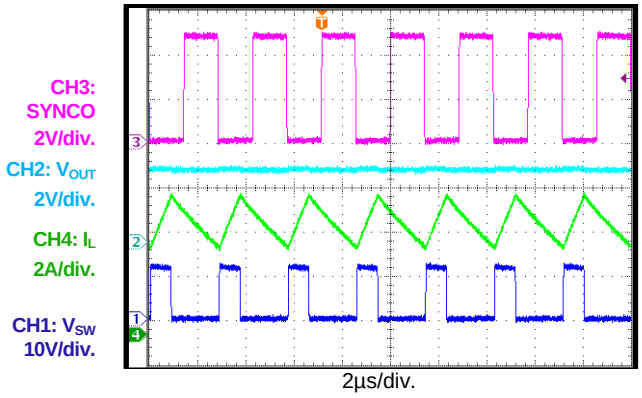
SYNCIN Operation

I_{OUT} = 6A, SYNC frequency = 1000kHz



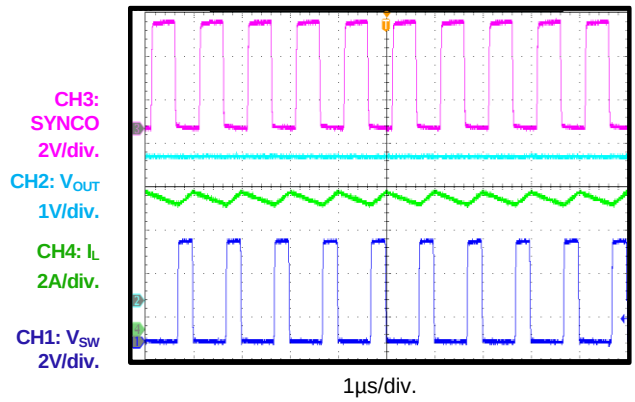
SYNCO Operation

I_{OUT} = 6A, SYNC frequency = 350kHz



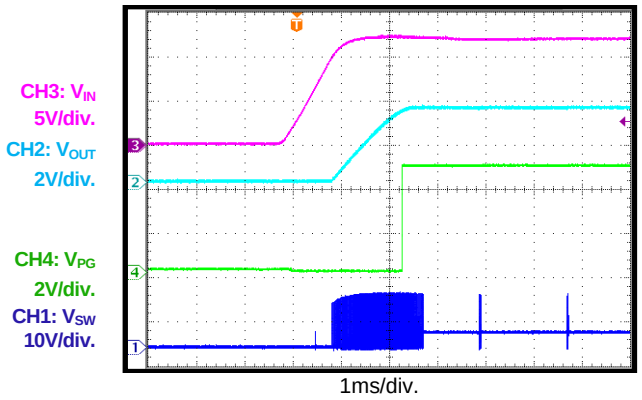
SYNCO Operation

I_{OUT} = 6A, SYNC frequency = 1000kHz



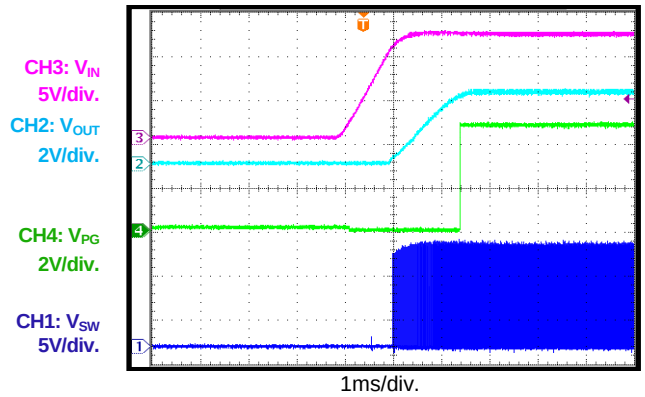
PG Start-Up through V_{IN}

I_{OUT} = 0A



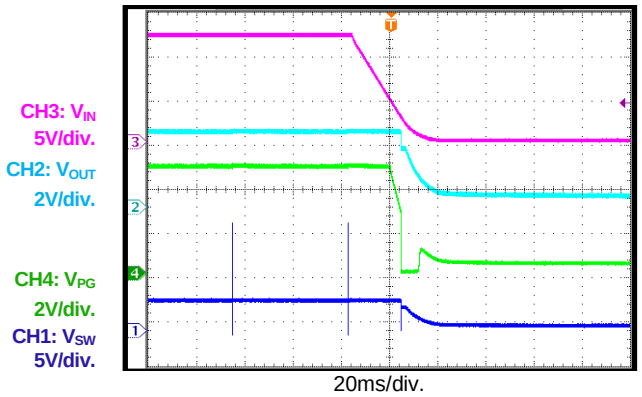
PG Start-Up through V_{IN}

I_{OUT} = 6A



PG Shutdown through V_{IN}

I_{OUT} = 0A

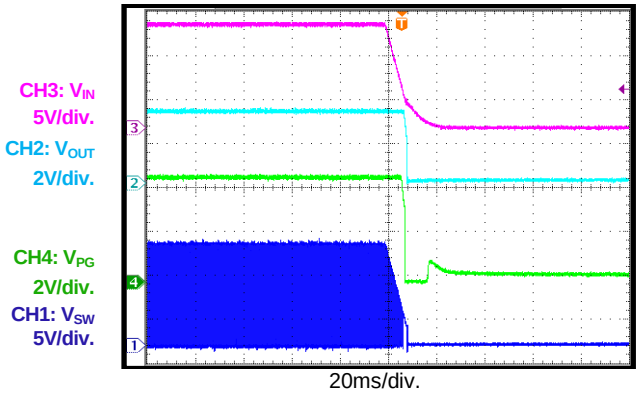


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

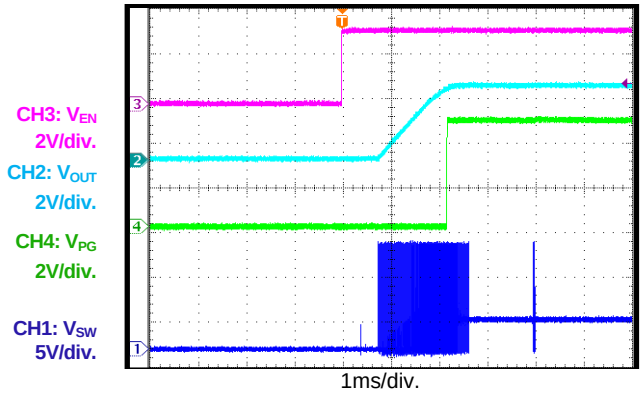
PG Shutdown through V_{IN}

I_{OUT} = 6A



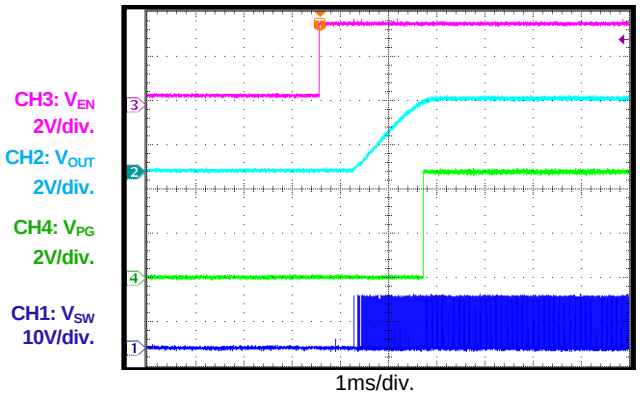
PG Start-Up through EN

I_{OUT} = 0A



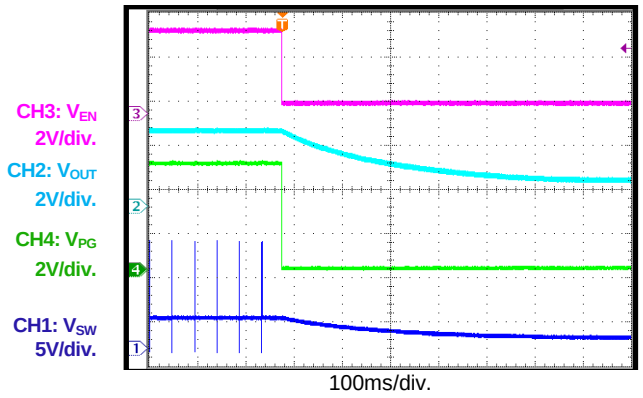
PG Start-Up through EN

I_{OUT} = 6A



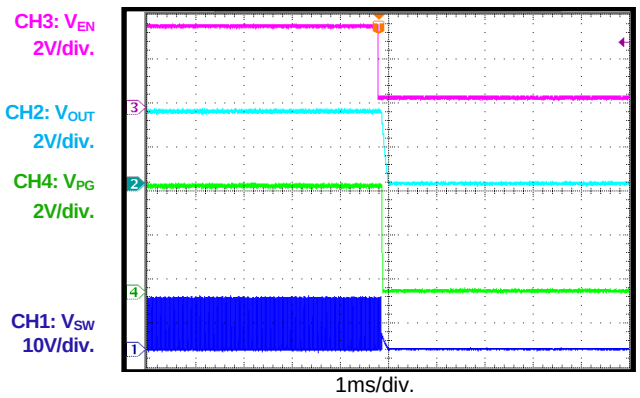
PG Shutdown through EN

I_{OUT} = 0A



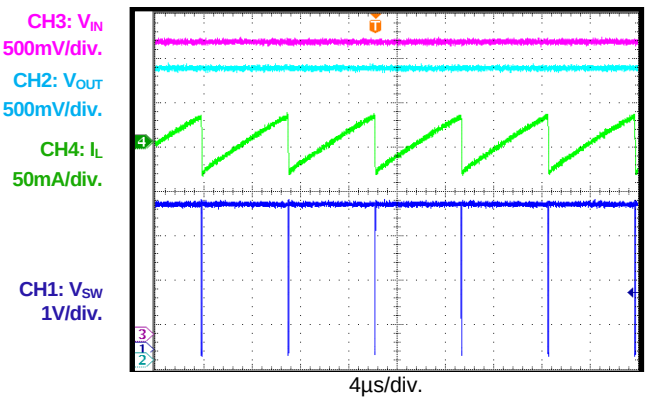
PG Shutdown through EN

I_{OUT} = 6A



Dropout Operation

V_{IN} = 3.3V, V_{OUT} set to 3.3V, I_{OUT} = 0A

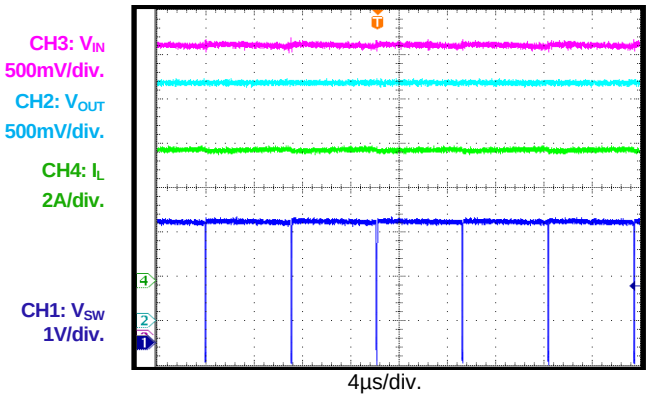


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

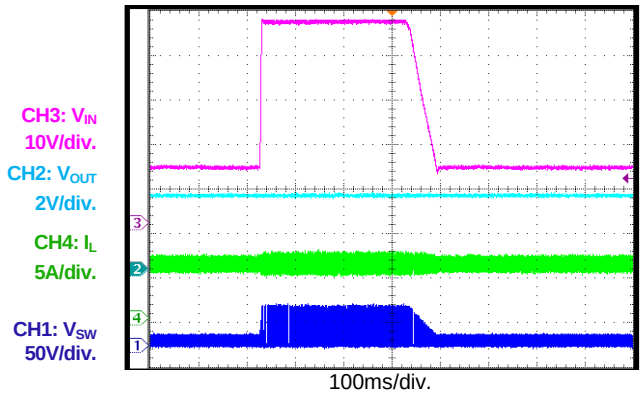
Dropout Operation

V_{IN} = 3.3V, V_{OUT} set to 3.3V, I_{OUT} = 6A



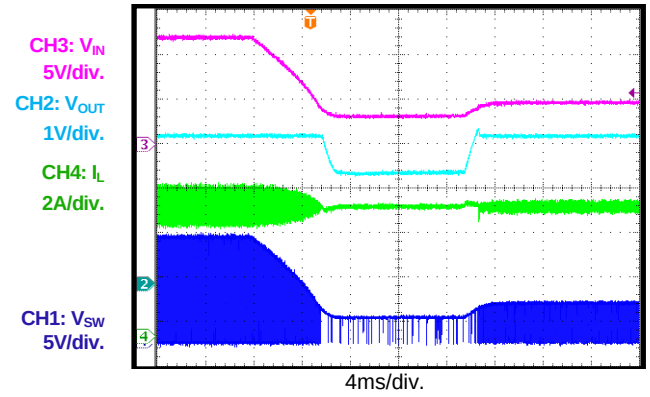
Load Dump

V_{IN} = 12V to 36V, I_{OUT} = 6A



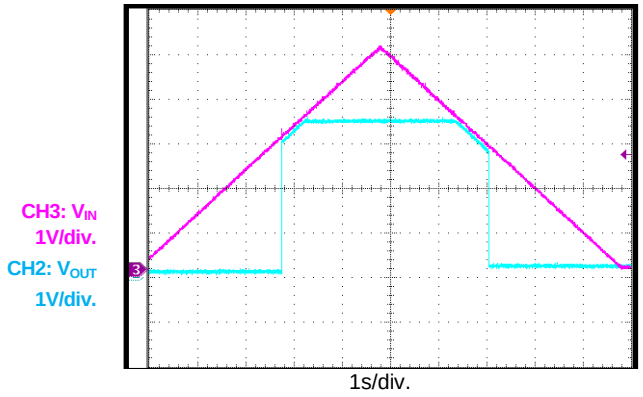
Cold Crank

V_{IN} = 12V to 3.3V to 5V, I_{OUT} = 6A



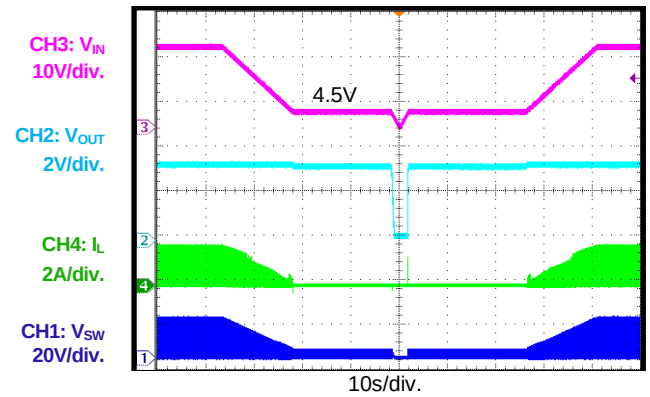
V_{IN} Ramp Up and Down

I_{OUT} = 0.1A



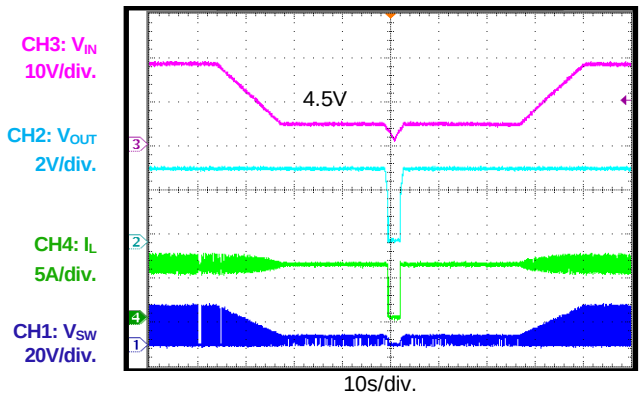
V_{IN} Ramp Down and Up

I_{OUT} = 1mA



V_{IN} Ramp Down and Up

I_{OUT} = 6A

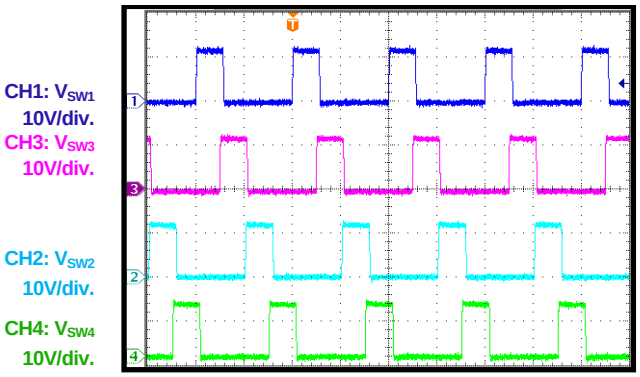


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

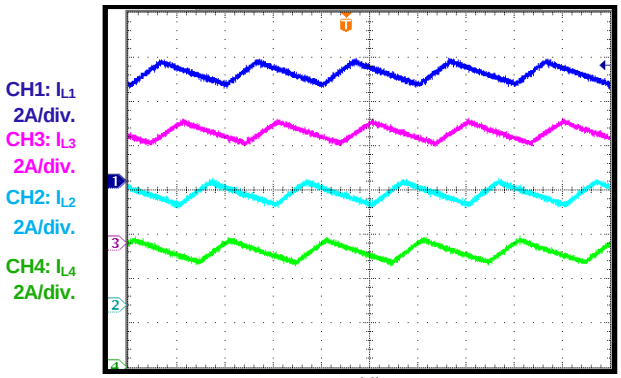
Steady State

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 20A, 4-phase



Steady State

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 20A, 4-phase



FUNCTION BLOCK DIAGRAM

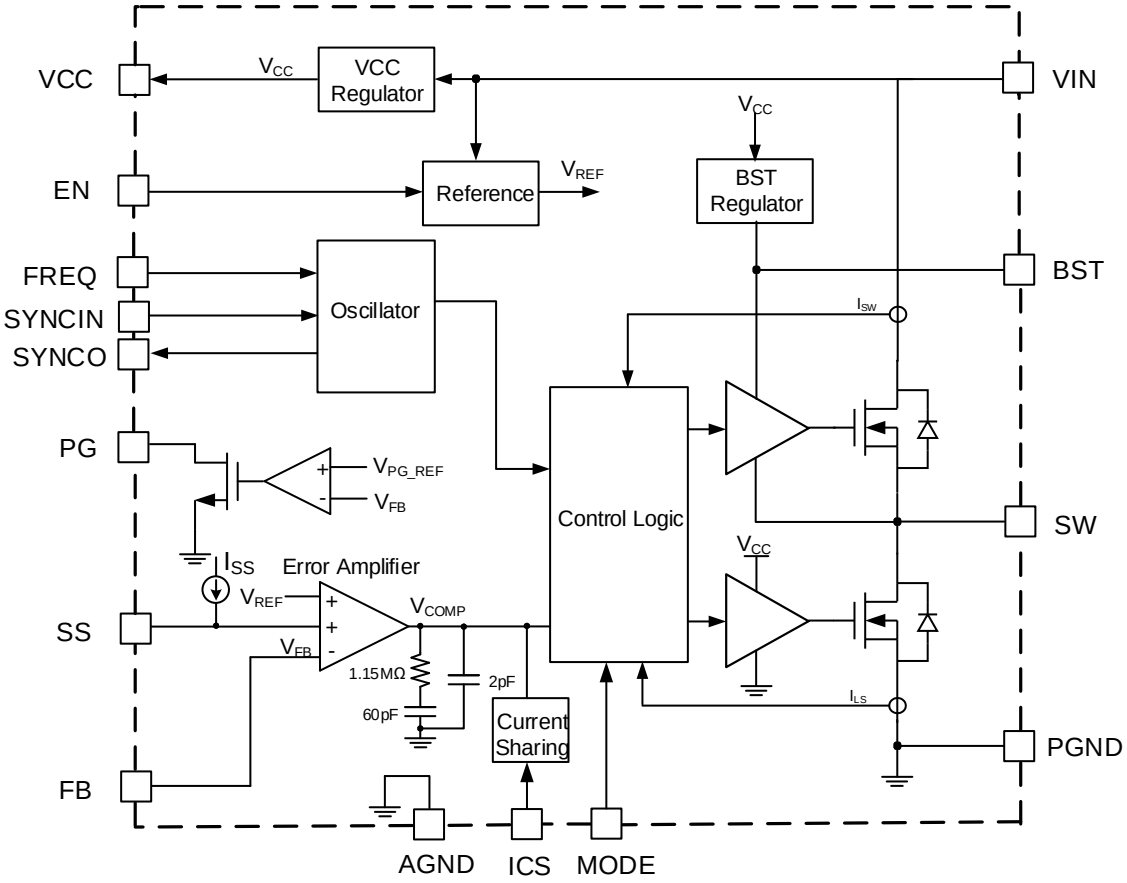


Figure 1: Functional Block Diagram

Timing Sequence

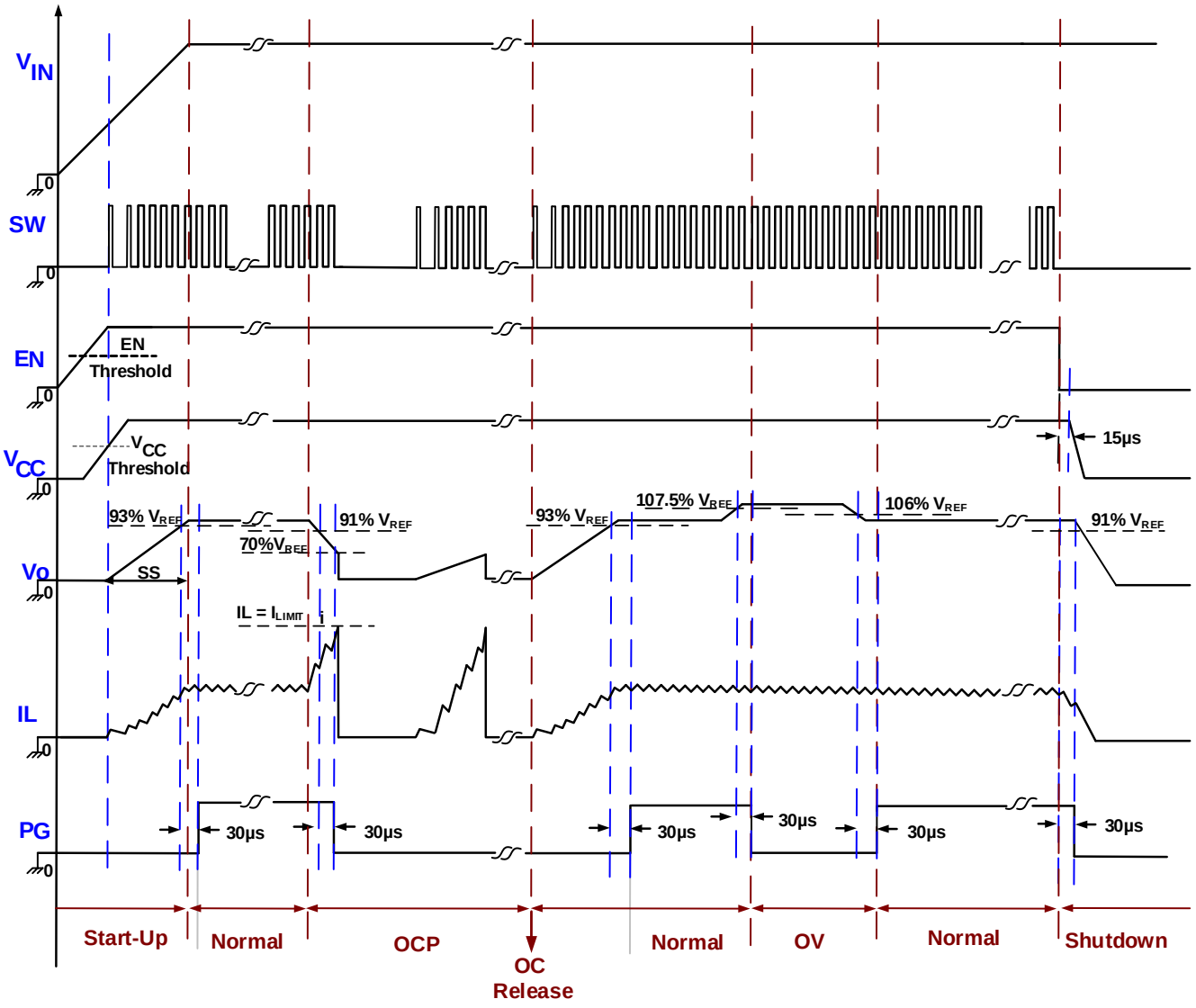


Figure 2: Timing Sequence

OPERATION

The MPQ4436/4436A is a synchronous, step-down switching regulator with integrated internal high-side and low-side power MOSFETs. It provides 6A of highly efficient output with current mode control.

It features a wide input voltage range, programmable switching frequency, external soft start, and precision current limiting. Its very low operational quiescent current makes it ideal for battery-powered applications.

PWM Control

At moderate to high output current, the MPQ4436/4436A operates in a fixed-frequency, peak current control mode to regulate the output voltage. A PWM cycle is initiated by the internal clock. At the rise edge of the clock, the high-side MOSFET (HS-FET) turns on and remains on until its current reaches the value set by the internal COMP voltage (V_{COMP}). Once the HS-FET is on, it remains on for at least 100ns.

When the high-side power switch is off, the low-side MOSFET (LS-FET) turns on immediately and remains on until the next cycle starts. Once the LS-FET is on, it remains on for at least 80ns before next cycle starts.

If, in one PWM period, the current in the HS-FET does not reach the COMP-set current value, the HS-FET remains on, saving a turn-off operation. The HS-FET is forced off if the on time lasts about 10µs, even though COMP is not reached.

Light-Load Operation

In a light-load condition, the MPQ4436/4436A can work at two different operation modes by setting the MODE pin to one of two different statuses.

The MPQ4436/4436A works in forced CCM when the CCM pin is pulled above 1.8V. The part works with fixed frequency from no load to full load at this mode. The advantage of CCM is the controllable frequency and lower output ripple at light load.

The MPQ4436/4436A works in asynchronous advanced mode (AAM) when the MODE pin is pulled below 0.4V. AAM is meant to optimize the efficiency during light-load and no-load conditions.

When AAM is enabled, the MPQ4436/4436A first enters non-synchronous operation as long as the inductor current approaches zero at light load. If the load is further decreased or there is no load that makes V_{COMP} decrease to the set value, the MPQ4436/4436A enters AAM. In AAM, the internal clock is reset every time V_{COMP} crosses over the set value. The crossover time is taken as the benchmark of the next clock. When the load increases and V_{COMP} exceeds the set value, the operation mode is DCM or CCM, which has a constant switching frequency (see Figure 3).

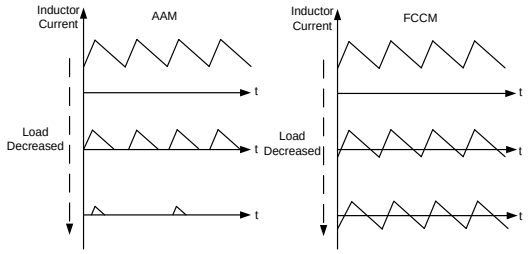


Figure 3: AAM and FCCM

Error Amplifier

The error amplifier compares the FB pin voltage with the internal reference (0.815V) and outputs a current proportional to the difference between the two. This output current is then used to charge the compensation network to form V_{COMP}, which is used to control the power MOSFET current.

During operation, the minimum V_{COMP} is clamped to 0.9V, and its maximum is clamped to 2.0V. COMP is internally pulled down to GND in shutdown mode.

Internal Regulator VCC

Most of the internal circuitry is powered on by the internal 4.9V VCC regulator. This regulator takes VIN as the input and operates in the full VIN range. When VIN is greater than 4.9V, VCC is in full regulation. When VIN is below this point, the output VCC degrades.

Bootstrap Charging

The bootstrap capacitor is charged and regulated to about 5V by the dedicated internal bootstrap regulator. When the voltage between a BST and SW nodes is lower than its regulation, a PMOS pass transistor connected from VCC to BST turns on to charge the bootstrap capacitor. External

circuitry should provide enough voltage headroom to facilitate the charging.

When the HS-FET is on, BST is above VCC, so the bootstrap capacitor cannot be charged.

In higher duty cycle operation conditions, the time period available to the bootstrap charging is less, so the bootstrap capacitor may not be charged sufficiently. If the external circuit has not had sufficient voltage and time to charge the bootstrap capacitor, extra external circuitry can be used to ensure the bootstrap voltage is in the normal operation range.

Low Dropout Operation and BST Refresh

To improve dropout, the MPQ4436/4436A is designed to operate at close to 100% duty cycle as long as the BST-to-SW voltage is greater than 2.5V. When the voltage from BST to SW drops below 2.5V, the HS-FET turns off using a UVLO circuit, which allows the LS-FET to conduct and refresh the charge on the BST capacitor. In DCM mode or PSM mode, the LS-FET is forced on to refresh the BST voltage.

Since the supply current sourced from the BST capacitor is low, the HS-FET remains on for more switching cycles than are required to refresh the capacitor. Therefore, the effective duty cycle of the switching regulator is high.

The effective duty cycle during dropout of the regulator is mainly influenced by the voltage drops across the power MOSFET, inductor resistance, the low-side diode, and PCB resistance.

Enable Control

EN is a digital control pin that turns the regulator on and off (see Figure 4). It offers two main features:

1) Enabled by external logic H/L signal

When EN is pulled below the falling voltage threshold (0.85V), the chip is put into the lowest shutdown current mode. Forcing this pin above the EN rising threshold voltage (1V) turns on the part.

2) Programmable VIN under-voltage lockout (UVLO)

With high enough V_{IN}, the chip can be enabled and disabled by the EN pin. With the internal current source, this circuit can generate a programmable V_{IN} UVLO and hysteresis.

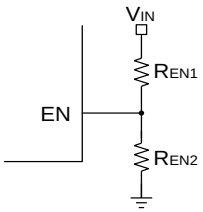


Figure 4: Enable Divider Circuit

Frequency Programmable and Foldback

The MPQ4436/4436A oscillating frequency is programmed either by an external resistor (R_{FREQ}) from the FREQ pin to ground, or by a logic level SYNC signal.

To get an expected switching frequency (f_{SW}), select the R_{FREQ} value following the f_{SW} vs. R_{FREQ} curve in the Typical Performance Characteristics (TPC) section on page 14. Note that f_{SW} will fold back at high V_{IN} when set at high values to avoid triggering the minimum on time and the output going out of regulation. The f_{SW} vs. V_{IN} curve in the TPC section shows an example when R_{FREQ} is 12kΩ. The corresponding f_{SW} is about 2.1MHz at VIN = 12V, and decreases to be below 1.5MHz when VIN is above 18V. Thus the switching frequency drops into the AM band (<1.8MHz), which should be avoided for car battery applications considering EMI compliance. So the recommended f_{SW} of the MPQ4436/4436A for car battery applications is 350kHz to 1000kHz. Higher frequencies may still be supported for the applications that do not have critical limits on the switching frequency or have relatively low, stable input voltages.

Frequency Spread Spectrum (MPQ4436A Only)

MPQ4436A uses a 12kHz modulation frequency with at most a 128-step triangular profile to spread the internal oscillator frequency over a 20% (±10%) window. The steps are fixed and independent of the setting oscillator frequency to optimize the frequency spread spectrum (FSS) performance (see Figure 5).

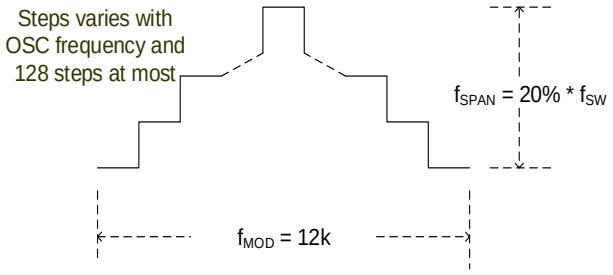


Figure 5: Spread Spectrum Scheme

Side bands are created by modulating the switching frequency with the triangle modulation waveform. The emission power of the fundamental switching frequency and its harmonics is distributed into smaller pieces. Thus, the peak EMI noise is reduced significantly.

Soft Start

Soft start is implemented to prevent the converter output voltage from overshooting during start-up.

When the soft-start period starts, an internal current source begins charging the external soft-start capacitor. When the soft-start voltage (SS) is below the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS exceeds REF, REF regains control. C_{SS} can be calculated with Equation (1):

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} = 6.25 \times t_{SS}(ms) \quad (1)$$

The SS pins can be used for tracking and sequencing.

Pre-Bias Start-Up

For the MPQ4436/4436A, if FB > SS - 150mV at start-up (which means the output has a pre-bias voltage), neither the HS-FET nor LS-FET are turned on until SS exceeds FB.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from thermally running away. When the silicon die temperature exceeds its upper threshold, it shuts down the power MOSFETs. When the temperature falls below its lower threshold, the chip is enabled again.

Current Comparator and Current Limit

The power MOSFET current is accurately sensed via a current-sense MOSFET. It is then fed to the high speed current comparator for current mode control. The current comparator takes this sensed current as one of its inputs.

When the HS-FET turns on, the comparator is blanked until the end of the turn-on transition to dodge the noise. Then, the comparator compares the power switch current with V_{COMP}. When the sensed current exceeds V_{COMP}, the comparator outputs low to turn off the HS-FET . The maximum current of the internal power MOSFET is internally limited cycle by cycle.

Hiccup Protection

When the output is shorted to ground, causing the output voltage to drop below 70% of its nominal output, the IC is shut down momentarily and begins discharging the soft-start capacitor. It restarts with a full soft start when the soft-start capacitor is fully discharged. This hiccup process is repeated until the fault is removed.

Start-Up and Shutdown

If both VIN and EN exceed their respective thresholds, the chip starts. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

While the internal supply rail is up, an internal timer holds the power MOSFET off for about 50µs to blank the start-up glitches. When the soft-start block is enabled, it first holds its SS output low to ensure the remaining circuitries are ready, then slowly ramps up.

Three events shut down the chip: EN low, VIN low, and thermal shutdown. In the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

Power Good Output

The MPQ4436/4436A includes an open-drain power good output that indicates the output. A pull-up resistor to power source is needed if PG is used. It goes high if the output voltage is within 93% to 106% of the nominal voltage, and goes low when the output voltage is above 107.5% or below 91% of the nominal voltage.

SYNCIN and SYNCO

The switching frequency can be synced to the rising edge of the clock signal applied at SYNCIN. The recommended SYNCIN frequency range is 350kHz to 1000kHz. Ensure that the off time of SYNCIN is shorter than the internal oscillator period, otherwise the internal clock may turn on the HS-FET before the rising edge of SYNCIN. There is no other special limit on the pulse width of SYNCIN, but note that there is always parasitic capacitance of the pad there. If the

pulse width is too short, a clear rising and falling edge may not be seen due to the parasitic capacitance. A pulse longer than 100ns is recommended in application.

When applying SYNCIN in AAM, Drive SYNCIN below its specified threshold (0.4V) or leaving SYNCIN floating before MPQ4436/4436A starting up to enter AAM. And then adding external SYNCIN clock.

The SYNCO pin provides a default 180º phase-shifted clock to the internal oscillator when there is no SYNCIN signal or a clock signal reverse to SYNCIN if an external clock signal is applied at SYNCIN (see Figure 6). This makes enabling a dual-phase, interleaved configuration easy (see Figure 7).

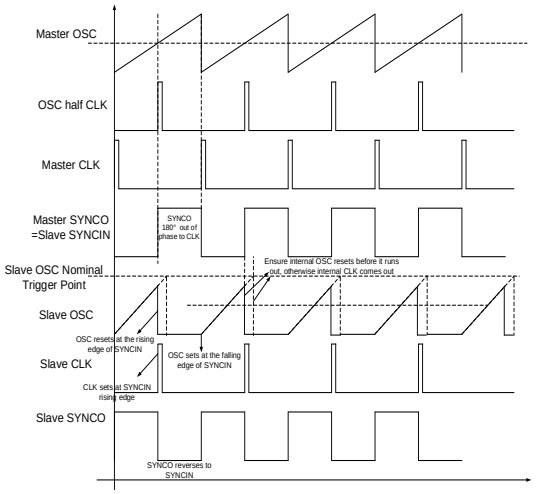


Figure 6: SYNCIN & SYNCO Scheme

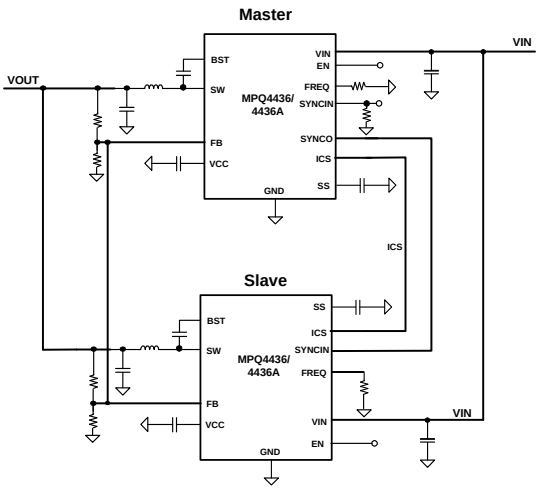


Figure 7: Dual-Phase Configuration

For multi-phase applications, VOUT, FB, and ICS of the chips in parallel need to be connected together. SYNCO of the master is connected to the SYNCIN pin of the slave for phase interleaved configurations (see Figure 8).

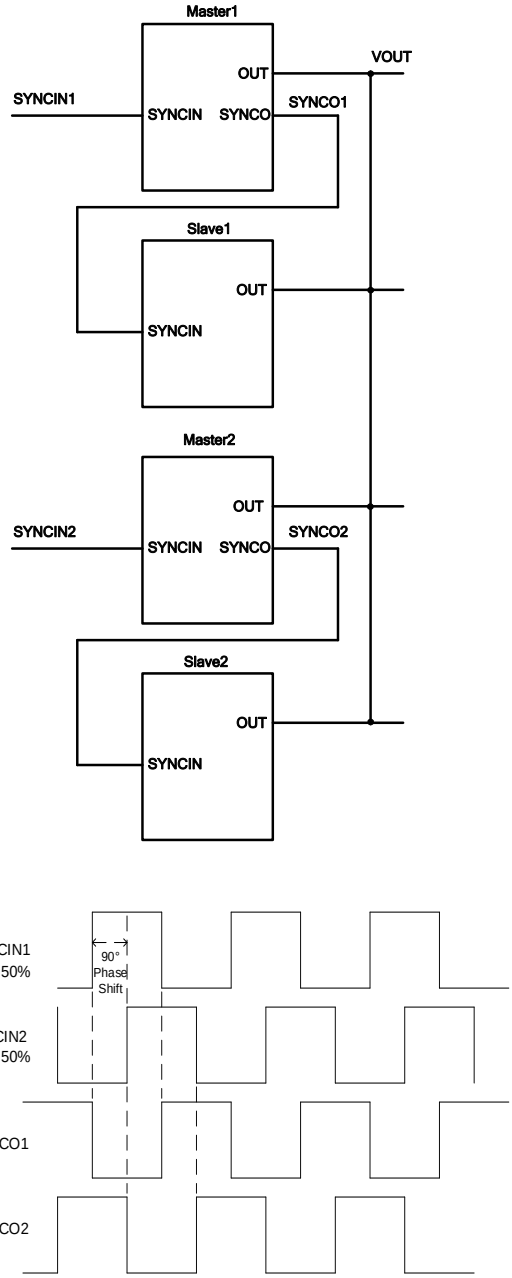


Figure 8: Four-Phase Configuration

APPLICATION INFORMATION

Setting the BST Capacitor

If using the MPQ4436/4436A in CCM only, use a BST capacitor of 0.2µF or greater nominal. If using AAM mode, the external BST capacitor should be greater than 0.2µF. Alternately, choose the BST capacitor with Equation (2) and Equation (3):

$$C_{BST}(\mu F) \geq \frac{75 \times C_{OUT}(\mu F) \times 10^{-3}}{I_{MIN}(\mu A)} \quad (2)$$

$$C_{BST}(\mu F) \geq \frac{80}{I_{MIN}(\mu A) \times L(\mu H)} \quad (3)$$

If the calculated C_{BST} is greater than 6.8µF, contact a field applications engineer to verify the design.

Setting the VCC Capacitor

The VCC capacitor should be 10 times larger than the boost capacitor, and at least 4.7µF nominal. A VCC capacitor greater than 68µF nominal is not recommended.

Setting the Output Voltage

The external resistor divider connected to FB sets the output voltage (see Figure 9).

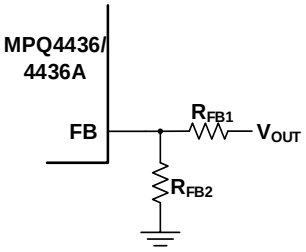


Figure 9: Feedback Network

Choose R_{FB1} to be about 40kΩ. Then calculate R_{FB2} with Equation (4):

$$R_{FB2} \geq \frac{R_{FB1}}{\frac{V_{OUT}}{0.8V} - 1} \quad (4)$$

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 1: Resistor Selection for Output Voltages

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)
3.3	100 (1%)	31.6 (1%)
5	100 (1%)	19.1 (1%)

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, use a 4.7µF to 10µF capacitor. It is strongly recommended to use another, lower value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and GND as possible.

Since C_{IN} absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (5):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (5)$$

The worst-case condition occurs at VIN = $2V_{OUT}$, calculated with Equation (6):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low-ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \cdot (1 - \frac{V_{OUT}}{V_{IN}}) \cdot (R_{ESR} + \frac{1}{8 f_{SW} \times C_{OUT}}) \quad (8)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (10)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ4436/4436A can be optimized for a wide range of capacitance and ESR values.

Selecting the Inductor

A 1µH to 10µH inductor with a DC current rating at least 25% higher than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductor value is to allow the inductor ripple current to be approximately 30% of the maximum load current. The inductance value can be calculated with Equation (11):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (12):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (12)$$

VIN UVLO Setting

The MPQ4436/4436A has an internal, fixed under-voltage lockout (UVLO) threshold. The rising threshold is 3V, while the falling threshold is about 2.65V. For applications that need a higher UVLO point, an external resistor divider between VIN and EN can be used to achieve a higher equivalent UVLO threshold (see Figure 10).

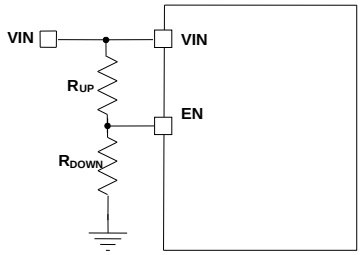


Figure 10: Adjustable UVLO Using EN Divider

The UVLO threshold can be calculated with Equation (13) and Equation (14):

$$INUV_{RISING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN\_RISING} \quad (13)$$

$$INUV_{FALLING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN\_FALLING} \quad (14)$$

Where V_{EN_RISING} is 1V, and $V_{EN\_FALLING}$ is 0.85V.

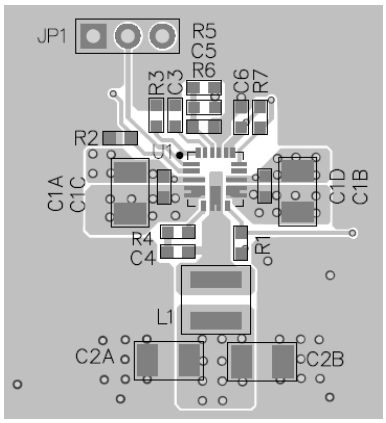
PCB Layout Guidelines [7]

Efficient PCB layout, especially for input capacitor placement, is critical for stable operation. A 4-layer layout is strongly recommended to achieve better thermal performance. For best results, refer to Figure 11 and follow the guidelines below:

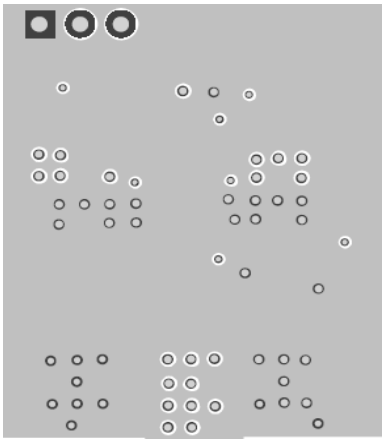
1. Place symmetric input capacitors as close to VIN and GND as possible.
2. Use a large ground plane to connect directly to PGND.
3. Add vias near PGND if the bottom layer is a ground plane.
4. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
5. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to minimize high-frequency noise.
6. Keep the connection of the input capacitor and VIN as short and wide as possible.
7. Place the VCC capacitor as close to VCC and GND as possible.
8. Route SW and BST away from sensitive analog areas, such as FB.
9. Place the feedback resistors close to the chip to ensure the trace that connects to FB is as short as possible.
10. Use multiple vias to connect the power planes to the internal layers.

Note:

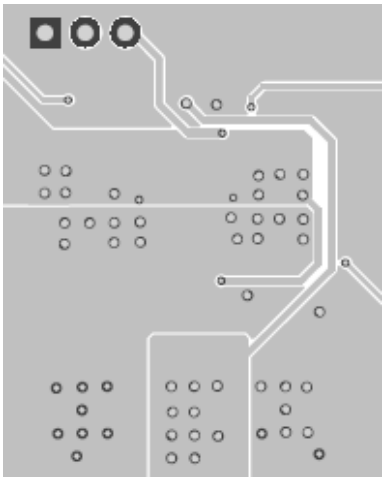
7) The recommended PCB layout is based on Figure 12.



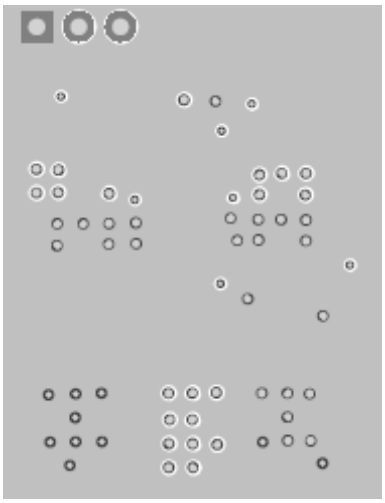
Top Layer



Inner Layer 1



Inner Layer 2



Bottom Layer

Figure 11: Recommended PCB Layout

TYPICAL APPLICATION

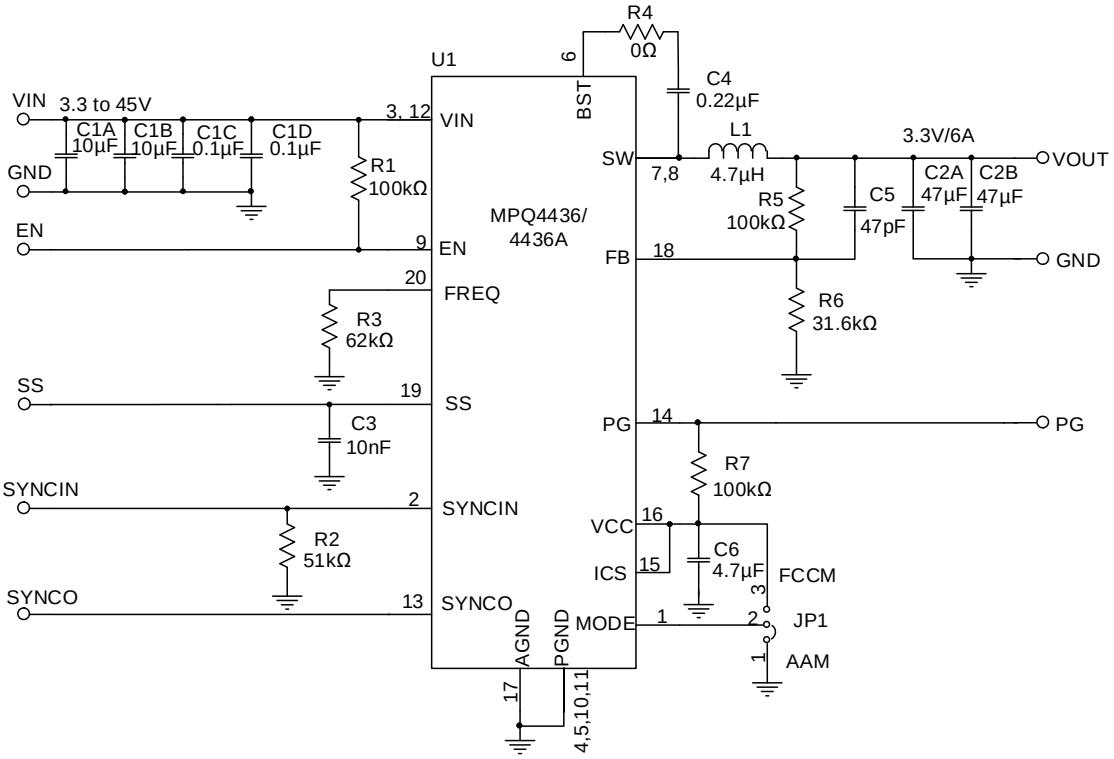


Figure 12: Single-Phase, V_{OUT} = 3.3V, f_{SW} = 470kHz

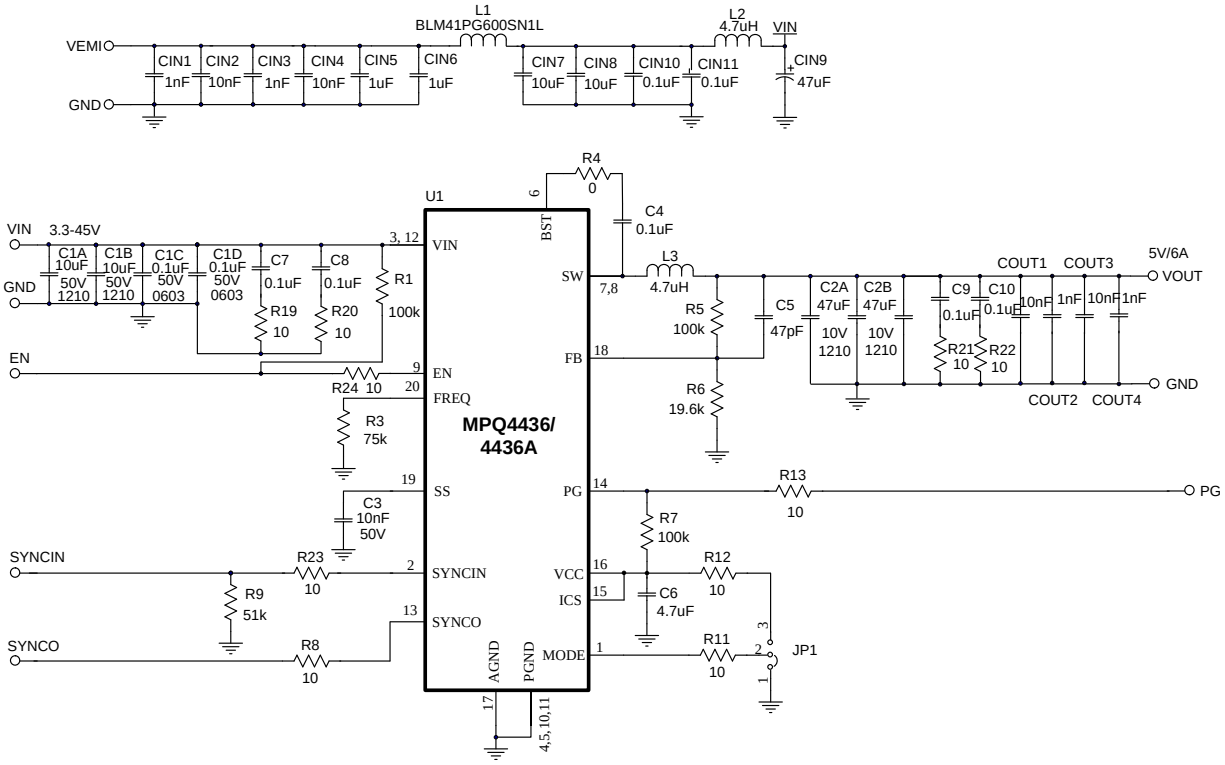


Figure 13: V_{OUT} = 5V, f_{SW} = 410kHz with EMI Filters

TYPICAL APPLICATION *(continued)*

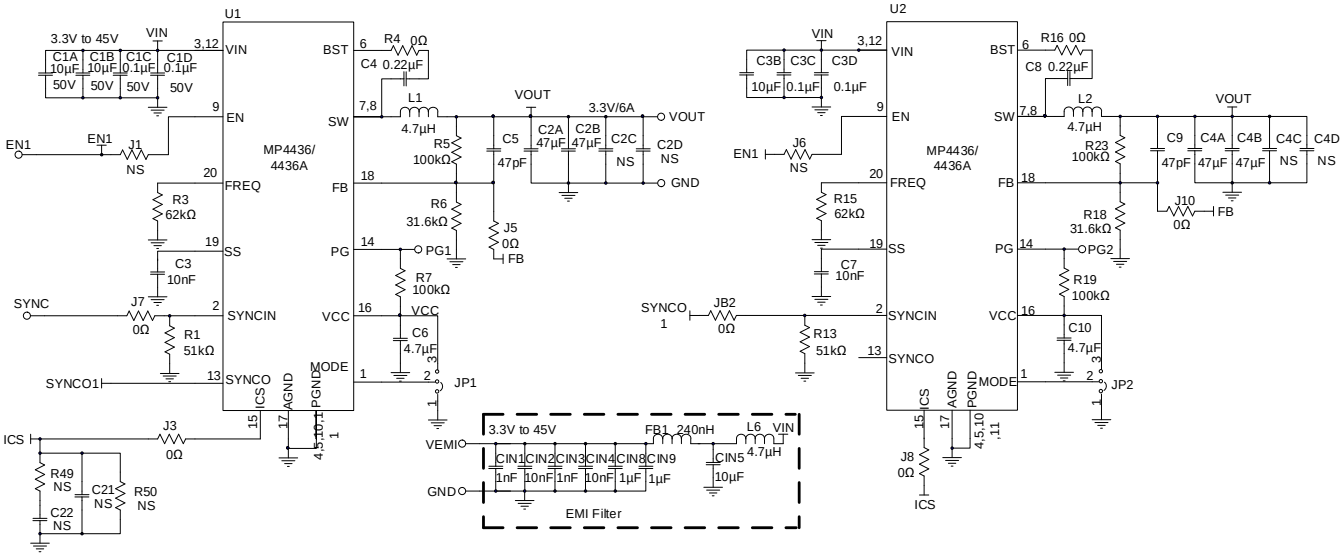


Figure 14: Dual-Phase, V_{OUT} = 3.3V, f_{SW} = 470kHz

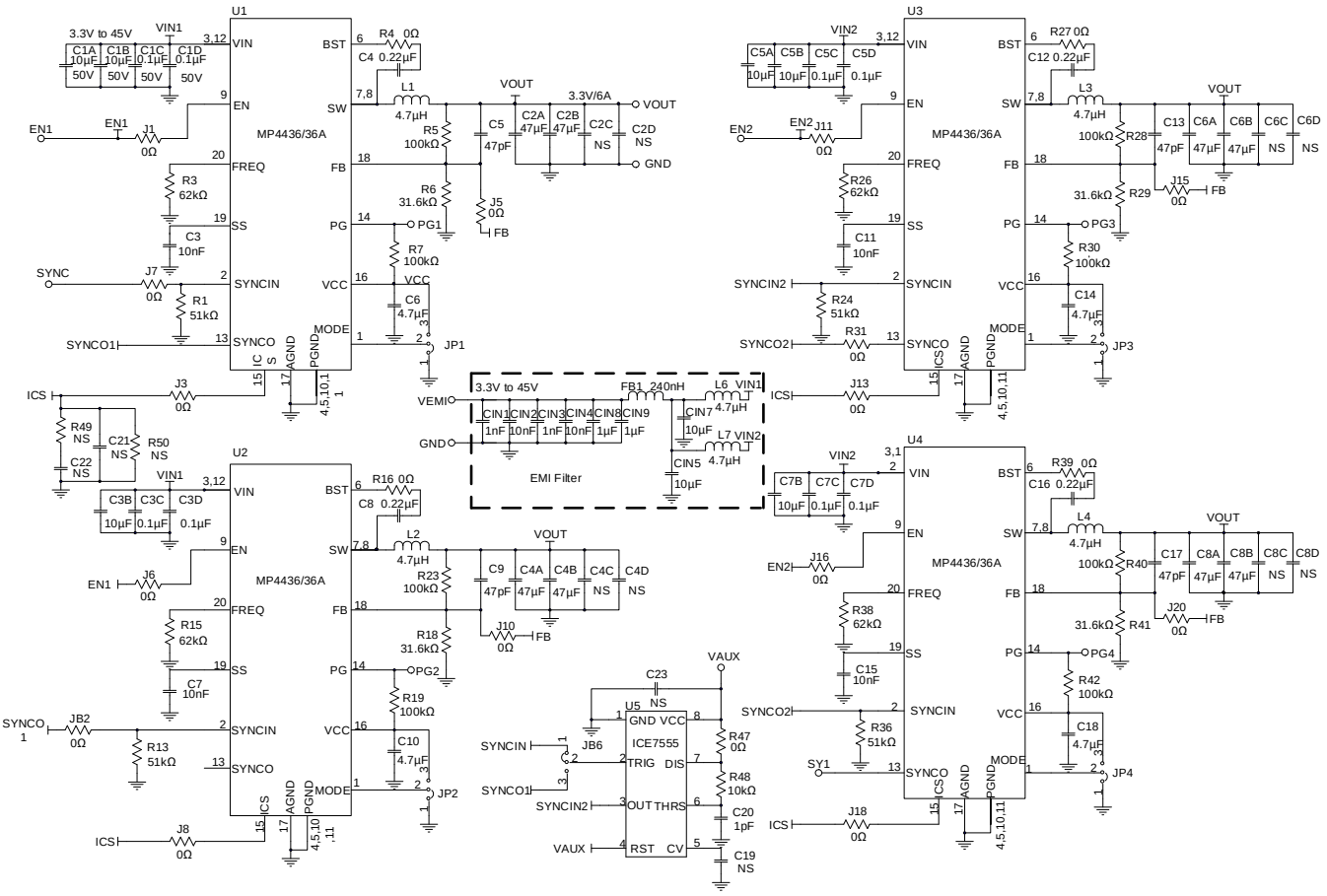
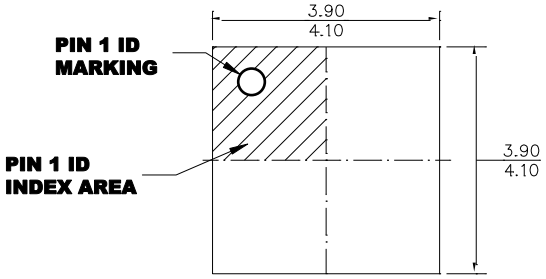


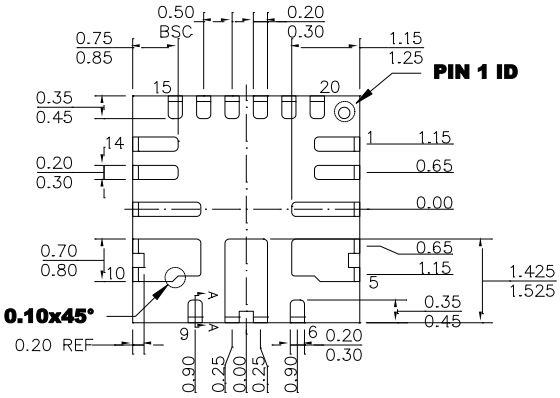
Figure 15: Four-Phase, V_{OUT} = 3.3V, f_{SW} = 470kHz

PACKAGE INFORMATION

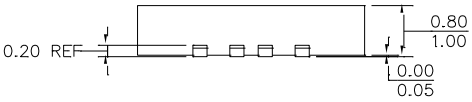
QFN-20 (4mmx4mm)
Wettable Flank



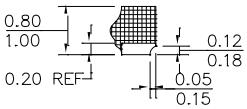
TOP VIEW



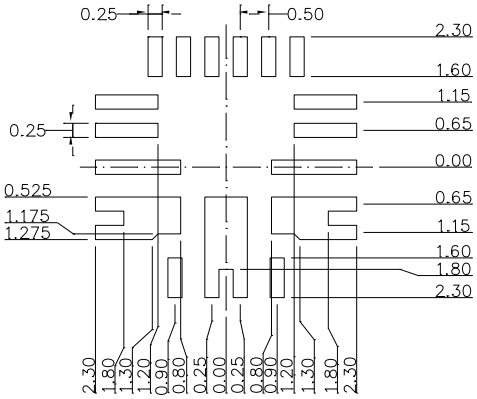
BOTTOM VIEW



SIDE VIEW



SECTION A-A

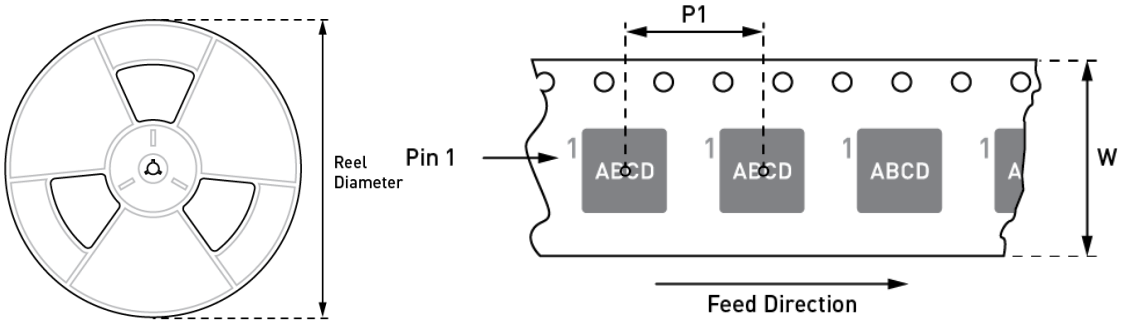


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube*	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4436GRE-Z	QFN-20 (4mmx4mm)	5000	N/A	13in	12mm	-8mm
MPQ4436GRE-AEC1-Z						
MPQ4436AGRE-Z						
MPQ4436AGRE-AEC1-Z						