MPQ4488B

36V, 6A, Step-Down Converter with Programmable Frequency, Spread Spectrum Dual USB Charging Ports, AEC-Q100 Qualified

DESCRIPTION

The MPQ4488B integrates a monolithic, step-down, switch-mode converter with two USB current-limit switches and charging port identification circuitry for each port. The MPQ4488B achieves 6A of output current, with excellent load and line regulation over a wide input supply range.

The output of each USB switch is current-limited. Both USB ports support DCP schemes for battery charging specification (BC1.2), Apple 3A Divider mode, 1.2V/1.2V mode, and USB Type-C 5V @ 3A DFP mode, eliminating the need for outside user interaction.

Full protection features include hiccup current limiting, output over-voltage protection (OVP), and thermal shutdown.

The MPQ4488B requires a minimal number of readily available, standard external components, and is available in a QFN-26 (5mmx5mm) package.

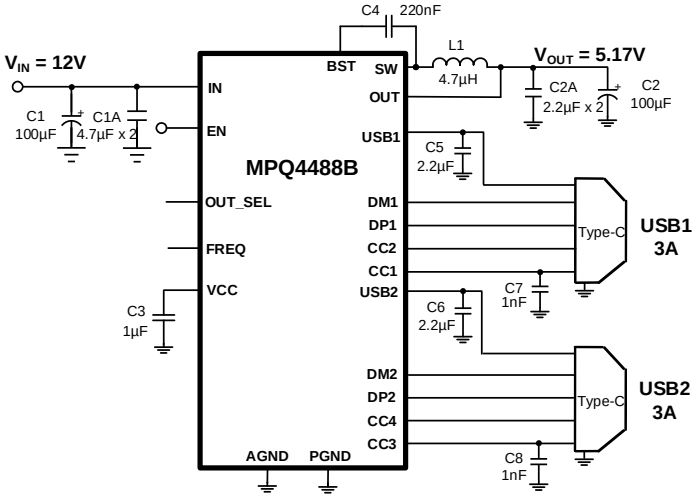
FEATURES

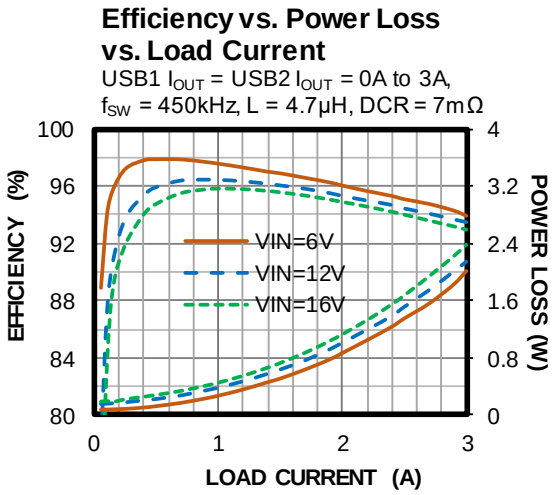
- Wide 6V to 36V Operating Input Voltage Range
- Passes Apple MFI R33 Certification Test
- Passes USB-IF Type-C Certification Test, TID: 3133
- +135°C Load-Shedding Entry Temperature
- Supports DCP Schemes for BC1.2, Apple 3A Divider Mode, and 1.2V/1.2V Mode
- Selectable 5.1V, 5.17V, or 5.3V Output Voltage
- 100mV Line Drop Compensation
- Accurate USB1/USB2 Output Current Limit
- 18mΩ/15mΩ Low $R_{DS(ON)}$ Internal Buck Power MOSFETs
- 18mΩ/18mΩ Low $R_{DS(ON)}$ Internal USB1/USB2 Power MOSFETs
- Adjustable 250kHz to 2.2MHz Frequency
- Frequency Spread Spectrum for MPQ4488BGU-FD-AEC1 Version
- Forced Continuous Conduction Mode (FCCM)
- Hiccup Current Limiting for both Buck and USB
- Supports USB Type-C 5V @ 3A DFP Mode
- Available in a QFN-26 (5mmx5mm) Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- USB Dedicated Charging Ports (DCPs)
- USB Type-C Charging Ports

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ4488BGU-AEC1	QFN-26 (5mmx5mm)	*See Below*	1
MPQ4488BGU-FD-AEC1			

* For Tape & Reel, add suffix –Z (e.g. MPQ4488BGU-AEC1–Z; MPQ4488BGU-FD-AEC1–Z).

DEVICE COMPARISON INFORMATION

Part Number	Frequency Spread Spectrum
MPQ4488BGU-AEC1	No
MPQ4488BGU-FD-AEC1	Yes

TOP MARKING (MPQ4488BGU-AEC1)

MPSYYWW
MP4488B
LLLLLLL

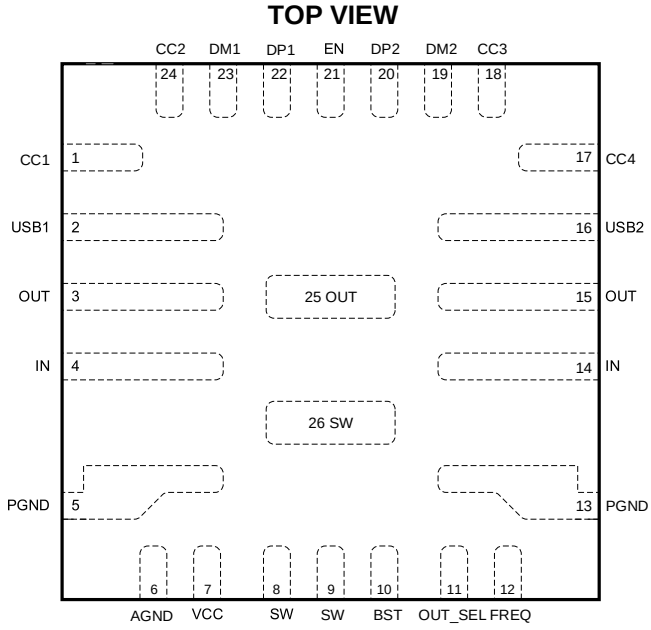
MPS: MPS prefix
YY: Year code
WW: Week code
MP4488B: Part number
LLLLLLL: Lot number

TOP MARKING (MPQ4488BGU-FD-AEC1)

MPSYYWW
MP4488B
LLLLLLL
FD

MPS: MPS prefix
YY: Year code
WW: Week code
MP4488B: Part number
LLLLLLL: Lot number
FD: Part number suffix

PACKAGE REFERENCE



QFN-26 (5mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
1	CC1	**Configuration channel.** CC1 is used to detect connections and configure the interface across the USB1 Type-C cables and connectors. Once a connection is established, CC1 or CC2 is reassigned to provide power across the VCONN of the plug.
2	USB1	**USB1 output.**
3, 15, 25	OUT	**Buck output.** OUT is the input for USB1 and USB2.
4, 14	IN	**Supply voltage.** IN is the drain of the internal power device, and provides the power supply for the entire chip. The MPQ4488B operates from a 6V to 36V input voltage. A capacitor (C_{IN}) prevents large voltage spikes at the input. Place C_{IN} as close to the IC as possible.
5, 13	PGND	**Power ground.** PGND is the reference ground of the regulated output voltage. PGND requires careful consideration during PCB layout. Connect PGND with copper traces and vias.
6	AGND	**Analog ground.** Connect AGND to PGND.
7	VCC	**Internal 4.6V LDO regulator output.** Decouple VCC with a 1µF capacitor.
8, 9, 26	SW	**Switch output.** Use a wide PCB trace to make the connection between the SW pins and the inductor.
10	BST	**Bootstrap.** Connect a 0.22µF capacitor between SW and BST to form a floating supply across the high-side switch driver.
11	OUT_SEL	**Buck output voltage set.** Pull OUT_SEL low, float it, or pull it low to set the output voltage to 5.1V, 5.17V, or 5.3V, respectively.
12	FREQ	**Switching frequency program input.** Connect a resistor between FREQ and GND to set the switching frequency. Float FREQ or connect FREQ to VCC for the default 450kHz frequency. Connect FREQ to ground for a 250kHz internal frequency. For the MPQ4488BGU-FD-AEC1, float FREQ or connect FREQ to VCC to achieve a ±10% frequency spread spectrum based on 420kHz. Connect a resistor between FREQ and GND or pull FREQ to GND to set the switching frequency without frequency spread spectrum.
16	USB2	**USB2 output.**
17	CC4	**Configuration channel.** CC4 is used to detect connections and configure the interface across the USB2 Type-C cables and connectors. Once a connection is established, CC3 or CC4 is reassigned to provide power across the VCONN pin of the plug.
18	CC3	**Configuration channel.** CC3 is used to detect connections and configure the interface across the USB2 Type-C cables and connectors. Once a connection is established, CC3 or CC4 is reassigned to provide power across the VCONN pin of the plug.
19	DM2	**D- data line to USB2 connector.** This input/output is used for handshaking with portable devices.
20	DP2	**D+ data line to USB2 connector.** This input/output is used for handshaking with portable devices.
21	EN	**On/off control input.** An internal 8µA pull-up current source pulls up EN automatically. Do not add a capacitor above 1nF on the EN pin.
22	DP1	**D+ data line to USB1 connector.** This input/output is used for handshaking with portable devices.
23	DM1	**D- data line to USB1 connector.** This input/output is used for handshaking with portable devices.
24	CC2	**Configuration channel.** CC2 is used to detect connections and configure the interface across the USB1 Type-C cables and connectors. Once a connection is established, CC1 or CC2 is reassigned to provide power across the VCONN pin of the plug.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.4V to +40V
V_{SW}.....-0.3V (-5V for <10ns) to V_{IN} + 0.3V (43V for <10ns)
V_{BST} ..... V_{SW} + 5.5V
V_{EN}.....-0.3V to +10V (2)
V_{OUT}, V_{USB}.....-0.3V to +6.5V
All other pins .....-0.3V to +5.5V
Continuous power dissipation (T_A = +25°C) (3) (8)
QFN-26 (5mmx5mm)..... 6.25W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings (4)

CC1/CC2/CC3/CC4 (HBM) (5)..... ±7kV
DP1/DP2/DM1/DM2/USB1/USB2 (HBM) (5) .... ±8kV
All other pins (HBM)..... ±1.8kV
All pins (CDM) ..... ±1kV

Recommended Operating Conditions (6)

Operation input voltage range .....6V to 36V
Output current.....3A for USB1, 3A for USB2
Operating junction temp (T_J)..... ..... -40°C to +125°C (7)

Thermal Resistance θ_{JA} θ_{JC}

QFN-26 (5mmx5mm)

EVQ4488B-U-00A (8)	20	2	°C/W
JESD51-7 (9)	44	9	°C/W

Notes:

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) For details on EN's ABS Max rating, see the Enable (EN) Control section on page 16.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101, AEC specification AEC-Q100-011. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
5) HBM with regard to GND.
6) The device is not guaranteed to function outside of its operating conditions.
7) Operating devices at junction temperature greater than 125°C is possible; contact MPS for details.
8) Measured on 4-layer, 50mmx50mm PCB.
9) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, CC1 to ground with a 5.1kΩ resistor, CC3 to ground with a 5.1kΩ resistor, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		13	18	μA
Supply current (quiescent)	I_{Q1}	Type-C attached, V_{OUT} = 5.4V, buck not switching		1	2	mA
	I_{Q2}	Type-C unattached, buck not switching, T_J = 25°C		200	300	μA
EN rising threshold	V_{EN_RISING}		-3%	1.235	+3%	V
EN hysteresis	V_{EN_HYS}			230		mV
EN pull-up current	I_{EN}		4	8	12	μA
Thermal shutdown (10)	T_{TSD}			165		°C
Thermal hysteresis (10)	T_{TSD_HYS}			20		°C
VCC regulator	V_{CC}		4.3	4.6	4.9	V
VCC load regulation	V_{CC_LOG}	I_{CC} = 50mA		1	3	%
Step-Down Converter						
V_{IN} under-voltage lockout (ULVO) rising threshold	V_{IN_UVLO}		4.6	5.0	5.4	V
V_{IN} ULVO threshold hysteresis	V_{UVLO_HYS}			800		mV
HS-FET on resistance	$R_{DS(ON)\_HS}$			18	40	mΩ
LS-FET on resistance	$R_{DS(ON)\_LS}$			15	30	mΩ
Output voltage	V_{OUT}	OUT_SEL = low	-2%	5.10	+2%	V
		OUT_SEL = floating, T_J = 25°C	-1%	5.17	+1%	
		OUT_SEL = floating, T_J = -40°C to 125°C	-2%	5.17	+2%	
		OUT_SEL = high	-2%	5.30	+2%	
Output over-voltage protection (OVP)	V_{OVP_R}		5.45	5.85	6.25	V
Output OVP recovery	V_{OVP_F}		5.3	5.7	6.1	V
Output-to-ground resistance	R_{FB}	EN = 0V, T_J = 25°C	100	160	220	kΩ
Low-side current limit	I_{LS_LIMIT}			-2		A
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 36V,T_J = 25°C			1	μA
		V_{EN} = 0V, V_{SW} = 36V, T_J = -40°C to +125°C			5	
High-side current limit	I_{LIMIT}	V_{OUT} = 0V	8	12	16	A
Oscillator frequency	f_{SW1}	Pull R_{FREQ} to GND	185	250	315	kHz
	f_{SW2}	R_{FREQ} = 66.5kΩ	250	350	450	
	f_{SW3}	R_{FREQ} = 9.53kΩ	1800	2200	2600	
	f_{SW4}	R_{FREQ} = floating	360	450	540	
Frequency spread spectrum span (only for the MPQ4488BGU-FD-AEC1)	f_{SS}	R_{FREQ} = floating, based on 420kHz		±10		%

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, CC1 to ground with a 5.1kΩ resistor, CC3 to ground with a 5.1kΩ resistor, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Maximum duty cycle	D_{MAX}	FREQ = 450kHz	91	95	99	%
Minimum off time	t_{OFF_MIN}			110		ns
Minimum on time (10)	t_{ON_MIN}			130		ns
Soft-start time	t_{SS}	Output from 10% to 90%	1	2	3.4	ms
USB Switch (USB1 and USB2)						
UVLO rising threshold	V_{USB_UVR}		3.7	4	4.3	V
UVLO threshold hysteresis	V_{USB_UVHYS}			200		mV
Switch on resistance	R_{DSON_SW}			18	35	mΩ
Output impedance	R_{DIS_USB}	Apply 5V voltage on USB output, CC floating	350	600	850	kΩ
USB OVP clamp	V_{USB_OV}		5.3	5.6	6.0	V
Current limit	I_{LIMIT1}	V_{OUT} drops 10%, Type-C/A mode, T_J = 25°C	-6%	3.55	+6%	A
Line drop compensation	V_{DROP_COM}	I_{OUT} = 3A, V_{OUT} = 5.17V	50	100	150	mV
V_{BUS} soft-start time	t_{SS_VBUS}	Output from 10% to 90%	1	2	3	ms
V_{BUS} OC hiccup on time	t_{HICP_ON}	OC, Hiccup on time, T_J = +25°C		3		ms
Hiccup mode off time	t_{HICP_OFF}	V_{OUT} connected to GND	1	2	3	sec
BC1.2 DCP Mode						
DP and DM short resistance	R_{DP/DM_SHORT}	V_{DP} = 0.8V, I_{DM} = 1mA, T_J = 25°C		85	155	Ω
		V_{DP} = 0.8V, I_{DM} = 1mA, T_J = -40°C to +125°C		85	160	
Divider Mode						
DP output voltage	$V_{DP\_DIVIDER}$		2.55	2.7	2.85	V
DP output impedance	$R_{DP\_DIVIDER}$	T_J = 25°C	14	22	30	kΩ
		T_J = -40°C to +125°C	12	22	34	
DM output voltage	$V_{DM\_DIVIDER}$		3	3.3	3.6	V
DM output impedance	$R_{DM\_DIVIDER}$	T_J = 25°C	10	18	26	kΩ
		T_J = -40°C to +125°C	8	18	30	
1.2V/1.2V Mode						
DP/DM output voltage	$V_{DP/DM\_1.2V}$	V_{OUT} = 5V, T_J = 25°C	1.12	1.2	1.28	V
		V_{OUT} = 5V, T_J = -40°C to +125°C	1.1	1.2	1.3	
DP/DM output impedance	$R_{DP/DM\_1.2V}$	T_J = 25°C	70	105	140	kΩ
		T_J = -40°C to +125°C	60	105	150	

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, CC1 to ground with a 5.1kΩ resistor, CC3 to ground with a 5.1kΩ resistor, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
USB Type-C 5V @ 3A Mode – CC1, CC2, CC3 and CC4						
CC resistor to disable Type-C mode	R_A	CC1 and CC3 pins. For Type-C mode application, a 1nF capacitor should be added on both CC1 and CC3	90		96	kΩ
CC voltage to enable VCONN	V_{RA}				0.75	V
CC voltage to enable V_{BUS}	V_{RD}		0.9		2.45	V
CC detach threshold	V_{OPEN}		2.75			V
CC voltage falling debounce timer	$T_{CC\_DEBOUNCE}$	V_{BUS} enable deglitch	100	144	200	ms
CC voltage rising debounce timer	$T_{PD\_DEBOUNCE}$	V_{BUS} disable deglitch	10	15	20	ms
VCONN output power	P_{VCONN}	VCONN comes from buck output with some series resistance, T_J = 25°C	1			W

Note:

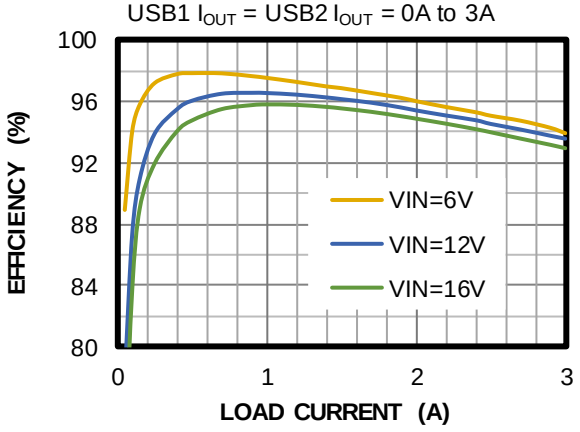
10) Guaranteed by characterization testing.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5.17V, L = 4.7µH, CC1 to ground with a 5.1kΩ resistor, CC3 to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

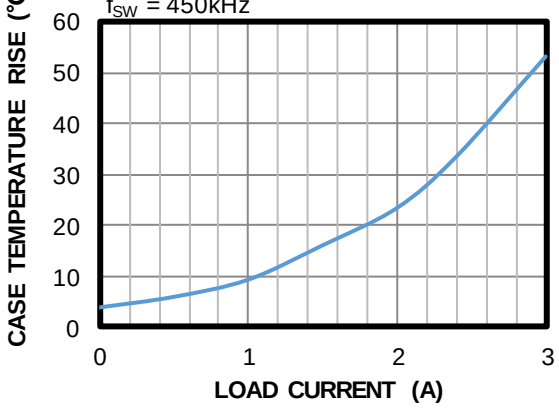
Efficiency vs. Load Current

USB1 I_{OUT} = USB2 I_{OUT} = 0A to 3A

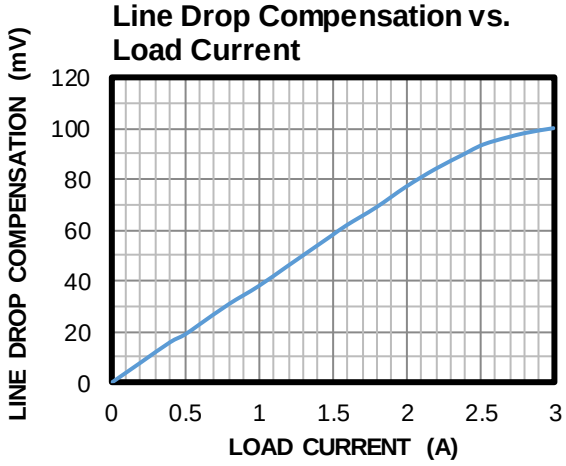


Case Temperature Rise vs. Load Current

USB1 I_{OUT} = USB2 I_{OUT} = 0A to 3A, f_{SW} = 450kHz

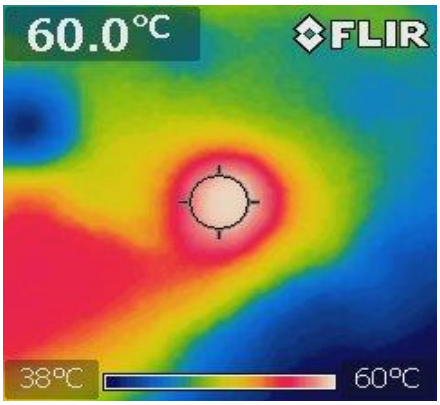


Line Drop Compensation vs. Load Current



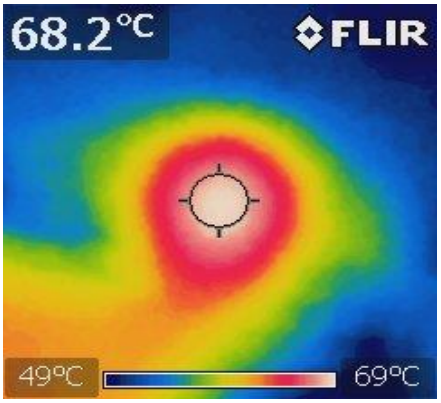
Thermal Imaging

V_{IN} = 12V, V_{OUT} = 5.17V, T_A = 25°C, USB1_I_{OUT} = USB2_I_{OUT} = 2.4A



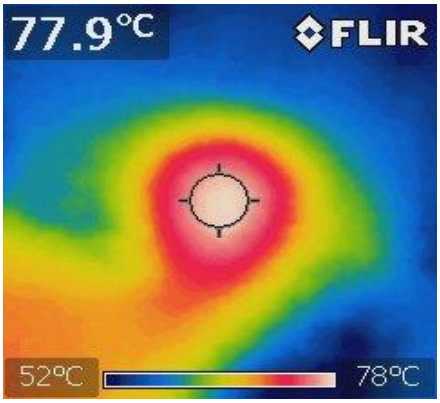
Thermal Imaging

V_{IN} = 12V, V_{OUT} = 5.17V, T_A = 25°C, USB1 I_{OUT} = 2.4A, USB2 I_{OUT} = 3A



Thermal Imaging

V_{IN} = 12V, V_{OUT} = 5.17V, T_A = 25°C, USB1 I_{OUT} = USB2 I_{OUT} = 3A



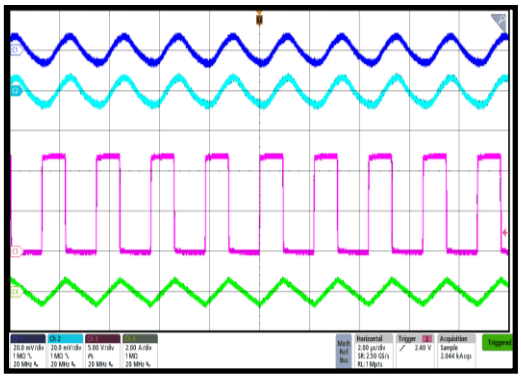
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5.17V, L = 4.7µH, CC1 to ground with a 5.1kΩ resistor, CC3 to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

Steady State

USB1 I_{OUT} = USB2 I_{OUT} = 0A

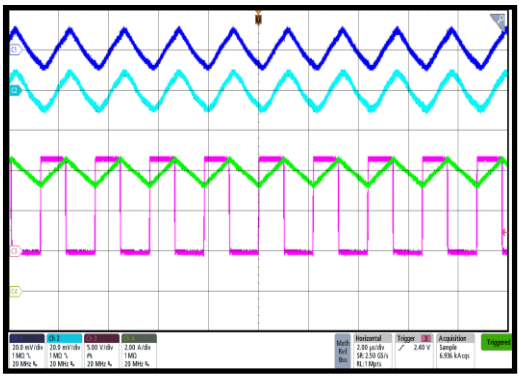
CH1: USB1/AC 20mV/div.
CH2: USB2/AC 20mV/div.
CH3: SW 5V/div.
CH4: I_L 2A/div



Steady State

USB1 I_{OUT} = USB2 I_{OUT} = 3A

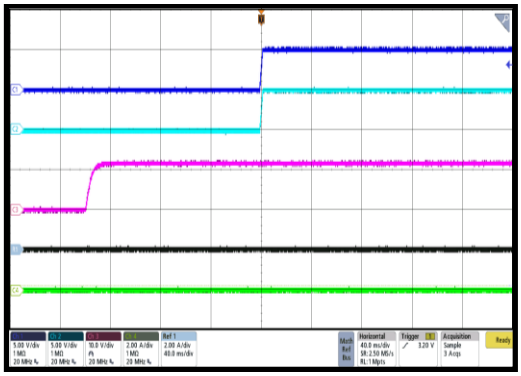
CH1: USB1/AC 20mV/div.
CH2: USB2/AC 20mV/div.
CH3: SW 5V/div.
CH4: I_L 2A/div.



Start-Up

USB1 I_{OUT} = USB2 I_{OUT} = 0A

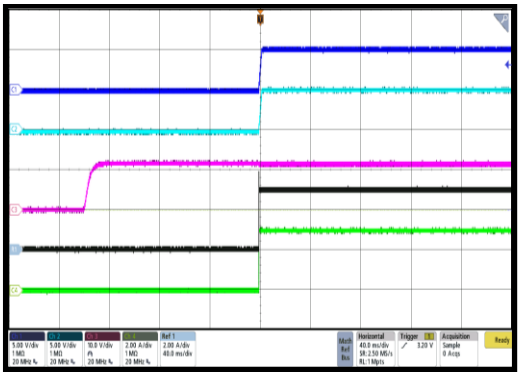
CH1: USB1 5V/div.
CH2: USB2 5V/div.
CH3: V_{IN} 10V/div.
R1: REF1
USB1 I_{OUT} 2A/div.
CH4: USB2 I_{OUT} 2A/div.



Start-Up

USB1 I_{OUT} = USB2 I_{OUT} = 3A

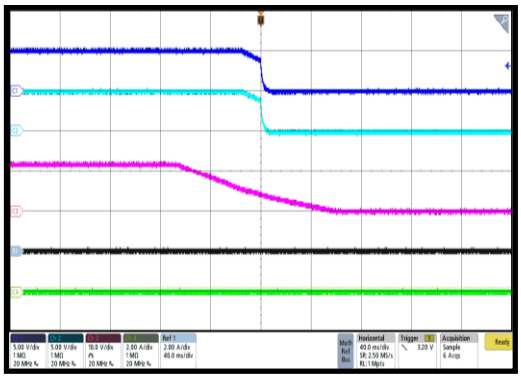
CH1: USB1 5V/div.
CH2: USB2 5V/div.
CH3: V_{IN} 10V/div.
R1: REF1
USB1 I_{OUT} 2A/div.
CH4: USB2 I_{OUT} 2A/div.



Shutdown

USB1 I_{OUT} = USB2 I_{OUT} = 0A

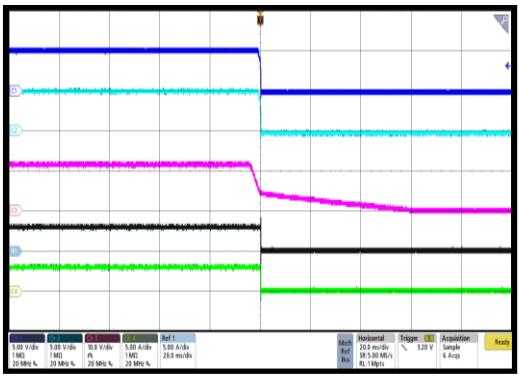
CH1: USB1 5V/div.
CH2: USB2 5V/div.
CH3: V_{IN} 10V/div.
R1: REF1
USB1 I_{OUT} 2A/div.
CH4: USB2 I_{OUT} 2A/div.



Shutdown

USB1 I_{OUT} = USB2 I_{OUT} = 3A

CH1: USB1 5V/div.
CH2: USB2 5V/div.
CH3: V_{IN} 10V/div.
R1: REF1
USB1 I_{OUT} 5A/div.
CH4: USB2 I_{OUT} 5A/div.



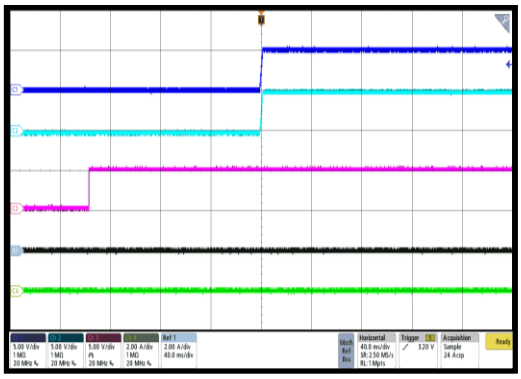
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5.17V, L = 4.7µH, CC1 to ground with a 5.1kΩ resistor, CC3 to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

Start-Up through EN

USB1 I_{OUT} = USB2 I_{OUT} = 0A

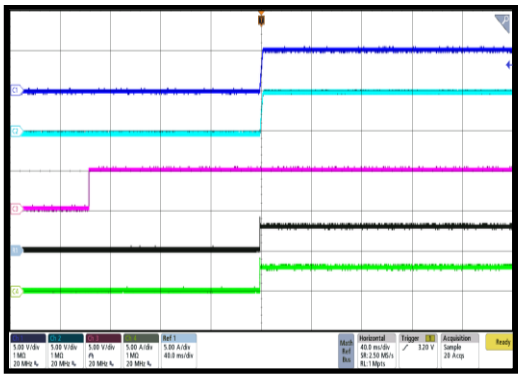
CH1: USB1 5V/div.
CH2: USB2 5V/div.
CH3: V_{EN} 5V/div.
R1: REF1
USB1 I_{OUT} 2A/div.
CH4: USB2 I_{OUT} 2A/div.



Start-Up through EN

USB1 I_{OUT} = USB2 I_{OUT} = 3A

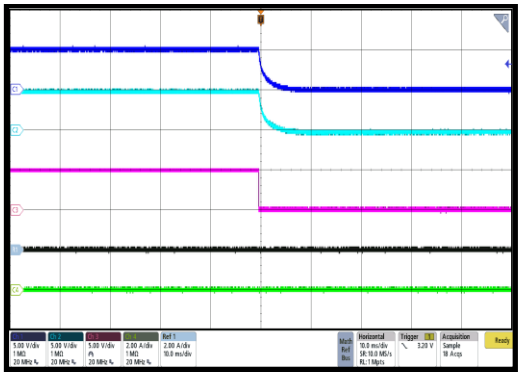
CH1: USB1 5V/div.
CH2: USB2 5V/div.
CH3: V_{EN} 5V/div.
R1: REF1
USB1 I_{OUT} 5A/div.
CH4: USB2 I_{OUT} 5A/div.



Shutdown through EN

USB1 I_{OUT} = USB2 I_{OUT} = 0A

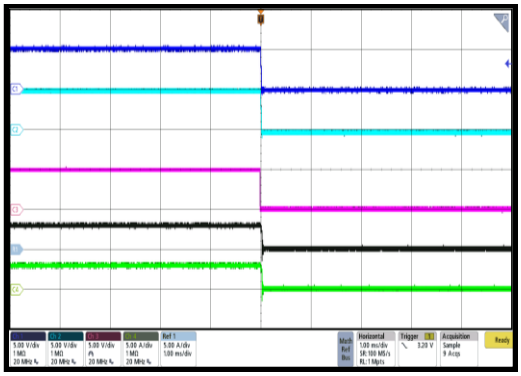
CH1: USB1 5V/div.
CH2: USB2 5V/div.
CH3: V_{EN} 5V/div.
R1: REF1
USB1 I_{OUT} 2A/div.
CH4: USB2 I_{OUT} 2A/div.



Shutdown through EN

USB1 I_{OUT} = USB2 I_{OUT} = 3A

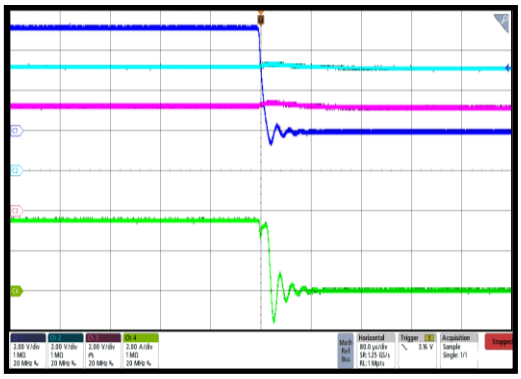
CH1: USB1 5V/div.
CH2: USB2 5V/div.
CH3: V_{EN} 5V/div.
R1: REF1
USB1 I_{OUT} 5A/div.
CH4: USB2 I_{OUT} 5A/div.



USB1 Over-Current Protection

Ramp up load current slowly

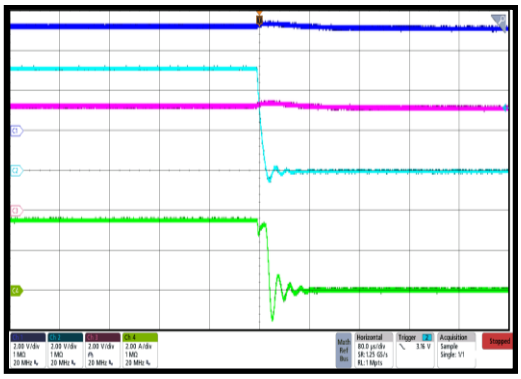
CH1: USB1 2V/div.
CH2: USB2 2V/div.
CH3: Buck V_{OUT} 2V/div.
CH4: USB1 I_{OUT} 2A/div.



USB2 Over-Current Protection

Ramp up load current slowly

CH1: USB1 2V/div.
CH2: USB2 2V/div.
CH3: Buck V_{OUT} 2V/div.
CH4: USB1 I_{OUT} 2A/div.



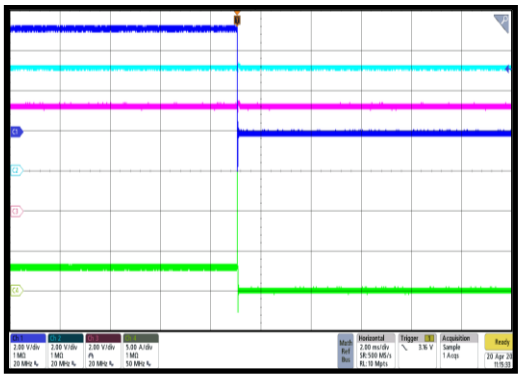
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5.17V, L = 4.7µH, CC1 to ground with a 5.1kΩ resistor, CC3 to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

USB1 SCP Entry

USB1 I_{OUT} = USB2 I_{OUT} = 3A

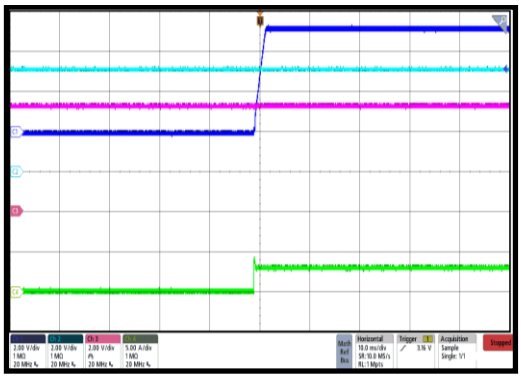
CH1: USB1 2V/div.
CH2: USB2 2V/div.
CH3: Buck V_{OUT} 2V/div.
CH4: USB1 I_{OUT} 5A/div.



USB1 SCP Recovery

USB1 I_{OUT} = USB2 I_{OUT} = 3A

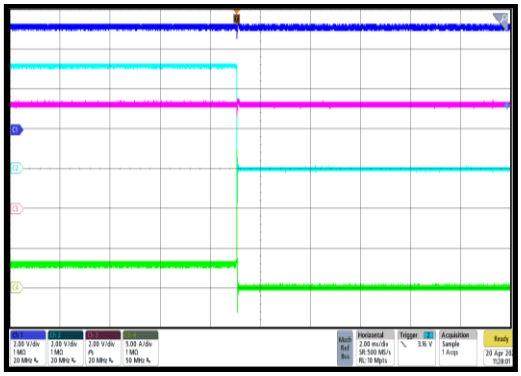
CH1: USB1 2V/div.
CH2: USB2 2V/div.
CH3: Buck V_{OUT} 2V/div.
CH4: USB1 I_{OUT} 5A/div.



USB2 SCP Entry

USB1 I_{OUT} = USB2 I_{OUT} = 3A

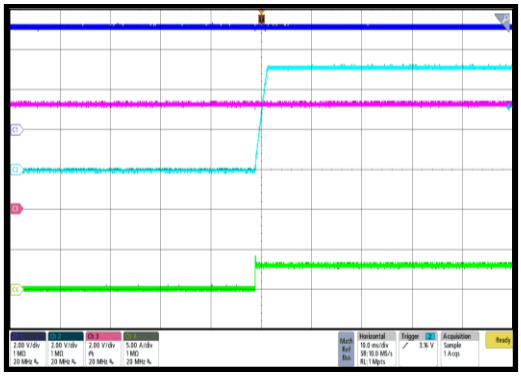
CH1: USB1 2V/div.
CH2: USB2 2V/div.
CH3: Buck V_{OUT} 2V/div.
CH4: USB1 I_{OUT} 5A/div.



USB2 SCP Recovery

USB1 I_{OUT} = USB2 I_{OUT} = 3A

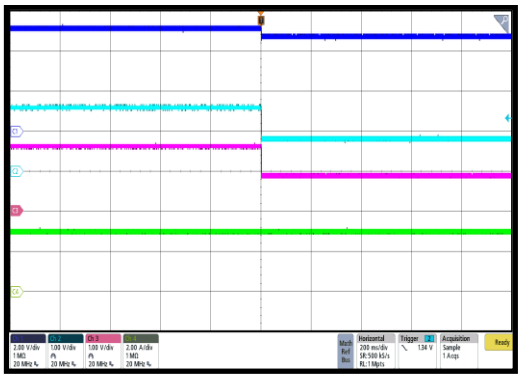
CH1: USB1 2V/div.
CH2: USB2 2V/div.
CH3: Buck V_{OUT} 2V/div.
CH4: USB1 I_{OUT} 5A/div.



Load-Shedding Entry

USB1 I_{OUT} = USB2 I_{OUT} = 3A

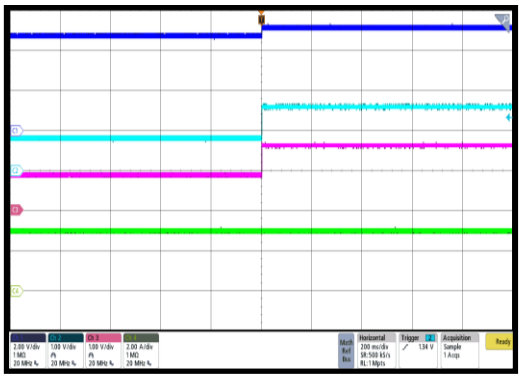
CH1: USB1 2V/div.
CH2: CC1 1V/div.
CH3: CC3 1V/div.
CH4: USB1 I_{OUT} 2A/div.



Load-Shedding Recovery

USB1 I_{OUT} = USB2 I_{OUT} = 3A

CH1: USB1 2V/div.
CH2: CC1 1V/div.
CH3: CC3 1V/div.
CH4: USB1 I_{OUT} 2A/div.

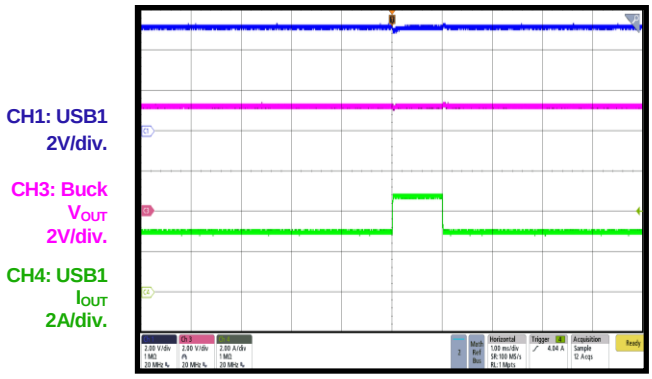


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5.17V, L = 4.7µH, CC1 to ground with a 5.1kΩ resistor, CC3 to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

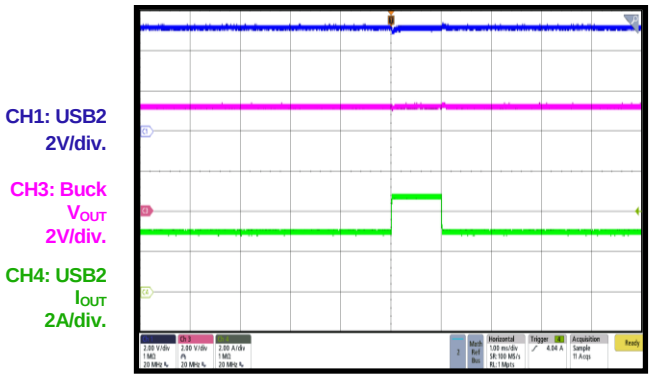
USB1 Load Transient

I_{OUT} = 3A to 4.8A, 1ms hold time



USB2 Load Transient

I_{OUT} = 3A to 4.8A, 1ms hold time



FUNCTIONAL BLOCK DIAGRAM

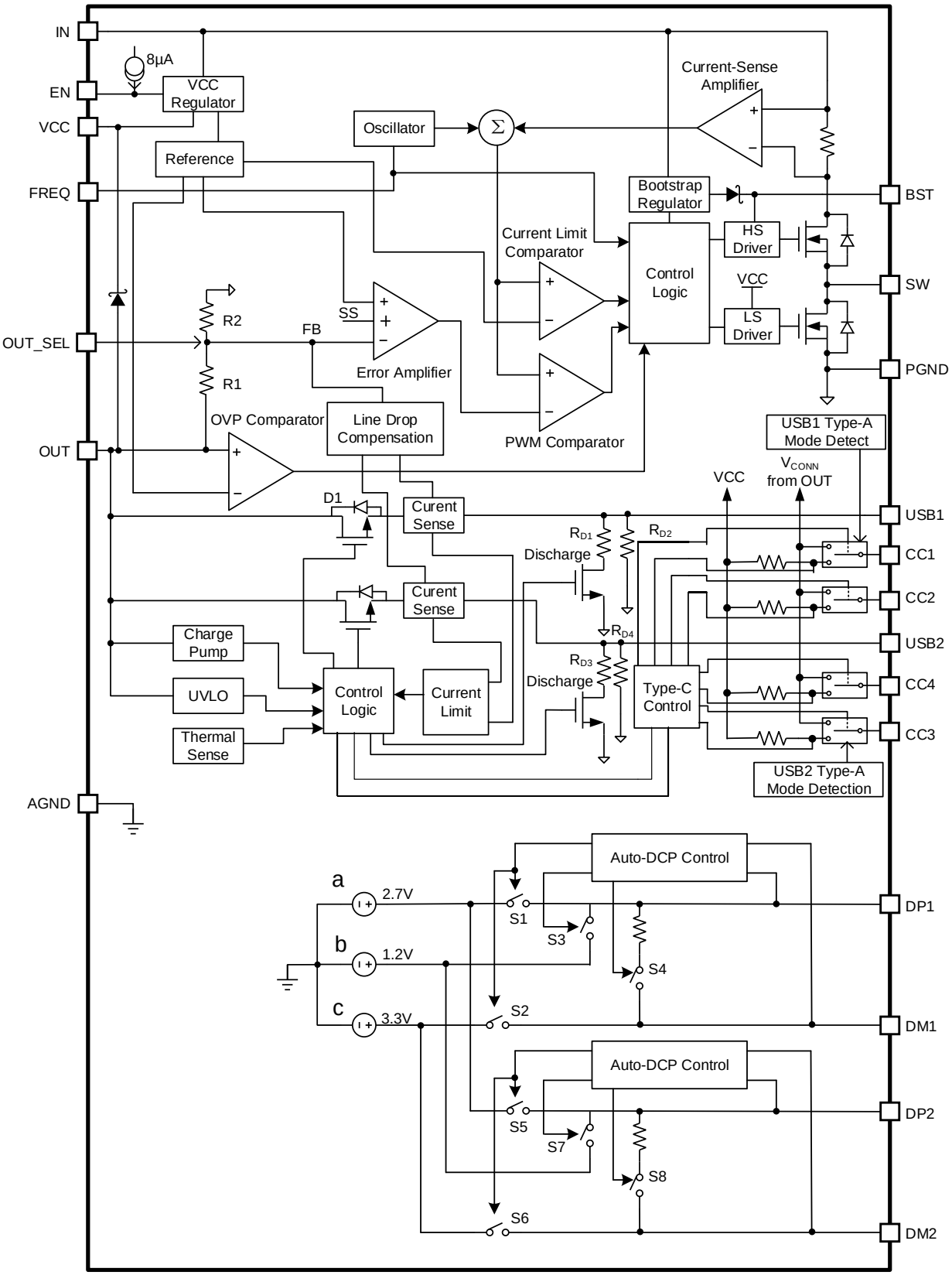


Figure 1: Functional Block Diagram

OPERATION

BUCK CONVERTER

The MPQ4488B integrates a monolithic, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs and two USB current-limit switches that feature charging port auto-detection. The MPQ4488B offers a compact solution that achieves 6A of continuous output current, with excellent load and line regulation over a wide input supply range.

The MPQ4488B operates in a fixed-frequency, peak current mode control to regulate the output voltage. The internal clock initiates the pulse-width modulation (PWM) cycle, which turns on the integrated high-side power MOSFET (HS-FET). The HS-FET remains on until its current reaches the value set by the COMP voltage (V_{COMP}). When the MOSFET is off, it remains off until the next clock cycle begins. If the duty cycle reaches 95% (450kHz switching frequency) within one PWM period, then the MOSFET current does not reach the COMP-set current value and the MOSFET turns off.

Error Amplifier (EA)

The error amplifier (EA) compares the internal feedback voltage (V_{FB}) against the internal reference voltage (V_{REF}) and outputs V_{COMP}. V_{COMP} controls the power MOSFET current. The optimized, internal compensation network minimizes the external component count and simplifies control loop design.

Internal VCC Regulator

The 4.6V internal regulator powers most of the internal circuitries. This regulator takes V_{IN} and operates in the full V_{IN} range. If V_{IN} exceeds 4.6V, the output of the regulator is in full regulation. If V_{IN} drops below 4.6V, the output decreases with V_{IN}. VCC requires an external 1µF ceramic decoupling capacitor.

After the buck output start-up, the internal VCC LDO output is biased by the buck output through a Schottky diode.

Enable (EN) Control

The MPQ4488B has an enable (EN) control pin. There is an internal 8µA pull-up current that allows EN to be floated for automatic start-up. Pull EN high or float it to enables the IC; pulling EN low to disable the IC.

EN is clamped internally using a 7.6V series Zener diode and 10V ESD cell breakdown voltage (see Figure 2).

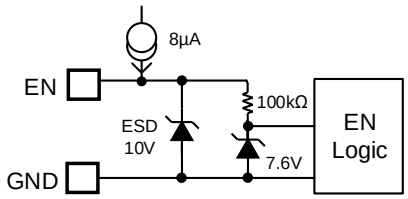


Figure 2: Zener Diode between EN and GND

It is recommended to connect EN to VIN and GND through resistor dividers. When selecting a pull-up resistor, ensure that it has enough resistance to limit the current flowing into the EN to below 100µA. For example, if the EN pull-up resistor is 100kΩ and the pull-down resistor is 34kΩ, then IC starts up when V_{IN} exceeds the under-voltage lockout (UVLO) rising threshold, and shuts down when V_{IN} falls below the UVLO falling threshold.

Do not add a capacitor greater than 1nF on the EN pin.

Setting the Switching Frequency

Connect a frequency-programmable resistor (R_{FREQ}) from FREQ to ground to set the switching frequency (see Table 1).

Table 1: Recommended Resistor Values for Typical Switching Frequencies

R_{FREQ} (kΩ)	f_{SW} (kHz)
0	250
66.5	350
NC	450
45.8	500
22.3	1000
14.6	1500
9.53	2200

The frequency value can be estimated with Equation (1):

$$FREQ(kHz) = \frac{1000000}{42.5 \times R_{FREQ}(k\Omega) + 53.7} \quad (1)$$

Figure 3 shows the relationship between frequency and R_{FREQ}.

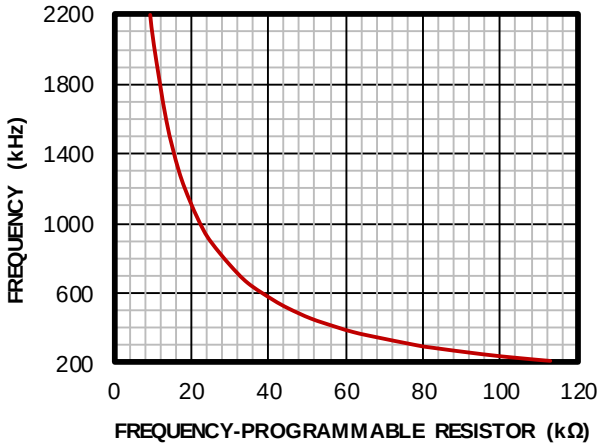


Figure 3: Switching Frequency vs. R_{FREQ}

When running the part at a high switching frequency (e.g. 2.2MHz), it is important to consider the minimum on time, minimum off time, and the thermal rise.

Two internal comparators monitor the FREQ pin's logic voltage to enable FREQ to float or short to GND. During start-up, there is another internal source current on FREQ. If a voltage above 2V is sensed on FREQ for longer than 8µs, then the frequency is locked at 450kHz. If a voltage below 0.1V is sensed on FREQ for longer than 8µs, then the frequency is locked at 250kHz. Leave FREQ floating or connect FREQ to VCC to set the switching frequency to 450kHz (default). Short FREQ to ground to set the switching frequency to 250kHz (see Figure 4).

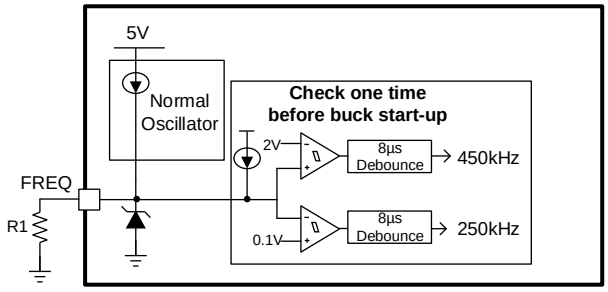


Figure 4: Switching Frequency Functional Block

Frequency Spread Spectrum

The purpose of spread spectrum is to minimize the peak emissions at a specific frequency.

The MPQ4488BGU-FD-AEC1 uses a 4kHz triangle wave (125µs rising, 125µs falling) to modulate the internal oscillator. The spread spectrum operation frequency span is ±10% (see Figure 5).

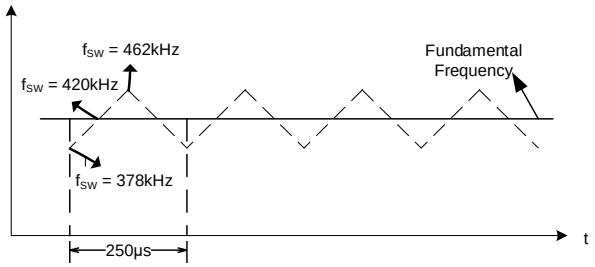


Figure 5: Frequency Spread Spectrum

FREQ must be floated or connected to VCC when using the spread spectrum function. The MPQ4488B can work without switching frequency spread spectrum when FREQ is connected to an external resistor or shorted to GND.

Pull FREQ to GND to set the fixed switching frequency at 250kHz without frequency spread spectrum. When connecting FREQ to GND through a resistor, the frequency is determined by an external resistor.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the input voltage. The UVLO rising threshold is 5V, and its falling threshold is 4.2V.

Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a SS voltage (V_{SS}) that ramps up from 0V to 5V. When V_{SS} is below V_{REF}, the EA uses V_{SS} as the reference. When V_{SS} is above V_{REF}, the EA uses V_{REF} as the reference. The SS time (t_{SS}) is set to 2ms internally. If the MPQ4488B's output is pre-biased to a certain voltage during start-up, the IC disables the switching of both the HS-FET and LS-FET until the voltage on the internal SS capacitor (C_{SS}) exceeds the internal V_{FB}.

Forced Continuous Conduction Mode (FCCM)

The MPQ4488B works in forced continuous conduction mode (FCCM). In this mode, it operates with a fixed switching frequency, regardless of whether it is operating under a light load or full load. The advantages of FCCM are the controllable frequency, smaller output ripple, and sufficient bootstrap charge time; however, it also has low efficiency under light-load

conditions. A proper inductance should be selected to avoid triggering the LS-FET's negative current limit (typically 2A, from SW to GND). If the negative current limit is triggered, the LS-FET turns off, and the HS-FET turns on when the internal clock starts.

Buck Over-Current Protection (OCP)

The MPQ4488B implements cycle-by-cycle over-current (OC) limiting when the inductor's peak current exceeds the current-limit threshold and V_{FB} drops below the under-voltage (UV) threshold (typically 50% below the reference). Once UV is triggered, the MPQ4488B enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground. This greatly reduces the average short-circuit current, alleviates thermal issues, and protects the regulator. Once the OC condition is removed, the MPQ4488B exits hiccup mode and resumes normal operation.

Buck Output Over-Voltage Protection (OVP)

The MPQ4488B has output over-voltage protection (OVP). If the output exceeds 5.85V, the HS-FET stops turning on. The LS-FET turns on to discharge the output voltage until the output decreases to 5.7V, and then the IC resumes normal operation.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver (PMOS). This floating driver has its own UVLO protection. The UVLO rising threshold is 2.2V, with a 150mV hysteresis. The bootstrap capacitor voltage is regulated internally by V_{IN} and VCC through D1, D2, M1, C4, L1, and C2 (see Figure 6).

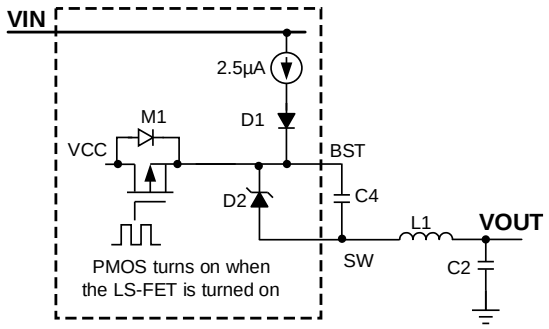


Figure 6: Internal Bootstrap Charging Circuit

The BST capacitor (C4) voltage is charged up quickly by VCC through M1 when the LS-FET switch is turned on. The 2.5μA input to the BST current source can also charge the BST capacitor when the LS-FET does not turn on.

Start-Up and Shutdown

If both IN and EN exceed their respective thresholds, the MPQ4488B is enabled. The reference block starts first, generating a stable reference voltage and current, then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, IN low, and thermal shutdown. During shutdown, the signaling path is blocked to avoid any fault triggering. Then V_{COMP} and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

Buck Output Impedance

The buck converter has a discharge path when it detects that EN is off or CC is unattached. The buck discharges until V_{OUT} < 1.4V, then the discharge path turns off. There are two feedback resistors connected to the OUT pin, which have a typical resistance of 160kΩ to discharge V_{OUT} slowly.

USB CURRENT-LIMIT SWITCH SECTION

Over-Current Protection (OCP) and Hiccup Mode

The MPQ4488B integrates two USB current-limit switches. The MPQ4488B provides built-in soft-start circuitry that controls the rising slew rate of the output voltage to limit inrush current and voltage surges.

During normal operation, the MPQ4488B starts a 2ms counter once the load current reaches the current-limit threshold. The MPQ4488B does not limit the output current within this 2ms period (see Figure 7).

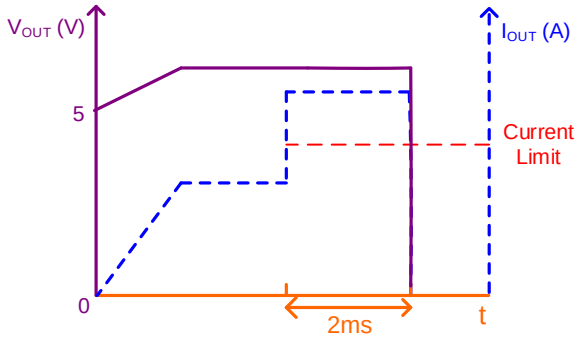


Figure 7: Over-Current Limit

If the 2ms timer is exceeded, the USB channel enters hiccup mode with 2ms of on time and 2s of off time. Other USB channels still work normally. The MPQ4488B resets the time counter if the OC signal disappears during the 2ms timer.

Fast Response for Short-Circuit Protection (SCP)

If the load current increases rapidly due to a short-circuit event, the current may exceed the current-limit threshold before the control loop is able to respond. If the current reaches the 10.5A secondary current limit level, a fast turn-off circuit is active to turn off the power MOSFET. This can help limit the peak current through the MOSFET, keeping the buck output voltage from dropping too much and affect another USB channel. The total short-circuit response time is less than 1µs.

When the fast turn-off function is triggered, the MOSFET turns off for 100µs and restarts with a soft start. During the restart process, if the short still remains, the MPQ4488B regulates the gate voltage to hold the current at a normal current limit level.

Output Line Drop Compensation

The MPQ4488B can compensate for an output-voltage drop, such as high impedance caused by a long trace, to maintain a fairly constant output voltage at the load-side voltage.

The internal comparator compares the current-sense output voltage of the two current-limit switches, and uses the larger current-sense output voltage to compensate for the line drop voltage.

The line drop compensation amplitude increases linearly as the load current increases. It also has an upper limitation. At output currents above 3A, the line drop compensation is 100mV.

USB Output Over-Voltage Clamp

To protect the device at the cable terminal, the USB switch output has a fixed over-voltage protection (OVP) threshold. When the input voltage exceeds the OVP threshold, the output voltage is clamped to its OVP threshold value.

USB Output Discharge and Impedance

Each USB switch has a fast discharge path that can discharge the external output capacitor's energy quickly during power shutdown. This function is active when the CC pins are released or the part is disabled (V_{IN} is below the UVLO threshold or EN is off). If the USB output voltage is discharged below 50mV, the discharge path turns off. After the fast discharge path turns off, there is only a high-impedance resistor (typically 600kΩ) from USB1 or USB2 to ground.

Auto-Detection

The MPQ4488B integrates a USB-dedicated charging port auto-detection function. This function recognizes most mainstream portable devices, and supports the following charging schemes:

- USB Battery Charging Specification BC1.2/ Chinese Telecommunications Industry Standard YD/T 1591-2009
- Apple 3A Divider mode
- 1.2V/1.2V mode
- USB Type-C 5V @ 3A DFP mode

The auto-detection function is a state machine that supports all of the DCP charging schemes listed above. The state machine starts in 3A Divider mode. If a BC1.2 device is attached, the MPQ4488B exits 3A Divider mode and enters BC1.2 short mode. 1.2V/1.2V mode turns on during the time window when the MPQ4488B enters BC1.2 short mode. If the downstream device releases the DP/DM line or is unplugged, the MPQ4488B goes back to 3A Divider mode.

Apple 3A Divider Mode

Apple devices (iPhone, iPod, and iPad) have a proprietary charger detection protocol to distinguish a charger from a standard USB device. A non-zero voltage (applied by the charger) on D+ and D- is used to indicate charger capability. The MPQ4488B applies different D+ and D- voltage and resistor value to meet Apple 3A Divider network specifications which are defined in Accessory Interface Specification R33.

USB Type-C Mode and VCONN

For USB Type-C solutions, two pins (CC1 and CC2) on the connector are used to establish and manage the source-to-sink connection. The general concept for setting up a valid connection between a source and a sink is based on being able to detect terminations residing in the product being attached. To aid in defining the

functional behavior of CC, a pull-up (R_P) and pull-down (R_D = 5.1kΩ) termination model is used based on a pull-up resistor and pull-down resistor (see Figure 8).

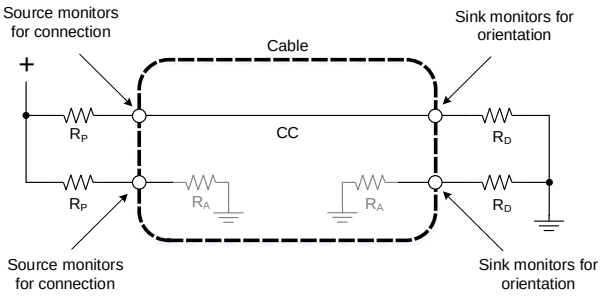


Figure 8: Current Source/Pull-Down CC Model

Initially, a source exposes independent R_P terminations on its CC1 and CC2 pins, and a sink exposes independent R_D terminations on its CC1 and CC2 pins. The source-to-sink combination of this circuit configuration represents a valid connection. To detect this, the source monitors CC1 and CC2 for a voltage below its unterminated voltage. The choice of R_P is a function of the pull-up termination voltage and the source's detection circuit. This indicates that either a sink, a powered cable, or a sink connected via a powered cable has been attached.

Prior to the application of VCONN, a powered cable exposes R_A (typically 1kΩ) on its VCONN pin. R_A represents the load on VCONN plus any resistive elements to ground. In some cable plugs, this might be a pure resistance, while in others, it may simply be the load.

The source must be able to differentiate between the presence of R_D and R_A to know whether there is a sink attached and where to apply VCONN. The source is not required to supply to VCONN unless R_A is detected.

Two special termination combinations on the CC pins (as seen by a source) are defined for directly attached accessory modes: R_A/R_A for audio adapter accessory mode, and R_D/R_D for debug accessory mode (see Figure 9 below and Table 2 on page 21).

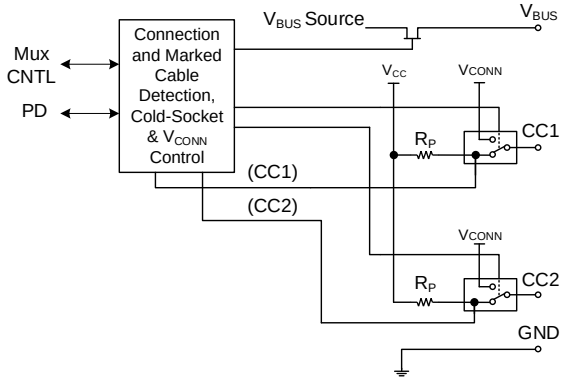


Figure 9: CC Pin Functional Block

A port that behaves as a source has the following functional procedure:

1. The source uses a MOSFET to enable or disable power delivery across V_{BUS}. Initially, the source is disabled.
2. The source supplies pull-up resistors (R_P) on CC1 and CC2, and monitors both to detect a sink. The presence of a pull-down resistor (R_D) on either CC1 or CC2 indicates that a sink is being attached. The value of R_P indicates the initial USB Type-C current level supported by the host. The MPQ4488B's default R_P value is 10kΩ, which represents a 3A current level.
3. The source uses the CC pull-down characteristic to detect and determine which CC pin is intended to supply VCONN (when R_A is determined).
4. Once a sink is detected, the source enables V_{BUS} and VCONN.
5. The source can dynamically adjust the value of R_P to indicate a change in the available USB Type-C current to a sink. For example, at high temperatures, the MPQ4488B changes R_P to 22kΩ to indicate a 1.5A current ability.
6. The source monitors the continued presence of R_D to detect whether a sink has been detached. When a detach event is detected, the source is removed, and V_{BUS} and VCONN return to step 2.

Disable Type-C Mode (Type-A Mode)

During the MPQ4488B initial start-up, it sources 10μA for 40μs on CC1. If the CC1 voltage falls to a voltage between 0.7V and 1.2V, USB1 latches in Type-A mode unless the part is re-enabled. Type-C mode is disabled, so CC1's attach and detach logic is disabled, and V_{BUS} is always enabled. The current limit changes to a Type-A specifications. The same logic is implemented on CC3 for USB2.

To trigger Type-A mode, the external pull-down resistor should be between 90kΩ and 96kΩ. Do not connect extra capacitors on CC1 and CC3.

In normal Type-C mode applications, a 1nF capacitor should be added on CC1 and CC3 to avoid falsely triggering Type-A mode. If two R_A resistors pull down CC1 and CC2, or two R_D resistors pull down CC1 and CC2, there is no action in the IC (V_{BUS} is not enabled).

Load-Shedding vs. Temperature

The MPQ4488B monitors the die temperature and changes its output current capability dynamically. This feature is supported by both Type-C and USB2.0 applications.

If the die temperature exceeds 135°C, the USB port's CC pin pull-up resistance (Rp) changes to 22kΩ to indicate that its source capability has changed to 1.5A. Meanwhile, V_{BUS} changes to 4.77V.

If the die temperature falls below 110°C for 16s, V_{BUS} reverts back to the normal voltage set by OUT_SEL. Meanwhile, the USB Type-C current capability changes back to 3A (R_P = 10kΩ). The current limit threshold remains at 3.55A during this period.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 165°C, the entire chip shuts down. When the temperature returns to below its lower threshold (typically 145°C), the chip is enabled again and resumes normal operation.

Table 2: CC Logic Truth Table

EN	CC of USB1 (11)	CC of USB2 (11)	Buck	VCONN (USB1)	USB1	VCONN (USB2)	USB2
0	X (12)	X	Disabled	Disabled	Disabled	Disabled	Disabled
1	Audio	Open, audio, or debug	Disabled	Disabled	Disabled	Disabled	Disabled
	Debug		Disabled	Disabled	Disabled	Disabled	Disabled
	"A" (13)		Enabled	Disabled	Enabled	Disabled	Disabled
	R_D, R_A		Enabled	Enabled	Enabled	Disabled	Disabled
	Open		Disabled	Disabled	Disabled	Disabled	Disabled
1	Audio	R_D, R_A	Enabled	Disabled	Disabled	Enabled	Enabled
	Debug		Enabled	Disabled	Disabled	Enabled	Enabled
	"A"		Enabled	Disabled	Enabled	Enabled	Enabled
	R_D, R_A		Enabled	Enabled	Enabled	Enabled	Enabled
	Open		Enabled	Disabled	Disabled	Enabled	Enabled
1	Audio	"A"	Enabled	Disabled	Disabled	Disabled	Enabled
	Debug		Enabled	Disabled	Disabled	Disabled	Enabled
	"A"		Enabled	Disabled	Enabled	Disabled	Enabled
	R_D, R_A		Enabled	Enabled	Enabled	Disabled	Enabled
	Open		Enabled	Disabled	Disabled	Disabled	Enabled

Notes:

11) USB1 and USB2 are symmetrical to one another.
12) "X" means all states of the CCx pin.
13) "A" means Type-A mode. CC1 (CC3 for USB2) must to be pulled down by a 95.3kΩ resistor to enter this mode.

APPLICATION INFORMATION

Selecting the Inductor

For most applications, use an inductor with a DC current rating at least 25% above the maximum load current. Select an inductor with a small DC resistance for optimum efficiency. For most designs, the inductor value can be calculated with Equation (2):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (2)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% to 50% of the maximum load current. Calculate the maximum inductor peak current with Equation (3):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (3)$$

Selecting the Buck Input Capacitor

The step-down converter has a discontinuous input current, and therefore requires a capacitor to supply AC current while maintaining the DC input voltage. Use low-ESR capacitors for optimum performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. It is recommended to use one 100µF electrolytic and two 4.7µF ceramic capacitors for automotive applications at a 450kHz switching frequency.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (4):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (5):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using an electrolytic capacitor, place two additional high-quality ceramic capacitors as close to IN as possible. Estimate the input voltage ripple caused by the capacitance with Equation (6):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

Selecting the Buck Output Capacitor

The device requires an output capacitor (C2) to maintain the DC output voltage. Estimate the output voltage ripple with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (7)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For an electrolytic capacitor, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (8)$$

It is recommended to use a 100µF to 270µF capacitor with an ESR below 50mΩ (e.g. polymer or tantalum capacitors) and two 2.2µF ceramic capacitors in application (see Table 3).

Table 3: Recommended External Components

f_{SW}	Inductor	Input Capacitors	Buck Output Capacitors
250kHz	8µH	2 x 4.7µF ceramic capacitor + 100µF electrolytic capacitor	2 x 2.2µF ceramic capacitor + 100µF polymer capacitor
450kHz	4.7µH	2 x 4.7µF ceramic capacitor + 100µF electrolytic capacitor	2 x 2.2µF ceramic capacitor + 100µF polymer capacitor

ESD Protection for I/O Pins

Higher ESD levels should be considered for all USB I/O pins. The MPQ4488B features high ESD protection up to ±8kV human body model on DP, DM, USB1, and USB2, and ±7kV human

body model on CC1 through CC4. The ESD structures can withstand high ESD both during normal operation and when the device is powered off. In order to further extend the DP, DM, and CCx pins' ESD level for covering complicated application environments, an additional ESD diode should be added on all pins (see Figure 10).

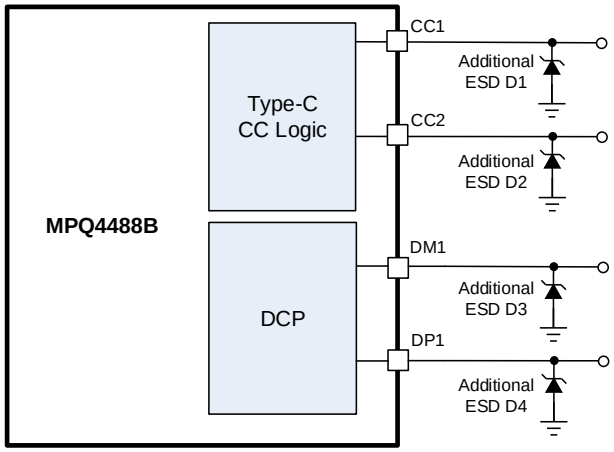


Figure 10: Recommended I/O Pins for ESD Enhancing

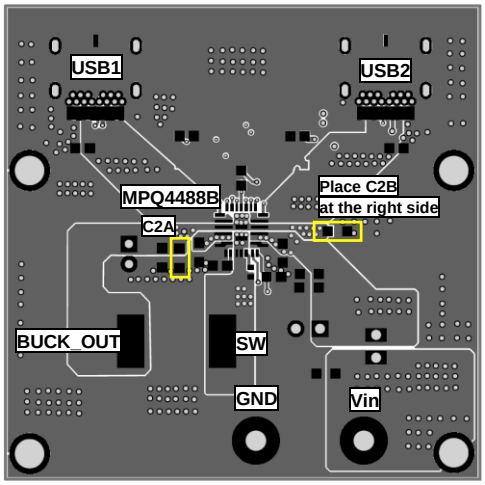
PCB Layout Guidelines (14)

Efficient PCB layout is critical for stable operation and thermal dissipation. For the best results, refer to Figure 11 and follow the PCB layout guidelines below:

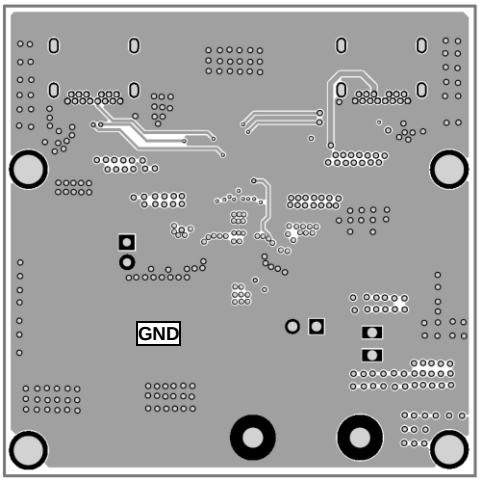
1. Use short, direct, and wide traces to connect OUT.
2. Add multiple vias to improve thermal dissipation, including under the IC.
3. Route the OUT, USB1, and USB2 traces on both PCB layers.
4. Place buck output ceramic capacitor C2A on the left side, and C2B on the right side.
5. Place a large copper plane for PGND.
6. Connect AGND to PGND.
7. Use a large copper plane for SW, USB, and USB2.
8. Place two ceramic input decoupling capacitors as close to IN and PGND as possible to improve EMI performance.
9. Place the symmetrical C_{IN} capacitors on each side of the IC.
10. Place the BST capacitor close to BST and SW.
11. Place the VCC decoupling capacitor as close to VCC as possible.

Note:

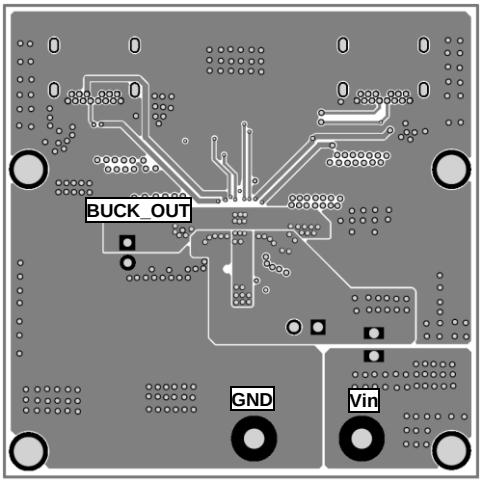
14) The recommended layout is based on the Typical Application Circuits (see Figure 12, Figure 13, Figure 14, and Figure 15).



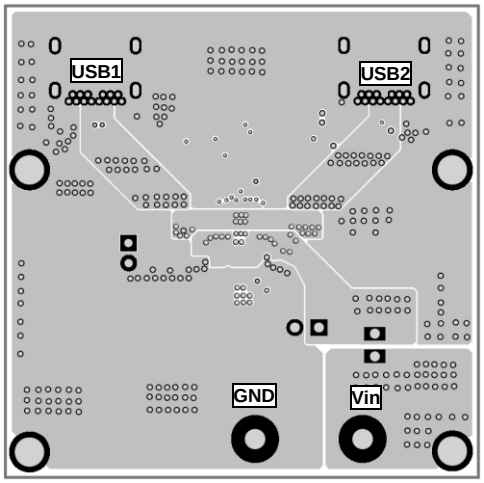
Top Layer



Mid-Layer 2



Mid-Layer 1



Bottom Layer

Figure 11: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

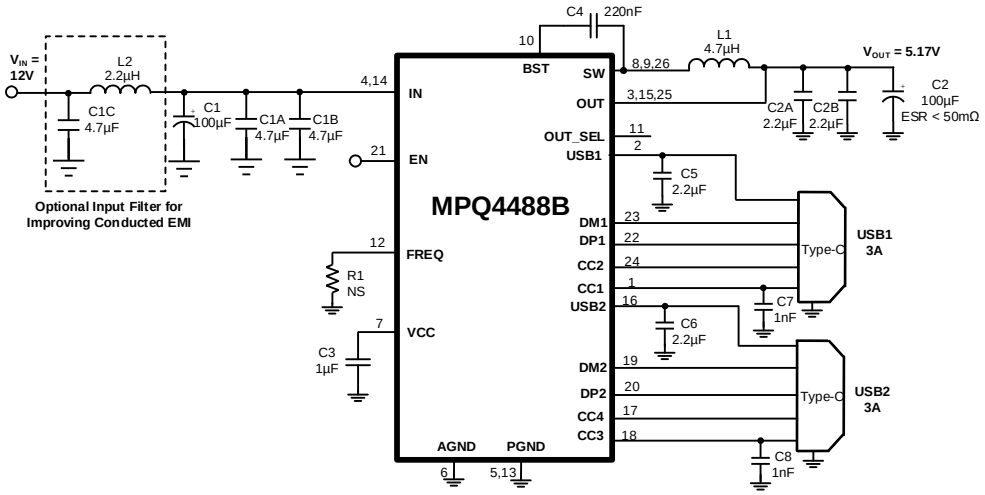


Figure 12: Dual USB Type-C 5V/3A DFP Ports (15)

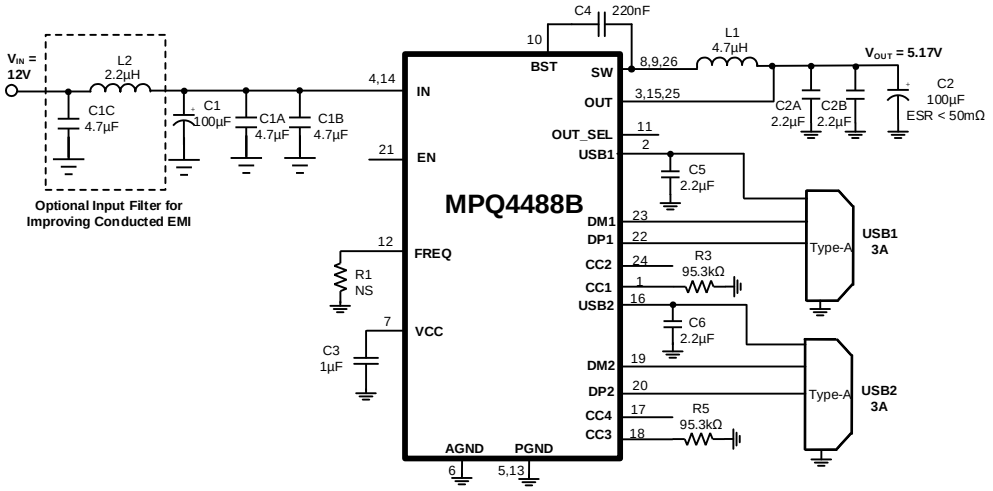


Figure 13: Dual USB Type-A 5V/3A Ports (15)

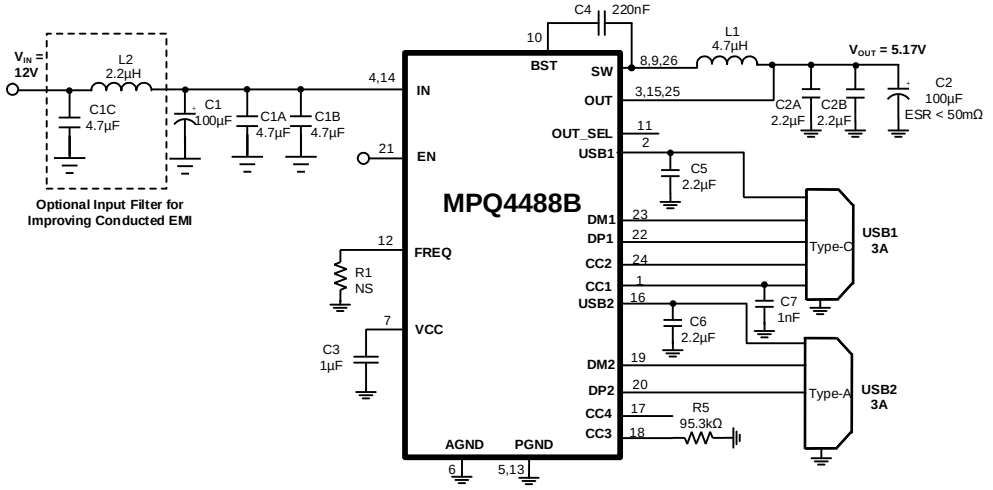


Figure 14: Single USB Type-C 5V/3A DFP Port, Single Type-A 5V/3A Port (15)

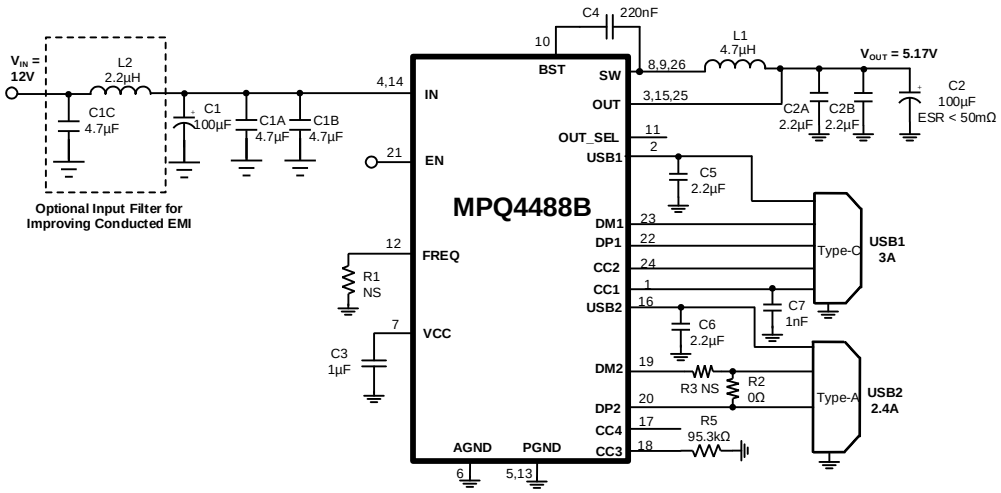


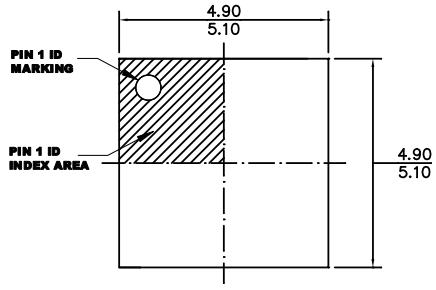
Figure 15: Single Type-C 5V/3A DFP Port, Single Type-A 5V/2.4A Port (2.7V Divider 3 Mode) (15)

Note:

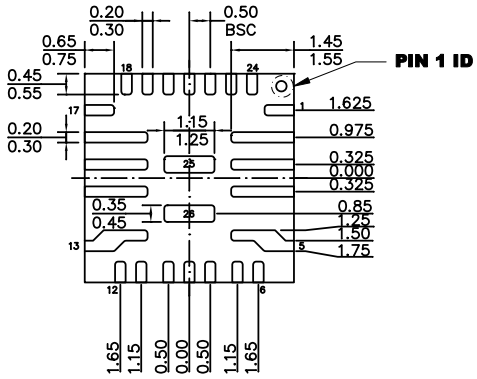
15) See Figure 10 for details on I/O pins ESD protection enhancement.

PACKAGE INFORMATION

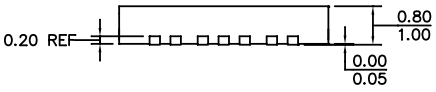
QFN-26 (5mmx5mm)



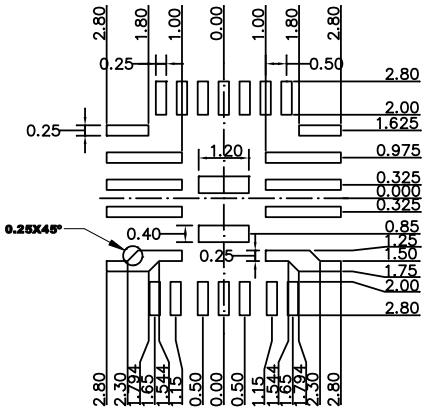
TOP VIEW



BOTTOM VIEW



SIDE VIEW

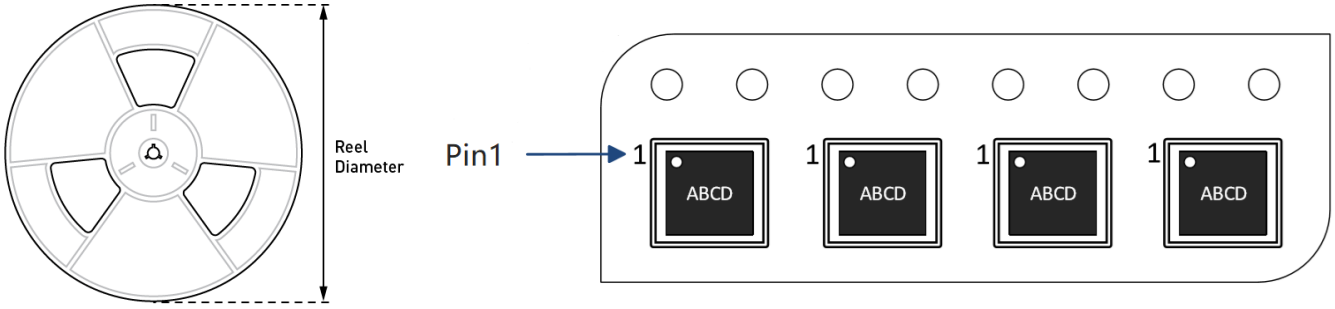


RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PINS 2~4 AND PINS 14~16 HAVE THE SAME LENGTH AND WIDTH.
2) LAND PATTERNS OF PIN 5 AND PIN 13 HAVE THE SAME LENGTH AND WIDTH.
3) ALL DIMENSIONS ARE IN MILLIMETERS.
4) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
5) REFERENCEIS MO-220.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity /Reel	Quantity /Tube	Quantity /Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4488BGU-AEC1–Z	QFN-26 (5mmx5mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ4488BGU-FD-AEC1–Z	QFN-26 (5mmx5mm)	5000	N/A	N/A	13in	12mm	8mm