

FEATURES

- Fast 35 ns Read/Write cycle
- SRAM compatible timing, uses existing SRAM controllers without redesign
- Unlimited Read & Write endurance
- Data non-volatile for >20 years at temperature
- One memory replaces Flash, SRAM, EEPROM and BBSRAM in a system for simpler, more efficient design
- Replaces battery-backed SRAM solutions with MRAM to improve reliability
- 3.3 volt power supply
- Automatic data protection on power loss
- Commercial, Industrial, Extended temperatures
- AEC-Q100 Grade 1 option
- All products meet MSL-3 moisture sensitivity level
- RoHS-compliant SRAM TSOP2 and BGA Packages

128K x 16 MRAM Memory



INTRODUCTION

The **MR1A16A** is a 2,097,152-bit magnetoresistive random access memory (MRAM) device organized as 131,072 words of 16 bits. The **MR1A16A** offers SRAM compatible 35 ns read/write timing with unlimited endurance. Data is always non-volatile for greater than 20 years. Data is automatically protected on power loss by low-voltage inhibit circuitry to prevent writes with voltage out of specification.

The **MR1A16A** is the ideal memory solution for applications that must permanently store and retrieve critical data and programs quickly.

The **MR1A16A** is available in a small footprint 48-pin ball grid array (BGA) package and a 44-pin thin small outline package (TSOP Type 2). These packages are compatible with similar low-power SRAM products and other nonvolatile RAM products.

The **MR1A16A** provides highly reliable data storage over a wide range of temperatures. The product is offered with Commercial (0 to +70 °C), Industrial (-40 to +85 °C), Extended (-40 to +105 °C), and AEC-Q100 Grade 1 (-40 to +125 °C) operating temperature range options.

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BLOCK DIAGRAM AND PIN ASSIGNMENTS

Figure 1 – Block Diagram

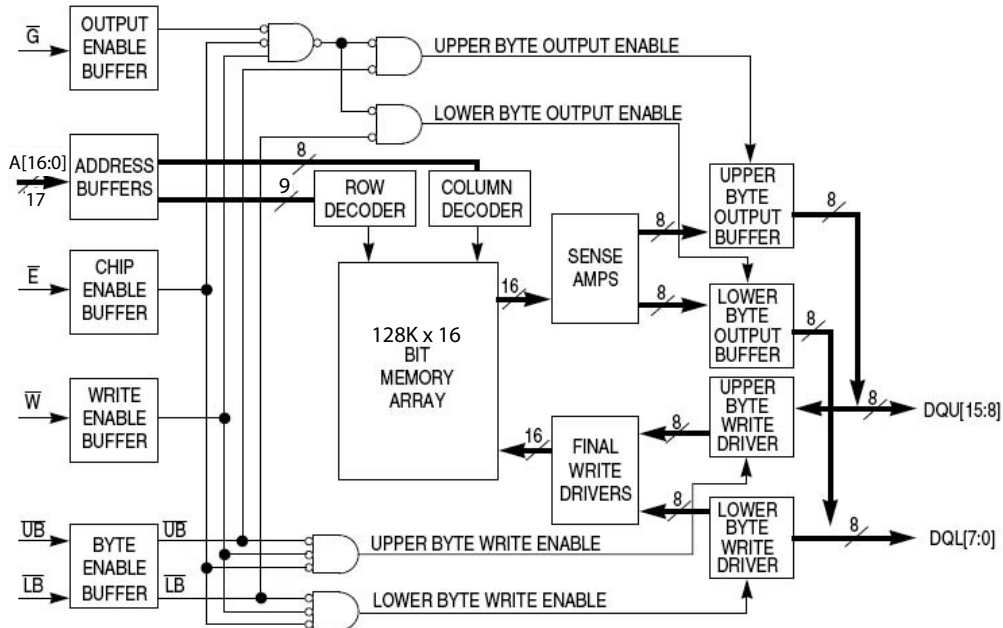
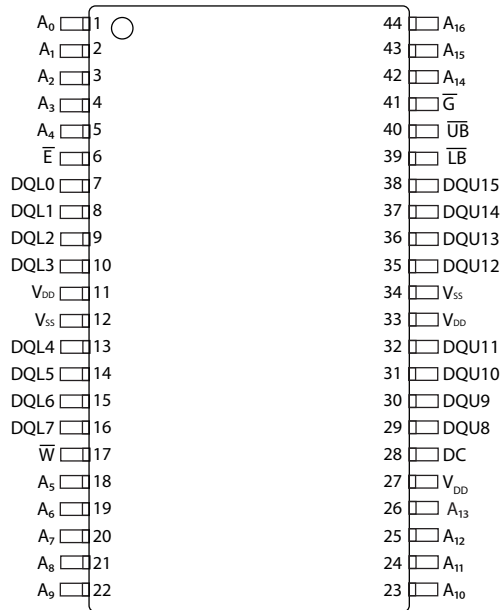


Figure 1. Block Diagram

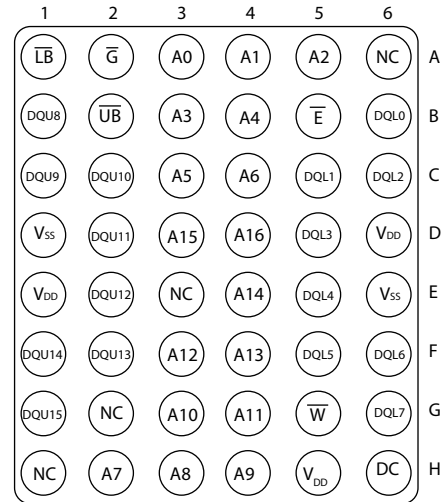
Table 1 – Pin Functions

| Signal Name | Function |
|-------------|-------------------|
| A | Address Input |
| \bar{E} | Chip Enable |
| \bar{W} | Write Enable |
| \bar{G} | Output Enable |
| \bar{UB} | Upper Byte Enable |
| \bar{LB} | Lower Byte Enable |
| DQ | Data I/O |
| V_{DD} | Power Supply |
| V_{SS} | Ground |
| DC | Do Not Connect |
| NC | No Connection |

Figure 2 – Pin Diagrams for Available Packages (Top View)



44-Pin TSOP Type2



48-Pin BGA

Table 2 – Operating Modes

| \bar{E}^1 | \bar{G}^1 | \bar{W}^1 | \bar{LB}^1 | \bar{UB}^1 | Mode | V _{DD} Current | DQL[7:0] ² | DQU[15:8] ² |
|-------------|-------------|-------------|--------------|--------------|------------------|-------------------------------------|-----------------------|------------------------|
| H | X | X | X | X | Not selected | I _{SB1} , I _{SB2} | Hi-Z | Hi-Z |
| L | H | H | X | X | Output disabled | I _{DDR} | Hi-Z | Hi-Z |
| L | X | X | H | H | Output disabled | I _{DDR} | Hi-Z | Hi-Z |
| L | L | H | L | H | Lower Byte Read | I _{DDR} | D _{Out} | Hi-Z |
| L | L | H | H | L | Upper Byte Read | I _{DDR} | Hi-Z | D _{Out} |
| L | L | H | L | L | Word Read | I _{DDR} | D _{Out} | D _{Out} |
| L | X | L | L | H | Lower Byte Write | I _{DDW} | D _{in} | Hi-Z |
| L | X | L | H | L | Upper Byte Write | I _{DDW} | Hi-Z | D _{in} |
| L | X | L | L | L | Word Write | I _{DDW} | D _{in} | D _{in} |

Notes:

1. H = high, L = low, X = don't care
2. Hi-Z = high impedance

ABSOLUTE MAXIMUM RATINGS

Table 3 – Absolute Maximum Ratings

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings. ¹

| Symbol | Parameter | Temp Range | Package | Value | Unit |
|------------------|---|----------------------|------------|------------------------|------|
| V_{DD} | Supply voltage ² | - | - | -0.5 to 4.0 | V |
| V_{IN} | Voltage on any pin ² | - | - | -0.5 to $V_{DD} + 0.5$ | V |
| I_{OUT} | Output current per pin | - | - | ± 20 | mA |
| P_D | Package power dissipation ³ | - | Note 3 | 0.600 | W |
| T_{BIAS} | Temperature under bias | Commercial | - | -10 to 85 | °C |
| | | Industrial | - | -45 to 95 | |
| | | Extended | - | -45 to 110 | |
| | | AEC-Q100 Grade 1 | - | -45 to 130 | |
| T_{stg} | Storage Temperature | - | - | -55 to 150 | °C |
| T_{Lead} | Lead temperature during solder (3 minute max) | - | - | 260 | °C |
| H_{max_write} | Maximum magnetic field during write | Commercial | TSOP2, BGA | 2,000 | A/m |
| | | Industrial, Extended | BGA | 2,000 | |
| | | | TSOP2 | 10,000 | |
| | | AEC-Q100 Grade 1 | TSOP2 | 2,000 | |
| H_{max_read} | Maximum magnetic field during read or standby | Commercial | TSOP2, BGA | 8,000 | A/m |
| | | Industrial, Extended | BGA | 8,000 | |
| | | | TSOP2 | 10,000 | |
| | | AEC-Q100 Grade 1 | TSOP2 | 8,000 | |

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.
2. All voltages are referenced to V_{SS} .
3. Power dissipation capability depends on package characteristics and use environment.

OPERATING CONDITIONS

| Parameter | Symbol | Min | Typical | Max | Unit |
|--|----------|------------------------|---------|-----------------------------|------|
| Power supply voltage ¹ | V_{DD} | 3.0 | 3.3 | 3.6 | V |
| Write inhibit voltage | V_{WI} | 2.5 | 2.7 | 3.0 ¹ | V |
| Input high voltage | V_{IH} | 2.2 | - | $V_{DD} + 0.3$ ² | V |
| Input low voltage | V_{IL} | -0.5 ³ | - | 0.8 | V |
| Temperature under bias MR1A16A (Commercial) MR1A16AC (Industrial) MR1A16AV (Extended) MR1A16AM (AEC-Q100 Grade 1) ⁴ | T_A | 0 -40 -40 -40 | | 70 85 105 125 | °C |

Notes:

1. There is a 2 ms startup time once V_{DD} exceeds $V_{DD, (max)}$. See "Power Up and Power Down Sequencing" on page 8.
2. $V_{IH(max)} = V_{DD} + 0.3 V_{DC}$; $V_{IH(max)} = V_{DD} + 2.0 V_{AC}$ (pulse width ≤ 10 ns) for $I \leq 20.0$ mA.
3. $V_{IL(min)} = -0.5 V_{DC}$; $V_{IL(min)} = -2.0 V_{AC}$ (pulse width ≤ 10 ns) for $I \leq 20.0$ mA.
4. AEC-Q100 Grade 1 temperature profile assumes 10% duty cycle at maximum temperature (2 years out of 20 years life.)

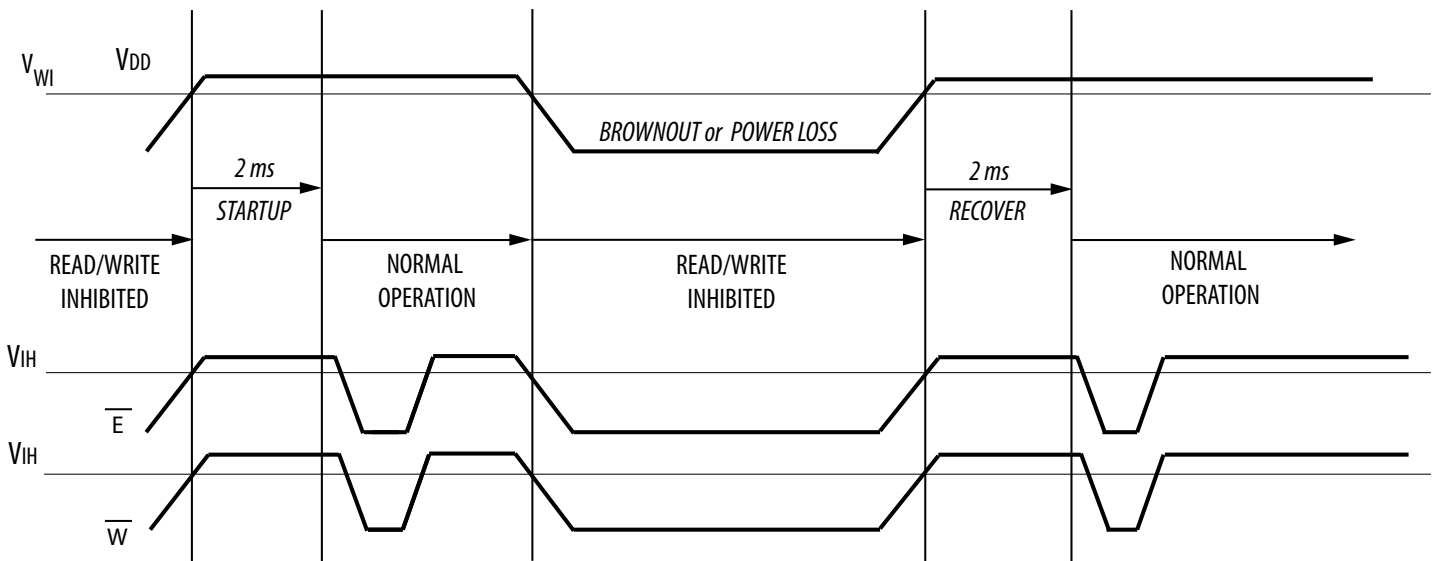
Power Up and Power Down Sequencing

The MRAM is protected from write operations whenever V_{DD} is less than V_{WI} . As soon as V_{DD} exceeds $V_{DD}(\min)$, there is a startup time of 2 ms before read or write operations can start. This time allows memory power supplies to stabilize.

The \bar{E} and \bar{W} control signals should track V_{DD} on power up to $V_{DD} - 0.2\text{ V}$ or V_{IH} (whichever is lower) and remain high for the startup time. In most systems, this means that these signals should be pulled up with a resistor so that signal remains high if the driving signal is Hi-Z during power up. Any logic that drives E and W should hold the signals high with a power-on reset signal for longer than the startup time.

During power loss or brownout where V_{DD} goes below V_{WI} , writes are protected and a startup time must be observed when power returns above $V_{DD}(\min)$.

Figure 3 – Power Up and Power Down Sequencing Timing Diagram



DC CHARACTERISTICS

Table 4 – DC Characteristics

| Parameter | Symbol | Min | Typical | Max | Unit |
|--|--------------|-----------------------|---------|-----------------------|---------|
| Input leakage current | $I_{lkg(I)}$ | - | - | ± 1 | μA |
| Output leakage current | $I_{lkg(O)}$ | - | - | ± 1 | μA |
| Output low voltage ($I_{OL} = +4 \text{ mA}$) ($I_{OL} = +100 \mu A$) | V_{OL} | - | - | 0.4 $V_{SS} + 0.2$ | V |
| Output high voltage ($I_{OH} = -4 \text{ mA}$) ($I_{OH} = -100 \mu A$) | V_{OH} | 2.4 $V_{DD} - 0.2$ | - | - | V |

Table 5 – Power Supply Characteristics

| Parameter | Symbol | Typical | Max | Unit |
|---|-----------|--------------------------|--------------------------|------|
| AC active supply current - read modes ¹ ($I_{OUT} = 0 \text{ mA}, V_{DD} = \text{max}$) | I_{DDR} | 55 | 80 | mA |
| AC active supply current - write modes ¹ ($V_{DD} = \text{max}$) Commercial Grade Industrial Grade Extended Grade AEC-Q100 Grade | I_{DDW} | 105 105 105 105 | 155 165 165 165 | mA |
| AC standby current ($V_{DD} = \text{max}, \bar{E} = V_{IH}$) <i>no other restrictions on other inputs</i> | I_{SB1} | 18 | 28 | mA |
| CMOS standby current ($\bar{E} \geq V_{DD} - 0.2 \text{ V}$ and $V_{In} \leq V_{SS} + 0.2 \text{ V}$ or $\geq V_{DD} - 0.2 \text{ V}$) ($V_{DD} = \text{max}, f = 0 \text{ MHz}$) | I_{SB2} | 9 | 12 | mA |

Notes:

1. All active current measurements are measured with one address transition per cycle and at minimum cycle time.

TIMING SPECIFICATIONS

Table 6 – Capacitance

| Parameter ¹ | Symbol | Typical | Max | Unit |
|---------------------------|-----------|---------|-----|------|
| Address input capacitance | C_{In} | - | 6 | pF |
| Control input capacitance | C_{In} | - | 6 | pF |
| Input/Output capacitance | $C_{I/O}$ | - | 8 | pF |

Notes:

- $f = 1.0 \text{ MHz}$, $dV = 3.0 \text{ V}$, $T_A = 25 \text{ }^\circ\text{C}$, periodically sampled rather than 100% tested.

Table 7 – AC Measurement Conditions

| Parameter | Value | Unit |
|---|--------------|------|
| Logic input timing measurement reference level | 1.5 | V |
| Logic output timing measurement reference level | 1.5 | V |
| Logic input pulse levels | 0 or 3.0 | V |
| Input rise/fall time | 2 | ns |
| Output load for low and high impedance parameters | See Figure 4 | |
| Output load for all other timing parameters | See Figure 5 | |

Figure 4 – Output Load Test Low and High

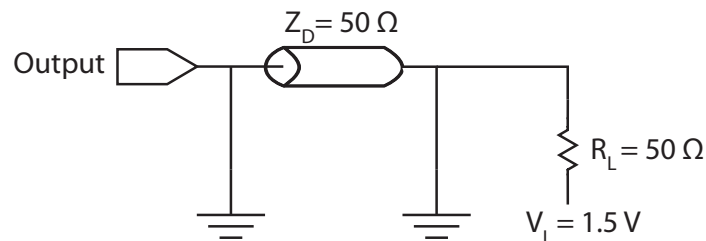
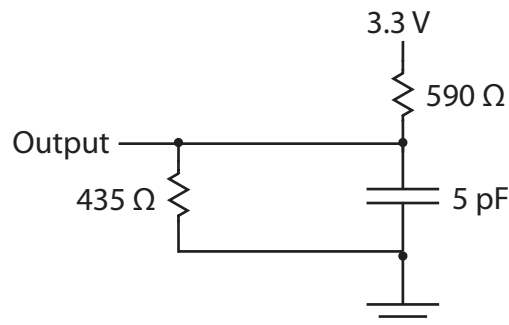


Figure 5 – Output Load Test All Others



Read Mode

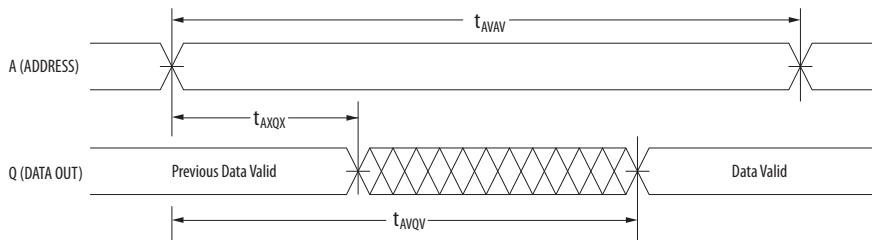
Table 8 – Read Cycle Timing

| Parameter ¹ | Symbol | Min | Max | Unit |
|---|------------|-----|-----|------|
| Read cycle time | t_{AVAV} | 35 | - | ns |
| Address access time | t_{AVQV} | - | 35 | ns |
| Enable access time ² | t_{ELQV} | - | 35 | ns |
| Output enable access time | t_{GLQV} | - | 15 | ns |
| Byte enable access time | t_{BLQV} | - | 15 | ns |
| Output hold from address change | t_{AXQX} | 3 | - | ns |
| Enable low to output active ³ | t_{ELQX} | 3 | - | ns |
| Output enable low to output active ³ | t_{GLQX} | 0 | - | ns |
| Byte enable low to output active ³ | t_{BLQX} | 0 | - | ns |
| Enable high to output Hi-Z ³ | t_{EHQZ} | 0 | 15 | ns |
| Output enable high to output Hi-Z ³ | t_{GHQZ} | 0 | 10 | ns |
| Byte high to output Hi-Z ³ | t_{BHQZ} | 0 | 10 | ns |

Notes:

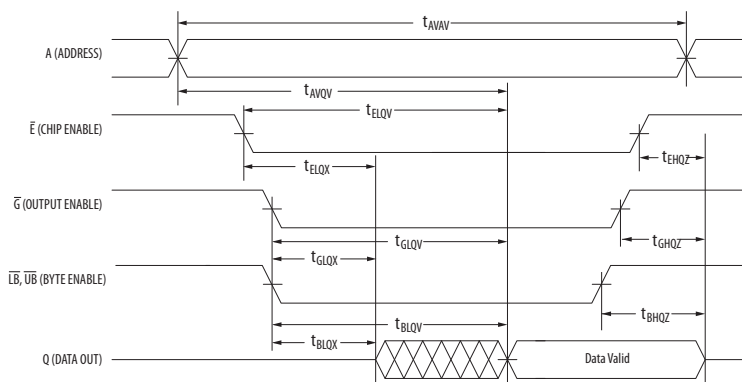
- \bar{W} is high for read cycle. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles.
- Addresses valid before or at the same time \bar{E} goes low.
- This parameter is sampled and not 100% tested. Transition is measured ± 200 mV from the steady-state voltage.

Figure 6 – Read Cycle 1



Note: Device is continuously selected ($\bar{E} \leq V_{IL}$, $\bar{G} \leq V_{IL}$).

Figure 7 – Read Cycle 2



Write Mode

Table 9 – Write Cycle Timing 1 (\overline{W} Controlled)

| Parameter ¹ | Symbol | Min | Max | Unit |
|--|--------------------------|-----|-----|------|
| Write cycle time ² | t_{AVAV} | 35 | - | ns |
| Address set-up time | t_{AVWL} | 0 | - | ns |
| Address valid to end of write (\overline{G} high) | t_{AVWH} | 18 | - | ns |
| Address valid to end of write (\overline{G} low) | t_{AVWH} | 20 | - | ns |
| Write pulse width (\overline{G} high) | t_{WLWH} t_{WLEH} | 15 | - | ns |
| Write pulse width (\overline{G} low) | t_{WLWH} t_{WLEH} | 15 | - | ns |
| Data valid to end of write | t_{DVWH} | 10 | - | ns |
| Data hold time | t_{WHDX} | 0 | - | ns |
| Write low to data Hi-Z ³ | t_{WLQZ} | 0 | 12 | ns |
| Write high to output active ³ | t_{WHQX} | 3 | - | ns |
| Write recovery time | t_{WHAX} | 12 | - | ns |

Notes:

- All write occurs during the overlap of \overline{E} low and \overline{W} low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If \overline{G} goes low at the same time or after \overline{W} goes low, the output will remain in a high impedance state. After \overline{W} , \overline{E} or $\overline{UB}/\overline{LB}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between \overline{E} being asserted low in one cycle to \overline{E} being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
- All write cycle timings are referenced from the last valid address to the first transition address.
- This parameter is sampled and not 100% tested. Transition is measured ± 200 mV from the steady-state voltage. At any given voltage or temperate, $t_{WLQZ}(\max) < t_{WHQX}(\min)$

Figure 8 – Write Cycle Timing 1 (\overline{W} Controlled)

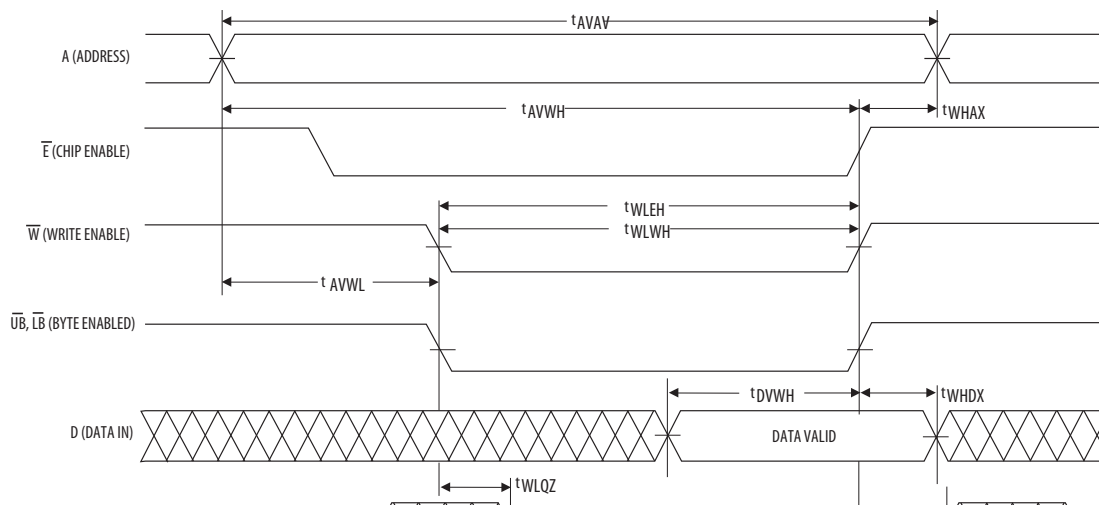


Table 10 – Write Cycle Timing 2 (\bar{E} Controlled)

| Parameter ¹ | Symbol | Min | Max | Unit |
|--|--------------------------|-----|-----|------|
| Write cycle time ² | t_{AVAV} | 35 | - | ns |
| Address set-up time | t_{AVEL} | 0 | - | ns |
| Address valid to end of write (\bar{G} high) | t_{AVEH} | 18 | - | ns |
| Address valid to end of write (\bar{G} low) | t_{AVEH} | 20 | - | ns |
| Enable to end of write (\bar{G} high) | t_{ELEH} t_{ELWH} | 15 | - | ns |
| Enable to end of write (\bar{G} low) ³ | t_{ELEH} t_{ELWH} | 15 | - | ns |
| Data valid to end of write | t_{DVEH} | 10 | - | ns |
| Data hold time | t_{EHDX} | 0 | - | ns |
| Write recovery time | t_{EHAX} | 12 | - | ns |

Notes:

1. All write occurs during the overlap of \bar{E} low and \bar{W} low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If \bar{G} goes low at the same time or after \bar{W} goes low, the output will remain in a high impedance state. After \bar{W} , \bar{E} or \bar{UB}/\bar{LB} has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between \bar{E} being asserted low in one cycle to \bar{E} being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
2. All write cycle timings are referenced from the last valid address to the first transition address.
3. If \bar{E} goes low at the same time or after \bar{W} goes low, the output will remain in a high-impedance state. If \bar{E} goes high at the same time or before \bar{W} goes high, the output will remain in a high-impedance state.

Figure 9 – Write Cycle Timing 2 (\bar{E} Controlled)

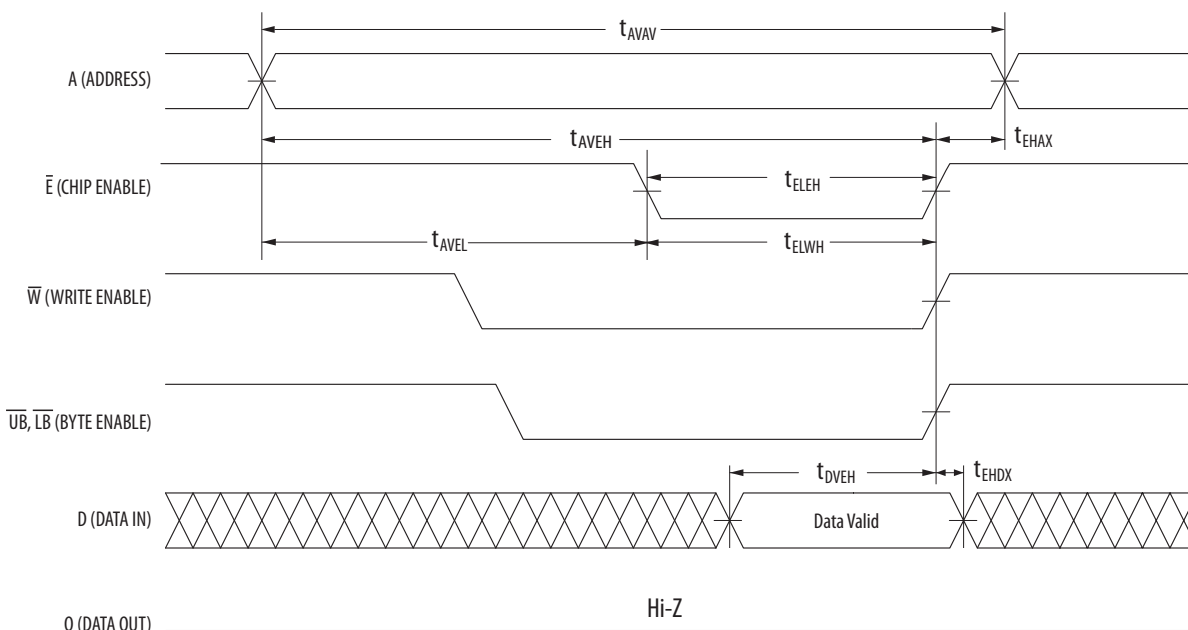


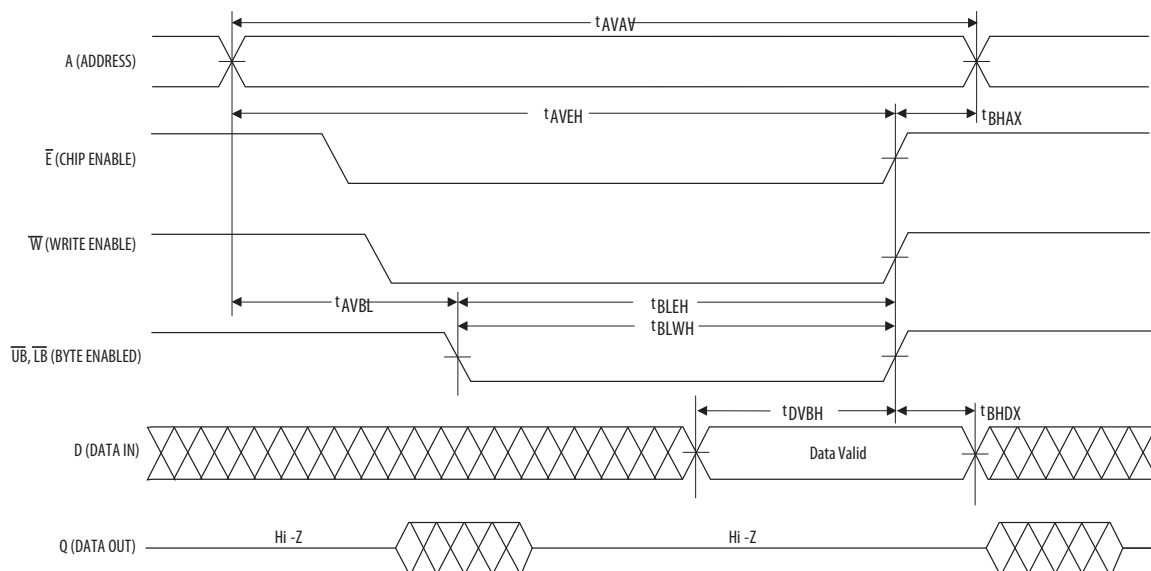
Table 11 – Write Cycle Timing 3 (\overline{LB} / \overline{UB} Controlled)

| Parameter ¹ | Symbol | Min | Max | Unit |
|--|--------------------------|-----|-----|------|
| Write cycle time ² | t_{AVAV} | 35 | - | ns |
| Address set-up time | t_{AVBL} | 0 | - | ns |
| Address valid to end of write (\overline{G} high) | t_{AVBH} | 18 | - | ns |
| Address valid to end of write (\overline{G} low) | t_{AVBH} | 20 | - | ns |
| Write pulse width (\overline{G} high) | t_{BLEH} t_{BLWH} | 15 | - | ns |
| Write pulse width (\overline{G} low) | t_{BLEH} t_{BLWH} | 15 | - | ns |
| Data valid to end of write | t_{DVBH} | 10 | - | ns |
| Data hold time | t_{BHDX} | 0 | - | ns |
| Write recovery time | t_{BHAX} | 12 | - | ns |

Notes:

- All write occurs during the overlap of \overline{E} low and \overline{W} low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If \overline{G} goes low at the same time or after \overline{W} goes low, the output will remain in a high impedance state. After \overline{W} , \overline{E} or $\overline{LB}/\overline{UB}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. If both byte control signals are asserted, the two signals must have no more than 2 ns skew between them. The minimum time between \overline{E} being asserted low in one cycle to \overline{E} being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
- All write cycle timings are referenced from the last valid address to the first transition address.

Figure 10 – Write Cycle Timing 3 (\overline{LB} / \overline{UB} Controlled)



ORDERING INFORMATION

Table 12 – Ordering Part Number System for Parallel I/O MRAM

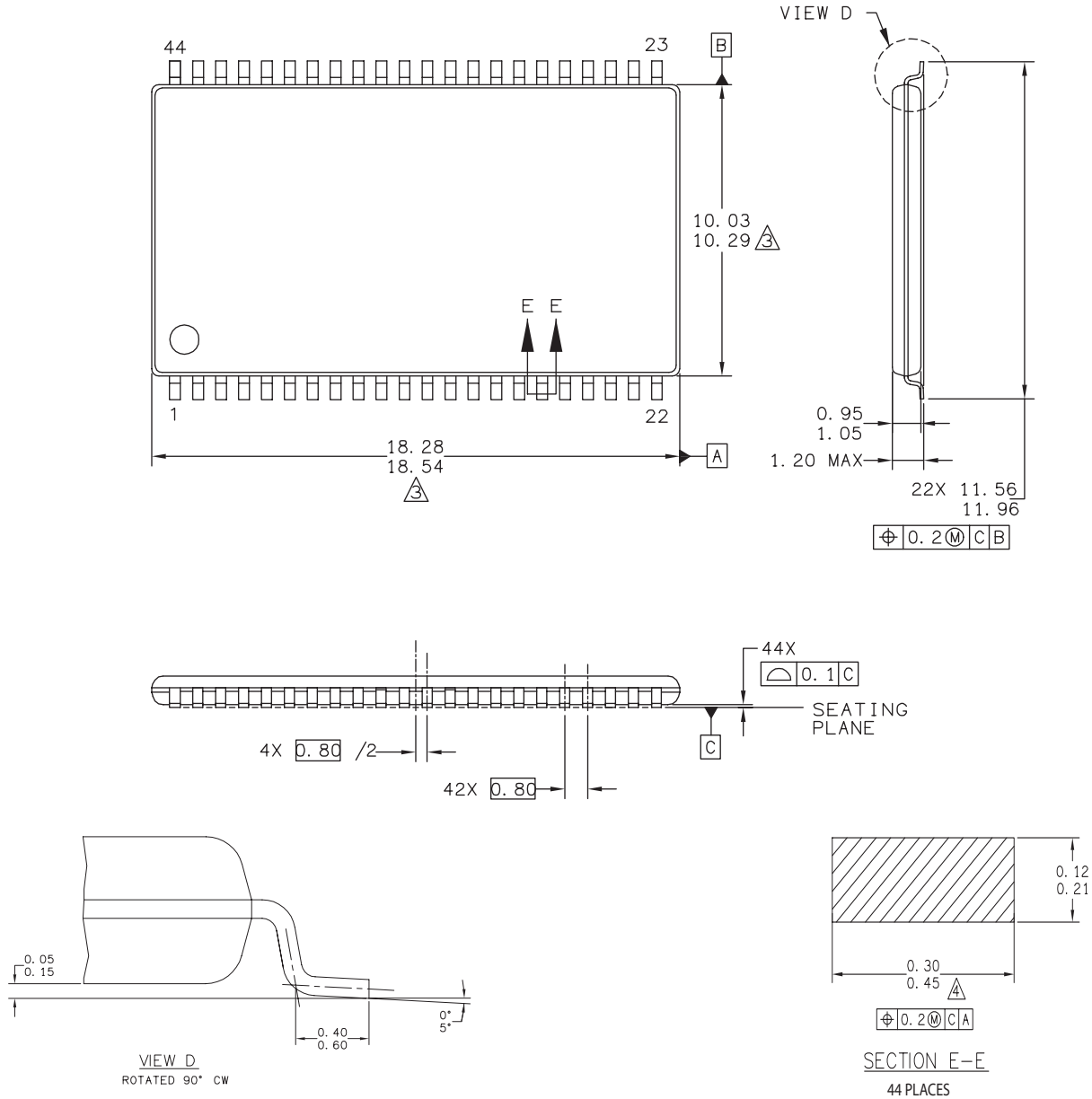
| Example Ordering Part Number | | Memory | Density | Type | I/O Width | Rev. | Temp | Package | Speed | Packing | Grade |
|---|--------------|--------|---------|------|-----------|------|------|---------|-------|---------|-------|
| MRAM | MR | MR | 1 | A | 16 | A | C | MA | 35 | R | |
| 256 Kb | 256 | | | | | | | | | | |
| 1 Mb | 0 | | | | | | | | | | |
| 2 Mb | 1 | | | | | | | | | | |
| 4 Mb | 2 | | | | | | | | | | |
| 8 Mb | 3 | | | | | | | | | | |
| 16Mb | 4 | | | | | | | | | | |
| 32Mb | 5 | | | | | | | | | | |
| Async 3.3v | A | | | | | | | | | | |
| Async 3.3v Vdd and 1.8v Vddq | D | | | | | | | | | | |
| Async 3.3v Vdd and 1.8v Vddq with 2.7v min. Vdd | DL | | | | | | | | | | |
| 8-bit | 08 | | | | | | | | | | |
| 16-bit | 16 | | | | | | | | | | |
| Rev A | A | | | | | | | | | | |
| Rev B | B | | | | | | | | | | |
| Commercial | 0 to 70°C | Blank | | | | | | | | | |
| Industrial | -40 to 85°C | C | | | | | | | | | |
| AEC Q-100 Grade 3 | -40 to 85°C | P | | | | | | | | | |
| Extended | -40 to 105°C | V | | | | | | | | | |
| AEC Q-100 Grade 2 | -40 to 105°C | N | | | | | | | | | |
| Automotive | -40 to 125°C | U | | | | | | | | | |
| AEC-Q100 Grade 1 | -40 to 125°C | M | | | | | | | | | |
| 44-TSOP2 | YS | | | | | | | | | | |
| 48-BGA | MA | | | | | | | | | | |
| 35 ns | 35 | | | | | | | | | | |
| 45 ns | 45 | | | | | | | | | | |
| Tray | Blank | | | | | | | | | | |
| Tape and Reel | R | | | | | | | | | | |
| Engineering Samples | ES | | | | | | | | | | |
| Customer Samples | CS | | | | | | | | | | |
| Mass Production | Blank | | | | | | | | | | |

Table 13 – MR1A16A Ordering Part Numbers

| Temp Grade | Temp | Package | Shipping | Ordering Part Number |
|-----------------------------|----------------|----------|---------------|----------------------|
| Commercial | 0 to +70 °C | 44-TSOP2 | Tray | MR1A16AYS35 |
| | | | Tape and Reel | MR1A16AYS35R |
| | | 48-BGA | Tray | MR1A16AMA35 |
| | | | Tape and Reel | MR1A16AMA35R |
| Industrial | -40 to +85 °C | 44-TSOP2 | Tray | MR1A16ACYS35 |
| | | | Tape and Reel | MR1A16ACYS35R |
| | | 48-BGA | Tray | MR1A16ACMA35 |
| | | | Tape and Reel | MR1A16ACMA35R |
| Extended | -40 to +105 °C | 44-TSOP2 | Tray | MR1A16AVYS35 |
| | | | Tape and Reel | MR1A16AVYS35R |
| | | 48-BGA | Tray | MR1A16AVMA35 |
| | | | Tape and Reel | MR1A16AVMA35R |
| Automotive AEC-Q100 Grade 1 | -40 to +125 °C | 44-TSOP2 | Tray | MR1A16AMYS35 |
| | | | Tape and Reel | MR1A16AMYS35R |

PACKAGE OUTLINE DRAWINGS

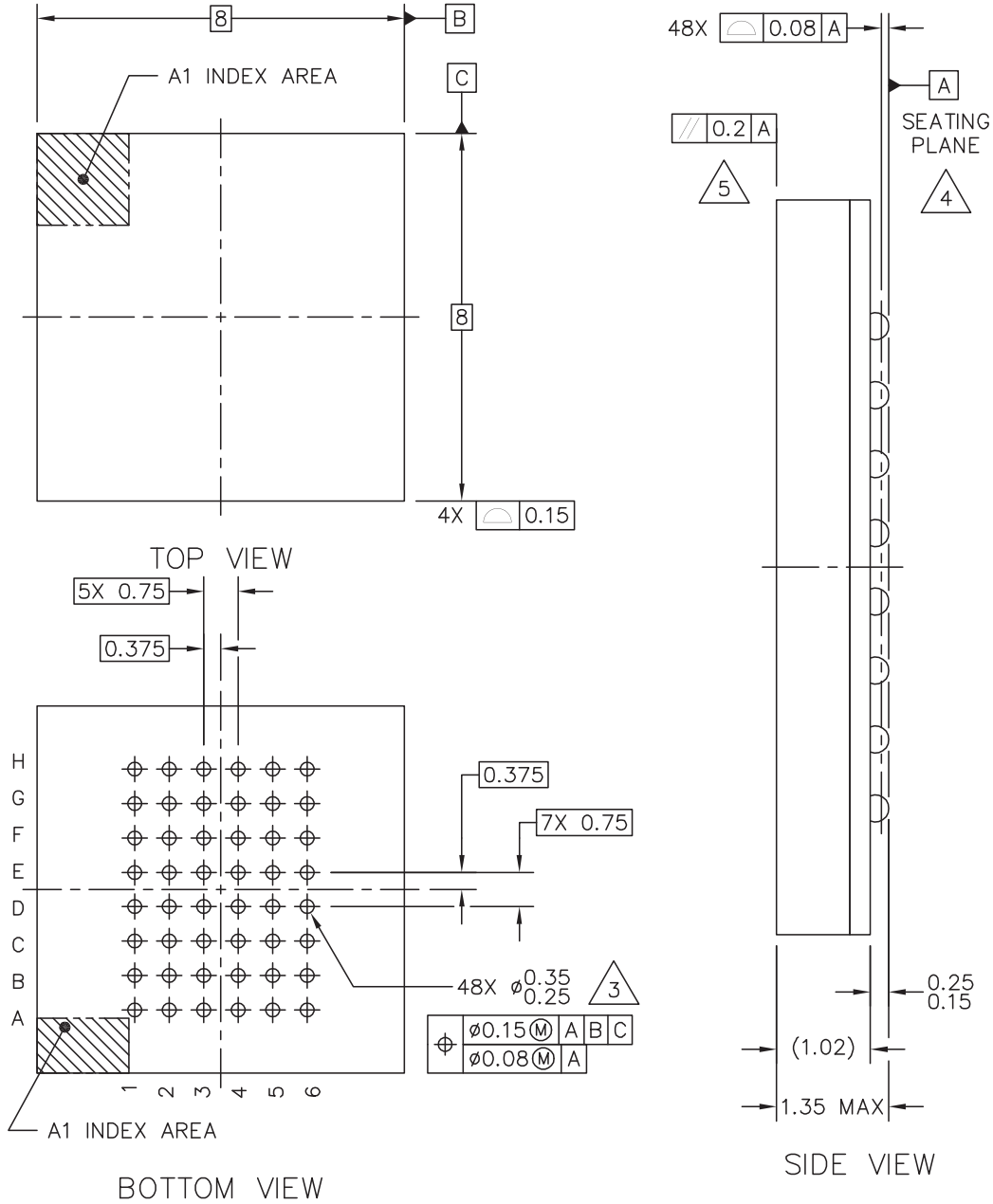
Figure 11 – 44-TSOP2 Package Outline



Print Version Not To Scale

1. Dimensions and tolerances per ASME Y14.5M - 1994.
2. Dimensions in Millimeters.
3. Dimensions do not include mold protrusion.
4. Dimension does not include DAM bar protrusions.
DAM Bar protrusion shall not cause the lead width to exceed 0.58.

Figure 12 – 48-FBGA Package Outline



Notes:

1. Dimensions in Millimeters.
2. Dimensions and tolerances per ASMEY14.5M - 1994.
3. Maximum solder ball diameter measured parallel to DATUM A.
4. DATUM A, the seating plane is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.

REVISION HISTORY

| Revision | Date | Description of Change |
|-----------------|-----------------|--|
| 1.0 | October 1, 2019 | Initial data sheet release |
| 1.1 | March 10, 2020 | Updated Table 12 to correct temperature designator |