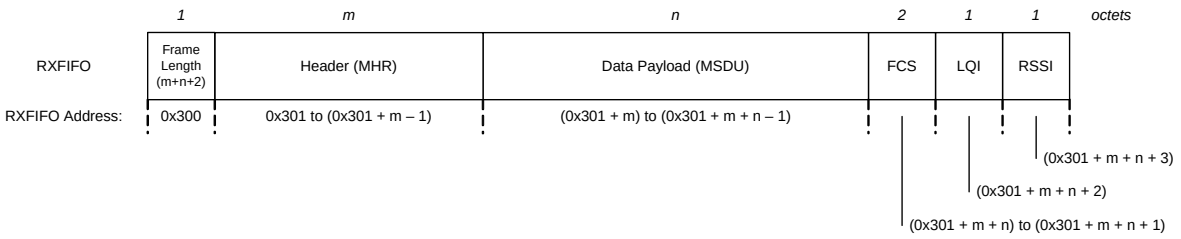
3.17.2 MAC SUBLAYER RECEIVE DECRYPTION

To receive and decrypt a secured frame from the RXFIFO, perform the following steps:

1. When a packet is received and the security enable bit = 1 in the frame control field, the MRF24J40 issues a Security Interrupt, SECIF (INTSTAT 0x31[4]). The Security Interrupt indicates to the host microcontroller that the received frame was secured. The host microcontroller can choose to decrypt or ignore the frame. The format of the received frame is shown in Example 3-22.

FIGURE 3-22: SECURITY RX FIFO FORMAT



2. If the decryption should be ignored, set the SECIGNORE (SECCON0 0x2C[7]) bit = 1. The encrypted packet can be discarded or read from the RXFIFO and processed in the upper layers.
3. The host microcontroller loads the security key into the RX FIFO Security Key memory location as shown in Table 3-25.

TABLE 3-25: DECRYPTION SECURITY KEY AND CONTROL REGISTER BITS

FIFO	Security Key Memory Address
RX FIFO	0x2B0-0x2BF

4. Select the security suite and program the RXCIPHER (SECCON0 0x2C[5:3]) bits. The security suite selection values are shown in Table 3-24.
5. Start the decryption by setting the SECSTART (SECCON0 0x2C[6]) bit = 1.
6. When the decryption process is complete, a Receive Interrupt (RXIF 0x31[3]) is issued.
7. Check the decryption status by reading SECDECERR (RXSR 0x30[2])
   SECDECERR = 0: No Decryption Error
   SECDECERR = 1: Decryption Error

Note: If decryption error has occurred and the packet in the FIFO needs to be discarded, then set RXFLUSH (RXFLUSH 0x0D[0]) bit = 1.