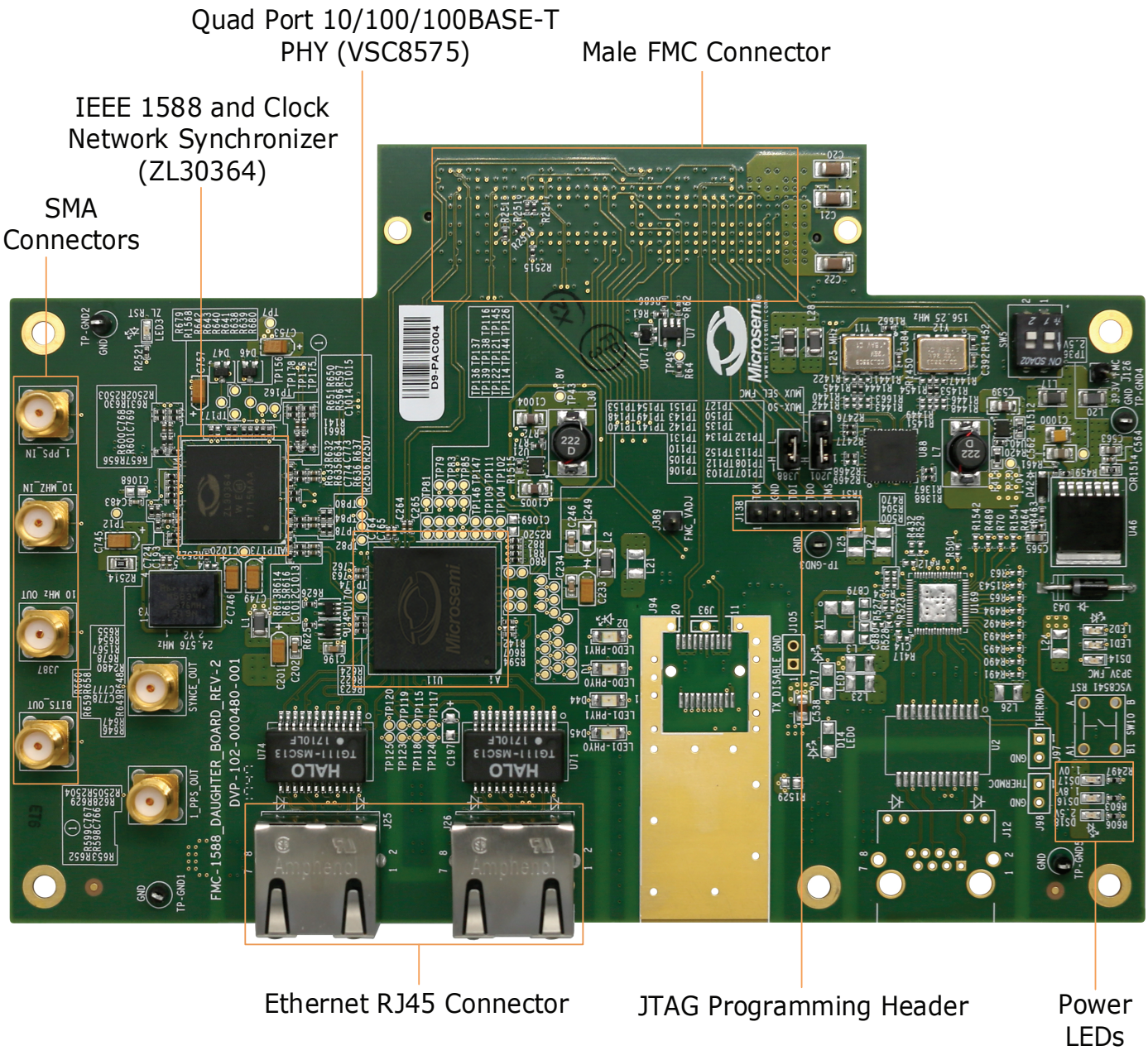
IEEE 1588 Timing Synchronization FMC Daughter Card Quickstart Card

Kit Contents—MSCC-1588-DB

Quantity	Description
1	FMC daughter card containing the ZL30363 IEEE 1588 phase-locked loop (PLL) and VSC8575 Ethernet PHY
1	Quickstart card



Overview

Microsemi IEEE™ 1588 Timing Synchronization Module (TSM) solution comprises of an IEEE 1588 FMC daughter card, software, and firmware. The solution combines best-in-class capabilities from Microsemi's broad product portfolios by leveraging the company's SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA), ZL30363 IEEE 1588 phase-locked loop (PLL), and VSC8575 Ethernet PHY devices.

Microsemi's IEEE 1588 FMC daughter card is the hardware evaluation platform for evaluating and testing the PTP engine and time-synchronization algorithm (firmware). The daughter card works with SmartFusion2 SoC FPGA Advanced Development Kit, which features the SmartFusion2 system-on-chip (SoC) field programmable gate array (FPGA) device. This kit needs to be purchased separately. This chipset runs the highly optimized IEEE 1588 protocol-compliant PTP engine and time-synchronization algorithm combined with accurate timestamping in the PHY. Customers interface to the TSM through a command line interface (CLI) through 1000BASE-X or UART communications. The solution provides nanosecond-level time stamping accuracy across network with up to 4 client/slave nodes.

Applications

IEEE 1588 technology is used across many applications, including the following:

- Mobile infrastructure
- Enterprise infrastructure
- Industrial Ethernet networking
- Defense
- Smart energy

Key Features

- Supports BC, OC-client/slave
- Up to 4 clients
- High-accuracy time stamping
- Frequency and phase synchronization
- Reference switching
- Precision frequency and phase control
- Multiple profiles, including IEEE 1588-2008 Annex J.3 End-to-End
- IEEE 1588-2008 Annex J.4 Peer-to-Peer
- IEEE C37.238-2011 Power Profile
- ITU-T G.8275.1 Telecom Profile for Phase
- ITU-T G.8265.1 Telecom Profile for Frequency

Hardware Setup

To evaluate Microsemi's IEEE 1588 Timing Synchronization Module, a two-board hardware setup is utilized. The daughter card is plugged into the SmartFusion2 SoC FPGA Advanced Development Kit (using the FMC HPC connecter on each board), which features the SmartFusion2 system-on-chip (SoC) field programmable gate array (FPGA) device. Both development boards are required and must be purchased separately.

Programming

The Smartfusion2 Advanced Development Kit must be programmed before use. An .stp file is available as part of the IEEE 1588 Timing Synchronization FMC Daughter Card download support package.

See www.microsemi.com/products/fpga-soc/design-resources/dev-kits/smartfusion2/ieee-1588-module#documentation for more information about programming procedures.

Jumper Settings

The following table lists the required jumper settings on the IEEE 1588 Timing Synchronization FMC Daughter Card.

Jumper	Setting	Comment
J201	On 1-2	3-pin header
J388	On	
DIP1	Off	
DIP2	Off	
J105		Not fitted
J97		Not fitted
J98		Not fitted

See https://www.microsemi.com/products/fpga-soc/design-resources/dev-kits/smartfusion2/ieee-1588-module#documentation for full details about jumper settings.

Running the Demo

The TSM can be set up as an OC or BC. There are example configuration files in the download support package of each configuration. Once you setup you device, you need an PTP master or slave to demo the TSM working.

If you do not have a third-party master or slave, you can use a second TSM as the master/slave.