MT9M114EBLSTCZDH-GEVB

MT9M114 Evaluation Board User's Manual

ON Semiconductor®

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EVAL BOARD USER'S MANUAL

Evaluation Board Overview

The evaluation boards are designed to demonstrate the features of ON Semiconductor's image sensors products. This headboard is intended to plug directly into the Stereo Camera system. Test points and jumpers on the board provide access to the clock, I/Os, and other miscellaneous signals.

Features

- Clock Input
  - Default – 24 MHz Crystal Oscillator
- Two Wire Serial Interface
  - Selectable Base Address
- Parallel Interface
- MIPI Interface
- ROHS Compliant

Figure 1. MT9M114 Evaluation Board

Block Diagram

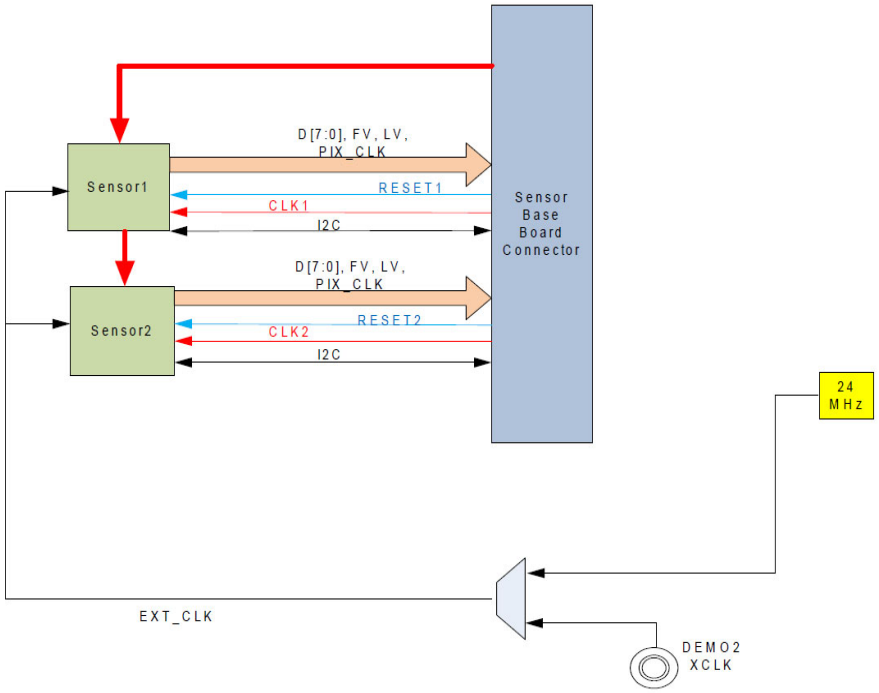

Figure 2. Block Diagram of MT9M114EBLSTCZDH–GEVB

Top View

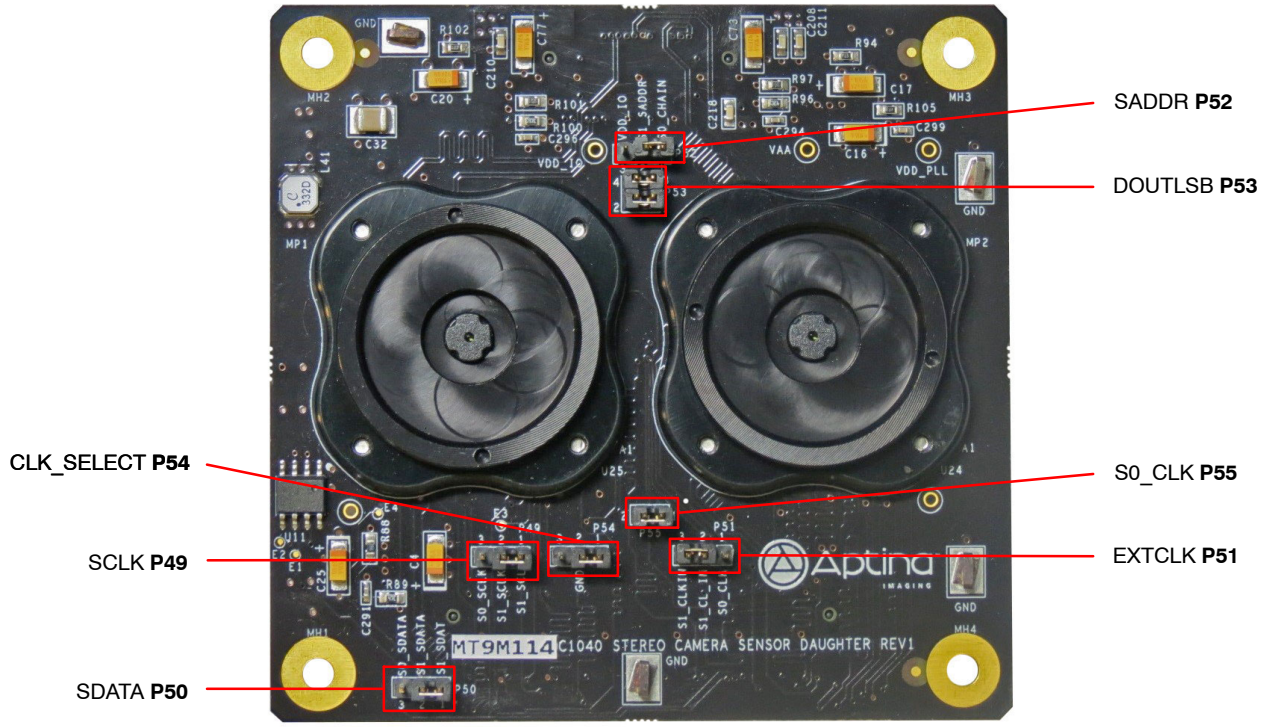

Figure 3. Top View of Evaluation Board − Default Jumpers

Bottom View

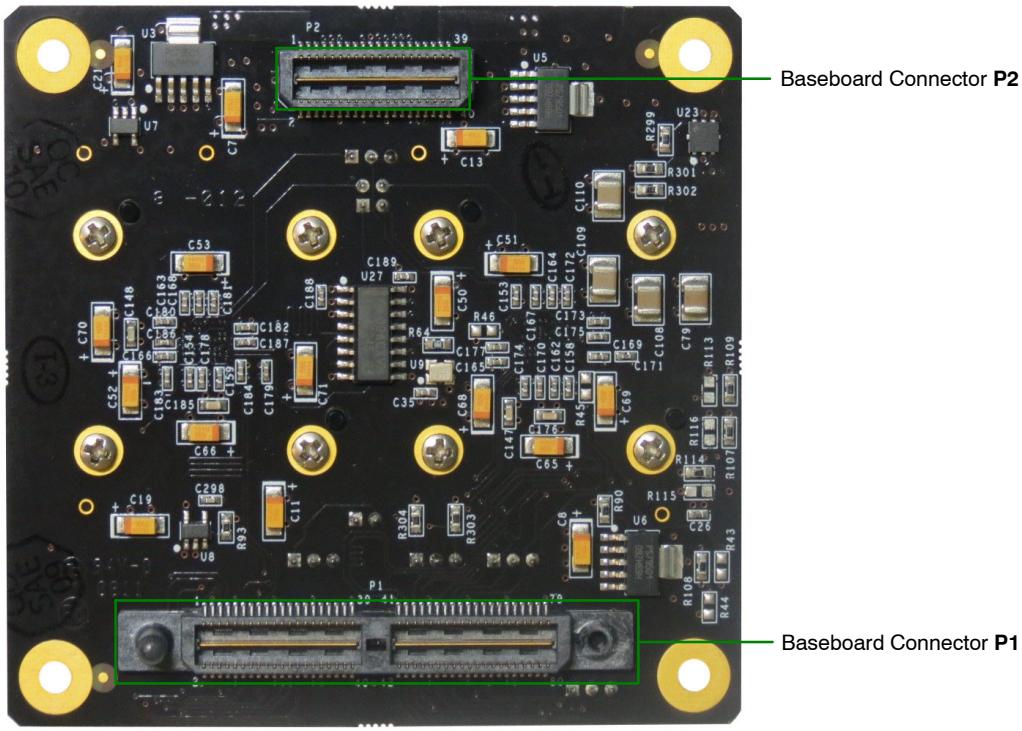

Figure 4. Bottom View of the Evaluation Board − Connectors

Jumper Pin Locations

The jumpers on headboards start with Pin 1 on the leftmost side of the pin. Grouped jumpers increase in pin size with each jumper added.

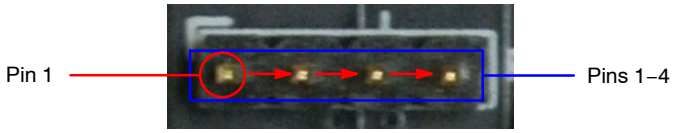

Figure 5. Pin Locations for a Single Jumper. Pin 1 is Located at the Leftmost Side and Increases as it Moves to the Right

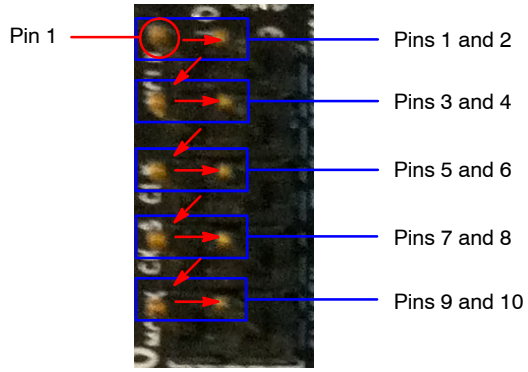

Figure 6. Pin Locations and Assignments of Grouped Jumpers. Pin 1 is Located at the Top-Left Corner and Increases in a Zigzag Fashion Shown in the Picture

Jumper/Header Functions & Default Positions

Table 1. JUMPERS AND HEADERS

Jumper/Header No.	Jumper/Header Name	Pins	Description
J5	SCLK	1−2 (Default)	SCLK set to S1_SCL
		2−3	SCLK set to S0_SCLK
P50	SDATA	1−2 (Default)	SDATA set to S1_SDAT
		2−3	S0_SDATA set to S0_SDATA
P51	EXTCLK	1−2 (Default)	EXCLK set to S1_CLKIN
		1−2	EXTCLK set to S0_CLK
P52	SADDR	1−2 (Default)	SADDR set to S0_CHAIN
		2−3	SADDR set to +VDDIO
P53	DOUTLSB	1−2, 3−4 (Default)	DOUTLSB[1:0] are used (sensor in 10-bit configuration)
		Open	DOUTLSB[1:0] are not used (sensor in 8-bit configuration)
P54	CLK_SELECT	1−2 (Default)	24 MHz oscillator to sensor external clock inputs
		2−3	FPGA clock to sensor external clock inputs
P55	S0_CLK	1−2 (Default)	S0_CLK connected to EXTCLK
		Open	External connection to EXTCLK

Interfacing to ON Semiconductor Stereo Camera Baseboard

The ON Semiconductor Stereo Camera baseboard has a similar 88-pin connector and 44-pin connector which mate with P1 and P2 of the headboard. The four mounting holes secure the baseboard and the headboard with spacers and screws.