

# DDR4 SDRAM RDIMM Addendum

## MTA18ASF4G72PDZ – 32GB

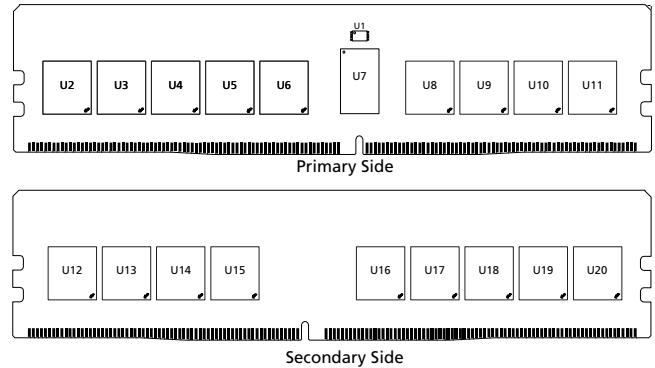
### Introduction

Information provided here is in addition to or supersedes information provided in the Micron DDR4 RDIMM Core data sheet.

### Features

- DDR4 functionality and operations supported as defined in the component data sheet
- Features and specifications defined in the Micron DDR4 RDIMM core data sheet
- 288-pin, registered dual in-line memory module (RDIMM)
- Fast data transfer rates: PC4-3200, PC4-2933
- 32GB (4 Gig × 72)
- Data bus inversion (DBI) for data bus
- Dual-rank
- 16 internal banks; 4 groups of 4 banks each

**Figure 1: 288-Pin RDIMM (MO-309, R/C-E3)**



### Options

- Operating temperature
  - Commercial ( $0^{\circ}\text{C} \leq T_{\text{OPER}} \leq 95^{\circ}\text{C}$ )
- Package
  - 288-pin DIMM (Green)
- Frequency/CAS latency
  - 0.625ns @ CL = 22 (DDR4-3200)
  - 0.682ns @ CL = 21 (DDR4-2933)

### Marking

- None
- Z
- 3G2
- 2G9

**Table 1: Addressing**

Parameter	32GB
Row address	128K A[16:0]
Column address	1K A[9:0]
Device bank group address	4 BG[1:0]
Device bank address per group	4 BA[1:0]
Device configuration	16Gb (2 Gig × 8), 16 banks
Module rank address	2 CS_n[1:0]

**Table 2: Part Numbers and Timing Parameters – 32GB Modules**

Base device: MT40A2G8,<sup>1</sup> 16Gb DDR4 SDRAM

Part Number <sup>2</sup>	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-nRCD-nRP)
MTA18ASF4G72PDZ-3G2__	32GB	4 Gig × 72	25.6 GB/s	0.625ns/3200 MT/s	22-22-22
MTA18ASF4G72PDZ-2G9__	32GB	4 Gig × 72	23.47 GB/s	0.682ns/2933 MT/s	21-21-21

- Notes:
1. The data sheet for the base device can be found on [micron.com](http://micron.com).
  2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MTA18ASF4G72PDZ-3G2B1.

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## DQ Map

Table 3: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U2	0	3	157	U3	0	11	168
	1	0	5		1	8	16
	2	2	12		2	10	23
	3	1	150		3	9	161
	4	7	155		4	15	166
	5	4	3		5	12	14
	6	6	10		6	14	21
	7	5	148		7	13	159
U4	0	19	179	U5	0	27	190
	1	16	27		1	24	38
	2	18	34		2	26	45
	3	17	172		3	25	183
	4	23	177		4	31	188
	5	20	25		5	28	36
	6	22	32		6	30	43
	7	21	170		7	29	181
U6	0	CB3	201	U8	0	35	249
	1	CB0	49		1	32	97
	2	CB2	56		2	34	104
	3	CB1	194		3	33	242
	4	CB7	199		4	39	247
	5	CB4	47		5	36	95
	6	CB6	54		6	38	102
	7	CB5	192		7	37	240
U9	0	43	260	U10	0	51	271
	1	40	108		1	48	119
	2	42	115		2	50	126
	3	41	253		3	49	264
	4	47	258		4	55	269
	5	44	106		5	52	117
	6	46	113		6	54	124
	7	45	251		7	53	262
U11	0	59	282	U12	0	56	130
	1	56	130		1	59	282
	2	58	137		2	57	275
	3	57	275		3	58	137
	4	63	280		4	60	128
	5	60	128		5	63	280
	6	62	135		6	61	273
	7	61	273		7	62	135



**Table 3: Component-to-Module DQ Map (Continued)**

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U13	0	48	119	U14	0	40	108
	1	51	271		1	43	260
	2	49	264		2	41	253
	3	50	126		3	42	115
	4	52	117		4	44	106
	5	55	269		5	47	258
	6	53	262		6	45	251
	7	54	124		7	46	113
U15	0	32	97	U16	0	CB0	49
	1	35	249		1	CB3	201
	2	33	242		2	CB1	194
	3	34	104		3	CB2	56
	4	36	95		4	CB4	47
	5	39	247		5	CB7	199
	6	37	240		6	CB5	192
	7	38	102		7	CB6	54
U17	0	24	38	U18	0	16	27
	1	27	190		1	19	179
	2	25	183		2	17	172
	3	26	45		3	18	34
	4	28	36		4	20	25
	5	31	188		5	23	177
	6	29	181		6	21	170
	7	30	43		7	22	32
U19	0	8	16	U20	0	0	5
	1	11	168		1	3	157
	2	9	161		2	1	150
	3	10	23		3	2	12
	4	12	14		4	4	3
	5	15	166		5	7	155
	6	13	159		6	5	148
	7	14	21		7	6	10

## I<sub>DD</sub> Specifications

**Table 4: DDR4 I<sub>DD</sub> Specifications and Conditions – 32GB (Die Revision E)**

Values are for the MT40A2G8 DDR4 SDRAM only and are computed from values specified in the 16Gb (2 Gig × 8) component data sheet.

Parameter	Symbol	3200	2933	Units
One bank ACTIVATE-PRECHARGE current	I <sub>DD0</sub> <sup>1</sup>	882	873	mA
One bank ACTIVATE-PRECHARGE, wordline boost, I <sub>pp</sub> current	I <sub>PP0</sub> <sup>1</sup>	45	45	mA
One bank ACTIVATE-READ-PRECHARGE current	I <sub>DD1</sub> <sup>1</sup>	981	972	mA
Precharge standby current	I <sub>DD2N</sub> <sup>2</sup>	810	792	mA
Precharge standby ODT current	I <sub>DD2NT</sub> <sup>1</sup>	801	792	mA
Precharge power-down current	I <sub>DD2P</sub> <sup>2</sup>	684	684	mA
Precharge quite standby current	I <sub>DD2Q</sub> <sup>2</sup>	756	756	mA
Active standby current	I <sub>DD3N</sub> <sup>2</sup>	1098	1080	mA
Active standby I <sub>pp</sub> current	I <sub>PP3N</sub> <sup>2</sup>	36	36	mA
Active power-down current	I <sub>DD3P</sub> <sup>2</sup>	900	882	mA
Burst read current	I <sub>DD4R</sub> <sup>1</sup>	1800	1728	mA
Burst write current	I <sub>DD4W</sub> <sup>1</sup>	1494	1449	mA
Different logic rank burst refresh current (1x REF)	I <sub>DD5R</sub> <sup>1</sup>	954	954	mA
Different logic rank burst refresh I <sub>pp</sub> current (1x REF)	I <sub>PP5R</sub> <sup>1</sup>	54	54	mA
Self refresh current: Normal temperature range (0°C to 85°C)	I <sub>DD6N (0-85°C)</sub> <sup>2</sup>	954	954	mA
Self refresh current: Extended temperature range (0°C to 95°C)	I <sub>DD6E (0-95°C)</sub> <sup>2</sup>	2034	2034	mA
Self refresh current: Reduced temperature range (0°C to 45°C)	I <sub>DD6R (0-45°C)</sub> <sup>2</sup>	360	360	mA
Auto self refresh current (25°C)	I <sub>DD6A (25°C)</sub> <sup>2</sup>	198	198	mA
Auto self refresh current (45°C)	I <sub>DD6A (45°C)</sub> <sup>2</sup>	360	360	mA
Auto self refresh current (75°C)	I <sub>DD6A (75°C)</sub> <sup>2</sup>	918	918	mA
Auto self refresh current (95°C)	I <sub>DD6A (95°C)</sub> <sup>2</sup>	2034	2034	mA
Auto self refresh I <sub>pp</sub> current (0°C to 95°C)	I <sub>PP6X</sub> <sup>2</sup>	108	108	mA
Bank interleave read current	I <sub>DD7</sub> <sup>1</sup>	2007	1989	mA
Bank interleave read I <sub>pp</sub> current	I <sub>PP7</sub> <sup>1</sup>	144	144	mA
Maximum power-down current	I <sub>DD8</sub> <sup>2</sup>	648	648	mA

- Notes: 1. One module rank in the active I<sub>DD/PP</sub>, the other rank in I<sub>DD2P/PP3N</sub>.  
2. All ranks in this I<sub>DD/PP</sub> condition.

**Table 5: DDR4 I<sub>DD</sub> Specifications and Conditions – 32GB (Die Revision B)**

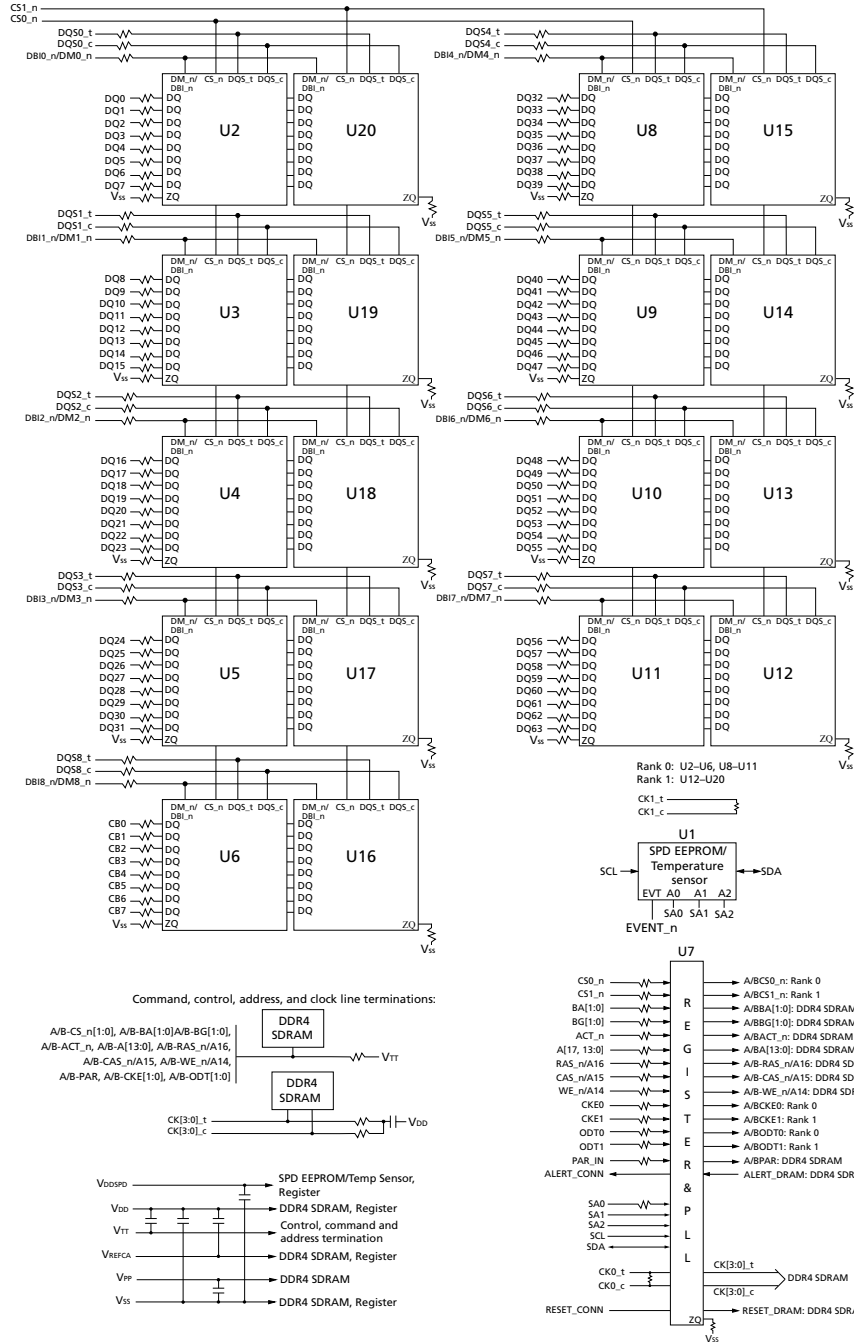
Values are for the MT40A2G8 DDR4 SDRAM only and are computed from values specified in the 16Gb (2 Gig x 8) component data sheet.

Parameter	Symbol	3200	2933	Units
One bank ACTIVATE-PRECHARGE current	I <sub>DD0</sub> <sup>1</sup>	954	945	mA
One bank ACTIVATE-PRECHARGE, wordline boost, I <sub>PP</sub> current	I <sub>PP0</sub> <sup>1</sup>	63	63	mA
One bank ACTIVATE-READ-PRECHARGE current	I <sub>DD1</sub> <sup>1</sup>	1053	1044	mA
Precharge standby current	I <sub>DD2N</sub> <sup>2</sup>	936	918	mA
Precharge standby ODT current	I <sub>DD2NT</sub> <sup>1</sup>	891	882	mA
Precharge power-down current	I <sub>DD2P</sub> <sup>2</sup>	774	774	mA
Precharge quite standby current	I <sub>DD2Q</sub> <sup>2</sup>	846	846	mA
Active standby current	I <sub>DD3N</sub> <sup>2</sup>	1440	1422	mA
Active standby I <sub>PP</sub> current	I <sub>PP3N</sub> <sup>2</sup>	54	54	mA
Active power-down current	I <sub>DD3P</sub> <sup>2</sup>	1242	1242	mA
Burst read current	I <sub>DD4R</sub> <sup>1</sup>	2205	2115	mA
Burst write current	I <sub>DD4W</sub> <sup>1</sup>	2034	1962	mA
Different logic rank burst refresh current (1x REF)	I <sub>DD5R</sub> <sup>1</sup>	1098	1089	mA
Different logic rank burst refresh I <sub>PP</sub> current (1x REF)	I <sub>PP5R</sub> <sup>1</sup>	72	72	mA
Self refresh current: Normal temperature range (0°C to 85°C)	I <sub>DD6N (0-85°C)</sub> <sup>2</sup>	1206	1206	mA
Self refresh current: Extended temperature range (0°C to 95°C)	I <sub>DD6E (0-95°C)</sub> <sup>2</sup>	2178	2178	mA
Self refresh current: Reduced temperature range (0°C to 45°C)	I <sub>DD6R (0-45°C)</sub> <sup>2</sup>	522	522	mA
Auto self refresh current (25°C)	I <sub>DD6A (25°C)</sub> <sup>2</sup>	180	180	mA
Auto self refresh current (45°C)	I <sub>DD6A (45°C)</sub> <sup>2</sup>	522	522	mA
Auto self refresh current (75°C)	I <sub>DD6A (75°C)</sub> <sup>2</sup>	1098	1098	mA
Auto self refresh current (95°C)	I <sub>DD6A (95°C)</sub> <sup>2</sup>	2178	2178	mA
Auto self refresh I <sub>PP</sub> current (0°C to 95°C)	I <sub>PP6X</sub> <sup>2</sup>	198	198	mA
Bank interleave read current	I <sub>DD7</sub> <sup>1</sup>	2151	2124	mA
Bank interleave read I <sub>PP</sub> current	I <sub>PP7</sub> <sup>1</sup>	117	117	mA
Maximum power-down current	I <sub>DD8</sub> <sup>2</sup>	720	720	mA

- Notes: 1. One module rank in the active I<sub>DD/PP</sub>, the other rank in I<sub>DD2P/PP3N</sub>.  
2. All ranks in this I<sub>DD/PP</sub> condition.

## Functional Block Diagram

Figure 2: Functional Block Diagram



**Note:** 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.