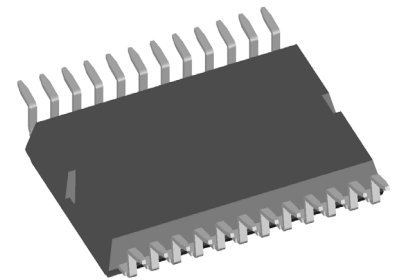


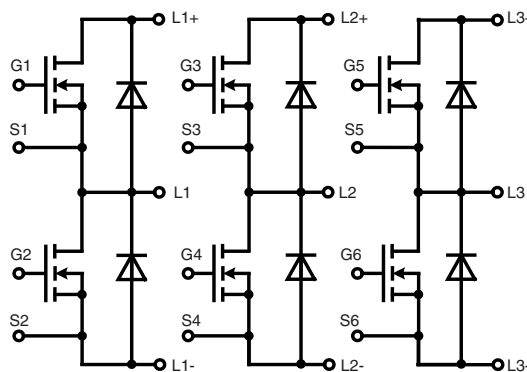
Three phase full Bridge with Trench MOSFETs in DCB-isolated high-current package

$V_{DSS} = 100\text{ V}$
 $I_{D25} = 190\text{ A}$
 $R_{DSon\ typ.} = 1.7\text{ m}\Omega$

Part number
MTI145WX100GD



Surface Mount Device



Features / Advantages:

- MOSFETs in trench technology:
 - low R_{DSon}
 - optimized intrinsic reverse diode
- Package:
 - high level of integration
 - high current capability
 - aux. terminals for MOSFET control
 - terminals for soldering or welding connections
 - isolated DCB ceramic base plate with optimized heat transfer
- Space and weight savings

Applications:

- AC drives
- in automobiles
 - electric power steering
 - starter generator
 - in industrial vehicles
 - propulsion drives
 - fork lift drives
 - in battery supplied equipment

Package: ISOPLUS-DIL®

- High level of integration
- RoHS compliant
- High current capability
- Aux. Terminals for MOSFET control
- Terminals for soldering or welding connections
- Space and weight savings

Terms & Conditions of usage

The data contained in this product data sheet is exclusively intended for technically trained staff. The user will have to evaluate the suitability of the product for the intended application and the completeness of the product data with respect to his application. The specifications of our components may not be considered as an assurance of component characteristics. The information in the valid application- and assembly notes must be considered. Should you require product information in excess of the data given in this product data sheet or which concerns the specific application of your product, please contact your local sales office.

Due to technical requirements our product may contain dangerous substances. For information on the types in question please contact your local sales office.

Should you intend to use the product in aviation, in health or life endangering or life support applications, please notify. For any such application we urgently recommend

- to perform joint risk and quality assessments;

- the conclusion of quality agreements;

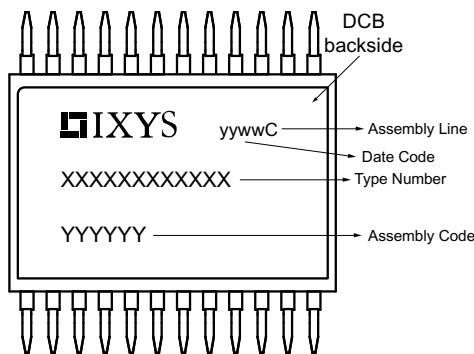
- to establish joint measures of an ongoing product survey, and that we may make delivery dependent on the realization of any such measures.

IXYS reserves the right to change limits, test conditions and dimensions.

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MOSFETs				Ratings			
Symbol	Definitions	Conditions	min.	typ.	max.	Unit	
V_{DSS}	drain source breakdown voltage	$T_{VJ} = 25^{\circ}\text{C to } 150^{\circ}\text{C}$			100	V	
V_{GS}	gate source voltage				± 15	V	
V_{GSM}	max. transient gate source voltage				± 20	V	
I_{D25}	continuous drain current	$T_C = 25^{\circ}\text{C}$			190	A	
I_{D90}		$T_C = 90^{\circ}\text{C}$			145	A	
$R_{DS(on)}^{1)}$	static drain source on resistance	on chip level at $I_D = 100\text{ A}; V_{GS} = 10\text{ V}$	$T_{VJ} = 25^{\circ}\text{C}$ $T_{VJ} = 125^{\circ}\text{C}$	1.7 2.9	2.2	m Ω m Ω	
$V_{GS(th)}$	gate threshold voltage	$I_D = 275\ \mu\text{A}; V_{DS} = V_{GS}$	$T_{VJ} = 25^{\circ}\text{C}$	2.0	2.7	3.5	V
I_{DSS}	drain source leakage current	$V_{DS} = V_{DSS}; V_{GS} = 0\text{ V}$	$T_{VJ} = 25^{\circ}\text{C}$ $T_{VJ} = 125^{\circ}\text{C}$		1 100	μA μA	
I_{GSS}	gate source leakage current	$V_{GS} = \pm 20\text{ V}; V_{DS} = 0\text{ V}$			500	nA	
R_G	gate resistance	on chip level		1.9		Ω	
C_{iss}	input capacitance	} $V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}; f = 1\text{ Mhz}$		11.1		nF	
C_{oss}	output capacitance			1.94		nF	
C_{rss}	reverse transfer capacitance			70		pF	
Q_g	total gate charge	} $V_{GS} = 10\text{ V}; V_{DS} = 50\text{ V}; I_D = 100\text{ A}$		155		nC	
Q_{gs}	gate source charge			48		nC	
Q_{gd}	gate drain (Miller) charge			27		nC	
$t_{d(on)}$	turn-on delay time	} inductive load $V_{GS} = 10\text{ V}; V_{DS} = 50\text{ V}$ $I_D = 100\text{ A}; R_G = 27\ \Omega$	$T_{VJ} = 125^{\circ}\text{C}$		135	ns	
t_r	current rise time				75	ns	
$t_{d(off)}$	turn-off delay time				600	ns	
t_f	current fall time				40	ns	
E_{on}	turn-on energy per pulse				200	μJ	
E_{off}	turn-off energy per pulse				600	μJ	
$E_{rec(off)}$	turn-off reverse recovery losses		36	μJ			
R_{thJC}	thermal resistance junction to case				0.85	K/W	
R_{thJH}	thermal resistance junction to heatsink	with heat transfer paste (IXYS test setup)		1.1	1.4	K/W	
$^1) V_{DS} = I_D \cdot (R_{DS(on)} + 2 \cdot R_{Pin\ to\ Chip})$							
Source-Drain Diode							
I_{F25}	forward current		$T_C = 25^{\circ}\text{C}$		180	A	
I_{F90}			$T_C = 90^{\circ}\text{C}$		105	A	
V_{SD}	source drain voltage	$I_F = 100\text{ A}; V_{GS} = 0\text{ V}$	$T_{VJ} = 25^{\circ}\text{C}$	0.9	1.2	V	
Q_{RM}	reverse recovery charge	} $V_R = 50\text{ V}; I_F = 100\text{ A}$ $R_G = 27\ \Omega$ (di/dt = 1700 A/ μs)	$T_{VJ} = 125^{\circ}\text{C}$		2	μC	
I_{RM}	max. reverse recovery current				54	A	
t_{rr}	reverse recovery time				60	ns	

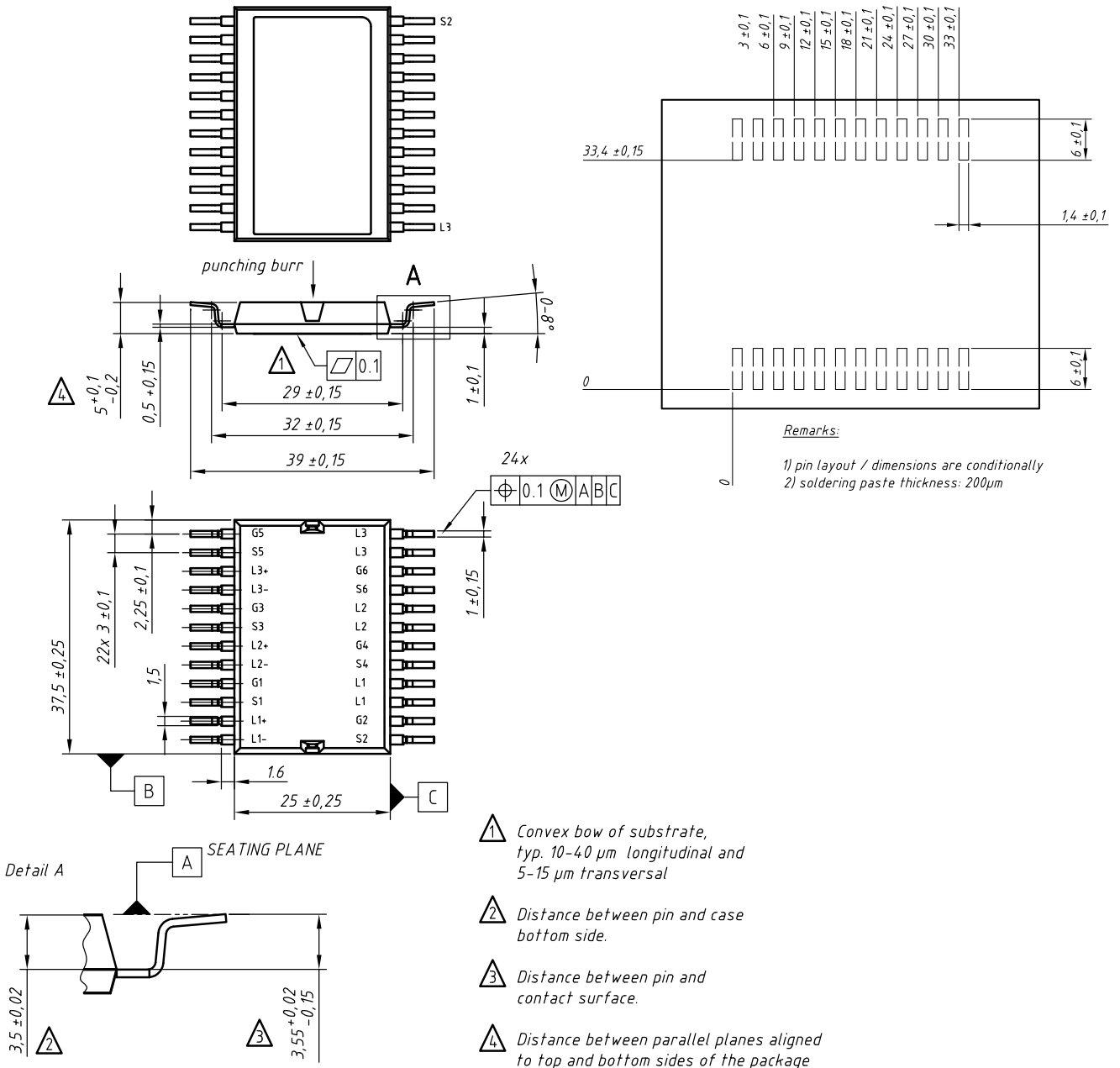
Package ISOPLUS-DIL®			Ratings			
Symbol	Definitions	Conditions	min.	typ.	max.	Unit
I_{RMS}	RMS current	per pin in main current paths (L1+...L3+, L1-...L3-, L1...L3) may be additionally limited by external connections (PCB tracks) 2 pins for output L1, L2, L3			75	A
T_{stg}	storage temperature		-55		125	°C
T_{op}	operation temperature		-55		150	°C
T_{VJ}	virtual junction temperature		-55		175	°C
Weight				13		g
F_C	mounting force with clip		50		250	N
V_{ISOL}	isolation voltage	$t = 1$ second	50/60 Hz, RMS, $I_{ISOL} \leq 1$ mA	1200		V
		$t = 1$ minute		1000		V
$R_{pin-chip}$	resistance terminal to chip	$V_{DS} = I_D \cdot (R_{DS(on)} + 2 \cdot R_{pin\ to\ chip})$		0.5		mΩ
C_P	coupling capacity	between shorted pins and back side metallization		160		pF


Part number

- M = MOSFET
- T = Trench
- I = Infineon Trench
- 145 = Current Rating [A]
- WX = 6-Pack with separated Phase Legs
- 100 = Reverse Voltage [V]
- GD = ISOPLUS-DIL

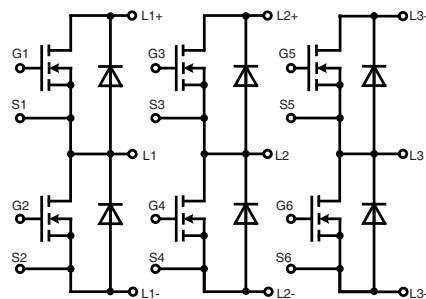
Ordering	Part Name	Marking on Product	Delivering Mode	Base Qty	Ordering Code
Standard	MTI145WX100GD-SMD	MTI145WX100GD	Tube	13	518023

Outlines ISOPLUS-DIL®



contact pin:

- galv. tin plating, per pin side: Sn 10...25 μm, undercoating Ni 0,2...1 μm
- stamping edges may be free of tin
- punching burr: ≤ 0,05mm



IXYS reserves the right to change limits, test conditions and dimensions.

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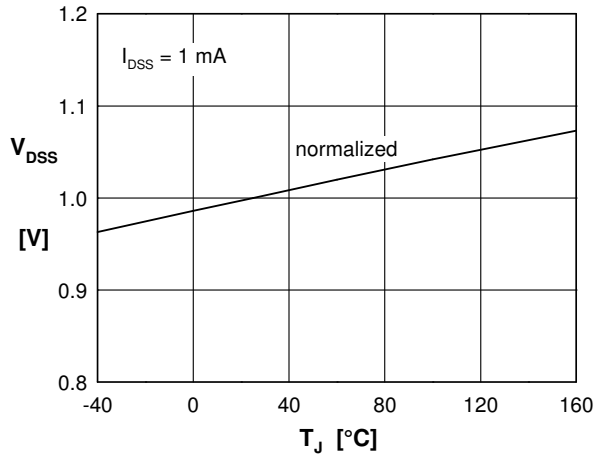


Fig. 1 Drain source breakdown voltage V_{DSS} vs. junction temperature T_{VJ}

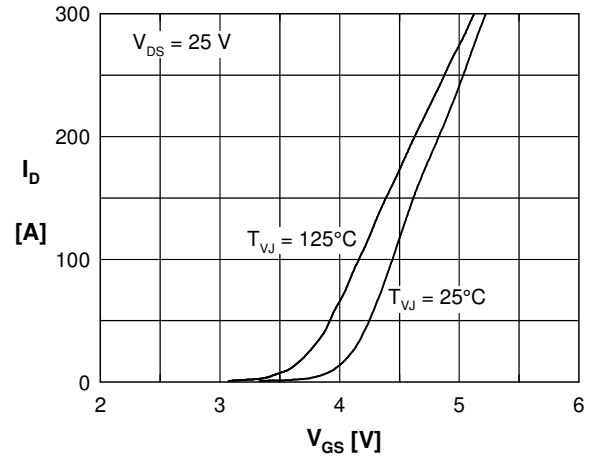


Fig. 2 Typ. transfer characteristics

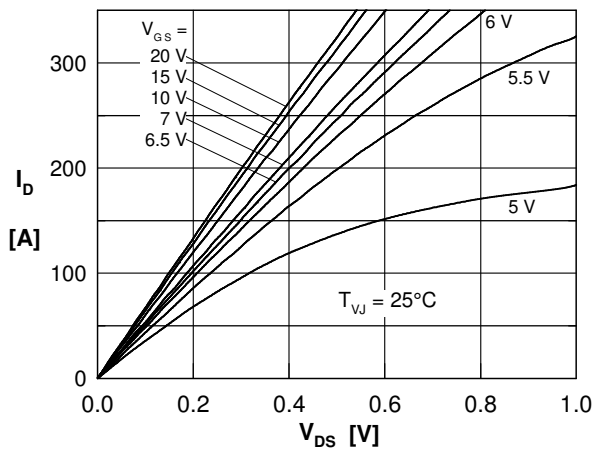


Fig. 3 Typ. output characteristics on die level

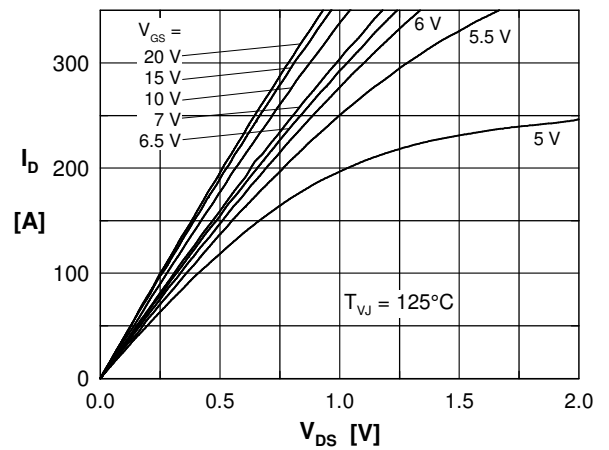


Fig. 4 Typ. output characteristics on die level

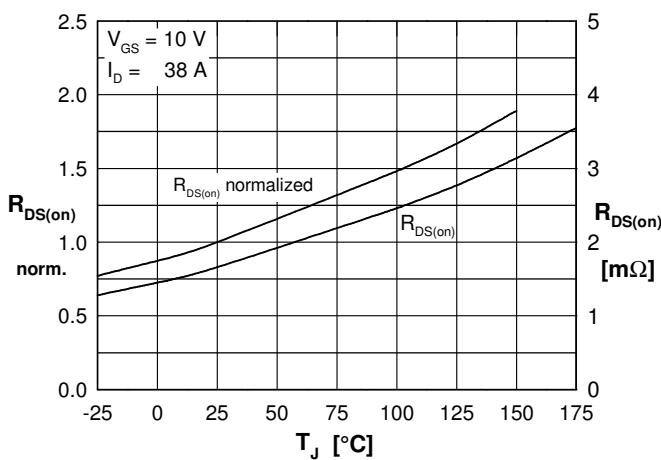


Fig. 5 Drain source on-state resistance $R_{DS(on)}$ vs. junction temperature T_{VJ} , on die level

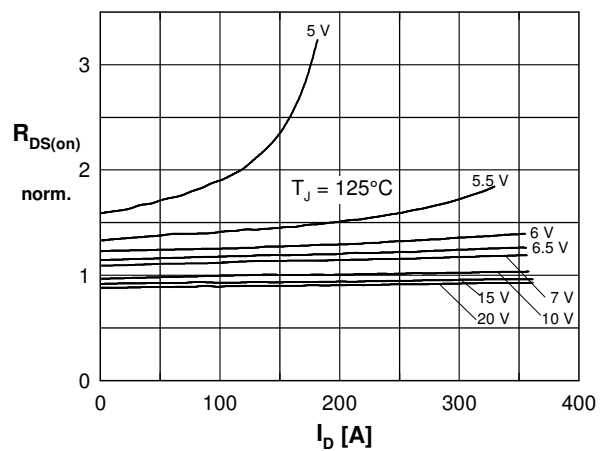


Fig. 6 Drain source on-state resistance $R_{DS(on)}$ versus I_D , on die level

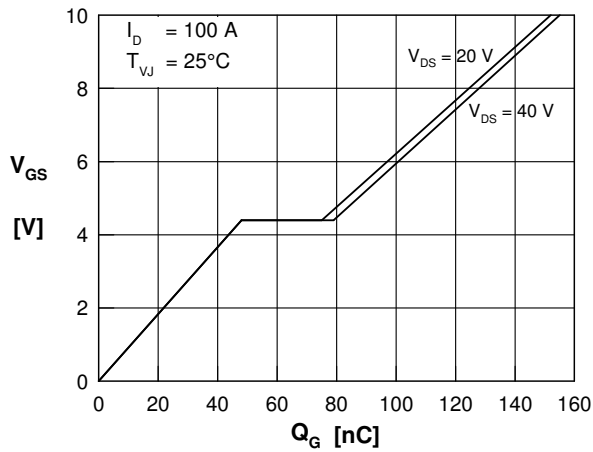


Fig. 7 Typical turn on gate charge

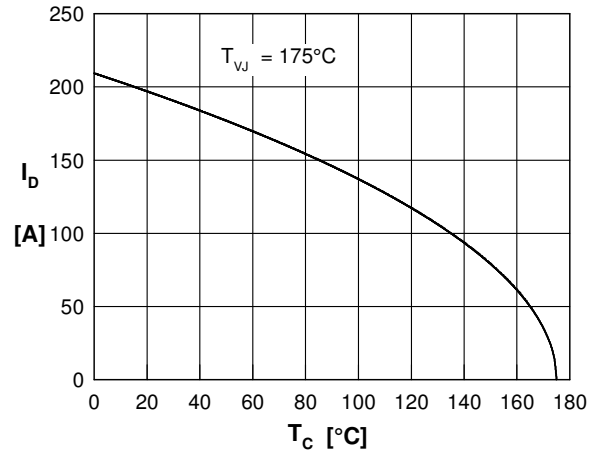


Fig. 8 Drain current I_D vs. case temperature T_C (Chip capability)

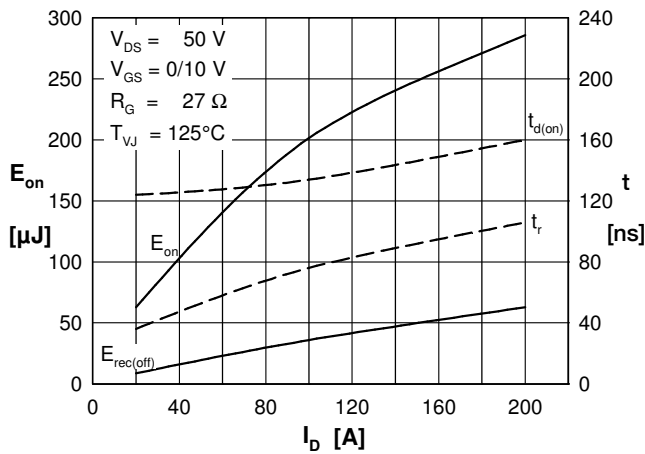


Fig. 9 Typ. turn-on energy and switching times versus drain current, inductive switching

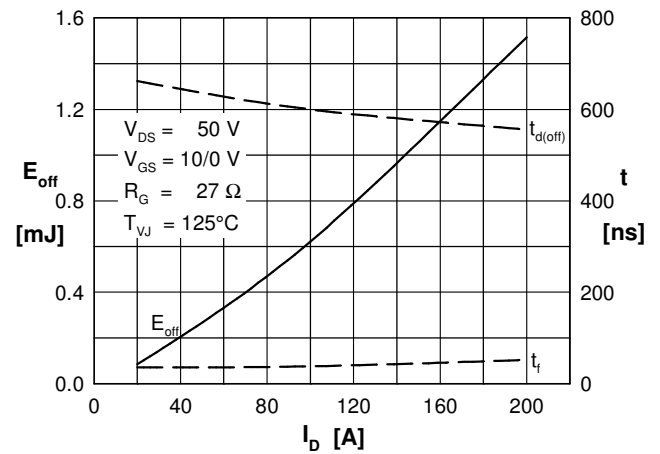


Fig. 10 Typ. turn-off energy and switching times versus drain-current, inductive switching

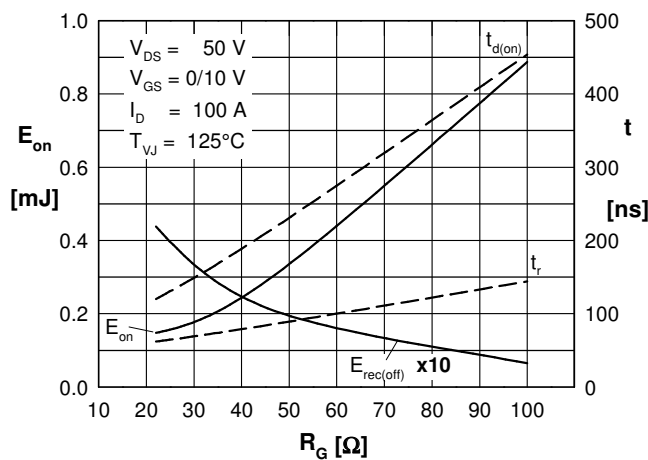


Fig. 11 Typ. turn-on energy and switching times versus gate resistor, inductive switching

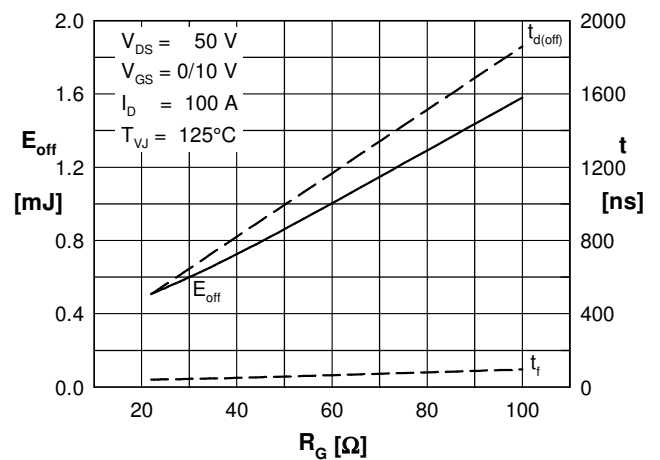


Fig. 12 Typ. turn-off energy and switching times versus gate resistor, inductive switching