VR5510

Multi-Output PMIC with SMPS and LDO

Rev. 4 — 6 October 2021 Product data sheet

1 General Description

The VR5510 is an automotive multi-output power management IC that focuses on Gateway, In-Vehicle Networks, Domain controllers, Telematics and V2X Communications. The device includes multiple high-efficiency switch modes and linear voltage regulators. It offers external frequency synchronization on inputs and outputs for optimized system EMC performance.

The VR5510 includes enhanced safety features with fail-safe outputs. The device covers ASIL B and ASIL D safety integrity levels. It complies with the ISO 26262 standard and is qualified in accordance with AEC-Q100 rev H (Grade1, MSL3). The VR5510 can be fully utilized in safety-oriented system partitioning and can also be configured to operate as a nonsafety QM-version part.

The VR5510 is available in several versions that support a variety of safety applications and offer numerous choices with respect to the number of output rails, output voltage settings, operating frequencies, and power-up sequencing.

2 Simplified Application Diagram

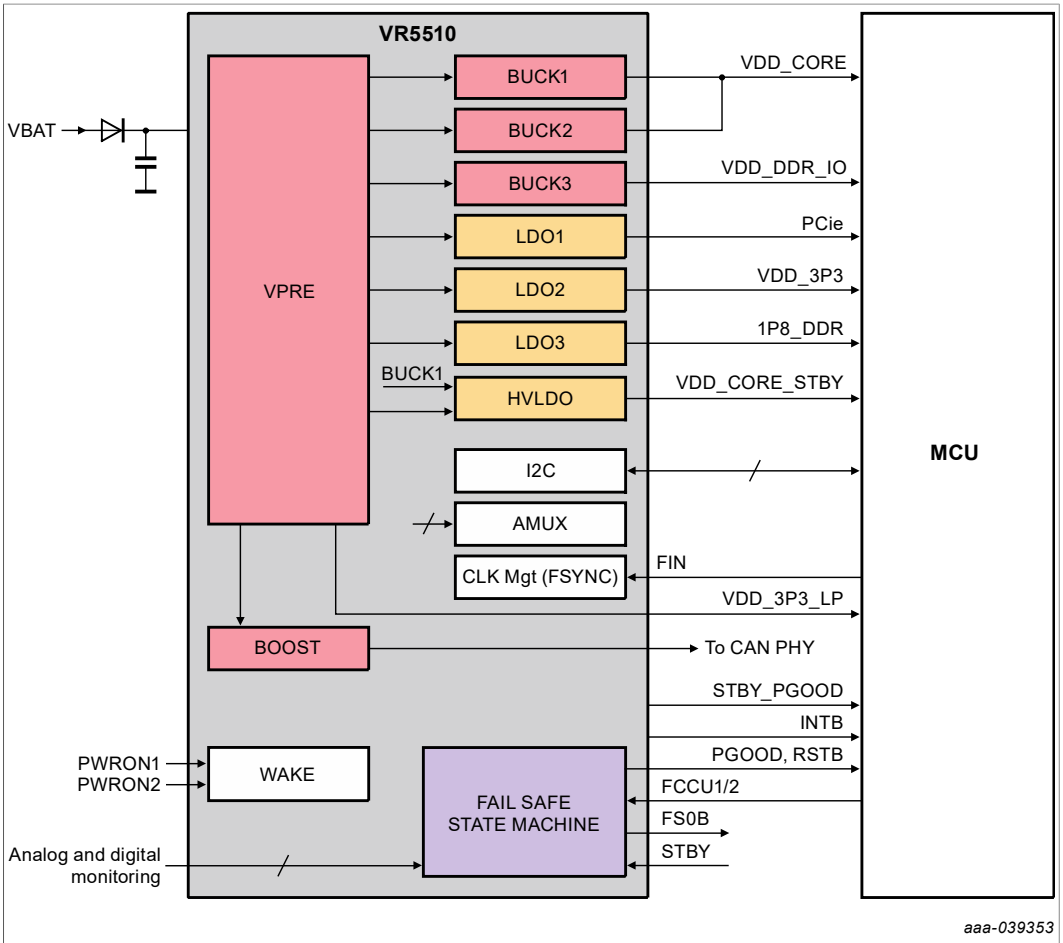


Figure 1. VR5510 simplified application diagram

3 Features and Benefits

- 60 VDC maximum input voltage
- VPRE synchronous buck controller with external MOSFETs; Configurable output voltage, switching frequency, and current capability up to 10 A
- Low-voltage integrated synchronous BUCK1 and BUCK2 converters dedicated to MCU core supply with SVS/DVS capability; Configurable output voltage and current capability up to 3.6 A peak; Dual-phase operation to extend the current capability up to 7.2 A peak
- Low-voltage integrated synchronous BUCK3 converter; Configurable output voltage and current capability up to 3.6 A peak
- BOOST converter with integrated low-side switch; Configurable output voltage and input current capability up to 2.25 A peak
- 3x linear voltage regulators (LDOx) for MCU IOs, DDR and ADC supplies; Configurable output voltage and current capability up to 400 mA
- High-voltage linear regulator (HVLDO) with current capability up to 10 mA in LDO mode and 100 mA in Switch Mode

- EMC optimization techniques, including SMPS frequency synchronization, spread spectrum, slew rate control, manual frequency tuning
- Low-power standby mode with very low quiescent current (35 µA with VPRE and HVLDO ON)
- 2x input pins for wake-up detection and battery voltage sense
- Device control via I^2C interface with CRC (up to 3.4 MHz)
- Dual device operation possible via dedicated synchronization pin
- Scalable portfolio from QM to ASIL B to ASIL D with Independent Monitoring Circuitry, dedicated interface for MCU monitoring, simple and challenger watchdog function, Power good, Reset and Interrupt, Built-in Self-Test, Fail-safe output
- Configuration by OTP programming; Prototype enablement to support custom setting during project development in engineering mode

4 Applications

- Gateway
- In-Vehicle Networks
- Domain controllers
- Telematics
- V2X Communications

5 Ordering Information

Table 1 shows the VR5510 part numbers available for purchase and highlights the key features associated with each part.

Table 1. Orderable parts

Family	Part Number [1][2][3]	Processor/ memory	Reference design	Safety Level	Auto / Indus	OTP ID
VR5510 [2]	MVR5510AMDA0ES	Nonprogrammed		ASIL D	Auto[4]	NA
	MVR5510AMBA0ES	Nonprogrammed		ASIL B	Auto	NA
	MVR5510AMMA0ES	Nonprogrammed		QM	Auto	NA
	MVR5510AVMA0EP	Nonprogrammed		QM	Indus[4]	NA
	MVR5510AMDA4ES	S32G / LPDDR4	S32G-V NP-RDB	ASIL D	Auto	http://www.nxp.com/MVR5510AMDA4ES-OTP-Report
	MVR5510AMBA4ES	S32G / LPDDR4	S32G-V NP-RDB	ASIL B	Auto	http://www.nxp.com/MVR5510AMBA4ES-OTP-Report
	MVR5510AMMA4ES	S32G / LPDDR4		QM	Auto	http://www.nxp.com/MVR5510AMMA4ES-OTP-Report
	MVR5510AVMA4EP	S32G / LPDDR4		QM	Indus	http://www.nxp.com/MVR5510AVMA4EP-OTP-Report
	MVR5510AMDAHES	S32G / LPDDR4	S32G-VN P-RDB2	ASIL D	Auto	http://www.nxp.com/MVR5510AMDAHES-OTP-Report
	MVR5510AMBAHES	S32G / LPDDR4	S32G-VN P-RDB2	ASIL B	Auto	http://www.nxp.com/MVR5510AMBAHES-OTP-Report
	MVR5510AMMAHES	S32G / LPDDR4		QM	Auto	http://www.nxp.com/MVR5510AMMAHES-OTP-Report
	MVR5510AVMAHEP	S32G / LPDDR4		QM	Indus	http://www.nxp.com/MVR5510AVMAHEP-OTP-Report

Table 1. Orderable parts...*continued*

Family	Part Number [1][2][3]	Processor/ memory	Reference design	Safety Level	Auto / Indus	OTP ID
	MVR5510AMDA6ES	S32G / DDR3L		ASIL D	Auto	http://www.nxp.com/MVR5510AMDA6ES-OTP-Report
	MVR5510AMBA6ES	S32G / DDR3L		ASIL B	Auto	http://www.nxp.com/MVR5510AMBA6ES-OTP-Report
	MVR5510AMMA6ES	S32G / DDR3L		QM	Auto	http://www.nxp.com/MVR5510AMMA6ES-OTP-Report
	MVR5510AVMA6EP	S32G / DDR3L		QM	Indus	http://www.nxp.com/MVR5510AVMA6EP-OTP-Report

[1] Part number delivery suffix: add R2 for tape & reel
[2] P are Prerelease parts, M are Production parts
[3] 8x8 56-pin QFN-EP
[4] Automotive package available as wettable flank; Industrial package not available as wettable flank

6 Internal Block Diagram

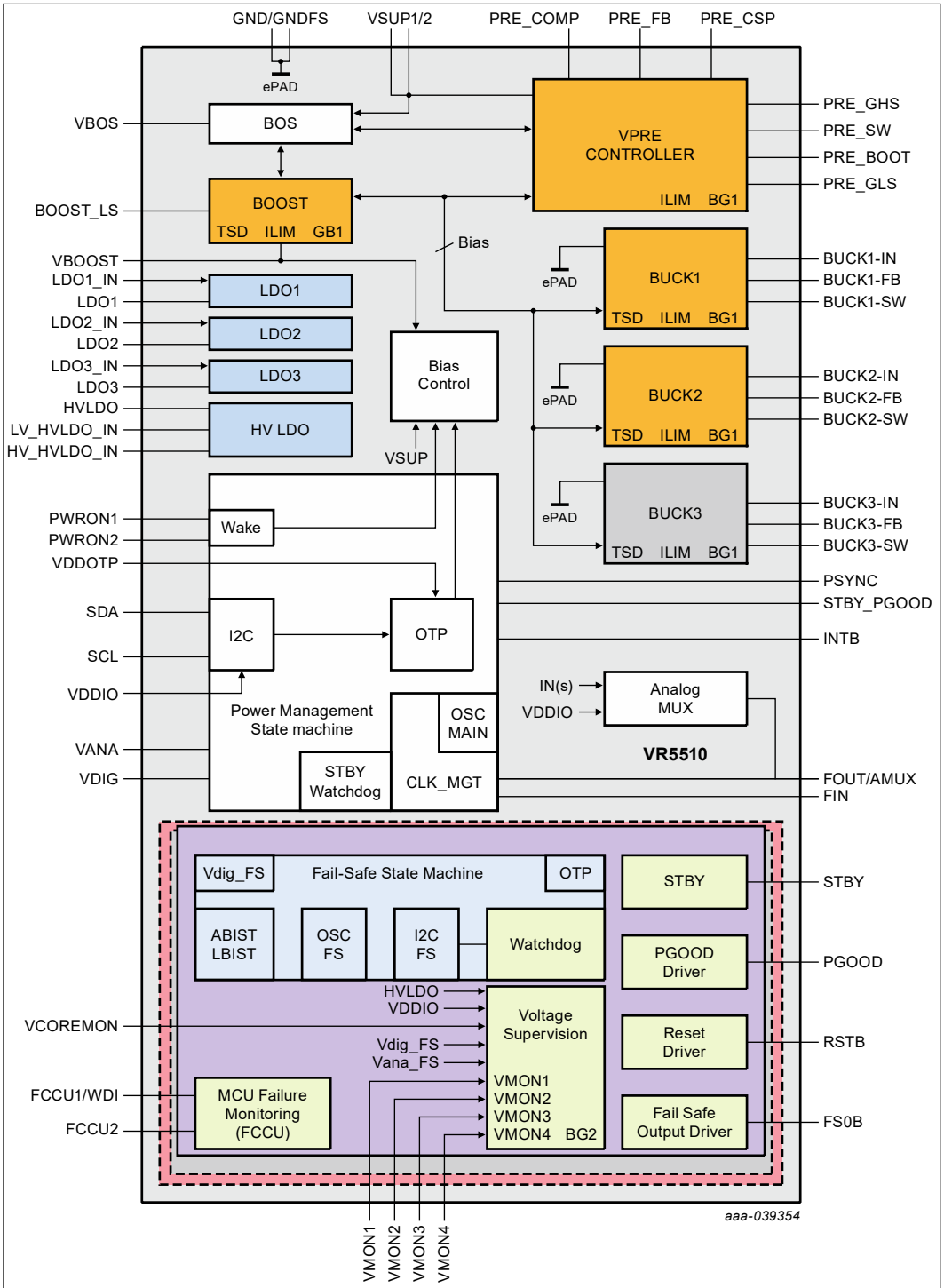


Figure 2. Internal block diagram

7 Pinout Information

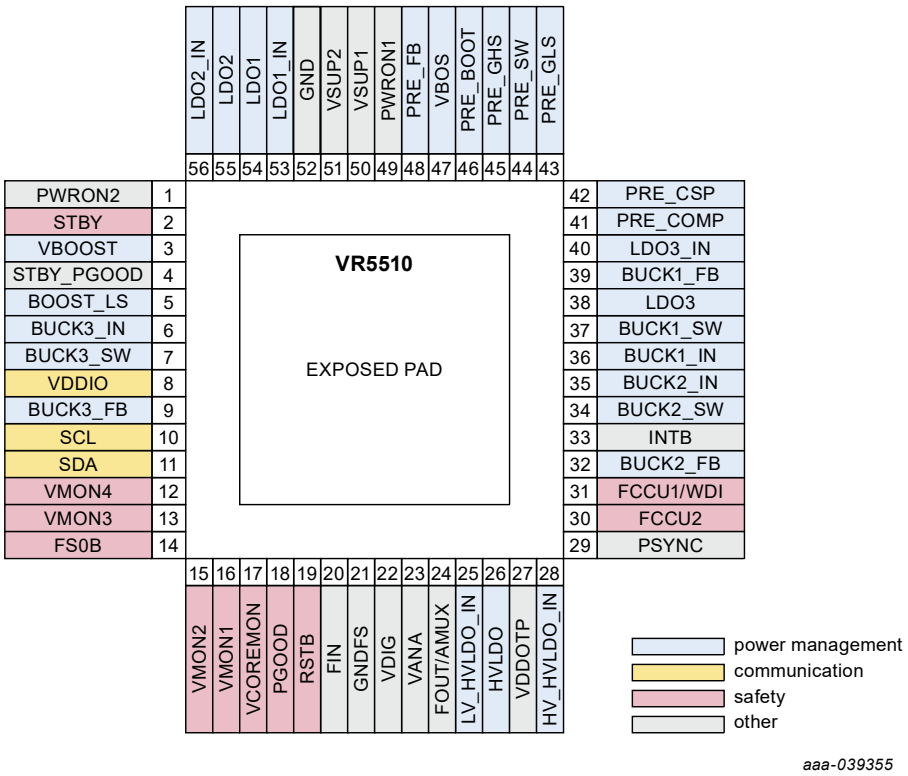


Figure 3. VR5510 Pin configuration in QFN 56-pin with exposed pad

7.1 Pin description

Table 2. VR5510 pin descriptions

Pin	Name	Type	Connection if not used	Description
1	PWRON2	A_IN	External pull down to GND	Power enable input 2
2	STBY	D_IN	Open	Standby pin
3	VBOOST	A_IN	Refer to Section 11 "Low Voltage Boost: VBOOST"	Boost voltage feedback
4	STBY_PGOOD	D_OUT	Open	Standby PGOOD Pin output dedicated to S32G
5	BOOST_LS	P_IN	Refer to Section 11 "Low Voltage Boost: VBOOST"	Boost Low Side Drain of internal MOSFET
6	BUCK3_IN	P_IN	Open	Low Voltage Buck3 input voltage
7	BUCK3_SW	P_OUT	Open	Low Voltage Buck3 switching node
8	VDDIO	A_IN	Connection mandatory	Input supply for the digital interfaces (I^2C, Interrupt, FIN and FOUT), 1.8 V or 3.3 V
9	BUCK3_FB	A_IN	Open	Low Voltage Buck3 voltage feedback
10	SCL	D_IN	External pull down to GND	I^2C Bus. Clock input

Table 2. VR5510 pin descriptions...*continued*

Pin	Name	Type	Connection if not used	Description
11	SDA	D_IN/OUT	External pull down to GND	I^2C Bus. Bidirectional data line
12	VMON4	A_IN	Open, refer Section 22 "Safety"	Voltage monitoring input 4
13	VMON3	A_IN	Open, refer to Section 22 "Safety"	Voltage monitoring input 3
14	FS0B	D_OUT	Open, refer to Section 22 "Safety"	Fail-safe Output 0. Active Low. Open drain structure.
15	VMON2	A_IN	Open, refer to Section 22 "Safety"	Voltage monitoring input 2
16	VMON1	A_IN	Open, refer to Section 22 "Safety"	Voltage monitoring input 1
17	VCOREMON	A_IN	Connection mandatory	VCORE monitoring input: Must be connected to Buck1 output voltage or Buck1/2 in dual phase
18	PGOOD	D_OUT	Connection mandatory	Power good output
19	RSTB	D_OUT/IN	Connection mandatory	Reset output. Active Low. The main function is to reset the MCU. Reset input voltage is monitored to detect external reset and fault conditions
20	FIN	D_IN	External pull down to GND	Frequency synchronization input
21	GNDFS	GND	Connection mandatory	Fail-safe ground
22	VDIG	A_OUT	Connection mandatory	VDIG output pin. A 1 µF capacitor is required at this pin
23	VANA	A_OUT	Connection mandatory	VANA output pin; A 1 µF capacitor is required at this pin
24	FOUT/AMUX	D_OUT/A_OUT	Open	Frequency synchronization output
25	LV_HVLDO_IN	P_IN	Open	Low Voltage HVLDO Input
26	HVLDO	P_OUT	Open	HVLDO output voltage
27	VDDOTP	A_IN	Pull down to GND	Voltage for OTP fuse programming and Debug mode
28	HV_HVLDO_IN	P_IN	Open	High Voltage HVLDO Input
29	PSYNC	D_IN/D_OUT	Open or pull down to GND	Power Synchronization input/output
30	FCCU2	D_IN	Pull up to VDDIO with a 5.1 kΩ resistor	Fault Collection and Control Unit input 2.
31	FCCU1/WDI	D_IN	Pull down to GND with a 22 kΩ resistor	Fault Collection and Control Unit input 2.
32	BUCK2_FB	A_IN	Open	Low Voltage Buck2 voltage feedback
33	INTB	D_OUT	Open	Interrupt output
34	BUCK2_SW	P_OUT	Open	Low Voltage Buck2 switching node
35	BUCK2_IN	P_IN	Open	Low Voltage Buck2 input voltage
36	BUCK1_IN	P_IN	Connection mandatory	Low Voltage Buck1 input voltage

Table 2. VR5510 pin descriptions*...continued*

Pin	Name	Type	Connection if not used	Description
37	BUCK1_SW	P_OUT	Connection mandatory	Low Voltage Buck1 switching node
38	LDO3	P_OUT	Open	Output of the voltage regulator LDO3
39	BUCK1_FB	A_IN	Connection mandatory	Low Voltage Buck1 voltage feedback
40	LDO3_IN	P_IN	Open	Input of the voltage regulator LDO3
41	PRE_COMP	A_IN	Refer to Section 28.3.2 "VPRE"	VPRE, High Voltage Buck Controller compensation network
42	PRE_CSP	A_IN	Refer to Section 28.3.2 "VPRE"	VPRE, High Voltage Buck Controller current sense positive input
43	PRE_GLS	A_OUT	Refer to Section 28.3.2 "VPRE"	VPRE, Low Side gate driver output for external MOSFET
44	PRE_SW	P_OUT	Refer to Section 28.3.2 "VPRE"	VPRE, High Voltage Buck Controller switching output
45	PRE_GHS	A_OUT	Refer to Section 28.3.2 "VPRE"	VPRE, High Side gate driver output for external MOSFET
46	PRE_BOOT	A_IN/A_OUT	Refer to Section 28.3.2 "VPRE"	VPRE, High Voltage Buck Controller bootstrap connection. A capacitor is required at this pin
47	VBOS	P_OUT	Connection mandatory	Best of supply output voltage pin.
48	PRE_FB	A_IN	Refer to Section 28.3.2 "VPRE"	VPRE, High Voltage Buck Controller feedback voltage and current sense negative input
49	PWRON1	A_IN	External pull down to GND	Power Enable input 1
50	VSUP1	A_IN	Connection mandatory	Power supply 1 of the device. An external reverse battery protection diode in series is mandatory. Add a 0.1 µF decoupling close to VSUP1/2 points.
51	VSUP2	A_IN	Connection mandatory	Power supply 2 of the device. An external reverse battery protection diode in series is mandatory
52	GND	GND	Connection mandatory	Main ground
53	LDO1_IN	P_IN	Open	Linear regulator 1 input voltage
54	LDO1	P_OUT	Open	Linear regulator 1 output voltage
55	LDO2	P_OUT	Open	Linear regulator 2 output voltage
56	LDO2_IN	P_IN	Open	Linear regulator 2 input voltage
57	EP	GND	Connection mandatory	Exposed pad. Must be connected to GND
A: Analog, D: Digital, P: Power				

8 General Product Characteristics

8.1 Maximum ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Table 3. Maximum ratings

Symbol	Description (Rating)	Min	Max	Unit
Voltage ratings				
VSUP1/2, PWRON1, HV_HVLDO_IN	DC Voltage at Power Supply VSUP1/2, PWRON1, HV_HVLDO_IN pins	-0.3	60	V
PRE_SW	DC Voltage at PRE_SW pin	-2.0	60	V
VMONx, FS0B	DC Voltage at VMON1,2,3,4, VCOREMON, FS0B pins	-0.3	60	V
BUCKx_SW	Low Voltage Buckx switching node	-0.3	5.5	V
PRE_GHS, PRE_BOOT	DC Voltage at PRE_GHS, PRE_BOOT pins	-0.3	65.5	V
VDDOTP,	DC Voltage at VDDOTP	-0.3	10	V
VBOOST, BOOST_LS, LDO1_IN	DC Voltage at BOOST_LS, VBOOST, LDO1_IN pins	-0.3	8.5	V
VDIG, VANA	DC Voltage at VDIG, VANA pins	-0.3	1.65	V
All other pins	DC Voltage at all other pins	-0.3	5.5	V
ESD ratings				
Human Body Model (JESD22/A114): 100 pF, 1.5 kΩ				
V_{ESD_HBM1}	All pins	-2.0	2.0	kV
Charge Device Model (JESD22/C101)				
V_{ESD_CDM1}	All pins	-500	500	V
GUN (VSUP1, VSUP2, HV_HVLDO_IN, PWRON1, FS0B, VDDOTP)				
V_{ESD_GUN1}	Discharged contact test - 330 Ω/150 pF - IEC61000-4-2	-8	8	kV
V_{ESD_GUN2}	Discharged contact test - 2 kΩ/150 pF - ISO10605:2008	-8	8	kV
V_{ESD_GUN3}	Discharged contact test - 2 kΩ/330 pF - ISO10605:2008	-8	8	kV

8.2 Electrical characteristics

TA = –40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Table 4. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Power Supply					
I_{VSUP_NORMAL}	Current in Normal Mode, all regulators ON (I_{OUT}=0)	—	15	25	mA
QiSTBY	Current in Standby Mode, all regulators OFF, except VPRE, HVLDO Tj = 25° C, (I_{OUT}=0), VSUP = 12 V	—	35	50	µA
	Current in Standby Mode, all regulators OFF, except VPRE, HVLDO, BUCK3, LDO2, Tj = 25° C, (I_{OUT}=0), VSUP = 12 V	—	85	—	µA
QiDSM	Current in Deep Sleep Mode, all regulators OFF, except HVLDO, Tj = 25° C (I_{OUT}=0), VSUP = 12 V	—	15	25	µA
QiOFF	Current in OFF Mode, Tj = 25° C, VSUP = 12 V	—	15	25	µA
V_{SUP_UV7}	VSUP under-voltage threshold (7 V)	7.2	7.5	7.8	V
V_{SUP_UVH}	VSUP under-voltage threshold high (during power up and Vsup rising) OTP configuration VSUPCFG_OTP = 0 [1]	4.7	—	5.1	V
	VSUP under-voltage threshold high (during power up and Vsup rising) OTP configuration VSUPCFG_OTP = 1 [1]	6	—	6.4	V
V_{SUP_UVL}	VSUP under-voltage threshold low (during power-up and Vsup falling) OTP configuration VSUPCFG_OTP = 0	4.0	—	4.4	V
	VSUP under-voltage threshold low (during power-up and Vsup falling) OTP configuration VSUPCFG_OTP = 1	5.3	—	5.7	V
T_{SUP_UV}	V_{SUP_UV7}, V_{SUP_UVH} and V_{SUP_UVL} filtering time	6	10	15	us
VPRE_POR, VBOS_POR, VSUP_POR	VR5510 transitions to Unpowered state (also active in Standby mode)	2.5	2.6	2.7	V
Interface supply pins					
V_{DDIO}	VDDIO supply voltage range	1.75	—	3.4	V

[1] VSUPCFG_OTP should be set to 1 if VPRE > 4.5 V

8.3 Operating range

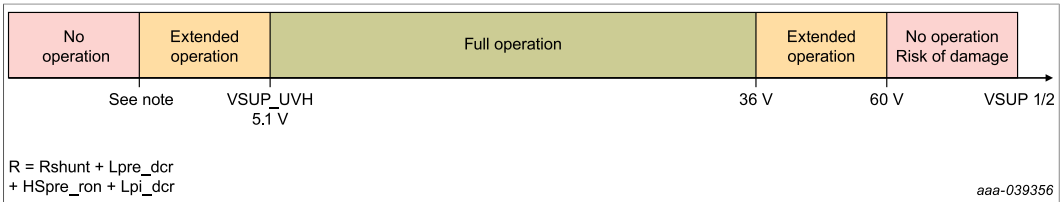


Figure 4. VR5510 Operating voltage range

Note: *See* Section 10.1

Below the VSUP_UVH threshold, the extended operation range depends on the VPRE output voltage configuration and the external components.

- When VPRE is configured at 5 V, VPRE might not remain in its regulation range
- VSUP minimum voltage depends on the external components (LPI_DCR) and the application conditions (IPRE, F_VPRESW).

When VPRE is switching at 455 kHz, the VR5510 maximum continuous operating voltage is 36 V. The part is validated at 48 V for a limited duration of 15 minutes at room temperature to satisfy the jump-start requirement of 24 V applications. It can sustain a 58 V load dump without external protection.

When VPRE is switching at 2.2 MHz, the VR5510 maximum continuous operating voltage is 18 V. The part is validated at 26 V for limited duration of 2 minutes at room temperature to satisfy the jump-start requirement of 12 V applications and a 35 V load dump.

8.4 Thermal ratings

Table 5. Thermal ratings

Symbol	Parameter	Conditions	Min	Max	Unit
$R_{\theta JA}$	Thermal Resistance Junction to Ambient[1]	2s2p circuit board[2]	—	27	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient[1]	2s8p circuit board[2]	—	17	°C/W
$R_{\theta JB}$	Junction to Board Thermal Resistance	2s2p circuit board[2]	—	22	°C/W
$R_{\theta JB}$	Junction to Board Thermal Resistance	2s8p circuit board[2]	—	15	°C/W
$R_{\theta JC\_BOTTOM}$	Junction to Case Bottom Thermal Resistance	2s8p and 2s2p circuit board[2]	—	1.5	°C/W
$R_{\theta JC\_TOP}$	Junction to Case Top Thermal Resistance	2s8p and 2s2p circuit board[2]	—	17	°C/W
Ψ_{JT_TOP}	Thermal Resistance Parameter Junction to top[1]	Between the package top and the junction temperature[1]	—	1	°C/W
T_A	Ambient Temperature (Automotive)		-40	125	°C
T_A	Ambient Temperature (Industrial)		-40	105	°C
T_J	Junction Temperature		-40	150	°C
T_{STG}	Storage Temperature		-55	150	°C

[1] Determined in accordance with JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment. Uniform power is assumed on die top surface.

[2] Thermal test board meets JEDEC specification for this package (JESD51-9)

8.5 EMC compliancy

Table 6. VR5510 EMC compliancy chart

Pin	Pin_Type	EMC Compliance
VBAT (VSUP1/2)	Global	Conducted Emissions – IEC 61967-4 (150 Ω method, 12-M level, 50% load on regulators) Conducted Immunity – IEC 62132-4 (36dBm, Class A, No state change on FS0B, RSTB, PGOOD, INTB, 50% load on all regulators and accuracy in spec
HV_HVLDO_IN	Global	
PWRON1	Global	
FS0B	Global	Conducted Emissions – IEC 61967-4 (150 Ω method, 12-M level, 50% load on regulators) Conducted Immunity – IEC 62132-4 (30dBm, Class A, No state change on FS0B, RSTB, PGOOD, INTB, 50% load on all regulators and accuracy in spec

Table 6. VR5510 EMC compliancy chart*...continued*

Pin	Pin_Type	EMC Compliance
BUCK1/2/3_IN	Local, Supply	Conducted Emissions – IEC 61967-4 (150 Ω method, 10-K level, 50% load on regulators) Conducted Immunity – IEC 62132-4 (12dBm, Class A, HVLDO in switch mode. No state change on FS0B, RSTB, PGOOD, INTB, 50% load on all regulators and accuracy in spec
LDO1/2/3_IN	Local, Supply	
LV_HVLDO_IN	Local, Supply	
VRE_FB	Local	Conducted Emissions – IEC 61967-4 (150 Ω method, 10-K level, 50% load on regulators) Conducted Immunity – IEC 62132-4 (12 dBm, Class A. No state change on FS0B, RSTB, PGOOD, INTB, 50% load on all regulators and accuracy in spec
BUCK1/2/3_FB	Local	
LDO1/2/3	Local	
HVLDO	Local	
VBOOST	Local	
VBOS	Local	
PWRON2	Local	Conducted Emissions – IEC 61967-4 (150 Ω method, 12-M level, 50% load on regulators) Conducted Immunity – IEC 62132-4 (12 dBm, Class A. No state change on FS0B, RSTB, PGOOD, INTB, 50% load on all regulators and accuracy in spec
PGOOD	Local	Conducted Emissions – IEC 61967-4 (150 Ω method, 10-K level, 50% load on regulators) Conducted Immunity – IEC 62132-4 (12 dBm, Class A. No state change on FS0B, RSTB, PGOOD, INTB, 50% load on all regulators and accuracy in spec
RSTB	Local	
STBY	Local	
STBY_PGOOD	Local	
VDDIO	Local	

8.6 Functional state diagram

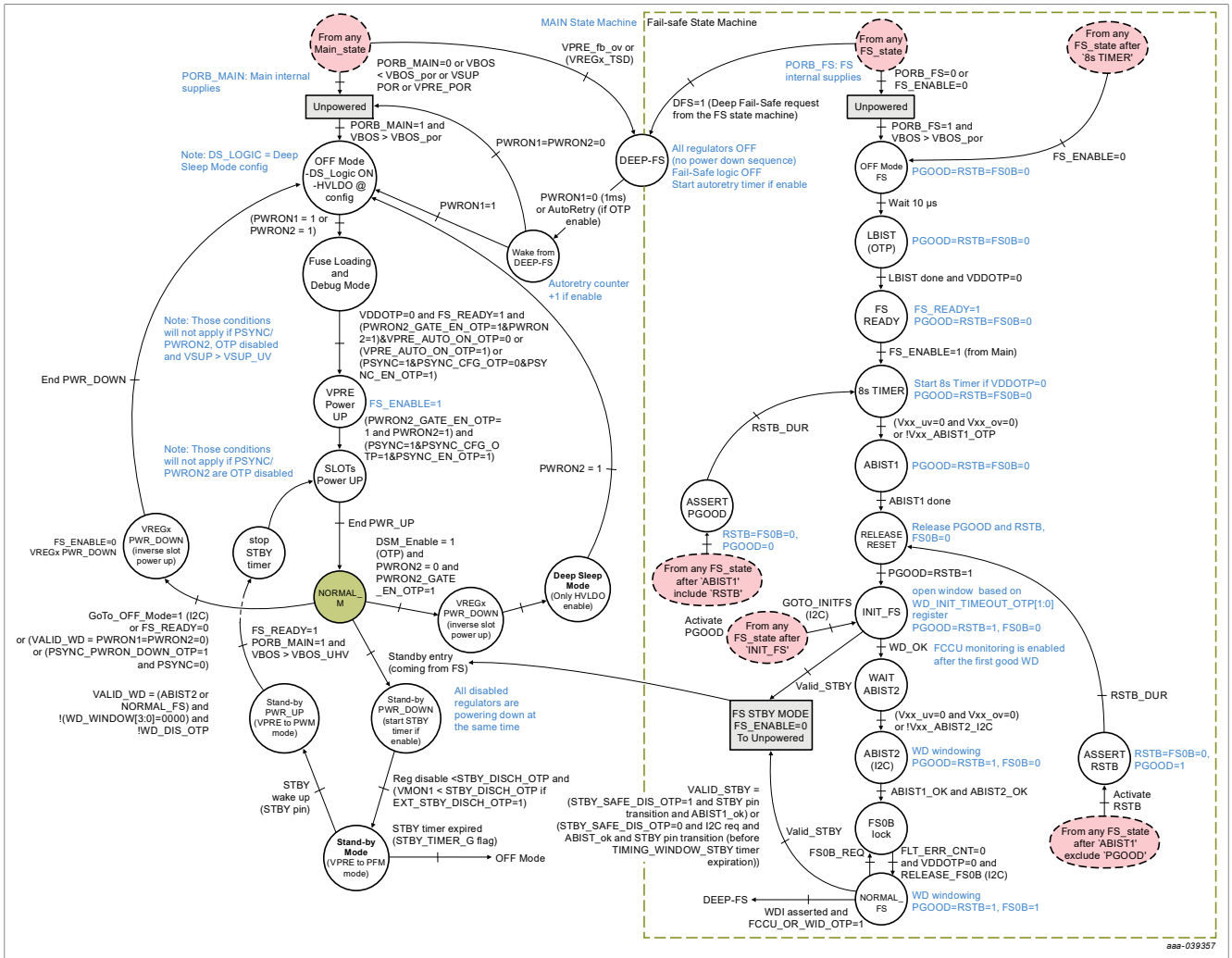


Figure 5. Functional state diagram

8.7 Functional device operation

The VR5510 device has two independent logic blocks. The Main state machine manages the power management, Standby mode, Deep Sleep mode, and the power-on sources. The Fail-safe sate machine manages entry into Standby and monitors power management and the MCU.

8.8 Main state machine

The VR5510 starts when VSUP > V_{SUP_UVH} and PWRON1 > $PWRON1_{VIH}$ or PWRON2 > $PWRON2_{VIH}$. VBOS powers up first, followed by VPRE. OTP programming determines the power-up sequence for the remaining regulators. When the power-up sequence is finished, the main state machine is in Normal_M mode, which is the application running mode with all the regulators on. Depending on the OTP configuration, HVLDO can be programmed to be the first regulator to start up.

The device can be put into Standby mode by toggling the STBY pin or by issuing an I^2C command in conjunction with toggling the STBY pin (refer to Section 8.16 "Standby mode entry" for further details). The device goes into Standby mode after verifying that all disabled regulators have been discharged to less than 100 mV.

The device can be put into Deep Sleep mode by toggling the PWRON2 pin (refer to Section 8.17 "Modes of operation" for further details). The device goes through the power-down sequence to reach the deep sleep state where only the HVLDO is kept alive.

The device can be put into OFF mode by an I^2C command from the MCU. For an application without MCU or QM, when the device is disabled, it goes into OFF mode when both PWRON1 and PWRON2 = 0. The device goes into OFF mode following the power-down sequence in order to stop all the regulators in the reverse order that they were powered up. When VPRE is supplying an external PMIC, VPRE shutdown can be delayed from 250 us or 32 ms by the VPRE_OFF_DLY_OTP bit (CFG_SM_ 2_OTP register) in order to wait for the external device's power-down sequence to complete.

If a VSUP loss (VSUP < V_{SUP_POR}), a VPRE loss (VPRE < V_{PRE_POR}), or a VBOS (VBOS < V_{BOS_POR}) loss occurs, the device halts operation, disables HVLDO and goes directly into UNPOWERED mode without initiating the power-down sequence. The device restarts again when VSUP > V_{SUP_UVH} and PWRON1> $PWRON1_{VIH}$ or PWRON2> $PWRON2_{VIH}$.

8.9 Deep Fail-safe state

The Deep Fail-safe state is part of the Main state machine.

If a VPRE_FB_OV or a TSD detection occurs on an enabled regulator or if the Fail-safe state machine issues a Deep Fail-safe request (DFS = 1), the device halts operation and goes directly to DEEP-FS mode without initiating the power-down sequence.

The device exits Deep Fail-safe mode when the PWRON1 pin is set to zero. If the OTP configuration (AUTORETRY_EN_OTP bit in CFG_SM_ 2_OTP register) has activated the auto-retry timeout feature (AUTORETRY_TIMEOUT_OTP bit in CFG_ CLOCK_ 3_OTP register), the device exits Deep Fail-safe mode after either 4 seconds or 100 ms.

OTP configuration can limit the number of auto-retries to 15 or can set the number of auto-retries to be unlimited (AUTORETRY_INFINITE_OTP bit in CFG_SM_ 2_OTP register).

The device restarts when VSUP > V_{SUP_UVH} and PWRON1> $PWRON1_{VIH}$.

8.10 Fail-safe state machine

The Fail-Safe state machine starts with LBIST execution (LBIST is OTP programmable and can be disabled to speed up the startup process) when VBOS > V_{BOS_POR}. When the LBIST completes, the 8-second timer monitoring the RSTB pin starts. ABIST1 starts automatically when all the regulators assigned to ABIST1 have passed their undervoltage and overvoltage checks. When the ABIST1 completes, the RSTB and PGOOD pins are released and the initialization of the device is opened via a programmable window based on the WD_INIT_TIMEOUT_OTP[1:0] bit field (CFG_ 2_OTP register). An ABIST1 fail does not prevent the release of RSTB and PGOOD.

The first good watchdog refresh closes the INIT_FS and the device waits for an I^2C command to execute the ABIST2. When the ABIST2 completes successfully, the fault counter must be cleared with the appropriate number of good watchdog refreshes in order to release the FS0B pin.

When the FS0B pin is released, the device is ready for application running mode with all the selected monitoring activated. In application running mode, the VR5510 reacts by asserting the safety pins (PGOOD, RSTB and FS0B) according to its configuration when a fault is detected (refer to the *VR5510 Safety Manual* for more details).

8.11 Power sequencing

VPRE is the first regulator to start automatically before SLOT_0. The other regulators start according to the OTP power sequencing configuration. Seven slots are available to program the start-up sequence of the BUCK1, BUCK2, BUCK3, BOOST, LDO1, LDO2, LDO3 and HVLDO regulators. Additionally, HVLDO can be programmed to start up (or not start up) in a slot by using the HVLDO_SLOT_EN_OTP bit (CFG_ SEQ_ 4_OTP register). For applications that require HVLDO to track BUCK1, BUCK1 and HVLDO are separated by one slot and HVLDO starts first, followed by BUCK1.

The power-up sequence starts at SLOT_0 and ends at SLOT_7; the power-down sequence is executed in reverse order. If not all seven of the slots are used, the state machine skips the unused slots. The regulators assigned to SLOT_7 are not started during the power-up sequence. They can be started (or not) later in Normal_M mode with an I^2C Write command to the M_REG_CTRL1/2 registers.

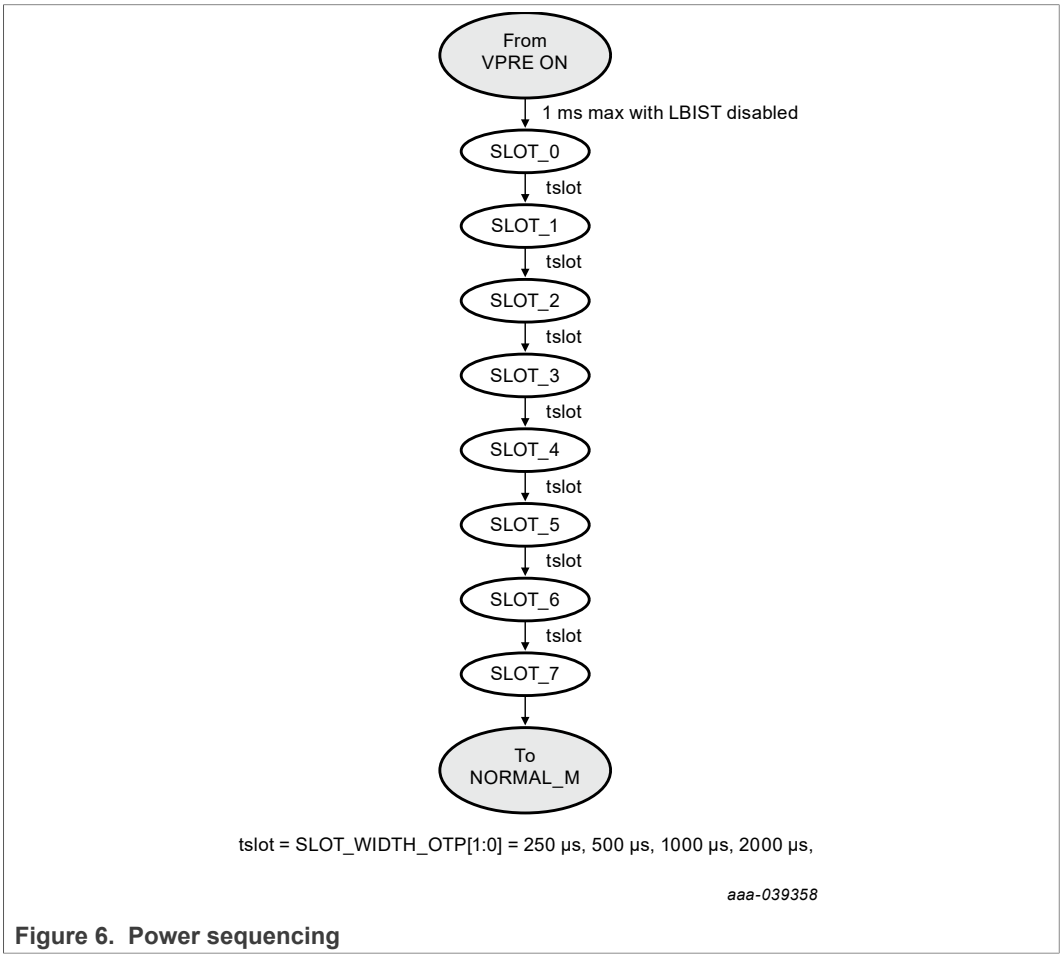


Figure 6. Power sequencing

Each regulator is assigned to a SLOT by OTP configuration using the following OTP bits:

BUCK1 regulator assigned to a slot using BUCK1S_OTP [2:0]

BUCK2 regulator assigned to a slot using BUCK2S_OTP [2:0]

BUCK3 regulator assigned to a slot using BUCK3S_OTP [2:0]

LDO1 regulator assigned to a slot using LDO1S_OTP [2:0]

LDO2 regulator assigned to a slot using LDO2S_OTP [2:0]

LDO3 regulator assigned to a slot using LDO3S_OTP [2:0]

HVLDO regulator assigned to a slot using HVLDOS_OTP [2:0]

BOOST regulator assigned to a slot using BOOSTS_OTP [2:0]

The width of each slot is configurable via OTP using the SLOT_WIDTH_OTP [1:0] bitfield

SLOT_WIDTH_OTP [1:0] = 00 (Default) corresponds to 250 µs slot width

SLOT_WIDTH_OTP [1:0] = 01 corresponds to 500 µs slot width

SLOT_WIDTH_OTP [1:0] = 10 corresponds to 1000 µs slot width

SLOT_WIDTH_OTP [1:0] = 11 corresponds to 2000 µs slot width

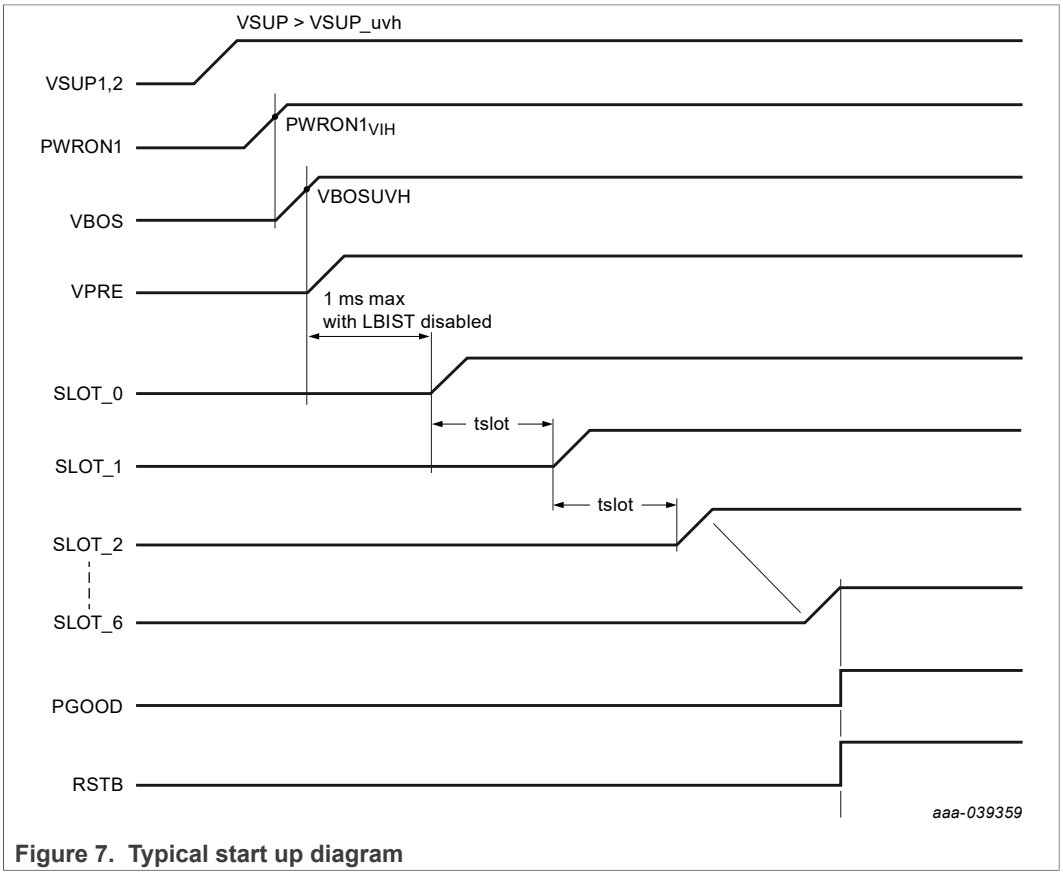


Figure 7. Typical start up diagram

The real power-up sequence depends not only on the slot OTP setting but also on the different soft-start times for each regulator. If the LBIST is enabled, VBOSUVH to SLOT_0 timing can be higher than 1 ms. LBIST typical duration is 3 ms.

8.12 Entering Debug mode using the VDDOTP pin

The VR5510 provides a means of evaluating the device in Debug mode. Debug mode allows users, via the I^2C interface, to access the OTP register set, modify the registers, and test device functions. During Debug mode all regulators remain off.

The VR5510 enters in Debug mode with the following sequence:

1. Apply VDDOTP pin > 5 V.
2. Apply VSUP1/2 > V_{SUP_UVH} and PWRON1 > $PWRON1_{VIH}$ or PWRON2 > $PWRON2_{VIH}$.
3. The device now starts in Debug mode, ready for debugging or OTP programming.
4. Apply VDDOTP = 0 V to turn on the device with the modified configuration.

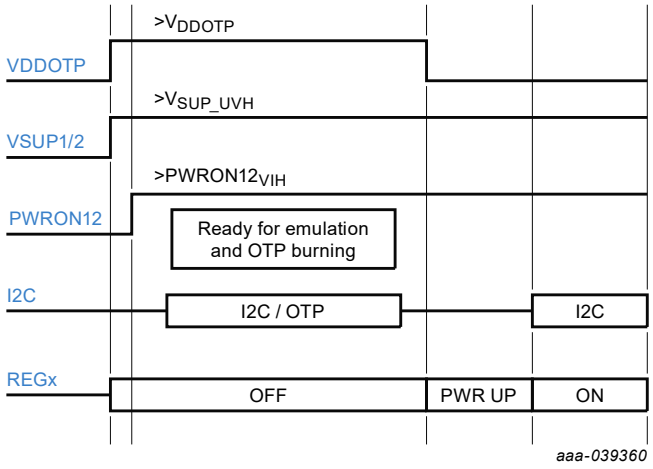


Figure 8. Debug mode entry

If VDBG voltage is maintained at the VDDOTP pin, a new OTP configuration can be emulated or programmed by I^2C communication using the NXP GUI Interface and NXP socket EVB. When the OTP process completes, the device starts with the new OTP configuration when the VDDOTP pin is asserted low. OTP emulation/programming is possible during engineering development only. OTP programming in production is done by NXP.

In Debug mode, the Watchdog window is fully opened, the Deep Fail-safe request from the Fail-safe state machine (DFS = 1) is masked, the 8-second timer monitoring the RSTB pin is disabled and the Failsafe output pin FS0B cannot be released. Entering Standby mode is not possible while the device is in Debug mode.

In Debug mode, the I^2C address is fixed at 0x20 for Main digital access and 0x21 for Fail-safe digital access.

In Debug mode, no watchdog refresh is required in order to facilitate debugging of the hardware and software routines (i.e. I^2C commands). However, the watchdog functionality is kept on (seed, LFSR, WD refresh counter, WD error counter). WD errors are detected and counted and are reacted to on the RSTB pin.

To release FS0B without taking care of the Watchdog window, disable the Watchdog window with WD_WINDOW [3:0] = 0000 in the FS_WD_WINDOW register before leaving Debug mode. To leave Debug mode, write DBG_EXIT bit = 1 in the FS_STATES register.

TA = –40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Table 7. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{DDOTP}	Debug mode entry threshold	5	-	8	V
T_{DBG}	Debug mode entry filtering time	4	-	8	µs

8.13 Flow charts

The following flow charts describe how the device starts, how to go in Standby mode, and what to do when the RSTB pin is released.

8.14 Application flow charts

In application mode, the VDDOTP pin is connected to GND and a watchdog refresh is required as soon as INIT_FS is closed.

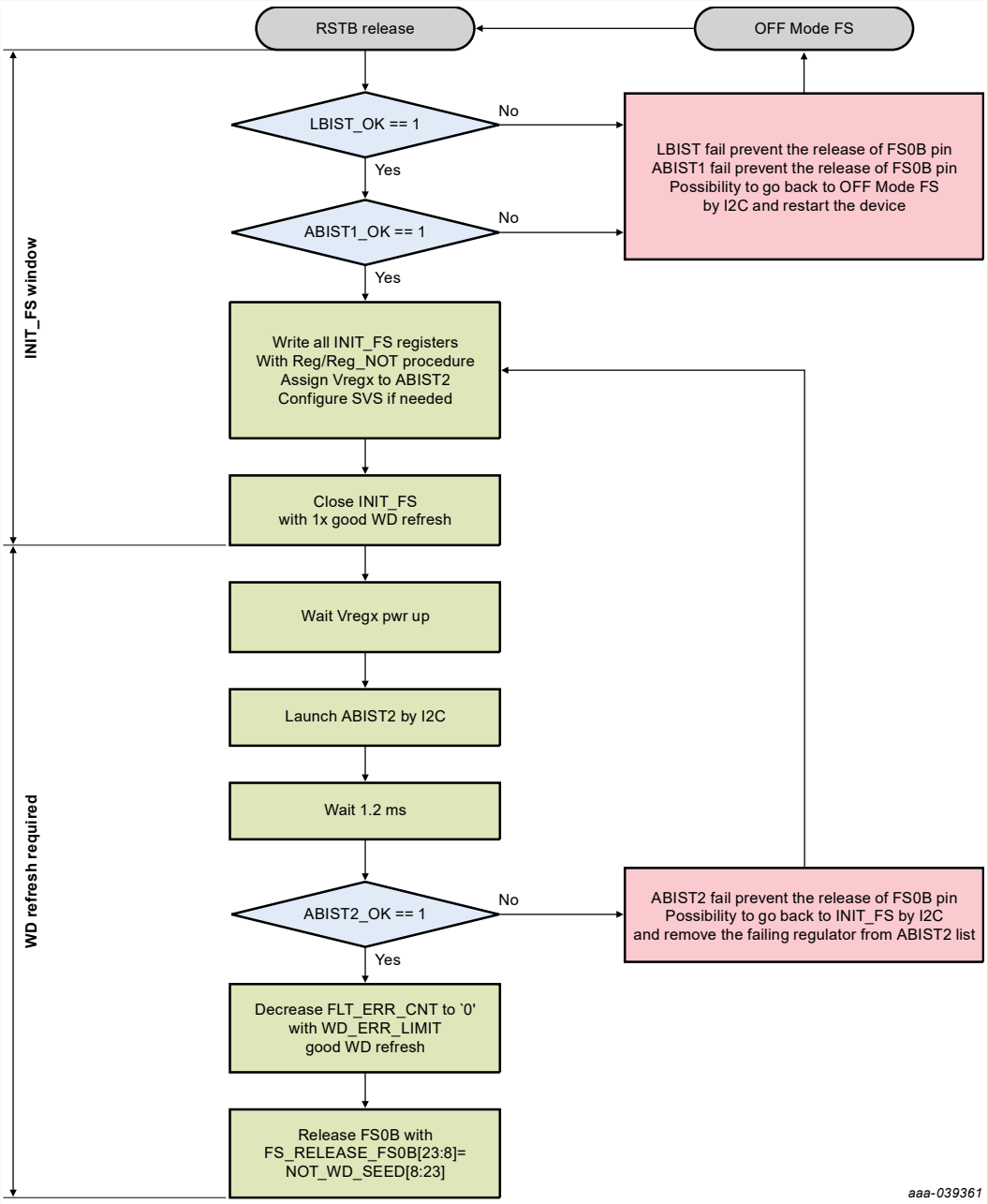


Figure 9. Application flow chart

8.15 Debug flow charts

In Debug mode, the VDDOTP pin is managed as described in Section 8.12 "Entering Debug mode using the VDDOTP pin". The watchdog window is fully open and a watchdog refresh is not required.

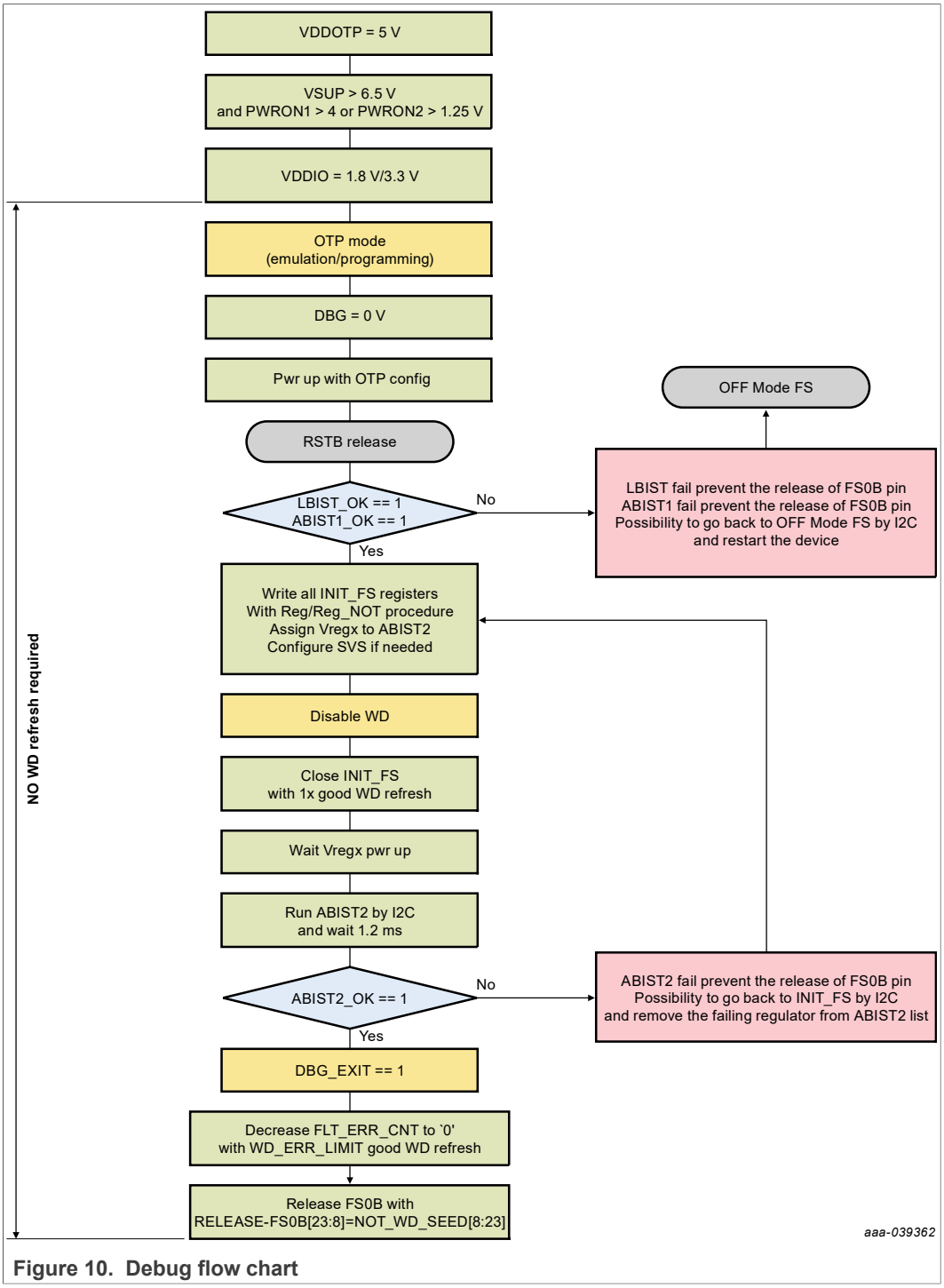


Figure 10. Debug flow chart

Note: Use I^2C to disable the watchdog before INIT_FS closure and Debug mode exit in order to allow FS0B to be released. Otherwise, FS0B remains stuck low in debug mode.

8.16 Standby mode entry

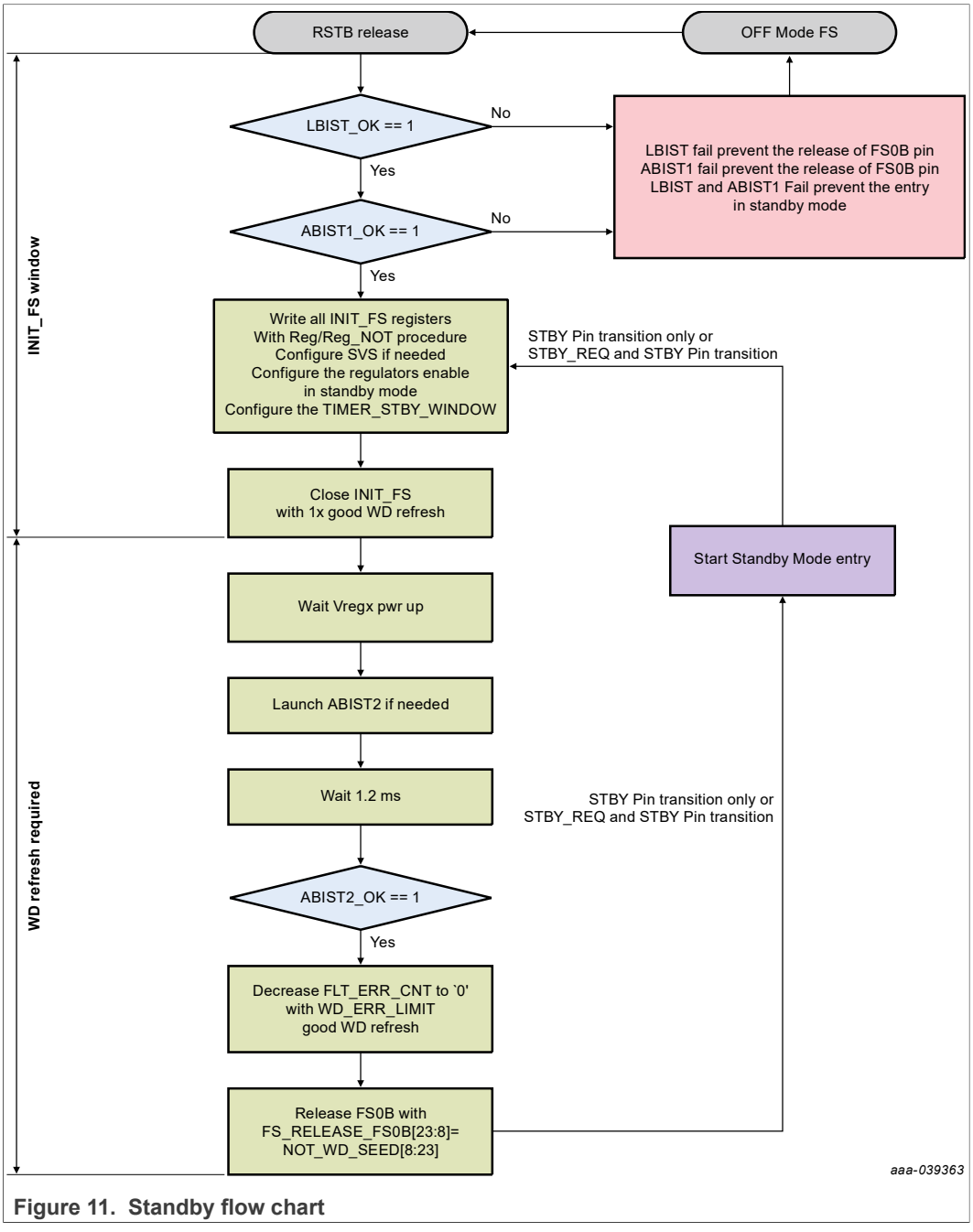


Figure 11. Standby flow chart

8.17 Modes of operation

Depending on the application, VR5510 allows several modes of operation: OFF mode, Deep Sleep mode, Standby mode, and Normal mode.

1. OFF mode:

OFF mode is the initial state of the device where all the regulators are off.

2. Deep Sleep mode:

Deep Sleep mode shuts down all VR5510 regulators except the HVLDO in LDO mode. The PWRON2 input detector is active in Deep Sleep mode and can trigger a turn-on event.

The DSM_EN_OTP bit (DSM_EN_OTP register) enables or disables the Deep Sleep (DSM) mode of operation.

Table 8. Deep Sleep mode OTP bit settings

	OTP description	Deep Sleep mode	
DSM_EN_OTP	Enables or disables Deep Sleep mode of operation	0	DSM Disabled
		1	DSM Enabled

When DS mode is enabled, the PWRON2 pin is used to transition to DSM mode from normal operation, in which case, the PWRON2_DSM_EN bit (M_MODE register) should be enabled.

If Deep Sleep mode is enabled, the HVLDO cannot be assigned to a slot and always starts first on the power-up sequence (before VPRE).

In Deep Sleep Mode, the HVLDO can be only use in LDO mode.

3. Standby mode:

Standby mode is a low-power mode used when the device is required to go into a minimal supply current mode while maintaining minimal preset output voltages. Standby mode is entered by toggling the STBY pin when conditions are programmed correctly with the STBY_EN_OTP bit (CFG_ VPRE_ 2_OTP register) and the STBY_WINDOW_EN_OTP bit (CFG_ 2_OTP register).

The main regulators switched on during low-power Standby mode are VPRE and the HVLDO. VPRE is forced to operate in PFM mode while the HVLDO operates in LDO mode. An option is available to operate other regulators (except BOOST) as well, but the switchers are then forced to operate only in PFM.

The BUCKx_STBY_EN bit enables or disables the Buck regulators in Standby mode.

The LDOx_STBY bit enables or disables the LDOs in Standby mode.

The HVLDO_STBY bit enables or disables the LDOs in Standby mode.

Refer to AN12880 for more Standby mode examples and details.

4. Normal mode:

In Normal mode, the device operates with the regulators turned-on according to the preprogrammed settings. The device stays in Normal mode until the processor requests a transition into Standby mode or Deep Sleep mode. The device exits Normal mode and goes into OFF mode or Deep Fail-safe mode when an internal fault is detected or an external fault is indicated by the processor.

9 Best Of Supply

9.1 Functional description

The VBOS regulator manages the best of supply from VSUP, VPRE, or VBOOST to efficiently provide a 5.0 V output for the device's internal biasing. VBOS also supplies the VPRE high-side and low-side gate drivers and the VBOOST low-side gate driver.

A VBOS undervoltage could result in the device not being fully functional. Consequently, VBOS_UVL detection powers down the device

A VSUP_UV7 undervoltage threshold is used to enable the path from VSUP to VBOS when VSUP < VSUP_UV7. This provides a low drop path from VSUP while VRPE is going low and when the device is powering up with VPRE not started. When VSUP > VSUP_UV7, VBOS is forced to use either VPRE or VBOOST to optimize efficiency.

9.2 Electrical characteristics

TA = –40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Table 9. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Best Of Supply					
V_{BOS}	Best of supply output voltage	3.3	5.0	5.25	V
V_{BOSUVH}	VBOS under voltage threshold high	4.1	—	4.5	V
V_{BOS_UVL}	VBOS under voltage threshold low	3.2	—	3.4	V
T_{BOS_UV}	V_{BOSUVH} and V_{BOS_UVL} filtering time	6	10	15	us
T_{BOS_POR}	VBOS under voltage threshold filtering time	0.5	—	1.5	us
I_{BOS}	Best of supply current capability	—	—	60	mA
C_{Out_BOS}	Effective output capacitor	4.7	—	10	uF
	Output decoupling capacitor	—	0.1	-	uF

10 High Voltage Buck: VPRE

10.1 Functional description

VPRE is a high voltage, synchronous, peak current mode buck controller that uses an external logical level NMOS. VPRE works in PWM mode during Normal operation and in PFM mode in Standby operation. VPRE input voltage is limited to **VSUP = LPI_DCR × IPRE + VPRE_UVL / DMAX with DMAX = 1 − (FPRE_SW × VPRETOFF_MIN)**. A bootstrap capacitor is required to supply the gate drive circuit of the high-side NMOS. The output voltage is configurable by OTP from 3.3 V to 5.2 V using the VPREV_OTP [5:0] bit field (CFG_ VPRE_ 1_OTP register), and the switching frequency is configurable by OTP using the VPRE_CLK_SEL_OTP bit (CFG_ CLOCK_ 4_OTP register). For 12-Volt automotive applications, the frequency can be set to 455 kHz or 2.2 MHz. For 24-Volt applications, the frequency should set to 455 kHz.

Stability is ensured by an external Type 2 compensation network with slope compensation.

The output current is sensed via an external shunt in series with the inductor. The external components (NMOS gate charge, inductor, shunt resistor), the gate driver current capability, and the switching frequency define the maximum current capability. Overcurrent detection is implemented to protect the external MOSFETs. If an overcurrent is detected after the HS minimum TON time, the HS turns off and turns on again at the next rising edge of the switching clock. The overcurrent induces a duty cycle reduction

that could lead to the output voltage gradually dropping, causing an under-voltage condition on VPRE or on one of the cascaded regulators.

The maximum input voltage is 60 V, which allows operation in 24-Volt truck applications without external protection to sustain ISO 16750-2:2012 load dump pulse 5b. VPRE typically is the input supply for all the regulators and VSUP must be the high voltage input for HVLDO during Deep Sleep mode. VPRE can be the supply for local loads remaining inside the ECU.

By default, the VPRE switching frequency is derived from the internal oscillator and can be synchronized with an external frequency signal applied at FIN input pin. The change from internal oscillator to external clock or vice versa is controlled by I^2C.

V_{PRE_UVH}, V_{PRE_UVL}, and $V_{PRE\_FB\_OV}$ thresholds are monitored from the PRE_FB pin and manage certain transitions of the Main state machine, as described in Section 8.6 "Functional state diagram". These monitorings are not safety related.

10.2 Application schematic

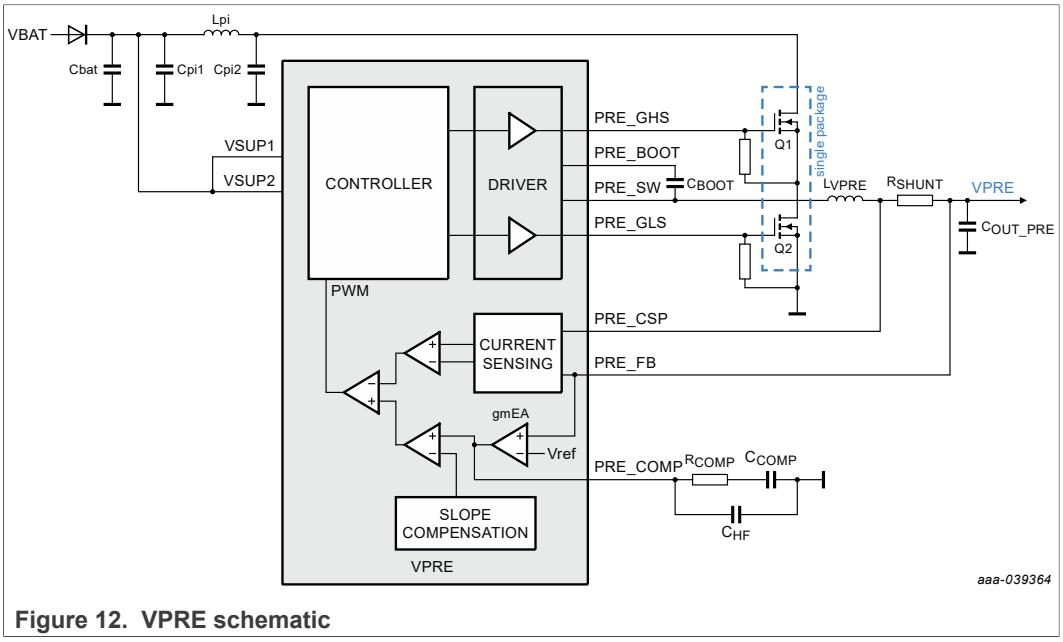


Figure 12. VPRE schematic

A PI filter, as shown in Figure 12, with $F_{RES} = 1 / [2\pi \times \sqrt{(LC)}]$ and calculated for $F_{RES} < VPRE\_FSW / 10$, is required to filter the VPRE switching frequency on the Battery line. For a clean biasing of the device, The VSUP1,2 pins must be connected ahead of the PI filter. The Cpi1 capacitor must be implemented close to the VSUP1,2 pins. The Cpi2 capacitor must be implemented close to the external MOSFET(Q1). The bootstrap capacitor value should be sized to be greater than 10 times the Gate Source capacitor of Q. Gate to Source resistor on Q1 and Q2 are recommended in order to guarantee a passive switch-off of the transistors when a pin disconnection occurs.

10.3 Compensation network

The external compensation network, made with R_{COMP}, C_{COMP} and C_{HF} must be calculated for the best compromise between stability and transient response, based on the below conceptual plot of the Type 2 compensation network transfer function.

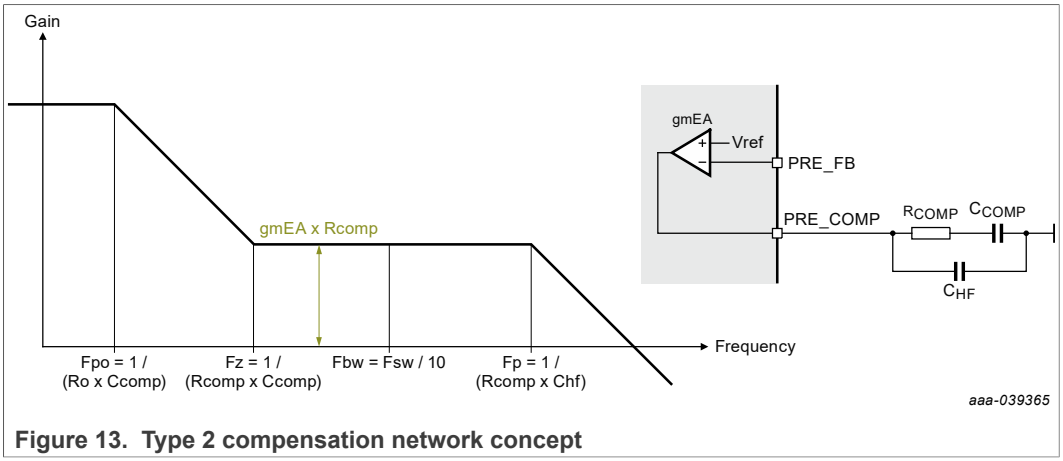


Figure 13. Type 2 compensation network concept

Table 10. Recommended compensation network components

VPRE output voltage	VPRE switching Frequency	RCOMP	CCOMP	CHF
3.3 V	455 kHz	1.5 k	22 nF	18 pF
5 V	455 kHz	2.3 k	20 nF	20 pF
3.3 V	2.2 MHz	8 k	20 nF	—
5 V	2.2 MHz	22 k	20 nF	—

10.4 Electrical characteristics

TA = –40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground. Typical values are based on TA = 25 °C.

Table 11. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
VPRE					
V_{PRE}	Output Voltage (VPREV_OTP[5:0] configuration) **(VSUPCFG_OTP bit should be set to 1 when VPRE is set above 4.5 V)**	—	3.3	—	V
		—	3.4	—	V
		—	3.5	—	V
		—	3.7	—	V
		—	4.0	—	V
		—	4.5	—	V
		—	5.0	—	V
		—	5.1	—	V
		—	5.2	—	V
V_{PREACC_PWM}	Output Voltage Accuracy, PWM Mode	-1.5	—	1.5	%
V_{PREACC_PFM}	Output Voltage Accuracy, PFM Mode	-3	—	3	%
V_{PRE_TON}	Maximum turn on time, output voltage to 90%	—	—	1	ms
$V_{PRE\_FB\_OV}$	Over voltage threshold protection (all voltages settings except 3.3 V)	5.5	—	6.5	V

Table 11. Electrical characteristics*...continued*

Symbol	Parameter	Min	Typ	Max	Unit
$V_{PRE\_FB\_OV}$	Over voltage threshold protection if VPREV_OTP[5:0] set to 3.3 V	3.7	—	4	V
$T_{PRE\_FB\_OV}$	$V_{PRE\_FB\_OV}$ filtering time	1	2	3	µs
V_{PRE_UVH}	Under voltage threshold high	2.9	—	3.1	V
V_{PRE_UVL}	Under voltage threshold low	2.5	—	2.7	V
T_{PRE_UV}	V_{PRE_UVH} and V_{PRE_UVL} filtering time	6	10	15	µs
VPRE_FSW	Switching Frequency Range (OTP configuration)	430	455	480	kHz
		2.1	2.22	2.35	MHz
L_{VPRE}	Typical inductor value for VPRE_FSW =455 kHz	3.3	4.7	6.8	µH
	Typical inductor value for VPRE_FSW =2.22 MHz	1	1.5	2.2	µH
	Typical inductor DCR value	—	10	—	mΩ
$V_{PRE\_LOAD\_REG}$	Transient load regulation Vsup= 6 V to 18 V, from 1 A to 3 A, di/dt = 300 mA/µs	-3	—	3	%
$V_{PRE\_LOAD\_REG}$	Transient load regulation, Vsup= 36 V, from 1 A to 3 A, di/dt = 300 mA/µs	-6	—	6	%
$V_{PRE\_LINE\_REG}$	Transient line regulation at 455 kHz, Vsup= 6 V to 18 V and Vsup=12 V to 36 V, dv/dt = 100 mV/µs	-3	—	3	%
R_{SHUNT}	Current sense resistor (±1%) for 455 kHz	10	—	20	mΩ
	Current sense resistor (±1%) for 2.22 MHz	15	—	20	mΩ
$V_{PRE\_LIM\_GAIN}$	Current sense amplifier gain	4.5	5	5.5	
$V_{PRE\_LIM\_TH1}$	Current sense amplifier peak detection threshold (OTP configuration), VPREILIM_OTP [1:0] Note: 150 mV setting is not available for 2.22 MHz	35	50	65	mV
		60	80	100	mV
		96	120	144	mV
		120	150	180	mV
I_{LIM_PRE}	Inductor peak current limitation range (R_{SHUNT} = 10 mΩ, $V_{PRE\_LIM\_TH1 = 120mV)}$), I_{LIM_PRE} = $V_{PRE\_LIM\_TH}$ / R_{SHUNT}	9.6	12	14.4	A
V_{PRE_DRV}	HS and LS gate driver output voltage	-	VBOS	—	V
$I_{PRE\_GATE\_DRV}$	HS and LS gate driver pull up and pull down current capability (OTP default configuration + I^2C configuration)	54	130	220	mA
		108	260	440	mA
		216	520	880	mA
		378	900	1540	mA
COUT_PRE	Effective output capacitor for 455 kHz	44	66	240	µF
	Effective output capacitor for 2.22 MHz	22	44	120	µF
	Output decoupling capacitor	—	0.1	—	µF
CIN_PRE	Effective input capacitor	20	—	—	µF

Table 11. Electrical characteristics*...continued*

Symbol	Parameter	Min	Typ	Max	Unit
	Input decoupling capacitor	—	0.1	—	µF
IPRE_DRV	HS / LS gate driver average current capability IPRE_DRV < FPRE_FSW x (QCHS + QCLS) with QCHS = gate charge of Q2 at VBOS with QCLS = gate charge of Q1 at VBOS	—	—	50	mA
gmEA	Error Amplifier transconductance	1	1.5	2.3	mS
VPRESC	Slope compensation (VPRESC_OTP configuration)	29	41.4	53.8	mV/µs
		43.5	62.1	80.7	mV/µs
		50.8	72.5	94.3	mV/µs
		57.8	82.5	107.3	mV/µs
		94	134.3	174.6	mV/µs
		101.2	144.6	188	mV/µs
		137.1	195.9	254.7	mV/µs
		352.8	504	655.2	mV/µs
TPRE_UV_DFS	VPRE_UVL filtering time to go to DEEP-FS during VPRE start up	1.8	2	2.2	ms
T_{PRE_DR}	Dead time to avoid cross conduction (this timing does not take into account the external FET turn ON/OFF times)	20	30	40	ns
VPRE_OFF_DLY_OTP	Wait time VPRE OFF (VPRE_OFF_DLY_OTP configuration)	—	250	—	µs
		—	32	—	ms
RPRE_DIS	Discharge resistor (when VPRE is disabled)	250	500	1000	Ω
RDRV_OFF	HS and LS gate driver pull-down resistor when VPRE is disabled	5	—	35	kΩ
RBOOT_OFF	PRE_BOOT pull-down resistor when VPRE is disabled	1.1	—	2.6	kΩ

10.5 VPRE external MOSFETs

MOSFETs selection:

- Logical level NMOS, gate drive comes from VBOS (5 V)
- VDS > 60 V for 24 V truck, bus applications
- VDS > 40 V for 12 V automotive applications
- Low Qg, <15 nC @Vgs=5 V is recommended for 455 kHz
- Low Qg, <7 nC @Vgs=5 V is recommended for 2.2 MHz

Table 12. Recommended external MOSFETS

Applications	Fpre	Ipre < 2A	Ipre < 4A	Ipre < 6A	Ipre < 10A
12V	455 kHz	BUK9K25-40E, BUCK9K18-40E	BUK9K25-40E, BUCK9K18-40E	BUK9K18-40E	BUK9K18-40E, NVTFS5C471NLWFTAG, HS = BUK9M9R5-40H, LS = BUK9M3R3-40H
	2.22 MHz	BUK9K25-40E BUK9Y29-40E	BUK9K25-40E BUK9Y29-40E	BUK9K25-40E BUK9Y29-40E	NA
24 V	455 kHz	BUK9K35-60E, BUK9K52-60E	BUK9K35-60E, BUK9K52-60E	BUK9K35-60E	BUK9K12-60E

Other MOSFETs can be used, provided their performance is similar to that of the recommended parts. The maximum current at 2.22 MHz is limited to 6 A, for which the efficiency is equivalent to 10 A at 455 kHz. Above that value, power dissipation in the external MOSFETs becomes important and the junction temperature may rise above 175 °C.

VPRE switching slew rates can be configured by I^2C to align with the external MOSFET selection and the VPRE switching frequency, and to optimize power dissipation and EMC performance. Configure the maximum slew rate by OTP and reduce it later by I^2C if needed.

VR5510 uses the current source to drive the external MOSFET, so adding an external serial resistor with the gate does not affect the slew rate. To adjust the slew rate, change the current source selection by I^2C.

VPRE MOSFET switching time can be estimated as $T_{SW} = (Q_{GD} + Q_{GS} / 2) / I_{PRE\_GATE\_DRV}$ using the gate charge definition from Figure 14 below. Q_{GD} and Q_{GS} can be extracted from the MOSFET data sheet.

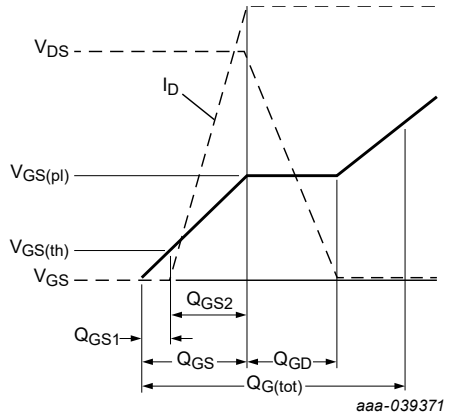
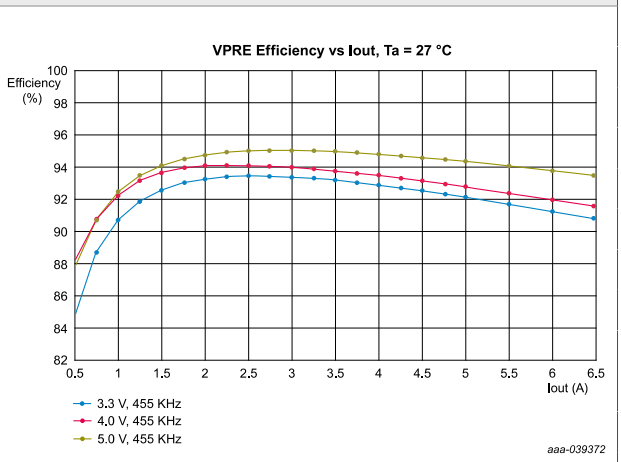


Figure 14. MOSFET gate charge definition

10.6 VPRE efficiency

VPRE efficiency versus current load is given for information based on the external component criteria provided and a VSUP voltage of 12 V.

Table 13. VPRE efficiency and the sample BOM used for measurement

Component	Type	Value	Unit	MFN Part #	
External Capacitors	Cin	44	µF	GCM32EC71H106KA03	
	ESR	3	mΩ		
	Cout	88	µF	GCM32ER71C226ME19	
	ESR	2.2	mΩ		
External Inductor	L	4.7	µH	XAL6060-472ME	
	DCR	13.1	mΩ		
External MOSFET	HS_Rdson	13.1	mΩ	NVMFD5C672NLT1G	
	LS_Rdson	13.1	mΩ		
	Qg_HS	6.4	nC		
	Qg_LS	6.4	nC		
	Vgs_HS	5	V		
	Vgs_LS	5	V		

10.7 VPRE PFM mode current load capability

In PFM mode, the current capability can be changed by the following parameters:

- Low power clock frequency: LOW_POWER_CLK [1:0],
- VPRE Typical TON in PFM mode: VPRE_PFM_TON_OTP[1:0].

Table 14. VPRE PFM current example with VPRE set to 3.3 V/5 V and VIN to 12 V for PFM TON

VPRE V	VPRE L	LOW POWER CLK	Typical PFM TON	Typical VPRE load in PFM
3.3 V	1.5 µH	100 kHz	300 ns	57 mA
			550 ns	212 mA
		300 kHz	300 ns	187 mA
			550 ns	690 mA
	4.7 µH	100 kHz	300 ns	20 mA
			550 ns	73 mA
		300 kHz	300 ns	60 mA
			550 ns	220 mA
5 V	1.5 µH	100 kHz	300 ns	32 mA
			550 ns	117 mA
		300 kHz	300 ns	105 mA
			550 ns	390 mA
	4.7 µH	100 kHz	300 ns	11 mA
			550 ns	41 mA
		300 kHz	300 ns	34 mA
			550 ns	124 mA

10.8 VPRE not populated

When two VR5510 are used, only one VPRE may be required. It is possible to not populate the external components of the second VPRE in order to reduce the number of items in the bill of materials.

In that case, specific connection of the VPRE2 pins is required:

- PRE_FB2 must be connected to PRE_FB1
- PRE_CSP2 must be connected to PRE_FB1
- PRE_COMP2 must be left open
- PRE_SW2 must be connected to GND
- PRE_BOOT2 must be connected to VBOS2
- PRE_GHS2 and PRE_GLS2 must be left open
- After the startup phase, VPRE2 must be disabled by I^2C with the VPREDIS bit.

11 Low Voltage Boost: VBOOST

11.1 Functional description

VBOOST block is a low voltage, asynchronous, peak current mode boost converter. VBOOST works in PWM and uses an external diode and an internal low-side FET. The BOOST regulator can be enabled using the BOOSTEN_OTP bit (CFG_ BOOST_ 2_OTP retister). The output voltage is configurable by OTP using the VBSTV_OTP[3:0] bitfield (CFG_BOOST_ 1_OTP register) from 4.5 V to 6 V. The switching frequency is 2.22 MHz and the output current is limited to a value set by the VBSTILIM_OTP[1:0] bitfield (CFG_BOOST_ 3_OTP register). The input of the boost is connected to the output of VPRE. Stability is ensured by an internal Type 2 compensation network with slope compensation.

By default, the VBOOST switching frequency is derived from the internal oscillator and can be synchronized with an external frequency signal applied on FIN input pin. The change from internal oscillator to external clock or vice versa is controlled by I^2C.

Overcurrent detection and thermal shutdown are implemented to protect the internal MOSFET. If an overcurrent is detected after the LS minimum TON time, the LS is turned off and is turned on again at the next rising edge of the switching clock. The overcurrent induces a duty cycle reduction that could lead to the output voltage gradually dropping, causing an undervoltage condition.

Because the current limitation is on the input current, the example in Table 15 summarizes the expected output current capability depending on VPRE and VBOOST voltage configurations for VBSTILIM_OTP[1:0] = 01.

Table 15. Output current example

VPRE	VBOOST	IBOOST_OUT
3.3 V	5 V	800 mA
4.4 V	5 V	1 A

An overvoltage protection is implemented on the BOOST_LS pin. When V_{BOOST_OV} is detected during two consecutive turn-on cycles, VBOOST is disabled. An I^2C command is required to enable it again. This monitoring is not safety related.

11.2 Application schematic

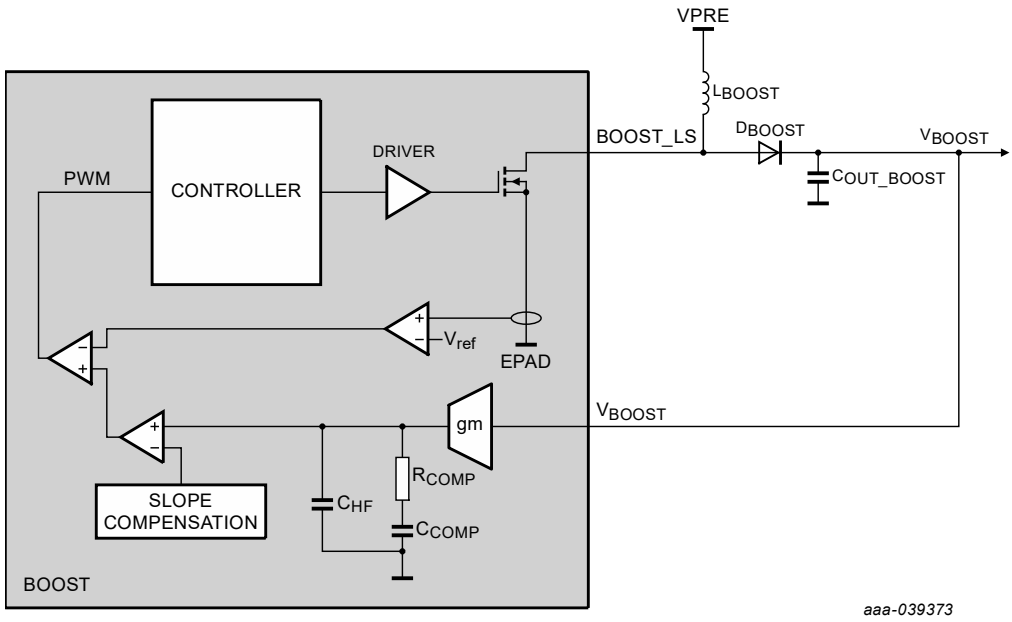


Figure 15. BOOST schematic

Select a Schottky diode for D_{BOOST} to limit the impact on the SMPS efficiency.

11.3 Compensation network and stability

The internal compensation network, made with R_{COMP}, C_{COMP}, and C_{HF} is optimized for the best compromise between stability and transient response. Depending on the current limit, the recommend settings should be:

For 3 A current limitation setting :

- Rcomp= 500 K, Ccomp= 125 pF, Slew rate= 500 V/µs, Slope Compensation= 67 mV/µs.

For 2 A current limitation setting:

- Rcomp= 750 K, Ccomp= 125 pF, Slew rate= 500 V/µs, Slope Compensation= 160 mV/µs.

11.4 Electrical characteristics

TA = –40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground. Typical values based on TA = 25 °C.

Table 16. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
VBOOST					
V_{BOOST}	Output Voltage (VBSTV_OTP[3:0] configuration)	—	4.5	—	V
		—	5	—	V
		—	5.09	—	V
		—	5.19	—	V
		—	5.4	—	V
		—	5.74	—	V
		—	6.0	—	V
$V_{BOOSTACC}$	Output Voltage Accuracy	-3	—	3	%
$V_{BOOST\_SOFT\_START}$	Soft start (from 10% to 90%)	250	500	750	µs
V_{BOOST_UVH}	Under voltage threshold high	3.3	—	3.7	V
T_{BOOST_UVH}	V_{BOOST_UVH} filtering time	6	10	15	µs
OV_{BOOST}	Over voltage protection threshold	7.4	—	7.9	V
V_{BOOST_SW}	Switching Frequency Range	—	2.22	—	MHz
L_{BOOST}	Inductor for V_{BOOST_SW} =2.22 MHz	—	4.7	—	µH
C_{OUT_BOOST}	Effective output capacitor	44	—	66	µF
$V_{BOOST\_LOAD\_REG1}$	Transient load regulation (C_{OUT_BOOST} = 44 µF, from 100 mA to 1 A, di/dt = 300 mA/µs)	-10	—	10	%
$V_{BOOST\_LOAD\_REG2}$	Transient load regulation (C_{OUT_BOOST} = 44 µF, from 50 mA to 100 mA, di/dt = 300 mA/µs)	-1	—	1	%
$V_{BOOST\_LOAD\_REG3}$	Transient load regulation (C_{OUT_BOOST} = 44 µF, from 100 mA to 200 mA, di/dt = 300 mA/µs)	-2	—	2	%
$V_{BOOST\_LOAD\_REG4}$	Transient load regulation (C_{OUT_BOOST} = 44 µF, from 100 mA to 500 mA, di/dt = 300 mA/µs)	-3.5	—	3.5	%
I_{LIM_BOOST}	Inductor peak current limitation range, VBSTILIM_OTP[1:0] = 01	1.5	2	2.5	A
	Inductor peak current limitation range, VBSTILIM_OTP[1:0] = 10	2.25	3	3.75	A
$T_{BOOST\_ON\_MIN}$	LS minimum ON time, VBSTTONTIME_OTP [1:0] = 00	40	—	80	ns
R_{BOOST_RON}	LS NMOS RDSon	—	150	280	mΩ
T_{BOOST_SR}	Switching output slew rate (OTP configuration + I^2C), VBSTSR_OTP [1:0] default + VBSTSR[1:0]	—	500	—	V/µs
gmEA	Error Amplifier transconductance	3.5	7	10	S
V_{BOOST_SLOPE}	Slope Compensation (default value for 2 A current limit) VBSTSC_OTP[4:0] = 00110	—	160	—	mV/µs
	Slope Compensation (default value for 3 A current limit) VBSTSC_OTP[4:0] = 01111	—	67	—	mV/µs
TSD_{BOOST}	Thermal shutdown threshold	155	—	—	°C
T_{BOOST_TSD}	Thermal shutdown filtering time	—	20	30	µs

11.5 VBOOST not populated

VBOOST may not be required when VPRE is configured at greater than 3.9 V. In this case, the external VBOOST components can be unpopulated to reduce the number of items in the bill of materials. The BOOSTEN_OTP bit (CFG_BOOST_ 2_OTP register) must be programmed to 0 and the VBOOST pin must be pulled up to VPRE. BOOST_LS pin must be left open.

VBOOST must be used to supply VBOS when VPRE is configured below 3.9 V.

12 Low Voltage Buck: BUCK1 and BUCK2

12.1 Functional description

BUCK1 and BUCK2 blocks are low voltage, synchronous, valley current mode buck converters with integrated HS PMOS and LS NMOS. BUCK1 and BUCK2 work in force PWM in Normal mode of operation and in PFM in Standby mode. The output voltage is configurable by OTP through the BUCK1V_OTP [7:0] bit field (CFG_ BUCK1_ 1_OTP register) or the BUCK2V_OTP [7:0] bit field (CFG_ BUCK2_ 1_OTP register) from 0.4 V to 1.8 V, the switching frequency is 2.22 MHz and the output current is limited to a maximum of 3.6 A peak. The input of the BUCK1 and BUCK2 blocks must be connected to the output of VPRE. Stability is ensured by an internal Type 2 compensation network with slope compensation.

By default, BUCK1 and BUCK2 switching frequencies are derived from the internal oscillator and can be synchronized with an external frequency signal applied on FIN input pin. The change from internal oscillator to external clock or vice versa is controlled by I^2C.

BUCK1 and BUCK2 can work independently or in dual-phase mode to double the output current capability. Dual-phase mode is configured by OTP. When BUCK1 and BUCK2 are used in dual-phase, they must have the same output voltage configuration. Any action (such as TSD, OV or being disabled by I^2C) on BUCK1 affects BUCK2 and vice versa.

Overcurrent detection and thermal shutdown are implemented on BUCK1 and BUCK2 to protect the internal MOSFETs. An overcurrent induces a duty cycle reduction that could lead to the output voltage gradually dropping, causing an under voltage condition.

Use soft ramp when the regulators are enabled or disabled with SVS control. Programmable phase shift control is implemented (see Section 18 "Clock Management").

12.2 Application schematic: single phase mode

In this configuration, BUCK1 and BUCK2 are configured as independent outputs. Each output is configured and controlled independently by I^2C.

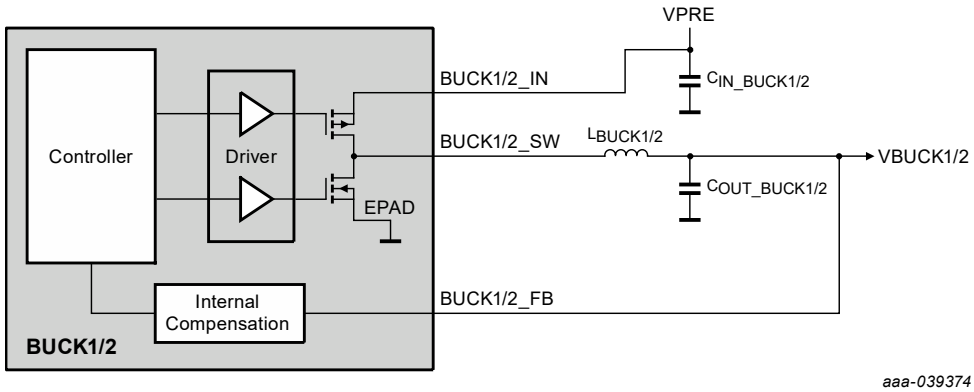


Figure 16. BUCK1/2 standalone schematic

12.3 Application schematic: dual-phase mode

In this configuration, BUCK1 and BUCK2 are configured in dual-phase mode to double the output current capability. Dual-phase mode is enabled by OTP via the VB12MULTIPH_OTP bit (CFG_ BUCK1_ 2_OTP register). The PCB layout of BUCK1 and BUCK2 must be symmetric for optimum EMC performance.

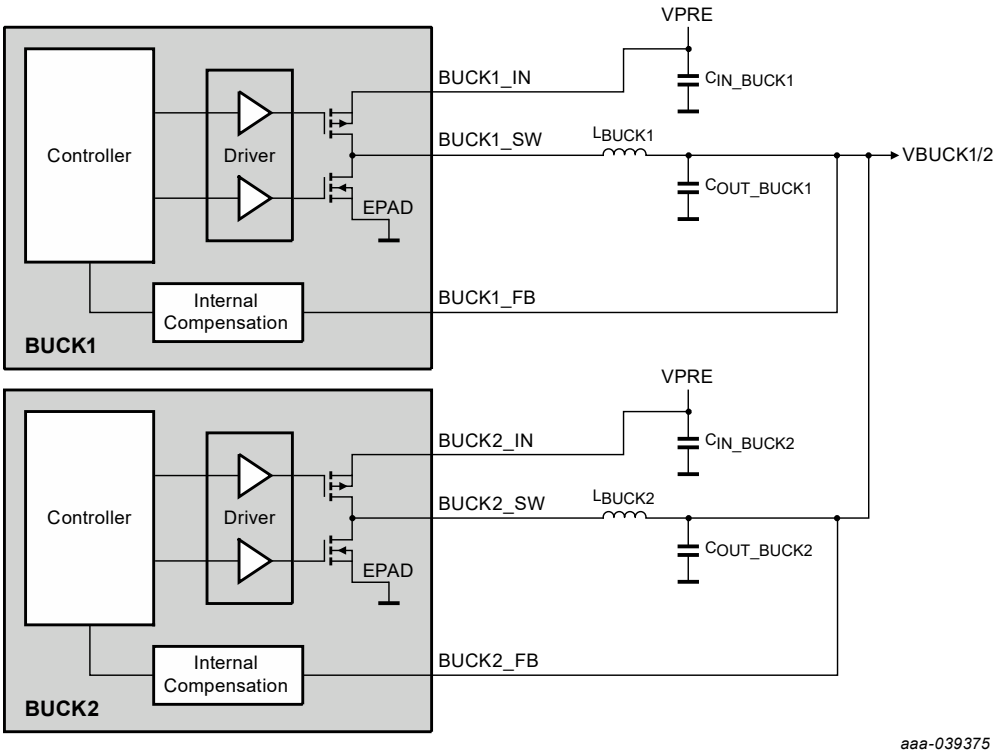


Figure 17. BUCK1/2 dual-phase schematic

12.4 Compensation network and stability

The internal compensation network ensures the stability and the transient response performance of the buck converter. The error amplifier gain is configurable with the

BUCKx_COMP_OTP[2:0] bitfields (CFG_ BUCK3_ 2_OTP register) for each BUCK 1 and BUCK2 regulator. Use the default value, which should cover most use cases.

12.5 Electrical characteristics

TA = –40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground. Typical values based on TA = 25 °C.

Table 17. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
BUCK1 and BUCK2					
V_{BUCK12_IN}	Input voltage range	2.5	—	5.5	V
V_{BUCK12}	Output voltage, Configurable by OTP, 6.25 mV resolution (<1.5 V)	0.4	—	1.8	V
I_{BUCK12}	Recommended DC output current capability (one phase)	—	2.5	—	A
$V_{BUCK12ACC}$	Output voltage accuracy (0.4 V< V_{BUCK12} < 0.7 V), PWM	-10	—	10	mV
	Output voltage accuracy (0.7 V ≤ V_{BUCK12} ≤ 0.8 V), PWM	-8	—	8	mV
	Output voltage accuracy (0.8 V< V_{BUCK12}≤ 1.5 V), PWM	-1.5	—	1.5	%
	Output voltage accuracy (V_{BUCK12} = 1.8 V), PWM	-2	—	2	%
	Output voltage accuracy (0.4 V< V_{BUCK12}< 1.5 V), PFM	- 30	—	30	mV
	Output voltage accuracy (V_{BUCK12} = 1.8 V), PFM	- 40	—	40	mV
I_{BUCK12_Q}	Quiescent Current, PFM Mode, VSUP = 12 V	—	12	—	µA
V_{BUCK12_SW}	Switching Frequency Range	2.1	2.22	2.35	MHz
L_{BUCK12}	Inductor for V_{BUCK12_SW} =2.22 MHz	—	1.0	—	µH
C_{OUT_BUCK12}	Effective output capacitor (for 1 phase)	35	—	160	µF
	Output decoupling capacitor	—	0.1	—	µF
C_{IN_BUCK12}	Effective input capacitor (one each close to BUCK1_IN and BUCK2_IN pins)	4.23	—	—	µF
	Input decoupling capacitor (one each close to BUCK1_IN and BUCK2_IN pins)	—	0.1	—	µF
V_{BUCK12_TLR}	Transient Load Regulation for V_{BUCK12} <1.2 V (Cout = 44 µF, from 200 mA to 1 A, di/dt = 2 A/µs) single phase (Cout = 44 µF, from 400 mA to 2 A, di/dt = 4 A/µs) dual phase	-25	—	+25	mV
V_{BUCK12_TLR}	Transient Load Regulation for V_{BUCK12} >1.2 V (Cout = 44 µF, from 200 mA to 1 A, di/dt = 2 A/µs) single phase (Cout = 44 µF, from 400 mA to 2 A, di/dt = 4 A/µs) dual phase	-3	—	+3	%
I_{LIM_BUCK12}	Inductor peak current limitation range for one phase (OTP configuration)	2.4	3	3.7	A
		3.6	4.5	5.45	A
$V_{BUCK12\_DVS\_UP}$ (0.4 V to 1.5 V)	DVS Ramp up Speed , BUCK12DVS_RAMP_OTP[1:0] = 00	9.5	15.6	23.6	mV/µs
	DVS Ramp up Speed , BUCK12DVS_RAMP_OTP[1:0] = 01	4.8	7.8	11.8	mV/µs
	DVS Ramp up Speed , BUCK12DVS_RAMP_OTP[1:0] = 10	1.56	2.6	3.94	mV/µs
	DVS Ramp up Speed , BUCK12DVS_RAMP_OTP[1:0] = 11	1.33	2.23	3.38	mV/µs

Table 17. Electrical characteristics*...continued*

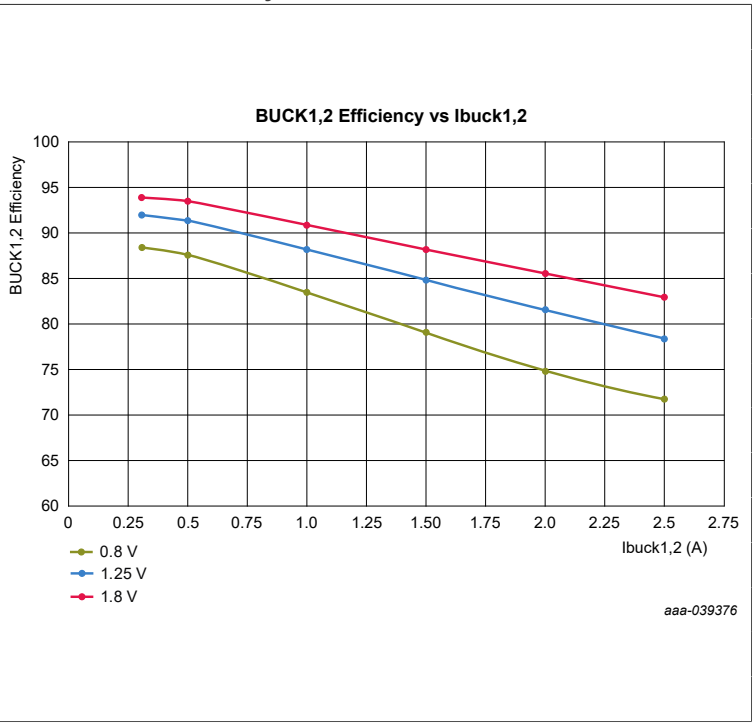
Symbol	Parameter	Min	Typ	Max	Unit
$V_{BUCK12\_DVS\_UP}$ (1.8 V)	DVS Ramp up Speed , BUCK12DVS_RAMP_OTP[1:0] = 00	11.87	19.53	29.5	mV/µs
	DVS Ramp up Speed , BUCK12DVS_RAMP_OTP[1:0] = 01	6	9.76	14.75	mV/µs
	DVS Ramp up Speed , BUCK12DVS_RAMP_OTP[1:0] = 10	1.95	3.25	4.92	mV/µs
	DVS Ramp up Speed , BUCK12DVS_RAMP_OTP[1:0] = 11	1.67	2.78	4.22	mV/µs
$V_{BUCK12\_DVS\_DOWN}$ (0.4 V to 1.5 V)	DVS Ramp down Speed , BUCK12DVS_RAMP_OTP[1:0] = 00	6.3	10.41	15.8	mV/µs
	DVS Ramp down Speed , BUCK12DVS_RAMP_OTP[1:0] = 01	3.1	5.2	7.9	mV/µs
	DVS Ramp down Speed , BUCK12DVS_RAMP_OTP[1:0] = 10	1.56	2.6	3.94	mV/µs
	DVS Ramp down Speed , BUCK12DVS_RAMP_OTP[1:0] = 11	1.33	2.23	3.38	mV/µs
$V_{BUCK12\_DVS\_DOWN}$ (1.8 V)	DVS Ramp down Speed , BUCK12DVS_RAMP_OTP[1:0] = 00	7.87	13.02	19.75	mV/µs
	DVS Ramp down Speed , BUCK12DVS_RAMP_OTP[1:0] = 01	3.87	6.51	9.87	mV/µs
	DVS Ramp down Speed , BUCK12DVS_RAMP_OTP[1:0] = 10	1.95	3.25	4.92	mV/µs
	DVS Ramp down Speed , BUCK12DVS_RAMP_OTP[1:0] = 11	1.67	2.78	4.22	mV/µs
$T_{BUCK12\_OFF\_MIN}$	HS minimum OFF time	9	27	54	ns
$R_{BUCK12\_HS\_RON}$	HS PMOS RDSon, 3.6 Vgs, Tj = 125 C	—	—	135	mΩ
$R_{BUCK12\_LS\_RON}$	LS NMOS RDSon, 3.6 Vgs, Tj = 125 C	—	—	80	mΩ
R_{BUCK12_DISch}	Discharge Resistance (when BUCK1,2 is disabled and ramp down completed)	—	20	40	Ω
TSD_{BUCK12}	Thermal shutdown threshold	155	—	—	°C
T_{BUCK12_TSD}	Thermal shutdown filtering time	—	20	30	µs

12.6 BUCK1 and BUCK2 efficiency

Table 18 shows BUCK1 and BUCK2 efficiency versus current load based on a typical external component and a 4.1 V VPRE voltage. For external components with characteristics different from the ones shown below, use the VR5510 Power Calculator tool to recalculate the theoretical efficiency. The real efficiency must be verified by measurement at the application level.

Table 18. BUCK1 and BUCK2 theoretical efficiency

Ext. C and L		
Cin	60	µF
ESR Cin	10	mΩ
Cout	44	µF
ESR Cout	10	mΩ
L coil	1	µH
DCR coil	30	mΩ
Int. MOSFET		
HS_Rdson	135	mΩ
QH	0.5	nC
THS_sw	5	ns
GHS_drive	5	V
LS-Rdson	80	mΩ
QLS	0.5	nC
TLS_sw	5	ns
GLS_drive	5	V



13 Low Voltage Buck: BUCK3

13.1 Functional description

BUCK3 is a low voltage, synchronous, peak current mode buck converter with integrated HS PMOS and LS NMOS. BUCK3 works in force PWM in Normal mode and in PFM in the Standby mode. The output voltage is configurable by OTP through the BUCK3V_OTP [4:0] bit field (CFG_ BUCK3_ 1_OTP) from 1.0 V to 4.1 V, the switching frequency is 2.22 MHz, and the output current is limited to 3.6 A peak. The input of BUCK3 must be connected to the output of VPRE. Stability is ensured by an internal Type 2 compensation network with slope compensation.

By default, the BUCK3 switching frequency is derived from the internal oscillator and can be synchronized with an external frequency signal applied on FIN input pin. The change from internal oscillator to external clock or vice versa is controlled by I^2C.

Overcurrent detection and thermal shutdown are implemented on BUCK3 to protect the internal MOSFETs. An overcurrent induces a duty cycle reduction that could lead to the output voltage gradually dropping, causing an undervoltage condition.

Programmable phase shift control is implemented (see Section 18 "Clock Management").

13.2 Application schematic

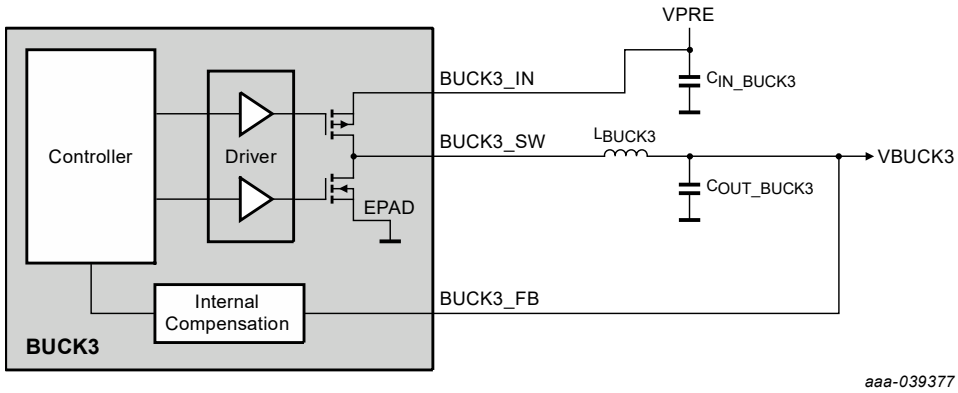


Figure 18. BUCK3 schematic

13.3 Compensation network and stability

The internal compensation network ensures the stability and the transient response performance of the buck converter.

Use the default values for BUCK3_GM_OTP bit (CFG_ BUCK2_ 2_OTP register) and BUCK3_RS_OTP, which should cover most use cases.

BUCK3_LSELECT_OTP[1:0] (CFG_ BUCK3_ 1_OTP register) scales the slope compensation and the Zero Cross Detection according to inductor value. The recommended inductor value for BUCK3 is1.0 µH.

13.4 Electrical characteristics

TA = –40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground. Typical values based on TA = 25 °C.

Table 19. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
BUCK3					
V_{BUCK3_IN}	Input voltage range	2.5	—	5.5	V
V_{BUCK3}	Output voltage, OTP settings available: 1.0 V, 1.1 V, 1.2 V, 1.25 V, 1.3 V, 1.35 V, 1.5 V, 1.6 V, 1.8 V 1.85 V, 2.0 V, 2.1 V, 2.15 V, 2.25 V, 2.3 V, 2.4 V, 2.5 V, 2.8 V, 3.15 V, 3.2 V, 3.25 V, 3.3 V, 3.35 V, 3.4 V, 3.5 V, 3.8 V, 4.0 V, 4.1 V	1.0	—	4.1	V
I_{BUCK3}	Recommended DC output current capability	—	2.5	—	A
$V_{BUCK3ACC}$	Output Voltage Accuracy, PWM	-2	—	2	%
	Output Voltage Accuracy, PWM, 1.1 V setting	-1	—	1	%
	Output Voltage Accuracy, PFM	-3	—	3	%
I_{BUCK3_Q}	Quiescent Current, PFM Mode, VSUP = 12 V	—	12	—	µA
V_{BUCK3_SW}	Switching Frequency Range	2.1	2.22	2.35	MHz

Table 19. Electrical characteristics*...continued*

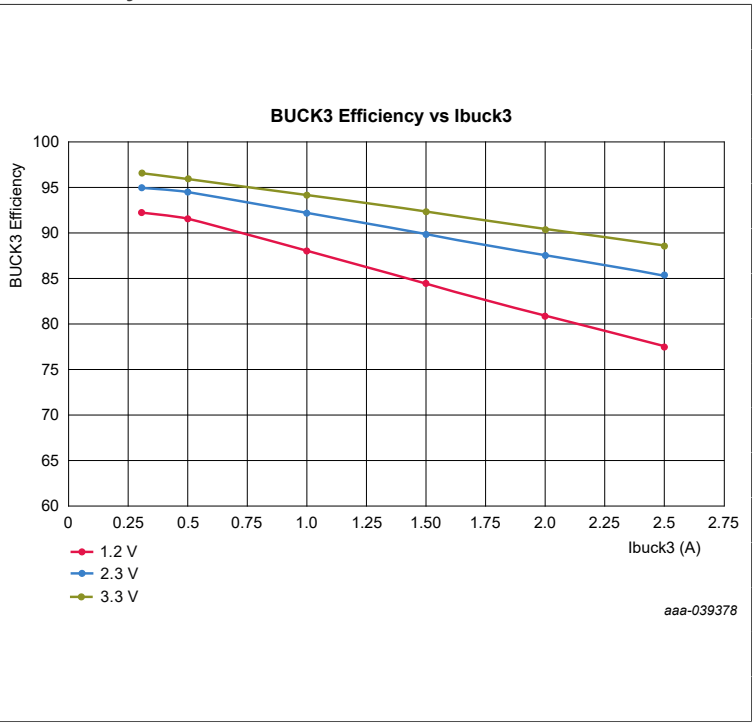
Symbol	Parameter	Min	Typ	Max	Unit
L_{BUCK3}	Inductor for V_{BUCK3_SW} =2.22 MHz	—	1.0	—	µH
C_{OUT_BUCK3}	Effective output capacitor	35	—	132	µF
	Output decoupling capacitor	—	0.1	—	µF
C_{IN_BUCK3}	Effective input capacitor (close to BUCK3_IN pin)	4.23	—	—	µF
	Input decoupling capacitor (close to BUCK3_IN pin)	—	0.1	—	µF
V_{BUCK3_TLR}	Transient Load Regulation (Cout = 44 µF, from 200 mA to 1 A, di/dt = 2 A/µs)	-50	—	50	mV
I_{LIM_BUCK3}	Inductor peak current limitation range (OTP configuration)	2.4	3	3.7	A
		3.6	4.5	5.45	A
$T_{BUCK3\_ON\_MIN}$	HS minimum ON time	5	50	80	ns
$V_{BUCK3\_DVS\_UP\_DOWN}$	DVS Ramp up/down Speed , BUCK3_RAMP_OTP[1:0] = 00	6	10.42	15	mV/µs
	DVS Ramp up/down Speed , BUCK3_RAMP_OTP[1:0] = 01	2	3.47	5	mV/µs
	DVS Ramp up/down Speed , BUCK3_RAMP_OTP[1:0] = 10	1.5	2.6	3.5	mV/µs
	DVS Ramp up/down Speed , BUCK3_RAMP_OTP[1:0] = 11	1	2.08	3	mV/µs
$V_{BUCK3\_SOFT\_START}$	Soft start (from 10% to 90%)	—	—	200	µs
$R_{BUCK3\_HS\_RON}$	HS PMOS RDSon	—	—	135	mΩ
$R_{BUCK3\_LS\_RON}$	LS NMOS RDSon	—	—	80	mΩ
$R_{dischBUCK3}$	Discharge Resistance (when BUCK3 is disabled)	—	20	40	Ω
TSD_{BUCK3}	Thermal shutdown threshold	155	—	—	°C
T_{BUCK3_TSD}	Thermal shutdown filtering time	—	20	30	µs

13.5 BUCK3 efficiency

Table 20 shows BUCK3 efficiency versus current load based on a typical external component and a 4.1 V VPRE voltage. For external components with characteristics different from the ones shown below, use the VR5510 Power Calculator tool to recalculate the theoretical efficiency. The real efficiency must be verified by measurement at the application level.

Table 20. BUCK3 theoretical efficiency

Ext. C and L		
Cin	60	µF
ESR Cin	10	mΩ
Cout	44	µF
ESR Cout	10	mΩ
L coil	1	µH
DCR coil	30	mΩ
Int. MOSFET		
HS_Rdson	135	mΩ
QH	0.5	nC
THS_sw	5	ns
GHS_drive	5	V
LS-Rdson	80	mΩ
QLS	0.5	nC
TLS_sw	5	ns
GLS_drive	5	V



14 Linear Voltage Regulator: LDO1

14.1 Functional description

LDO1 is a medium voltage linear regulator. The output voltage is configurable from 1.1 V to 5 V by OTP through the LDO1V_OTP [2:0] bit field (CFG_ LDO_ ALL2_OTP register). A minimum voltage drop is required, depending on the output current capability (0.5 V for 150 mA and 1 V for 400 mA). The LDO current capability is linear with the voltage drop and can be estimated to I(mA) = 500 x V_{LDO1_DROP} -100 for an intermediate voltage drop between 0.5 V and 1 V.

Overcurrent detection and a thermal shutdown are implemented on LDO1 to protect the internal pass device.

14.2 Application schematics

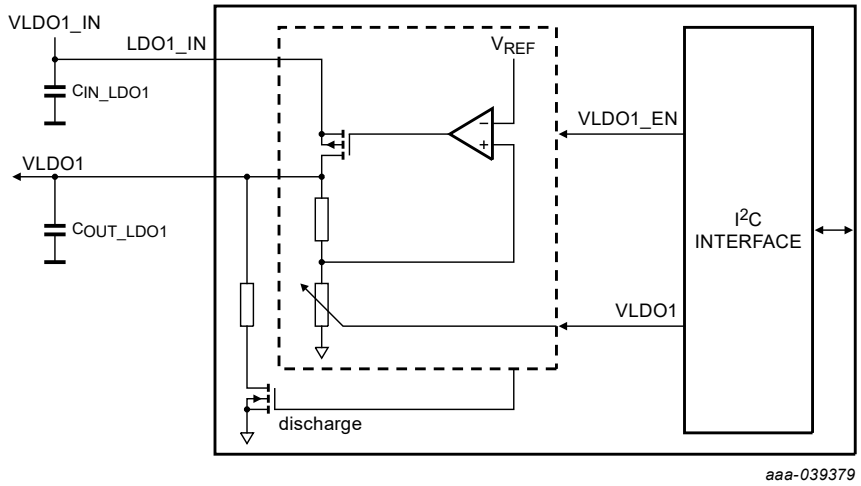


Figure 19. LDO1 block diagram

14.3 Electrical characteristics

TA = –40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground. Typical values based on TA = 25 °C.

Table 21. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
LDO1					
V_{LDO1_IN}	Input voltage range	2.5	—	6.5	V
V_{LDO1}	Output voltage, OTP settings available: 1.1 V, 1.2 V, 1.6 V, 1.8 V, 2.5 V, 2.8 V, 3.3 V, 5.0 V	1.1	—	5.0	V
V_{LDO1_ACC}	Output Voltage accuracy	-2	—	+2	%
$V_{LDO1\_DROP\_150}$	Minimum Voltage drop for 150 mA current capability	0.5	—	—	V
$V_{LDO1\_DROP\_400}$	Minimum Voltage drop for 400 mA current capability	1.0	—	—	V
I_{LDO1_Q}	Quiescent Current, No load, VSUP = 12 V	—	40	—	µA
C_{IN_LDO1}	Input capacitor (close to LDO1_IN pin)	1.0	—	—	µF
$C_{OUT\_LDO1\_150}$	Effective output capacitor, 150 mA current capability	3	—	100	µF
$C_{OUT\_LDO1\_400}$	Effective output capacitor, 400 mA current capability	4.5	—	100	µF
C_{OUT_LDO1}	Output decoupling capacitor	0.1	—	—	µF
$V_{LDO1\_LTR\_150}$	Transient Load Regulation (from 10 mA to 150 mA in 2 µs)	-4	—	+4	%
$V_{LDO1\_LTR\_400}$	Transient Load Regulation (from 10 mA to 400 mA in 4 µs)	-5	—	+5	%
V_{LDO1_LR}	Line Regulation	—	—	0.5	%
$V_{LDO1\_ILIM\_150}$	Current limitation, 150 mA current capability	180	280	500	mA
$V_{LDO1\_ILIM\_400}$	Current limitation, 400 mA current capability	460	560	850	mA

Table 21. Electrical characteristics*...continued*

Symbol	Parameter	Min	Typ	Max	Unit
$V_{LDO1\_SOFT\_START}$	Soft start (Enable to 90%)	0.7	1	1.3	ms
R_{LDO1_DISCH}	Discharge Resistance (when LDO1 is disabled)	—	20	40	Ω
TSD_{LDO1}	Thermal shutdown threshold	155	—	—	°C
T_{LDO1_TSD}	Thermal shutdown filtering time	—	20	30	µs

15 Linear Voltage Regulator: LDO2, LDO3

15.1 Functional description

The LDO2 and LDO3 blocks are linear voltage regulators. The output voltage is configurable from 1.5 V to 5 V by OTP through the LDO2V_OTP [3:0] bit field (CFG_ LDO_ ALL2_OTP register) and the LDO3V_OTP [3:0] (CFG_ LDO_ ALL1_OTP registers).

LDO2 and LDO3 can be programmed to operate in load switch mode by OTP through the LDO2_LS_OTP and LDO3_LS_OTP bits (both in the CFG_ SEQ_ 1_OTP).

In load switch mode, the input supply must be kept within the LDO operating input voltage range (2.5 V to 5.5 V).

The LDO2 and LDO3 input supplies are externally connected to VPRE. Overcurrent detection and a thermal shutdown are implemented on LDO2 and LDO3 to protect the internal pass device.

15.2 Application schematics

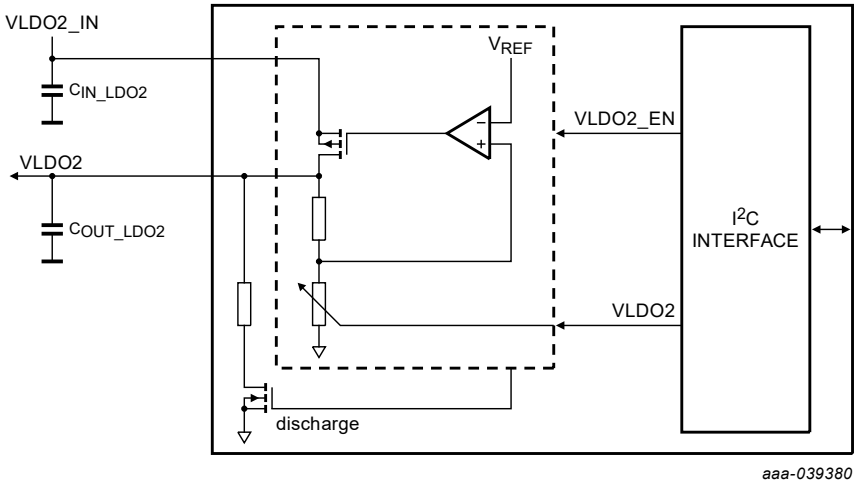


Figure 20. LDO2 block diagram

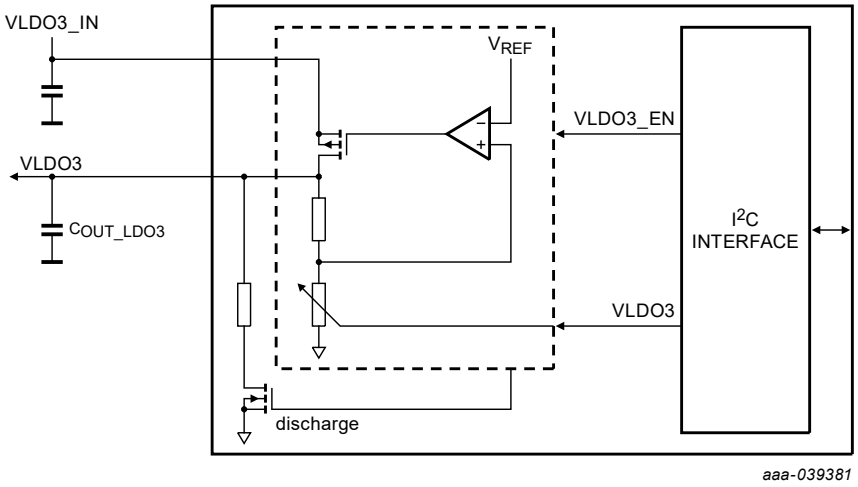


Figure 21. LDO3 block diagram

15.3 Electrical characteristics

TA = –40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground. Typical values based on TA = 25 °C.

Table 22. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
LDO2 and LDO3					
V_{LDO23_IN}	Input voltage range (1.5 V < VLDO23 < 2.25 V)	2.5	—	5.5	V
V_{LDO23_IN}	Input voltage range (2.25 V < VLDO23 < 5 V)	VLDO23 + 0.25	—	5.5	V
V_{LDO23}	Output voltage, OTP settings available: 1.5 V, 1.6 V, 1.8 V, 1.85 V, 2.15 V, 2.5 V, 2.8 V, 3.0 V, 3.1 V, 3.15 V, 3.2 V, 3.3 V, 3.35 V, 4 V, 4.9 V, 5.0 V	1.5	—	5.0	V
V_{LDO23_ACC}	Output Voltage accuracy, 400 mA current capability	-2	—	+2	%
I_{LDO23_Q}	Quiescent Current, No load, VSUP = 12 V	—	7	—	µA
C_{IN_LDO23}	Input capacitor (close to LDO23_IN pin)	1.0	—	—	µF
C_{OUT_LDO23}	Effective output capacitor	3.3	—	100	µF
C_{OUT_LDO23}	Output decoupling capacitor	—	0.1	—	µF
V_{LDO23_LTR}	Transient Load Regulation (from 10 mA to 200 mA in 2 us)	-6	—	6	%
V_{LDO23_LR}	Line Regulation, V_{LDOxIN} = 2.5 V, 10 us	-5	—	5	%
V_{LDO23_ILIM}	Current limitation, LDO mode	450	850	1475	mA
$V_{LDO23\_ILIM\_SWITCH}$	Current limitation, Switch mode	450	850	1475	mA
R_{LDO23_RON}	LDO23 RDSon (drop-out / load switch)	—	—	220	mΩ
$V_{LDO23\_SOFT\_START}$	Soft start (Enable to 90%)	130	220	360	µs
R_{LDO23_DISCH}	Discharge Resistance (when LDO2,3 is disabled)	—	20	40	Ω

Table 22. Electrical characteristics*...continued*

Symbol	Parameter	Min	Typ	Max	Unit
TSD_{LDO23}	Thermal shutdown threshold	155	—	—	°C
T_{LDO23_TSD}	Thermal shutdown filtering time	—	20	30	µs

16 Linear Voltage Regulator: HVLDO

16.1 Functional description

HVLDO is a high-voltage, low-power, low drop-out linear regulator. The regulator can be programmed via the HVLDO_TRANS_MODE_OTP bit (CFG_SEQ_4_OTP register) to operate as a load switch in Normal mode and an LDO in Standby mode or to operate as an LDO all of the time. The output voltage is OTP-configurable to either 0.8 V or 3.3 V through the HVLDOV_OTP [1:0] bit field (CFG_ SEQ_ 2_OTP register).

In Deep Sleep mode, HVLDO is the only supply enabled. In that case, HVLDO must be set to 3.3 V.

HV_HVLDO_IN is connected to either VPRE or VBAT and LV_HVLDO_IN can be connected to either VBUCK1/2 or VPRE.

If HVLDO is enabled in Normal mode and configured as disabled in Standby mode, then the HVLDO cannot automatically restart when the device wakes up from STBY mode. In that case, it must be enabled via I^2C.

16.2 Application schematics

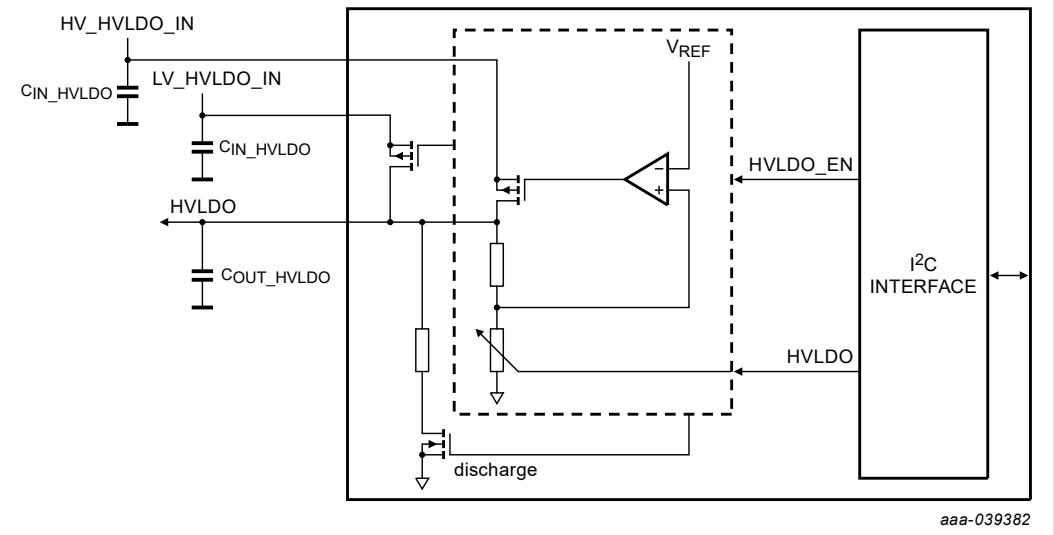


Figure 22. HVLDO block diagram

16.3 Electrical characteristics

TA = –40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground. Typical values based on TA = 25 °C.

Table 23. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
HVLDO					
V_{HVLDO_IN}	Input voltage range, HV_HVLDO_IN, HVLDO = 0.8 V	2.7	—	60	V
V_{HVLDO_IN}	Input voltage range, HV_HVLDO_IN, HVLDO = 3.3 V	3.8	—	60	V
V_{HVLDO_IN}	Input voltage range, LV_HVLDO_IN, Load Switch Input (0.8 VOUT)	0.69	—	0.88	V
V_{HVLDO_IN}	Input voltage range, LV_HVLDO_IN, Load Switch Input (3.3 VOUT)	2.97	—	5.5	V
V_{HVLDO_ACC}	Output Voltage accuracy in LDO mode, 0.8 V	0.784	0.8	0.816	V
	Output Voltage accuracy in LDO mode, 3.3 V	3.2	3.3	3.4	V
I_{HVLDO_Q}	Quiescent Current, No load, VSUP = 12 V	—	10	—	µA
C_{IN_HVLDO}	Effective input capacitor (close to HVLDO_IN pin)	—	1.0	—	µF
C_{OUT_HVLDO}	Effective output capacitor	2.2	—	—	µF
	Output decoupling capacitor	—	0.1	—	µF
V_{HVLDO_LTR}	Transient Load Regulation, Low Power LDO to Normal Switch Mode	-4	—	4	%
$V_{HVLDO\_ILIM\_LDO}$	Current limitation, LDO Mode, 10 mA capability	11	—	40	mA
$V_{HVLDO\_ILIM\_SW}$	Current limitation, Switch Mode, 100 mA capability	110	—	350	mA
$V_{HVLDO\_SOFT\_START}$	Soft start (Enable to 90%), Switch Mode	—	—	250	µs
$V_{HVLDO\_SOFT\_START}$	Soft start (Enable to 90%), LDO Mode	—	—	1	ms
R_{HVLDO_ON}	ON Resistance, Switch Mode, 0.8 V	—	—	1	Ω
	ON Resistance, Switch Mode, 3.3 V	—	—	1.5	Ω
$R_{HVLDO\_DISCH\_DIS}$	Discharge Resistance (when HVLDO is disabled)	—	60	100	Ω
TSD_{HVLDO}	Thermal shutdown threshold	155	—	—	°C
T_{HVLDO_TSD}	Thermal shutdown filtering time	—	20	30	µs

17 Thermal Management

17.1 Functional description

The VR5510 device has an independent thermal monitor sensor for each regulator. When a thermal shutdown threshold is exceeded, each monitor can be programmed to simply shutdown the regulator or to shutdown the regulator and transition the device into the Deep Fail-safe state.

When the regulator shutdown only setting is selected, the regulator starts up automatically when the temperature goes down.

At each startup, a BIST is run to assure that each TSD sensor is not stuck high or low. The results can be checked in the TSD_BIST_ERR_FLG bit (M_INT_MASK2 register).

A thermal sensor at the center of the die generates interrupts for the MCU whenever the temperature exceeds a certain threshold. The center die temperature threshold is programmable through the DIE_CENTER_TEMP_OTP [2:0] bit field (CFG_SM_ 2_OTP register).

Table 24. Center die temperature thresholds

DIE_CENTER_TEMP_OTP	Threshold (±10 °C)
000	75 °C
001	90 °C
010	105 °C
011	120 °C
100	135 °C
101	150 °C

17.2 Electrical characteristics

TA = –40 °C to 125 °C, unless otherwise specified.

Table 25. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Thermal Monitor					
TSD_{REG}	Thermal shutdown threshold for all independent thermal shutdown	155	—	175	°C
TSD_{HYST}	Thermal shutdown threshold hysteresis	1	—	10	°C
T_{TSD}	Thermal shutdown filtering time	—	20	30	µs

18 Clock Management

18.1 Clock description

The clock management block consists of a 20 MHz internal oscillator, a low power 100 kHz to 600 kHz oscillator, a Phase Locked Loop (PLL), and multiple dividers. This block generates the clock used by the internal digital state machines, by the switching regulators, and for external clock synchronization.

The internal oscillator runs at 20 MHz by default after startup. The frequency is programmable by I^2C. A spread spectrum feature can be activated by I^2C to mitigate the effects of EMI by spreading the energy of the oscillator's fundamental frequency.

The VPRE switching frequency comes from CLK2 (455 kHz) or CLK1 (2.22 MHz). The BUCK1, BUCK2, BUCK3, and BOOST switching frequency comes from CLK1 (2.22 MHz). The switching regulators can be synchronized with an external frequency coming from the FIN pin. A dedicated watchdog monitor verifies and reports the correct FIN frequency range. Different clocks can be sent to the FOUT pin to synchronize an external IC or for diagnostic purposes.

The device selects the internal clock if the SYNCIN signal is lost, but the PLL_LOCK bit randomly asserts low, or remains high when repeatedly applying and removing SYNCIN.

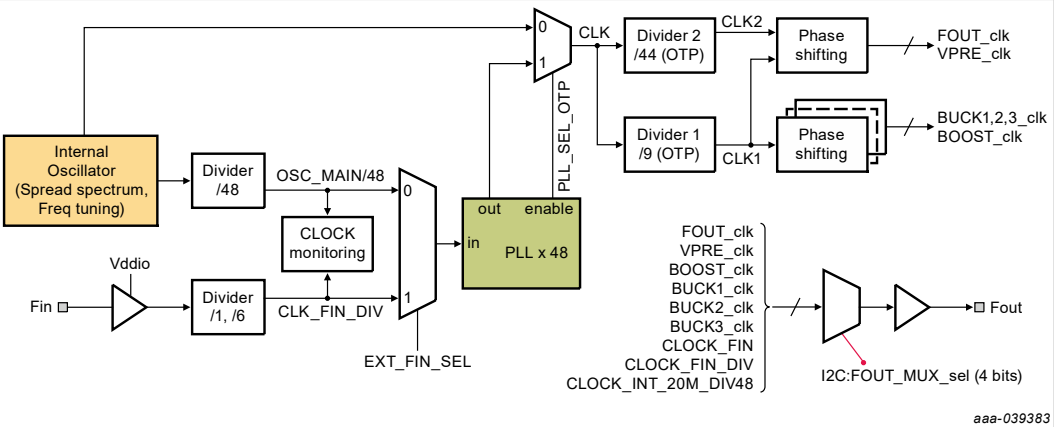


Figure 23. Clock management block diagram

18.2 Phase shifting

To reduce peak current and improve EMC performance, the clocks of the switching regulators (VPRE_clk, BOOST_clk, BUCK1_clk, BUCK2_clk, and BUCK3_clk) can be delayed to prevent all regulators from turning on at the same time.

Each clock of each regulator can be shifted from one to seven CLK clock cycles running at 20 MHz, which corresponds to 50 ns. The phase shift configuration is done by using VPRE_PH_OTP[2:0], VBST_PH_OTP[2:0], BUCK1_PH_OTP[2:0] (CFG_ CLOCK_ 2_OTP register), BUCK2_PH_OTP[2:0] (CFG_ CLOCK_ 3_OTP register), and BUCK3_PH_OTP[2:0] (CFG_ CLOCK_ 3_OTP register).

VPRE and BUCK3 have a peak current detection architecture. The PWM synchronizes the turning on of the High Side switch. BUCK1 and BUCK2 have a valley current detection architecture. The PWM synchronizes the turning on of the Low Side switch.

18.3 Manual frequency tuning

The internal oscillator frequency (20 MHz by default) can be programmed by I^2C commands to frequencies ranging from 16 MHz to 24 MHz in 1 MHz steps. The oscillator's functionality is guaranteed for frequency increments of one step at a time in either direction, with a minimum of 10 µs between steps. For any unused code in the CLK_INT_FREQ [3:0] bit field (M_CLOCK1 register), the internal oscillator is set at the default 20 MHz frequency.

To change the internal oscillator frequency from 20 MHz to 24 MHz, four I^2C commands are required with a 10 µs wait time between each command. To change the internal oscillator frequency from 24 MHz to 16 MHz, eight I^2C commands are required with a 10 µs wait time between each command.

Table 26. Manual Frequency Tuning configuration

CLK_INT_FREQ [3:0]	Oscillator Frequency [MHz]
0000 (default)	20
0001	21
0010	22
0011	23

Table 26. Manual Frequency Tuning configuration*...continued*

CLK_INT_FREQ [3:0]	Oscillator Frequency [MHz]
0100	24
1001	16
1010	17
1011	18
1100	19
Reset condition	POR

18.4 Spread spectrum

The internal oscillator can be modulated with a triangular carrier frequency of 23.15 kHz or 92.6 kHz with ±5% deviation from the oscillator frequency. The spread spectrum feature can be activated by using I^2C commands to set the MOD_EN bit (M_CLOCK1 register). The carrier frequency can be selected by I^2C with the MOD_CONF bit (M_CLOCK1 register). By default, the spread spectrum is disabled. The spread spectrum and the manual frequency tuning functions cannot be used at the same time.

The main purpose of the spread spectrum is to improve the EMC performance by spreading the energy of the internal oscillator and VPRE frequency on the VBAT frequency spectrum. For best performance, select a 23.15 kHz carrier frequency when VPRE is configured at 455 kHz and a 92.6 kHz carrier frequency when VPRE is configured at 2.22 MHz.

18.5 External clock synchronization

The PLL must be enabled with the PLL_SEL_OTP bit (CFG_CLOCK_4_OTP register) to synchronize the switching regulators with an external frequency coming from the FIN pin. To assure that the PLL output clock (CLK) remains in the digital blocks' 16 MHz to 24 MHz working range, the FIN pin accepts two frequency ranges selectable by the FIN_DIV bit (M_CLOCK1 register). When FIN_DIV is set to zero, the input frequency range must be between 333 kHz and 500 kHz. When FIN_DIV is set to one, the input frequency range must be between 2 MHz and 3 MHz. If FIN is out of range, CLK moves back to the internal oscillator and reports the error through the FIN_CLKWD_OK bit (M_FLAG3 register).

After the FIN divider has been configured by the FIN_DIV bit, the FIN clock is routed to the PLL input by the EXT_FIN_SEL bit (M_CLOCK1 register). The PLL output clock (CLK) changes from the internal oscillator to the FIN external clock depending on the EXT_FIN_SEL bit setting. The configuration procedure is FIN_DIV first, then apply FIN, and finally set EXT_FIN_SEL.

The FOUT pin can be used to synchronize an external device with the VR5510. The frequency sent to FOUT is selected by using I^2C commands to set the FOUT_MUX_SEL [3:0] bits (M_CLOCK1 register) according to Table 27.

Table 27. FOUT multiplexer selection

FOUT_MUX_SEL [3:0]	FOUT Multiplexer selection
0000 (default)	No signal, FOUT is low
0001	VPRE_clk
0010	BOOST_clk
0011	BUCK1_clk
0100	BUCK2_clk
0101	BUCK3_clk
0110	FOUT_clk
0111	CLK20M_MAIN_DIV48
1000	CLK20M_FS_DIV48
1001	CLK_FIN_DIV
Others	No signal, FOUT is low
Reset condition	POR

18.6 Low power oscillator

The low-power oscillator operates in Standby mode only. The main purpose of this block is to reduce the current consumption of the device during Standby mode. The oscillator frequency is typically 100 kHz with an option to choose either 300 kHz or 600 kHz, depending on the current load expected in Standby mode.

For DDR Self Refresh mode, use the 600 kHz setting.

The frequency setting can be changed using the LOW_POWER_CLK [1:0] bit field (M_CLOCK2 register). However, the I^2C command to change the frequency setting must be sent at least 40 µs before going into Standby mode.

Table 28. Low Power Clock Selection

LOW_POWER_CLK [1:0]	Low power oscillator frequency
00 / 01 **(default)**	100 kHz
10	300 kHz
11	600 kHz

18.7 Electrical characteristics

TA = –40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground. Typical values based on TA = 25 °C.

Table 29. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
20 MHz Internal Oscillator					
F_{20MHz}	Oscillator nominal frequency (programmable)	—	20	—	MHz
F_{20MHz_ACC}	Oscillator accuracy	-6	—	+6	%
T_{20MHz_step}	Oscillator frequency tuning step transition time	—	10	—	µs

Table 29. Electrical characteristics*...continued*

Symbol	Parameter	Min	Typ	Max	Unit
Spread spectrum					
FSS_{MOD}	Spread spectrum frequency modulation (MOD_CONF I2C configuration)	—	23.15	—	kHz
		—	92.6	—	kHz
FSS_{RANGE}	Spread spectrum Range (around the nominal frequency)	-5	—	+5	%
Clock synchronization (PLL)					
DC_{FIN_FOUT}	FIN and FOUT duty cycle	40	—	60	%
FIN_{RANGE}	FIN input frequency range (FIN_DIV I^2C configuration)	333	—	500	kHz
		2	—	3	MHz
FIN_{VIL}	FIN Low Voltage Threshold	0.3 x V_{DDIO}	—	—	V
FIN_{VIH}	FIN High Voltage Threshold	—	—	0.7 x V_{DDIO}	V
FIN_{ERR_LONG}	CLK_FIN_DIV monitoring, long deviation detection	5	—	—	µs
FIN_{ERR_SHORT}	CLK_FIN_DIV monitoring, short deviation detection	—	—	1.5	µs
FIN_{TLOST}	Time to switch to internal oscillator when FIN is lost	—	—	3	µs
FIN_{DLY}	FIN input buffer propagation delay	—	—	8	ns
$FOUT_{VOL}$	FOUT Low Voltage Threshold at 2 mA	—	—	0.5	V
$FOUT_{VOH}$	FOUT High Voltage Threshold at -2 mA	V_{DDIO} - 0.5	—	—	V
$FOUT_{TRISE}$	FOUT rise time (from 20% to 80% of VDDIO, Cout=30 pF)	—	—	20	ns
$FOUT_{TFALL}$	FOUT fall time (from 80% to 20% of VDDIO, Cout=30 pF)	—	—	20	ns
PLL_{TLOCK}	PLL lock time	—	—	90	µs
PLL_{TSET}	PLL settling time (from EXT_FIN_DIS enable to ±1% of output frequency)	—	—	125	µs
Low Power Oscillator					
F_{LPMHz}	Oscillator nominal frequency (programmable)	100	300	600	kHz
F_{LPMHz_ACC}	Oscillator accuracy	-10	—	10	%

19 Analog Multiplexer: AMUX

19.1 Functional description

The AMUX pin delivers 32 analog voltage channel outputs to the MCU ADC input. The AMUX output is buffered through the AMUX/FOUT pin. The AMUX_FOUT bit (CFG_BUCK2_2_OTP register) programs this pin to function as either an AMUX or an FOUT pin. The voltage channels delivered to the AMUX pin are selected by I^2C commands. The maximum AMUX output voltage is 1.8 V.

19.2 Block diagram

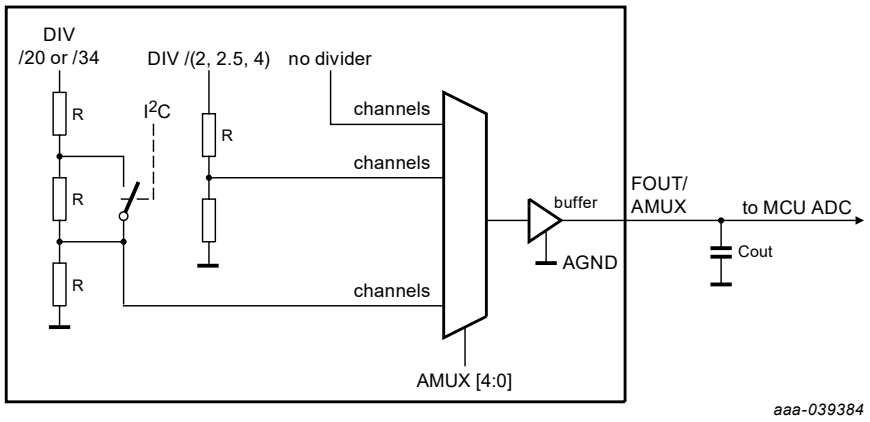


Figure 24. AMUX block diagram

19.3 AMUX channel selection

Table 30. AMUX output selection

AMUX [4:0]	Signal selection for AMUX output
00000 (default)	GND
00001	VDDIO voltage divided by 2
00010	AMUX Temperature Sensor
00011	Bandgap Main
00100	Bandgap Fail-safe
00101	BUCK1 voltage
00110	BUCK2 voltage
00111	BUCK3 voltage divided by 2.5
01000	VPRE voltage divided by 4
01001	BOOST Voltage divided by 4
01010	LDO1 voltage divided by 4
01011	LDO2 voltage divided by 4
01100	BOS voltage divided by 4
01101	Reserved
01110	VSUP1 voltage divided by 20 or 34 (I^2C configuration with bit RATIO in M_ AMUX register)
01111	PWRON1 voltage divided by 20 or 34 (I^2C configuration with bit RATIO in M_AMUX register)
10000	PWRON2 voltage divided by 4
10001	HVLDO voltage divided by 2
10010	LDO3 voltage divided by 4
Others	Same as default value (00000): GND

19.4 Electrical characteristics

TA = –40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground. Typical values based on TA = 25 °C.

Table 31. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
AMUX					
V_{AMUX_IN}	Input voltage range for VSUP, PWRON1, • Ratio 20 • Ratio 34	2.7 2.7	— —	36 60	V
I_{AMUX}	Output buffer current capability	—	—	2.0	mA
V_{AMUX_OFF}	AMUX Offset voltage (Iout = 1 mA) 0.7 V to 2.2 V	-8	—	8	mV
	AMUX Offset voltage (Iout = 1 mA) 0.1 V to 3.0 V	-10	—	10	mV
V_{AMUX_RATIO}	Ratio accuracy				
	Ratio 1	-0.75	—	0.75	%
	Ratio 2	-1.5	—	1.5	
	Ratio 2.5	-1.5	—	1.5	
	Ratio 4	-3.75	—	3.75	
	Ratio 20	-2	—	2	
	Ratio 34	-2	—	2	
V_{AMUX_BRIDGE}	VSUP1, PWRON1 resistor bridge	—	0.5	—	MΩ
V_{TEMP25}	Temperature sensor voltage at 25 °C	0.67	0.69	0.71	V
V_{TEMP_COEFF}	Temperature sensor coefficient	-2	—	-1.9	mV/°C
T_{AMUX_SET}	Settling time (from 10% to 90% of 1.8 V, Cout=1 nF)	—	—	10	µs
C_{AMUX_OUT}	Output capacitance	—	0.01	—	µF

20 I/O Interface Pins

20.1 PWRON1, PWRON2

PWRON pins are used to manage the internal biasing of the device and the Main state machine transitions.

- When PWRON1 or PWRON2 > $PWRON12_{VIH}$, the internal biasing starts and the equivalent digital state is 1
- When PWRON1 or PWRON2 < $PWRON12_{VIL}$, the equivalent digital state is 0
- When PWRON1 and PWRON2 < $PWRON12_{AVIL}$, the internal biasing is stopped

PWRON1 and PWRON2 are level-based power-up input signals with an analog measurement capability through AMUX. PWRON1 can be connected to VBAT and PWRON2 to the MCU. When the PWRON1 pin is used as a global pin, a C – R – C protection filter is required, as shown in the application schematics in Section 21 "Application Schematic".

When Deep Sleep mode is enabled via OTP, the PWRON2 pin is used to transition to Deep Sleep mode from normal operation. The PWRON2_DSM_EN bit (M_MODE register) should be enabled in that case.

TA = –40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Table 32. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
PWRON1, PWRON2					
$PWRON1_{VIN}$	PWRON1 input supply range	—	—	60	V
$PWRON2_{VIN}$	PWRON2 input supply range	—	—	5.5	V
$PWRON1_{VIL}$	Digital Low input voltage threshold	—	—	2.7	V
$PWRON2_{VIL}$	Digital Low input voltage threshold	—	—	0.7	V
$PWRON1_{VIH}$	Digital High input voltage threshold	3.5	—	—	V
$PWRON2_{VIH}$	Digital High input voltage threshold	1.15	—	—	V
$T_{PWRON12}$	Filtering time	50	70	100	µs

20.2 INTB

INTB is an open-drain output pin that generates a pulse to inform the MCU when an internal interrupt occurs. Each interrupt can be masked by setting the corresponding inhibit interrupt bit in the M_INT_MASK1 or M_INT_MASK2 register for the Main logic and FS_INTB_MASK register for the Fail Safe logic.

TA = –40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground. Typical values based on TA = 25 °C.

Table 33. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Interrupt pin					
$INTB_{PULL-up}$	External pull-up resistor to VDDIO	—	5.1	—	kΩ
$INTB_{VOL}$	Low output level threshold (I = 2.0 mA)	—	—	0.4	V
$INTB_{PULSE}$	Pulse duration	90	100	110	µs

Table 34. List of interrupts from Main logic

Interrupt Main	Description
VSUPUV7	VSUP Under Voltage 7 V
VSUPUVH	VSUP Under Voltage high
VSUPUVL	VSUP Under Voltage low
VBOSUVH	VBOS Under Voltage high
VPREOC	VPRE Over current
VPRE_FB_OV	VPRE Over Voltage protection

Table 34. List of interrupts from Main logic*...continued*

Interrupt Main	Description
VPREUVH	VPRE Under Voltage high
VPREUVL	VPRE Under Voltage low
BUCK1_TSDFLG	BUCK1 Over temperature shutdown event
BUCK1OC	BUCK1 Over current
BUCK2_TSDFLG	BUCK2 Over temperature shutdown event
BUCK2OC	BUCK2 Over current
BUCK3_TSDFLG	BUCK3 over temperature shutdown event
BUCK3_OC	BUCK3 Over current
BOOST_TSDFLG	BOOST Over temperature shutdown event
HVLDOOC	HVLDO Over current
HVLDO_TSDFLG	HVLDO Over temperature shutdown event
VBOOSTOV	BOOST Over Voltage
VBOOSTUVH	BOOST Under Voltage high
LDO1_TSDFLG	LDO1 Over temperature shutdown event
LDO1OC	LDO1 Over current
LDO2_TSDFLG	LDO2 Over temperature shutdown event
LDO2OC	LDO2 Over current
LDO3_TSDFLG	LDO3 Over temperature shutdown event
LDO3OC	LDO3 Over current
PWRON1FLG	PWRON1 transition
PWRON2FLG	PWRON2 transition
COM_ERR	I^2C communication error
DIE_CENTER_TEMPFLG	Die Center temperature
TSD_BIST_ERR_FLG	TSD check during BIST

Table 35. List of interrupts from Fail-safe logic

Interrupt Fail-safe	Description
FCCU12	FCCU12 bi-stable error detected
FCCU1	FCCU1 single error detected
FCCU2	FCCU2 single error detected
VCOREMON_OV	VCOREMON over-voltage detected
VCOREMON_UV	VCOREMON under-voltage detected
VDDIO_OV	VDDIO over-voltage detected
VDDIO_UV	VDDIO under-voltage detected
VMON1_OV	VMON1 over-voltage detected
VMON1_UV	VMON1 under-voltage detected

Table 35. List of interrupts from Fail-safe logic*...continued*

Interrupt Fail-safe	Description
VMON2_OV	VMON2 over-voltage detected
VMON2_UV	VMON2 under-voltage detected
VMON3_OV	VMON3 over-voltage detected
VMON3_UV	VMON3 under-voltage detected
VMON4_OV	VMON4 over-voltage detected
VMON4_UV	VMON4 under-voltage detected
HVLDO_OV	HVLDO VMON over-voltage detected
HVLDO_UV	HVLDO VMON under-voltage detected
WD_BAD_DATA	Wrong watchdog refresh – wrong data
WD_BAD_TIMING	Wrong watchdog refresh – CLOSED window or timeout

20.3 PSYNC

PSYNC function allows the management of complex start-up sequences with multiple power management ICs, such as two VR5510s or one VR5510 and one external device (e.g. a PF8200). This function is enabled with the PSYNC_EN_OTP bit (CFG_SM_2_OTP register). PSYNC_CFG_OTP=0 specifies two VR5510; PSYNC_CFG_OTP=1 specifies a VR5510 and an external device, such as a PF8200.

When PSYNC is used to synchronize two VR5510 devices, the PSYNC pin of each device must be connected and pulled up to the VBOS pin of the VR5510 master device as shown in Figure 25. In this configuration, the VR5510#1 state machine stops and waits for VR5510#2 in order to synchronize the two VPRE start-ups.

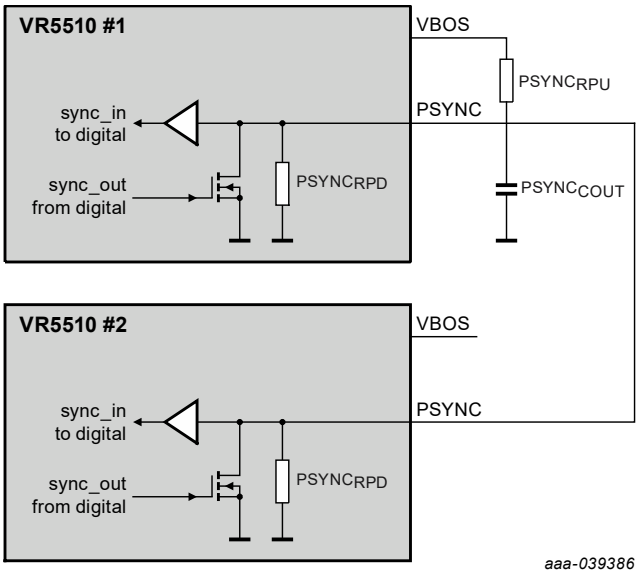


Figure 25. Synchronization of two VR5510

When PSYNC is used to synchronize one VR5510 and one PF8200 (or other PMICs), the PSYNC pin of the VR5510 must be connected to the PGOOD pin of the PF8200. PSYNC can be pulled up to the VBOS or VSNS pin. In this configuration, after VPRE

starts, the VR5510 state machine stops and waits for the PF8200 PGOOD to be released before continuing its own power-up sequence.

The VPRE_OFF_DLY_OTP bit (CFG_SM_2_OTP register) allows the VR5510 power-down sequence to delay the VPRE turn-off time (250 µs or 32 ms).

The PSYNC_PWRDWN_EN_OTP bit (CFG_BUCK2_1_OTP register) can be set to enable PSYNC to power down the VR5510 when the PSYNC level is low.

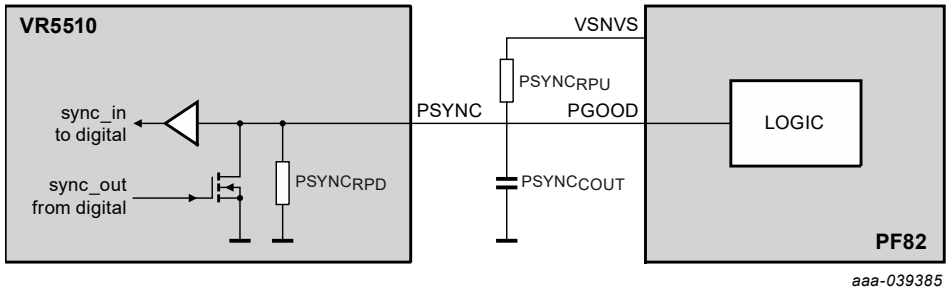


Figure 26. Synchronization of one VR5510 and one PF82

The PSYNC_PGOOD_EXT_OTP bit (CFG_SM_2_OTP register) allows the HVLDO to transition in switch mode (only from standby wake up) in the state NORMAL_M when PSYNC is going high. This function is available only if PSYNC_EN_OTP=0.

Table 36. PSYNC_PGOOD_EXT_OTP configuration

PSYNC_PGOOD_EXT_OTP	HVLDO transition in switch mode based on PSYNC pin
0	Disabled
1	Enabled

TA = –40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground. Typical values based on TA = 25 °C.

Table 37. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
PSYNC					
$PSYNC_{VIL}$	Low Level Input Threshold	0.7	—	—	V
$PSYNC_{VIH}$	High Level Input Threshold	—	—	1.4	V
$PSYNC_{VOL}$	Low Level Output Threshold (I = 2.0 mA)	—	—	0.5	V
$PSYNC_{RPU}$	External Pull Up resistor to VBOS	—	10	—	KΩ
$PSYNC_{RPD}$	Internal Pull Down resistor (weak pull-down when VR5510 is not powered)	—	400	—	KΩ
$PSYNC_{COUT}$	External decoupling capacitor	—	0.1	—	µF
$PSYNC_{TFB}$	Feedback filtering time	6	10	15	µs

20.4 STBY_PGOOD

STBY_PGOOD is an output that can be connected in the application to the MCU. The standby PGOOD feature is enabled through the STBY_PGOOD_EN_OTP bit (CFG_DEVID_OTP register). The STBY_PGOOD pin is high in Normal mode and is

asserted low in Standby mode to indicate a safe transition into Standby mode when the regulators are discharged below the STBY_DISCH_OTP (CFG_DEVID_OTP register) setting.

Table 38. STBY_DISCH_OTP configuration

STBY_DISCH_OTP	Discharge threshold selection
0	75 mV
1	150 mV

An option is available to monitor the discharge of an external regulator via the VMON1.

Table 39. EXT_STBY_DISCH_OTP configuration

EXT_STBY_DISCH_OTP	Enable the discharge monitoring of an external PMIC on VMON1
0	Disabled
1	Enabled, threshold is based on STBY_DISCH_OTP setting

The STBY_PGOOD_DLY_OTP bit (CFG_BUCK1_ 2_OTP register) selects the length of the delay before releasing the STBY_PGOOD pin in NORMAL_M state when waking up from Standby mode. The length of the delay depends on the HVLDO voltage setting configuration:

Table 40. STBY_PGOOD_DLY_OTP configuration

STBY_PGOOD_DLY_OTP	STBY_PGOOD delay in NORMAL_M state
0	400 µs for HVLDO set to 3.3 V
1	300 µs for HVLDO set to 0.8 V

The STBY_PGOOD_TEST_EN bit enables the STBY_PGOOD test function. When the test function is enabled, the output level is controlled via the STBY_PGOOD_TEST_LVL bit. This function can be used by the MCU to check that the STBY_PIN is toggling correctly. Both bits are located in the M_MODE register.

TA = –40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Table 41. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
STBY_PGOOD					
$V_{STBY\_PG\_OL}$	Low output level threshold (I = 2.0 mA)	—	—	0.4	V
$V_{STBY\_PG\_OH}$	High output level threshold (I = 2.0 mA)	0.83*VPRE	—	—	V

20.5 STBY input

The STBY pin is an input that can be connected in the application to the MCU. The standby input pin polarity can be programmed through STBY_POLARITY_OTP bit (CFG_ DEVID_ OTP) to either active high or active low in Standby mode.

The Fail-safe logic manages STBY entry.

TA = –40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Table 42. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
STANDBY					
V_{STBY_IL}	Low input level threshold	0.7	—	—	V
V_{STBY_IH}	High input level threshold	—	—	1.4	V
V_{STBY_FLT}	Standby filter time	27.3	—	44.4	µs

In Standby mode, a standby timer in the Main logic automatically turns the VR5510 off if a timeout occurs. This timer is enabled by setting both the STBY_TIMER_EN_OTP bit (CFG_ DEVID_ OTP register) and the STBY_TIMER_EN bit (M_SM_CTRL1 register) to one. The STBY_TIMER_EN_OTP bit can be set using I^2C commands. The STBY_TIMER_EN bit can only be enabled by OTP.

The timer window duration is programmable by using I^2C to set the TIMER_STBY_WINDOW[3:0] bits (M_SM_CTRL1 register) (see Table 43).

Table 43. Standby timer duration

TIMER_STBY_WINDOW[3:0]	Configure the standby timer duration
0000 (default)	**16 ms**
0001	32 ms
0010	128 ms
0011	512 ms
0100	1024 ms
0101	4096 ms
0110	8192 ms
0111	16384 ms
1000	65536 ms
1001	131072 ms
1010	262144 ms
1011	524288 ms
1100	1048576 ms
1101	2097152 ms
1110	4194304 ms
1111	8388608 ms

20.6 PWRON2 for Deep Sleep mode

The PWRON2 pin manages the transition to Deep Sleep mode if both the DSM_EN_OTP bit (CFG_CLOCK_3_OTP) and the PWRON2_DSM_EN bit (M_MODE register) are set to 1.

Deep Sleep mode shuts down all VR5510 regulators except the HVLDO. When the device is in Deep Sleep mode, the HVLDO regulator can only operate as an LDO at 3.3 V.

Only the PWRON2 input detector is active in Deep Sleep mode, so only that pin can be used to exit the mode.

21 Application Schematic

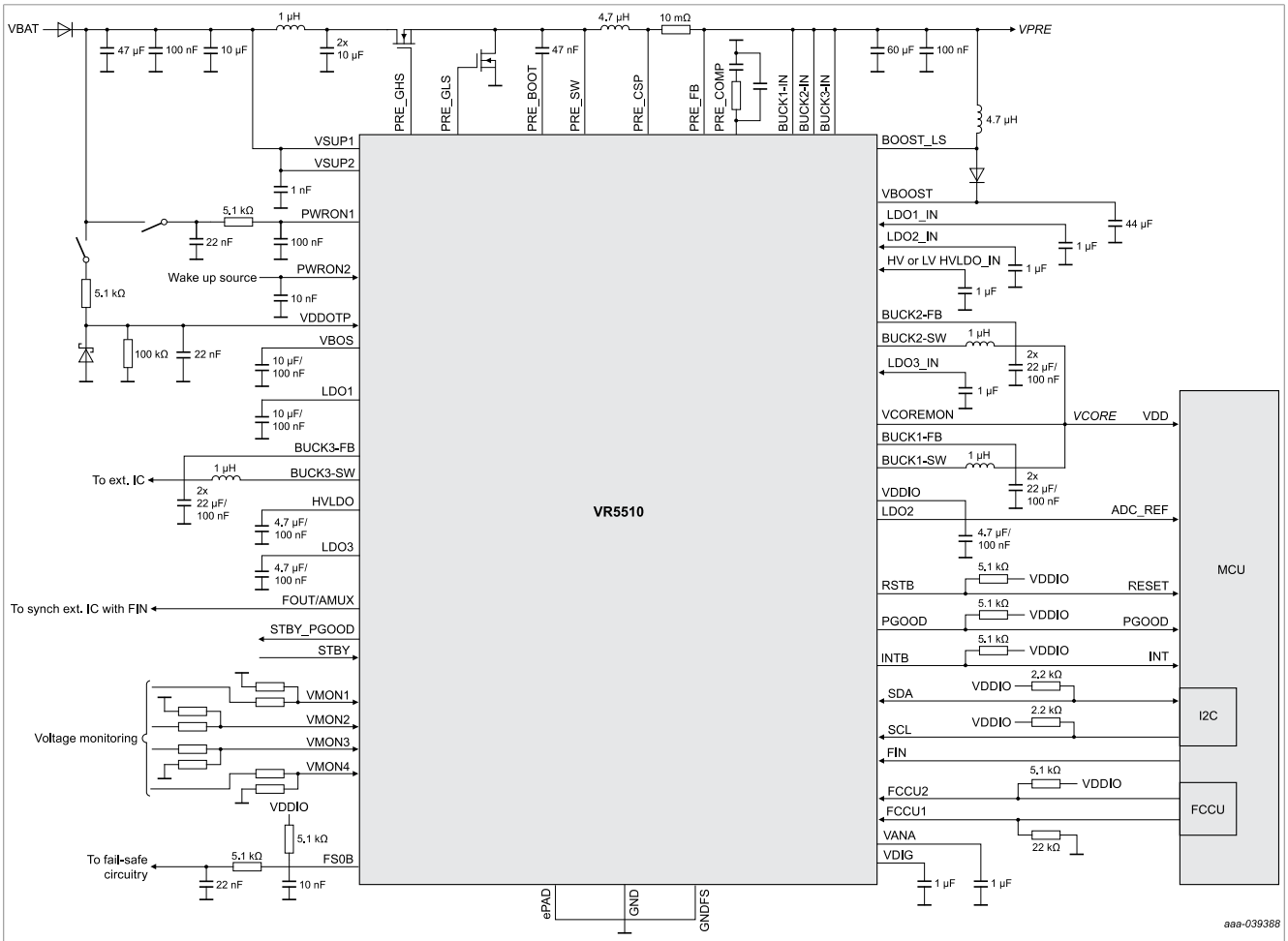


Figure 27. Application schematic

Refer to the VR5510 Device Guideline for more details on the schematic

22 Safety

22.1 Functional description

The Fail-safe domain is electrically independent and physically isolated. The Fail-safe domain is supplied by its own reference voltages and current, has its own oscillator, has a duplicate analog path to minimize common cause failures, and has LBIST/ABIST to cover latent faults. The Fail-safe domain offers QM, ASIL B or ASIL D compliancy depending on device part number. Fail-safe timings are derived from the Fail-safe oscillator with ±10% accuracy, unless otherwise specified.

The Fail-Safe domain and its dedicated pins are shown in Figure 28.

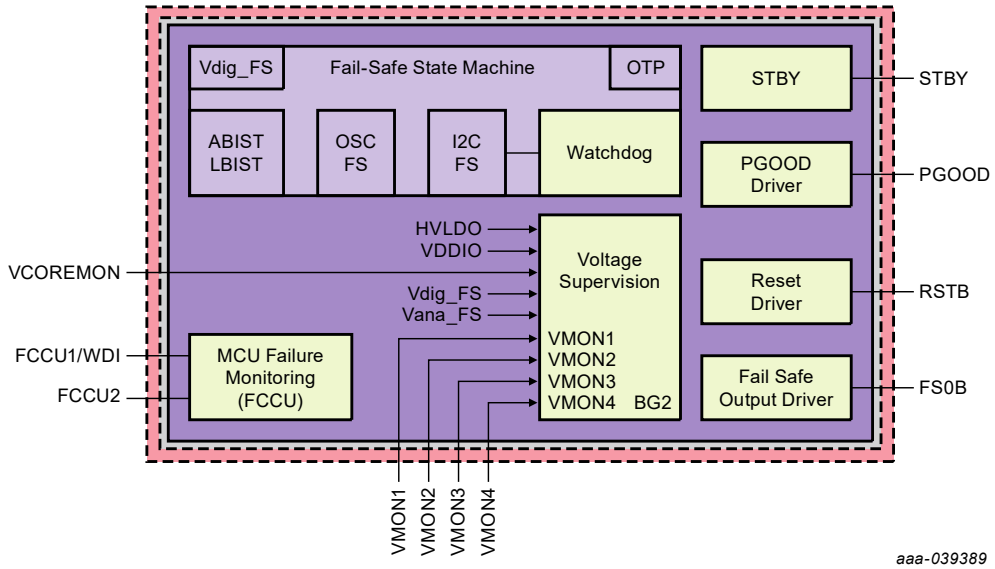


Figure 28. Fail Safe block diagram

Note: Refer to the VR5510 Device Guideline for more details on the schematic.

22.2 QM versus ASIL-B versus ASIL-D

Table 44. QM VS ASIL-B VS ASIL-D safety features

Safety Features	QM	ASIL B	ASIL D
PGOOD output pin	Yes	Yes	Yes
RSTB output pin	Yes	Yes	Yes
FS0B output pin	No	Yes	Yes
Watchdog monitoring	No	Simple WD	Challenger WD
FCCU monitoring	No	Yes	Yes
MCU Fault Recovery Strategy	No	No	Yes
Analog BIST (ABIST)	No	Yes	Yes
Logical BIST (LBIST)	No	No	Yes

22.3 Fail-safe initialization

After POR or a wake-up from Standby mode or Deep Sleep mode, when the RSTB pin is released, the Fail-Safe State Machine enters into the INIT_FS phase for initialization. To secure the writing process during INIT_FS (in addition to CRC computation during I^2C transfer), the MCU must perform the following sequence for all INIT_FS registers. The procedure is described below, where the *Register_A* suffix stands for the suffix of any INIT_FS register (e.g. FS_I_*FSSM*, FSI_I_*SVS*, etc.).

1. Write the desired data in the FS_I_*Register_A* (DATA)
2. Write the one's complement of the FS_I_*Register A* in the FS_I_NOT_*Register_A* (DATA_NOT)

For example, if FS_I_*Register_A* = 0xABCD, then 0x5432 (the one's complement of 0xABCD) must be written to FS_I_NOT_*Register_A*. Only the utility bits must be inverted

in the DATA_NOT content. The RESERVED bits are not considered and can be written to zero.

A real-time comparison process (XOR) is performed by the VR5510 to ensure DATA RS_I_Register_A=DATA_NOT FS_I_NOT_Register_A. If the comparison result is correct, then the REG_CORRUPT bit (FS_STATES register) is set to zero. If the comparison result is wrong, then the REG_CORRUPT bit is set to one. REG_CORRUPT monitoring is active as soon as the INIT_FS phase is closed by the first good watchdog refresh.

INIT_FS must be closed by the first good watchdog refresh before the window timeout. The window duration is programmable via the WD_INIT_TIMEOUT_OTP[1:0] bits (CFG_2_OTP register).

After the INIT_FS phase closes, it can be re-entered again from any other FS_state by setting the GOTO_INITFS bit (FS_SAFE_IOS register).

22.4 Watchdog

The watchdog is a windowed watchdog for the Simple and the Challenger watchdog. The first part of the window is referred to as the CLOSED window and the second part is referred to as the OPEN window. A good watchdog refresh is a good watchdog response during the OPEN window. A bad watchdog refresh is a bad watchdog response during the OPEN window, no watchdog refresh during the OPEN window or a good watchdog response during the CLOSED window. After a good or a bad watchdog refresh, a new window period starts immediately so that the MCU stays synchronized with the windowed watchdog. Figure 29 illustrates the watchdog window error possibilities:

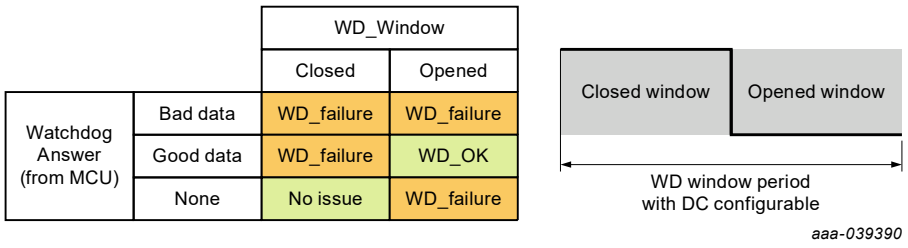


Figure 29. Watchdog window error

The first good watchdog refresh closes the INIT_FS phase. The watchdog window continues running and the MCU must refresh the watchdog in the OPEN window of the watchdog window period. The duration of the watchdog window is configurable from 1 ms to 1024 ms with the WD_WINDOW [3:0] bits (FS_WD_WINDOW register). The new watchdog window takes effect after the next watchdog refresh. The watchdog window can only be disabled during the INIT_FS phase. A watchdog disable takes effect when INIT_FS closes.

Table 45. Watchdog window period configuration

WD_WINDOW[3:0]	Watchdog Window Period
0000	DISABLE (during INIT_FS only)
0001	1.0 ms
0010	2.0 ms
0011 (default)	**3.0 ms**
0100	4.0 ms

Table 45. Watchdog window period configuration*...continued*

WD_WINDOW[3:0]	Watchdog Window Period
0101	6.0 ms
0110	8.0 ms
0111	12 ms
1000	16 ms
1001	24 ms
1010	32 ms
1011	64 ms
1100	128 ms
1101	256 ms
1110	512 ms
1111	1024 ms
Reset condition	POR

The duty cycle of the watchdog window is configurable from 31.25% to 68.75% with the WDW_DC [2:0] bits (FS_WD_WINDOW register). The new duty cycle is effective after the next watchdog refresh.

Table 46. Watchdog window duty cycle configuration

WDW_DC [2:0]	CLOSED window	OPEN window
000	31.25%	68.75%
001	37.5%	62.5%
010 (default)	**50%**	**50%**
011	62.5%	37.5%
100	68.75%	31.25%
Others	50%	50%
Reset condition	POR	

22.4.1 Simple watchdog

The Simple watchdog uses a unique seed. The MCU can send its own seed to the WD_SEED bit field (FS_WD_SEED register) or it can use the default value 0x5AB2. This seed must be written in the WD_ANSWER bit field (FS_WD_ANSWER register) during the OPEN watchdog window. When the result is correct, the watchdog window is restarted. When the result is incorrect, the WD error counter is incremented and the watchdog window is restarted. In Simple watchdog configuration, a 0xFFFF and 0x0000 value cannot be written to WD_SEED. If a 0x0000 or 0xFFFF write is attempted, a communication error is reported.

22.4.2 Challenger watchdog

The Challenger watchdog is based on a question/answer exchange between the VR5510 and the MCU. During the INIT_FS phase, the VR5510 implements a Linear Feedback Shift Register (LFSR) to generate a 16-bit pseudo-random word. The MCU can send

a different LFSR seed or use the default VR5510 LFSR value (0x5AB2) to perform a predefined calculation. The result is sent through by I^2C during the OPEN watchdog window and verified by the VR5510. When the result is correct, the watchdog window is restarted and a new LFSR is generated. When the result is wrong, the WD error counter is incremented, the watchdog window is restarted and the LFSR value is not changed.

During the initialization phase (INIT_FS), the MCU sends the seed for the LFSR, or uses the default LFSR value generated by the VR5510 (0x5AB2), available in the WD_SEED register. Using this LFSR, the MCU performs a simple calculation based on below formula and sends the results in the WD_ANSWER register.

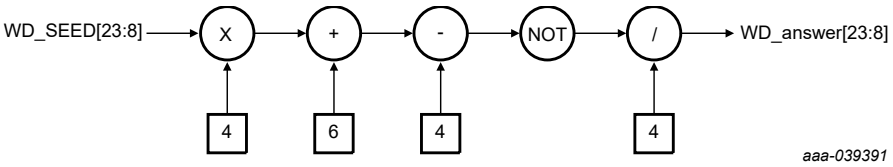


Figure 30. Challenger watchdog formula

22.4.3 Watchdog error counter

The watchdog error strategy is available for the Challenger watchdog and the Simple watchdog. The watchdog error counter is implemented in the device to filter the incorrect watchdog refresh. Each time a watchdog failure occurs, the device increments the counter by two. The watchdog error counter is decremented by one each time the watchdog is properly refreshed. This principle ensures that a cyclic 'OK/NOK' behavior converges on a failure detection.

To allow flexibility in the application, the maximum value of the watchdog error counter is configurable with the WD_ERR_LIMIT[1:0] bit field (FS_I_WD_CFG register) during the INIT_FS phase.

Table 47. Watchdog error counter

WD_ERR_LIMIT[1:0]	Watchdog Error Counter value
00	8
01 (default)	**6**
10	4
11	2
Reset condition	POR

The watchdog error counter value can be read by the MCU for diagnostic purposes from the WD_ERR_CNT[3:0] bit field (FS_I_WD_CFG register).

Figure 31. Watchdog error counter configurations

22.4.4 Watchdog refresh counter

The watchdog refresh strategy is available for the Challenger watchdog and the Simple watchdog. The watchdog refresh counter is used to decrement the fault error counter. Each time the watchdog is properly refreshed, the watchdog refresh counter is incremented by one. Each time the watchdog refresh counter reaches its maximum value (six by default), if the next WD refresh is also good, the fault error counter is decremented by one. Whatever position the watchdog refresh counter is in, each time a wrong refresh watchdog occurs, the watchdog refresh counter is reset to zero.

To allow flexibility in the application, the maximum value of the watchdog refresh counter is configurable with the WD_RFR_LIMIT[1:0] bit field (FS_I_WD_CFG register) during the INIT_FS phase.

Table 48. Watchdog refresh counter configuration

WD_RFR_LIMIT[1:0]	Watchdog Refresh Counter value
00 (default)	**6**
01	4
10	2
11	1
Reset condition	POR

The watchdog refresh counter value can be read by the MCU for diagnostic purposes with the WD_RFR_CNT[2:0] bit field (FS_I_WD_CFG register).

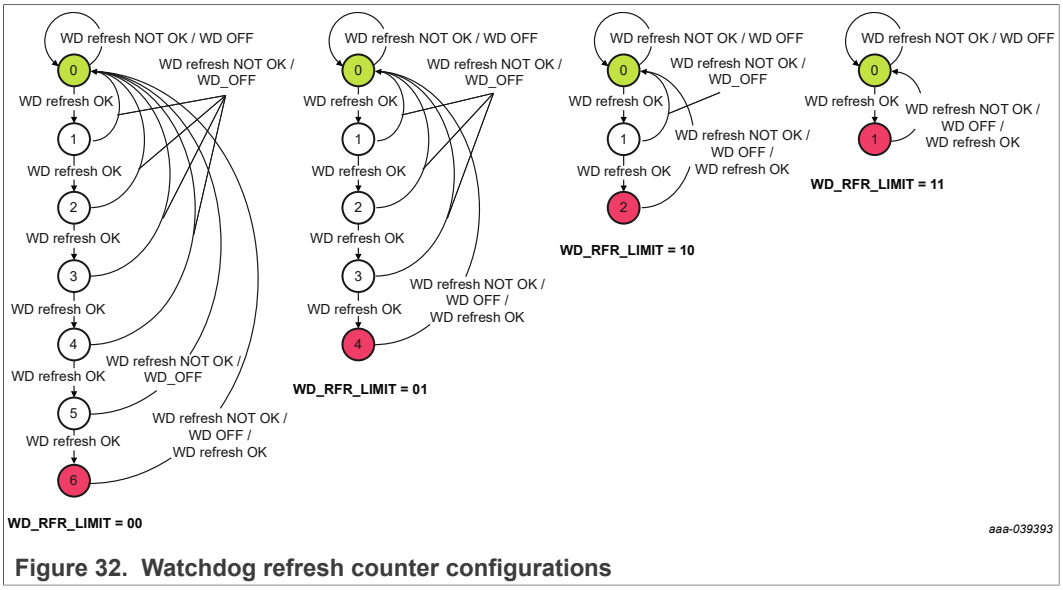


Figure 32. Watchdog refresh counter configurations

22.4.5 Watchdog error impact

When the watchdog error counter reaches its maximum value, the Fail-safe reaction on RSTB and/or FS0B is configurable with the WD_FS_IMPACT[1:0] bit field (FS_I_WD_CFG register) during the INIT_FS phase.

Table 49. Watchdog error impact configuration

WD_FS_IMPACT[1:0]	Watchdog Error Impact on RSTB/FS0B
00	No action on RSTB and FS0B
01	FS0B only is asserted if WD error counter = WD_ERR_LIMIT[1:0]
1x	**FS0B and RSTB are asserted if WD error counter = WD_ERR_LIMIT[1:0]**
Reset condition	POR

22.4.6 MCU fault recovery strategy

This functionality extends the watchdog window to allow the MCU to perform a fault recovery strategy. The goal is to prevent the MCU from being reset while it is trying to recover the application after a failure event.

When a fault is triggered by the MCU via its FCCU pins, the device asserts the FS0B pin and the watchdog window duration automatically becomes an open window (no more duty cycle). This open window duration is configurable with the WDW_RECOVERY [3:0] bit field (FS_WD_WINDOW register) during the INIT_FS phase.

Table 50. Fault recovery window configuration

WDW_RECOVERY [3:0]	Watchdog Window Duration when the device is in Fault Recovery Strategy
0000	DISABLE
0001	1.0 ms
0010	2.0 ms
0011	3.0 ms

Table 50. Fault recovery window configuration*...continued*

WDW_RECOVERY [3:0]	Watchdog Window Duration when the device is in Fault Recovery Strategy
0100	4.0 ms
0101	6.0 ms
0110	8.0 ms
0111	12 ms
1000	16 ms
1001	24 ms
1010	32 ms
1011(default)	**64 ms**
1100	128 ms
1101	256 ms
1110	512 ms
1111	1024 ms
Reset condition	POR

The transition from WD_WINDOW to WDW_RECOVERY happens when the FCCU pin indicates an error and FS0B is asserted.

If the MCU sends a good watchdog refresh before the end of the WDW_RECOVERY duration, the device switches back to the WD_WINDOW duration and the associated duty cycle if the FCCU pins no longer indicate an error. Otherwise, a new WDW_RECOVERY period is started.

If the MCU does not send a good watchdog refresh before the end of the WDW_RECOVERY duration, a reset pulse is generated and the Fail-safe state machine moves back to INIT_FS.

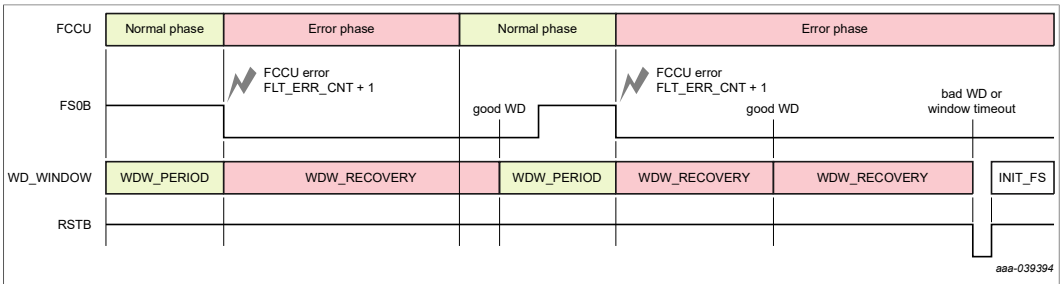


Figure 33. Fault recovery strategy

22.5 FCCU monitoring

The FCCU input pins monitor hardware failures from the MCU. The FCCU input pins can be configured by pair, or as single independent inputs. FCCU monitoring is active as soon as the INIT_FS is closed by the first good watchdog refresh. The FCCU input pins are configured by pair, or single independent inputs with the FCCU_CFG[1:0] bit field (FS_I_SAFE_INPUTS register).

Table 51. FCCU pins configuration

FCCU_CFG[1:0]	FCCU pins configuration
00	No monitoring
01 (default)	**FCCU1 and FCCU2 monitoring by pair (bi-stable protocol)**
10	FCCU1 or FCCU2 input monitoring
11	FCCU1 input monitoring only
Reset condition	POR

22.5.1 FCCU12 monitoring by pair

When FCCU12 are used by pair, the bi-stable protocol is supported as shown in Figure 34:

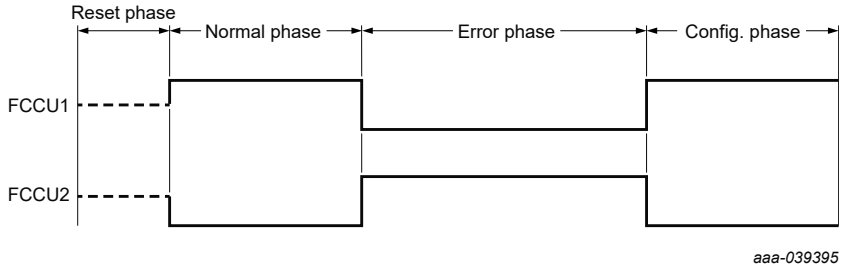


Figure 34. FCCU bi-stable protocol

The polarity of the FCCU fault signals is configurable with FCCU12_FLT_POL bit (FS_I_SAFE_INPUTS register) during the INIT_FS phase.

Table 52. FCCU12 polarity configuration

FCCU12_FLT_POL	FCCU12 polarity
0 (default)	**FCCU1=0 or FCCU2=1 level is a fault**
1	FCCU1=1 or FCCU2=0 level is a fault
Reset condition	POR

When an FCCU fault is detected, the Fail-safe reaction on RSTB and/or FS0B is configurable with the FCCU12_FS_IMPACT bit (FS_I_SAFE_INPUTS register) during the INIT_FS phase.

Table 53. FCCU12 FS impact configuration

FCCU12_FS_IMPACT	FCCU12 impact on RSTB/FS0B
0	FS0B only is asserted
1 (default)	**FS0B and RSTB are asserted**
Reset condition	POR

External pull-up/down resistors are required to provide a passive error state if the MCU does not drive its FCCU output pins.

Regardless of the VDDIO voltage (1.8 V or 3.3 V), the pull-down resistor value must be at least four times greater than the value of the pull-up resistor in order to detect an FCCU1 short to FCCU2 failure mode.

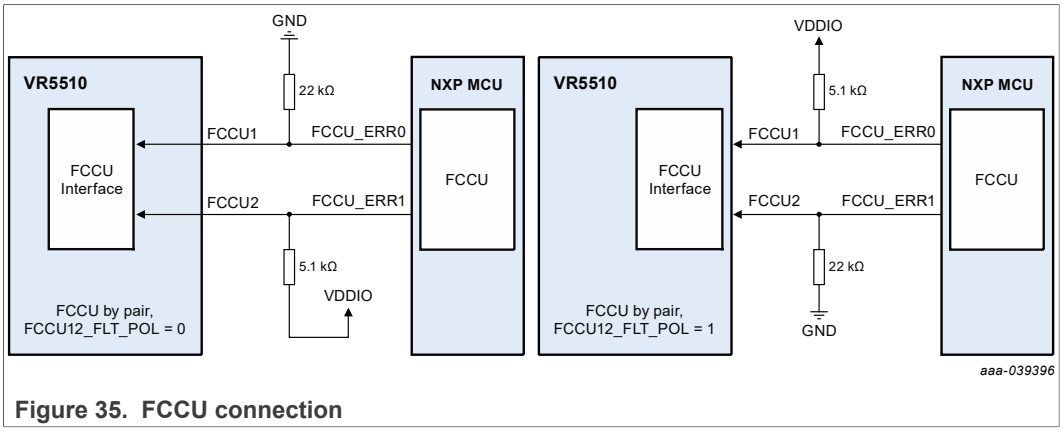


Figure 35. FCCU connection

22.5.2 FCCU12 independent monitoring

When FCCU1 and/or FCCU2 are used independently, the FCCU inputs can monitor two different and independent error signals. For each input, the polarity of the FCCU fault signal is configurable with the FCCU1_FLT_POL and FCCU2_FLT_POL bits (FS_I_SAFE_INPUTS register) during the INIT_FS phase.

Table 54. FCCU12 polarity configuration

FCCU1_FLT_POL	FCCU1 polarity configuration
0 (default)	**FCCU1 low level is a fault**
1	FCCU1 high level is a fault
Reset condition	POR
FCCU2_FLT_POL	**FCCU2_FLT_POL**
0 (default)	**FCCU2 low level is a fault**
1	FCCU2 high level is a fault
Reset condition	POR

When an FCCU fault is detected, the Fail-safe reaction on RSTB and/or FS0B is configurable with the FCCU1_FS_IMPACT and FCCU2_FS_IMPACT bits (FS_I_SAFE_INPUTS register) during the INIT_FS phase.

Table 55. FCCU12 impact configuration

FCCU1_FS_IMPACT	FCCU1 impact on RSTB/FS0B
0	FS0B only is asserted
1 (default)	**FS0B and RSTB are asserted**
Reset condition	POR
FCCU2_FS_IMPACT	**FCCU2 impact on RSTB/FS0B**
0	FS0B only is asserted
1 (default)	**FS0B and RSTB are asserted**
Reset condition	POR

22.5.3 FCCU1 WDI function for i.MX processor

FCCU1 can be configured by OTP to work as the WDI pin in order to be compatible with an i.MX processor applications.

To configure FCCU1 as the WDI pin, set the FCCU_OR_WDI_OTP bit (CFG_1_OTP register) to one. The polarity is configured through the WDI_POL_OTP bit (CFG_I2C_OTP register).

When the WDI pin is asserted by the MCU, the system transitions to Deep Fail-safe and then restarts the application.

22.5.4 FCCU12 electrical characteristics

TA = –40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground. Typical values based on TA = 25 °C.

Table 56. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
FCCU1,2					
$FCCU12_{TERR}$	FCCU1,2 filtering time	4.0	—	8.0	µs
$FCCU12_{VIH}$	FCCU1,2 High level input voltage	—	—	0.7 x V_{DDIO}	V
$FCCU12_{VIL}$	FCCU1,2 Low level input voltage	0.3 x V_{DDIO}	—	—	V
$FCCU12_{HYST}$	FCCU1,2 input voltage hysteresis	0.1	—	—	V
$FCCU1_{WDI\_FILT}$	Debounce filter when FCCU1 is used in WDI Mode	—	10	—	µs

22.6 Voltage supervisor

The voltage supervisor monitors overvoltage and undervoltage occurrences on the VCOREMON, HVLDO, VDDIO and VMON1/2/3/4 input pins. When an overvoltage occurs on a VR5510 regulator monitored by one of these pins, the associated VR5510 regulator is switched off until the fault is removed. Voltage monitoring is active as soon as FS_ENABLE=1. UV/OV flags are reported accordingly.

22.6.1 VCOREMON voltage monitoring

The VCOREMON input pin is dedicated to BUCK1 or BUCK1 & BUCK2 in dual phase operation. When an overvoltage or undervoltage fault is detected, the Fail-safe reaction on RSTB and/or FS0B is configurable with the VCOREMON_OV_FS_IMPACT[1:0] and VCOREMON_UV_FS_IMPACT[1:0] bitfields (FS_I_OVUV_SAFE_REACTION1 register) during the INIT_FS phase.

Table 57. VCOREMON impact configuration

VCOREMON_OV_FS_IMPACT[1:0]	VCOREMON OV impact on RSTB/FS0B
00	No effect on RSTB and FS0B
01	FS0B only is asserted
10 & 11 (default)	**FS0B and RSTB are asserted**
Reset condition	POR

Table 57. VCOREMON impact configuration*...continued*

VCOREMON_UV_FS_IMPACT[1:0]	VCOREMON UV impact on RSTB/FS0B
00	No effect on RSTB and FS0B
01 (default)	**FS0B only is asserted**
10 & 11	FS0B and RSTB are asserted
Reset condition	POR

VCOREMON OV threshold is configurable via the OTP VCOREOVTH_OTP[3:0] bit field (CFG_ UVOV_ 2_OTP register).

VCOREMON UV threshold is configurable via the OTP VCOREUVTH_OTP[3:0] bit field (CFG_ UVOV_ 6_OTP register).

VCOREMON OV filtering is configurable via the OTP OV_MCU_OTP bit field and the UV via UV_MCU_OTP[1:0] bit field. Both bitfields are in register CFG_ DEGLITCH1_ OTP.

TA = –40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Table 58. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
VCOREMON					
VCOREMON_OV_min	Overvoltage threshold minimum	—	+2.5	—	%
VCOREMON_OV_max	Overvoltage threshold maximum	—	+10	—	%
VCOREMON_OV_step	Overvoltage threshold step (VCOREOVTH[3:0])	—	+0.5	—	%
VCOREMON_OV_acc	Overvoltage threshold accuracy	-2	—	1.5	%
TCOREMON_OV	Overvoltage filtering time (OV_MCU_OTP)	20	25	30	µs
		40	45	50	µs
VCOREMON_UV_min	Undervoltage threshold minimum	—	-2.5	—	%
VCOREMON_UV_max	Undervoltage threshold maximum	—	-10	—	%
VCOREMON_UV_step	Undervoltage threshold step (VCOREUVTH_OTP[3:0])	—	-0.5	—	%
VCOREMON_UV_acc	Undervoltage threshold accuracy	-1.5	—	1.5	%
TCOREMON_UV	Undervoltage filtering time (UV_MCU_OTP[1:0])	2.5	5	7.5	µs
		10	15	20	µs
		20	25	30	µs
		35	40	45	µs

22.6.2 Static Voltage Scaling (SVS)

The Static Voltage Scaling function allows the MCU to reduce or increase the output voltage initially configured at the start-up of BUCK1 (and BUCK2 if used in multiphase). The SVS configuration must be done in the INIT_FS phase.

The offset value is configurable by I^2C with the SVS_OFFSET[5:0] bit field (FS_I_SVS register) and the exact complemented value must be written in the NOT_SVS_OFFSET[5:0] bits.

Table 59. SVS offset configuration

SVS_OFFSET[5:0]	NOT_SVS_OFFSET[5:0]	Offset applied to BUCK1 (and BUCK2 if used in multiphase).
000000 (default)	**111111**	**0 mV**
000001	111110	6.25 mV
- - - - -	- - - - -	6.25 mV step per bit
111111	000000	393.75 mV
Reset condition	POR	

The VCORE_SVS_CLAMP_OTP[5:0] bit field (CFG_ UVOV_ 3_OTP register) sets the maximum value of steps available for the application.

Table 60. SVS clamp configuration

VCORE_SVS_CLAMP_OTP[5:0]	SVS Max steps
000000	**No SVS**
000001	2 steps available
000011	4 steps available
000111	8 steps available
001111	16 steps available
011111	32 steps available
111111	64 steps available

A VCORE_SVS_FULL_OFFSET_OTP bit field (CFG_ UVOV_ 3_OTP register) sets the full offset range to be either negative offset only or both negative and positive offset.

If the full offset range is set, the SVS_OFFSET_SIGN bit (FS_I_SVS register) selects the sign of the offset.

The BUCK1/2 output voltage transition starts when the NOT_SVS_OFFSET[5:0] I^2C command is received and confirmed good. If the NOT_SVS_OFFSET[5:0] value sent by I^2C command is not the one's compliment of the SVS_OFFSET[5:0] value sent by I^2C command, the SVS procedure is not executed and the BUCK1 output voltage remains at its original value.

The OV/UV threshold changes immediately when the NOT_SVS_OFFSET[5:0] I^2C command is received and confirmed good. Therefore, the BUCK1 output voltage transition is done within the OV/UV filtering time. Depending on the required offset, the voltages may need to be changed in multiple steps to avoid triggering an OV/UV event.

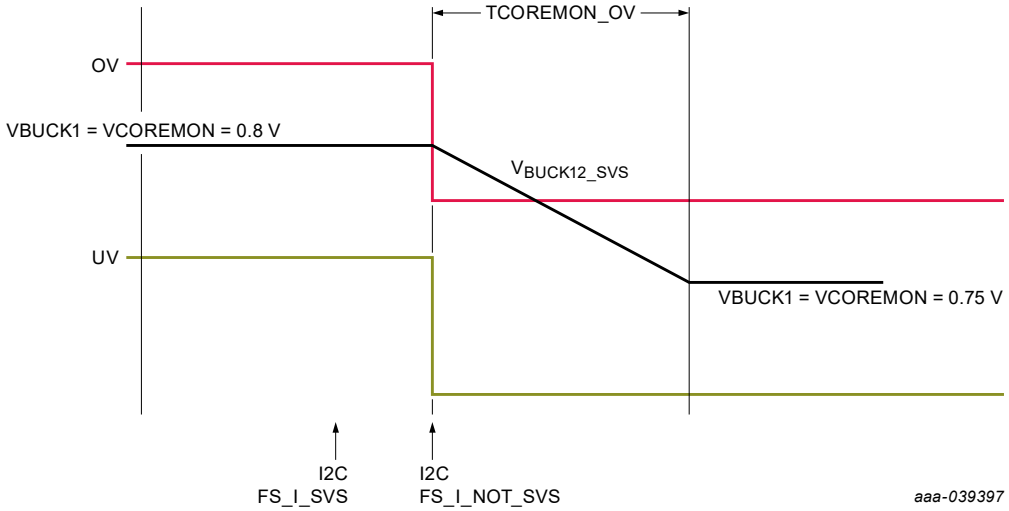


Figure 36. SVS principle

22.6.3 VDDIO monitoring

The VDDIO input pin can be connected to VPRE, LDO1, LDO2, LDO3, BUCK2, BUCK3, or an external regulator. The regulator connected to VDDIO must be at 1.8 V or 3.3 V to be compatible with overvoltage and undervoltage monitoring thresholds. Specifying which regulator is connected to VDDIO (and hence, which regulator is turned off when an overvoltage detection occurs) is done by configuration settings in the VDDIO_REG_ASSIGN_OTP[2:0] bit field (CFG_I2C_OTP register).

If an external regulator is connected to VDDIO, this regulator cannot be turned off, but the overvoltage flag is reported to the MCU which can take appropriate action.

In all cases, the Fail-safe reaction on RSTB and/or FS0B is configured with the VDDIO_OV_FS_IMPACT[1:0] and VDDIO_UV_FS_IMPACT[1:0] bitfields in the FS_I_OVUV_SAFE_REACTION1 register.

The Fail-safe VDDIO voltage (1.8 V or 3.3 V) can be set via the VDDIO_V_OTP bit (CFG_ 1_OTP register).

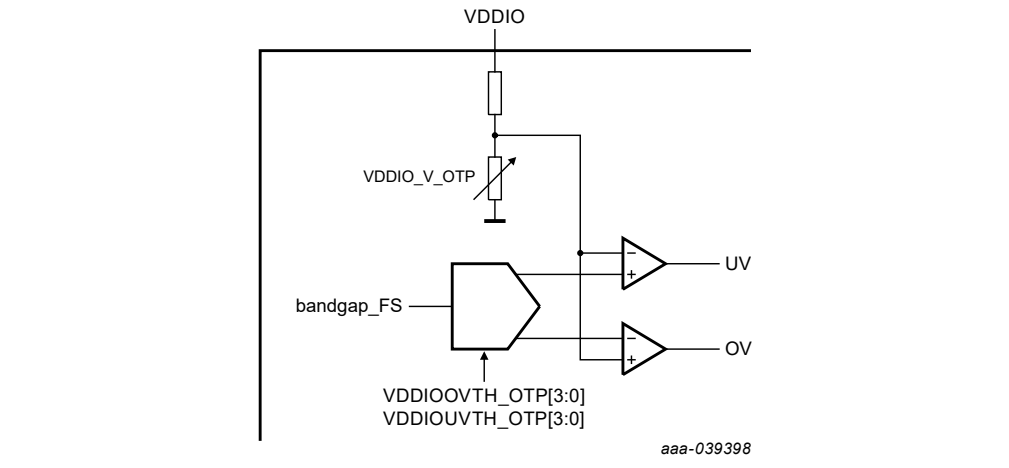


Figure 37. VDDIO monitor principle

Table 61. VDDIO FS impact configuration

VDDIO_OV_FS_IMPACT[1:0]	VDDIO OV impact on RSTB/FS0B
00	No effect on RSTB and FS0B
01	FS0B only is asserted
10 & 11 (default)	**FS0B and RSTB are asserted**
Reset condition	POR
VDDIO_UV_FS_IMPACT[1:0]	**VDDIO UV impact on RSTB/FS0B**
00	No effect on RSTB and FS0B
01 (default)	**FS0B only is asserted**
10 & 11	FS0B and RSTB are asserted
Reset condition	POR

VDDIO OV threshold is configurable via the OTP VDDIOOVTH_OTP[3:0] bit field (CFG_UVOV_2_OTP register).

VDDIO UV threshold is configurable via the OTP VDDIOUVTH_OTP[3:0] bit field (CFG_UVOV_6_OTP register).

VDDIO OV filtering is configurable via the OTP register OV_VDDIO_OTP bit (CFG_DEGLITCH1_OTP register) and the UV via UV_VDDIO_OTP[1:0] bit field (CFG_DEGLITCH1_OTP register).

TA = –40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Table 62. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
VDDIO					
VDDIO_OV_min	Over-voltage threshold minimum	—	+2.5	—	%
VDDIO_OV_max	Over-voltage threshold maximum	—	+10	—	%
VDDIO_OV_step	Over-voltage threshold step (VDDIOOVTH_OTP[3:0])	—	+0.5	—	%
VDDIO_OV_acc	Over-voltage threshold accuracy	-2	—	1.5	%
TVDDIO_OV	Over-voltage filtering time (OV_VDDIO_OTP)	20	25	30	µs
		40	45	50	µs
VDDIO_UV_min	Under-voltage threshold minimum	—	-2.5	—	%
VDDIO_UV_max	Under -voltage threshold maximum	—	-10	—	%
VDDIO_UV_step	Under -voltage threshold step (VDDIOUVTH_OTP[3:0] bits)	—	-0.5	—	%
VDDIO_UV_acc	Under -voltage threshold accuracy	-1.5	—	1.5	%
TVDDIO_UV	Under-voltage filtering time (UV_VDDIO_OTP[1:0])	2.5	5	7.5	µs
		10	15	20	µs
		20	25	30	µs
		35	40	45	µs

22.6.4 HVLDO monitoring

The HVLDO voltage monitor is internally connected to the HVLDO output.

HVLDO VMON can be configured in two modes—Switch mode and LDO mode— via the HVLDO_MODE_OTP bit (CFG_1_OTP register). In Switch mode, the reference internally tracks the Buck1 DVS DAC.

Switch mode can only be used at 0.8 V. In LDO mode, the voltage can be set either to 0.8 V or 3.3 V via the HVLDO_V_OTP bit (CFG_1_OTP register).

In all cases, the Fail-safe reaction on RSTB and/or FS0B is configured by the HVLDO_VMON_OV_FS_IMPACT[1:0] and HVLDO_VMON_UV_FS_IMPACT[1:0] bitfields. Both bit fields are in the FS_I_OVUV_SAFE_REACTION1 register.

Table 63. HVLDO monitor FS impact configuration

HVLDO_VMON_OV_FS_IMPACT[1:0]	HVLDO VMON OV impact on RSTB/FS0B
00	No effect on RSTB and FS0B
01	FS0B only is asserted
10 & 11 (default)	**FS0B and RSTB are asserted**
Reset condition	POR
HVLDO_VMON_UV_FS_IMPACT[1:0]	**HVLDO VMON UV impact on RSTB/FS0B**
00	No effect on RSTB and FS0B
01 (default)	**FS0B only is asserted**
10 & 11	FS0B and RSTB are asserted
Reset condition	POR

HVLDO VMON OV threshold is configurable via the OTP HVLDO_VMON_OVTH_OTP[3:0] bit field (CFG_ UVOV_ 9_OTP register).

HVLDO VMON UV threshold is configurable via the OTP HVLDO_VMON_UVTH_OTP[3:0] (CFG_ UVOV_ 9_OTP register).

HVLDO VMON OV filtering is configurable via the OTP OV_HVLDO_OTP bit and the UV via UV_HVLDO_OTP[1:0] bit field. Both are in the CFG_ DEGLITCH1_ OTP register.

TA = –40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Table 64. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
HVLDO					
HVLDO_OV_min	Overvoltage threshold minimum	—	+2.5	—	%
HVLDO_OV_max	Overvoltage threshold maximum	—	+10	—	%
HVLDO_OV_step	Overvoltage threshold step (HVLDO_VMON_OVTH_OTP[3:0])	—	+0.5	—	%
VHLDO_OV_acc	Overvoltage threshold accuracy	-2	—	1.5	%
HVLDO_OV	Overvoltage filtering time (OV_HVLDO_OTP)	20	25	30	µs
		40	45	50	µs

Table 64. Electrical characteristics*...continued*

Symbol	Parameter	Min	Typ	Max	Unit
HVLDO_UV_min	Undervoltage threshold minimum	—	-2.5	—	%
HVLDO_UV_max	Undervoltage threshold maximum	—	-10	—	%
HVLDO_UV_step	Undervoltage threshold step (HVLDO_VMON_UVTH_OTP[3:0] bits)	—	-0.5	—	%
HVLDO_UV_acc	VHVLDO=0.8 V accuracy	-1.5	—	1.5	%
	VHVLDO=3.3 V accuracy	-2	—	1.5	%
HVLDO_UV	Undervoltage filtering time (UV_HVLDO_OTP[1:0])	2.5	5	7.5	µs
		10	15	20	µs
		20	25	30	µs
		35	40	45	µs

22.6.5 VMONx monitoring

The VMONx input pins can be connected to VPRE, LDO1, LDO2, LDO3, BUCK1, BUCK2, BUCK3, BOOST, or to an external regulator.

Specifying which regulator is connected to a VMONx pin (and hence, which regulator is turned off when an overvoltage detection occurs) is done by I^2C in the M_VMON_REGx register.

If an external regulator is connected to a VMONx pin, this regulator cannot be turned off, but the overvoltage flag is reported to the MCU which can take appropriate action.

In all cases, the Fail-safe reaction on RSTB and/or FS0B is configured with the VMONx_OV_FS_IMPACT[1:0] and VMONx_UV_FS_IMPACT[1:0] bitfields in the FS_I_OVUV_SAFE_REACTION2 register.

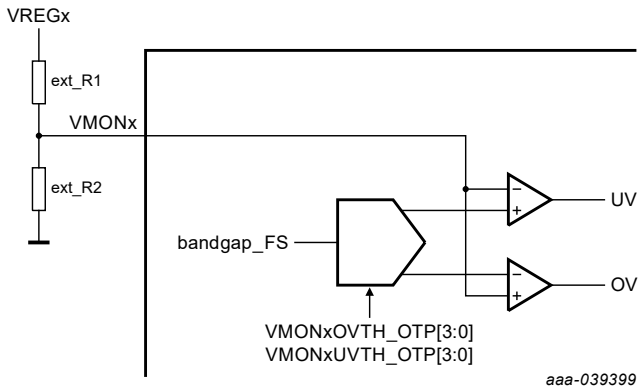


Figure 38. VMONx monitor principle

The external resistor bridge connected to VMONx must be calculated to deliver a midpoint of 0.8 V. Use ±0.1% or less resistor accuracy.

Table 65. VMONx FS impact configuration

VMONx_OV_FS_IMPACT[1:0]	VMONx OV impact on RSTB/FS0B
00	No effect on RSTB and FS0B
01	FS0B only is asserted
10 & 11 (default)	**FS0B and RSTB are asserted**
Reset condition	POR
VMONx_UV_FS_IMPACT[1:0]	**VMONx UV impact on RSTB/FS0B**
00	No effect on RSTB and FS0B
01 (default)	**FS0B only is asserted**
10 & 11	FS0B and RSTB are asserted
Reset condition	POR

VMONx OV threshold is configurable via the OTP VMONxOVTH_OTP[3:0] bit field (CFG_ UVOV_ 4_OTP and CFG_ UVOV_ 5_OTP registers).

VMONx UV threshold is configurable via the OTP VMONxUVTH_OTP[3:0] bit field (CFG_ UVOV_ 7_OTP and CFG_ UVOV_ 8_OTP registers).

VMONx OV filtering is configurable via the OTP OV_VMONx_OTP bit and the UV via UV_VMONx_OTP[1:0] bit field (CFG_ DEGLITCHx_OTP registers).

TA = –40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Table 66. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
VMONx *(without ext resistor accuracy)*					
VMONx_OV_min	Overvoltage threshold minimum	—	+2.5	—	%
VMONx_OV_max	Overvoltage threshold maximum	—	+10	—	%
VMONx_OV_step	Overvoltage threshold step (VMONxOVTH_OTP[3:0])	—	+0.5	—	%
VMONx_OV_acc	Overvoltage threshold accuracy	-2	—	1.5	%
TMONx_OV	Overvoltage filtering time (OV_VMONx_OTP)	20	25	30	µs
		40	45	50	µs
VMONx_UV_min	Undervoltage threshold minimum	—	-2.5	—	%
VMONx_UV_max	Undervoltage threshold maximum	—	-10	—	%
VMONx_UV_step	Undervoltage threshold step (VMONxUVTH_OTP[3:0] bits)	—	-0.5	—	%
VMON1_UV_acc	Undervoltage threshold accuracy	-1.4	—	1	%
VMON2_UV_acc	Undervoltage threshold accuracy	-1.3	—	1	%
VMON3_UV_acc	Undervoltage threshold accuracy	-1.5	—	1	%
VMON4_UV_acc	Undervoltage threshold accuracy	-1.4	—	1	%
TMONx_UV	Undervoltage filtering time (UV_VMONx_OTP[1:0])	2.5	5	7.5	µs
		10	15	20	µs

Table 66. Electrical characteristics*...continued*

Symbol	Parameter	Min	Typ	Max	Unit
		20	25	30	µs
		35	40	45	µs
VMONx_PD	Internal passive pull-down	1	2	4	MΩ

22.7 Fault management

22.7.1 Fault Error Counter

The VR5510 integrates a configurable fault error counter that counts the number of faults related to the device itself as well as those caused by external events.

The Fault Error Counter starts at level 1 after a POR or after resuming from Standby. The final value of the Fault Error Counter is used to transition into Deep Fail-safe mode. The maximum value of this counter is configurable with the FLT_ERR_CNT_LIMIT[1:0] bitfield (FS_I_FSSM register) during the INIT_FS phase.

Table 67. Fault Error Counter configuration

FLT_ERR_CNT_LIMIT[1:0]	Fault Error Counter max value configuration	Fault Error Counter intermediate value
00	2	1
01 (default)	**6**	**3**
10	8	4
11	12	6
Reset condition	POR	

The Fault Error Counter has two output values: Intermediate and Final. The intermediate value can be used to force FS0B activation or to generate a RSTB pulse according to the configuration in the FLT_ERR_IMPACT[1:0] bit field (FS_I_FSSM register).

Table 68. Fault Error Counter impact configuration

FLT_ERR_IMPACT[1:0]	Fault Error Counter intermediate value impact on RSTB/FS0B
00	No effect on RSTB and FS0B
01	FS0B only is asserted if FLT_ERR_CNT = intermediate value
10 & 11 (default)	**FS0B and RSTB area asserted if FLT_ERR_CNT = intermediate value**
Reset condition	POR

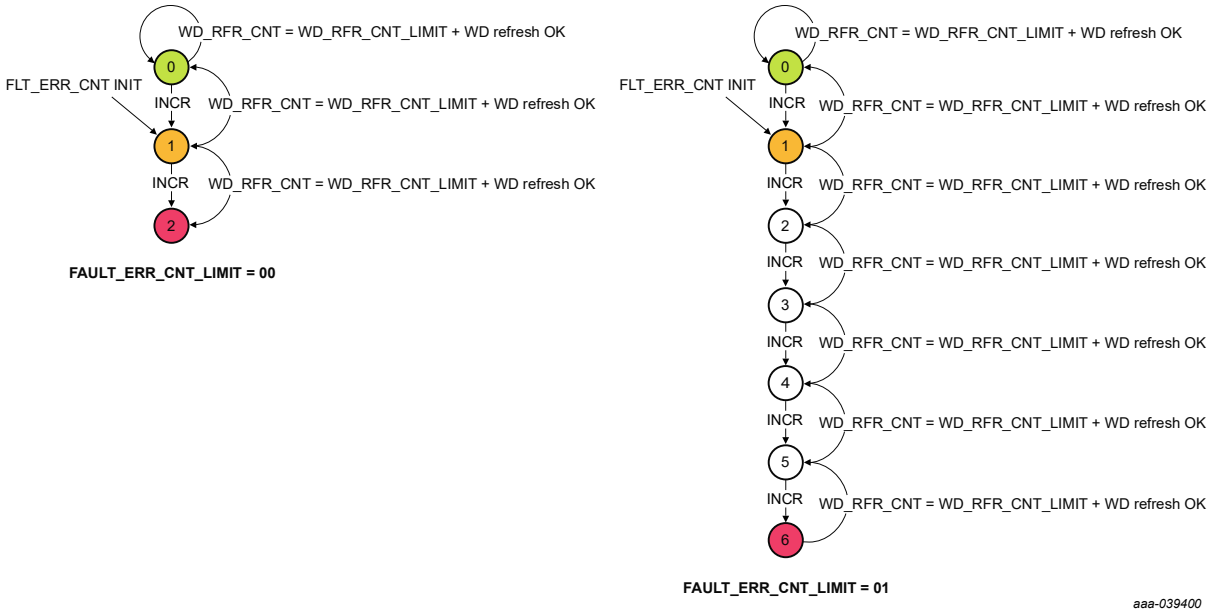


Figure 39. Fault Error Counter max value 2 or 6 example

22.7.2 Fault source and reaction

In normal operation, when FS0B and RSTB are released, the Fault Error Counter gets incremented when a fault is detected by the VR5510 Fail-safe Sate Machine. Table 69 lists all the faults and their impact on the PGOOD, RSTB and FS0B pins according to the device configuration. Faults not configured to assert RSTB and FS0B will not increment the fault error counter. In that case, only the flags are available for MCU diagnostic.

When FS0B is asserted, the Fault Error Counter continues to be incremented by +1 each time the WD Error Counter reaches its maximum value.

Table 69. Fail Safe fault list and reaction [1]

Apps related Fail-safe Faults	FLT_ ERR_CNT increment	FS0B assertion	RSTB assertion	PGOOD assertion
VCOREMON_OV	+1	VCOREMON_OV_FS_IMPACT	VCOREMON_OV_FS_ IMPACT	OTP config
VDDIO_OV	+1	VDDIO_OV_FS_IMPACT	VDDIO_OV_FS_IMPACT	OTP config
HVLDO_OV	+1	HVLDO_VMON_OV_FS_ IMPACT	HVLDO_VMON_OV_FS_ IMPACT	OTP config
VMONx_OV	+1	VMONX_OV_FS_IMPACT	VMONX_OV_FS_IMPACT	OTP config
VCOREMON_UV	+1	VCOREMON_UV_FS_IMPACT	VCOREMON_UV_FS_IMPACT	OTP config
VDDIO_UV	+1	VDDIO_UV_FS_IMPACT	VDDIO_UV_FS_IMPACT	OTP config
HVLDO_UV	+1	HVLDO_VMON_UV_FS_ IMPACT	HVLDO_VMON_UV_FS_ IMPACT	OTP config
VMONx_UV	+1	VMONX_UV_FS_IMPACT	VMONX_UV_FS_IMPACT	OTP config
FCCU12 (pair)	+1	FCCU12__FS_IMPACT	FCCU12__FS_IMPACT	No
FCCU1 (single)	+1	FCCU1_FS_IMPACT	FCCU1_FS_IMPACT	No

Table 69. Fail Safe fault list and reaction [1] *...continued*

Apps related Fail-safe Faults	FLT_ ERR_CNT increment	FS0B assertion	RSTB assertion	PGOOD assertion
FCCU2 (single)	+1	FCCU2_FS_IMPACT	FCCU2_FS_IMPACT	No
WD error counter = max value	+1	WD_FS_IMPACT	WD_FS_IMPACT	No
Fault Error Counter impact at intermediate Value	No	FLT_ERR_IMPACT	FLT_ERR_IMPACT	No
Wrong WD refresh in INIT_FS	+1	Yes	Yes	No
No WD refresh in INIT_FS	+1	Yes	Yes	No
External RESET (out of extended RSTB)	+1	No	Yes (low externally)	No
RSTB pulse request by MCU	No	No	Yes	No
RSTB Short to high	+1	Yes	No (high externally)	No
FS0B Short to high	+1	No (high externally)	BACKUP_SAFETY_PATH	No
FS0B request by the MCU	No	Yes	No	No
Standby Timer Window error	+1	No	Yes	No
REG_CORRUPT = 1	+1	Yes	No	No
OTP_CORRUPT = 1	+1	Yes	No	No
GOTO_INITFS request by MCU	No	Yes	No	No

[1] Orange cells indicate that the reaction is not configurable.
Green cells indicate that the reaction is configurable by OTP for PGOOD and by I^2C for RSTB/FS0B during INIT_FS.

If RSTB2PGOOD_OTP = 0, the RSTB and PGOOD pins work independently (see Table 49. If RSTB2PGOOD_OTP = 1 (default configuration), the RSTB and PGOOD pins work concurrently and all the faults asserting RSTB also assert PGOOD, except for external RSTB detections.

22.8 PGOOD, RSTB, FS0B, STBY

The three safety output pins (PGOOD, RSTB, FS0B) are prioritized hierarchically in order to guarantee the safe state.

- PGOOD has priority one. If PGOOD is asserted, RSTB and FS0B are asserted.
- RSTB has priority two. If RSTB is asserted, FS0B is asserted, but PGOOD may not be asserted.
- FS0B has priority three. If FS0B is asserted, RSTB and PGOOD may not be asserted.

RSTB's release is managed by the Fail-safe state machine and depends on PGOOD's release and the execution of ABIST1.

The voltage monitoring assigned to PGOOD and to ABIST1 determines when RSTB is released. This configuration is done by OTP.

The STBY input pin is used to enter or exit Standby mode. Standby entry is handled by the Fail-safe state machine. Standby exit is handled by the Main state machine.

22.8.1 PGOOD

PGOOD is an open-drain output that can be connected in the application to the MCU's PORB pin. PGOOD requires an external pull-up resistor to VDDIO or VPRE and a filtering capacitor to GND for immunity.

An internal pull-down RPD ensures that PGOOD remains at low level when the device is off or powering down.

When PGOOD is asserted low, RSTB and FS0B are also asserted low. An internal pull-up on the gate of the low side MOS ensures PGOOD remains at low level when an FS_LOGIC failure occurs.

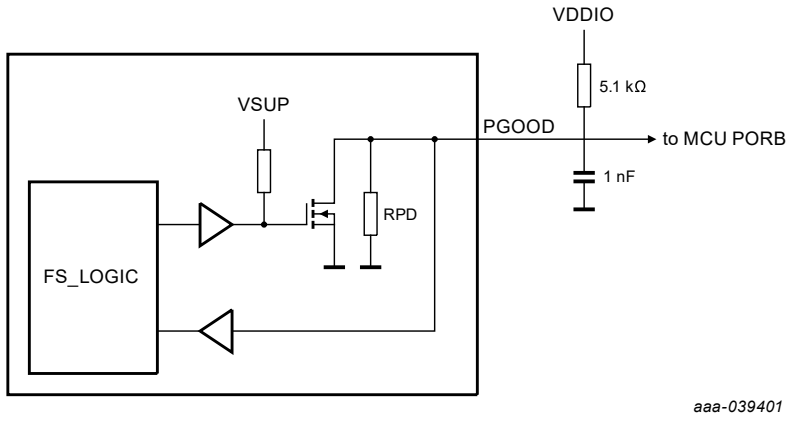


Figure 40. PGOOD pin architecture

TA = –40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Table 70. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
PGOOD					
$PGOOD_{VIL}$	Low level input voltage	0.7	—	—	V
$PGOOD_{VIH}$	High level input voltage	—	—	1.5	V
$PGOOD_{HYST}$	Input voltage Hysteresis	100	—	—	mV
$PGOOD_{VOL}$	Low level output voltage (I = 2.0 mA)	—	—	0.4	V
$PGOOD_{RPD}$	Internal pull down resistor	200	400	800	kΩ
$PGOOD_{ILIM}$	Current limitation	4.0	—	22	mA
$PGOOD_{TFB}$	Feedback filtering time	8.0	—	15	µs
$PGOOD_{FALL}$	PGOOD Falling time	—	—	4	µs

22.8.2 RSTB

RSTB is an open-drain output that can be connected in the application to the MCU's RESET pin. RSTB requires an external pull-up resistor to VDDIO or VPRE and a filtering capacitor to GND for immunity.

An internal pull-down RPD ensures that RSTB remains at low level when the device is off or powering down. RSTB assertion depends on the device configuration during INIT_FS phase.

When RSTB is asserted low, FS0B is also asserted low. An internal pull-up on the gate of the low side MOS ensures that RSTB remains at low level when an FS_LOGIC failure occurs. When RSTB is stuck low for more than $RSTB_{T8S}$, the device transitions into Deep Fail-safe mode.

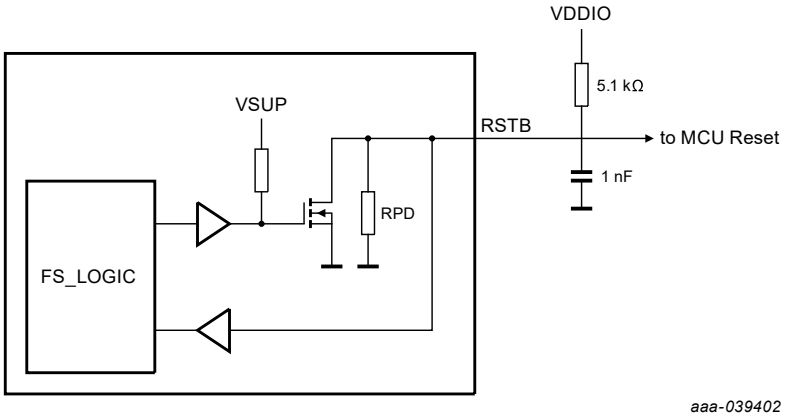


Figure 41. RSTB pin architecture

TA = –40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground. Typical values based on TA = 25 °C.

Table 71. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
RSTB					
$RSTB_{VIL}$	Low level Input voltage	0.7	—	—	V
$RSTB_{VIH}$	High level Input voltage	—	—	1.5	V
$RSTB_{HYST}$	Input voltage hysteresis	100	—	—	mV
$RSTB_{VOL}$	Low level output voltage (I = 2.0 mA)	—	—	0.4	V
$RSTB_{RPB}$	Internal pull-down resistor	200	400	800	kΩ
$RSTB_{ILIM}$	Current limitation	6.0	—	22	mA
$RSTB_{TFB}$	Feedback filtering time	8.0	—	15	µs
$RSTB_{TSC}$	Short to high filtering time	500	—	800	µs
$RSTB_{TLG}$	Long pulse (configurable with RSTB_DUR bit)	9.0	—	11	ms
$RSTB_{TST}$	Short pulse (configurable with RSTB_DUR bit)	0.9	—	1.1	ms
$RSTB_{T8S}$	8 second timer	7.0	8.0	9.0	s
$RSTB_{TRELEASE}$	Time to release RSTB from Wake Up or POR with all regulators started in Slot 0	—	5	—	ms
$RSTB_{FALL}$	RSTB Falling time	—	—	4	µs

22.8.3 FS0B

FS0B is an open-drain output that can be used to transition the system into safe state. FS0B requires an external pull-up resistor to VDDIO or VSUP, a 10 nF filtering capacitor to GND for immunity when FS0B is a local pin, and an additional RC network when FS0B is a global pin to be robust against ESD GUN and ISO 7637 transient pulses.

An internal pull-down RPD ensures that FS0B remains low level when the device is in Standby or power-down mode. FS0B assertion depends on the device configuration during INIT_FS phase. An internal pull-up on the gate of the low side MOS ensures that FS0B remains at low level when an FS_LOGIC failure occurs.

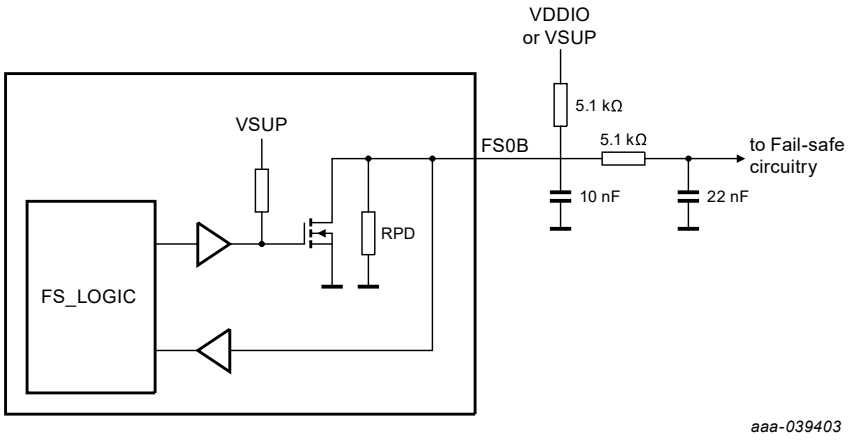


Figure 42. FS0B pin architecture

TA = –40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground. Typical values based on TA = 25 °C.

Table 72. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
FS0B					
$FS0B_{VIL}$	Low level Input voltage	0.7	—	—	V
$FS0B_{VIH}$	High level Input voltage	—	—	1.5	V
$FS0B_{HYST}$	Input voltage hysteresis	100	—	—	mV
$FS0B_{VOL}$	Low level output voltage (I = 2.0 mA)	—	—	0.4	V
$FS0B_{RPD}$	Internal pull down resistor	1	2	4	MΩ
$FS0B_{ILIM}$	Current limitation	4.0	—	22	mA
$FS0B_{TSC}$	Short to high filtering time	500	—	800	µs
$FS0B_{FALL}$	FS0B Falling time	—	—	10	µs

22.8.4 FS0B release

When the fail-safe output FS0B is asserted low by the device due to a fault, three conditions must be validated before allowing the pin to be released by the device. The conditions are:

- LBIST_OK = ABIST1_OK = ABIST2_OK = 1

- Fault Error Counter = 0
- FS_RELEASE_FS0B register filled with ongoing WD_SEED bit field (FS_WD_SEED register) reversed and complemented

Table 73. FS_RELEASE_FS0B register based on WD_SEED

WD_SEED[23:16]	B23	B22	B21	B20	B19	B18	B17	B16
FS_RELEASE_ FS0B	Not(B8)	Not(B9)	Not(B10)	Not(B11)	Not(B12)	Not(B13)	Not(B14)	Not(B15)
WD_SEED[15:8]	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
FS_RELEASE_ FS0B	Not(B16)	Not(B17)	Not(B18)	Not(B19)	Not(B20)	Not(B21)	Not(B22)	Not(B23)

22.8.5 STBY

STBY is an input that can be connected in the application to the MCU. The standby input pin polarity can be programmed through the STBY_POLARITY_OTP bit (CFG_DEVID_OTP register) to either active high in Standby mode/low in Normal mode or active low in Standby mode/high in Normal mode.

The STBY function is enabled via the STBY_EN_OTP bit (CFG_2_OTP register).

There are two possible paths to enter Standby mode, depending on the STBY_SAFE_DIS_OTP bit (CFG_2_OTP register) setting:

- The Standard path using only the STBY pin transition
- The Safety path using an I^2C request (STBY_REQ bit in the FS_SAFE_IOS register) and the STBY pin transition

If the Safety path is used, a standby timing window register, enabled by the STBY_WINDOW_EN_OTP bit (CFG_ 2_OTP register), is used to define the maximum time between the I^2C request and the STBY pin transition.

The standby timing window is configurable by I^2C during the INIT_FS phase through the TIMING_WINDOW_STBY[3:0] bit field (FS_I_SAFE_INPUTS register).

Table 74. Standby timing window

TIMING_WINDOW_STBY[3:0]	Configure the window duration
0000	Disable
0001	Reserved
0010	Reserved
0011	Reserved
0100	60 µs
0101	80 µs
0110	100 µs
0111	200 µs
1000	300 µs
1001	500 µs
1010 (default)	**1 ms**
1011	2 ms

Table 74. Standby timing window*...continued*

TIMING_WINDOW_STBY[3:0]	Configure the window duration
1100	3 ms
1101	5 ms
1110	8 ms
1111	10 ms

22.9 Built in Self-Test (BIST)

22.9.1 Logical BIST

The Fail-safe state machine includes a Logical Built in Self-Test (LBIST) to verify the correct functionality of the safety logic monitoring. The LBIST is performed after each POR, or after each wake up from Standby. If the LBIST fails, RSTB and PGOOD are released but FS0B remains stuck low and cannot be released.

The flag LBIST_PASS (FS_DIAG_SAFETY register) is available through I^2C for MCU diagnostics.

The typical LBIST duration is 3 ms and the maximum LBIST duration is 5 ms.

22.9.2 Analog BIST

The Fail-safe state machine includes two Analog Built in Self-Test (ABIST) to verify the correct functionality of the safety analog monitoring.

ABIST1 is executed automatically after each POR, or after each wake up from Standby. The assignment of which regulator is checked during ABIST1 is done by OTP.

ABIST2 is executed by I^2C with the Vxxx_ABIST2 bit (FS_I_ABIST2_CTRL register) after the INIT_FS phase. If the ABIST fails, RSTB and PGOOD are released but FS0B remains stuck low and cannot be released. The flags ABIST1_OK and ABIST2_OK (both in FS_DIAG_SAFETY register) are available through I^2C for MCU diagnostics.

Table 75. ABIST coverage

Parameter	Over voltage	Under voltage	Short to High	Low speed	High speed	ABIST1	ABIST2
VCOREMON	X	X				OTP	I^2C
VDDIO	X	X				OTP	I^2C
HVLDO_VMON	X	X				OTP	I^2C
VMONx	X	X				OTP	I^2C
OSC				X	X	X	
V1p6D_FS	X					X	
PGOOD			X			X	
RSTB			X			X	
FS0B			X			X	

Note: *When waking up from standby mode, ABIST1 checks that the RSTB and PGOOD pins are at a high state. If the pins are low, an ABIST1 error will be detected.*

Table 76. ABIST2 setting

VCORE_ABIST2	VCOREMON BIST executed during ABIST2
0 (default)	**No ABIST2**
1	VCOREMON BIST executed during ABIST2
Reset condition	POR
VDDIO_ABIST2	**VDDIO BIST executed during ABIST2**
0 (default)	**No ABIST2**
1	VDDIO BIST executed during ABIST2
Reset condition	POR
VMONx_ABIST2	**VMONx BIST executed during ABIST2**
0 (default)	**No ABIST2**
1	VMONx BIST executed during ABIST2
Reset condition	POR
HVLDO_VMON_ABIST2	**HVLDO VMON BIST executed during ABIST2**
0 (default)	**No ABIST2**
1	HVLDO VMON BIST executed during ABIST2
Reset condition	POR

An RSTB_DELAY_OTP bit is available to add a 5 ms delay between the end of the ABIST1 and RSTB/PGOOD release.

TA = –40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground

Table 77. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
ABIST					
$ABIST1_{TDUR}$	ABIST1 duration • MIN with **no** voltage monitoring assigned by OTP • MAX with **all** voltage monitoring assigned by OTP	0.2	—	1.4	ms
$ABIST2_{TDUR}$	ABIST2 duration • MIN with **no** voltage monitoring selected by I^2C • MAX with **all** voltage monitoring selected by I^2C	0.2	—	1.4	ms

23 I^2C

23.1 High level overview

The VR5510 uses an I^2C interface following the High-Speed mode definition up to 3.4 Mbit/s. I^2C interface protocol requires a device address for addressing the target IC on a multi-device bus. The VR5510 has two device addresses: one to access the Main logic and one to access the Fail-safe logic. These two I^2C addresses are set by OTP.

The I^2C interface uses VDDIO as the main supply and is compatible with 1.8 V / 3.3 V input supply. The SCL and SDA pins can be pulled up to VDDIO by a 2.2 kΩ resistors.

Timing, diagrams, and further details can be found in the NXP I²C specification UM10204 rev6.

I^2C message arrangement:

B39	B38	B37	B36	B35	B34	B33	B32	B31	B30	B29	B28	B27	B26	B25	B24
ID_6-0							R/W	0	0	Adr_5-0					
Device Address							Read/Write			Register Address					
B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8
Data_15	Data_14	Data_13	Data_12	Data_11	Data_10	Data_9	Data_8	Data_7	Data_6	Data_5	Data_4	Data_3	Data_2	Data_1	Data_0
Data MSB								Data LSB							
								B7	B6	B5	B4	B3	B2	B1	B0
								CRC_7	CRC_6	CRC_5	CRC_4	CRC_3	CRC_2	CRC_1	CRC_0
								CRC_7	CRC_6	CRC_5	CRC_4	CRC_3	CRC_2	CRC_1	CRC_0

23.2 Device address

The VR5510 has two device addresses: one to access the Main logic and one to access the Fail-safe logic. The device address is a 7-bit register that can be set using the I2CDEVADDR_OTP bitfield (CFG_ I2C_OTP register).

The I^2C addresses have the following arrangement:

Table 78. I^2C address arrangement

B39	B38	B37	B36	B35	B34	B33
0	1	OTP	0TP	OTP	OTP	0/1

- Bit 39: 0
- Bit 38: 1
- Bits 37 to 34: OTP value
- Bit 33: 0 to access the Main logic, 1 to access the Fail-safe logic

23.3 Cyclic Redundant Check

An 8-bit CRC is required for each Write and Read I^2C command. Computation of a cyclic redundancy check is derived from the mathematics of polynomial division, modulo two. The CRC polynomial used is x^8+x^4+x^3+x^2+1 (or 0x1D), and the SEED value is 0xFF.

CRC_7 = XOR (B38, B35, B32, B31, B24, B23, B22, B20, B17, B13, B12, B11, 1, 1, 1)

CRC_6 = XOR (B37, B34, B23, B22, B21, B19, B16, B12, B11, B10, 1, 1)

CRC_5 = XOR (B39, B36, B33, B30, B29, B22, B21, B20, B18, B15, B11, B10, B9, 1, 1, 1)

CRC_4 = XOR (B39, B38, B35, B32, B29, B28, B21, B20, B19, B17, B14, B10, B9, B8, 1, 1, 1, 1)

CRC_3 = XOR (B37, B35, B34, B32, B28, B27, B24, B23, B22, B19, B18, B17, B16, B12, B11, B9, B8, 1, 1, 1, 1)

CRC_2 = XOR (B39, B38, B36, B35, B34, B33, B32, B27, B26, B24, B21, B20, B18, B16, B15, B13, B12 B10, B8, 1,1,1,1,1,1,1,1)

CRC_1 = XOR (B37, B34, B33, B26, B25, B24, B22, B19, B15, B14, B13, B9, 1, 1, 1)

CRC_0 = XOR (B39, B36, B33, B32, B25, B24, B23, B21, B18, B14, B13, B12, B8, 1, 1, 1, 1)

Hint to calculate CRC with I^2C communication:

I^2C write command: DEVADDR-W + REG_ADDR + MASTER_DATA_MSB + MASTER_DATA_LSB + CRC

➔ CRC is calculated with bits from B39 to B8

I^2C read sequence: DEVADDR-W + REG_ADDR + I2C_REPEAT_START + DEVADDR-R + SLAVE_DATA_MSB + SLAVE_DATA_LSB + CRC

➔ CRC is calculated with bits from DEVADDR-R + REG_ADDR + SLAVE_DATA_MSB + SLAVE_DATA_LSB

23.4 Electrical characteristics

TA = –40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Table 79. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
I^2C					
VDDIO	I^2C interface power input	1.62	1.8	1.98	V
		2.97	3.3	3.63	V
F_{SCL}	SCL clock frequency	—	—	3.4	MHz
$I2C_{VIL}$	SCL, SDA Low level input voltage	0.3 x V_{DDIO}	—	—	V
$I2C_{VIH}$	SCL, SDA High level input voltage	—	—	0.7 x V_{DDIO}	V
SDA_{VOL}	Low level output voltage at SDA pin (I = 20 mA)	—	—	0.4	V
C_{I2C}	Input capacitance at SCL / SDA	—	—	10	pF
t_{SPSCL}	SLC pulse width filtering time, when 50 ns filter selected (Fast speed, Fast speed plus)	40	—	150	ns
t_{SPSDA}	SDA pulse width filtering time, when 50 ns filter selected (Fast speed, Fast speed plus)	40	—	150	ns
t_{SPHSCL}	SLC pulse width filtering time, when 10 ns filter selected (High speed)	10	—	25	ns
t_{SPHSDA}	SDA pulse width filtering time, when 10 ns filter selected (High speed)	10	—	25	ns

24 Register Mapping

Table 80. Register mapping

Register	Main/FS	Address						R/W	Read / Write
		Adr_5	Adr_4	Adr_3	Adr_2	Adr_1	Adr_0		
M_FLAG	0	0	0	0	0	0	0	0	Read only
M_MODE	0	0	0	0	0	0	1	0(W) /1(R)	Read / Write
M_SM_CTRL1	0	0	0	0	0	1	0	0(W) /1(R)	Read / Write
M_REG_CTRL1	0	0	0	0	0	1	1	0(W) /1(R)	Write only
M_REG_CTRL2	0	0	0	0	1	0	0	0(W) /1(R)	Read / Write
M_REG_CTRL3	0	0	0	0	1	0	1	0(W) /1(R)	Read / Write
M_TSD_CFG	0	0	0	0	1	1	0	0(W) /1(R)	Read / Write
M_AMUX	0	0	0	0	1	1	1	0(W) /1(R)	Read / Write
M_CLOCK1	0	0	0	1	0	0	0	0(W) /1(R)	Read / Write
M_CLOCK2	0	0	0	1	0	0	1	0(W) /1(R)	Read / Write
M_INT_MASK1	0	0	0	1	0	1	0	0(W) /1(R)	Read / Write
M_INT_MASK2	0	0	0	1	0	1	1	0(W) /1(R)	Read / Write
M_FLAG1	0	0	0	1	1	0	0	0(W) /1(R)	Read / Write
M_FLAG2	0	0	0	1	1	0	1	0(W) /1(R)	Read / Write
M_FLAG3	0	0	0	1	1	1	0	0(W) /1(R)	Read / Write
M_VMON_REGX	0	0	0	1	1	1	1	0(W) /1(R)	Read / Write
M_LVB1_SVS	0	0	1	0	0	0	0	0	Read only
M_LVB1_STBY_DVS	0	0	1	0	0	0	1	0(W) /1(R)	Read / Write
M_MEMORY0	0	1	0	1	0	0	1	0(W) /1(R)	Read / Write
M_MEMORY1	0	1	0	1	0	1	0	0(W) /1(R)	Read / Write
M_DEVICEID	0	1	0	1	0	1	1	0	Read only
FS_GRL_FLAGS	1	0	0	0	0	0	0	0	Read only

Table 80. Register mapping...*continued*

Register	Main/FS	Address						R/W	Read / Write
		Adr_5	Adr_4	Adr_3	Adr_2	Adr_1	Adr_0		
FS_I_OVUV_SAFE_REACTION1	1	0	0	0	0	0	1	0(W) /1(R)	Write during INIT then Read only
FS_I_NOT_OVUV_SAFE_ REACTION1	1	0	0	0	0	1	0	0(W) /1(R)	Write during INIT then Read only
FS_I_OVUV_SAFE_REACTION2	1	0	0	0	0	1	1	0(W) /1(R)	Write during INIT then Read only
FS_I_NOT_OVUV_SAFE_ REACTION2	1	0	0	0	1	0	0	0(W) /1(R)	Write during INIT then Read only
FS_I_ABIST2_CTRL	1	0	0	0	1	0	1	0(W) /1(R)	Write during INIT then Read only
FS_I_NOT_ABIST2_CTRL	1	0	0	0	1	1	0	0(W) /1(R)	Write during INIT then Read only
FS_I_WD_CFG	1	0	0	0	1	1	1	0(W) /1(R)	Write during INIT then Read only
FS_I_NOT_WD_CFG	1	0	0	1	0	0	0	0(W) /1(R)	Write during INIT then Read only
FS_I_SAFE_INPUTS	1	0	0	1	0	0	1	0(W) /1(R)	Write during INIT then Read only
FS_I_NOT_SAFE_INPUTS	1	0	0	1	0	1	0	0(W) /1(R)	Write during INIT then Read only
FS_I_FSSM	1	0	0	1	0	1	1	0(W) /1(R)	Write during INIT then Read only
FS_I_NOT_FSSM	1	0	0	1	1	0	0	0(W) /1(R)	Write during INIT then Read only
FS_I_SVS	1	0	0	1	1	0	1	0(W) /1(R)	Write during INIT then Read only
FS_I_NOT_SVS	1	0	0	1	1	1	0	0(W) /1(R)	Write during INIT then Read only
FS_WD_WINDOW	1	0	0	1	1	1	1	0(W) /1(R)	Read / Write
FS_NOT_WD_WINDOW	1	0	1	0	0	0	0	0(W) /1(R)	Read / Write

Table 80. Register mapping...*continued*

Register	Main/FS	Address						R/W	Read / Write
		Adr_5	Adr_4	Adr_3	Adr_2	Adr_1	Adr_0		
FS_WD_SEED	1	0	1	0	0	0	1	0(W) /1(R)	Read / Write
FS_WD_ANSWER	1	0	1	0	0	1	0	0(W) /1(R)	Read / Write
FS_OVUVREG_STATUS	1	0	1	0	0	1	1	0(W) /1(R)	Read / Write
FS_RELEASE_FS0B	1	0	1	0	1	0	0	0(W) /1(R)	Read / Write
FS_SAFE_IOS	1	0	1	0	1	0	1	0(W) /1(R)	Read / Write
FS_DIAG_SAFETY	1	0	1	0	1	1	0	0(W) /1(R)	Read / Write
FS_INTB_MASK	1	0	1	0	1	1	1	0(W) /1(R)	Read / Write
FS_STATES	1	0	1	1	0	0	0	0(W) /1(R)	Read / Write

25 Main I2C Register Mapping

25.1 M_FLAG register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	0	0	0	0	0	0	0	0
Read	**DIE_ CENTER_ TEMPFLG_ G**	**VBOS_G**	**COM_ERR**	**PWRON_G**	**VPRE_G**	**BOOST_G**	**BUCK1_G**	**BUCK2_G**
Reset	0	0	0	0	0	0	0	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
0	0	0	0	0	0	0	0
BUCK3_G	**LDO1_G**	**LDO2_G**	**LDO3_G**	**HVLDO_G**	**STBY_TIMER_G**	**VSUP_G**	**TSD_BIST_ ERR_G**
0	0	0	0	0	0	0	0

Table 81. M_FLAG register description

DIE_CENTER_ TEMPFLG_G	Description	Report a die center temperature Flag for the MCU
	0	No event
	1	Event occurred
	Reset condition	POR
VBOS_G	Description	Report a VBOS UVH event
	0	No event
	1	Event occurred
	Reset condition	POR
COM_ERR	Description	Report an I2C communication error
	0	No error
	1	Error occurred
	Reset condition	POR
PWRON_G	Description	Report a wake-up event: PWRON1 or PWRON2
	0	No wake event
	1	Wake event
	Reset condition	POR
VPRE_G	Description	Report an event on VPRE (status change or failure)
	0	No event
	1	Event occurred
	Reset condition	POR
BOOST_G	Description	Report an event on BOOST (status change or failure)
	0	No event
	1	Event occurred
	Reset condition	POR
BUCK1_G	Description	Report an event on BUCK1 (status change or failure)
	0	No event
	1	Event occurred
	Reset condition	POR
BUCK2_G	Description	Report an event on BUCK2 (status change or failure)
	0	No event
	1	Event occurred
	Reset condition	POR
BUCK3_G	Description	Report an event on BUCK3 (status change or failure)
	0	No event
	1	Event occurred
	Reset condition	POR
LDO1_G	Description	Report an event on LDO1 (status change or failure)

Table 81. M_FLAG register description...*continued*

	0	No event
	1	Event occurred
	Reset condition	POR
LDO2_G	Description	Report an event on LDO2 (status change or failure)
	0	No event
	1	Event occurred
	Reset condition	POR
LDO3_G	Description	Report an event on LDO3 (status change or failure)
	0	No event
	1	Event occurred
	Reset condition	POR
HVLDO_G	Description	Report an event on HVLDO (status change or failure)
	0	No event
	1	Event occurred
	Reset condition	POR
STBY_TIMER_G	Description	Report a Standby timer expiration
	0	No error
	1	Standby timer expiration
	Reset condition	POR
VSUP_G	Description	Report a VSUP UVL, UVH and UV7
	0	No event
	1	Event occurred
	Reset condition	POR
TSD_BIST_ERR_G	Description	Report a TSD event
	0	No event
	1	Event occurred
	Reset condition	POR

25.2 M_MODE register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	0	0	0	0	0	0	0	0
Read	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reset	0	0	0	0	0	0	0	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
0	**EXT_ FIN_DIS**	0	**PWRON2_ DSM_EN**	**STBY_ PGOOD_ TEST_LVL**	**PWRON2DIS**	**PWRON1DIS**	**STBY_ PGOOD_ TEST_EN**
PLL_ LOCKED	Reserved	**MAIN_ NORMAL**	**PWRON2_ DSM_EN**	**STBY_ PGOOD_ TEST_LVL**	**PWRON2DIS**	**PWRON1DIS**	**STBY_ PGOOD_ TEST_EN**
0	0	0	0	0	0	0	0

Table 82. M_MODE register description

STBY_PGOOD_ TEST_EN	Description	Enable or disable the Standby PGOOD test function (only available if OTP enable)
	0	Disabled
	1	Enabled
	Reset condition	POR
PWRON1DIS	Description	Disable the wake-up feature on PWRON1 input
	0	Wake up enabled
	1	Wake up disabled
	Reset condition	POR
PWRON2DIS	Description	Disable the wake-up feature on PWRON2 input
	0	Wake up enabled
	1	Wake up disabled
	Reset condition	POR
STBY_PGOOD_ TEST_LVL	Description	Change the STBY_PGOOD output level if STBY_PGOOD_TEST_EN = 1
	0	High
	1	Low
	Reset condition	POR
PWRON2_DSM_EN	Description	Enable / Disable Deep Sleep Mode request via the PWRON2 pin if DSM_ EN_OTP = 1
	0	No transition to DSM
	1	Transition to DSM
	Reset condition	POR
MAIN_NORMAL	Description	Main state machine status
	0	Main state machine not in normal mode
	1	Main state machine is in normal mode (M15)
	Reset condition	POR
EXT_FIN_DIS	Description	Disable the external FIN selection at PLL input
	0	No effect
	1	Disable FIN selection
	Reset condition	POR

Table 82. M_MODE register description...*continued*

PLL_LOCKED	Description	Indicate if the PLL is locked
	0	Not Locked
	1	Locked
	Reset condition	POR

25.3 M_SM_CTRL1 register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	**TIMER_STBY_WINDOW [3:0]**				0	**STBY_ TIMER_EN**	0	0
Read	**TIMER_STBY_WINDOW [3:0]**				RESE RVED	**STBY_ TIMER_EN**	RESERVED	RESERVED
Reset	0	0	0	0	0	OTP	0	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
0	0	0	0	0	0	0	**GOTO_OFF**
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
0	0	0	0	0	0	0	0

Table 83. M_SM_CTRL1 register description

GOTO_OFF	Description	Entry to OFF mode/state
	0	No effect; Device remains in current state
	1	Device will enter OFF mode (M1)
	Reset condition	POR
STBY_TIMER_EN	Description	Enable or disable the standby timer
	0	Disabled
	1	Enabled
	Reset condition	POR
TIMER_STBY_ WINDOW [3:0]	Description	Set the standby timer window duration (ms)
	[0,1,10,11,100,101,110,111]	[16,32,128,512,1024,4096,8192,16384]
	[1000,1001,1010,1011 ,1100,1101,1110,1111]	[65536,131072,262144,524288,1048576,2097152,4194304,8388608]
	Reset condition	POR

25.4 M_REG_CTRL1 register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	**VPREDIS**	**BOOSTDIS**	**BUCK1DIS**	**BUCK2DIS**	**BUCK3DIS**	**LDO1DIS**	**LDO2DIS**	**LDO3DIS**
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
RESERVED	**BOOSTEN**	**BUCK1EN**	**BUCK2EN**	**BUCK3EN**	**LDO1EN**	**LDO2EN**	**LDO3EN**
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
0	0	0	0	0	0	0	0

Table 84. M_REG_CTRL1 register description

LDO3EN	Description	Enable request of LDO3
	0	no effect (regulator remains in existing state)
	1	LDO3 Enable Request
	Reset condition	POR
LDO2EN	Description	Enable request of LDO2
	0	no effect (regulator remains in existing state)
	1	LDO2 Enable Request
	Reset condition	POR
LDO1EN	Description	Enable request of LDO1
	0	no effect (regulator remains in existing state)
	1	LDO1 Enable Request
	Reset condition	POR
BUCK3EN	Description	Enable request of BUCK3
	0	no effect (regulator remains in existing state)
	1	BUCK3 Enable Request
	Reset condition	POR
BUCK2EN	Description	Enable request of BUCK2
	0	no effect (regulator remains in existing state)
	1	BUCK2 Enable Request
	Reset condition	POR
BUCK1EN	Description	Enable request of BUCK1
	0	no effect (regulator remains in existing state)
	1	BUCK1 Enable Request
	Reset condition	POR
BOOSTEN	Description	Enable request of BOOST
	0	no effect (regulator remains in existing state)

Table 84. M_REG_CTRL1 register description*...continued*

	1	BOOST Enable Request
	Reset condition	POR
	Description	Disable request of LDO3
	0	no effect (regulator remains in existing state)
	1	LDO3 Disable Request
	Reset condition	POR
LDO3DIS	Description	Disable request of LDO3
	0	no effect (regulator remains in existing state)
	1	LDO3 Disable Request
	Reset condition	POR
LDO2DIS	Description	Disable request of LDO2
	0	no effect (regulator remains in existing state)
	1	LDO2 Disable Request
	Reset condition	POR
LDO1DIS	Description	Disable request of LDO1
	0	no effect (regulator remains in existing state)
	1	LDO1 Disable Request
	Reset condition	POR
BUCK3DIS	Description	Disable request of BUCK3
	0	no effect (regulator remains in existing state)
	1	BUCK3 Disable Request
	Reset condition	POR
BUCK2DIS	Description	Disable request of BUCK2
	0	no effect (regulator remains in existing state)
	1	BUCK2 Disable Request
	Reset condition	POR
BUCK1DIS	Description	Disable request of BUCK1
	0	no effect (regulator remains in existing state)
	1	BUCK1 Disable Request
	Reset condition	POR
BOOSTDIS	Description	Disable request of BOOST
	0	no effect (regulator remains in existing state)
	1	BOOST Disable Request
	Reset condition	POR
VPREDIS	Description	Disable request of VPRE in case of 2xVR5510 are used
	0	no effect (regulator remains in existing state)
	1	VPRE Disable Request

Table 84. M_REG_CTRL1 register description...*continued*

	Reset condition	POR

25.5 M_REG_CTRL2 register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	0	0	**VPRESRHS_MSB [1:0]**		0	0	0	**HVLDODIS**
Read	RESERVED	RESERVED	**VPRESRHS_MSB [1:0]**		RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	OTP		0	0	0	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
HVLDOEN	**VPRE_ PLDWN_DIS**	**VBSTSR [1:0]**		**VPRESRLS [1:0]**		**VPRESRHS [1:0]**	
RESERVED	**VPRE_ PLDWN_DIS**	**VBSTSR [1:0]**		**VPRESRLS [1:0]**		**VPRESRHS [1:0]**	
0	0	OTP		OTP		OTP	

Table 85. M_REG_CTRL2 register description

VPRESRHS [1:0]	Description	VPRE High Side pull down slew rate control
	10	520mA typical drive capability - fast
	11	900mA typical drive capability - ultra fast
	Reset condition	POR
VPRESRLS [1:0]	Description	VPRE Low Side slew rate control
	00	130mA typical drive capability - slow
	01	260mA typical drive capability - medium
	10	520mA typical drive capability - fast
	11	900mA typical drive capability - ultra fast
	Reset condition	POR
VBSTSR [1:0]	Description	VBOOST Low Side slew rate control
	00	50V/us
	01	100V/us
	10	300V/us - fast
	11	500V/us - ultra fast
	Reset condition	POR
VPRE_ PLDWN_DIS	Description	Force disable of VPRE pull down
	0	No effect (VPRE pull down will be automatically controlled by the logic)
	1	VPRE pull down is disabled

Table 85. M_REG_CTRL2 register description*...continued*

	Reset condition	POR
HVLDOEN	Description	Enable of HVLDO
	0	No effect (regulator remains in existing state)
	1	Enable
	Reset condition	POR
HVLDODIS	Description	Disable of HVLDO
	0	No effect (regulator remains in existing state)
	1	HVLDO Disable
	Reset condition	POR
VPRESRHS_ MSB [1:0]	Description	VPRE High Side pull up slew rate control
	00	130mA typical drive capability - slow
	01	260mA typical drive capability - medium
	10	520mA typical drive capability - fast
	11	900mA typical drive capability - ultra fast
	Reset condition	POR

25.6 M_REG_CTRL3 register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	0	**LDO3 _ STBY**	0	**LDO2 _ STBY**	0	**LDO1 _ STBY**	0	**HVLDO _STBY**
Read	RESERVED	**LDO3 _ STBY**	RESERVED	**LDO2 _ STBY**	RESERVED	**LDO1 _ STBY**	RESERVED	**HVLDO _STBY**
Reset	0	1	0	1	0	1	0	1

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
0	**VPREV_ STBY**	0	**BUCK3_ STBY**	0	**BUCK2_ STBY**	0	**BUCK1_ STBY**
RESERVED	**VPREV_ STBY**	RESERVED	**BUCK3_ STBY**	RESERVED	**BUCK2_ STBY**	RESERVED	**BUCK1_ STBY**
0	1	0	1	0	1	0	1

Table 86. M_REG_CTRL3 register description

BUCK1_STBY	Description	Enable/Disable BUCK1 in standby mode
	0	Disabled
	1	Enabled
	Reset condition	POR

Table 86. M_REG_CTRL3 register description*...continued*

BUCK2_STBY	Description	Enable/Disable BUCK2 in standby mode
	0	Disabled
	1	Enabled
	Reset condition	POR
BUCK3_STBY	Description	Enable/Disable BUCK3 in standby mode
	0	Disabled
	1	Enabled
	Reset condition	POR
VPREV_STBY	Description	Set the VPRE voltage in standby mode (only if VPREV_STBY_EN_OTP = 1)
	0	3.3V
	1	3V (setting only available if VPRE is set at 3.3V in normal mode)
	Reset condition	POR
HVLDO_STBY	Description	Enable/Disable HVLDO in standby mode
	0	Disabled
	1	Enabled
	Reset condition	POR
LDO1_STBY	Description	Enable/Disable LDO1 in standby mode
	0	Disabled
	1	Enabled
	Reset condition	POR
LDO2_STBY	Description	Enable/Disable LDO2 in standby mode
	0	Disabled
	1	Enabled
	Reset condition	
LDO3_STBY	Description	Enable/Disable LDO3 in standby mode
	0	Disabled
	1	Enabled
	Reset condition	POR

25.7 M_TSD_CFG register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	0	0	0	0	0	**DIE_CENTER_TEMP [2:0]**		
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	**DIE_CENTER_TEMP [2:0]**		
Reset	0	0	0	0	0	OTP		

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
BOOST_ TSDCFG	**BUCK1_ TSDCFG**	**BUCK2_ TSDCFG**	**BUCK3_ TSDCFG**	**LDO1_ TSDCFG**	**LDO2_ TSDCFG**	**LDO3_ TSDCFG**	**HVLDO_ TSDCFG**
BOOST_ TSDCFG	**BUCK1_ TSDCFG**	**BUCK2_ TSDCFG**	**BUCK3_ TSDCFG**	**LDO1_ TSDCFG**	**LDO2_ TSDCFG**	**LDO3_ TSDCFG**	**HVLDO_ TSDCFG**
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP

Table 87. M_TSD_CFG register description

HVLDO_TSDCFG	Description	Behavior in case of thermal shutdown
	0	HVLDO Shutdown
	1	HVLDO Shutdown + state machine transition to DFS
	Reset condition	POR
LDO3_TSDCFG	Description	Behavior in case of thermal shutdown
	0	LDO3 Shutdown
	1	LDO3 Shutdown + state machine transition to DFS
	Reset condition	POR
LDO2_TSDCFG	Description	Behavior in case of thermal shutdown
	0	LDO2 Shutdown
	1	LDO2 Shutdown + state machine transition to DFS
	Reset condition	POR
LDO1_TSDCFG	Description	Behavior in case of thermal shutdown
	0	LDO1 Shutdown
	1	LDO1 Shutdown + state machine transition to DFS
	Reset condition	POR
BUCK3_TSDCFG	Description	Behavior in case of thermal shutdown
	0	BUCK3 Shutdown
	1	BUCK3 Shutdown + state machine transition to DFS
	Reset condition	POR
BUCK2_TSDCFG	Description	Behavior in case of thermal shutdown
	0	BUCK2 Shutdown
	1	BUCK2 Shutdown + state machine transition to DFS
	Reset condition	POR
BUCK1_TSDCFG	Description	Behavior in case of thermal shutdown
	0	BUCK1 Shutdown
	1	BUCK1 Shutdown + state machine transition to DFS
	Reset condition	POR
BOOST_TSDCFG	Description	Behavior in case of thermal shutdown
	0	BOOST Shutdown

Table 87. M_TSD_CFG register description*...continued*

	1	BOOST Shutdown + state machine transition to DFS
	Reset condition	POR
DIE_CENTER_TEMP[2:0]	Description	Die center temperature indicator
	000	75°C
	001	90°C
	010	105°C
	011	120°C
	100	135°C
	101	150°C
	Reset condition	POR

25.8 M_AMUX register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
0	0	**RATIO**	**AMUX [4:0]**				
RESERVED	RESERVED	**RATIO**	**AMUX [4:0]**				
0	0	0	0	0	0	0	0

Table 88. M_AMUX register description

AMUX [4:0]	Refer to **Table 21**	
RATIO	Description	Selection of divider ratio for VSUP, PWRON1 inputs
	0	Ratio = 20
	1	Ration = 34
	Reset condition	POR

25.9 M_CLOCK1 register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	**MOD_CONF**	**FOUT_MUX_SEL[3:0]**				**FOUT_PHASE[2:0]**		
Read	**MOD_CONF**	**FOUT_MUX_SEL[3:0]**				**FOUT_PHASE[2:0]**		

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Reset	0	0	0	0	0	0	0	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
FOUT_SEL	**EXT_ FIN_SEL**	**FIN_DIV**	**MOD_EN**	**CLK_INT_FREQ[3:0]**			
FOUT_SEL	RESERVED	**FIN_DIV**	**MOD_EN**	**CLK_INT_FREQ[3:0]**			
0	0	0	0	0	0	0	0

Table 89. M_CLOCK1 register description

CLK_INT_FREQ [3:0]	Manual frequency tuning: Refer to **Table 17**	
MOD_EN	Description	CLOCK Modulation
	0	Modulation Disable
	1	Modulation Enable
	Reset condition	POR
FIN_DIV	Description	FIN input signal divider selection
	0	Divider by 1
	1	Divider by 6
	Reset condition	POR
EXT_FIN_SEL	Description	EXT FIN selection at PLL input
	0	Disabled
	1	Enabled
	Reset condition	POR
FOUT_SEL	Description	FOUT frequency selection (CLK1 or CLK2)
	0	CLK1
	1	CLK2
	Reset condition	POR
FOUT_PHASE[2:0]	Description	FOUT phase and delay setting
	000	No delay/phase
	001	1 clk cycle from OSCPLL
	010	2 clk cycle from OSCPLL
	011	3 clk cycle from OSCPLL
	100	4 clk cycle from OSCPLL
	101	5 clk cycle from OSCPLL
	110	6 clk cycle from OSCPLL
	111	7 clk cycle from OSCPLL
	Reset condition	POR

Table 89. M_CLOCK1 register description...*continued*

FOUT_MUX_SEL [3:0]	Refer to **Table 15**	
MOD_CONF	Description	CLOCK Modulation Configuration (spread spectrum)
	0	range +- 5% 23.15 kHz
	1	range +- 5% 92.6 kHz
	Reset condition	POR

25.10 M_CLOCK2 register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
0	0	0	0	0	0	**LOW_POWER_CLK [1 :0]**	
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	**LOW_POWER_CLK [1 :0]**	
0	0	0	0	0	0	0	0

Table 90. M_CLOCK2 register description

LOW_POWER_CLK [1:0]	Description	Low Power Clock frequency selection
	00	100 kHz
	01	100 kHz
	10	300 kHz
	11	600 kHz
	Reset condition	POR

25.11 M_INT_MASK1 register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	**HVLDOOC_M**	0	**BUCK1OC_M**	**BUCK2OC_M**	**BUCK3OC_M**	**LDO1OC_M**	**LDO2OC_M**	**LDO3OC_M**
Read	**HVLDOOC_M**	RESERVED	**BUCK1OC_M**	**BUCK2OC_M**	**BUCK3OC_M**	**LDO1OC_M**	**LDO2OC_M**	**LDO3OC_M**

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Reset	0	0	0	0	0	0	0	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
HVLDO_ TSDFLG_M	**BOOST_ TSDFLG_M**	**BUCK1_ TSDFLG_M**	**BUCK2_ TSDFLG_M**	**BUCK3_ TSDFLG_M**	**LDO1_ TSDFLG_M**	**LDO2_ TSDFLG_M**	**LDO3_ TSDFLG_M**
HVLDO_ TSDFLG_M	**BOOST_ TSDFLG_M**	**BUCK1_ TSDFLG_M**	**BUCK2_ TSDFLG_M**	**BUCK3_ TSDFLG_M**	**LDO1_ TSDFLG_M**	**LDO2_ TSDFLG_M**	**LDO3_ TSDFLG_M**
0	0	0	0	0	0	0	0

Table 91. M_INT_MASK1 register description

LDO3_TSDFLG_M	Description	Inhibit INTERRUPT for LDO3 over temperature shutdown event
	0	INT not masked
	1	INT masked
	Reset condition	POR
LDO2_TSDFLG_M	Description	Inhibit INTERRUPT for LDO2 over temperature shutdown event
	0	INT not masked
	1	INT masked
	Reset condition	POR
LDO1_TSDFLG_M	Description	Inhibit INTERRUPT for LDO1 over temperature shutdown event
	0	INT not masked
	1	INT masked
	Reset condition	POR
BUCK3_TSDFLG_M	Description	Inhibit INTERRUPT for BUCK3 over temperature shutdown event
	0	INT not masked
	1	INT masked
	Reset condition	POR
BUCK2_TSDFLG_M	Description	Inhibit INTERRUPT for BUCK2 over temperature shutdown event
	0	INT not masked
	1	INT masked
	Reset condition	POR
BUCK1_TSDFLG_M	Description	Inhibit INTERRUPT for BUCK1 over temperature shutdown event
	0	INT not masked
	1	INT masked
	Reset condition	POR
BOOST_TSDFLG_M	Description	Inhibit INTERRUPT for BOOST over temperature shutdown event
	0	INT not masked

Table 91. M_INT_MASK1 register description...*continued*

	1	INT masked
	Reset condition	POR
HVLDO_TSDFLG_M	Description	Inhibit INTERRUPT for HVLDO over temperature shutdown event
	0	INT not masked
	1	INT masked
	Reset condition	POR
LDO3OC_M	Description	Inhibit INTERRUPT for LDO3 Over current
	0	INT not masked
	1	INT masked
	Reset condition	POR
LDO2OC_M	Description	Inhibit INTERRUPT for LDO2 Over current
	0	INT not masked
	1	INT masked
	Reset condition	POR
LDO1OC_M	Description	Inhibit INTERRUPT for LDO1 Over current
	0	INT not masked
	1	INT masked
	Reset condition	POR
BUCK3OC_M	Description	Inhibit INTERRUPT for BUCK3 Over current
	0	INT not masked
	1	INT masked
	Reset condition	POR
BUCK2OC_M	Description	Inhibit INTERRUPT for BUCK2 Over current
	0	INT not masked
	1	INT masked
	Reset condition	POR
BUCK1OC_M	Description	Inhibit INTERRUPT for BUCK1 Over current
	0	INT not masked
	1	INT masked
	Reset condition	POR
HVLDOOC_M	Description	Inhibit INTERRUPT for HVLDO Over current
	0	INT not masked
	1	INT masked
	Reset condition	POR

25.12 M_INT_MASK2 register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	DIE_ CENTER_ TEMP FLG_M	COM_ ERR_M	VBOS UVH_M	VBOOST UVH_M	VBOOST OV_M	TSD_ BIST_ ERR_ FLG_M	HVLDO_ INPUT UVL_M	VPRE OV2_M
Read	DIE_ CENTER_ TEMP FLG_M	COM_ ERR_M	VBOS UVH_M	VBOOST UVH_M	VBOOST OV_M	TSD_ BIST_ ERR_ FLG_M	HVLDO_ INPUT UVL_M	VPRE OV2_M
Reset	0	0	0	0	0	0	0	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
VPREOC_M	VPREUVL_M	VPREUVH_M	VSUPUV7_M	VSUP UVL_M	VSUP UVH_M	PWRON2 FLG_M	PWRON1 FLG_M
VPREOC_M	VPREUVL_M	VPREUVH_M	VSUPUV7_M	VSUP UVL_M	VSUP UVH_M	PWRON2 FLG_M	PWRON1 FLG_M
0	0	0	0	0	0	0	0

Table 92. M_INT_MASK2 register description

PWRON1FLG_M	Description	Inhibit interrupt for transition on PWRON1
	0	INT not masked
	1	INT masked
	Reset condition	POR
PWRON2FLG_M	Description	Inhibit interrupt for transition on PWRON2
	0	INT not masked
	1	INT masked
	Reset condition	POR
VSUPUVH_M	Description	Inhibit interrupt for VSUP_UVH
	0	INT not masked
	1	INT masked
	Reset condition	POR
VSUPUVL_M	Description	Inhibit interrupt for VSUP_UVL
	0	INT not masked
	1	INT masked
	Reset condition	POR
VSUPUV7_M	Description	Inhibit interrupt for VSUP_UV7
	0	INT not masked
	1	INT masked
	Reset condition	POR

Table 92. M_INT_MASK2 register description*...continued*

VPREUVH_M	Description	Inhibit interrupt for VPRE_UVH
	0	INT not masked
	1	INT masked
	Reset condition	POR
VPREUVL_M	Description	Inhibit interrupt for VPRE_UVL
	0	INT not masked
	1	INT masked
	Reset condition	POR
VPREOC_M	Description	Inhibit interrupt for VPRE overcurrent event
	0	INT not masked
	1	INT masked
	Reset condition	POR
VPREOV2_M	Description	Inhibit interrupt for VPRE OV event
	0	INT not masked
	1	INT masked
	Reset condition	POR
HVLDO_ INPUT_UVL_M	Description	Inhibit interrupt for HVLDO UVL
	0	INT not masked
	1	INT masked
	Reset condition	POR
TSD_BIST_ ERR_FLG_M	Description	Inhibit interrupt for TSD BIST error
	0	INT not masked
	1	INT masked
	Reset condition	POR
VBOOSTOV_M	Description	Inhibit interrupt for VBOOST OV
	0	INT not masked
	1	INT masked
	Reset condition	POR
VBOOSTUVH_M	Description	Inhibit interrupt for VBOOST UVH
	0	INT not masked
	1	INT masked
	Reset condition	POR
VBOSUVH_M	Description	Inhibit interrupt for VBOS UVH
	0	INT not masked
	1	INT masked
	Reset condition	POR
COM_ERR_M	Description	Inhibit interrupt for I2C communication error

Table 92. M_INT_MASK2 register description...*continued*

	0	INT not masked
	1	INT masked
	Reset condition	POR
DIE_CENTER_ TEMPFLG_M	Description	Inhibit interrupt for thermal event on the central thermal sensor
	0	INT not masked
	1	INT masked
	Reset condition	POR

25.13 M_FLAG1 register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	**HVLDOOC**	0	**BUCK1OC**	**BUCK2OC**	**BUCK3OC**	**LDO1OC**	**LDO2OC**	**LDO3OC**
Read	**HVLDOOC**	RESERVED	**BUCK1OC**	**BUCK2OC**	**BUCK3OC**	**LDO1OC**	**LDO2OC**	**LDO3OC**
Reset	0	0	0	0	0	0	0	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
HVLDO_ TSDFLG	**BOOST_ TSDFLG**	**BUCK1_ TSDFLG**	**BUCK2_ TSDFLG**	**BUCK3_ TSDFLG**	**LDO1_ TSDFLG**	**LDO2_ TSDFLG**	**LDO3_ TSDFLG**
HVLDO_ TSDFLG	**BOOST_ TSDFLG**	**BUCK1_ TSDFLG**	**BUCK2_ TSDFLG**	**BUCK3_ TSDFLG**	**LDO1_ TSDFLG**	**LDO2_ TSDFLG**	**LDO3_ TSDFLG**
0	0	0	0	0	0	0	0

When the device starts-up, clear the flags by writing 1 to all bits.

Table 93. M_FLAG1 register description

LDO3_TSDFLG	Description	LDO3 over temperature shutdown event
	0	No event
	1	Event occurred
	Reset condition	POR / Clear on Write (write ‘1’)
LDO2_TSDFLG	Description	LDO2 over temperature shutdown event
	0	No event
	1	Event occurred
	Reset condition	POR / Clear on Write (write ‘1’)
LDO1_TSDFLG	Description	LDO1 over temperature shutdown event
	0	No event
	1	Event occurred
	Reset condition	POR / Clear on Write (write ‘1’)
BUCK3_TSDFLG	Description	BUCK3 over temperature shutdown event

Table 93. M_FLAG1 register description...*continued*

	0	No event
	1	Event occurred
	Reset condition	POR / Clear on Write (write '1')
BUCK2_TSDFLG	Description	BUCK2 over temperature shutdown event
	0	No event
	1	Event occurred
	Reset condition	POR / Clear on Write (write '1')
BUCK1_TSDFLG	Description	BUCK1 over temperature shutdown event
	0	No event
	1	Event occurred
	Reset condition	POR / Clear on Write (write '1')
BOOST_TSDFLG	Description	BOOST over temperature shutdown event
	0	No event
	1	Event occurred
	Reset condition	POR / Clear on Write (write '1')
HVLDO_TSDFLG	Description	HVLDO over temperature shutdown event
	0	No event
	1	Event occurred
	Reset condition	POR / Clear on Write (write '1')
LDO3OC	Description	LDO3 Over current
	0	No event
	1	Event occurred
	Reset condition	POR / Clear on Write (write '1')
LDO2OC	Description	LDO2 Over current
	0	No event
	1	Event occurred
	Reset condition	POR / Clear on Write (write '1')
LDO1OC	Description	LDO1 Over current
	0	No event
	1	Event occurred
	Reset condition	POR / Clear on Write (write '1')
BUCK3OC	Description	BUCK3 Over current
	0	No event
	1	Event occurred
	Reset condition	POR / Clear on Write (write '1')
BUCK2OC	Description	BUCK2 Over current
	0	No event

Table 93. M_FLAG1 register description...*continued*

	1	Event occurred
	Reset condition	POR / Clear on Write (write '1')
BUCK1OC	Description	BUCK1 Over current
	0	No event
	1	Event occurred
	Reset condition	POR / Clear on Write (write '1')
HVLDOOC	Description	HVLDO Over current
	0	No event
	1	Event occurred
	Reset condition	POR / Clear on Write (write '1')

25.14 M_FLAG2 register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	**DIE_ CENTER_ TEMPFLG**	**TSD_BIST_ ERR_FLG**	**VBOSUVH**	**VBOO STUVH**	**VBOO STOV**	**STBY_ TIMER_ FLG**	**HVLDO_ INPUT_ UVL**	**VPRE_ FB_OV**
Read	**DIE_ CENTER_ TEMPFLG**	**TSD_BIST_ ERR_FLG**	**VBOSUVH**	**VBOO STUVH**	**VBOO STOV**	**STBY_ TIMER_ FLG**	**HVLDO_ INPUT_ UVL**	**VPRE_ FB_OV**
Reset	0	0	0	0	0	0	0	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
VPREOC	**VPREUVL**	**VPREUVH**	**VSUPUV7**	**VSUPUVL**	**VSUPUVH**	**PWRO N2FLG**	**PWRO N1FLG**
VPREOC	**VPREUVL**	**VPREUVH**	**VSUPUV7**	**VSUPUVL**	**VSUPUVH**	**PWRO N2FLG**	**PWRO N1FLG**
0	0	0	0	0	0	0	0

When the device starts-up, clear the flags by writing 1 to all bits.

Table 94. M_FLAG2 register description

PWRON1FLG	Description	PWRON1 wake up source flag
	0	No event
	1	Low to high wake event occurred
	Reset condition	POR / Clear on Write (write '1')
PWRON2FLG	Description	PWRON2 wake up source flag
	0	No event
	1	Low to high wake event occurred

Table 94. M_FLAG2 register description*...continued*

	Reset condition	POR / Clear on Write (write '1')
VSUPUVH	Description	VSUP_UVH event
	0	No event
	1	Event occurred
	Reset condition	POR / Clear on Write (write '1')
VSUPUVL	Description	VSUP_UVL event
	0	No event
	1	Event occurred
	Reset condition	POR / Clear on Write (write '1')
VSUPUV7	Description	VSUP_UV7 event
	0	No event
	1	Event occurred
	Reset condition	POR / Clear on Write (write '1')
VPREUVH	Description	VPRE_UVH event
	0	No event
	1	Event occurred
	Reset condition	POR / Clear on Write (write '1')
VPREUVL	Description	VPRE_UVL event
	0	No event
	1	Event occurred
	Reset condition	POR / Clear on Write (write '1')
VPREOC	Description	VPRE overcurrent event
	0	No event
	1	Event occurred
	Reset condition	POR / Clear on Write (write '1')
VPRE_FB_OV	Description	VPRE_FB_OV event
	0	No event
	1	Event occurred
	Reset condition	POR / Clear on Write (write '1')
HVLDO_INPUT_UVL	Description	HVLDO input UVL event
	0	No event
	1	Event occurred
	Reset condition	POR / Clear on Write (write '1')
STBY_TIMER_FLG	Description	STBY Timer event
	0	No event
	1	Event occurred
	Reset condition	POR / Clear on Write (write '1')

Table 94. M_FLAG2 register description...*continued*

VBOOSTOV	Description	VBOOST OV event
	0	No event
	1	Event occurred
	Reset condition	POR / Clear on Write (write '1')
VBOOSTUVH	Description	VBOOST UVH event
	0	No event
	1	Event occurred
	Reset condition	POR / Clear on Write (write '1')
VBOSUVH	Description	VBOS UVH event
	0	No event
	1	Event occurred
	Reset condition	POR / Clear on Write (write '1')
TSD_BIST_ERR_FLG	Description	TSD BIST flag
	0	TSD BIST OK
	1	TSD BIST NOT OK
	Reset condition	POR / Clear on Write (write '1')
DIE_CENTER_TEMPFLG	Description	Report a thermal event on the central thermal sensor
	0	No event
	1	Event occurred
	Reset condition	POR / Clear on Write (write '1')

25.15 M_FLAG3 register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	0	0	0	0	0	0	0	0
Read	**VPRE_ST**	**HVLDO_ST**	**BOOST_ST**	**BUCK1_ST**	**BUCK2_ST**	**BUCK3_ST**	**LDO1_ST**	**LDO2_ST**
Reset	0	0	0	0	0	0	0	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
0	0	0	0	0	0	**I2C_M_CRC**	**I2C_M_REQ**
LDO3_ST	**FIN_CLKWD_OK**	RESERVED	RESERVED	**PWRON2RT**	**PWRON1RT**	**I2C_M_CRC**	**I2C_M_REQ**
0	0	0	0	0	0	0	0

When the device starts-up, clear the flags by writing 1 to all bits.

Table 95. M_FLAG3 register description

I2C_M_REQ	Description	Invalid main domain I2C access
	0	No Error
	1	Error occurred
	Reset condition	POR / Clear on Write (write ‘1’)
I2C_M_CRC	Description	I2C communication CRC error
	0	No error
	1	Error occurred
	Reset condition	POR / Clear on Write (write ‘1’)
PWRON1RT	Description	Report event: PWRON1 real time state
	0	PWRON1 is low level
	1	PWRON1 is high
	Reset condition	Real time information
PWRON2RT	Description	Report event: PWRON2 real time state
	0	PWRON2 is low level
	1	PWRON2 is high
	Reset condition	Real time information
FIN_CLKWD_OK	Description	CLK watchdog monitoring
	0	Not used or out of range
	1	FIN_CLKWD_OK
	Reset condition	POR
LDO3_ST	Description	LDO3 state
	0	regulator OFF
	1	regulator ON
	Reset condition	Real time information
LDO2_ST	Description	LDO2 state
	0	regulator OFF
	1	regulator ON
	Reset condition	Real time information
LDO1_ST	Description	LDO1 state
	0	regulator OFF
	1	regulator ON
	Reset condition	Real time information
BUCK3_ST	Description	BUCK3 state
	0	regulator OFF
	1	regulator ON
	Reset condition	Real time information
BUCK2_ST	Description	BUCK2 state

Table 95. M_FLAG3 register description...*continued*

	0	regulator OFF
	1	regulator ON
	Reset condition	Real time information
BUCK1_ST	Description	BUCK1 state
	0	regulator OFF
	1	regulator ON
	Reset condition	Real time information
BOOST_ST	Description	BOOST state
	0	regulator OFF
	1	regulator ON
	Reset condition	Real time information
HVLDO_ST	Description	HVLDO state
	0	regulator OFF
	1	regulator ON
	Reset condition	Real time information
VPRE_ST	Description	VPRE state
	0	regulator OFF
	1	regulator ON
	Reset condition	Real time information

25.16 M_VMON_REGx register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	0	0	0	0	**VMON4_REG_ASSIGN [2:0]**			**VMON3_ REG_ASSIGN**
Read	RESERVED	RESERVED	RESERVED	RESERVED	**VMON4_REG_ASSIGN [2:0]**			**VMON3_ REG_ASSIGN**
Reset	0	0	0	0	0	0	0	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
VMON3_REG_ASSIGN [2:0]		**VMON2_REG_ASSIGN [2:0]**			**VMON1_REG_ASSIGN [2:0]**		
VMON3_REG_ASSIGN [2:0]		**VMON2_REG_ASSIGN [2:0]**			**VMON1_REG_ASSIGN [2:0]**		
0	0	0	0	0	0	0	0

Table 96. M_VMON_REGX register description

VMON1_REG_ ASSIGN [2:0]	Description	Regulator Assignment to VMON1
	000	External Regulator
	001	VPRE
	010	LDO1
	011	LDO2
	100	BUCK3
	101	BOOST
	110	LDO3
	111	BUCK2
	Reset condition	POR
VMON2_REG_ ASSIGN [2:0]	Description	Regulator Assignment to VMON2
	000	External Regulator
	001	VPRE
	010	LDO1
	011	LDO2
	100	BUCK3
	101	BOOST
	110	LDO3
	111	BUCK2
	Reset condition	POR
VMON3_REG_ ASSIGN [2:0]	Description	Regulator Assignment to VMON3
	000	External Regulator
	001	VPRE
	010	LDO1
	011	LDO2
	100	BUCK3
	101	BOOST
	110	LDO3
	111	BUCK2
	Reset condition	POR
VMON4_REG_ ASSIGN [2:0]	Description	Regulator Assignment to VMON4
	000	External Regulator
	001	VPRE
	010	LDO1
	011	LDO2
	100	BUCK3
	101	BOOST

Table 96. M_VMON_REGX register description*...continued*

	110	LDO3
	111	BUCK2
	Reset condition	POR

25.17 M_LVB1_SVS register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
0	0						
RESERVED	**LVB1_SVS [6:0]**						
0	0	0	0	0	0	0	0

Table 97. M_LVB1_SVS register description

	Description	Static Voltage Scaling offset (mV)
LVB1_SVS [6:0]	0000000	0
	0000001	6.25
	0000010	12.50
	0000011	18.75
	0000100	25
	0000101	31.25
	0000110	37.5
	0000111	43.75
	0001000	50
	0001001	56.25
	0001010	62.5
	0001011	68.75
	0001100	75
	0001101	81.25
	0001110	87.5
	0001111	93.75
	0010000	100

Table 97. M_LVB1_SVS register description...*continued*

	0010001	106.25
	0010010	112.5
	0010011	118.75
	0010100	125
	0010101	131.25
	0010110	137.5
	0010111	143.75
	0011000	150
	0011001	156.25
	0011010	162.5
	0011011	168.75
	0011100	175
	0011101	181.25
	0011110	187.5
	0011111	193.75
	0100000	200
	0100001	206.25
	0100010	212.5
	0100011	218.75
	0100100	225
	0100101	231.25
	0100110	237.5
	0100111	243.75
	0101000	250
	0101001	256.25
	0101010	262.5
	0101011	268.75
	0101100	275
	0101101	281.25
	0101110	287.5
	0101111	293.75
	0110000	300
	0110001	306.25
	0110010	312.5
	0110011	318.75
	0110100	325
	0110101	331.25

Table 97. M_LVB1_SVS register description...*continued*

	0110110	337.5
	0110111	343.75
	0111000	350
	0111001	356.25
	0111010	362.5
	0111011	368.75
	0111100	375
	0111101	381.25
	0111110	387.5
	0111111	393.75
	Reset condition	POR

25.18 M_LVB1_STBY_DVS register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
BUCK1_STBY [7:0]							
BUCK1_STBY [7:0]							
OTP							

Table 98. M_LVB1_STBY_DVS register description

	BUCK1 output voltage in standby mode	
BUCK1_STBY[7:0]	00000000 to 11111111	0.4V to 1.8V

25.19 M_MEMORY0 register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	**M_MEMORY0[15:0]**							
Read	**M_MEMORY0[15:0]**							
Reset	0	0	0	0	0	0	0	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
M_MEMORY0 [15:0]							
M_MEMORY0 [15:0]							
0	0	0	0	0	0	0	0

Table 99. M_MEMORY0 register description

M_MEMORY0 [15:0]	Description	Free memory field for data storage
	0...	16 bits free memory
	...1	
	Reset condition	POR

25.20 M_MEMORY1 register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	M_MEMORY1 [15:0]							
Read	M_MEMORY1 [15:0]							
Reset	0	0	0	0	0	0	0	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
RW							
M_MEMORY1 [15:0]							
0	0	0	0	0	0	0	0

Table 100. M_MEMORY1 register description

M_MEMORY1 [15:0]	Description	Free memory field for data storage
	0…	16 bits free memory
	…1	
	Reset condition	POR

25.21 M_DEVICEID register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	0	0			0	0		
Read	RESERVED	**FMREV[2:0]**			RESERVED	**MMREV[2:0]**		

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Reset (for B1)	0	0	1	0	0	0	0	1

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
0				0			
FAM_ID[3:0]				**DEV_ID [3:0]**			
0	1	1	0	0	0	0	1

RO: Read Only; RW: Read/Write; W: Write, RWOTP: default value loaded from OTP, FLGWC: clear on write flag

Table 101. M_DEVICEID register description

DEV_ID[3:0]	Description	Device ID
	[3:0]	0001: default value for VR5510
	Reset condition	POR
FAM_ID[3:0]	Description	Family ID
	[3:0]	0110: default value for VR5510
	Reset condition	POR
MMREV[2:0]	Description	Metal Mask Revision
	[2:0]	Metal Mask Revision configured by metal connection
	Reset condition	POR
FMREV[2:0]	Description	Full Mask Revision
	[2:0]	Full Mask Revision configured by metal connection
	Reset condition	POR

26 Fail-Safe Register Mapping

26.1 FS_GRL_FLAGS register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	0	0	0	0	**TIMING_ WINDOW_ STBY_FLG**	**STBY_ WAKE_UP**	0	0
Read	**FS_COM_G**	**FS_WD_G**	**FS_IO_G**	**FS_REG_ OVUV_G**	**TIMING_ WINDOW_ STBY_FLG**	**STBY_ WAKE_UP**	**FCCU1_RT**	**FCCU2_RT**
Reset	0	0	0	0	0	0	0	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
0	0	0	0	0	0	0	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
0	0	0	0	0	0	0	0

Table 102. FS_GRL_FLAGS register description

FCCU2_RT	Description	Report the real state of the FCCU2 status
	0	FCCU2 low
	1	FCCU2 high
	Reset condition	Real time information
FCCU1_RT	Description	Report the real state of the FCCU1 status
	0	FCCU1 low
	1	FCCU1 high
	Reset condition	Real time information
STBY_WAKE_UP	Description	Indicate startup from Standby mode
	0	Cold wake up
	1	Standby wake up
	Reset condition	POR / Clear on Write (write ‘1’)
TIMING_WINDOW_ STBY_FLG	Description	Report a bad timing window for standby entry
	0	No Error
	1	Error
	Reset condition	POR / Clear on Write (write ‘1’)
FS_REG_OVUV_G	Description	Report an error in one of the voltage monitor
	0	No Failure
	1	Failure
	Reset condition	POR
FS_IO_G	Description	Report an error in one of the Failsafe I/Os (FS_IO_G = PGOOD_DIAG or RSTB_DIAG or FS0B_DIAG)
	0	No Failure
	1	Failure
	Reset condition	POR
FS_WD_G	Description	Report an error on watchdog refresh
	0	Good WD refresh
	1	Bad WD refresh
	Reset condition	POR
FS_COM_G	Description	Report an error on the I2C Communication
	0	No Failure
	1	Failure

Table 102. FS_GRL_FLAGS register description...*continued*

	Reset condition	POR

26.2 FS_I_OVUV_SAFE_REACTION1 register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	0	0	0	0	**VCOREMON_OV_ FS_IMPACT [1:0]**		**VCOREMON_UV_ FS_IMPACT [1:0]**	
Read	RESERVED	RESERVED	RESERVED	RESERVED	**VCOREMON_OV_ FS_IMPACT [1:0]**		**VCOREMON_UV_ FS_IMPACT [1:0]**	
Reset	0	0	0	0	1	0	0	1

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
HVLDO_VMON_OV_ FS_IMPACT [1:0]		**HVLDO_VMON_UV_ FS_IMPACT [1:0]**		**VDDIO_OV_ FS_IMPACT [1:0]**		**VDDIO_UV _FS_IMPACT [1:0]**	
HVLDO_VMON_OV_ FS_IMPACT [1:0]		**HVLDO_VMON_UV_ FS_IMPACT [1:0]**		**VDDIO_OV_ FS_IMPACT [1:0]**		**VDDIO_UV _FS_IMPACT [1:0]**	
1	0	0	1	1	0	0	1

Table 103. FS_I_OVUV_SAFE_REACTION1 register description

VDDIO_UV _FS_IMPACT [1:0]	Description	Reaction on RSTB or FS0B output in case of UV detection on VDDIO
	00	No effect on RSTB and FS0B
	01	VDDIO UV asserts FS0B only
	10	VDDIO UV asserts RSTB and FS0B
	11	VDDIO UV asserts RSTB and FS0B
	Reset condition	POR
VDDIO_OV_ FS_IMPACT [1:0]	Description	Reaction on RSTB or FS0B output in case of OV detection on VDDIO
	00	No effect on RSTB and FS0B
	01	VDDIO OV asserts FS0B only
	10	VDDIO OV asserts RSTB and FS0B
	11	VDDIO OV asserts RSTB and FS0B
	Reset condition	POR
HVLDO_VMON_UV_ FS_IMPACT [1:0]	Description	Reaction on RSTB or FS0B output in case of UV detection on HVLDO
	00	No effect on RSTB and FS0B
	01	HVLDO UV asserts FS0B only
	10	HVLDO UV asserts RSTB and FS0B

Table 103. FS_I_OVUV_SAFE_REACTION1 register description...*continued*

	11	HVLDO UV asserts RSTB and FS0B
	Reset condition	POR
HVLDO_VMON_OV_ FS_IMPACT [1:0]	Description	Reaction on RSTB or FS0B output in case of OV detection on HVLDO
	00	No effect on RSTB and FS0B
	01	HVLDO OV asserts FS0B only
	10	HVLDO OV asserts RSTB and FS0B
	11	HVLDO OV asserts RSTB and FS0B
	Reset condition	POR
VCOREMON_UV_ FS_IMPACT [1:0]	Description	Reaction on RSTB or FS0B output in case of UV detection on VCOREMON
	00	No effect on RSTB and FS0B
	01	VCOREMON UV asserts FS0B only
	10	VCOREMON UV asserts RSTB and FS0B
	11	VCOREMON UV asserts RSTB and FS0B
	Reset condition	POR
VCOREMON_OV_ FS_IMPACT [1:0]	Description	Reaction on RSTB or FS0B output in case of OV detection on VCOREMON
	00	No effect on RSTB and FS0B
	01	VCOREMON OV asserts FS0B only
	10	VCOREMON OV asserts RSTB and FS0B
	11	VCOREMON OV asserts RSTB and FS0B
	Reset condition	POR

26.3 FS_I_OVUV_SAFE_REACTION2 register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	**VMON4_OV_FS_ IMPACT [1:0]**		**VMON4_UV_FS_ IMPACT [1:0]**		**VMON3_OV_ FS_IMPACT[1:0]**		**VMON3_UV_FS_ IMPACT [1:0]**	
Read	**VMON4_OV_FS_ IMPACT [1:0]**		**VMON4_UV_FS_ IMPACT [1:0]**		**VMON3_OV_ FS_IMPACT[1:0]**		**VMON3_UV_FS_ IMPACT [1:0]**	
Reset	1	0	0	1	1	0	0	1

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
VMON2_OV_FS_ IMPACT [1:0]		**VMON2_UV_FS_ IMPACT [1:0]**		**VMON1_OV_FS_ IMPACT [1:0]**		**VMON1_UV_FS_ IMPACT [1:0]**	
VMON2_OV_FS_ IMPACT [1:0]		**VMON2_UV_FS_ IMPACT [1:0]**		**VMON1_OV_FS_ IMPACT [1:0]**		**VMON1_UV_FS_ IMPACT [1:0]**	

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
1	0	0	1	1	0	0	1

Table 104. FS_I_OVUV_SAFE_REACTION2 register description

VMON1_UV_ FS_IMPACT [1:0]	Description	Reaction on RSTB or FS0B output in case of UV detection on VMON1
	00	No effect on RSTB and FS0B
	01	VMON1 UV asserts FS0B only
	10	VMON1 UV asserts RSTB and FS0B
	11	VMON1 UV asserts RSTB and FS0B
	Reset condition	POR
VMON1_OV_ FS_IMPACT [1:0]	Description	Reaction on RSTB or FS0B output in case of OV detection on VMON1
	00	No effect on RSTB and FS0B
	01	VMON1 OV asserts FS0B only
	10	VMON1 OV asserts RSTB and FS0B
	11	VMON1 OV asserts RSTB and FS0B
	Reset condition	POR
VMON2_UV_ FS_IMPACT [1:0]	Description	Reaction on RSTB or FS0B output in case of UV detection on VMON2
	00	No effect on RSTB and FS0B
	01	VMON2 UV asserts FS0B only
	10	VMON2 UV asserts RSTB and FS0B
	11	VMON2 UV asserts RSTB and FS0B
	Reset condition	POR
VMON2_OV_ FS_IMPACT [1:0]	Description	Reaction on RSTB or FS0B output in case of OV detection on VMON2
	00	No effect on RSTB and FS0B
	01	VMON2 OV asserts FS0B only
	10	VMON2 OV asserts RSTB and FS0B
	11	VMON2 OV asserts RSTB and FS0B
	Reset condition	POR
VMON3_UV_ FS_IMPACT [1:0]	Description	Reaction on RSTB or FS0B output in case of UV detection on VMON3
	00	No effect on RSTB and FS0B
	01	VMON3 UV asserts FS0B only
	10	VMON3 UV asserts RSTB and FS0B
	11	VMON3 UV asserts RSTB and FS0B
	Reset condition	POR

Table 104. FS_I_OVUV_SAFE_REACTION2 register description*...continued*

VMON3_OV_ FS_IMPACT [1:0]	Description	Reaction on RSTB or FS0B output in case of OV detection on VMON3
	00	No effect on RSTB and FS0B
	01	VMON3 OV asserts FS0B only
	10	VMON3 OV asserts RSTB and FS0B
	11	VMON3 OV asserts RSTB and FS0B
	Reset condition	POR
VMON4_UV_ FS_IMPACT [1:0]	Description	Reaction on RSTB or FS0B output in case of UV detection on VMON4
	00	No effect on RSTB and FS0B
	01	VMON4 UV asserts FS0B only
	10	VMON4 UV asserts RSTB and FS0B
	11	VMON4 UV asserts RSTB and FS0B
	Reset condition	POR
VMON4_OV_ FS_IMPACT [1:0]	Description	Reaction on RSTB or FS0B output in case of OV detection on VMON4
	00	No effect on RSTB and FS0B
	01	VMON4 OV asserts FS0B only
	10	VMON4 OV asserts RSTB and FS0B
	11	VMON4 OV asserts RSTB and FS0B
	Reset condition	POR

26.4 FS_I_ABIST2_CTRL register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
0	**VMON4_ ABIST2**	**VMON3_ ABIST2**	**VMON2_ ABIST2**	**VMON1_ ABIST2**	**HVLDO_ VMON_ ABIST2**	**VCORE_ ABIST2**	**VDDIO_ ABIST2**
RESERVED	**VMON4_ ABIST2**	**VMON3_ ABIST2**	**VMON2_ ABIST2**	**VMON1_ ABIST2**	**HVLDO_ VMON_ ABIST2**	**VCORE_ ABIST2**	**VDDIO_ ABIST2**
0	0	0	0	0	0	0	0

Table 105. FS_I_ABIST2_CTRL register description

VDDIO_ABIST2	Description	VDDIO ABIST2 configuration
	0	No ABIST
	1	Run ABIST on VDDIO after INIT
	Reset condition	POR
VCORE_ABIST2	Description	VCORE ABIST2 configuration
	0	No ABIST
	1	Run ABIST on VCOREMON after INIT
	Reset condition	POR
HVLDO_VMON_ABIST2	Description	HVLDO ABIST2 configuration
	0	No ABIST
	1	Run ABIST on HVLDO after INIT
	Reset condition	POR
VMON1_ABIST2	Description	VMON1 ABIST2 configuration
	0	No ABIST
	1	Run ABIST on VMON1 after INIT
	Reset condition	POR
VMON2_ABIST2	Description	VMON2 ABIST2 configuration
	0	No ABIST
	1	Run ABIST on VMON2 after INIT
	Reset condition	POR
VMON3_ABIST2	Description	VMON3 ABIST2 configuration
	0	No ABIST
	1	Run ABIST on VMON3 after INIT
	Reset condition	POR
VMON4_ABIST2	Description	VMON4 ABIST2 configuration
	0	No ABIST
	1	Run ABIST on VMON4 after INIT
	Reset condition	POR

26.5 FS_I_WD_CFG register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	**WD_ERR_LIMIT[1:0]**		0	**WD_RFR_LIMIT[1:0]**		0	**WD_FS_IMPACT[1:0]**	
Read	**WD_ERR_LIMIT[1:0]**		RESERVED	**WD_RFR_LIMIT[1:0]**		RESERVED	**WD_FS_IMPACT[1:0]**	
Reset	0	1	0	0	0	0	1	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
0	WD_RFR_CNT[2:0]			WD_ERR_CNT[3:0]			
RESERVED	WD_RFR_CNT[2:0]			WD_ERR_CNT[3:0]			
0	0	0	0	0	0	0	0

Table 106. FS_I_WD_CFG register description

WD_ERR_LIMIT[1:0]	Refer to Table 47	
WD_RFR_LIMIT[1:0]	Refer to Table 39	
WD_FS_IMPACT[1:0]	Refer to Table 40	
WD_RFR_CNT[2:0]	Description	Reflect the value of the Watchdog Refresh Counter
	000	0
	001	1
	010	2
	011	3
	100	4
	101	5
	110	6
	111	7
	Reset condition	POR
WD_ERR_CNT[3:0]	Description	Reflect the value of the Watchdog Error Counter
	0000	0
	0001	1
	0010	2
	0011	3
	0100	4
	0101	5
	0110	6
	0111	7
	1000	8
	Reset condition	POR

26.6 FS_I_SAFE_INPUTS register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	**FCCU_CFG[1:0]**		0	**FCCU12_ FLT_POL**	**FCCU1_ FLT_POL**	**FCCU2_ FLT_POL**	0	**FCCU12_ FS_ IMPACT**

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Read	FCCU_CFG[1:0]		RESERVED	FCCU12_ FLT_POL	FCCU1_ FLT_POL	FCCU2_ FLT_POL	RESERVED	FCCU12_ FS_ IMPACT
Reset	0	1	0	0	0	0	0	1

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
FCCU1_ FS_IMPACT	FCCU2_ FS_IMPACT	0	0	TIMING_WINDOW_STBY[3:0]			
FCCU1_ FS_IMPACT	FCCU2_ FS_IMPACT	RESERVED	RESERVED	TIMING_WINDOW_STBY[3:0]			
1	1	0	0	1	0	1	0

Table 107. FS_I_SAFE_INPUTS register description

TIMING_WINDOW_STBY[3:0]	Refer to Table 74
FCCU2_FS_IMPACT	Refer to Table 55
FCCU1_FS_IMPACT	Refer to Table 55
FCCU12_FS_IMPACT	Refer to Table 53
FCCU2_FLT_POL	Refer to Table 54
FCCU1_FLT_POL	Refer to Table 54
FCCU12_FLT_POL	Refer to Table 52
FCCU_CFG[1:0]	Refer to Table 51

26.7 FS_I_FSSM register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	FLT_ERR_ CNT_LIMIT[1:0]		0	FLT_ERR_IMPACT[1:0]		0	RSTB_DUR	0
Read	FLT_ERR_ CNT_LIMIT[1:0]		RESERVED	FLT_ERR_IMPACT[1:0]		RESERVED	RSTB_DUR	RESERVED
Reset	0	1	0	1	0	0	0	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
BACKUP_ SAFETY_ PATH	LPCLK_ MON_DIS	CLK_ MON_DIS	DIS8S	0			
BACKUP_ SAFETY_ PATH	LPCLK_ MON_DIS	CLK_ MON_DIS	DIS8S	FLT_ERR_CNT[3:0]			

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
1	0	0	0	0	0	0	1

Table 108. FS_I_FSSM register description

RSTB_DUR	Description	RSTB pulse duration configuration
	0	10 ms
	1	1 ms
	Reset condition	POR
BACKUP_SAFETY_PATH	Description	Assert RSTB in case of a short to high detected on FS0B
	0	RSTB is not asserted
	1	RSTB is asserted
	Reset condition	POR
CLK_MON_DIS	Description	Disable Clock Monitoring
	0	Clock Monitoring enabled
	1	Clock Monitoring disabled
	Reset condition	POR
LPCLK_MON_DIS	Description	Disable Low Power Clock Monitoring
	0	Low Power Clock Monitoring enabled
	1	Low Power Clock Monitoring disabled
	Reset condition	POR
DIS8S	Description	Disable 8S timer
	0	RSTB low 8s counter enabled
	1	RSTB low 8s counter disabled
	Reset condition	POR
FLT_ERR_CNT[3:0]	Description	Reflect the value of the Fault Error Counter
	0000	0
	0001	1
	0010	2
	0011	3
	0100	4
	0101	5
	0110	6
	0111	7
	1000	8
	1001	9
	1010	10
	1011	11

Table 108. FS_I_FSSM register description...*continued*

	1100	12
	Reset condition	POR
FLT_ERR_IMPACT[1:0]	Refer to **Table 55**	
FLT_ERR_CNT_LIMIT[1:0]	Refer to **Table 54**	

26.8 FS_I_SVS register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	**SVS_OFFSET[5:0]**						**SVS_ OFFSET_ SIGN**	0
Read	**SVS_OFFSET[5:0]**						**SVS_ OFFSET_ SIGN**	RESERVED
Reset	0	0	0	0	0	0	0	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
0	0	0	0	0	0	0	0
RESERVED	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**
0	0	0	0	0	0	0	0

Table 109. FS_I_SVS register description

	Description	Static Voltage Scaling offset (mV)
SVS_OFFSET[5:0]	0000000	0
	0000001	6.25
	0000010	12.50
	0000011	18.75
	0000100	25
	0000101	31.25
	0000110	37.5
	0000111	43.75
	0001000	50
	0001001	56.25
	0001010	62.5
	0001011	68.75
	0001100	75
	0001101	81.25

Table 109. FS_I_SVS register description...*continued*

	0001110	87.5
	0001111	93.75
	0010000	100
	0010001	106.25
	0010010	112.5
	0010011	118.75
	0010100	125
	0010101	131.25
	0010110	137.5
	0010111	143.75
	0011000	150
	0011001	156.25
	0011010	162.5
	0011011	168.75
	0011100	175
	0011101	181.25
	0011110	187.5
	0011111	193.75
	0100000	200
	0100001	206.25
	0100010	212.5
	0100011	218.75
	0100100	225
	0100101	231.25
	0100110	237.5
	0100111	243.75
	0101000	250
	0101001	256.25
	0101010	262.5
	0101011	268.75
	0101100	275
	0101101	281.25
	0101110	287.5
	0101111	293.75
	0110000	300
	0110001	306.25
	0110010	312.5

Table 109. FS_I_SVS register description...*continued*

	0110011	318.75
	0110100	325
	0110101	331.25
	0110110	337.5
	0110111	343.75
	0111000	350
	0111001	356.25
	0111010	362.5
	0111011	368.75
	0111100	375
	0111101	381.25
	0111110	387.5
	0111111	393.75
	Reset condition	POR
SVS_OFFSET_SIGN	Description	SVS offset negative or positive
	0	Negative offset
	1	Positive offset
	Reset condition	POR

26.9 FS_WD_WINDOW register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	**WD_WINDOW[3:0]**				0	**WDW_DC[2:0]**		
Read	**WD_WINDOW[3:0]**				RESERVED	**WDW_DC[2:0]**		
Reset	0	0	1	1	0	0	1	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
0	0	0	0	**WDW_RECOVERY[3:0]**			
RESERVED	RESERVED	RESERVED	RESERVED	**WDW_RECOVERY[3:0]**			
0	0	0	0	1	0	1	1

Table 110. FS_WD_WINDOW register description

WD_WINDOW[3:0]	Refer to Table 45
WDW_DC[2:0]	Refer to Table 46
WDW_RECOVERY[3:0]	Refer to Table 50

26.10 FS_WD_SEED register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	WD_SEED[15:0]							
Read	WD_SEED[15:0]							
Reset	0	1	0	1	1	0	1	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
WD_SEED[15:0]							
WD_SEED[15:0]							
1	0	1	1	1	0	1	0

Table 111. FS_WD_SEED register description

WD_SEED [15:0]	Description	Watchdog LFSR value
	0…	0x5AB2 default value at startup
	…1	
	Reset condition	POR

26.11 FS_WD_ANSWER register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	WD_ANSWER[15:0]							
Read	WD_ANSWER[15:0]							
Reset	0	0	0	0	0	0	0	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
WD_ANSWER[15:0]							
WD_ANSWER[15:0]							
0	0	0	0	0	0	0	0

Table 112. FS_WD_ANSWER register description

WD_ANSWER [15:0]	Description	Watchdog answer value from the MCU
	0…	Challenger WD Answer = (NOT(((LFSR x 4)+6)–4))/4 (refer to Section 22.4.2 "Challenger watchdog") Simple WD Answer = 0x5AB2 (refer to Section 22.4.1 "Simple watchdog")
	…1	

Table 112. FS_WD_ANSWER register description*...continued*

	Reset condition	POR

26.12 FS_OVUVREG_STATUS register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	**VCORE MON_OV**	**VCORE MON_UV**	**VDDIO_OV**	**VDDIO_UV**	**VMON4_ OV**	**VMON4_UV**	**VMON3_ OV**	**VMON3_UV**
Read	**VCORE MON_OV**	**VCORE MON_UV**	**VDDIO_OV**	**VDDIO_UV**	**VMON4_ OV**	**VMON4_UV**	**VMON3_ OV**	**VMON3_UV**
Reset	0	0	0	0	0	0	0	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
VMON2_OV	**VMON2_UV**	**VMON1_OV**	**VMON1_UV**	**HVLDO_ VMON_OV**	**HVLDO_ VMON_UV**	**FS_ DIGREF_OV**	**FS_OSC_ DRIFT**
VMON2_OV	**VMON2_UV**	**VMON1_OV**	**VMON1_UV**	**HVLDO_ VMON_OV**	**HVLDO_ VMON_UV**	**FS_ DIGREF_OV**	**FS_OSC_ DRIFT**
0	0	0	0	0	0	0	0

Table 113. FS_OVUVREG_STATUS register description

VCOREMON_OV	Description	Overvoltage Monitoring on VCOREMON
	0	No Overvoltage
	1	Overvoltage Reported on VCOREMON
	Reset condition	POR / Clear on Write (write ‘1’)
VCOREMON_UV	Description	Undervoltage Monitoring on VCOREMON
	0	No Undervoltage
	1	Undervoltage Reported on VCOREMON
	Reset condition	POR / Clear on Write (write ‘1’)
VDDIO_OV	Description	Overvoltage Monitoring on VDDIO
	0	No Overvoltage
	1	Overvoltage Reported on VDDIO
	Reset condition	POR / Clear on Write (write ‘1’)
VDDIO_UV	Description	Undervoltage Monitoring on VDDIO
	0	No Undervoltage
	1	Undervoltage Reported on VDDIO
	Reset condition	POR / Clear on Write (write ‘1’)
VMON4_OV	Description	Overvoltage Monitoring on VMON4
	0	No Overvoltage

Table 113. FS_OVUVREG_STATUS register description*...continued*

	1	Overvoltage Reported on VMON4
	Reset condition	POR / Clear on Write (write '1')
VMON4_UV	Description	Undervoltage Monitoring on VMON4
	0	No Undervoltage
	1	Undervoltage Reported on VMON4
	Reset condition	POR / Clear on Write (write '1')
VMON3_OV	Description	Overvoltage Monitoring on VMON3
	0	No Overvoltage
	1	Overvoltage Reported on VMON3
	Reset condition	POR / Clear on Write (write '1')
VMON3_UV	Description	Undervoltage Monitoring on VMON3
	0	No Undervoltage
	1	Undervoltage Reported on VMON3
	Reset condition	POR / Clear on Write (write '1')
VMON2_OV	Description	Overvoltage Monitoring on VMON2
	0	No Overvoltage
	1	Overvoltage Reported on VMON2
	Reset condition	POR / Clear on Write (write '1')
VMON2_UV	Description	Undervoltage Monitoring on VMON2
	0	No Undervoltage
	1	Undervoltage Reported on VMON2
	Reset condition	POR / Clear on Write (write '1')
VMON1_OV	Description	Overvoltage Monitoring on VMON1
	0	No Overvoltage
	1	Overvoltage Reported on VMON1
	Reset condition	POR / Clear on Write (write '1')
VMON1_UV	Description	Undervoltage Monitoring on VMON1
	0	No Undervoltage
	1	Undervoltage Reported on VMON1
	Reset condition	POR / Clear on Write (write '1')
HVLDO_VMON_OV	Description	Overvoltage Monitoring on HVLDO
	0	No Overvoltage
	1	Overvoltage Reported on HVLDO VMON
	Reset condition	POR / Clear on Write (write '1')
HVLDO_VMON_UV	Description	Undervoltage Monitoring on HVLDO
	0	No Undervoltage
	1	Undervoltage Reported on HVLDO VMON

Table 113. FS_OVUVREG_STATUS register description*...continued*

	Reset condition	POR / Clear on Write (write '1')
FS_DIG_REF_OV	Description	Overvoltage of the Internal Digital Fail Safe reference voltage
	0	No overvoltage
	1	Overvoltage reported of the internal digital fail safe reference voltage
	Reset condition	POR / Clear on Write (write '1')
FS_OSC_DRIFT	Description	Drift of the Fail Safe OSC
	0	No Drift
	1	Oscillator Drift
	Reset condition	POR / Clear on Write (write '1')

26.13 FS_RELEASE_FS0B register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	**FS_RELEASE_FS0B[15:0]**							
Read	**FS_RELEASE_FS0B[15:0]**							
Reset	0	0	0	0	0	0	0	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
FS_RELEASE_FS0B[15:0]							
FS_RELEASE_FS0B[15:0]							
0	0	0	0	0	0	0	0

Table 114. FS_RELEASE_FS0B register description

RELEASE_ FS0B [15:0]	Description	Secure 16bits word to release FS0B
	0…	Depend on WD_SEED value and calculation
	…1	
	Reset condition	POR

26.14 FS_SAFE_IOS register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	**PGOOD_ DIAG**	**PGOOD_ EVENT**	**0**	**EXT_RSTB**	**0**	**0**	**RSTB_ EVENT**	**RSTB_ DIAG**
Read	**PGOOD_ DIAG**	**PGOOD_ EVENT**	**PGOOD_ SNS**	**EXT_RSTB**	**RSTB_DRV**	**RSTB_SNS**	**RSTB_ EVENT**	**RSTB_ DIAG**
Reset	0	0	0	0	0	0	0	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
RSTB_REQ	**0**	**0**	**FS0B_DIAG**	**FS0B_REQ**	**GO_TO_ INITFS**	**STBY_REQ**	0
Reserved	**FS0B_DRV**	**FS0B_SNS**	**FS0B_DIAG**	**Reserved**	**Reserved**	**Reserved**	RESERVED
0	0	0	0	0	0	0	0

Table 115. FS_SAFE_IOS register description

FS0B_REQ	Description	Request assertion of FS0B
	0	No Assertion
	1	FS0B Assertion
	Reset condition	POR
FS0B_DIAG	Description	Report a Failure on FS0B
	0	No Failure
	1	Short Circuit High
	Reset condition	POR / Clear on Write (write ‘1’)
FS0B_SNS	Description	Sense of FS0B pad
	0	FS0B pad sensed low
	1	FS0B pad sensed high
	Reset condition	Real time information
FS0B_DRV	Description	FS0B driver – digital command
	0	FS0B driver command sensed low
	1	FS0B driver command sensed high
	Reset condition	Real time information
RSTB_REQ	Description	Request assertion of RSTB (Pulse)
	0	No Assertion
	1	RSTB Assertion (Pulse)
	Reset condition	POR
EXT_RSTB	Description	Report an External RESET
	0	No External RESET
	1	External RESET
	Reset condition	POR / Clear on Write (write ‘1’)
RSTB_DIAG	Description	Report a RSTB Short to High
	0	No Failure
	1	Short Circuit High
	Reset condition	POR / Clear on Write (write ‘1’)
RSTB_EVENT	Description	Report a RSTB event
	0	No RESET
	1	RESET occurred

Table 115. FS_SAFE_IOS register description*...continued*

	Reset condition	POR / Clear on Write (write '1')
RSTB_SNS	Description	Sense of RSTB pad
	0	RSTB pad sensed low
	1	RSTB pad sensed high
	Reset condition	Real time information
RSTB_DRV	Description	RSTB driver – digital command
	0	RSTB driver command sensed low
	1	RSTB driver command sensed high
	Reset condition	Real time information
PGOOD_DIAG	Description	Report a PGOOD Short to High
	0	No Failure
	1	Short-Circuit HIGH
	Reset condition	POR / Clear on Write (write '1')
PGOOD_EVENT	Description	Report a Power GOOD event
	0	No Power GOOD
	1	Power Good event occurred
	Reset condition	POR / Clear on Write (write '1')
PGOOD_SNS	Description	Sense of PGOOD pad
	0	PGOOD pad sensed low
	1	PGOOD pad sensed high
	Reset condition	Real time information
STBY_REQ	Description	Standby request from the MCU
	0	No Standby request
	1	Standby request from the MCU
	Reset condition	0
GOTO_INITFS	Description	Go back to INIT Fail Safe request
	0	No action
	1	Go back to INIT_FS
	Reset condition	POR

26.15 FS_DIAG_SAFETY register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	**FCCU12**	**FCCU1**	**FCCU2**	**BAD_ WD_DATA**	**BAD_WD_ TIMING**	**0**	**0**	**LPCLK_ FREQ2HIGH**
Read	**FCCU12**	**FCCU1**	**FCCU2**	**BAD_ WD_DATA**	**BAD_WD_ TIMING**	**ABIST1_ OK**	**ABIST2_ OK**	**LPCLK_ FREQ2HIGH**

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Reset	0	0	0	0	0	0	0	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
LPCLK_ FREQ2LOW	**I2C_FS_CRC**	**I2C_FS_REQ**	**0**	**0**	**0**	0	0
LPCLK_ FREQ2LOW	**I2C_FS_CRC**	**I2C_FS_REQ**	**LBIST_ BYPASSED**	**LBIST_ DONE**	**LBIST_PASS**	RESERVED	RESERVED
0	0	0	0	0	0	0	0

Table 116. FS_DIAG_SAFETY register description

FCCU12	Description	Report an error in the FCCU12 input
	0	No error
	1	Error detected
	Reset condition	POR / Clear on Write (write ‘1’)
FCCU1	Description	Report an error in the FCCU1 input
	0	No error
	1	Error detected
	Reset condition	POR / Clear on Write (write ‘1’)
FCCU2	Description	Report an error in the FCCU2 input
	0	No error
	1	Error detected
	Reset condition	POR / Clear on Write (write ‘1’)
BAD_WD_DATA	Description	WD Refresh status - Data
	0	Good WD Refresh
	1	Bad WD refresh, error in the DATA
	Reset condition	POR / Clear on Write (write ‘1’)
BAD_WD_TIMING	Description	WD refresh status - Timing
	0	Good WD Refresh
	1	Bad WD refresh, wrong window or in timeout
	Reset condition	POR / Clear on Write (write ‘1’)
ABIST1_OK	Description	Diagnostic of Analog BIST1
	0	ABIST1 FAIL
	1	ABIST1 PASS
	Reset condition	Real time information
ABIST2_OK	Description	Diagnostic of Analog BIST2
	0	ABIST2 FAIL or NOT EXECUTED

Table 116. FS_DIAG_SAFETY register description...*continued*

	1	ABIST2 PASS
	Reset condition	Real time information
LPCLK_FREQ2HIGH	Description	Report an error in the Low Power Clock Frequency
	0	No error
	1	Error detected, Frequency too high
	Reset condition	POR / Clear on Write (write '1')
LPCLK_FREQ2LOW	Description	Report an error in the Low Power Clock Frequency
	0	No error
	1	Error detected, Frequency too low
	Reset condition	POR / Clear on Write (write '1')
I2C_FS_CRC	Description	Fail Safe I2C communication CRC issue
	0	No error
	1	Error detected in the CRC
	Reset condition	POR / Clear on Write (write '1')
I2C_FS_REQ	Description	Invalid Fail Safe I2C access (Wrong Write or Read, Write to INIT registers in normal mode, wrong address)
	0	No error
	1	I2C Violation
	Reset condition	POR / Clear on Write (write '1')
LBIST_BYPASSED	Description	Diagnostic of Logical BIST
	0	LBIST not bypassed
	1	LBIST bypassed
	Reset condition	Real time information
LBIST_DONE	Description	Diagnostic of Logical BIST
	0	LBIST did not run
	1	LBIST ran
	Reset condition	Real time information
LBIST_PASS	Description	Diagnostic of Logical BIST
	0	LBIST FAIL or did not run
	1	LBIST PASS
	Reset condition	Real time information

26.16 FS_INTB_MASK register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	0	0	0	0	0	0	**INT_INH_VMON4_OV_UV**	**INT_INH_VMON3_OV_UV**

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	**INT_INH_VMON4_OV_UV**	**INT_INH_VMON3_OV_UV**
Reset	0	0	0	0	0	0	0	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
INT_INH_VMON2_OV_UV	**INT_INH_VMON1_OV_UV**	**INT_INH_VDDIO_OV_UV**	**INT_INH_VCOREMON_OV_UV**	**INT_INH_BAD_WD_REFRESH**	**INT_INH_HVLDO_VMON_OV_UV**	**INT_INH_FCCU2**	**INT_INH_FCCU1**
INT_INH_VMON2_OV_UV	**INT_INH_VMON1_OV_UV**	**INT_INH_VDDIO_OV_UV**	**INT_INH_VCOREMON_OV_UV**	**INT_INH_BAD_WD_REFRESH**	**INT_INH_HVLDO_VMON_OV_UV**	**INT_INH_FCCU2**	**INT_INH_FCCU1**
0	0	0	0	0	0	0	0

Table 117. FS_INTB_MASK register description

INT_INH_FCCU1	Description	Inhibit INTERRUPT on FCCU1 event
	0	Interruption NOT MASKED
	1	Interruption MASKED
	Reset condition	POR
INT_INH_FCCU2	Description	Inhibit INTERRUPT on FCCU2 event
	0	Interruption NOT MASKED
	1	Interruption MASKED
	Reset condition	POR
INT_INH_HVLDO_VMON_OV_UV	Description	Inhibit INTERRUPT on HVLDO VMON OV and UV event
	0	Interruption NOT MASKED
	1	Interruption MASKED
	Reset condition	POR
INT_INH_BAD_WD_REFRESH	Description	Inhibit INTERRUPT on bad WD refresh event
	0	Interruption NOT MASKED
	1	Interruption MASKED
	Reset condition	POR
INT_INH_VCOREMON_OV_UV	Description	Inhibit INTERRUPT on VCOREMON OV and UV event
	0	Interruption NOT MASKED
	1	Interruption MASKED
	Reset condition	POR
INT_INH_VDDIO_OV_UV	Description	Inhibit INTERRUPT on VDDIO OV and UV event

Table 117. FS_INTB_MASK register description...*continued*

	0	Interruption NOT MASKED
	1	Interruption MASKED
	Reset condition	POR
INT_INH_VMON1_OV_UV	Description	Inhibit INTERRUPT on VMON1 OV and UV event
	0	Interruption NOT MASKED
	1	Interruption MASKED
	Reset condition	POR
INT_INH_VMON2_OV_UV	Description	Inhibit INTERRUPT on VMON2 OV and UV event
	0	Interruption NOT MASKED
	1	Interruption MASKED
	Reset condition	POR
INT_INH_VMON3_OV_UV	Description	Inhibit INTERRUPT on VMON3 OV and UV event
	0	Interruption NOT MASKED
	1	Interruption MASKED
	Reset condition	POR
INT_INH_VMON4_OV_UV	Description	Inhibit INTERRUPT on VMON4 OV and UV event
	0	Interruption NOT MASKED
	1	Interruption MASKED
	Reset condition	POR

26.17 FS_STATES register

Return to Register Map

Bits	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
Write	0	**DBG_EXIT**	**0**	0	**OTP_ CORRUPT**	0	**REG_ CORRUPT**	0
Read	RESERVED	**Reserved**	**DBG_ MODE**	RESERVED	**OTP_ CORRUPT**	RESERVED	**REG_ CORRUPT**	RESERVED
Reset	0	0	0	0	0	0	0	0

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
0	0	0	**0**				
RESERVED	RESERVED	RESERVED	**FSM_STATES[4:0]**				
0	0	0	0	0	0	0	0

Table 118. FS_STATES register description

DBG_EXIT	Description	Leave DEBUG mode
	0	No action
	1	Leave DEBUG mode
	Reset condition	POR
DBG_MODE	Description	DEBUG mode status
	0	NOT in DEBUG mode
	1	In DEBUG mode
	Reset condition	Real time information
OTP_CORRUPT	Description	OTP bits corruption detection (5ms cyclic check)
	0	No error
	1	OTP CRC error detected
	Reset condition	POR / Clear on Write (write ‘1’)
REG_CORRUPT	Description	INIT register corruption detection (real time comparison)
	0	No error
	1	INIT register content error detected (mismatch between FS_I_Register / FS_I_NOT_Register)
	Reset condition	POR / Clear on Write (write ‘1’)
FSM_STATE[4:0]	Description	Report Fail-safe state machine current state
	00110	INIT_FS
	00111	WAIT_ABIST2
	01000	ABIST2
	01001	ASSERT_FS0B
	01010	NORMAL _FS
	Reset condition	Real time information

27 OTP Bits Configuration

27.1 Main OTP map overview

Table 119. Main OTP map overview

Addr.	Register Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
18	CFG_ VPRE_ 1_OTP	0	0	VPREV_OTP[5:0]					
19	CFG_ VPRE_ 2_OTP	VPREDIS_ OTP	VPREV_ STBY_ EN_OTP	VPRESC_OTP[5:0]					
1A	CFG_ VPRE_ 3_OTP	VPREILIM_OTP[1:0]		VPRETOFF_OTP[1:0]		VPRESRLS_OTP[1:0]		VPRESRHS_ OTP[1:0]	

Table 119. Main OTP map overview*...continued*

Addr.	Register Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
1B	CFG_ BOOST_ 1_OTP	0	PSYNC_ PGOOD_ EXT_OTP	EXT_ STBY_ DISCH_ OTP	VBOS_ VBOOST_ OTP	VBSTV_OTP[3:0]			
1C	CFG_ BOOST_ 2_OTP	BOOSTEN_ OTP	VBSTTONTIME_OTP[1:0]		VBSTSC_OTP[4:0]				
1D	CFG_ BOOST_ 3_OTP	VBSTRCOMP_OTP[1:0]		VBSTCCOMP_ OTP[1:0]		VBSTILIM_OTP[1:0]		VBSTSR_OTP[1:0]	
1E	CFG_ BUCK1_ 1_OTP	BUCK1V_OTP[7:0]							
1F	CFG_ BUCK1_ 2_OTP	PSYNC_ PWRDWN_ EN_OTP	PWRON2_ GATE_ EN_OTP	STBY_ PGOOD_ DLY_OTP	BUCK1_LSELECT_ OTP[1:0]		BUCK1_ILIM_ OTP[1:0]		VB12MUL TIPH_ OTP
20	CFG_ BUCK2_ 1_OTP	BUCK2V_OTP[7:0]							
21	CFG_ BUCK2_ 2_OTP	AMUX_ FOUT	BUCK2_LSELECT_ OTP[1:0]		BUCK2EN_ OTP	BUCK2_ILIM_ OTP[1:0]		BUCK3_ RC_OTP	BUCK3_ GM_OTP
22	CFG_ BUCK3_ 1_OTP	BUCK3EN_ OTP	BUCK3_LSELECT_ OTP[1:0]		BUCK3V_OTP[4:0]				
23	CFG_ BUCK3_ 2_OTP	BUCK2_COMP_OTP[2:0]			BUCK1_COMP_OTP[2:0]			BUCK3_ILIM_ OTP[1:0]	
24	CFG_ LDO_ ALL1_OTP	LDO3V_OTP[3:0]				HVLDOEN_ OTP	LDO3EN_ OTP	LDO2EN_ OTP	LDO1EN_ OTP
25	CFG_ LDO_ ALL2_OTP	LDO2V_OTP[3:0]				LDO1ILIM_ OTP	LDO1V_OTP[2:0]		
26	CFG_ SEQ_ 1_OTP	LDO3_ LS_OTP	LDO2_ LS_OTP	BUCK3S_OTP[2:0]			BUCK2S_OTP[2:0]		
27	CFG_ SEQ_ 2_OTP	HVLDOV_OTP[1:0]		BUCK1S_OTP[2:0]			LDO3S_OTP[2:0]		
28	CFG_ SEQ_ 3_OTP	SLOT_WIDTH_OTP[1:0]		LDO2S_OTP[2:0]			LDO1S_OTP[2:0]		
29	CFG_ SEQ_ 4_OTP	HVLDO_ TRANS_ MODE_OTP	HVLDO_ SLOT_ EN_OTP	HVLDOS_OTP[2:0]			BOOSTS_OTP[2:0]		

Table 119. Main OTP map overview*...continued*

Addr.	Register Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
2A	CFG_CLOCK_1_OTP	VPRE_PFM_TON_OTP[1:0]		VPRE_PH_OTP[2:0]			CLK_DIV2_OTP[2:0]		
2B	CFG_CLOCK_2_OTP	VPRE_AUTO_ON_OTP	VPRE_SSRAMP_OTP	BUCK1_PH_OTP[2:0]			VBST_PH_OTP[2:0]		
2C	CFG_CLOCK_3_OTP	DSM_EN_OTP	AUTORETRY_TIMEOUT_OTP	BUCK3_PH_OTP[2:0]			BUCK2_PH_OTP[2:0]		
2D	CFG_CLOCK_4_OTP	BUCK3_CLK_SEL_OTP	BUCK2_CLK_SEL_OTP	BUCK1_CLK_SEL_OTP	VBST_CLK_SEL_OTP	VPRE_CLK_SEL_OTP	PLL_SEL_OTP	CLK_DIV1_OTP[1:0]	
2E	CFG_SM_1_OTP	BOOST_TSDCFG_OTP	BUCK1_TSDCFG_OTP	BUCK2_TSDCFG_OTP	BUCK3_TSDCFG_OTP	LDO1_TSDCFG_OTP	LDO2_TSDCFG_OTP	LDO3_TSDCFG_OTP	HVLDO_TSDCFG_OTP
2F	CFG_SM_2_OTP	DIE_CENTER_TEMP_OTP[2:0]			VPRE_OFF_DLY_OTP	AUTO RETRY_INFINITE_OTP	AUTO RETRY_EN_OTP	PSYNC_CFG_OTP	PSYNC_EN_OTP
30	CFG_I2C_OTP	VDDIO_REG_ASSIGN_OTP[2:0]			I2CDEVADDR_OTP[3:0]				VSUPCFG_OTP
31	CFG_DEVID_OTP	STBY_PGOOD_EN_OTP	STBY_POLARITY_OTP	STBY_DISCH_OTP	STBY_TIMER_EN_OTP	DEVICEID_OTP[3:0]			
32	CFG_SSRAMP_OTP	VPRESHRH_MSB_OTP[1:0]		VPRE_TON_MIN_OTP[1:0]		BUCK3_RAMP_OTP[1:0]		BUCK12DVS_RAMP_OTP[1:0]	

27.2 Main OTP map description

Table 120. Main OTP map description

Address	Register	Bit	Symbol	Value	Description
18	CFG_VPRE_1_OTP	5 to 0	VPREV_OTP[5:0]		VPRE output voltage
				001111	3.3 V
				010000	3.4 V
				010001	3.5 V
				010011	3.7 V
				010110	4 V
				011011	4.5 V
				100000	5 V
				100001	5.1 V
				100010	5.2 V

Table 120. Main OTP map description*...continued*

Address	Register	Bit	Symbol	Value	Description
19	CFG_VPRE_2_OTP	7	VPREDIS_OTP		Disable VPRE when 2 VR5510 are used
				0	VPRE enable
				1	VPRE disable
		6	VPREV_STBY_EN_OTP		Enable 3 V for VPRE in standby mode
				0	Disabled
				1	Enabled
		5 to 0	VPRESC_OTP[5:0]		VPRE slope compensation
				000100	**41.4 mV/µs (default value for 3.3 V/455 kHz)**
				0010000	**82.5 mV/µs (default value for 5 V/455 kHz)**
				001101	**134.3 mV/µs (default value for 3.3 V/2.2 MHz)**
				100000	**504 mV/µs (default value for 5 V/2.2 MHz)**
1A	CFG_VPRE_3_OTP	7 to 6	VPREILIM_OTP[1:0]		VPRE current limitation threshold
				00	50 mV
				01	80 mV
				10	120 mV
				11	150 mV
		5 to 4	VPRETOFF_OTP[1:0]		VPRE minimum OFF time
				00	80 ns
				01	Reserved
				10	Reserved
				11	Reserved
		3 to 2	VPRESRLS_OTP[1:0]		VPRE Low Side slew rate control
				00	PU/PD/130 mA
				01	PU/PD/260 mA
				10	PU/PD/520 mA
				11	**PU/PD/900 mA (default value)**
		1 to 0	VPRESRHS_OTP[1:0]		VPRE High Side pull down slew rate control
				10	**PD/520 mA (455 kHz default value)**
				11	**PD/900 mA (2.2 MHz default value)**
1B	CFG_BOOST_1_OTP	6	PSYNC_PGOOD_EXT_OTP	0	Disabled
				1	Enabled
		5	EXT_STBY_DISCH_OTP	0	Disabled

Table 120. Main OTP map description*...continued*

Address	Register	Bit	Symbol	Value	Description
				1	Enabled, setting based on STBY_DISCH_OTP
		4	VBOS_VBOOST_OTP		Enable BOS to VBOOST path
				0	Enabled
				1	Disabled (when BOOST not populated)
		3 to 0	VBSTV_OTP[3:0]		BOOST output voltage
				0000	4.5 V
				0110	5 V
				0111	5.09 V
				1000	5.19 V
				1010	5.4 V
				1101	5.74 V
				1111	6 V
1C	CFG_BOOST_2_OTP	7	BOOSTEN_OTP		Enable/Disable BOOST regulator
				0	Disabled
				1	Enabled
		6 to 5	VBSTTONTIME_OTP[1:0]		BOOST minimum ON time
				00	**60 ns (default value)**
				01	50 ns
				10	70 ns
				11	80 ns
		4 to 0	VBSTSC_OTP[4:0]		BOOST slope compensation
				00110	160 mV/µs
				01100	125 mV/µs
				01110	79 mV/µs
				01111	**67 mV/µs (default value)**
1D	CFG_BOOST_3_OTP	7 to 6	VBSTRCOMP_OTP[1:0]		BOOST compensation network resistor Rcomp
				00	750 kΩ
				01	500 kΩ
				10	1000 kΩ
				11	**250 kΩ (default)**
		5 to 4	VBSTCCOMP_OTP[1:0]		BOOST compensation network resistor Ccomp
				00	**125 pF (default)**
				01	75 pF
				10	175 pF

Table 120. Main OTP map description*...continued*

Address	Register	Bit	Symbol	Value	Description
				11	125 pF
		3 to 2	VBSTILIM_OTP[1:0]		BOOST inductor peak current limit
				01	1.5 A
				10	2.25 A
		1 to 0	VBSTSR_OTP[1:0]		BOOST Low Side slew rate
				01	Reserved
				10	Reserved
				11	**500 V/µs (default value)**
1E	CFG_BUCK1_1_OTP	7 to 0	BUCK1V_OTP[7:0]		BUCK1 output voltage
				00000000	0.4 V
				01000000	…to (6.25 mV step) 0.8 V
				10110000	1.5 V
				10110001	1.8 V
1F	CFG_BUCK1_2_OTP	7	PSYNC_PWRDWN_EN_OTP		Use PSYNC pin to power down
				0	Disabled
				1	Enabled
		6	PWRON2_GATE_EN_OTP		Use PWRON2 for power up and down
				0	PWRON2 not used for power up/down
				1	PWRON2 used for power up/down
		5	STBY_PGOOD_DLY_OTP		Delay to release the STBY_PGOOD pin
				0	400 µs for HVLDO = 3.3 V
				1	300 µs for HVLDO = 0.8 V
		4 to 3	BUCK1_LSELECT_OTP[1:0]		BUCK1 inductor selection
				00	1 µH
				01	Reserved
				10	Reserved
		2 to 1	BUCK1_ILIM_OTP[1:0]		BUCK1 current limitation
				10	2.4 A
				11	3.6 A
		0	VB12MULTIPH_OTP		BUCK1/2 Multiphase operation
				0	Disabled
				1	Enabled
20	CFG_BUCK2_1_OTP	7 to 0	BUCK2V_OTP[7:0]		BUCK2 output voltage
				00000000	0.4 V
				01000000	…to (6.25 mV step) 0.8 V
				10110000	1.5 V

Table 120. Main OTP map description*...continued*

Address	Register	Bit	Symbol	Value	Description
				10110001	1.8 V
21	CFG_BUCK2_2_OTP	7	AMUX_FOUT		Select AMUX or FOUT
				0	AMUX
				1	FOUT
		6 to 5	BUCK2_LSELECT_OTP[1:0]		BUCK2 inductor selection
				00	1 µH
				01	Reserved
				10	Reserved
		4	BUCK2EN_OTP		BUCK2 Enable
				0	Disabled
				1	Enabled
		3 to 2	BUCK2_ILIM_OTP[1:0]		BUCK2 current limitation
				10	2.4 A
				11	3.6 A
		1	BUCK3_RC_OTP		BUCK3 internal feedback loop resistor
				0	**56 kΩ (default value)**
				1	106 kΩ
		0	BUCK3_GM_OTP		BUCK3 gain margin
				0	**65 GM (default value)**
				1	32.5 GM
22	CFG_BUCK3_1_OTP	7	BUCK3EN_OTP		BUCK3 Enable
				0	Disabled
				1	Enabled
		6 to 5	BUCK3_LSELECT_OTP[1:0]		BUCK3 inductor selection
				00	1 µH
				01	Reserved
				10	Reserved
		4 to 0	BUCK3V_OTP[4:0]		BUCK3 output voltage
				00000	1 V
				00001	1.1 V
				00010	1.2 V
				00011	1.25 V
				00100	1.3 V
				00101	1.35 V
				00110	1.5 V
				00111	1.6 V

Table 120. Main OTP map description*...continued*

Address	Register	Bit	Symbol	Value	Description
				01000	1.8 V
				01001	1.85 V
				01010	2 V
				01011	2.10 V
				01100	2.15 V
				01101	2.25 V
				01110	2.3 V
				01111	2.4 V
				10000	2.5 V
				10001	2.8 V
				10010	3.15 V
				10011	3.20 V
				10100	3.3 V
				10110	3.35 V
				10111	3.4 V
				11000	3.5 V
				11001	3.8 V
				11010	4 V
				11011	4.1 V
23	CFG_BUCK3_2_OTP	7 to 5	BUCK2_COMP_OTP[2:0]		BUCK2 Compensation Network
				001	16.25 GM
				010	32.5 GM
				011	48.75 GM
				100	**65 GM (default value)**
				101	81.25 GM
				110	97.5 GM
				111	113.75 GM
		4 to 2	BUCK1_COMP_OTP[2:0]		BUCK1 Compensation Network
				001	16.25 GM
				010	32.5 GM
				011	48.75 GM
				100	**65 GM (default value)**
				101	81.25 GM
				110	97.5 GM
				111	113.75 GM
		1 to 0	BUCK3_ILIM_OTP[1:0]		BUCK3 current limitation

Table 120. Main OTP map description*...continued*

Address	Register	Bit	Symbol	Value	Description
				10	2.4 A
				11	3.6 A
24	CFG_LDO_ ALL1_OTP	7 to 4	LDO3V_OTP[3:0]		LDO3 output voltage
				0000	1.5 V
				0001	1.6 V
				0010	1.8 V
				0011	1.85 V
				0100	2.15 V
				0101	2.5 V
				0110	2.8 V
				0111	3 V
				1000	3.1 V
				1001	3.15 V
				1010	3.2 V
				1011	3.3 V
				1100	3.35 V
				1101	4 V
				1110	4.9 V
				1111	5 V
		3	HVLDOEN_OTP		HVLDO Enable
				0	Disabled
				1	Enabled
		2	LDO3EN_OTP		LDO3 Enable
				0	Disabled
				1	Enabled
		1	LDO2EN_OTP		LDO2 Enable
				0	Disabled
				1	Enabled
		0	LDO1EN_OTP		LDO1 Enable
				0	Disabled
				1	Enabled
25	CFG_LDO_ ALL2_OTP	7 to 4	LDO2V_OTP[3:0]		LDO2 output voltage
				0000	1.5 V
				0001	1.6 V
				0010	1.8 V
				0011	1.85 V

Table 120. Main OTP map description*...continued*

Address	Register	Bit	Symbol	Value	Description
				0100	2.15 V
				0101	2.5 V
				0110	2.8 V
				0111	3 V
				1000	3.1 V
				1001	3.15 V
				1010	3.2 V
				1011	3.3 V
				1100	3.35 V
				1101	4 V
				1110	4.9 V
				1111	5 V
		3	LDO1ILIM_OTP		LDO1 current limitation
				0	400 mA
				1	150 mA
		2 to 0	LDO1V_OTP[2:0]		LDO1 output voltage
				000	1.1 V
				001	1.2 V
				010	1.6 V
				011	1.8 V
				100	2.5 V
				110	3.3 V
				111	5 V
26	CFG_SEQ_1_OTP	7	LDO3_LS_OTP		Enable load switch mode for LDO3
				0	LDO mode
				1	Switch mode
		6	LDO2_LS_OTP		Enable load switch mode for LDO2
				0	LDO mode
				1	Switch mode
		5 to 3	BUCK3S_OTP[2:0]		BUCK3 sequencing slot
				000	Regulator start and stop in slot 0
				001	Regulator start and stop in slot 1
				010	Regulator start and stop in slot 2
				011	Regulator start and stop in slot 3
				100	Regulator start and stop in slot 4
				101	Regulator start and stop in slot 5

Table 120. Main OTP map description*...continued*

Address	Register	Bit	Symbol	Value	Description
				110	Regulator start and stop in slot 6
				111	Regulator does not start (enable via I^2C)
		2 to 0	BUCK2S_OTP[2:0]		BUCK2 sequencing slot
				000	Regulator start and stop in slot 0
				001	Regulator start and stop in slot 1
				010	Regulator start and stop in slot 2
				011	Regulator start and stop in slot 3
				100	Regulator start and stop in slot 4
				101	Regulator start and stop in slot 5
				110	Regulator start and stop in slot 6
				111	Regulator does not start (enable via I2C)
27	CFG_SEQ_2_OTP	7 to 6	HVLDOV_OTP[1:0]		HVLDO output voltage
				00	0.8 V
				10	3.3 V
		5 to 3	BUCK1S_OTP[2:0]		BUCK1 sequencing slot
				000	Regulator start and stop in slot 0
				001	Regulator start and stop in slot 1
				010	Regulator start and stop in slot 2
				011	Regulator start and stop in slot 3
				100	Regulator start and stop in slot 4
				101	Regulator start and stop in slot 5
				110	Regulator start and stop in slot 6
				111	Regulator does not start (enable via I^2C)
		2 to 0	LDO3S_OTP[2:0]		LDO3 sequencing slot
				000	Regulator start and stop in slot 0
				001	Regulator start and stop in slot 1
				010	Regulator start and stop in slot 2
				011	Regulator start and stop in slot 3
				100	Regulator start and stop in slot 4
				101	Regulator start and stop in slot 5
				110	Regulator start and stop in slot 6
				111	Regulator does not start (enable via I2C)
28	CFG_SEQ_3_OTP	7 to 6	SLOT_WIDTH_OTP[1:0]		Timing between slots
				00	250 µs

Table 120. Main OTP map description*...continued*

Address	Register	Bit	Symbol	Value	Description
				01	500 µs
				10	1 ms
				11	2 ms
		5 to 3	LDO2S_OTP[2:0]		LDO2 sequencing slot
				000	Regulator start and stop in slot 0
				001	Regulator start and stop in slot 1
				010	Regulator start and stop in slot 2
				011	Regulator start and stop in slot 3
				100	Regulator start and stop in slot 4
				101	Regulator start and stop in slot 5
				110	Regulator start and stop in slot 6
				111	Regulator does not start (enable via I^2C)
		2 to 0	LDO1S_OTP[2:0]		LDO2 sequencing slot
				000	Regulator start and stop in slot 0
				001	Regulator start and stop in slot 1
				010	Regulator start and stop in slot 2
				011	Regulator start and stop in slot 3
				100	Regulator start and stop in slot 4
				101	Regulator start and stop in slot 5
				110	Regulator start and stop in slot 6
				111	Regulator does not start (enable via I^2C)
29	CFG_SEQ_4_OTP	7	HVLDO_TRANS_ MODE_OTP		HVLDO mode during normal/STBY mode
				0	HVLDO always in LDO mode
				1	HVLDO in switch mode in normal mode, LDO mode in standby mode
		6	HVLDO_SLOT_EN_OTP		HVLDO starting sequence
				0	First supply to start
				1	Assigned to a slot
		5 to 3	HVLDOS_OTP[2:0]		HVLDO sequencing slot
				000	Regulator start and stop in slot 0
				001	Regulator start and stop in slot 1
				010	Regulator start and stop in slot 2
				011	Regulator start and stop in slot 3
				100	Regulator start and stop in slot 4
				101	Regulator start and stop in slot 5

Table 120. Main OTP map description*...continued*

Address	Register	Bit	Symbol	Value	Description
				110	Regulator start and stop in slot 6
				111	Regulator does not start (enable via I^2C)
		2 to 0	BOOSTS_OTP[2:0]		BOOST sequencing slot
				000	Regulator start and stop in slot 0
				001	Regulator start and stop in slot 1
				010	Regulator start and stop in slot 2
				011	Regulator start and stop in slot 3
				100	Regulator start and stop in slot 4
				101	Regulator start and stop in slot 5
				110	Regulator start and stop in slot 6
				111	Regulator does not start (enable via I^2C)
2A	CFG_CLOCK_1_OTP	7 to 6	VPRE_PFM_TON_OTP[1:0]		Typical VPRE minimum ON time in PFM
				00	Reserved
				01	Reserved
				10	300 ns
				11	**550 ns (default value)**
		5 to 3	VPRE_PH_OTP[2:0]		VPRE phase selection
				000	No delay
				001	delay 1
				010	delay 2
				011	delay 3
				100	delay 4
				101	delay 5
				110	delay 6
				111	delay 7
		2 to 0	CLK_DIV2_OTP[2:0]		Selection of CLK2 frequency
				000	Reserved
				001	Reserved
				100	455 kHz
2B	CFG_CLOCK_2_OTP	7	VPRE_AUTO_ON_OTP		VPRE automatic startup
				0	Disabled, startup based on state machine
				1	Enabled (auto)
		6	VPRE_SSRAMP_OTP		VPRE Internal Reference soft start ramp

Table 120. Main OTP map description*...continued*

Address	Register	Bit	Symbol	Value	Description
				0	1 mV/µs (VPRE will ramp up in 1 ms for 3.3 V setting)
				1	2 mV/µs (VPRE will ramp up in 500 µs for 3.3 V setting)
		5 to 3	BUCK1_PH_OTP[2:0]		BUCK1 phase selection
				000	No delay
				001	delay 1
				010	delay 2
				011	delay 3
				100	delay 4
				101	delay 5
				110	delay 6
				111	delay 7
		2 to 0	VBST_PH_OTP[2:0]		BOOST phase selection
				000	No delay
				001	delay 1
				010	delay 2
				011	delay 3
				100	delay 4
				101	delay 5
				110	delay 6
				111	delay 7
2C	CFG_CLOCK_3_OTP	7	DSM_EN_OTP		Deep Sleep Mode enable
				0	Disabled
				1	Enabled
		6	AUTORETRY_TIMEOUT_OTP		Time between each autoretry
				0	4 s
				1	100 ms
		5 to 3	BUCK3_PH_OTP[2:0]		BUCK3 phase selection
				000	No delay
				001	delay 1
				010	delay 2
				011	delay 3
				100	delay 4
				101	delay 5

Table 120. Main OTP map description*...continued*

Address	Register	Bit	Symbol	Value	Description
				110	delay 6
				111	delay 7
		2 to 0	BUCK2_PH_OTP[2:0]		BUCK2 phase selection
				000	No delay
				001	delay 1
				010	delay 2
				011	delay 3
				100	delay 4
				101	delay 5
				110	delay 6
				111	delay 7
2D	CFG_CLOCK_4_OTP	7	BUCK3_CLK_SEL_OTP		BUCK1 clock selection
				0	CLK_DIV1
				1	Reserved
		6	BUCK2_CLK_SEL_OTP		BUCK2 clock selection
				0	CLK_DIV1
				1	Reserved
		5	BUCK1_CLK_SEL_OTP		BUCK1 clock selection
				0	CLK_DIV1
				1	Reserved
		4	VBST_CLK_SEL_OTP		VBST clock selection
				0	CLK_DIV1
				1	Reserved
		3	VPRE_CLK_SEL_OTP		VPRE clock selection
				0	CLK_DIV1
				1	CLK_DIV2
		2	PLL_SEL_OTP		PLL enable
				0	Disabled
				1	Enabled
		1 to 0	CLK_DIV1_OTP[1:0]		Selection of CLK1 frequency
				10	2.22 MHz
				01	Reserved
2E	CFG_SM_1_OTP	7	BOOST_TSDCFG_OTP		Boost behavior in case of TSD
				0	Shutdown
				1	Shutdown + Deep Fail Safe
		6	BUCK1_TSDCFG_OTP		BUCK1 behavior in case of TSD

Table 120. Main OTP map description*...continued*

Address	Register	Bit	Symbol	Value	Description
				0	Shutdown
				1	Shutdown + Deep Fail Safe
		5	BUCK2_TSDCFG_OTP		BUCK2 behavior in case of TSD
				0	Shutdown
				1	Shutdown + Deep Fail Safe
		4	BUCK3_TSDCFG_OTP		BUCK3 behavior in case of TSD
				0	Shutdown
				1	Shutdown + Deep Fail Safe
		3	LDO1_TSDCFG_OTP		LDO1 behavior in case of TSD
				0	Shutdown
				1	Shutdown + Deep Fail Safe
		2	LDO2_TSDCFG_OTP		LDO2 behavior in case of TSD
				0	Shutdown
				1	Shutdown + Deep Fail Safe
		1	LDO3_TSDCFG_OTP		LDO3 behavior in case of TSD
				0	Shutdown
				1	Shutdown + Deep Fail Safe
		0	HVLDO_TSDCFG_OTP		HVLDO behavior in case of TSD
				0	Shutdown
				1	Shutdown + Deep Fail Safe
2F	CFG_SM_2_OTP	7 to 5	DIE_CENTER_ TEMP_OTP[2:0]		Die center temperature warning
				000	75 °C
				001	95 °C
				010	105 °C
				011	120 °C
				100	135 °C
				101	150 °C
		4	VPRE_OFF_DLY_OTP		Delay to turn OFF VPRE at power down
				0	SLOT_WIDTH_OTP[1:0]
				1	32 ms
		3	AUTORETRY_ INFINITE_OTP		Numbers of auto retry sequence
				0	15 times
				1	Endless
		2	AUTORETRY_EN_OTP		Auto retry enable
				0	Disabled
				1	Enabled

Table 120. Main OTP map description*...continued*

Address	Register	Bit	Symbol	Value	Description
		1	PSYNC_CFG_OTP		Synchronization
				0	2 x VR5510
				1	1 x VR5510 + 1 x External PMIC
		0	PSYNC_EN_OTP		Enable PSYNC function
				0	Disabled
				1	Enabled
30	CFG_I2C_OTP	7 to 5	VDDIO_REG_ ASSIGN_OTP[2:0]		Regulator assigned to VDDIO
				000	External regulator
				001	VPRE
				010	LDO1
				011	LDO2
				100	BUCK2
				101	BUCK3
				110	LDO3
				111	External regulator
		4 to 1	I2CDEVADDR_OTP[3:0]		VR5510 I^2C address
				0000	D0
				…	
				1111	D15
		0	VSUPCFG_OTP		VSUP threshold for startup
				0	4.9 V
				1	6.2 V
31	CFG_DEVID_OTP	7	STBY_PGOOD_EN_OTP		Enable STBY_PGOOD function
				0	Disabled
				1	Enabled
		6	STBY_POLARITY_OTP		STBY Polarity selection
				0	High in normal mode / Low in standby mode
				1	Low in normal mode / High in standby mode
		5	STBY_DISCH_OTP		Threshold selection
				0	75 mV
				1	150 mV
		4	STBY_TIMER_EN_OTP		STBY timer enable
				0	Disabled
				1	Enabled
		3 to 0	DEVICEID_OTP[3:0]		Reserved

Table 120. Main OTP map description*...continued*

Address	Register	Bit	Symbol	Value	Description
32	CFG_ SSRAMP_OTP	7 to 6	VPRESRHS_MSB_OTP[1:0]		VPRE High Side pull up slew rate control
				00	PU/130 mA
				01	PU/260 mA
				10	**PU/520 mA (455 kHz default value)**
				11	**PU/900 mA (2.2 MHz default value)**
		5 to 4	VPRE_TON_MIN_OTP[1:0]		Minimum TON in PWM mode
				00	**45 ns (455 kHz default value)**
				01	65 ns
				10	**25 ns (2.2 MHz default value)**
				11	45 ns
		3 to 2	BUCK3_RAMP_OTP[1:0]		BUCK3 RAMP selection
				00	10.42 mV/µs (power up/down)
				01	3.47 mV/µs (power up/down)
				10	2.6 mV/µs (power up/down)
				11	2.08 mV/µs (power up/down)
		1 to 0	BUCK12DVS_ RAMP_OTP[1:0]		BUCK1/2 DVS RAMP selection
				00	15.6 mV/µs (power up) / 10.4 mV/µs (power down)
				01	7.8 mV/µs (power up) / 5.2 mV/µs (power down)
				10	2.6 mV/µs (power up/down)
				11	2.23 mV/µs (power up/down)

27.3 Fail Safe OTP map overview

Table 121. Fail Safe OTP map overview

Addr.	Register Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0B	CFG_ UVOV_ 1_OTP	VCORE_V_OTP[7:0]							
0C	CFG_ UVOV_ 2_OTP	VDDIOOVTH_OTP[3:0]				VCOREOVTH_OTP[3:0]			
0D	CFG_ UVOV_ 3_OTP	0	VCORE_ SVS_FULL_ OFFSET_OTP	VCORE_SVS_CLAMP_OTP[5:0]					
0E	CFG_ UVOV_ 4_OTP	VMON2OVTH_OTP[3:0]				VMON1OVTH_OTP[3:0]			

Table 121. Fail Safe OTP map overview*...continued*

Addr.	Register Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0F	CFG_UVOV_5_OTP	VMON4OVTH_OTP[3:0]				VMON3OVTH_OTP[3:0]			
10	CFG_UVOV_6_OTP	VDDIOUVTH_OTP[3:0]				VCOREUVTH_OTP[3:0]			
11	CFG_UVOV_7_OTP	VMON2UVTH_OTP[3:0]				VMON1UVTH_OTP[3:0]			
12	CFG_UVOV_8_OTP	VMON4UVTH_OTP[3:0]				VMON3UVTH_OTP[3:0]			
13	CFG_UVOV_9_OTP	HVLDO_VMON_UVTH_OTP[3:0]				HVLDO_VMON_OVTH_OTP[3:0]			
14	CFG_PGOOD_OTP	PGOOD_HVLDO_VMON_OTP	RSTB2PGOOD_OTP	PGOOD_VMON4_OTP	PGOOD_VMON3_OTP	PGOOD_VMON2_OTP	PGOOD_VMON1_OTP	PGOOD_VDDIO_OTP	PGOOD_VCORE_OTP
15	CFG_ABIST1_OTP	DIS8S_OTP	ABIST1_HVLDO_VMON_OTP	ABIST1_VMON4_OTP	ABIST1_VMON3_OTP	ABIST1_VMON2_OTP	ABIST1_VMON1_OTP	ABIST1_VDDIO_OTP	ABIST1_VCORE_OTP
16	CFG_ASIL_OTP	0	0	HVLDO_VMON_EN_OTP	0	VMON4_EN_OTP	VMON3_EN_OTP	VMON2_EN_OTP	VMON1_EN_OTP
17	CFG_I2C_OTP	0	VDDIO_VMON_EN_OTP	WDI_POL_OTP	0	I2CDEVID_OTP[3:0]			
18	CFG_1_OTP	HVLDO_V_OTP[1:0]		HVLDO_MODE_OTP	0	FCCU_OR_WDI_OTP	VDDIO_V_OTP	0	0
19	CFG_2_OTP	WD_INIT_TIMEOUT_OTP[1:0]		STBY_WINDOW_EN_OTP	STBY_SAFE_DIS_OTP	STBY_POLARITY_FS_OTP	STBY_EN_OTP	RSTB_DELAY_OTP	0
1A	CFG_DEGLITCH1_OTP	OV_VMON1_OTP	OV_HVLDO_OTP	UV_VDDIO_OTP[1:0]		OV_VDDIO_OTP	UV_MCU_OTP[1:0]		OV_MCU_OTP
1B	CFG_DEGLITCH2_OTP	OV_VMON3_OTP	UV_VMON2_OTP[1:0]		OV_VMON2_OTP	UV_VMON1_OTP[1:0]		UV_HVLDO_OTP[1:0]	
1C	CFG_DEGLITCH3_OTP	0	0	0	UV_VMON4_OTP[1:0]		OV_VMON4_OTP	UV_VMON4_OTP[1:0]	

27.4 Fail Safe OTP map description and S32G default setting

Table 122. Fail Safe OTP map description and S32G default setting

Address	Register	Bit	Symbol	Value	Description
0B	CFG_UVOV_1_OTP	7 to 0	VCORE_V_OTP[7:0]		BUCK1 output voltage
				0000 0000	0.4 V
				0100 0000	…to (6.25 mV step) 0.8 V
				1011 0000	1.5 V
				1011 0001	1.8 V
0C	CFG_UVOV_2_OTP	7 to 4	VDDIOOVTH_OTP[3:0]		VDDIO over-voltage threshold
				0000	104.5%
				0001	105%
				0010	105.5%
				0011	106%
				0100	106.5%
				0101	107%
				0110	107.5%
				0111	108%
				1000	108.5%
				1001	109%
				1010	109.5%
				1011	110%
				1100	102.5%
				1101	103%
				1110	103.5%
				1111	104%
		3 to 0	VCOREOVTH_OTP[3:0]		VCOREMON over-voltage threshold
				0000	104.5%
				0001	105%
				0010	105.5%
				0011	106%
				0100	106.5%
				0101	107%
				0110	107.5%
				0111	108%
				1000	108.5%

Table 122. Fail Safe OTP map description and S32G default setting*...continued*

Address	Register	Bit	Symbol	Value	Description
				1001	109%
				1010	109.5%
				1011	110%
				1100	102.5%
				1101	103%
				1110	103.5%
				1111	104%
0D	CFG_UVOV_3_OTP	6	VCORE_SVS_ FULL_OFFSET_OTP		Enable full offset range for SVS
				0	Only negative offset
				1	Positive or negative offset
		5 to 0	VCORE_SVS_ CLAMP_OTP[5:0]		SVS max steps value available
				000000	No SVS
				000001	2 steps available
				000011	4 steps available
				000111	8 steps available
				001111	16 steps available
				011111	32 steps available
				111111	64 steps available
0E	CFG_UVOV_4_OTP	7 to 4	VMON2OVTH_OTP[3:0]		VMON2 over-voltage threshold
				0000	104.5%
				0001	105%
				0010	105.5%
				0011	106%
				0100	106.5%
				0101	107%
				0110	107.5%
				0111	108%
				1000	108.5%
				1001	109%
				1010	109.5%
				1011	110%
				1100	102.5%
				1101	103%
				1110	103.5%
				1111	104%
		3 to 0	VMON1OVTH_OTP[3:0]		VMON1 over-voltage threshold

Table 122. Fail Safe OTP map description and S32G default setting*...continued*

Address	Register	Bit	Symbol	Value	Description
				0000	104.5%
				0001	105%
				0010	105.5%
				0011	106%
				0100	106.5%
				0101	107%
				0110	107.5%
				0111	108%
				1000	108.5%
				1001	109%
				1010	109.5%
				1011	110%
				1100	102.5%
				1101	103%
				1110	103.5%
				1111	104%
0F	CFG_UVOV_5_OTP	7 to 4	VMON4OVTH_OTP[3:0]		VMON4 over-voltage threshold
				0000	104.5%
				0001	105%
				0010	105.5%
				0011	106%
				0100	106.5%
				0101	107%
				0110	107.5%
				0111	108%
				1000	108.5%
				1001	109%
				1010	109.5%
				1011	110%
				1100	102.5%
				1101	103%
				1110	103.5%
				1111	104%
		3 to 0	VMON3OVTH_OTP[3:0]		VMON3 over-voltage threshold
				0000	104.5%
				0001	105%

Table 122. Fail Safe OTP map description and S32G default setting*...continued*

Address	Register	Bit	Symbol	Value	Description
				0010	105.5%
				0011	106%
				0100	106.5%
				0101	107%
				0110	107.5%
				0111	108%
				1000	108.5%
				1001	109%
				1010	109.5%
				1011	110%
				1100	102.5%
				1101	103%
				1110	103.5%
				1111	104%
10	CFG_UVOV_6_OTP	7 to 4	VDDIOUVTH_OTP[3:0]		VDDIO under-voltage threshold
				0000	95.5%
				0001	95%
				0010	94.5%
				0011	94%
				0100	93.5%
				0101	93%
				0110	92.5%
				0111	92%
				1000	91.5%
				1001	91%
				1010	90.5%
				1011	90%
				1100	97.5%
				1101	97%
				1110	96.5%
				1111	96%
		3 to 0	VCOREUVTH_OTP[3:0]		VCOREMON under-voltage threshold
				0000	95.5%
				0001	95%
				0010	94.5%
				0011	94%

Table 122. Fail Safe OTP map description and S32G default setting*...continued*

Address	Register	Bit	Symbol	Value	Description
				0100	93.5%
				0101	93%
				0110	92.5%
				0111	92%
				1000	91.5%
				1001	91%
				1010	90.5%
				1011	90%
				1100	97.5%
				1101	97%
				1110	96.5.5%
				1111	96%
11	CFG_UVOV_7_OTP	7 to 4	VMON2UVTH_OTP[3:0]		VMON2 under-voltage threshold
				0000	95.5%
				0001	95%
				0010	94.5%
				0011	94%
				0100	93.5%
				0101	93%
				0110	92.5%
				0111	92%
				1000	91.5%
				1001	91%
				1010	90.5%
				1011	90%
				1100	97.5%
				1101	97%
				1110	96.5%
				1111	96%
		3 to 0	VMON1UVTH_OTP[3:0]		VMON1 under-voltage threshold
				0000	95.5%
				0001	95%
				0010	94.5%
				0011	94%
				0100	93.5%
				0101	93%

Table 122. Fail Safe OTP map description and S32G default setting*...continued*

Address	Register	Bit	Symbol	Value	Description
				0110	92.5%
				0111	92%
				1000	91.5%
				1001	91%
				1010	90.5%
				1011	90%
				1100	97.5%
				1101	97%
				1110	96.5%
				1111	96%
12	CFG_UVOV_8_OTP	7 to 4	VMON4UVTH_OTP[3:0]		VMON4 under-voltage threshold
				0000	95.5%
				0001	95%
				0010	94.5%
				0011	94%
				0100	93.5%
				0101	93%
				0110	92.5%
				0111	92%
				1000	91.5%
				1001	91%
				1010	90.5%
				1011	90%
				1100	97.5%
				1101	97%
				1110	96.5%
				1111	96%
		3 to 0	VMON3UVTH_OTP[3:0]		VMON3 under-voltage threshold
				0000	95.5%
				0001	95%
				0010	94.5%
				0011	94%
				0100	93.5%
				0101	93%
				0110	92.5%
				0111	92%

Table 122. Fail Safe OTP map description and S32G default setting*...continued*

Address	Register	Bit	Symbol	Value	Description
				1000	91.5%
				1001	91%
				1010	90.5%
				1011	90%
				1100	97.5%
				1101	97%
				1110	96.5%
				1111	96%
13	CFG_UVOV_9_OTP	7 to 4	HVLDO_VMON_ UVTH_OTP[3:0]		HVLDO VMON under-voltage threshold
				0000	95.5%
				0001	95%
				0010	94.5%
				0011	94%
				0100	93.5%
				0101	93%
				0110	92.5%
				0111	92%
				1000	91.5%
				1001	91%
				1010	90.5%
				1011	90%
				1100	97.5%
				1101	97%
				1110	96.5%
				1111	96%
		3 to 0	HVLDO_VMON_ OVTH_OTP[3:0]		HVLDO VMON over-voltage threshold
				0000	104.5%
				0001	105%
				0010	105.5%
				0011	106%
				0100	106.5%
				0101	107%
				0110	107.5%
				0111	108%
				1000	108.5%

Table 122. Fail Safe OTP map description and S32G default setting*...continued*

Address	Register	Bit	Symbol	Value	Description
				1001	109%
				1010	109.5%
				1011	110%
				1100	102.5%
				1101	103%
				1110	103.5%
				1111	104%
14	CFG_PGOOD_OTP	7	PGOOD_HVLDO_ VMON_OTP		HVLDO VMON assigned to PGOOD
				0	Not assigned
				1	Assigned
		6	RSTB2PGOOD_OTP		RSTB assigned to PGOOD
				0	Not assigned
				1	Assigned
		5	PGOOD_VMON4_OTP		VMON4 assigned to PGOOD
				0	Not assigned
				1	Assigned
		4	PGOOD_VMON3_OTP		VMON3 assigned to PGOOD
				0	Not assigned
				1	Assigned
		3	PGOOD_VMON2_OTP		VMON2 assigned to PGOOD
				0	Not assigned
				1	Assigned
		2	PGOOD_VMON1_OTP		VMON1 assigned to PGOOD
				0	Not assigned
				1	Assigned
		1	PGOOD_VDDIO_OTP		VDDIO VMON assigned to PGOOD
				0	Not assigned
				1	Assigned
		0	PGOOD_VCORE_OTP		VCOREMON assigned to PGOOD
				0	Not assigned
				1	Assigned
15	CFG_ABIST1_OTP	7	DIS8S_OTP		Disable the Fail Safe 8s counter
				0	Counter activated
				1	Disabled
		6	ABIST1_HVLDO_ VMON_OTP		HVLDO VMON assignment to ABIST1
				0	Not assigned

Table 122. Fail Safe OTP map description and S32G default setting*...continued*

Address	Register	Bit	Symbol	Value	Description
				1	Assigned
		5	ABIST1_VMON4_OTP		VMON4 assignment to ABIST1
				0	Not assigned
				1	Assigned
		4	ABIST1_VMON3_OTP		VMON3 assignment to ABIST1
				0	Not assigned
				1	Assigned
		3	ABIST1_VMON2_OTP		VMON2 assignment to ABIST1
				0	Not assigned
				1	Assigned
		2	ABIST1_VMON1_OTP		VMON1 assignment to ABIST1
				0	Not assigned
				1	Assigned
		1	ABIST1_VDDIO_OTP		VDDIO VMON assignment to ABIST1
				0	Not assigned
				1	Assigned
		0	ABIST1_VCORE_OTP		VCOREMON assignment to ABIST1
				0	Not assigned
				1	Assigned
16	CFG_ASIL_OTP	5	HVLDO_VMON_EN_OTP		HVLDO VMON enable
				0	Disabled
				1	Enabled
		3	VMON4_EN_OTP		VMON4 enable
				0	Disabled
				1	Enabled
		2	VMON3_EN_OTP		VMON3 enable
				0	Disabled
				1	Enabled
		1	VMON2_EN_OTP		VMON2 enable
				0	Disabled
				1	Enabled
		0	VMON1_EN_OTP		VMON1 enable
				0	Disabled
				1	Enabled
17	CFG_I2C_OTP	6	VDDIO_VMON_EN_OTP		VDDIO VMON enable
				0	Disabled

Table 122. Fail Safe OTP map description and S32G default setting*...continued*

Address	Register	Bit	Symbol	Value	Description
				1	Enabled
		5	WDI_POL_OTP		WDI Polarity configuration
				0	Falling edge
				1	Rising edge
		3 to 0	I2CDEVID_OTP[3:0]		VR5510 I^2C address
				0000	Address is D0
				…	
				1111	Address is D15
18	CFG_1_OTP	7 to 6	HVLDO_V_OTP[1:0]		HVLDO VMON voltage selection
				00	0.8 V
				10	3.3 V
		5	HVLDO_MODE_OTP		HVLDO mode selection
				0	Switch mode connected to BUCK1
				1	LDO mode
		3	FCCU_OR_WDI_OTP		Enable WDI function on FCCU1
				0	Disabled
				1	Enabled
		2	VDDIO_V_OTP		VDDIO VMON selection
				0	1.8 V
				1	3.3 V
19	CFG_2_OTP	7 to 6	WD_INIT_ TIMEOUT_OTP[1:0]	00	256 ms
				01	1024 ms
				10	32.5 s
				11	67 s
		5	STBY_WINDOW_EN_OTP		Enable standby window function
				0	Disabled
				1	Enabled
		4	STBY_SAFE_DIS_OTP		Enable safe standby entry
				0	I^2C command + STBY Pin transition
				1	STBY pin transition
		3	STBY_POLARITY_FS_OTP		STBY Pin polarity
				0	High in normal mode / Low in standby mode
				1	Low in normal mode / High in standby mode
		2	STBY_EN_OTP		Enable standby function
				0	Disabled

Table 122. Fail Safe OTP map description and S32G default setting*...continued*

Address	Register	Bit	Symbol	Value	Description
				1	Enabled
		1	RSTB_DELAY_OTP		Add delay to release RSTB/PGOOD pins
				0	No delay
				1	5 ms delay
1A	CFG_ DEGLITCH1_OTP	7	OV_VMON1_OTP		VMON1 OV filtering time
				0	25 µs
				1	45 µs
		6	OV_HVLDO_OTP		HVLDO VMON OV filtering time
				0	25 µs
				1	45us
		5 to 4	UV_VDDIO_OTP[1:0]		VDDIO UV filtering time
				00	5 µs
				01	15 µs
				10	25 µs
				11	40 µs
		3	OV_VDDIO_OTP		VDDIO VMON OV filtering time
				0	25 µs
				1	45 µs
		2 to 1	UV_MCU_OTP[1:0]		VCOREMON UV filtering time
				00	5 µs
				01	15 µs
				10	25 µs
				11	40 µs
		0	OV_MCU_OTP		VCOREMON OV filtering time
				0	25 µs
				1	45 µs
1B	CFG_ DEGLITCH2_OTP	7	OV_VMON3_OTP		VMON3 OV filtering time
				0	25 µs
				1	45 µs
		6 to 5	UV_VMON2_OTP[1:0]		VMON2 UV filtering time
				00	5 µs
				01	15 µs
				10	25 µs
				11	40us
		4	OV_VMON2_OTP		VMON2 OV filtering time
				0	25 µs

Table 122. Fail Safe OTP map description and S32G default setting*...continued*

Address	Register	Bit	Symbol	Value	Description
				1	45 µs
		3 to 2	UV_VMON1_OTP[1:0]		VMON1 UV filtering time
				00	5 µs
				01	15 µs
				10	25 µs
				11	40 µs
		1 to 0	UV_HVLDO_OTP[1:0]		HVLDO VMON UV filtering time
				00	5 µs
				01	15 µs
				10	25 µs
				11	40 µs
1C	CFG_ DEGLITCH3_OTP	4 to 3	UV_VMON4_OTP[1:0]		VMON4 UV filtering time
				00	5 µs
				01	15 µs
				10	25 µs
				11	40 µs
		2	OV_VMON4_OTP		VMON4 OV filtering time
				0	25 µs
				1	45 µs
		1 to 0	UV_VMON3_OTP[1:0]		VMON3 UV filtering time
				00	5 µs
				01	15 µs
				10	25 µs
				11	40 µs

28 Package Drawing and PCB Guidelines

28.1 Landing pad information for Automotive part numbers

VR5510 package is a QFN (sawn), thermally enhanced wettable flanks, 8x8x0.85, 0.5 pitch, 56 pins.

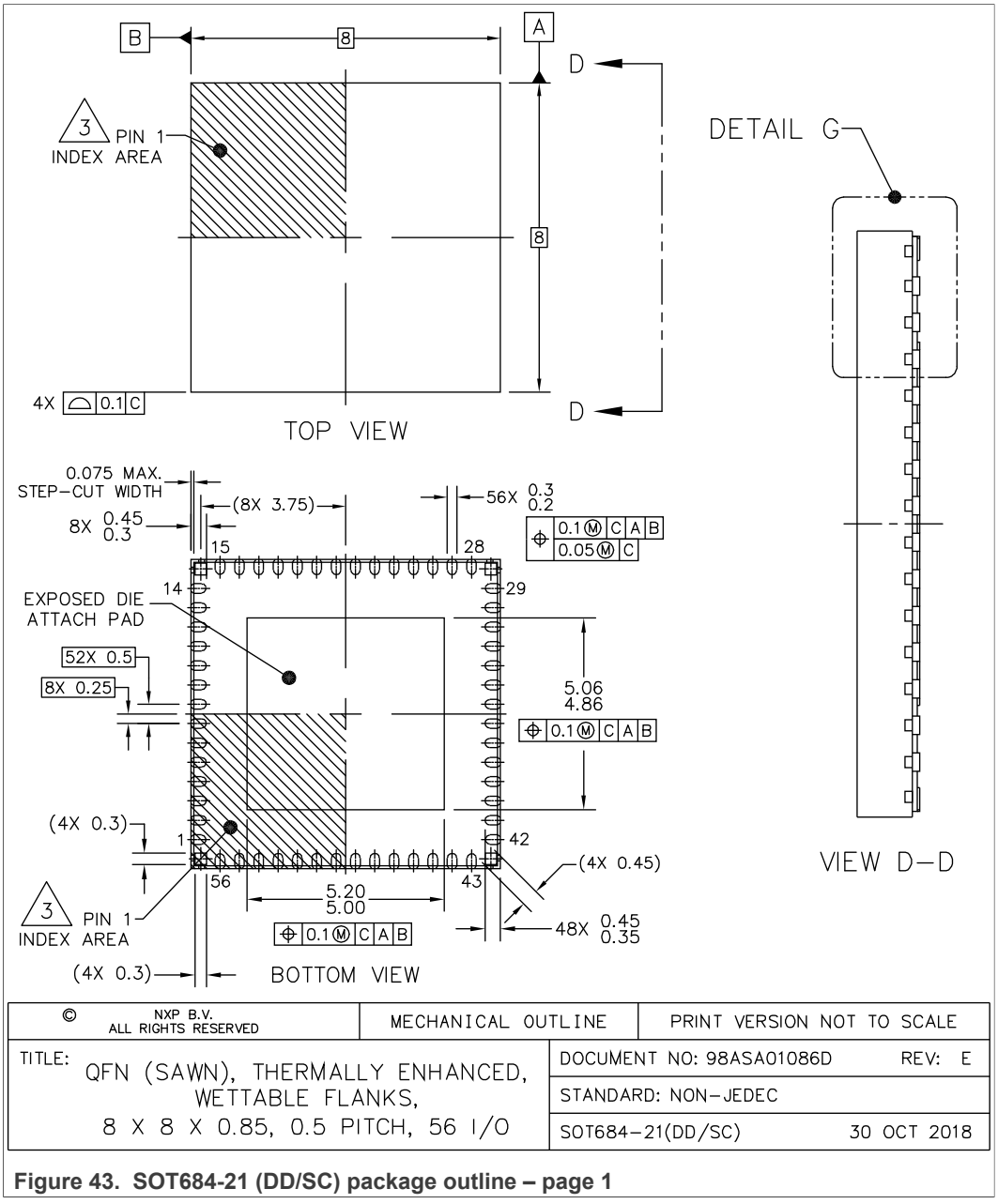
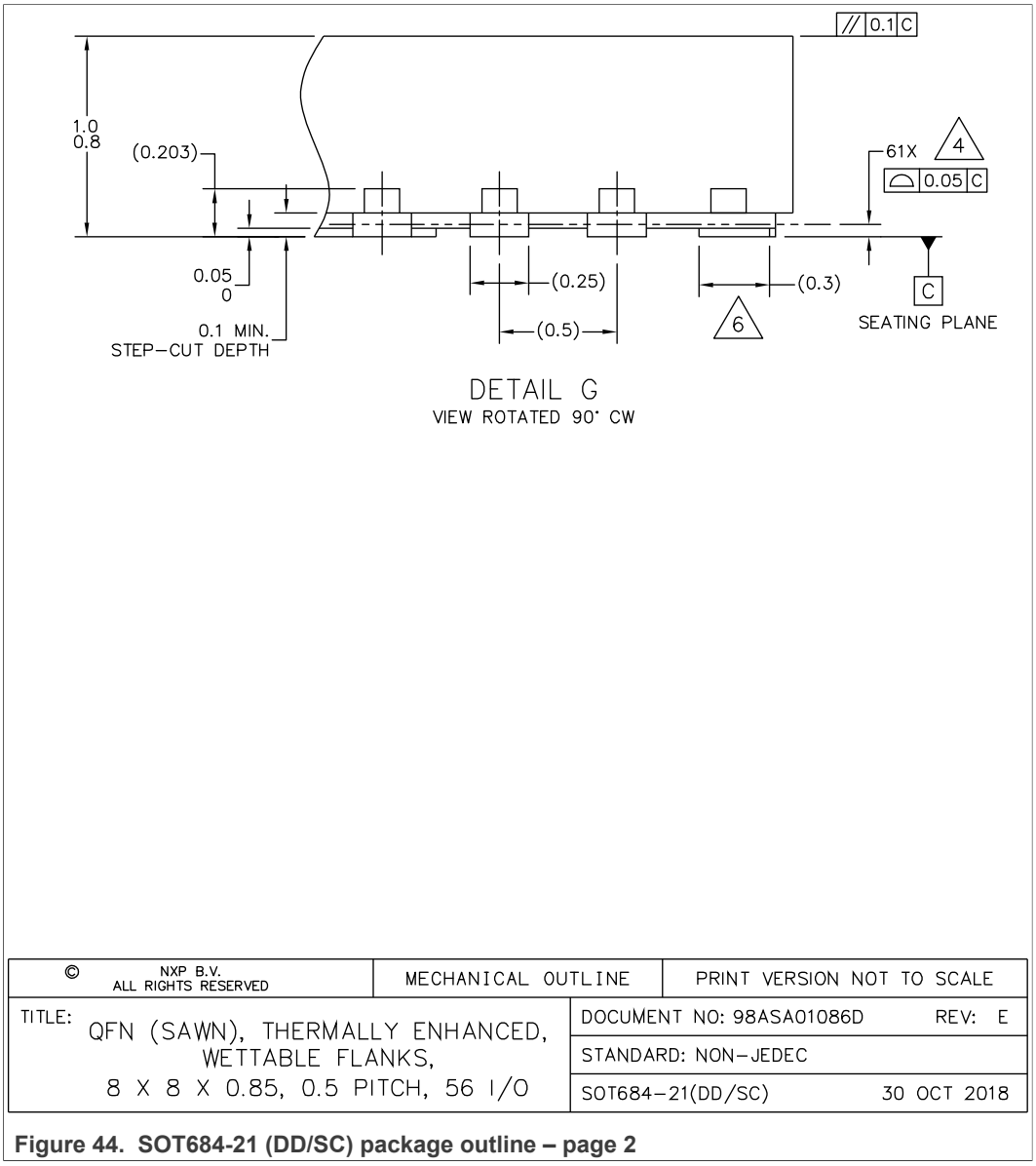


Figure 43. SOT684-21 (DD/SC) package outline – page 1



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TITLE: QFN (SAWN), THERMALLY ENHANCED, WETTABLE FLANKS, 8 X 8 X 0.85, 0.5 PITCH, 56 I/O	DOCUMENT NO: 98ASA01086D	REV: E
	STANDARD: NON–JEDEC	
	SOT684–21(DD/SC)	30 OCT 2018

Figure 44. SOT684-21 (DD/SC) package outline – page 2

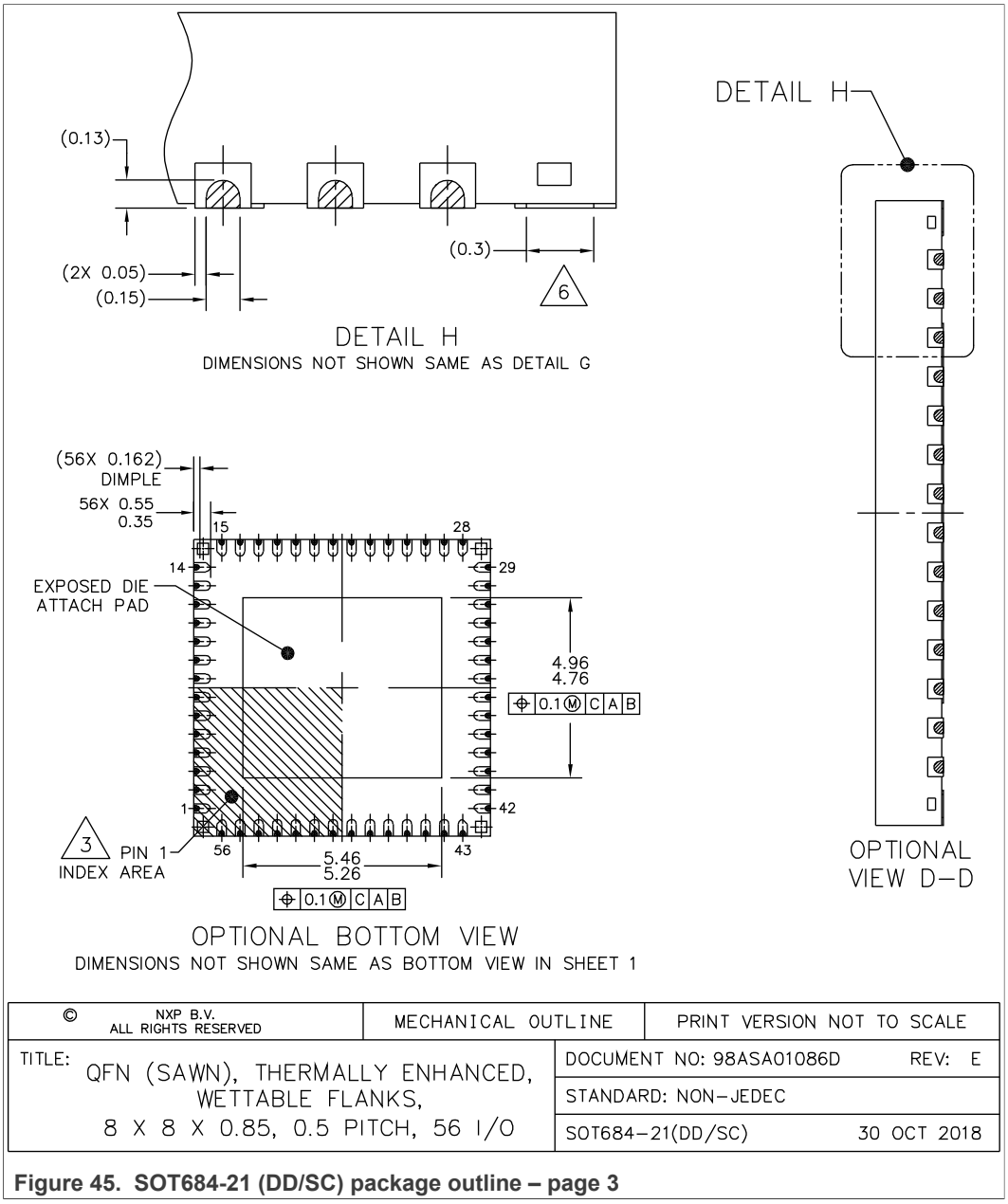


Figure 45. SOT684-21 (DD/SC) package outline – page 3

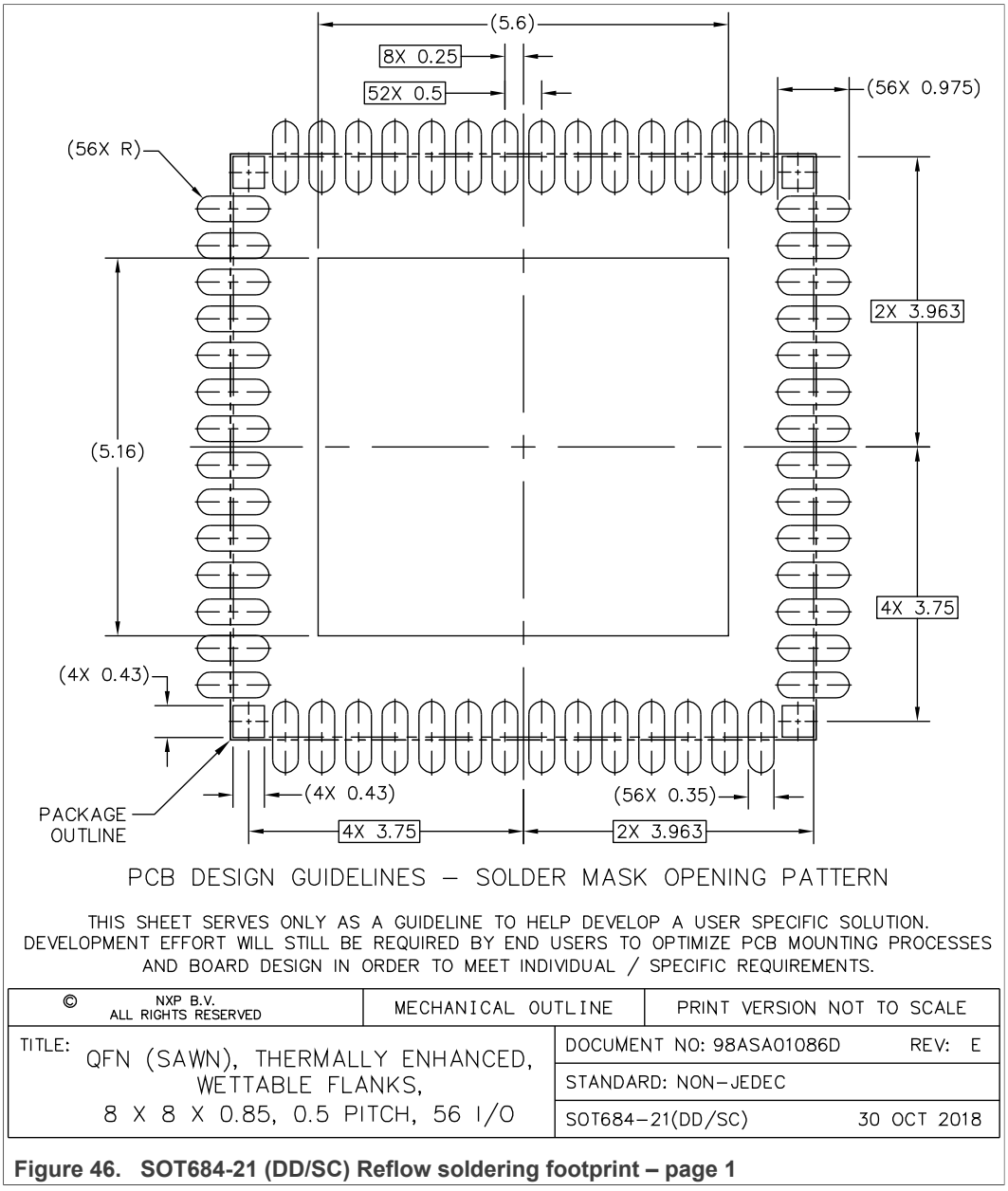


Figure 46. SOT684-21 (DD/SC) Reflow soldering footprint – page 1

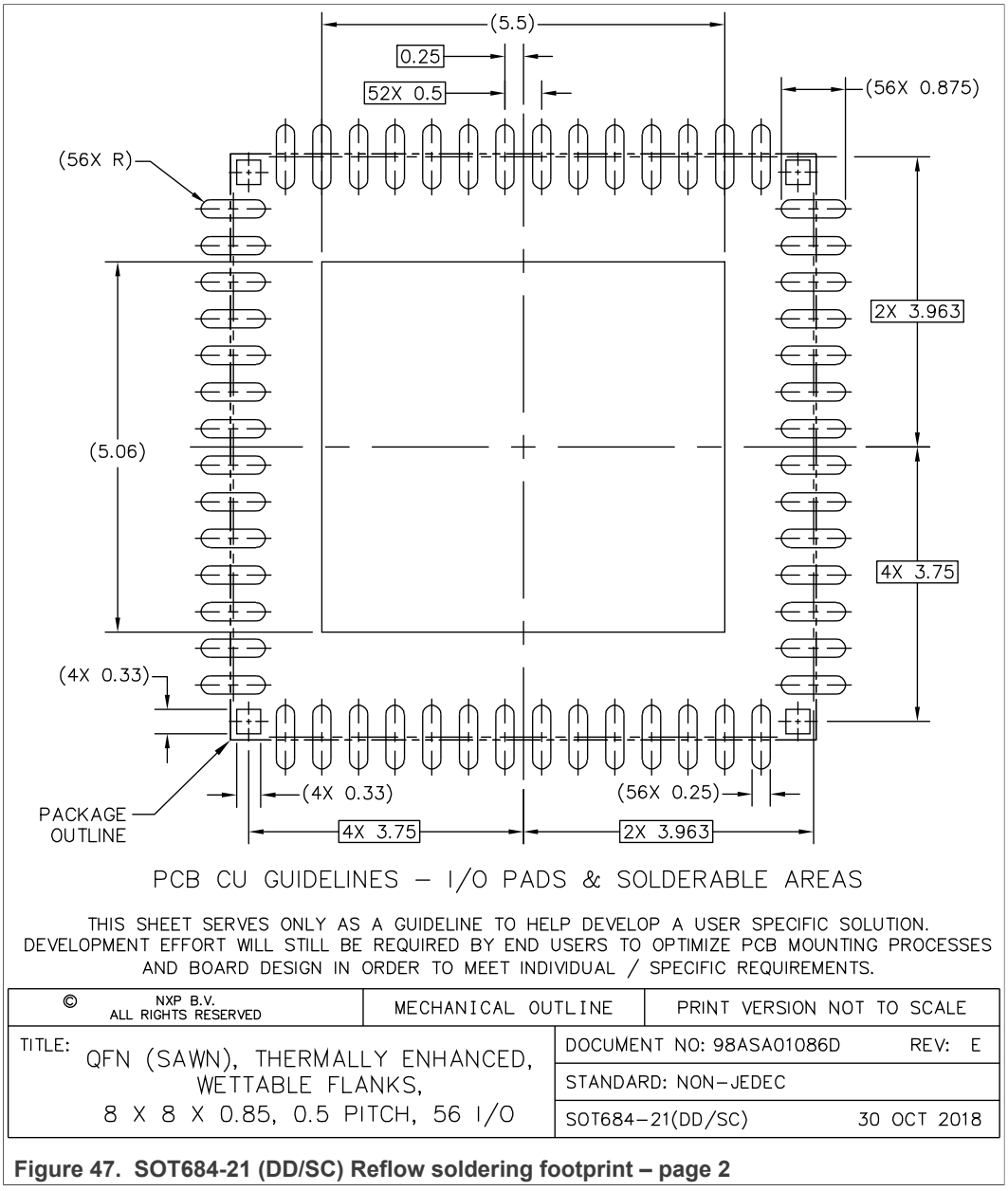


Figure 47. SOT684-21 (DD/SC) Reflow soldering footprint – page 2

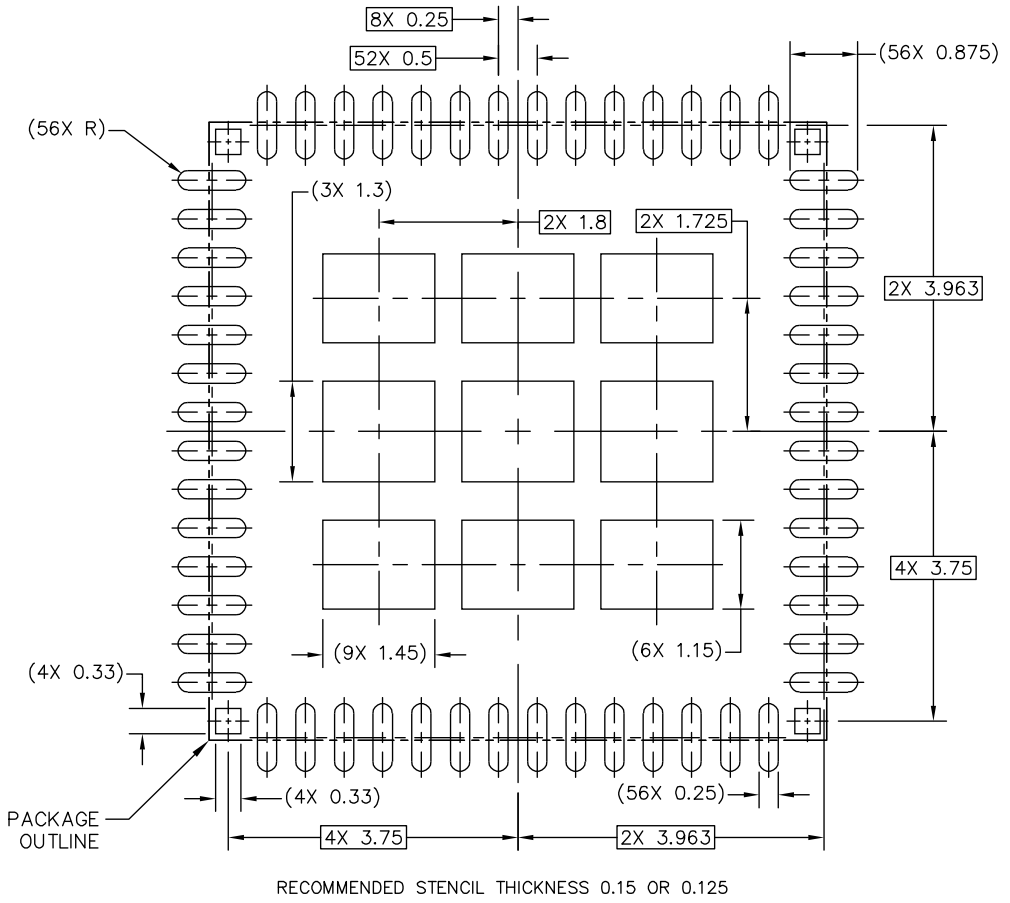


Figure 48. SOT684-21 (DD/SC) Reflow soldering footprint – page 3

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN ONE CONFIGURATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS, DIE ATTACH FLAG AND CORNER NON–FUNCTIONAL PADS.
5. MIN. METAL GAP SHOULD BE 0.25 MM.
6. ANCHORING PADS.

Figure 49. SOT684-21 (DD/SC) Reflow soldering footprint – page 4

28.2 Landing pad information for Industrial part numbers

VR5510 package is a QFN (sawn), 8x8x0.85, 0.5 pitch, 56 pins.

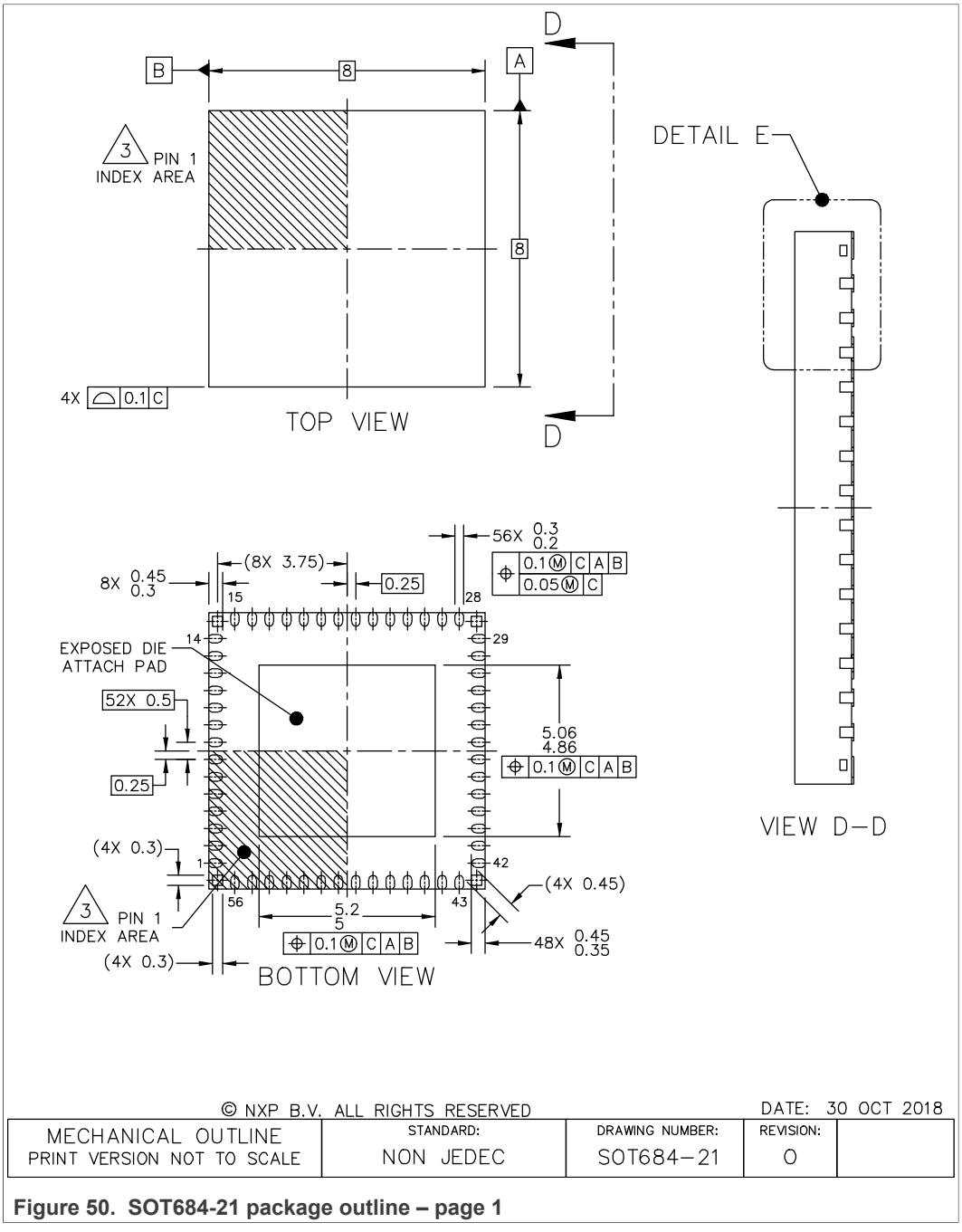


Figure 50. SOT684-21 package outline – page 1

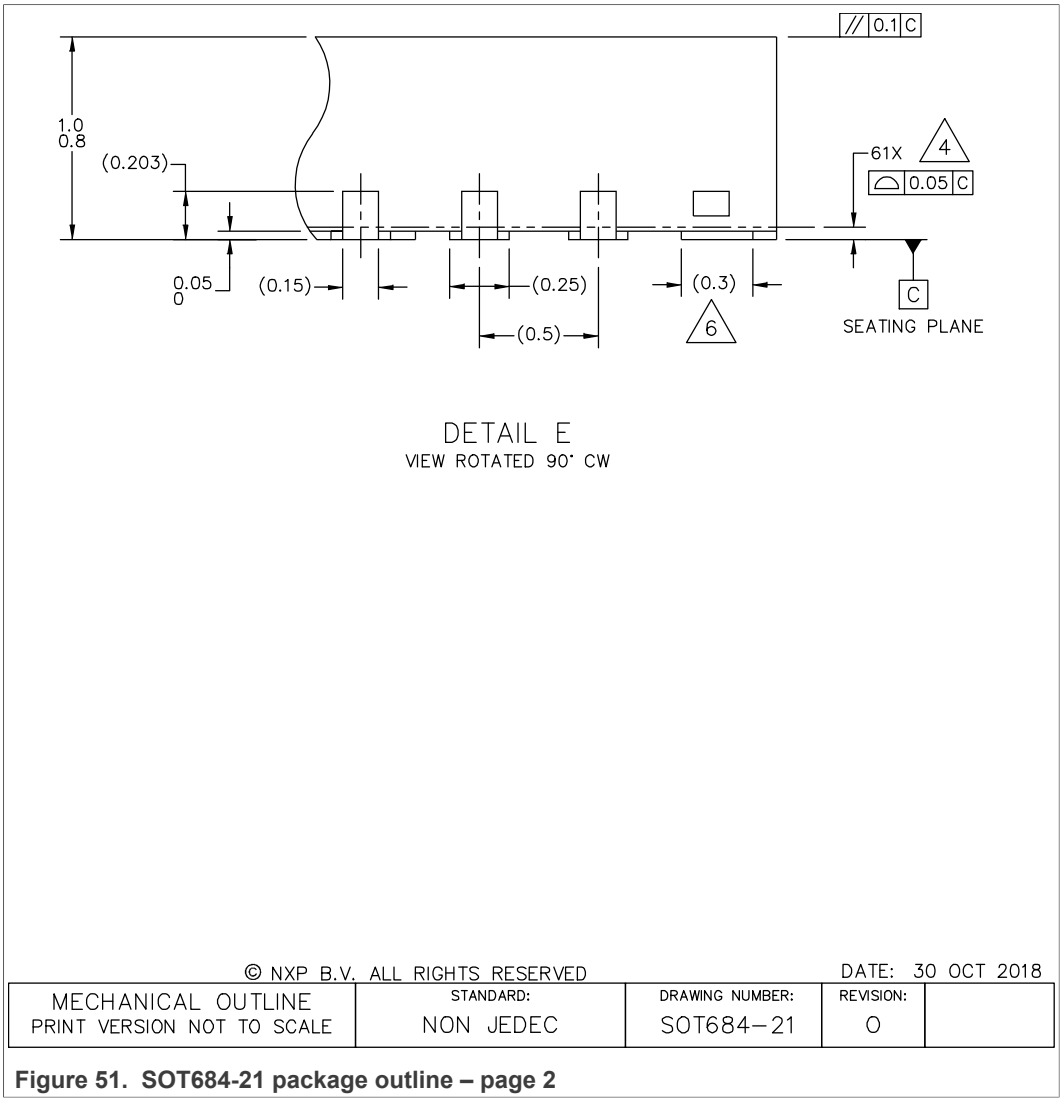


Figure 51. SOT684-21 package outline – page 2

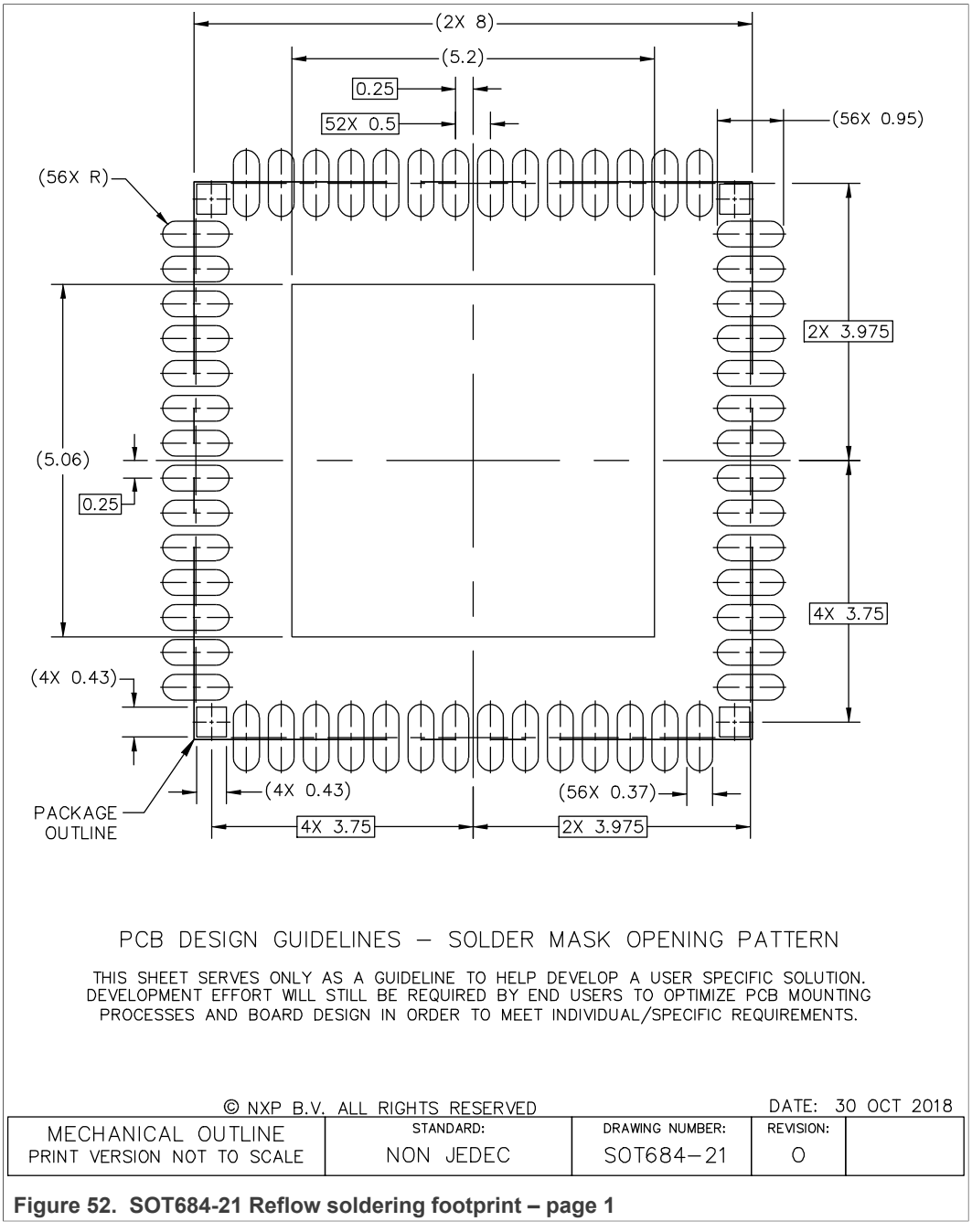


Figure 52. SOT684-21 Reflow soldering footprint – page 1

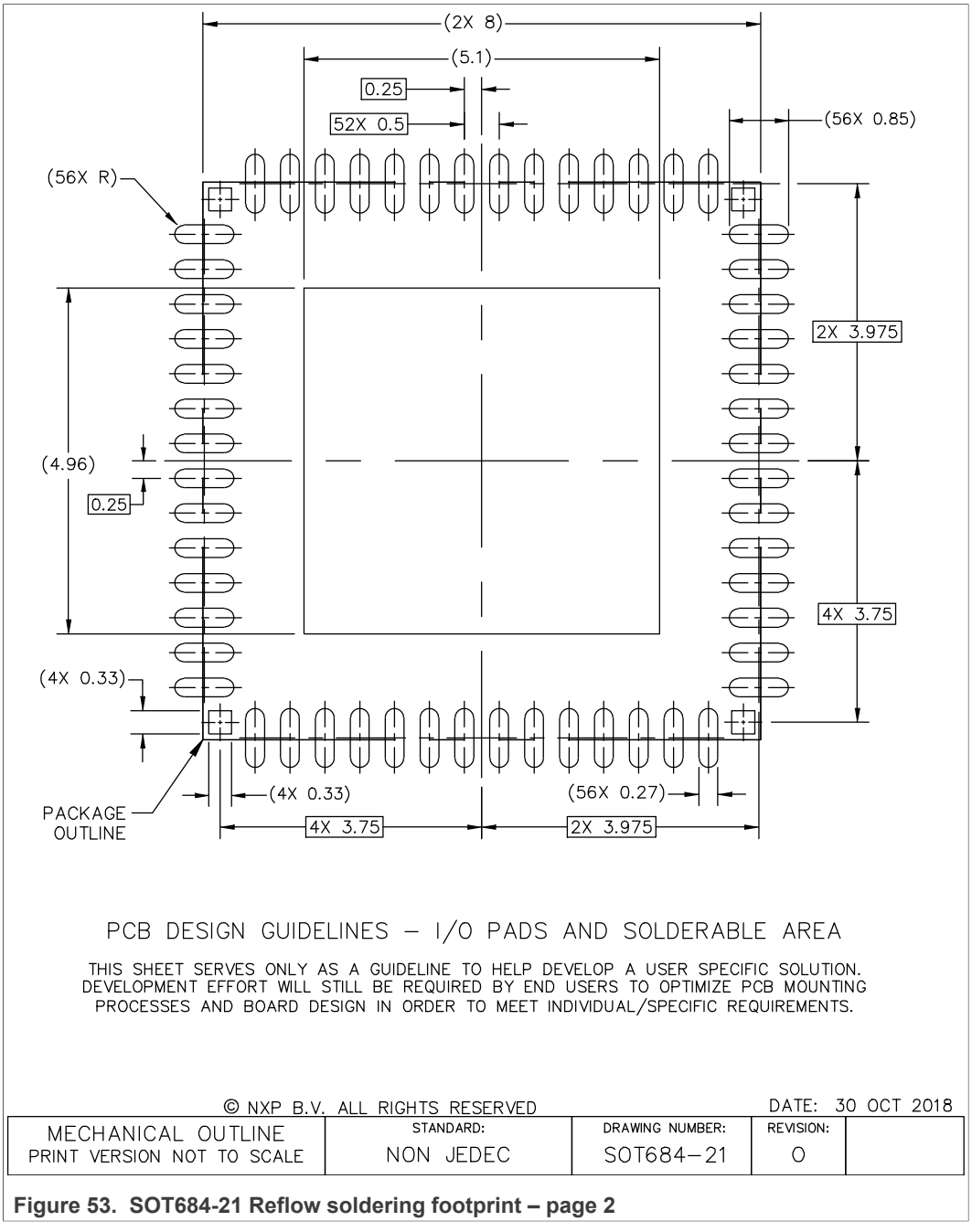


Figure 53. SOT684-21 Reflow soldering footprint – page 2

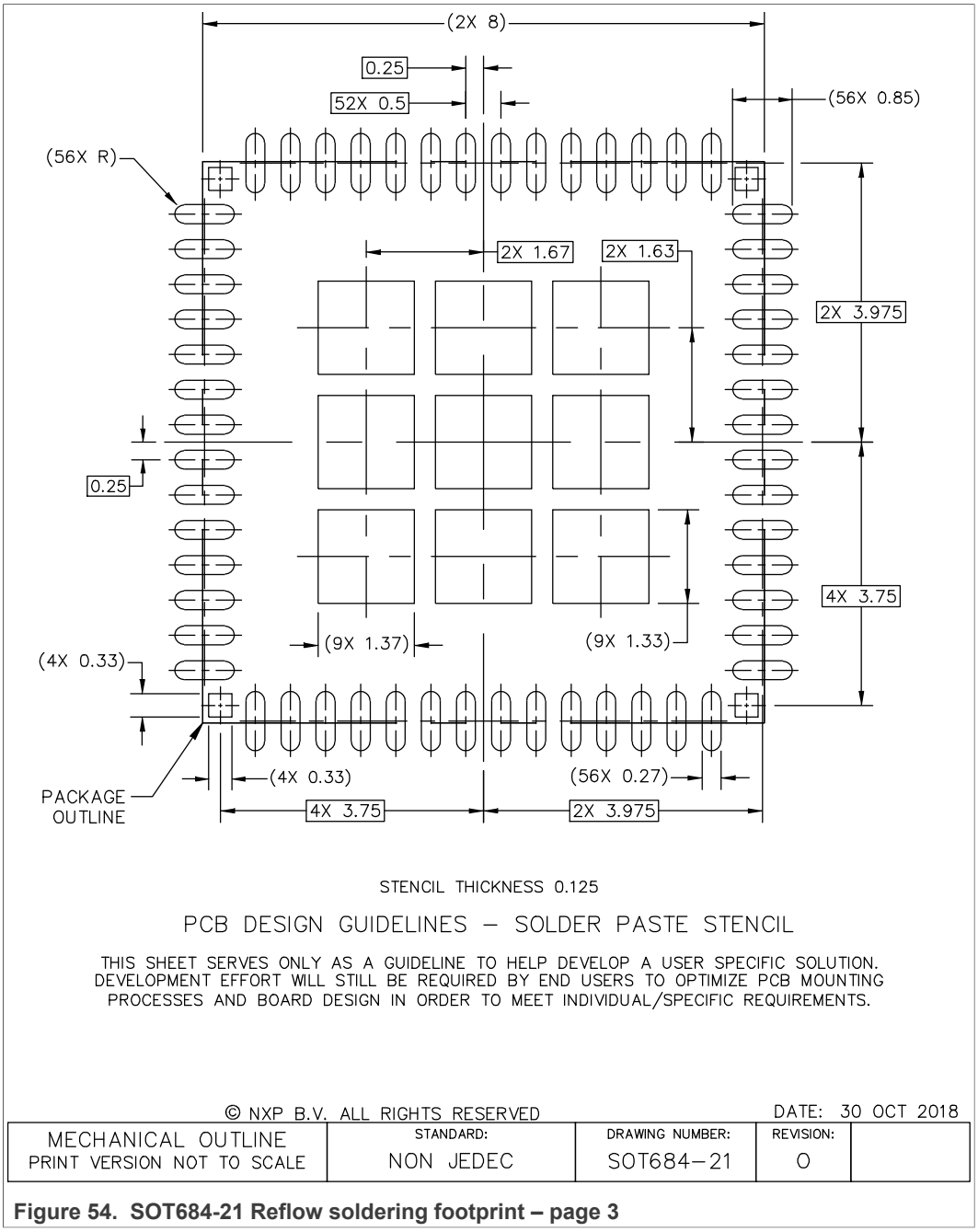


Figure 54. SOT684-21 Reflow soldering footprint – page 3

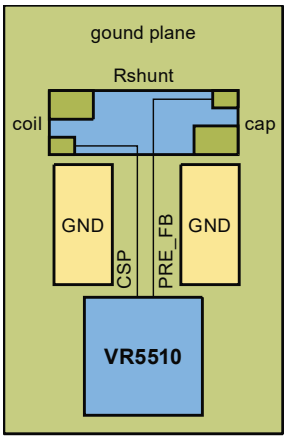
28.3 PCB guidelines

28.3.1 Component selection

- SMPS input and output capacitors must be chosen with low ESR (ceramic or MLCC type of capacitors). X7R ceramic type is preferred. Input decoupling capacitors must be placed as close as possible to the device pin. Output capacitor voltage rating must be selected to be 3x the voltage output value to minimize the DC bias degradation.
- SMPS inductors must be chosen with ISAT higher than maximum inductor peak current.

28.3.2 VPRE

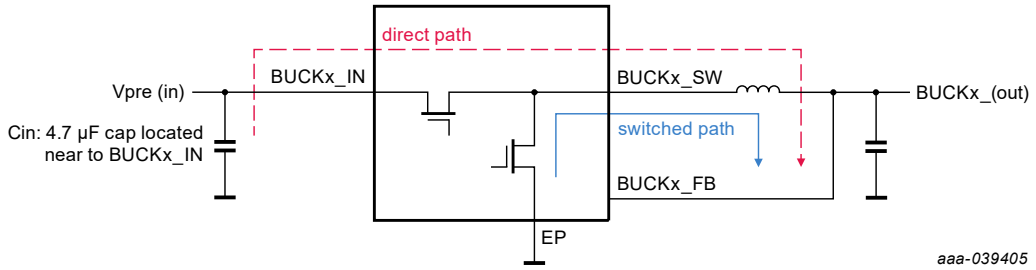
- Inductor charging and discharging current loop must be designed as small as possible.
- Input decoupling capacitors must be placed close to the high-side drain transistor pin.
- The bootstrap capacitor must be placed close to the device pin using wide and short track to connect to the external low-side drain transistor.
- PRE_GLS, PRE_GHS and PRE_SW tracks must be wide and short and should not cross any sensitive signal (current sensing, for example).
- PRE_FB used as voltage feedback AND current sense must be connected to RSHUNT and routed as a pair with CSP:



- The external transistor thermal shape should be in the range of 25 x 25 mm for optimum Rth.
- See LFPAK56 application note for more details: http://assets.nexperia.com/documents/application-note/AN10874.pdf

28.3.3 LVBUCKs

- Inductor charging and discharging current loop must be designed as small as possible:



- Input decoupling capacitors must be placed close to BUCKx_IN pins.

29 References

Table 123. References

Document	Description	URL
VR5510 Safety Manual	Safety manual	Available at DocStore
VR5510 FMEDA	FMEDA	Available at DocStore
VR5510 GUI	NXP GUI for VR5510 (includes OTP and power dissipation tools)	https://www.nxp.com/products/power-management/pmics-and-sbcs/pmics/multi-channel-9-pmic-for-s32g-processor-8-high-power-1-low-power-fit-for-asil-d-safety-level:VR5510?tab=Design_Tools_Tab
AN13118	VR5510 S32G Safety Concept	https://www.nxp.com/docs/en/application-note/AN13118.pdf
AN12880	VR5510 Low Power Standby Mode	https://www.nxp.com/docs/en/application-note/AN12880.pdf

30 Revision History

Table 124. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
VR5510 v.4	20211006	Product data sheet	202109034I	VR5510 v.3
Modifications	• Section 1 – First paragraph - Changed to "...focuses on Gateway, In-Vehicle Networks, Domain controllers, Telematics and V2X Communications. " from "...focuses on Gateway, ADAS, V2X, and Infotainment applications. • Section 4 – Changed to "In-Vehicle Networks" from "Infotainment" – Changed to "Domain controllers" from "ADAS" – Changed to "Telematics" from "Clusters" – Changed to "V2X Communications" from "V2x" – Deleted "Radio" and "Vision" • Figure 4 – Changed to "See Section 10.1" from "V_{PRE_UVL} + R x I_{PRE}" • Table 5 – Added "$R_{\theta JC\_BOTTOM}$" and associated values – Added "$R_{\theta JC\_TOP}$" and associated values • Figure 5 – Changed note to "Those conditions will not apply if PSYNC/PWRON2, OTP disabled and VSUP > VSUP_UV" from "Those conditions will not apply if PSYNC/PWRON2 are OTP disabled" – In two places, changed to "RSTB_DUR" from "RSTB delay expired" • Figure 7 – Changed to "VBOSUVH" from "VBOS_uvh" • Table 9 – Deleted "V_{BOS_POR}" and associated values • Section 10.1 – Changed to "The output voltage is configurable by OTP from 3.3 V to 5.2 V" from "The output voltage is configurable by OTP from 3.3 V to 5.3 V" – Changed to "V_{PRE_UVH}, V_{PRE_UVL}, and $V_{PRE\_FB\_OV}$ thresholds..." from "V_{PRE_UVH}, V_{PRE_UVL}, and V_{PREOV2} thresholds..." • Section 10.3 – Deleted "Calculation guidelines, Use case calculation..., Use case stability verification, and associated list items – Deleted Figure 14, Phase and gain margin simulation – Deleted Figure 15, Transient response simulation – Added Table 10		

Table 124. Revision history...*continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
	• Table 11 – Changed to "V_{TON}" from "V_{PRE_START}" and deleted "(Softstart ramp = 2 mV/µs, VPRE = 5 V)" from the same row – VPRESC, Added rows with the following Min values: 57.8, 94, and 352.8 • Table 13 – Deleted "VR5100 Parameters" and associated values • Section 11.1 – Changed to "...(CFG_BOOST_ 1_OTP register) from 4.5 V to 6 V." from "...(CFG_BOOST_ 1_OTP register) from 4.5 V to 5.74 V." – Table 15, Deleted "5 V" and associated values • Table 17 – I_{BUCK12_Q}, Changed parameter to "Quiescent Current, PFM Mode, VSUP = 12 V" from "Quiescent Current, PFM Mode" – C_{OUT_BUCK12}, Changed Min to "35" from "44" – C_{IN_BUCK12}, Changed Min to "4.23" from "4.7" • Table 19 – I_{BUCK3_Q}, Changed parameter to "Quiescent Current, PFM Mode, VSUP = 12 V" from "Quiescent Current, PFM Mode" – C_{OUT_BUCK3}, Changed Min to "35" from "44" – C_{IN_BUCK3}, Changed Min to "4.23" from "4.7" • Table 21 – I_{LDO1_Q}, Changed parameter to "Quiescent Current, No load, VSUP = 12 V" from "Quiescent Current, No load" – $C_{OUT\_LDO1\_150}$, Changed to "Effective output capacitor, 150 mA current capability" from "Output capacitor, 150 mA current capability" and changed Min to "3" from "4.7" and changed Max to "100" from "—" – $C_{OUT\_LDO1\_400}$, Changed to "Effective output capacitor, 400 mA current capability" from "Output capacitor, 400 mA current capability" and changed Min to "4.5" from "6.8" and changed Max to "100" from "—" • Table 22 – I_{LDO23_Q}, Changed parameter to "Quiescent Current, No load, VSUP = 12 V" from "Quiescent Current, No load" – C_{OUT_LDO23}, Changed Min to "3.3" from "4.7" and changed Max to "100" from "—" • Section 16.3 – C_{OUT_HVLDO}, Changed Min to "2.2" from "4.7" • Table 24 – Added " (± 10°C)" to "Threshold" header • Table 29 – FIN_{RANGE}, (FIN_DIV I2C configuration), Changed units to "MHz" from "kHz" • Table 32 – $PWRON1_{VIL}$, Changed Min to "—" from "3.25" and Max to "2.7" from "—" – $PWRON2_{VIL}$, Changed Min to "—" from "1" and Max to "0.7" from "—" – $PWRON1_{VIH}$, Changed Min to "3.5" from "—" and Max to "—" from "3" – $PWRON2_{VIH}$, Changed Min to "1.15" from "—" and Max to "—" from "0.85" • Table 120 – Address 19, Value 100000, Changed to "504 mV/µs" from "655.2 mV/µs" – Address 2B, Changed to "VPRE Internal Reference soft start ramp" from "VPRE soft start ramp" – Address 2B, Value 0, Added "(VPRE will ramp up in 1 ms for 3.3 V setting)" – Address 2B, Value 1, Added "(VPRE will ramp up in 500 µms for 3.3 V setting)"		
VR5510 v.3	20210303	Product data sheet	NA	VR5510 v.2
VR5510 v.2	20201222	Product data sheet	NA	VR5510 v.1
VR5510 v.1	20201117	Product data sheet	**NA**	NA

31 Legal information

31.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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