NXP Semiconductors
Data Sheet

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MWCT1213VLH/AVLH/VLL DS

Features

- Compliant with the latest version Wireless Power Consortium (WPC) Qi V1.2.4 power class 0 specification power transmitter design and can be designed for V1.3 with authentication.
- Supports wide transmitter DC input voltage range of 5V to 24V.
- Integrated digital demodulation.
- Supports two-way communication, transmitter to receiver by FSK and receiver to transmitter by ASK.
- Supports Q factor detection and calibrated power loss based Foreign Object Detection (FOD) framework
- Supports low standby power.
- Uses rail voltage control, phase shift control or duty cycle control with the fixed operation frequency to alleviate EMI in the EMI sensitive system.
- Supports operation frequency dithering technology to minimize the peak emissions at specific frequencies.
- Supports CAN/IIC/SCI/SPI interfaces.
- LED for system status indication.
- Over-voltage/current/temperature protection.
- Software based solution to provide maximum design freedom and product differentiation.
- Supported two EPP RXs for WCT1213VLH, and an additional watch for WCT1213VLL.
- MWCT1213AVLH qualified to AEC100 Test Group A&B.

Applications

- Automotive and Industrial and Consumer
- Single coil or multi-coil
- Single Transmitter or Multi Transmitters controlled by the same device
- WPC Baseline and Extended Power Profile compliant (BPP and EPP).
- Customer proprietary protocol

Overview Description

The MWCT1213VLH/AVLH/VLL is a wireless power transmitter controller that integrates all required functions for WPC “Qi” compliant wireless power transmitter design. It is an intelligent device that works with the NXP uses periodically analog PING to detect a mobile device for charging while gaining super low standby power. Once the mobile device is detected, the MWCT1213VLH/AVLH/VLL controls the power transfer by adjusting the rail voltage, the phase shift, or the duty cycle of the power stage according to message packets sent by the mobile device.

To maximize the design freedom and product differentiation, the MWCT1213VLH/AVLH/VLL supports the extended power profile industrial/consumer power transmitter design (WPC MP-Ax types or customization) using the fixed operation frequency control methods such as rail voltage control, phase shift control or duty cycle control etc. by software based solution, which can support wireless charging with both extended power profile power receiver and baseline power profile power receiver. In addition, the easy-to-use FreeMASTER GUI tool has configuration, calibration and debugging functions to provide the user-friendly design experience and reduce time-to-market.

The MWCT1213VLH/AVLH/VLL includes 2 digital demodulation modules to reduce the external components, 2 FSK modulation modules to support two-way communication, protection module to handle the over-voltage/current/temperature protection, FOD module to protect from overheating by misplaced metallic foreign objects for each charging device, and general CAN/IIC/SCI/SPI interfaces for external communications. It also handles any abnormal condition and operational status and provides comprehensive indicator outputs for robust system design.

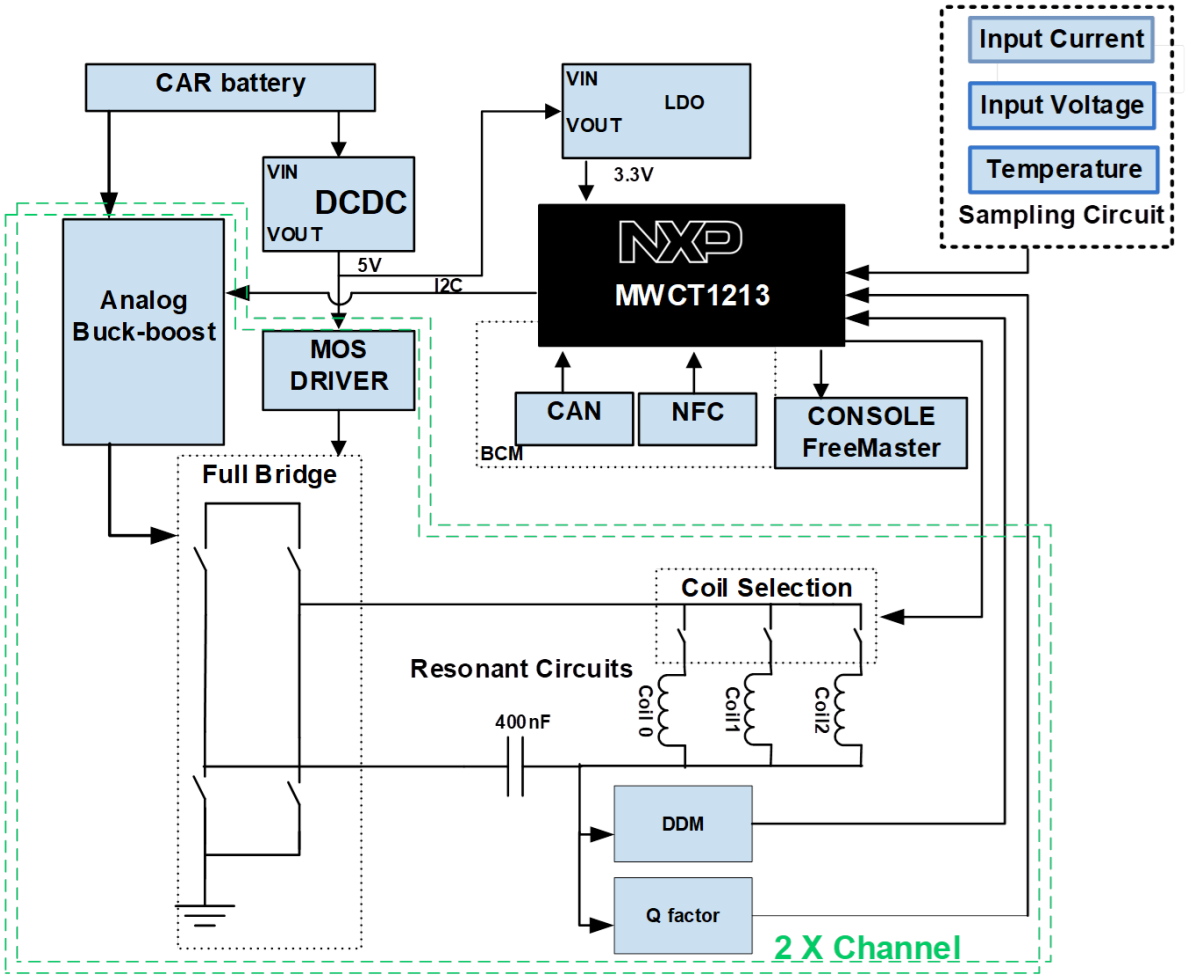

Figure 1. Wireless Charging System Functional Diagram

Contents

1 Absolute Maximum Ratings

1.1 Electrical operating ratings

Table 1. Absolute maximum electrical ratings (V_{SS} = 0 V, V_{SSA} = 0 V)

Characteristic	Symbol	Notes[1]	Min.	Max.	Unit
Supply Voltage Range	V_{DD}	-	-0.3	4.0	V
Analog Supply Voltage Range	V_{DDA}	-	-0.3	4.0	V
ADC High Voltage Reference	V_{REFHx}	-	-0.3	4.0	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}	-	-0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{ss}	-	-0.3	0.3	V
Digital Input Voltage Range	V_{IN}	Pin Group 1	-0.3	5.5	V
$\overline{\text{RESET}}$ Input Voltage Range	V_{IN_RESET}	Pin Group 2	-0.3	4.0	V
Oscillator Input Voltage Range	V_{OSC}	Pin Group 4	-0.4	4.0	V
Analog Input Voltage Range	V_{INA}	Pin Group 3	-0.3	4.0	V
Input clamp current, per pin ($V_{IN} < V_{SS}$ - 0.3 V)[2, 3]	V_{IC}	-	-	-5.0	mA
Output clamp current, per pin[4]	V_{OC}	-	-	±20.0	mA
Contiguous pin DC injection current—regional limit sum of 16 contiguous pins	I_{Icont}	-	-25	25	mA
Output Voltage Range (normal push-pull mode)	V_{OUT}	Pin Group 1,2	-0.3	4.0	V
Output Voltage Range (open drain mode)	V_{OUTOD}	Pin Group 1	-0.3	5.5	V
$\overline{\text{RESET}}$ Output Voltage Range	V_{OUTOD_RESET}	Pin Group 2	-0.3	4.0	V
DAC Output Voltage Range	V_{OUT_DAC}	Pin Group 5	-0.3	4.0	V
Ambient Temperature	T_A	-	-40	105	°C
Storage Temperature Range	T_{STG}	-	-55	150	°C

1. Default Mode:
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
   - Pin Group 5: DAC analog output
2. Continuous clamp current.
3. All 5 volt tolerant digital I/O pins are internally clamped to V_{SS} through an ESD protection diode. There is no diode connection to V_{DD}. If VIN greater than VDIO_MIN (=V_{SS} -0.3 V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed, then a current limiting resistor is required.
4. I/O is configured as push-pull mode.

1.2 Thermal handling ratings

Table 2. Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	-55	150	°C	1
T_{SDR}	Solder temperature, lead-free	-	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life.*
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.*

1.3 ESD handling ratings

Table 3. ESD handling ratings

Characteristic[1]	Min.	Max.	Unit
ESD for Human Body Model (HBM)	-2000	+2000	V
ESD for Machine Model (MM)	-200	+200	V
ESD for Charge Device Model (CDM)	-500	+500	V
Latch-up current at TA= 85°C (I_{LAT})	-100	+100	mA

1. Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

1.4 Moisture handling ratings

Table 4. Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	-	3	-	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.*

2 Electrical Characteristics

2.1 General characteristics

Table 5. General electrical characteristics

Recommended operating conditions (V_{REFLx} = 0 V, V_{SSA} = 0 V, V_{SS} = 0 V)							
Characteristic	**Symbol**	**Notes**	**Min.**	**Typ.**	**Max.**	**Unit**	**Test conditions**
Supply Voltage[2]	V_{DD} ,V_{DDA}	-	2.7	3.3	3.6	V	-
ADC (Cyclic) Reference Voltage High	V_{REFHA} V_{REFHB}	-	3.0	-	V_{DDA}	V	-
ADC (SAR) Reference Voltage High	V_{REFHC}	-	2.0	-	V_{DDA}	V	-
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}	-	-0.1	0	0.1	V	-
Voltage difference V_{SS} to V_{SSA}	ΔV_{ss}	-	-0.1	0	0.1	V	-
Input Voltage High (digital inputs)	V_{IH}	1 (Pin Group 1)	0.7×V_{DD}	-	5.5	V	-
$\overline{\text{RESET}}$ Voltage High	V_{IH_RESET}	1 (Pin Group 2)	0.7×V_{DD}	-	V_{DD}	V	-
Input Voltage Low (digital inputs)	V_{IL}	1 (Pin Group 1,2)	-	-	0.35×V_{DD}	V	-
Oscillator Input Voltage High XTAL driven by an external clock source	V_{IHOSC}	1 (Pin Group 4)	2.0	-	V_{DD} + 0.3	V	-
Oscillator Input Voltage Low	V_{ILOSC}	1 (Pin Group 4)	-0.3	-	0.8	V	-
Output Source Current High (at V_{OH} min.) [4,5] • Programmed for low drive strength • Programmed for high drive strength	I_{OH}	1 (Pin Group 1) 1 (Pin Group 1)	- -	-	-2 -9	mA	-
Output Source Current Low (at V_{OL} max.) [4,5] • Programmed for low drive strength • Programmed for high drive strength	I_{OL}	1 (Pin Group 1,2) 1 (Pin Group 1,2)	- -	-	2 9	mA	-

Output Voltage High	V_{OH}	1 (Pin Group 1)	V_{DD} - 0.5	-	-	V	$I_{OH} = I_{OHmax}$
Output Voltage Low	V_{OL}	1 (Pin Group 1,2)	-	-	0.5	V	$I_{OL} = I_{OLmax}$
Digital Input Current High pull-up enabled or disabled	I_{IH}	1 (Pin Group 1)	-	0	+/-2.5	µA	V_{IN} = 2.4 V to 5.5 V
		1 (Pin Group 2)					V_{IN} = 2.4 V to V_{DD}
Comparator Input Current High	I_{IHC}	1 (Pin Group 3)	-	0	+/-2	µA	$V_{IN} = V_{DDA}$
Oscillator Input Current High	I_{IHOSC}	1 (Pin Group 4)	-	0	+/-2	µA	$V_{IN} = V_{DDA}$
Internal Pull-Up Resistance	$R_{Pull-Up}$	-	20	-	50	kΩ	-
Internal Pull-Down Resistance	$R_{Pull-Down}$	-	20	-	50	kΩ	-
Comparator Input Current Low	I_{ILC}	1 (Pin Group 3)	-	0	+/-2	µA	V_{IN} = 0V
Oscillator Input Current Low	I_{ILOSC}	1 (Pin Group 4)	-	0	+/-2	µA	V_{IN} = 0V
DAC Output Voltage Range	V_{DAC}	1 (Pin Group 5)	V_{SSA} + 0.04	-	V_{DDA} - 0.04	V	R_{LD} = 3 kΩ, C_{LD} = 400 pF
Output Current[1] High Impedance State	I_{OZ}	1 (Pin Group 1,2)	-	0	+/-1	µA	-
Schmitt Trigger Input Hysteresis	V_{HYS}	1 (Pin Group 1,2)	0.06×V_{DD}	-	-	V	-
Input capacitance	C_{IN}	-	-	10	-	pF	-
Output capacitance	C_{OUT}	-	-	10	-	pF	-
GPIO pin interrupt pulse width[6]	T_{INT_Pulse}	7	1.5	-	-	Bus clock	-
Port rise and fall time (high drive strength). Slew disabled.	$T_{Port\_H\_DIS}$	8	5.5	-	15.1	ns	2.7 ≤ VDD ≤ 3.6 V
Port rise and fall time (high drive strength). Slew enabled.	$T_{Port\_H\_EN}$	8	1.5	-	6.8	ns	2.7 ≤ VDD ≤ 3.6 V
Port rise and fall time (low drive strength). Slew disabled.	$T_{Port\_L\_DIS}$	9	8.2	-	17.8	ns	2.7 ≤ VDD ≤ 3.6 V
Port rise and fall time (low drive strength). Slew enabled.	$T_{Port\_L\_EN}$	9	3.2	-	9.2	ns	2.7 ≤ VDD ≤ 3.6 V
Device (system and core) clock frequency	f_{SYSCLK}	-	0	-	100	MHz	-
Bus clock	f_{BUS}	10	-	-	100	MHz	-

1. Default Mode
    - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
    - Pin Group 2: $\overline{\text{RESET}}$
    - Pin Group 3: ADC and Comparator Analog Inputs
    - Pin Group 4: XTAL, EXTAL
    - Pin Group 5: DAC analog output
2. ADC (Cyclic) specifications are not guaranteed when VDDA is below 3.0 V.
3. Total chip source or sink current cannot exceed 75 mA.
4. Contiguous pin DC injection current of regional limit—including sum of negative injection currents or sum of positive injection currents of 16 contiguous pins—is 25 mA.
5. Applies to a pin only when it is configured as GPIO and configured to cause an interrupt by appropriately programming GPIOn_IPOLR and GPIOn_IENR.
6. The greater synchronous and asynchronous timing must be met.
7. 75 pF load
8. 15 pF load

2.2 Device characteristics

Table 6. General device characteristics

Power mode transition Behavior					
Symbol	**Description**	**Min.**	**Max.**	**Unit**	**Notes**
T_{POR}	After a POR event, the amount of delay from when VDD reaches 2.7 V to when the first instruction executes (over the operating temperature range).	199	225	µs	-
T_{S2R}	STOP mode to RUN mode	6.79	7.27	µs	1
$T_{LPS2LPR}$	LPS mode to LPRUN mode	240.9	551	µs	2
$T_{VLPS2VLPR}$	VLPS mode to VLPRUN mode	1424	1459	µs	4
T_{W2R}	WAIT mode to RUN mode	0.57	0.62	µs	3
$T_{LPW2LPR}$	LPWAIT mode to LPRUN mode	237.2	554	µs	2
$T_{VLPW2VLPR}$	VLPWAIT mode to VLPRUN mode	1413	1500	µs	4
Power consumption operating behaviors					
Mode	**Conditions**	**Max. frequency**	**Typical at 3.3 V, 25 °C**		**Notes**
			I_{DD}	**I_{DDA}**	

RUN2	100 MHz[5] core and peripheral clock, regulators are in full regulation, relaxation oscillator on, PLL powered on, continuous MAC instructions with fetches from program Flash, all peripheral modules enabled, TMRs and SCIs using 1× peripheral clock, NanoEdge within eFlexPWM using 2× peripheral clock, ADC/DAC (only one 12-bit DAC and all 6-bit DACs) powered on and clocked, comparator powered on, all ports configured as inputs with input low and no DC loads	100 MHz[5]	63.7 mA	16.7 mA	5
WAIT	100 MHz[5] core and peripheral clock, regulators are in full regulation, relaxation oscillator on, PLL powered on, core in WAIT state, all peripheral modules enabled, TMRs and SCIs using 1× clock, NanoEdge within eFlexPWM using 2× clock, ADC/DAC (one 12-bit DAC, all 6-bit DACs)/comparator powered off, all ports configured as inputs with input low and no DC loads	100 MHz[5]	43.5 mA	-/-	5
STOP	4 MHz core and peripheral clock, regulators are in full regulation, relaxation oscillator on, PLL powered off, core in STOP state, all peripheral module and core clocks are off, ADC/DAC/Comparator powered off, all ports configured as inputs with input low and no DC loads	4 MHz	10.1 mA	-/-	5
LPRUN	200 kHz core and peripheral clock from relaxation oscillator's low speed clock, relaxation oscillator in standby mode, regulators are in standby, PLL disabled, repeat NOP instructions, all peripheral modules enabled, except NanoEdge within eFlexPWM and cyclic ADCs, one 12-bit DAC and all 6-bit DACs enabled, simple loop with running from platform instruction buffer, all ports configured as inputs with input low and no DC loads	2 MHz	2.3 mA	2.73 mA	5
LPWAIT	200 kHz core and peripheral clock from relaxation oscillator's low speed clock, relaxation oscillator in standby mode, regulators are in standby, PLL disabled, all peripheral modules enabled, except NanoEdge within eFlexPWM and cyclic ADCs, one 12-bit DAC and all 6-bit DACs enabled, core in WAIT mode, all ports configured as inputs with input low and no DC loads	2 MHz	2.29 mA	2.73 mA	5

LPSTOP	200 kHz core and peripheral clock from relaxation oscillator's low speed clock, relaxation oscillator in standby mode, regulators are in standby, PLL disabled, only PITs and COP enabled, other peripheral modules disabled and clocks gated off, core in STOP mode, all ports configured as inputs with input low and no DC loads	2 MHz	1.55 mA	-	5
VLPRUN	32 kHz core and peripheral clock from a 64 kHz external clock source, oscillator in power down, all relaxation oscillators disabled, large regulator is in standby, small regulator is disabled, PLL disabled, repeat NOP instructions, all peripheral modules, except COP and EWM, disabled and clocks gated off, simple loop running from platform instruction buffer, all ports configured as inputs with input low and no DC loads	200 kHz	1.18 mA	-/-	5
VLPWAIT	32 kHz core and peripheral clock from a 64 kHz external clock source, oscillator in power down, all relaxation oscillators disabled, large regulator is in standby, small regulator is disabled, PLL disabled, all peripheral modules, except COP, disabled and clocks gated off, core in WAIT mode, all ports configured as inputs with input low and no DC loads	200 kHz	1.1 mA	-/-	5
VLPSTOP	32 kHz core and peripheral clock from a 64 kHz external clock source, oscillator in power down, all relaxation oscillators disabled, large regulator is in standby, small regulator is disabled, PLL disabled, all peripheral modules, except COP, disabled and clocks gated off, core in STOP mode, all ports configured as inputs with input low and no DC loads	200 kHz	1.03 mA	-/-	5

Reset and interrupt timing

Symbol	Characteristic	Min.	Max.	Unit	Notes
t_{RA}	Minimum $\overline{\text{RESET}}$ Assertion Duration	16	-	ns	6
t_{RDA}	$\overline{\text{RESET}}$ desertion to First Address Fetch	865 × T_{OSC} + 8 × T_{SYSCLK}	-	ns	7
t_{IF}	Delay from Interrupt Assertion to Fetch of first instruction (exiting STOP mode)	361.3	570.9	ns	-

PMC Low-Voltage Detection (LVD) and Power-On Reset (POR) parameters

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{POR_A}	POR Assert Voltage[8]	-	2.0	-	V

V_{POR_R}	POR Release Voltage[9]	-	2.7	-	V
V_{LVI_2p7}	LVI_2p7 Threshold Voltage	-	2.73	-	V
V_{LVI_2p2}	LVI_2p2 Threshold Voltage	-	2.23	-	V

JTAG timing

Symbol	Description	Min.	Max.	Unit	Notes
f_{OP}	TCK frequency of operation	DC	f_{SYSCLK}/16	MHz	10
t_{PW}	TCK clock pulse width	50	-	ns	-
t_{DS}	TMS, TDI data set-up time	5	-	ns	-
t_{DH}	TMS, TDI data hold time	5	-	ns	-
t_{DV}	TCK low to TDO data valid	-	30	ns	-
t_{TS}	TCK low to TDO tri-state	-	30	ns	-

Regulator 1.2 V parameters

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{CAP}	Output Voltage[11]	-	1.22	-	V
I_{SS}	Short Circuit Current[12]	-	600	-	mA
T_{RSC}	Short Circuit Tolerance (V_{CAP} shorted to ground)	-	-	30	Mins
V_{REF}	Reference Voltage (after trim)	-	1.21	-	V

External clock timing

Symbol	Characteristic	Min.	Typ.	Max.	Unit
f_{OSC}	Frequency of operation (external clock driver)	-	-	50	MHz
t_{PW}	Clock pulse width[13]	8	-	-	ns
t_{rise}	External clock input rise time[14]	-	-	1	ns
t_{fall}	External clock input fall time[15]	-	-	1	ns
V_{ih}	Input high voltage overdrive by an external clock	$0.85 \times V_{DD}$	-	-	V
V_{il}	Input low voltage overdrive by an external clock	-	-	$0.3 \times V_{DD}$	V

Phase-Locked Loop (PLL) timing

Symbol	Characteristic	Min.	Typ.	Max.	Unit
f_{Ref_PLL}	PLL input reference frequency[16]	8	8	16	MHz
f_{OP_PLL}	PLL output frequency[17]	240	-	400	MHz
t_{Lock_PLL}	PLL lock time[18]	35.5	-	73.2	µs
t_{DC_PLL}	Allowed Duty Cycle of input reference	40	50	60	%

External crystal or resonator specifications					
Symbol	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Unit**
f_{XOSC}	Frequency of operation	4	8	16	MHz
Relaxation oscillator electrical specifications					
Symbol	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Unit**
f_{ROSC_8M}	8 MHz Output Frequency[20] RUN Mode • 0 °C to 105 °C • -40 °C to 105 °C Standby Mode (IRC trimmed @ 8 MHz) • -40 °C to 105 °C	 7.84 7.76 -	 8 8 405	 8.16 8.24 -	 MHz MHz kHz
$f_{ROSC\_8M\_Delta}$	8 MHz Frequency Variation over 25 °C RUN Mode Due to temperature • 0 °C to 105 °C • -40 °C to 105 °C	 - -	 +/-1.5 +/-1.5	 +/-2 +/-3	 % %
f_{ROSC_32k}[19,20]	32 kHz Output Frequency[19,21] RUN Mode • -40 °C to 105 °C	 30.1	 32	 33.9	 kHz
$f_{ROSC\_32k\_Delta}$[19,20]	32 kHz Output Frequency Variation over 25 °C[19,21] RUN Mode Due to temperature • 0 °C to 85 °C • -40 °C to 105 °C[22]	 - -	 +/-1.5 +/-1.5 (2.5)	 +/-2 +/-3 (4)	 % %
t_{Stab}	Stabilization Time • 8 MHz output[23] • 32 kHz output[19,24]	 - -	 0.12 14.4	 - -	 µs µs
t_{DC_ROSC}	Output Duty Cycle	48	50	52	%
Flash specifications					
Symbol	**Description**	**Min.**	**Typ.**	**Max.**	**Unit**
t_{hvpgm4}	Longword Program high-voltage time	-	7.5	18	µs
$t_{hversscr}$	Sector Erase high-voltage time[25]	-	13	113	ms
$t_{hversall}$	Erase All high-voltage time[25,26]	-	52	452	ms
$t_{hversblk32k}$	Erase Block high-voltage time for 32 KB[25,27]	-	52	452	ms
$t_{hversblk256k}$	Erase Block high-voltage time for 256 KB[25,27]	-	104	904	ms
$t_{rd1sec1k/2k}$	Read 1s Section execution time (flash sector)[28]	-	-	60	µs

	Read 1s Block execution time[27]				
$t_{rd1blk32k}$	• 32 KB FlexNVM	-	-	0.5	ms
$t_{rd1blk256k}$	• 256 KB program Flash	-	-	1.7	ms
t_{pgmchk}	Program Check execution time[28]	-	-	45	µs
t_{rdrsrc}	Read Resource execution time[28]	-	-	30	µs
t_{pgm4}	Program Longword execution time	-	65	145	µs
t_{ersscr}	Erase Flash Sector execution time[29]	-	14	114	ms
	Erase Flash Block execution time[27,29]				
$t_{ersblk32k}$	• 32 KB FlexNVM	-	55	465	ms
$t_{ersblk256k}$	• 256 KB program Flash	-	122	985	ms
	Program Section execution time[27]				
$t_{pgmsec512p}$	• 512 B program Flash	-	2.4	-	ms
$t_{pgmsec512n}$	• 512 B FlexNVM	-	4.7	-	ms
$t_{pgmsec1kp}$	• 1 KB program Flash	-	4.7	-	ms
$t_{pgmsec1kn}$	• 1 KB FlexNVM	-	9.3	-	ms
t_{rd1all}	Read 1s All Blocks execution time	-	-	0.9/1.8[30]	ms
t_{rdonce}	Read Once execution time[28]	-	-	25	µs
$t_{pgmonce}$	Program Once execution time	-	65	-	µs
t_{ersall}	Erase All Blocks execution time[29]	-	70/175[30]	575/1500[30]	ms
t_{vfykey}	Verify Backdoor Access Key execution time[28]	-	-	30	µs
$t_{pgmpart32k}$	Program Partition for EEPROM execution time for 32 KB FlexNVM[27]	-	70	-	ms
	Set FlexRAM Function execution time[27]				
$t_{setramff}$	• Control Code 0xFF	-	50	-	µs
$t_{setram8k}$	• 8 KB EEPROM backup	-	0.3	0.5	ms
$t_{setram32k}$	• 32 KB EEPROM backup	-	0.7	1.0	ms
$t_{eewr8bers}$	Byte-write to erased FlexRAM location execution time[27,31]	-	175	260	µs
	Byte-write to FlexRAM execution time[27]				
$t_{eewr8b8k}$	• 8 KB EEPROM backup	-	340	1700	µs
$t_{eewr8b16k}$	• 16 KB EEPROM backup	-	385	1800	µs
$t_{eewr8b32k}$	• 32 KB EEPROM backup	-	475	2000	µs
$t_{eewr16bers}$	Word-write to erased FlexRAM location execution time[27]	-	175	260	µs
	Word-write to FlexRAM execution time[27]				
$t_{eewr16b8k}$	• 8 KB EEPROM backup	-	340	1700	µs
$t_{eewr16b16k}$	• 16 KB EEPROM backup	-	385	1800	µs
$t_{eewr16b32k}$	• 32 KB EEPROM backup	-	475	2000	µs
$t_{eewr32bers}$	Longword-write to erased FlexRAM location execution time[27]	-	360	540	µs

$t_{eewr32b8k}$ $t_{eewr32b16k}$ $t_{eewr32b32k}$	Longword-write to FlexRAM execution time[27] • 8 KB EEPROM backup • 16 KB EEPROM backup • 32 KB EEPROM backup	- - -	545 630 810	1950 2050 2250	µs µs µs
$t_{flashret10k}$	Data retention after up to 10 K cycles	5	50[32]	-	years
$t_{flashret1k}$	Data retention after up to 1 K cycles	20	100[32]	-	years
$n_{flashcyc}$	Cycling endurance[33]	10 K	50 K[32]	-	cycles
$t_{eeret100}$	Data retention up to 100% of write endurance[27]	5	50[32]	-	years
$t_{eeret10}$	Data retention up to 10% of write endurance[27]	20	100[32]	-	years
	Write endurance[27,34]				
n_{eewr16}	• EEPROM backup to FlexRAM ratio = 16	35 K	175 K	-	writes
$n_{eewr128}$	• EEPROM backup to FlexRAM ratio = 128	315 K	1.6 M	-	writes
$n_{eewr512}$	• EEPROM backup to FlexRAM ratio = 512	1.27 M	6.4 M	-	writes
n_{eewr4k}	• EEPROM backup to FlexRAM ratio = 4096	10 M	50 M	-	writes
n_{eewr8k}	• EEPROM backup to FlexRAM ratio = 8192	20 M	100 M	-	writes

12-bit cyclic ADC electrical specifications

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage[35]	3.0	3.3	3.6	V
V_{REFHX}	V_{REFH} supply voltage[36]	V_{DDA} - 0.6	-	V_{DDA}	V
f_{ADCCLK}	ADC conversion clock[37]	0.6	-	20	MHz
R_{ADC}	Conversion range[38] • Fully differential[26] • Single-ended/unipolar	 -(V_{REFH} - V_{REFL}) V_{REFL}	 - -	 V_{REFH} - V_{REFL} V_{REFH}	 V V
V_{ADCIN}	Input voltage range (per input)[39] • External Reference • Internal Reference	 V_{REFL} V_{SSA}	 - -	 V_{REFH} V_{DDA}	 V V
t_{ADC}	Conversion time[40]	-	6	-	t_{ADCCLK}
t_{ADCPU}	ADC power-up time (from adc_pdn)	-	13	-	t_{ADCCLK}

I_{ADCRUN}	ADC RUN current (per ADC block)[26] ADC RUN current (per ADC block)[27] • at 600 kHz ADC clock, LP mode • ⩽ 8.33 MHz ADC clock, 00 mode • ⩽ 12.5 MHz ADC clock, 01 mode • ⩽ 16.67 MHz ADC clock, 10 mode • ⩽ 20 MHz ADC clock, 11 mode	- - - - - -	1.8 1 5 9 15 19	- - - - - -	mA mA mA mA mA mA
$I_{ADPWRDWN}$	ADC power down current (adc_pdn enabled)[41]	-	0.02	-	µA
I_{VREFH}	V_{REFH} current (in external mode)[42]	-	0.001	-	µA
INL_{ADC}	Integral non-linearity[43]	-	+/- 1.5 (3)	+/- 2.2 (5)	LSB[44]
DNL_{ADC}	Differential non-linearity[43]	-	+/- 0.5 (0.6)	+/- 0.8 (1)	LSB[44]
V_{OFFSET}	Offset[45] • Fully differential[26] • Single ended/Unipolar[46]	 - -	 +/- 8 +/- 12 (13.7)	 - -	 mV mV
E_{GAIN}	Gain Error	- -	0.996 to 1.004[26] 0.801 to 0.809[27]	0.99 to 1.101[26] 0.798 to 0.814[27]	- -
ENOB	Effective number of bits[47]	-	10.6/9.5	-	bits
I_{INJ}	Input injection current[48]	-	-	+/-3	mA
C_{ADCI}	Input sampling capacitance	-	4.8	-	pF

16-bit SAR ADC electrical specifications[27]

Symbol	Characteristic	Min.	Typ.[49]	Max.	Unit
V_{DDA}	Supply voltage	2.7	-	3.6	V
ΔV_{DDA}	Supply voltage delta to V_{DD}	- 0.1	0	+ 0.1	V
ΔV_{SSA}	Supply voltage delta to V_{SS}	- 0.1	0	+ 0.1	V
V_{REFH}	ADC reference voltage high	V_{DDA}	V_{DDA}	V_{DDA}	V
V_{REFL}	ADC reference voltage low	V_{SSA}	V_{SSA}	V_{SSA}	V
V_{ADIN}	Input voltage range	V_{SSA}	-	V_{DDA}	V
C_{ADIN}	Input capacitance • 16-bit mode • 8-/10-/12-bit mode	 - -	 8 4	 10 5	 pF pF
R_{ADIN}	Input resistance	-	2	5	kΩ
f_{ADCK}	ADC conversion clock frequency[50] • 16-bit mode • 8-/10-/12-bit mode	 2 1	 - -	 12 18	 MHz MHz

C_{rate}	ADC conversion rate without ADC hardware averaging • 16-bit mode • 8-/10-/12-bit mode	 37.037 20.000	 - -	 461.467 818.330	 ksps ksps
I_{DDA_ADC}	Supply current[51]	-	-	1.7	mA
f_{ADACK}	ADC asynchronous clock source • ADLPC = 1, ADHSC = 0 • ADLPC = 1, ADHSC = 1 • ADLPC = 0, ADHSC = 0 • ADLPC = 0, ADHSC = 1	 1.2 3.0 2.4 4.4	 2.4 4.0 5.2 6.2	 3.9 7.3 6.1 9.5	 MHz MHz MHz MHz
INL_{AD}	Integral non-linearity[53] • 16-bit mode • 12-bit mode • < 12-bit modes	 - - -	 +/- 7.0 +/- 1.0 +/- 0.5	 - - 2.7 to + 1.9 - 0.7 to + 0.5	 LSB[52] LSB[52] LSB[52]
DNL_{AD}	Differential non-linearity[53] • 16-bit mode • 12-bit mode • < 12-bit modes	 - - -	 - 1.0 to + 4.0 +/- 0.7 +/- 0.2	 - - - 0.3 to + 0.5	 LSB[52] LSB[52] LSB[52]
E_{FS}	Full-scale error (V_{ADIN} = V_{DDA})[53] • 12-bit mode • < 12-bit modes	 - -	 - 4 - 1.4	 - 5.4 - 1.8	 LSB[52] LSB[52]
E_Q	Quantization error • 16-bit mode • 12-bit mode	 - -	 - 1 to 0 -	 - +/- 0.5	 LSB[52] LSB[52]
ENOB	Effective number of bits[54] 16-bit single-ended mode • Avg = 32 • Avg = 4 12-bit single-ended mode • Avg = 32 • Avg = 4	 12.2 11.4 - -	 13.9 13.1 10.8 10.2	 - - - -	 bits bits bits bits
S_{TEMP}	Temp sensor slope under -40 °C to 105 °C	-	1.715	-	mV/°C
V_{TEMP25}	Temp sensor voltage[55] at 25 °C	-	722	-	mV

12-bit DAC electrical specifications

Symbol	Characteristic	Min.	Typ.	Max.	Unit
t_{SETTLE}	Settling time[56] under R_{LD} = 3 kΩ, C_{LD} = 400 pF	-	1	-	µs

t_{DACPU}	DAC power-up time (from PWRDWN release to valid DACOUT)	-	-	11	µs
INL_{DAC}	Integral non-linearity[58]	-	+/- 3	+/- 4	LSB[57]
DNL_{DAC}	Differential non-linearity[58]	-	+/- 0.8	+/- 0.9	LSB[57]
MON_{DAC}	Monotonicity (> 6 sigma monotonicity, < 3.4 ppm non-monotonicity)	Guaranteed			-
V_{OFFSET}	Offset error[58] (5% to 95% of full range)	-	+ 25	+ 35	mV
E_{GAIN}	Gain error[58] (5% to 95% of full range)	-	+/- 0.5	+/- 1.5	%
V_{OUT}	Output voltage range	V_{SSA} + 0.04	-	V_{DDA} - 0.04	V
SNR	Signal-to-noise ratio	-	85	-	dB
ENOB	Effective number of bits	-	11	-	bits

Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	2.7	-	3.6	V
I_{DDHS}	Supply current, High-speed mode(EN=1, PMODE=1)[59]	-	300/-	-/200	µA
I_{DDLS}	Supply current, Low-speed mode(EN=1, PMODE=0)[59]	-	36/-	-/20	µA
V_{AIN}	Analog input voltage	V_{ss}	-	V_{DD}	V
V_{AIO}	Analog input offset voltage	-	-	20	mV
V_H	Analog comparator hysteresis[60] • CR0[HYSTCTR]=00 • CR0[HYSTCTR]=01 • CR0[HYSTCTR]=10 • CR0[HYSTCTR]=11	- - - -	5 25/10 55/20 80/30	13 48 105 148	mV mV mV mV
V_{CMPOh}	Output high	V_{DD} - 0.5	-	-	V
V_{CMPOl}	Output low	-	-	0.5	V
t_{DHS}	Propagation delay, high-speed mode(EN=1, PMODE=1)[61]	-	-	50	ns
t_{DLS}	Propagation delay, low-speed mode(EN=1, PMODE=0) [61]	-	-	200	ns
t_{DInit}	Analog comparator initialization delay[62]	-	40	-	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	-	7	-	µA
R_{DAC6b}	6-bit DAC reference inputs	V_{DDA}	-	V_{DD}	V
INL_{DAC6b}	6-bit DAC integral non-linearity	-0.5	-	0.5	LSB[63]

DNL_{DAC6b}	6-bit DAC differential non-linearity	-0.3	-	0.3	LSB[63]

PWM timing parameters

Symbol	Characteristic	Min.	Typ.	Max.	Unit
f_{PWM}	PWM clock frequency	-	100	-	MHz
S_{PWMNEP}	NanoEdge Placement (NEP) step size[64,65]	-	312	-	ps
t_{DFLT}	Delay for fault input activating to PWM output deactivated	1	-	-	ns
t_{PWMPU}	Power-up time[66]	-	25	-	µs

Quad timer timing

Symbol	Characteristic	Min.	Max.	Unit	Notes
P_{IN}	Timer input period	$2T_{timer} + 6$	-	ns	67
P_{INHL}	Timer input high/low period	$1T_{timer} + 3$	-	ns	67
P_{OUT}	Timer output period	$2T_{timer} - 2$	-	ns	67
P_{OUTHL}	Timer output high/low period	$1T_{timer} - 2$	-	ns	67

QSPI timing[68]

Symbol	Characteristic	Min.		Max.		Unit
		Master	Slave	Master	Slave	
t_C	Cycle time	60/35	60/35	-	-	ns
t_{ELD}	Enable lead time	-	20/17.5	-	-	ns
t_{ELG}	Enable lag time	-	20/17.5	-	-	ns
t_{CH}	Clock (SCLK) high time	28/16.6	28/16.6	-	-	ns
t_{CL}	Clock (SCLK) low time	28/16.6	28/16.6	-	-	ns
t_{DS}	Data set-up time required for inputs	20/16.5	1	-	-	ns
t_{DH}	Data hold time required for inputs	1	3	-	-	ns
t_A	Access time (time to data active from high-impedance state)	-	5	-	-	ns
t_D	Disable time (hold time to high-impedance state)	-	5	-	-	ns
t_{DV}	Data valid for outputs	-	-	-/5	-/15	ns
t_{DI}	Data invalid	0	0	-	-	ns
t_R	Rise time	-	-	1	1	ns
t_F	Fall time	-	-	1	1	ns

QSCI timing

Symbol	Characteristic	Min.	Max.	Unit	Notes
BR_{SCI}	Baud rate	-	(f_{MAX_SCI} /16)	Mbit/s	69
PW_{RXD}	RXD pulse width	$0.965/BR_{SCI}$	$1.04/BR_{SCI}$	µs	-
PW_{TXD}	TXD pulse width	$0.965/BR_{SCI}$	$1.04/BR_{SCI}$	µs	-

LIN Slave Mode					
$F_{TOL\_UNSYNCH}$	Deviation of slave node clock from nominal clock rate before synchronization	- 14	14	%	-
F_{TOL_SYNCH}	Deviation of slave node clock relative to the master node clock after synchronization	- 2	2	%	-
T_{BREAK}	Minimum break character length	13	-	Mater node bit periods	-
		11	-	Slave node bit periods	-

CAN timing

Symbol	Characteristic	Min.	Max.	Unit	Notes
BR_{CAN}	Baud rate	-	1	Mbit/s	-
T_{WAKEUP}	CAN Wakeup dominant pulse filtered	-	1.5/2	µs	70
T_{WAKEUP}	CAN Wakeup dominant pulse pass	5	-	µs	-

IIC timing

Symbol	Characteristic	Min.		Max.		Unit	Notes
		Min.	Max.	Min.	Max.		
f_{SCL}	SCL clock frequency	0	100	0	400	kHz	-
t_{HD_STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4	-	0.6	-	µs	-
t_{SCL_LOW}	LOW period of the SCL clock	4.7	-	1.3	-	µs	-
t_{SCL_HIGH}	HIGH period of the SCL clock	4	-	0.6	-	µs	-
t_{SU_STA}	Set-up time for a repeated START condition	4.7	-	0.6	-	µs	-
t_{HD_DAT}	Data hold time for IIC bus devices	0[71]	3.45[72]	0[73]	0.9[71]	µs	-
t_{SU_DAT}	Data set-up time	250[74]	-	100[75]	-	ns	72
t_r	Rise time of SDA and SCL signals	-	1000	20 + 0.1C_b	300	ns	76
t_f	Fall time of SDA and SCL signals	-	300	20 + 0.1C_b	300	ns	75
t_{SU_STOP}	Set-up time for STOP condition	4	-	0.6	-	µs	-
t_{BUS_Free}	Bus free time between STOP and START condition	4.7	-	1.3	-	µs	-
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	N/A	N/A	0	50	ns	-

1. CPU clock = 4 MHz and System running from 8 MHz IRC Applicable to all wakeup times: Wakeup times (in 1,2,3,4) are measured from GPIO toggle for wakeup till GPIO toggle at the wakeup interrupt subroutine from respective stop/wait mode.
2. CPU clock = 200 kHz and 8 MHz IRC on standby. Exit via interrupt on Port C GPIO.
3. N/A
4. Using 64 KHz external clock; CPU Clock = 32 KHz. Exit via an interrupt on PortC GPIO.
5. N/A
6. If the $\overline{\text{RESET}}$ pin filter is enabled by setting the RST_FLT bit in the SIM_CTRL register to 1, the minimum pulse assertion must be greater than 21 ns.

7. TOSC means oscillator clock cycle; TSYSCLK means system clock cycle.
8. During 3.3 V VDD power supply ramp down.
9. During 3.3 V VDD power supply ramp up (gated by LVI_2p7).
10. The maximum TCK operation frequency is f_{SYSCLK}/16 for MWCT1213VLH/AVLH/VLL.
11. Value is after trim.
12. Guaranteed by design.
13. The chip may not function if the high or low pulse width is smaller than 6.25 ns.
14. External clock input rise time is measured from 10% to 90%.
15. External clock input fall time is measured from 90% to 10%.
16. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8 MHz input.
17. The frequency of the core system clock cannot exceed 100 MHz. If the NanoEdge PWM is available, the PLL output must be set to 400 MHz. And the minimum PLL output frequency is 240 MHz for MWCT1213VLH/AVLH/VLL.
18. This is the time required after the PLL is enabled to ensure reliable operation.
19. 32 kHz internal RC oscillator on MWCT1213VLH/AVLH/VLL.
20. Frequency after application of 8 MHz trimmed.
21. Frequency after application of 32 kHz trimmed.
22. Typical +/-2.5%, maximum +/-4% frequency variation for 32 kHz internal RC oscillator.
23. Standby to run mode transition.
24. Power down to run mode transition. 14.4 µs stabilization time for 32 kHz internal RC oscillator.
25. Maximum time based on expectations at cycling end-of-life.
26. The specification is for backup
27. The specification is for MWCT1213VLH/AVLH/VLL.
28. Assumes 25 MHz flash clock frequency.
29. Maximum times for erase parameters based on expectations at cycling end-of-life.
30. 256 KB on MWCT1213. Longer all blocks command operation time for MWCT1213.
31. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.
32. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
33. Cycling endurance represents number of program/erase cycles at -40°C ≤ Tj ≤ 125°C.
34. Write endurance represents the number of writes to each FlexRAM location at -40°C ≤ Tj ≤ 125°C influenced by the cycling endurance of the FlexNVM and the allocated EEPROM backup. Minimum and typical values assume all byte-writes to FlexRAM.
35. The ADC functions up to VDDA = 2.7 V. When VDDA is below 3.0 V, ADC specifications are not guaranteed.
36. When the input is at the V_{REFL} level, the resulting output will be all zeros (hex 000), plus any error contribution due to offset and gain error. When the input is at the V_{REFH} level, the output will be all ones (hex FFF), minus any error contribution due to offset and gain error.
37. ADC clock duty cycle is 45% ~ 55%. MWCT1213 supports 20 MHz maximum ADC clock and 0.6 MHz minimum ADC clock.
38. Conversion range is defined for x1 gain setting. For x2 and x4 the range is 1/2 and 1/4, respectively.
39. In unipolar mode, positive input must be ensured to be always greater than negative input.
40. On MWCT1213, 8.5 clock cycles for the first conversion, 6 clock cycles for the subsequent conversion.
41. the power down current of ADC 0.02 µA forM WCT1213VLH/VLL.
42. the V_{REFH} current of ADC is 0.001 µA for MWCT1213VLH/AVLH/VLL.
43. INL_{ADC}/DNL_{ADC} is measured from VADCIN = VREFL to VADCIN = VREFH using Histogram method at x1 gain setting. On MWCT1213VLH/AVLH/VLL, typical value is +/- 3 LSB, and maximum value +/- 5 LSB for INL_{ADC}; typical value is +/- 0.6 LSB, and maximum value +/- 1 LSB for DNL_{ADC}.
44. Least Significant Bit = 0.806 mV at 3.3 V VDDA, x1 gain setting.
45. Any off-channel with 50 kHz full-scale input to the channel being sampled with DC input (isolation crosstalk).
46. Typical +/- 13.7 mV offset for MWCT1213VLH/AVLH/VLL.
47. Typical ENOB is 9.5 bits for MWCT1213VLH/AVLH/VLL.
48. The current that can be injected into or sourced from an unselected ADC input without affecting the performance of the ADC.
49. Typical values assume VDDA = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
50. To use the maximum ADC conversion clock frequency, the ADHSC bit must be set and the ADLPC bit must be clear.
51. The ADC supply current depends on the ADC conversion clock speed, conversion rate and the ADLPC bit (low power). For lowest power operation the ADLPC bit should be set, the HSC bit should be clear with 1MHz ADC conversion clock speed.
52. 1 LSB = (VREFH - VREFL)/2^N.

53. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11).
54. Input data is 100 Hz sine wave; ADC conversion clock < 12 MHz.
55. System clock = 4 MHz, ADC clock = 2 MHz, AVG = Max, Long Sampling = Max.
56. Settling time is swing range from VSSA to VDDA.
57. LSB = 0.806 mV.
58. No guaranteed specification within 5% of VDDA or VSSA.
59. Maximum supply current with high-speed mode is 200 µA, maximum supply current with low-speed mode is 20 µA on MWCT1213VLH/AVLH/VLL.
60. Typical hysteresis is measured with input voltage range limited to 0.7 to VDD-0.7 V. On MWCT1213, typical 10 mV for CR0[HYSTCTR] = 01, typical 20 mV for CR0[HYSTCTR] = 10, typical 30 mV for CR0[HYSTCTR] = 11.
61. Signal swing is 100 mV.
62. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
63. 1 LSB = Vreference/64.
64. Reference IPbus clock of 100 MHz in NanoEdge Placement mode.
65. Temperature and voltage variations do not affect NanoEdge Placement step size.
66. Powerdown to NanoEdge mode transition.
67. Ttimer = Timer input clock cycle. For 100 MHz operation, Ttimer = 10 ns.
68. For QSPI specifications, all data with xx/xx format, the former is for backup, the latter is for MWCT1213.
69. fMAX_SCI is the frequency of operation of the SCI clock in MHz, which can be selected as the bus clock or 2x bus clock for the device.
70. MWCT1213 supports maximum 2 us pulse filtered.
71. The master mode IIC deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
72. The maximum tHD_DAT must be met only if the device does not stretch the LOW period (tSCL_LOW) of the SCL signal.
73. Input signal Slew = 10 ns and Output Load = 50 pF
74. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
75. A Fast mode IIC bus device can be used in a Standard mode IIC bus system, but the requirement tSU_DAT ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line trmax + tSU_DAT = 1000 + 250 = 1250 ns (according to the Standard mode IIC bus specification) before the SCL line is released.
76. Cb = total capacitance of the one bus line in pF.

2.3 Thermal operating characteristics

Table 7. General thermal characteristics

Symbol	Description	Min	Max	Unit
T_J	Die junction temperature	-40	125	°C
T_A	Ambient temperature	-40	105	°C

3 Typical Performance Characteristics

3.1 System efficiency

The typical system efficiency (receiver output power vs. transmitter input power) on NXP MWCT1213VLH/AVLH/VLL -based transmitter solutions can usually reach more than 75%. The detailed number depends on the specific solution type.

Note: Power components are the main factor to determine the system efficiency, such as drivers and MOSFETs.

3.2 Standby power

The purpose of the standby mode of operation is to reduce the power consumption of a wireless power transfer system when power transfer is not required. There are two ways to enter standby mode. The first is when the transmitter does not detect the presence of a valid receiver. The second is when the receiver sends only an End Power Transfer Packet. In standby mode, the transmitter only monitors if a receiver is placed on the active charging area of the transmitter or removed from there.

It is recommended that the power consumption of the transmitter in standby mode meets the relative regional regulations especially for “No-load power consumption”.

3.3 Digital demodulation

To optimize system BOM cost, the MWCT1213 solution employs digital demodulation algorithm to communicate with the receiver. This method can achieve high performance, low cost, and very simple coil signal sensing circuit with less components number, and 2 channels can be supported.

3.4 Two-way communication

The MWCT1213 solution supports two-way communication and uses FSK to send messages to receiver. This method allows transmitter to negotiate with receiver to establish advanced power transfer contract, and calibrate power loss for more precise FOD protection.

3.5 Foreign object detection

The MWCT1213 solution supports power class 0 FOD framework, which is based on calibrated power loss method and quality factor (Q factor) method. With NXP FreeMASTER GUI tool, the FOD algorithm can be easily calibrated to get accurate power loss information especially for very sensitive foreign objects.

4 Device Information

4.1 Functional block diagram

This functional block diagram shows the common pin assignment information by all members of the family. For the detailed pin multiplexing information, see Section 4.4 “Pin Function Description”.

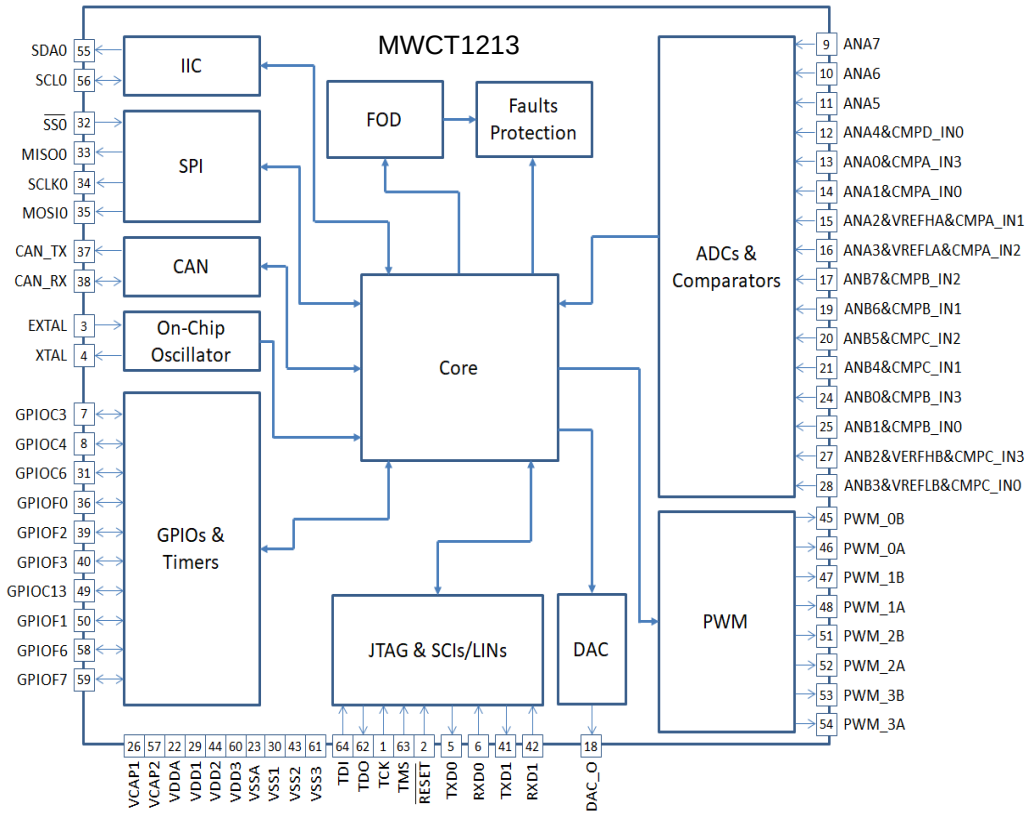

Figure 2. MWCT1213VLH/AVLH function block diagram 64Pins

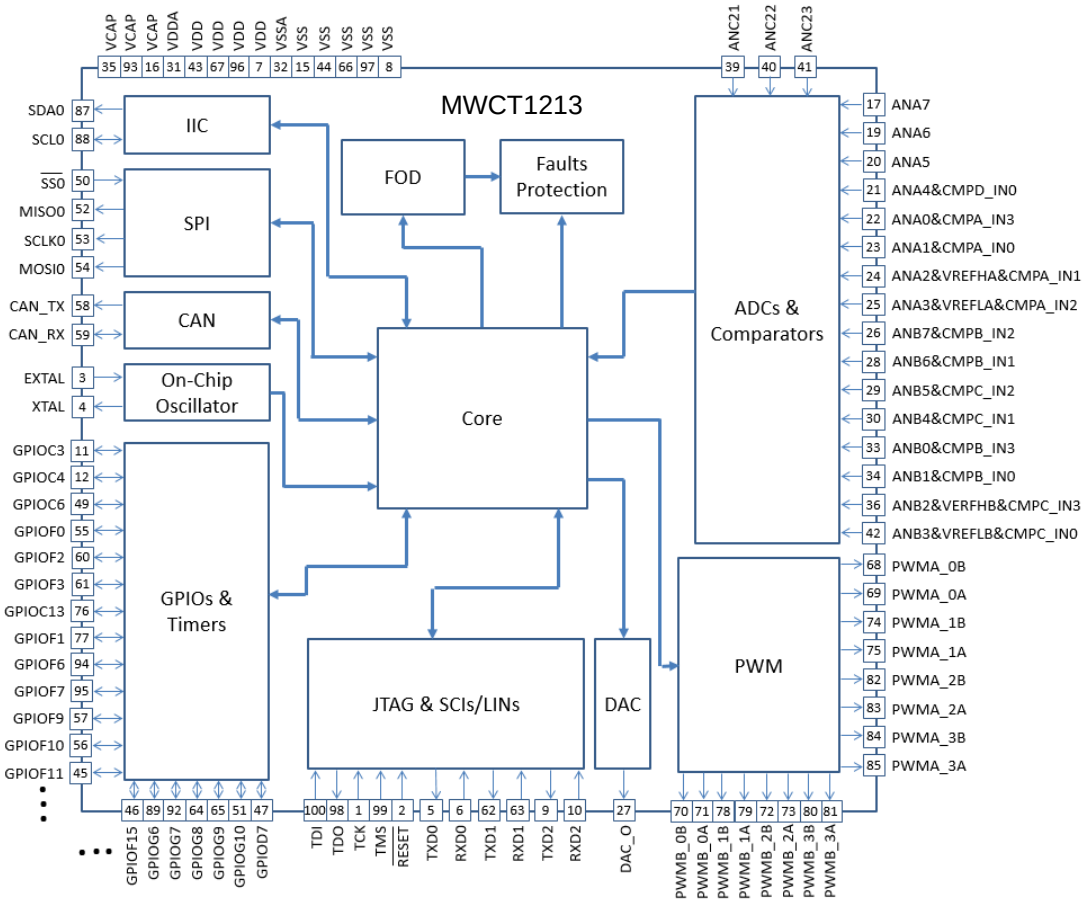

Figure 3. MWCT1213VLL function block diagram 100 Pins

4.2 Product features overview

The following table lists the features that differ among members of the family. Features not listed are shared in common by all members of the family.

Table 8. Feature for MWCT1213

Part		MWCT1213VLH MWCT1213AVLH	MWCT1213VLL
Maximum Core/Bus Clock (MHz)		100/100	100/100
Maximum Fully Run Current Consumption (mA)		63.7 (V_{DD}) + 16.7 (V_{DDA})	63.7 (V_{DD}) + 16.7 (V_{DDA})
On-Chip Flash Memory Size (KB)	Program Flash Memory	256	256
	FlexNVM/FlexRAM	32/2	32/2
	Total Flash Memory	288	288
On-Chip SRAM Memory Size (KB)		32	32
Memory Resource Protection		Yes	Yes
Inter-Peripheral Crossbar Switches with AOI		Yes	Yes

On-Chip Relaxation Oscillator		1 (8 MHz) + 1 (32 kHz)	1 (8 MHz) + 1 (32 kHz)
Computer Operating Properly (Watchdog)		1	1
External Watchdog Monitor		1	1
Cyclic Redundancy Check		1	1
Periodic Interrupt Timer		2	2
Quad Timer		2 x 4	2 x 4
Programmable Delay Block		2	2
12-bit Cyclic ADC Channels		2 x 8	2 x 8
16-bit SAR ADC Channels		1 x 8	1 x 16
PWM Channels	High-Resolution	8	8
	Standard	1	4
12-bit DAC		1	1
Analog Comparator /w 6-bit REF DAC		4	4
DMA Channels		4	4
Queued Serial Communications Interface		2	3
Queued Serial Peripheral Interface		1	3
Inter-Integrated Circuit		2	2
Controller Area Network		1 (FlexCAN)	1 (FlexCAN)
GPIO		54	82
Package		64 LQFP	100 LQFP

4.3 Pinout diagram

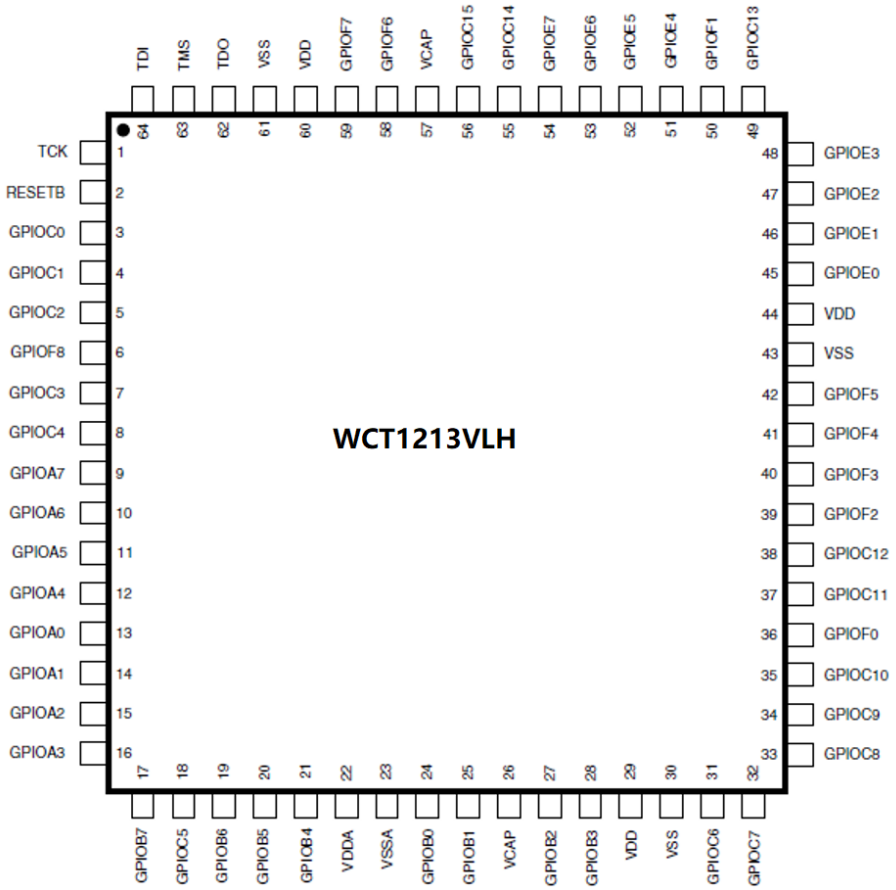

Figure 4. MWCT1213VLH/AVLH pinout diagram 64 Pins

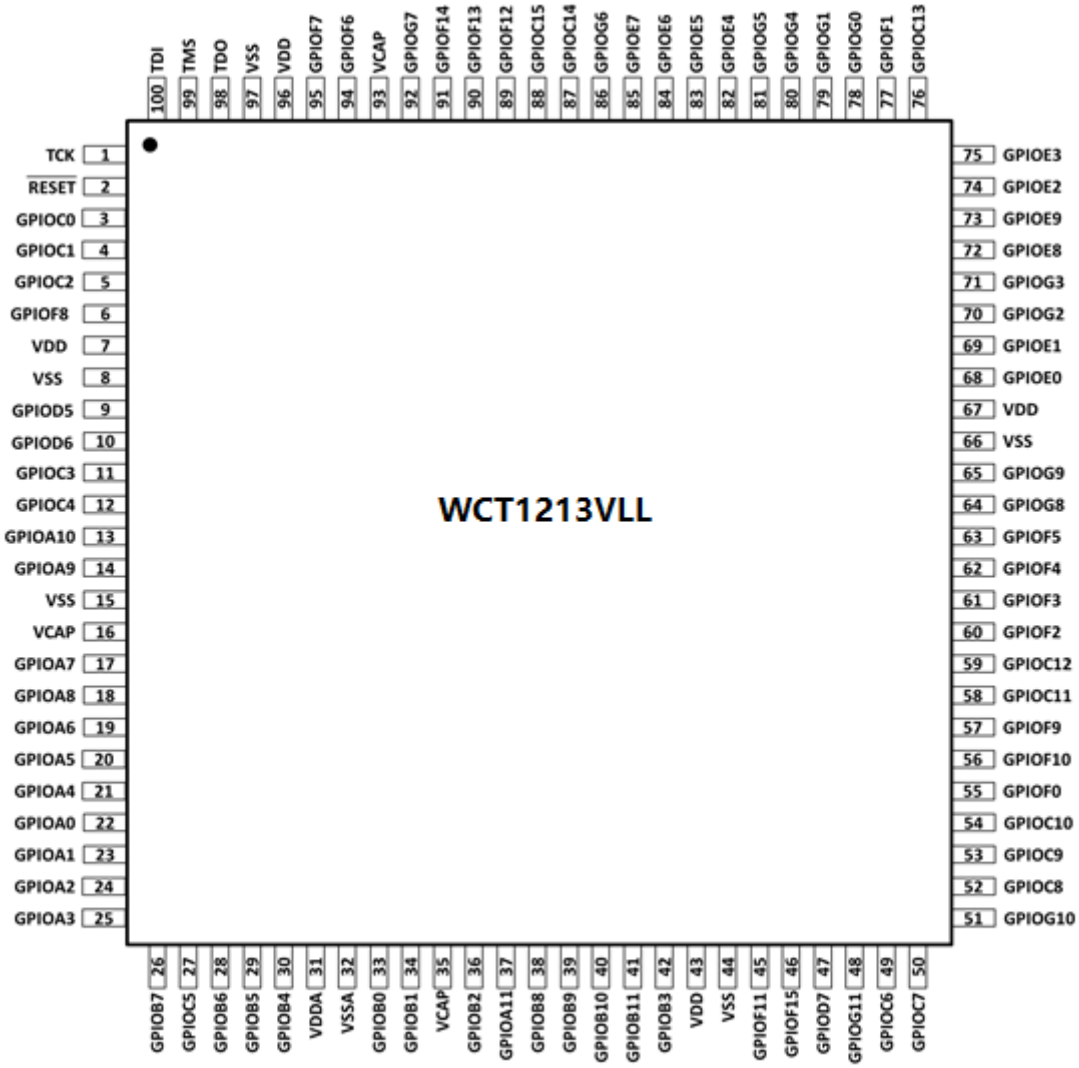

Figure 5. MWCT1213VLL pinout diagram 100 Pins

4.4 Pin function description

By default, each pin is configured for its primary function (listed first). Any alternative functionality, shown in parentheses, can be programmed through GPIO module peripheral enable registers and SIM module GPIO peripheral select registers.

Table 9. Pin signal descriptions

Signal name	100 Pin No.	64 Pin No.	Type	State During Reset	Function description
TCK	1	1	Input	Input, internal pullup	Test Clock Input — This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/EOnCE

				enabled	port. The pin is connected internally to a pullup resistor. A Schmitt-trigger input is used for noise immunity. After reset, the default state is TCK.
RESET	2	2	Input	Input, internal pullup enabled (This pin is 3.3V only.)	Reset — A direct hardware reset on the processor. When RESET is asserted low, the device is initialized and placed in the reset state. A Schmitt-trigger input is used for noise immunity. The internal reset signal is deasserted synchronously with the internal clocks after a fixed number of internal clocks. After reset, the default state is RESET. To filter noise on the RESETB pin, install a capacitor (up to 0.1 uF) on it.
GPIOC0	3	3	Input/ Output	Input	GPIO Port C0: After reset, the default state is GPIOC0.
GPIOC1	4	4	Input/ Output	Input	GPIO Port C1: After reset, the default state is GPIOC1.
GPIOC2	5	5	Input/ Output	Input	GPIO Port C2: After reset, the default state is GPIOC2.
GPIOF8	6	6	Input/ Output	Input	GPIO Port F8: After reset, the default state is GPIOF8.
VDD	7	-	Supply	Supply	I/O Power — Supplies 3.3 V power to the V chip I/O interface.
VSS	8	-	Supply	Supply	I/O Ground — Provide ground for the V device I/O interface.
GPIOD5	9	-	Input/ Output	Input	GPIO Port D5: After reset, the default state is GPIOD5.
GPIOD6	10	-	Input/ Output	Input	GPIO Port D6: After reset, the default state is GPIOD6.
GPIOC3	11	7	Input/ Output	Input	GPIO Port C3: After reset, the default state is GPIOC3.
GPIOC4	12	8	Input/ Output	Input	GPIO Port C4: After reset, the default state is GPIOC4.
GPIOA10	13	-	Input/ Output	Input	GPIO Port A10: After reset, the default state is GPIOA10.
GPIOA9	14	-	Input/ Output	Input	GPIO Port A9: After reset, the default state is GPIOA9.
VSS	15	-	Supply	Supply	I/O Ground — Provide ground for the V device I/O interface.
VCAP	16	-	On-chip regulator output voltage	On-chip regulator output voltage	Connect a 2.2uF or greater bypass capacitor between this pin and VSS to stabilize the core voltage regulator output required for proper device operation. V_{CAP} is used to observe core voltage.
GPIOA7	17	9	Input/ Output	Input	GPIO Port A7: After reset, the default state is GPIOA7.
GPIOA8	18	-	Input/ Output	Input	GPIO Port A8: After reset, the default state is GPIOA8.
GPIOA6	19	10	Input/ Output	Input	GPIO Port A6: After reset, the default state is GPIOA6.
GPIOA5	20	11	Input/ Output	Input	GPIO Port A5: After reset, the default state is GPIOA5.
GPIOA4	21	12	Input/ Output	Input	GPIO Port A4: After reset, the default state is GPIOA4.
GPIOA0	22	13	Input/ Output	Input	GPIO Port A0; after reset, the default state is GPIOA0.
GPIOA1	23	14	Input/ Output	Input	GPIO Port A1: After reset, the default state is GPIOA1.

GPIOA2	24	15	Input/ Output	Input	GPIO Port A2: After reset, the default state is GPIOA2.
GPIOA3	25	16	Input/ Output	Input	GPIO Port A3: After reset, the default state is GPIOA3.
GPIOB7	26	17	Input/ Output	Input	GPIO Port B7: After reset, the default state is GPIOB7.
GPIOC5	27	18	Input/ Output	Input	GPIO Port C5: After reset, the default state is GPIOC5.
GPIOB6	28	19	Input/ Output	Input	GPIO Port B6: After reset, the default state is GPIOB6.
GPIOB5	29	20	Input/ Output	Input	GPIO Port B5: After reset, the default state is GPIOB5.
GPIOB4	30	21	Input/ Output	Input	GPIO Port B4: After reset, the default state is GPIOB4.
VDDA	31	22	Supply	Supply	Analog Power — Supplies 3.3 V power to the analog modules. It must be connected to a clean analog power supply.
VSSA	32	23	Supply	Supply	Analog Ground — Supplies an analog ground to the analog modules. It must be connected to a clean power supply.
GPIOB0	33	24	Input/ Output	Input	GPIO Port B0: After reset, the default state is GPIOB0.
GPIOB1	34	25	Input/ Output	Input	GPIO Port B1: After reset, the default state is GPIOB1.
VCAP	35	26	On-chip regulator output voltage	On-chip regulator output voltage	Connect a 2.2uF or greater bypass capacitor between this pin and VSS to stabilize the core voltage regulator output required for proper device operation. V_{CAP} is used to observe core voltage.
GPIOB2	36	27	Input/ Output	Input	GPIO Port B2: After reset, the default state is GPIOB2.
GPIOA11	37	-	Input/ Output	Input	GPIO Port A11: After reset, the default state is GPIOA11.
GPIOB8	38	-	Input/ Output	Input	GPIO Port B8: After reset, the default state is GPIOB8.
GPIOB9	39	-	Input/ Output	Input	GPIO Port B9: After reset, the default state is GPIOB9.
GPIOB10	40	-	Input/ Output	Input	GPIO Port B10: After reset, the default state is GPIOB10.
GPIOB11	41	-	Input/ Output	Input	GPIO Port B11: After reset, the default state is GPIOB11.
GPIOB3	42	28	Input/ Output	Input	GPIO Port B3: After reset, the default state is GPIOB3.
VDD	43	29	Supply	Supply	I/O Power — Supplies 3.3 V power to the V chip I/O interface.
VSS	44	30	Supply	Supply	I/O Ground — Provide ground for the V device I/O interface.
GPIOF11	45	-	Input/ Output	Input	GPIO Port F11: After reset, the default state is GPIOF11.
GPIOF15	46	-	Input/ Output	Input	GPIO Port F15: After reset, the default state is GPIOF15.
GPIOD7	47	-	Input/ Output	Input	GPIO Port D7: After reset, the default state is GPIOD7.
GPIOG11	48	-	Input/ Output	Input	GPIO Port G11: After reset, the default state is GPIOG11.
GPIOC6	49	31	Input/ Output	Input	GPIO Port C6: After reset, the default state is GPIOC6
GPIOC7	50	32	Input/ Output	Input	GPIO Port C7: After reset, the default state is GPIOC7.

GPIOG10	51	-	Input/ Output	Input	GPIO Port G10: After reset, the default state is GPIOG10.
GPIOC8	52	33	Input/ Output	Input	GPIO Port C8: After reset, the default state is GPIOC8.
GPIOC9	53	34	Input/ Output	Input	GPIO Port C9: After reset, the default state is GPIOC9.
GPIOC10	54	35	Input/ Output	Input	GPIO Port C10: After reset, the default state is GPIOC10.
GPIOF0	55	36	Input/ Output	Input	GPIO Port F0: After reset, the default state is GPIOF0.
GPIOF10	56	-	Input/ Output	Input	GPIO Port F10: After reset, the default state is GPIOF10.
GPIOF9	57	-	Input/ Output	Input	GPIO Port F9: After reset, the default state is GPIOF9.
GPIOC11	58	37	Input/ Output	Input	GPIO Port C11: After reset, the default state is GPIOC11.
GPIOC12	59	38	Input/ Output	Input	GPIO Port C12: After reset, the default state is GPIOC12.
GPIOF2	60	39	Input/ Output	Input	GPIO Port F2: After reset, the default state is GPIOF2.
GPIOF3	61	40	Input/ Output	Input	GPIO Port F3: After reset, the default state is GPIOF3.
GPIOF4	62	41	Input/ Output	Input	GPIO Port F4: After reset, the default state is GPIOF4.
GPIOF5	63	42	Input/ Output	Input	GPIO Port F5: After reset, the default state is GPIOF5.
GPIOG8	64	-	Input/ Output	Input	GPIO Port G8: After reset, the default state is GPIOG8.
GPIOG9	65	-	Input/ Output	Input	GPIO Port G9: After reset, the default state is GPIOG9.
VSS	66	43	Supply	Supply	I/O Ground — Provide ground for the V device I/O interface.
VDD	67	44	Supply	Supply	I/O Power — Supplies 3.3 V power to the V chip I/O interface.
GPIOE0	68	45	Input/ Output	Input	GPIO Port E0: After reset, the default state is GPIOE0.
GPIOE1	69	46	Input/ Output	Input	GPIO Port E1: After reset, the default state is GPIOE1.
GPIOG2	70	-	Input/ Output	Input	GPIO Port G2: After reset, the default state is GPIOG2.
GPIOG3	71	-	Input/ Output	Input	GPIO Port G3: After reset, the default state is GPIOG3.
GPIOE8	72	-	Input/ Output	Input	GPIO Port E8: After reset, the default state is GPIOE8.
GPIOE9	73	-	Input/ Output	Input	GPIO Port E9: After reset, the default state is GPIOE9.
GPIOE2	74	47	Input/ Output	Input	GPIO Port E2: After reset, the default state is GPIOE2.
GPIOE3	75	48	Input/ Output	Input	GPIO Port E3: After reset, the default state is GPIOE3.
GPIOC13	76	49	Input/ Output	Input	GPIO Port C13: After reset, the default state is GPIOC13.
GPIOF1	77	50	Input/ Output	Input	GPIO Port F1: After reset, the default state is GPIOF1.
GPIOG0	78	-	Input/ Output	Input	GPIO Port G0: After reset, the default state is GPIOG0.
GPIOG1	79	-	Input/ Output	Input	GPIO Port G1: After reset, the default state is GPIOG1.
GPIOG4	80	-	Input/	Input	GPIO Port G4: After reset, the default state

			Output		is GPIOG4.
GPIOG5	81	-	Input/ Output	Input	GPIO Port G5: After reset, the default state is GPIOG5.
GPIOE4	82	51	Input/ Output	Input	GPIO Port E4: After reset, the default state is GPIOE4.
GPIOE5	83	52	Input/ Output	Input	GPIO Port E5: After reset, the default state is GPIOE5.
GPIOE6	84	53	Input/ Output	Input	GPIO Port E6: After reset, the default state is GPIOE6.
GPIOE7	85	54	Input/ Output	Input	GPIO Port E7: After reset, the default state is GPIOE7.
GPIOG6	86	-	Input/ Output	Input	GPIO Port G6: After reset, the default state is GPIOG6.
GPIOC14	87	55	Input/ Output	Input	GPIO Port C14: After reset, the default state is GPIOC14.
GPIOC15	88	56	Input/ Output	Input	GPIO Port C15: After reset, the default state is GPIOC15.
GPIOF12	89	-	Input/ Output	Input	GPIO Port F12: After reset, the default state is GPIOF12.
GPIOF12	90	-	Input/ Output	Input	GPIO Port F13: After reset, the default state is GPIOF13.
GPIOF14	91	-	Input/ Output	Input	GPIO Port F14: After reset, the default state is GPIOF14.
GPIOG7	92	-	Input/ Output	Input	GPIO Port G7: After reset, the default state is GPIOG7.
VCAP	93	57	On-chip regulator output voltage	On-chip regulator output voltage	Connect a 2.2uF or greater bypass capacitor between this pin and VSS to stabilize the core voltage regulator output required for proper device operation. V_{CAP} is used to observe core voltage.
GPIOF6	94	58	Input/ Output	Input	GPIO Port F6: After reset, the default state is GPIOF6.
GPIOF7	95	59	Input/ Output	Input	GPIO Port F7: After reset, the default state is GPIOF7.
VDD	96	60	Supply	Supply	I/O Power — Supplies 3.3 V power to the V chip I/O interface.
VSS	97	61	Supply	Supply	I/O Ground — Provide ground for the V device I/O interface.
TDO	98	62	Output	Output	Test Data Output — This tri-stateable pin provides a serial output data stream from the JTAG/EOnCE port. It is driven in the shift-IR and shift-DR controller states, and it changes on the falling edge of TCK. After reset, the default state is TDO.
TMS	99	63	Input	Input, internal pullup enabled	Test Mode Select Input — Used to sequence the JTAG TAP controller state machine. It is sampled on the rising edge of TCK and has an internal pullup resistor. After reset, the default state is TMS. **NOTE:** Always tie the TMS pin to VDD through a 2.2K resistor, if needed to keep an on-board debug capability. Otherwise, tie the TMS pin directly to VDD.
TDI	100	64	Input	Input, internal pullup enabled	Test Data Input — Provides a serial input data stream to the JTAG/EOnCE port. It is sampled on the rising edge of TCK and has an internal pullup resistor. After reset, the default state is TDI.

4.5 Ordering information

Table 10 lists the pertinent information needed to place an order. Consult a NXP Semiconductors sales office to determine availability and to order this device.

Table 10. MWCT1213VLH/AVLH/VLL ordering information

Device	Supply voltage	Package type	Pin count	Ambient temp.	Order number
MWCT1213VLH	2.7 to 3.6V	LQFP	64	-40 to +105℃	MWCT1213VLH
MWCT1213AVLH	2.7 to 3.6V	LQFP	64	-40 to +105℃	MWCT1213AVLH
MWCT1213VLL	2.7 to 3.6V	LQFP	100	-40 to +105℃	MWCT1213VLL

4.6 Package outline drawing

To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

- 64-pin LQFP 98ASS23234W
- 100-pin LQFP 98ASS23308W

5 Software Library

The software for MWCT1213VLH/AVLH/VLL is matured and tested for production ready. NXP provides a Wireless Charging Transmitter (WCT) software library for speeding user designs. In this library, low-level drivers of HAL (Hardware Abstract Layer), callback functions for library access are open to user. For the software API and library details, see the *WCT1213VLL/VLH A TX Library User's Guide* (WCT1213 ALIBUG).

5.1 Memory map

MWCT1213 has large on-chip Flash memory and RAM for user design. Besides wireless charging transmitter library code, the user can develop private functions and link it to library through predefined APIs.

Table 11. MWCT1213 memory footprint

Part	Memory	Total size	Library size	FreeMASTER size	EEPROM size	Free size
MWCT1213VLH/AVLH/VLL MWCT1213AVLH	Flash	288 Kbytes	41.9 Kbytes	3.5 Kbytes	1 Kbytes	241.6 Kbytes
	RAM	32 Kbytes	3.22 Kbytes	0.13 Kbytes	0 Kbytes	28.65 Kbytes

5.2 Software library and API description

For more information about WCT software library and API definition, see the *WCT1213 A TX Library User's Guide* (WCT1213 ALIBUG).

6 Design Considerations

6.1 Electrical design considerations

To ensure correct operations on the device and system, pay attention to the following points:

- The minimum bypass requirement is to place 0.01 - 0.1 μ F capacitors positioned as near as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the VDD/VSS pairs, including VDDA/VSSA. Ceramic and tantalum capacitors tend to provide better tolerances.
- Bypass the VDD and VSS with approximately 10 μ F, plus the number of 0.1 μ F ceramic capacitors.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the VDD and VSS circuits.
- Take special care to minimize noise levels on the VDDA and VSSA pins.
- It is recommended to use separate power planes for VDD and VDDA and use separate ground planes for VSS and VSSA. Connect the separate analog and digital power and ground planes as near as possible to power supply outputs. If an analog circuit and digital circuit are powered by the same power supply, connect a small inductor or ferrite bead in serial with VDDA trace.
- If desired, connect an external RC circuit to the RESET pin. The resistor value should be in the range of 4.7 kΩ - 10 kΩ; and the capacitor value should be in the range of 0.1 μ F - 4.7 μ F.
- Add a 2.2 kΩ external pull-up on the TMS pin of the JTAG port to keep device in a restate during normal operation if JTAG converter is not present.
- During reset and after reset but before I/O initialization, all I/O pins are at input mode with internal weak pull-up.
- To eliminate PCB trace impedance effect, each ADC input should have a no less than 33pF/10 Ω RC filter.
- To assure chip reliable operation, reserve enough margin for chip electrical design. Figure 6 shows the relationship between electrical ratings and electrical operating characteristics for correct chip operation.

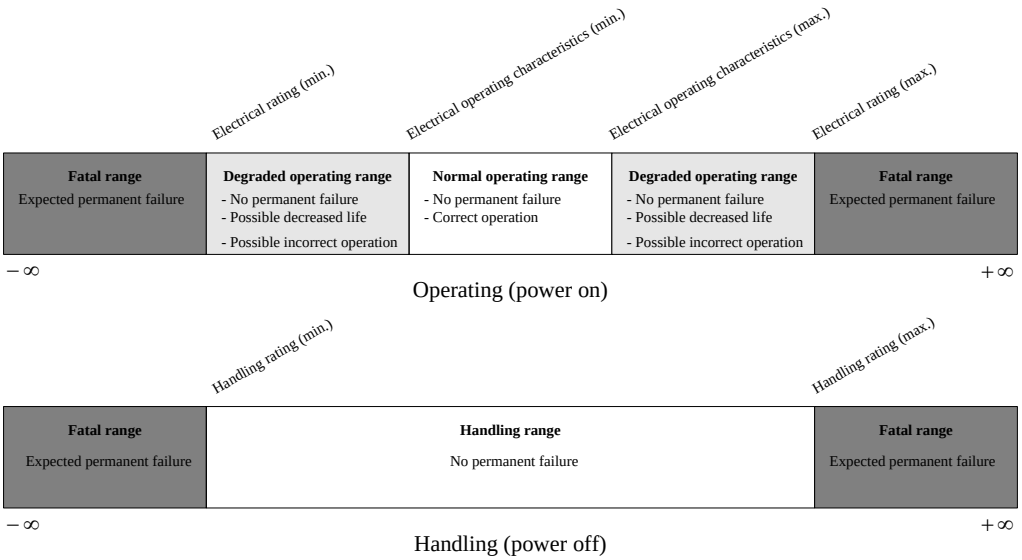

Figure 6. Relationship between ratings and operating characteristics

6.2 PCB layout considerations

- Provide a low-impedance path from the board power supply to each VDD pin on the device and from the board ground to each VSS pin.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip VDD and VSS pins are as short as possible.
- PCB trace lengths should be minimal for high-frequency signals.
- Physically separate analog components from noisy digital components by ground planes. Do not place an analog trace in parallel with digital traces. Place an analog ground trace around an analog signal trace to isolate it from digital traces.
- The decoupling capacitors of 0.1 μ F must be placed on the VDD pins as close as possible and place those ceramic capacitors on the same PCB layer with MWCT1213 device. VIA is not recommended between the VDD pins and decoupling capacitors.
- As the wireless charging system functions as a switching-mode power supply, the power components layout is very important for the whole system power transfer efficiency and EMI performance. The power routing loop should be as small and short as possible. Especially for the resonant network, the traces of this circuit should be short and wide, and the current loop should be optimized smaller for the MOSFETs, resonant capacitor and primary coil. Another important thing is that the control circuit and power circuit should be separated.

6.3 Thermal design considerations

MWCT1213VLH/AVLH/VLL power consumption is not so critical, so there is not additional part needed for power dissipation. However, the power inverter needs the additional PCB Cu copper to

dissipate the heat, so good thermal package MOSFET is recommended, such as DFN package, and for the resonant capacitor, COG material, and 1206 or 1210 package are recommended to meet the thermal requirement. The worst thermal case is on the inverter, so the user should make some special actions to dissipate the heat for good transmitter system thermal performance.

7 Links

- nxp.com
- nxp.com/products/power-management/wireless-charging-ics
- www.wirelesspowerconsortium.com

8 Revision History

This table summarizes revisions to this document.

Table 12. Revision history

Revision number	Date	Substantive changes
0	06/2020	Initial release.