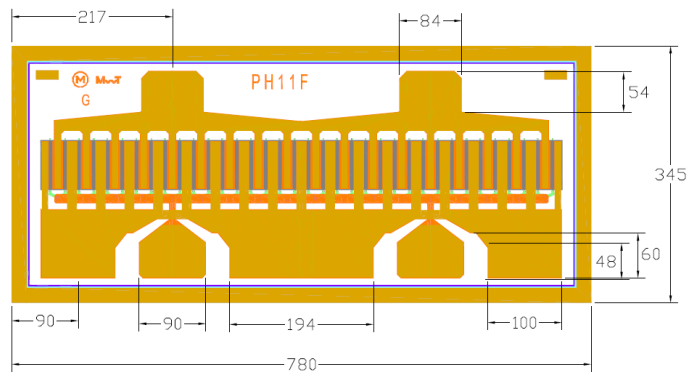


### Features:

- 33 dBm of Power at 12 GHz
- 12 dB Small Signal Gain at 12 GHz
- 45% PAE at 12 GHz
- 0.25 x 2400 Micron Refractory Metal/Gold Gate
- Excellent for High Power, and High Power Added Efficiency
- Ideal for Commercial, Military, Hi-Rel Space Applications
- Available with or without via holes



Chip Dimensions: 780 x 345 microns  
Chip Thickness: 100 microns

### Description:

The MwT-PH11F is a AlGaAs/InGaAs pHEMT (Pseudomorphic-High-Electron-Mobility-Transistor) device whose nominal 0.25 micron gate length and 2400 micron gate width make it ideally suited for applications requiring high power and high power added efficiency up to 12 GHz frequency range. The device is equally effective for either wideband or narrow-band applications. The chip is produced using reliable metal systems and passivated to insure excellent reliability.

### Electrical Specifications: at $T_a = 25\text{ }^\circ\text{C}$

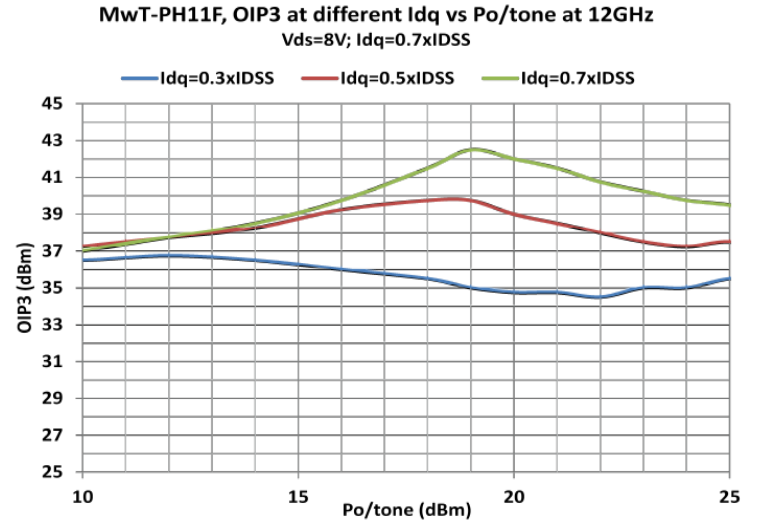
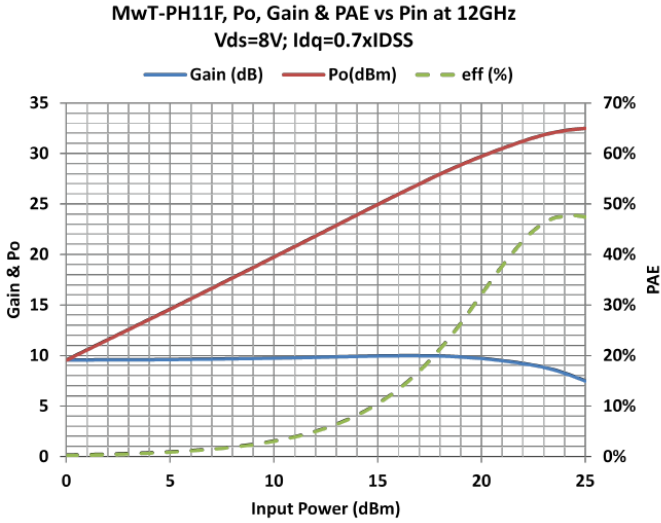
PARAMETERS & CONDITIONS	SYMBOL	FREQ	UNITS	MIN	TYP
Output Power at 1dB Compression $V_{ds}=8.0\text{V}$ $I_{ds}=0.7 \times I_{DSS}$	P1dB	12 GHz	dBm		32.0
Saturated Power $V_{ds}=8.0\text{V}$ $I_{ds}=0.7 \times I_{DSS}$	Psat	12 GHz	dBm		33.0
Output Third Order Intercept Point $V_{ds}=8.0\text{V}$ $I_{ds}=0.7 \times I_{DSS}$	OIP3	12 GHz	dBm		40.0
Small Signal Gain $V_{ds}=8.0\text{V}$ $I_{ds}=0.7 \times I_{DSS}$	SSG	12 GHz	dB		12.0
Power Added Efficiency at P1dB $V_{ds}=8.0\text{V}$ $I_{ds}=0.7 \times I_{DSS}$	PAE	12 GHz	%		45

Note:  $I_{ds}$  should be between 40% and 80% of  $I_{DSS}$ . Currently, our data shows  $I_{ds}$  at 70% of  $I_{DSS}$ . Low  $I_{ds}$  will improve efficiency, but high  $I_{ds}$  will make Psat and IP3 better.

### DC Specifications: at $T_a = 25\text{ }^\circ\text{C}$

PARAMETERS & CONDITIONS	SYMBOL	UNITS	MIN	TYP	MAX
Saturated Drain Current $V_{ds}= 3.0\text{ V}$ $V_{gs}= 0.0\text{ V}$	$I_{DSS}$	mA	480		520
Transconductance $V_{ds}= 2.5\text{ V}$ $V_{gs}= 0.0\text{ V}$	Gm	mS		700	
Pinch-off Voltage $V_{ds}= 3.0\text{ V}$ $I_{ds}= 1.0\text{ mA}$	$V_p$	V		-0.8	-1.0
Gate-to-Source Breakdown Voltage $I_{gs}= -0.3\text{ mA}$	BVGSO	V		-17.0	
Gate-to-Drain Breakdown Voltage $I_{gd}= -0.3\text{ mA}$	BVGDO	V		-18.0	
Chip Thermal Resistance	Chip & 71 pkg	Rth		25	

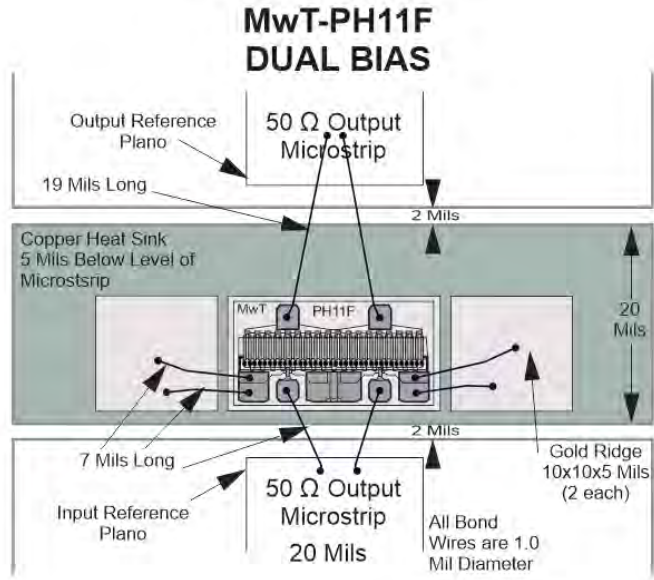
\* Overall Rth depends on case mounting



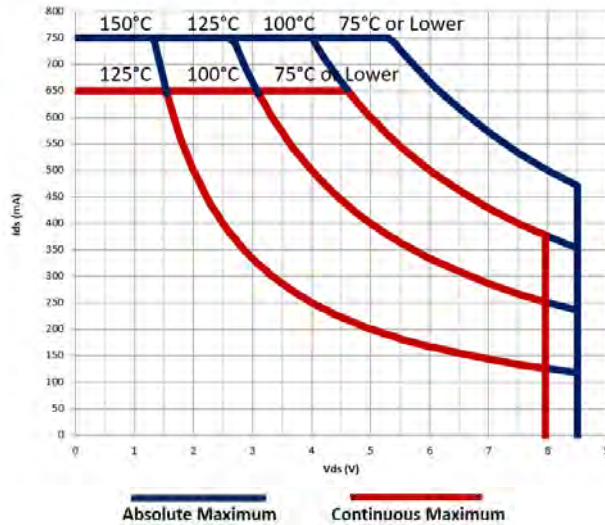
**MwT-PH11F, Load Pull data, Vds=8V, Idq=0.7xIdss**

Freq (GHz)	Z <sub>s</sub>		Z <sub>L</sub>		P <sub>sat</sub>
	Mag	phase	mag	phase	dBm
2	0.75	145.0	0.57	170.3	33.0
4	0.90	162.0	0.63	170.3	32.6
6	0.95	172.0	0.65	169.8	32.7
8	0.95	177.0	0.68	170.9	32.6
10	0.94	179.0	0.72	171.0	32.1
12	0.93	-177.0	0.72	171.0	32.3

The load pull data is based on nonlinear model provided by the foundry that processes the device.



**SAFE OPERATING LIMITS vs BACKSIDE TEMPERATURE**  
MwT-PH11F Chip and 71 Pkg



### Absolute Maximum Rating

Symbol	Parameter	Units	Cont Max1	Absolute Max2
VDS	Drain to Source Volt.	V	8.0	8.5
Tch	Channel Temperature	°C	+150	+175
Tst	Storage Temperature	°C	-65 to +150	+175
Pin	RF Input Power	mW	500	700

**Notes:**

1. Exceeding any one of these limits in continuous operation may reduce the mean-time-to-failure below the design goal.
2. Exceeding any one of these limits may cause permanent damage.