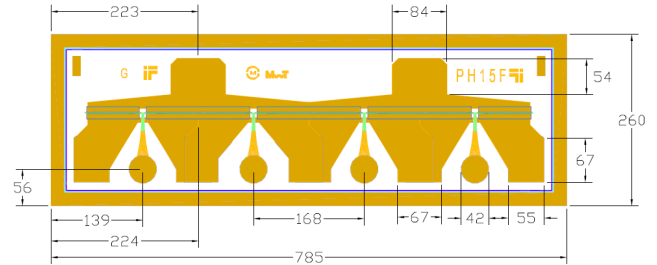


### Features:

- 28.5 dBm typical Output Power at 18 GHz
- 12 dB typical Small Signal Gain at 18 GHz
- 45% typical PAE at 18 GHz
- 0.25 x 630 Micron Refractory Metal/Gold Gate
- Excellent for Power, Gain, and High Power Added Efficiency
- Ideal for Commercial, Military, Hi-Rel Space Applications



Chip Dimensions: 785 x 260 microns  
Chip Thickness: 100 microns

### Description:

The MwT-PH15F is a AlGaAs/InGaAs pHEMT (Pseudomorphic-High-Electron-Mobility-Transistor) device whose nominal 0.25 micron gate length and 630 micron gate width make it ideally suited for applications requiring high-gain and medium power with frequency up to 28 GHz. The device is equally effective for either wideband (e.g. 6 to 18 GHz) or narrow-band applications. The chip is produced using reliable metal systems and passivated to insure excellent reliability.

### Electrical Specifications: • at $T_a = 25^\circ C$

PARAMETERS & CONDITIONS	SYMBOL	FREQ	UNITS	MIN	TYP
Output Power at 1dB Compression $V_{ds}=8V; I_{ds}=0.7 \times I_{DSS}$	P1dB	18 GHz	dBm		28.0
Saturated Power $V_{ds}=8V; I_{ds}=0.7 \times I_{DSS}$	Psat	18 GHz	dBm		28.5
Output Third Order Intercept Point $V_{ds}=8V; I_{ds}=0.7 \times I_{DSS}$	OIP3	18 GHz	dBm		34.0
Small Signal Gain $V_{ds}=8V; I_{ds}=0.7 \times I_{DSS}$	SSG	18 GHz	dB		12.0
Power Added Efficiency at P1dB $V_{ds}=8V; I_{ds}=0.7 \times I_{DSS}$	PAE	18 GHz	%		45

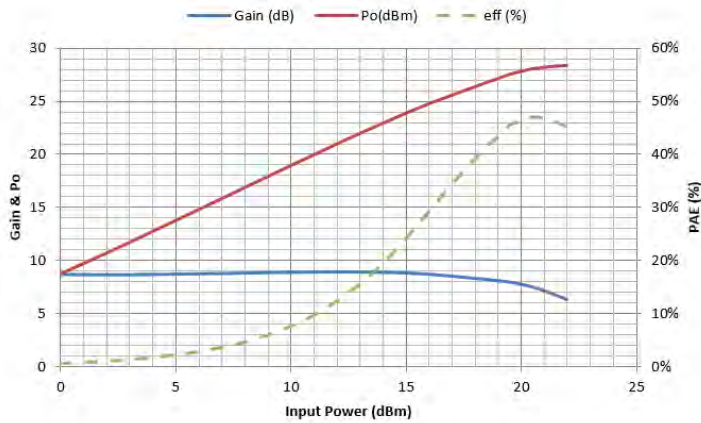
Note:  $I_{ds}$  should be between 40% and 80% of  $I_{DSS}$ . Currently, our data shows  $I_{ds}$  at 70% of  $I_{DSS}$ . Low  $I_{ds}$  will improve efficiency, but high  $I_{ds}$  will make Psat and IP3 better.

### DC Specifications: • at $T_a = 25^\circ C$

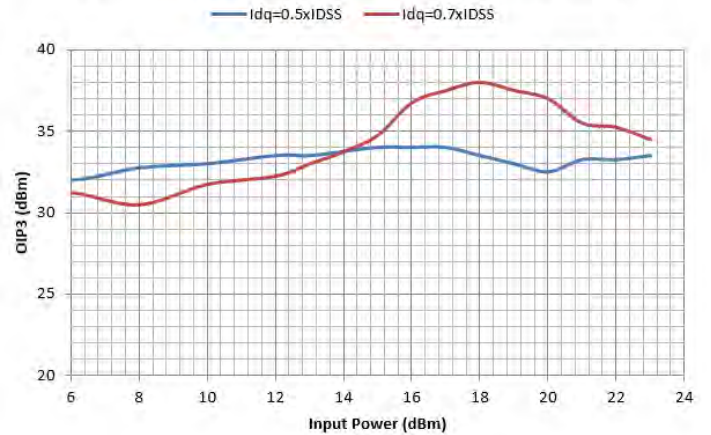
PARAMETERS & CONDITIONS	SYMBOL	UNITS	MIN	TYP	MAX
Saturated Drain Current $V_{ds}= 3.0 V; V_{gs}= 0.0 V$	$I_{DSS}$	mA	150		190
Transconductance $V_{ds}= 2.5 V; V_{gs}= 0.0 V$	$G_m$	mS		200	
Pinch-off Voltage $V_{ds}= 3.0 V; I_{ds}= 1.0 mA$	$V_p$	V		-0.8	-1.0
Gate-to-Source Breakdown Voltage $I_{gs}= -0.3 mA$	BVGSO	V		-17.0	
Gate-to-Drain Breakdown Voltage $I_{gd}= -0.3 mA$	BVGDO	V		-18.0	
Chip Thermal Resistance	$R_{th}$	C/W		150	350*

\* Overall  $R_{th}$  depends on case mounting

**MwTPH15F, Gain, Po & PAE vs Pin at 18GHz**  
**Vds=8V; Idq=0.7xIDSS**



**MwT-PH15F, OIP3 at different Idq vs Po/tone at 18GHz**

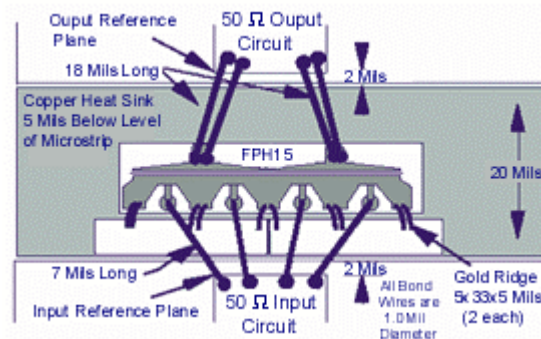


**MwT-PH15F, Load Power Data, Vds=8V, Idq=0.7xIdss**

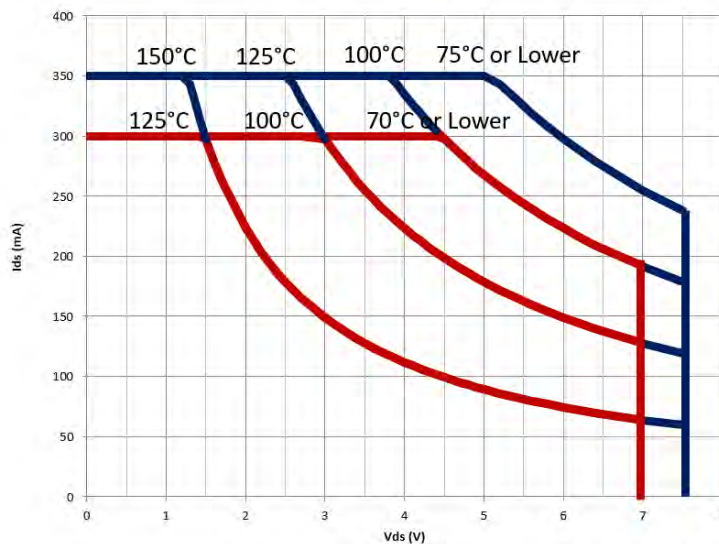
Freq (GHz)	Zs		ZL		P <sub>sat</sub> (dBm)
	Mag	phase	mag	phase	
2	0.60	80.0	0.09	173.3	28.4
4	0.70	120.0	0.19	136.2	28.1
6	0.75	140.0	0.19	143.3	28.4
8	0.87	145.0	0.25	131.7	28.2
10	0.84	160.0	0.29	127.4	28.1
12	0.87	158.0	0.29	131.3	28.5

The load pull data is based on nonlinear model provided by the foundry that processes the device.

### MwT-PH15F DUAL BIAS



SAFE OPERATING LIMITS vs BACKSIDE TEMPERATURE  
MwT-PH15F Chip and 71 Pkg



### MAXIMUM RATINGS AT Ta = 25 °C

Symbol	Parameter	Units	Cont Max1	Absolute Max2
<b>VDS</b>	Drain to Source Volt.	V	7.5	8.0
<b>Tch</b>	Channel Temperature	°C	+150	+175
<b>Tst</b>	Storage Temperature	°C	-65 to +150	+175
<b>Pin</b>	RF Input Power	mW	200	300
<b>Pt</b>	Total Power Dissipation	mW	1900	2300

**Notes:**

1. Exceeding any one of these limits in continuous operation may reduce the mean-time-to-failure below the design goal.
2. Exceeding any one of these limits may cause permanent damage.